PNSensor

There is never enough dynamic range - DEPFET active pixel sensors with analog signal compression

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Abstract

In recent years, the continuous exploration of accelerator-based X-ray sources has led to the development of what is now the 4th generation: so-called free electron lasers (FELs). FELs provide coherent, extremely intense and ultra-short X-ray flashes that bring completely new experimental opportunities to various fields of research including material science, chemistry, biology and physics.
Within the DSSC project, a new DEPFET active pixel sensor is being developed. It is dedicated to X-ray imaging at the European X-ray free electron laser facility currently under construction in Hamburg. In order to resolve the enormous contrasts occurring in FEL experiments, this new DSSC-DEPFET sensor is designed for nonlinear amplification, that is, high gain for low intensities in order to obtain single-photon detection capability, and reduced gain for high intensities to achieve high dynamic range for several thousand photons per pixel and frame.
This thesis addresses all crucial aspects of the DSSC-DEPFET development, including the fabrication process of the sensor as well as the experimental characterization of the first prototypes with respect to their amplification properties. In particular, experiments have been done on the impact of different layouts and changing operating conditions on the detector response. Moreover, a new internal charge injection mechanism will be presented which allows for fast, in-situ, pixel-wise calibration of the nonlinear detector response for large arrays of DSSC-DEPFET pixels. In addition to the measurement results, 2D and 3D device simulations allow for a better understanding of the complex physical processes during the operation of the DEPFET.
Finally, the findings of this thesis will form the basis for identifying the optimization potentials of DSSC prototypes as well as for presenting the expected performance of the next generation of DSSC-DEPFET devices.

Zusammenfassung

In den letzten Jahren führte die kontinuierliche Weiterentwicklung der beschleunigerbasierten Röntgenlichtquellen zur vierten und neuesten Generation, den sogenannten Freien-Elektronen-Lasern (FEL). Die FELs erzeugen kohärente, extrem intensive und ultrakurze Röntgenblitze, die völlig neue experimentelle Möglichkeiten in verschiedensten Bereichen der Wissenschaft, unter anderem in den Materialwissenschaften, der Chemie, der Biologie und der Physik, eröffnen werden.
Im Rahmen des DSSC Projekts wird für den europäischen XFEL, der derzeit in Hamburg gebaut wird, ein neuartiger aktiver DEPFET Pixelsensor zur bildgebenden Messung von Röntgenstrahlung entwickelt. Um die enormen Kontraste, die bei FEL Experimenten auftreten, überhaupt auflösen zu können, soll der neuartige DSSC-DEPFET Sensor eine nichtlineare Verstärkung aufweisen. Dabei soll eine hohe Verstärkung für kleine Signale den Nachweis einzelner niederenergetischer Photonen ermöglichen und eine reduzierte Verstärkung für große Signale den dynamischen Bereich auf mehrere Tausend Photonen pro Pixel und Bild erweitern.
Die folgende Arbeit befasst sich mit allen relevanten Aspekten der DSSC Sensorentwicklung. Dies umfasst sowohl den Herstellungsprozess der Sensoren als auch die experimentelle Charakterisierung der ersten Prototypen hinsichtlich ihrer Verstärkungseigenschaften. Insbesondere werden die Auswirkungen von Layout-Variationen und wechselnden Betriebsbedingungen auf die Detektorantwort untersucht. Darüber hinaus wird ein neuer Mechanismus einer internen Ladungsinjektion vorgestellt, die eine schnelle und pixelweise in-situ Kalibrierung der nichtlinearen Verstärkungskurve für große Arrays von DEPFET Pixeln ermöglicht. Neben den Messergebnissen werden 2D und 3D Bauelementesimulationen vorgestellt, die ein besseres Verständnis der beteiligten physikalischen Prozesse während des Betriebs des DEPFET erlauben.
Auf Basis der gezeigten Untersuchungen werden schließlich Optimierungspotenziale aufgezeigt und die zu erwartenden Eigenschaften der nächsten Bauelementegeneration zusammengefasst.

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1. Introduction

In history of science, hardly any technology has yielded more breakthrough developments in as many disciplines as microscopy. Progress in fields from biology, medicine and physics to electronics, pharmaceuticals and materials research still depends on microscopy. Within the discipline of light microscopy, a number of other techniques have been developed to investigate matter using electromagnetic waves. In order to explore ever-smaller structures, the wavelength of the light had to become constantly shorter. Nowadays, for example, routinely hard X-rays with wavelengths of less than 1 nm (billionths of a meter) are used to study matter. However, the smaller the objects to be examined, the more light is needed for a meaningful picture. As a result, applications have been limited due to insufficient light intensity from available X-ray sources.

In recent years "free electron laser" (FEL) technology has proven its ability to overcome the current limitations of X-ray diagnostics and thus provides a new basis for an advanced version of microscopy. Not only is the intensity of FEL light a billionfold higher than any previous X-ray experiment, but the light is also generated in ultra-short pulses so that even processes on extremely short time scales can be investigated. Similar to its predecessor, light microscopy, FEL technology will play a crucial role in the search for answers in a variety of disciplines.

The enormous potential of FEL technology has inspired the construction of numerous FEL facilities around the world. The most advanced and most powerful facility of its kind is the European X-ray free electron laser (XFEL) currently under construction in Hamburg. Starting in 2015, it will be the brightest man-made X-ray light source in the world, delivering extremely intense X-ray flashes on a femtosecond scale with a maximum repetition rate of 4.5 MHz. The light generated will have laser-like properties - it is fully coherent and highly focused. The European XFEL will provide technical capabilities for time-resolved 3D imaging of chemical and physical processes on an atomic level. For example, it will enable the "filming" of biochemical processes in individual cells, a technique that is an important basis for the development of new drugs. Equally important will be material investigations on an atomic scale, which will allow the study of catalytic processes in the chemicals industry or the development of new nanomaterials for energy storage. Apart from these examples, the European XFEL will also open new possibilities for scientific applications that have not even been considered yet.

The unprecedented properties of the European XFEL will require 2D imaging detector systems that will have to resolve the enormous contrasts occurring in FEL experiments and allow for frame rates in the MHz regime if they are to benefit from the high repetition rate of

the generated X-ray flashes. One of three 2D imaging and photon counting detector systems currently under development is the DSSC (DEPFET sensor with signal compression). It is based on a new DEPFET (depleted p-channel field effect transistor) active pixel sensor with nonlinear amplification, in other words, a high gain for small signals to obtain single-photon detection capability and a reduced gain for large signals to achieve a high dynamic range of several thousand photons per pixel and frame.

Within the framework of this thesis, first prototypes of the nonlinear DEPFET were developed and characterized in detail. The thesis contains comprehensive studies of the new device and the physical processes that occur during its operation. The newfound knowledge from measurements and simulations permits the improvement of the DEPFET and thus facilitates its optimization for application at the European XFEL.

The thesis is organized into four main chapters beginning with an introduction of free electron lasers and moving into a discussion of the special requirements for 2D photon counting detectors at the European XFEL. After a short overview of the DSSC detector system chapter three presents the basic DEPFET concept and its adaptation for FEL applications. Chapter four then represents the core of this thesis, which describes the first DEPFET prototypes with nonlinear amplification before moving on to an explanation of the test environment and the measurement procedures. After that the measurement results are presented and discussed together with device simulations. In chapter five the limitations of the prototypes are derived and the optimization potential for the next generation of nonlinear DEPFETs is evaluated.

2. The European X-ray free electron laser

The 4th and newest generation of accelerator-based X-ray sources is currently emerging on a worldwide level. With unprecedented beam intensity, these so-called free electron lasers (FELs) ring in a new era of atomic-scale X-ray diagnostics. The most powerful system of this kind is the European X-ray free electron laser (XFEL) in Hamburg and Schleswig-Holstein. It is currently under construction, but starting 2015 it will deliver ultra-short and extremely bright X-ray flashes for scientific operations. This chapter will briefly introduce the functional principle of the XFEL and give two examples of the new experimental possibilities for international and interdisciplinary researchers. We will then look at the requirements of the European XFEL for 2D imaging and photon counting detector systems before presenting the proposed DSSC detector system concept whose sensor development is the core of this thesis.

2.1. Working principle of free electron lasers

Radiation from a free electron laser (FEL) has much in common with radiation from conventional lasers: high output power, narrow bandwidth and spatial coherence. In a conventional laser, light is generated by the transition of exited electrons between bound atomic or molecular states in an active medium that is either a solid, a liquid or a gas.

In a free electron laser, the function of the active medium is taken over by unbound electrons moving freely in a vacuum within a relativistic electron beam. Figure 2.1 shows the basic structure of a high-gain single-pass SASE (self-amplified spontaneous emission) FEL. Initially, an electron gun generates free electrons that are subsequently accelerated to relativistic velocities within a linear accelerator. The light generation takes place in a so-called undulator, which is a linear sequence of dipole magnets with alternating north-south orientation. While traveling through the undulator, the electrons are deflected by the Lorentz force transverse to their main propagation (z-direction) and to the magnetic field (y-direction). Due to the periodic structure of the undulator, the electrons are forced on a sinusoidal path in the x-z plane and the acceleration of the electrons leads to the emission of synchrotron radiation in a narrow, forward-directed cone.

Like for a bending magnet, the half opening angle ϕ of the wavelength integrated radiation cone in small angle approximation is given by

$$\phi \approx \frac{1}{\gamma} = \frac{m_e c^2}{E_e} \tag{2.1}$$

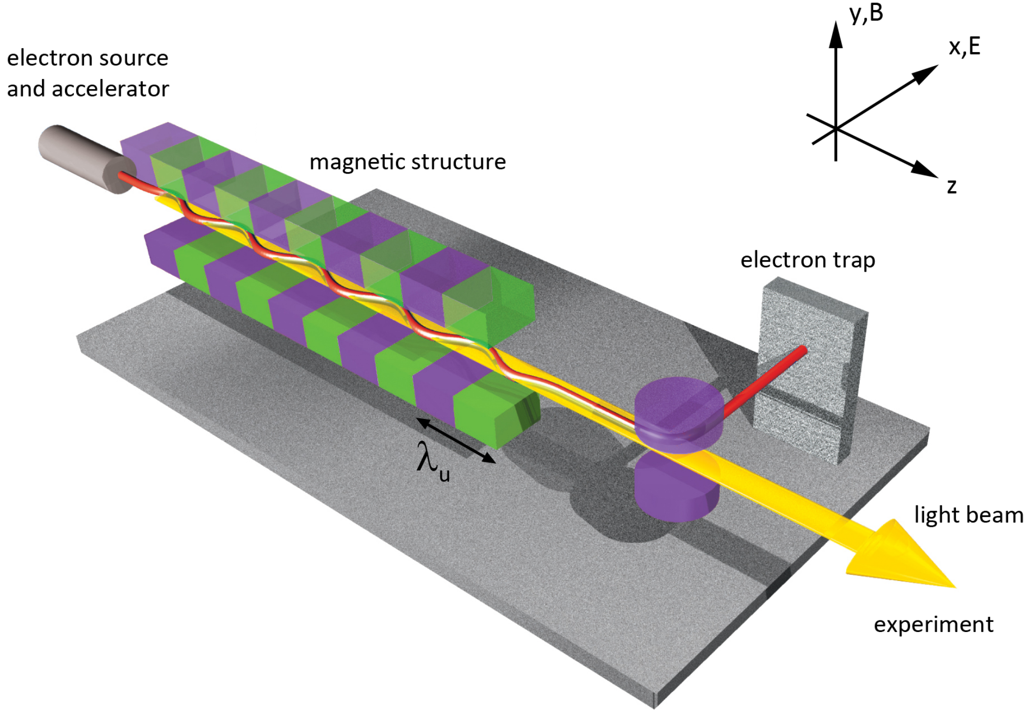

Figure 2.1: *Sketch of high-gain SASE FEL based on a single pass of the electron beam through a very long undulator. An electron bunch is accelerated to relativistic energies and passes the magnetic structure of the undulator where the radiation is generated. Afterward, the electron beam is dumped and the light beam goes to the experimental station [1].*

with $\gamma = \frac{1}{\sqrt{1-(\frac{v}{c})^2}}$ as the relativistic Lorentz factor, m_e as the electron mass, c as the speed of light, and E_e as the kinetic energy of the electrons [2].

To characterize the emission of the magnetic structure it is useful to introduce the dimensionless parameter K, which is given by the ratio between the maximum angular deviation of the electron beam from the forward direction δ and the opening angle of the emission cone ϕ. K can be expressed as

$$K = \frac{\delta}{\phi} = 0.934 \cdot B_0[T] \cdot \lambda_u[cm] \tag{2.2}$$

where λ_u is the length of the undulator period and B is the r.m.s. magnetic field strength in the undulator. While $K \geq 1$ applies for Wigglers, in the case of an undulator the maximum angular deviation from the forward direction is smaller than the opening angle of the emission cone and thus $K < 1$ [3]. This basically means that the radiation generated by the electrons overlaps with the electron beam during propagation through the individual magnetic periods of the undulator. Due to their wave-like trajectory, the electrons have a velocity component in parallel to the electric field, enabling the interaction between the electromagnetic wave and the electrons. This interaction forms the basis for the functional principle of free electron lasers.

In the case of an existing light wave, the interaction allows the energy exchange between the electrons and the wave according to

$$\frac{dE_e}{dt} = -e\vec{v} \cdot \vec{F} = -e \cdot v_x \cdot F_x \tag{2.3}$$

where E_e is the electron energy, $\vec{v}$ is the velocity vector of the electron, $\vec{F}$ is the electric field vector, and v_x and F_x are the respective components transverse to the main propagation and the magnetic field [4]. The equation indicates that electrons in phase with the electromagnetic wave are decelerated while electrons with a velocity anti-parallel to the electric field vector gain energy from the wave (compare Figure 2.2 (a)).

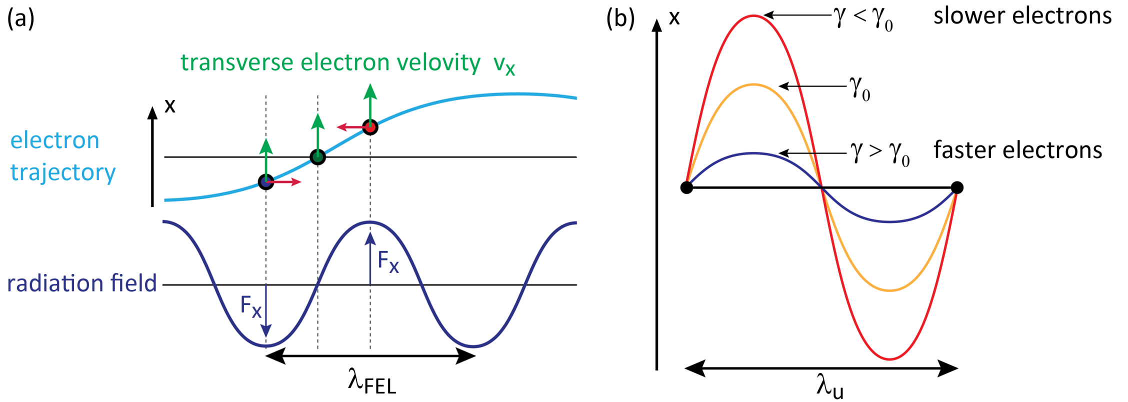

Figure 2.2: *(a) Illustration of the interaction between the electromagnetic wave and electrons. Electrons that are in phase with the electric field are decelerated, while electrons out of phase are accelerated. The resulting energy spread leads to dispersion induced by the magnetic field of the undulator (b). Faster electrons move on a shorter trajectory than slower electrons.*

As a result, the magnetic field of the undulator acts as a dispersive medium (b). The faster electrons that have been accelerated propagate on a shorter path due to their enhanced magnetic rigidity whereas the slower electrons are forced onto a longer path through the undulator. The energy exchange between the electron bunch and the electromagnetic wave combined with the dispersion due to the magnetic field results in the longitudinal modulation of the electron density within the bunch. This process is called 'microbunching': electrons are concentrated into slices located at the points where the electric field strength is zero. Since the slices are much shorter than the wavelength of the undulator radiation, they behave like a single particle with a high charge, which means they radiate coherently. In order to maintain the process of microbunching, a fixed phase relationship between the wave and the electron bunch is required. However, the light wave moves faster than the electrons since the electrons have a rest mass and move on a wiggly line. The only way out is that the light wave shifts exactly by one wavelength with respect to the electron bunch whenever the electrons move forward by a single undulator period.

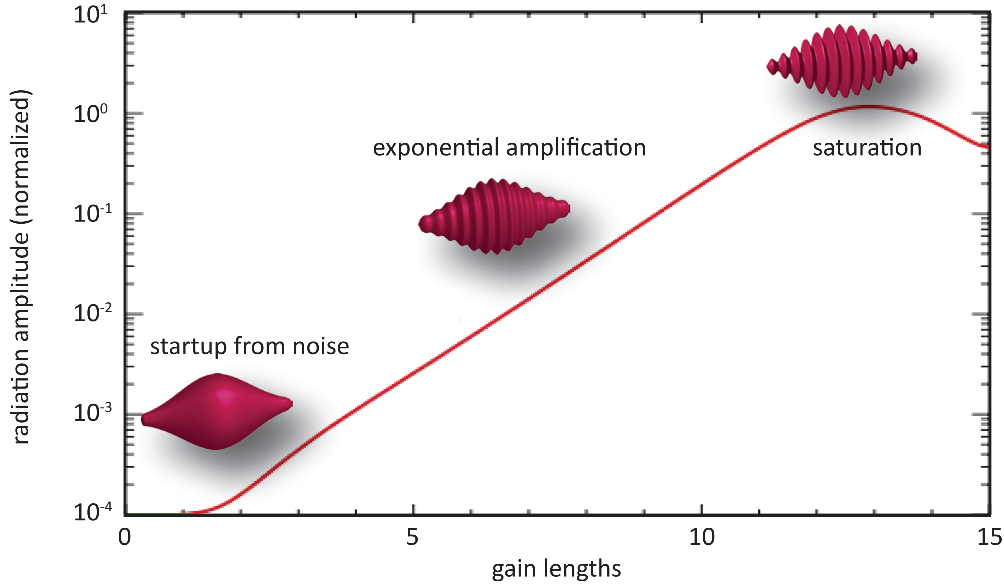

Figure 2.3: *Amplification of FEL radiation as a function of the distance within the undulator. The red cartoon illustrates the electron bunch at various positions. The radiation amplitude starts out from noise emitted by a randomly distributed electron bunch. Through the interaction with the electromagnetic wave, the electron bunch is microbunched, which leads to increased radiation emission and to exponential amplification. When microbunching reaches its equilibrium, the radiation amplitude saturates. If the electron bunch continues propagating in the undulator the field starts to transfer energy back into the electron bunch and the radiation amplitude starts to oscillate [5].*

On the undulator axis this so-called interference condition is only met for a radiation wavelength of

$$\lambda_{FEL} = \frac{\lambda_u}{2\gamma^2}\left(1 + \frac{K^2}{2}\right). \tag{2.4}$$

with λ_u as the length of the undulator period, γ as the relativistic Lorentz factor, and K as the undulator parameter [4]. Although the emitted synchrotron radiation is white, the constructive interference is only given for λ_{FEL} and higher harmonics. If the interference condition is fulfilled, the electrons emit light at different points of the undulator in phase with the actual present light wave. One of the main advantages of this coherent radiation is the significantly higher brilliance compared to incoherent sources. The intensity for coherent emission scales quadratically with the number of electrons (N_e), whereas for spontaneous radiation it scales only linearly with N_e. Therefore, the light emission strongly enhances the electric field strength in the undulator and in turn intensifies microbunching. This self-amplifying process leads to an exponential increase of the radiation amplitude with the undulator length, as it is shown in Figure 2.3.

At the beginning of the undulator there is no electromagnetic wave that can be amplified and the radiation power stays almost constant. The spontaneous emission of synchrotron

radiation within the first section of the undulator acts as a seed radiation for the FEL process. Once an initial wave is present, the self-organizing process of the electrons in the undulator leads to an exponential growth of the pulse energy with the undulator length. When the electron distribution has reached its equilibrium and microbunching cannot become more pronounced due to the electrostatic repulsion of the electrons, the radiation amplitude reaches saturation. In the case of further propagation of the electron bunch in the undulator, the field starts to transfer energy back into the electron bunch and the radiation pulse energy starts to decrease again.

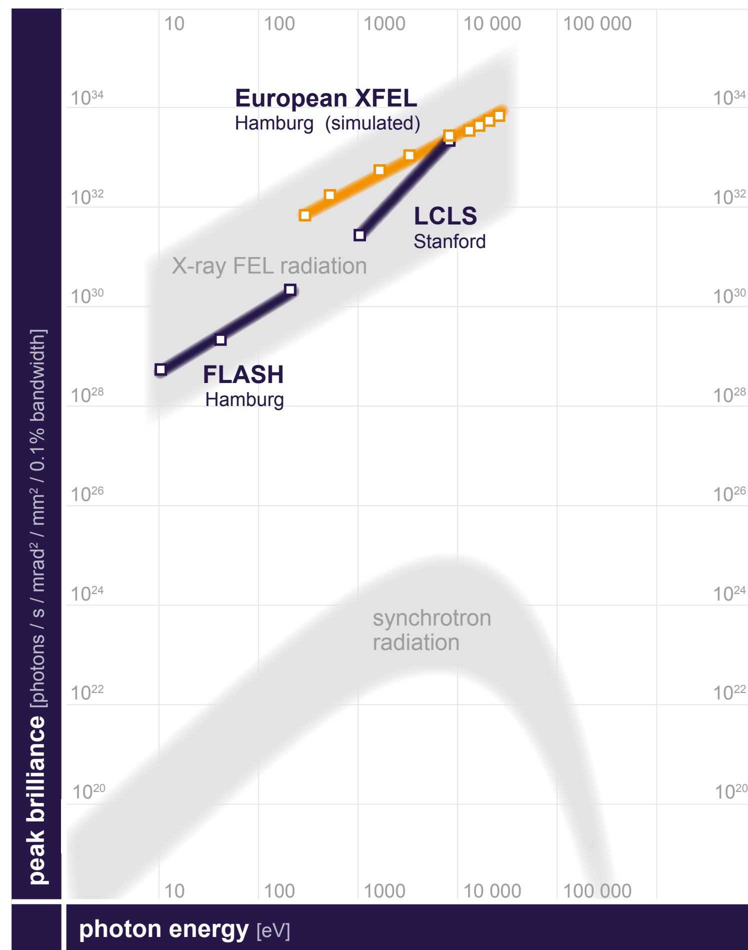

Figure 2.4: *The peak brilliance of free electron lasers exceeds that of most modern synchrotron radiation by many orders of magnitude. Starting in 2015, the European XFEL will be the brightest X-ray light source in the world [1].*

For a high-gain SASE FEL, saturation has to be achieved within a single pass. This demands not only very long undulators of several hundred meters but also a very high electron beam quality in order to maximize the overlap of the electrons with the emitted radiation and thus to achieve an increase in speed of microbunching. The required compression of the electrons into ultra-short bunches in the order of μm allows the generation of light pulses in the fs range.

The startup of the FEL process from noise without the need for any external seed radiation is called SASE (self-amplified spontaneous emission). It permits the startup at arbitrary wavelengths without the need for external seed radiation. Furthermore, an SASE FEL provides full amplification in a single pass and does not require an optical cavity with highly reflective mirrors. This extends the energy range of FELs into the X-ray realm and allows the radiation wavelength to be tuned by simply adjusting the energy of the electron beam (compare equation 2.4). As illustrated in Figure 2.4, the peak brilliance of FEL radiation is a billion times higher than for conventional synchrotron X-ray sources and the European XFEL will be the most powerful facility of its kind. It will provide ultra-short X-ray flashes with a typical duration of less than 100 fs with full lateral coherence. These unique and unprecedented properties of X-ray radiation will open up new experimental possibilities that will be briefly introduced in the following section.

2.2. New Opportunities at the FELs

A typical experiment performed at FEL facilities is illustrated in a simplified sketch in Figure 2.5.

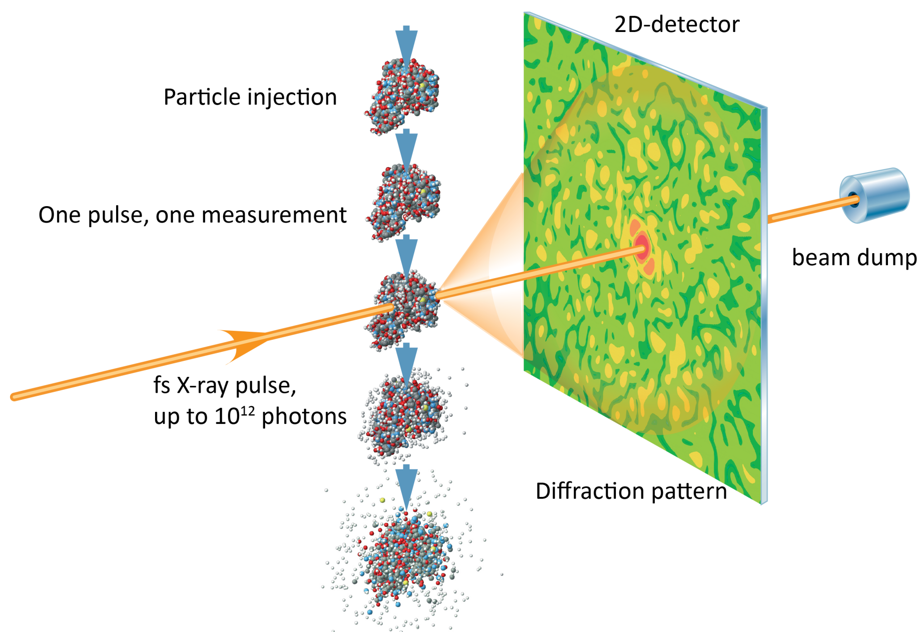

Figure 2.5: *Simplified sketch of an X-ray scattering experiment. A scattering target is injected into the photon beam and the diffraction pattern is recorded by a 2D imaging detector [1].*

The intense photon beam generated in the undulator is aligned to go through a central hole of a 2D imaging detector and is dumped by a beam stop behind. Whenever a target, like a molecule or a small nanocrystal, is brought into the photon beam, the X-rays are scattered and cause a diffraction pattern, which is recorded by the 2D detector. Using

dedicated analysis algorithms, the atomic structure of the target can then be calculated from the measured intensity distribution.

In principle, this is comparable to experiments performed for many years now at synchrotrons all around the world. However, the unprecedented properties of the FEL light open up a completely new class of experiments. In particular, it is the tremendous peak brilliance and the ultra-short, coherent light pulses that provide new opportunities previously inaccessible to accelerator based X-ray sources. Below, two experiments will be presented that convey an impression of the revolutionary potential of free electron lasers.

2.2.1. Imaging of biological samples

Analyzing the structure of molecules using scattering experiments is a standard application at conventional synchrotrons. In order to determine the molecular structure of the target, the recorded diffraction patterns need to provide sufficient statistics. This requires either long exposure time or crystalline samples that offer a large number of identical specimens. However, both approaches have significant limitations. On the one hand, many samples cannot be crystallized and thus only exist as an individual molecule. On the other hand, exposure times cannot be extended, especially for biological samples, because the radiation damage would lead to the degradation or even destruction of the target before the diffraction pattern is acquired. By using the ultra-short X-ray flashes of free electron lasers with a

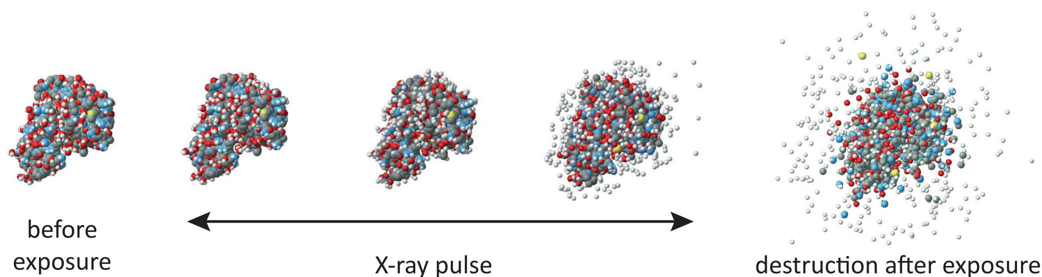

Figure 2.6: *Illustration of a molecule during a scattering experiment at a free electron laser facility. The molecule is injected and irradiated with an ultra-short X-ray flash. It hardly changes during exposure but is destroyed afterward due to the high energy deposition of the light pulse within the sample.*

typical duration of less than 100 fs, the issue of radiation damage can be mitigated since the timescale for most damaging mechanisms is much longer [6, 7]. As illustrated in Figure 2.6, the duration of the flashes is so short that the molecule hardly changes during the exposure. Only after the X-ray flash has passed, the target molecule does start to turn into plasma due to the enormous energy deposition of the intense light pulse [8]. Due to the extremely high peak brilliance of the FEL, each individual flash provides enough photons to record a full analyzable diffraction pattern. The coherence and the short wavelength further allow for holographic imaging with atomic resolution. The applicability of ultra-short X-ray flashes for structure analysis has already been shown for nanocrystals of Photosystem I,

one of the largest membrane protein complexes [8], as well as for a single mimivirus, one of the largest known viruses [9].
For these reasons, free electron lasers offer unique capabilities for the structural analysis of large and difficult-to-grow molecules that are sensitive to irradiation. This will surely open up new fields of research, one of which could be the human cell membrane proteins, one of the most important drug targets in the human body. The knowledge of their atomic structure would be a milestone for pharmaceutical research as the active substances in new medicines could be tailored to suit recipients, which would increase their effectiveness and reduce adverse effects.

2.2.2. Filming chemical reactions with atomic resolution

Besides the capability of taking snapshots of large molecules before they explode, the ultra-short light flashes of FELs will also enable researchers to resolve the transient behavior of molecules during chemical reactions by using pump-and-probe experiments.

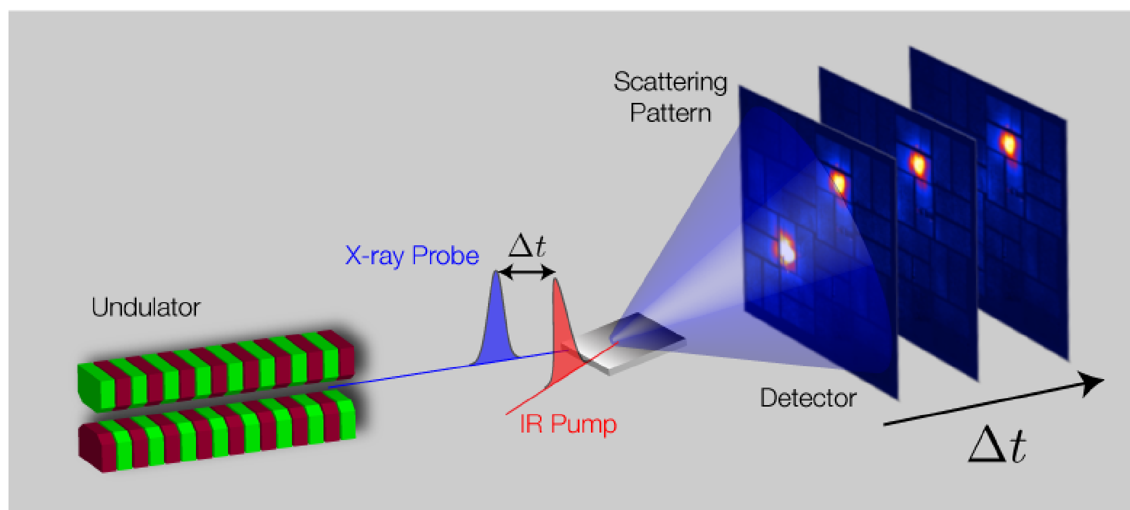

Figure 2.7: *Sketch of a typical pump-probe setup for ultra-fast measurements. An optical or IR pump excites a process and the dynamics of the sample are then observed by a time-delayed X-ray pulse of the FEL. The combination of measurements at varying delays Δt allows for the reconstruction of the dynamics in a stroboscopic fashion [10].*

Such an experiment typically consists of two individual light pulses. Initially a reaction is started with an optical or an infrared laser pulse before it is probed by the femtosecond X-ray pulse of the FEL. Alternatively, the X-ray pulse is split in two to act as both pump and probe [11]. Even if the probe pulse of the FEL leads to the destruction of the target, repeating the experiment with different time intervals between the trigger and the probe pulse allows you to monitor the state of the system as a function of time after the reaction has been initiated. The temporal resolution of this technique is given by the duration of the X-ray pulse and the jitter between the pump and the probe. By using

pump-and-probe experiments, movies of molecular reactions can be recorded with atomic resolution allowing researchers to follow the motion of atoms within molecules as well as the progress of chemical reactions, all in real time. This will lead to a better understanding of the dynamics of chemical processes, which is essential for many fields of research, for example in chemistry, where it will help improve catalytic converters and thus develop more efficient industrial production processes, or in biology where the knowledge gained will provide an essential basis for the development of new medicines.

2.3. Detector requirements of the European XFEL

In order to benefit from the exceptional properties of the European XFEL, new detector systems are required. The key requirements for future detector systems will be discussed in the following section.

2.3.1. Single-photon resolution and high dynamic range

Free electron lasers, and in particular the European XFEL, are single-shot machines. The high brilliance of their light flashes enables researchers to decipher the atomic structure of molecules using diffraction patterns obtained from single flashes of light. This capability is directly connected with enormous contrast on the diffraction patterns. Depending on the target there will be areas on the detector that will be hit by several thousand photons, whereas other areas see only a few or none at all. The new detector systems therefore have to provide a very high dynamic range in order to resolve these extreme differences in brightness.

Apart from the high dynamic range, future detector systems should also provide single-photon detection capability up to some tens of photons. This allows the observation of higher scattering orders and thus increases the precision of the reconstruction algorithms. In addition, it allows us to precisely determine the X-ray background that results from scattering processes either on residual gas in the vacuum tank or on the liquid jet, which is used to bring the sample molecules into the photon beam. In pump-and-probe experiments, stray light from optical pump lasers can also cause additional background. The knowledge of this background is crucial for data analysis.

For higher numbers of photons per pixel and frame, the necessity of single-photon counting is only limited because both photon generation in the undulator as well as the scattering process underlie Poisson statistics. As a result, higher measurement accuracy does not contain more physical information. Natural Poisson noise is given by the square root of the number of photons. For example, if an experiment delivers on average N photons per pixel and it would be possible to repeat the experiment under exactly the same conditions,

then the statistical fluctuations of the measured photon number would be

$$\Delta N = \sqrt{N}. \tag{2.5}$$

Future detector systems need to provide a dynamic range of several thousand photons per pixel and frame. Independent of the number of registered photons the measurement accuracy should always be better than the statistical fluctuation due to the Poisson noise.

2.3.2. Readout speed

In contrast to the single-photon detection capability and the large dynamic range that are common requirements of all free electron laser facilities, the European XFEL has significantly higher demand in terms of readout speed. The focused beam will have such a high photon density that the sample under study will not survive a single shot. Thus, every X-ray flash has to be treated as a separate experiment and the complete X-ray diffraction pattern from each pulse has to be recorded separately. The European XFEL provides 27,000 light pulses per second, far more than any other FEL facility in the world. Due to the superconducting accelerator technology, the flashes are not equally distributed in time but in a time scheme as illustrated in Figure 2.8.

The X-ray flashes are generated in so-called bunch trains of 600 μs length and a

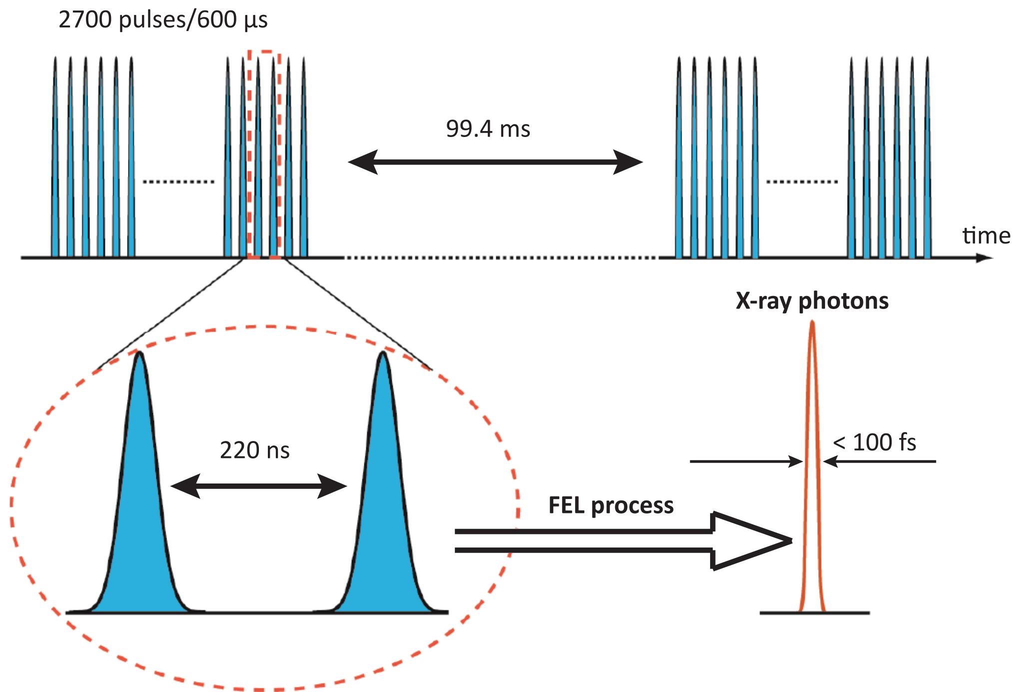

Figure 2.8: *X-ray bunch structure at the European XFEL. The XFEL machine generates bunch trains with a repetition rate of 10 Hz. Every bunch train is composed of 2,700 X-ray pulses with a temporal distance of 220 ns corresponding to a maximum repetition rate of 4.5 MHz*

repetition rate of 10 Hz. Each bunch train consists of 2,700 X-ray flashes with a temporal spacing of 220 ns. The 99.4 ms long gap between the bunch trains is required to cool the superconducting cavities in order to keep them below the superconducting transition temperature and thus to guarantee stable operation of the facility. To take advantage of the high repetition rate of the European XFEL within the bunch trains, detectors have to be able to process a full image within the 220 ns between two flashes. The only way to achieve the corresponding frame rate of 4.5 MHz for large-area 2D imaging detectors with one million pixels is to implement a full parallel readout of all pixels simultaneously.

2.3.3. Radiation hardness

In the radiation environment of free electron lasers, radiation tolerance is another major challenge for silicon-based 2D imaging detector systems. At this point, the expected radiation dose at the European XFEL cannot be derived from experimental data since the facility is still under construction. However, based on the following assumptions, H. Graafsma [12] has set up a worst-case assessment of the expected radiation dose:

- Performing constantly, a very harmful experiment with $5 \cdot 10^4$ photons per pulse and per 200 x 200 μm^2 pixel
- 1,250 hours of data acquisition per year for a single detector system
- 15,000 X-ray pulses per second (less than 27,000 per second due to electron beam dump limitations)

This scenario delivers $6.75 \cdot 10^{10}$ pulses and $3.4 \cdot 10^{15}$ photons for the hottest pixels per year and thus roughly $1 \cdot 10^{16}$ photons within a three-year operation. For 12 keV photons and a 500 μm thick silicon sensor, this corresponds to a total absorbed dose of 1 Giga Gray. It has to be pointed out that, even for the billionfold higher peak brilliance of the FELs, the time-integrated photon flux is comparable to 3rd generation storage rings. The calculation is certainly the upper limit of any radiation dose that can be expected and the total integrated dose might well be much lower. However, because they are strongly dependent on the experiments performed and the energy of the photons, no precise values can be given. The detectors should therefore be designed as radiation hard as possible to mitigate the restriction of the detector systems for certain kinds of experiments.

2.4. DSSC detector system

In addition to the LPD (**L**arge **P**ixel **D**etector) [13] and the AGIPD (**A**daptive **G**ain **I**ntegrating **P**ixel **D**etector) [14], the DSSC (**DEPFET** **S**ensor with **S**ignal **C**ompression) detector system is one of the three integrating and X-ray imaging detector systems currently under development for the use at the European XFEL. The DSSC will be a large-area detector system for high-speed photon counting with a focus on the low end of the XFEL's

energy range. Some of its main design parameters are listed in Table 2.1.

Energy range	0.5...25 keV (optimized for 0.5...6 keV)
Number of pixels	1,024 x 1,024
Sensor pixel shape	hexagonal
Sensor pixel pitch	204 μm x 236 μm
Dynamic range	>10,000 photons/pixel/pulse
Resolution	Single photon @ 1 keV (4.5 MHz)
Frame rate	up to 4.5 MHz
Stored frames per bunch train	>640
Operating sensor temperature	-20°C optimum, RT possible

Table 2.1: *Overview of design goals of DSSC detector system.*

The full DSSC camera head [15, 16] will be equipped with 1,024 x 1,024 hexagonal pixels covering a sensitive area of roughly 24 x 25 cm^2. Yet these impressive dimensions should not obscure the high degree of integration and the complexity of the system.
As indicated in Figure 2.9, the DSSC is subdivided into four equal, independent quadrants each having 512 x 512 pixels. The quadrants are arranged around a central hole, which is adjustable in size to let the direct, unscattered X-ray beam pass through. Each quadrant is again composed of four "ladder" modules, the smallest exchangeable detector unit, with a format of 128 x 512 pixels. A ladder comprises two identical sensor chips each with 128 x 256 pixels. To maintain the ladder module's four-side buttability, all mechanical, thermal, power and signal connections are implemented orthogonally to the sensor surface [17]. The dead area caused by sensor chip edges and gaps between ladders and quadrants is approximately 15%.
The modular design of the DSSC detector leads to a much higher yield of the sensor production and the module assembly process, which in turn guarantees the use of only flawless ladder modules. It also makes it possible to easily exchange individual ladders and thus replace certain regions of the detector that may be damaged or degraded due to the hostile radiation environment at the XFEL facility. In the future, this modular design will permit even further scalability of the detector area. That will enable either the registration of higher scattering orders or, in the case of greater distances between the detector and the interaction point, improved spatial resolution. Both options may even enhance the accuracy of structural analyses for irradiated targets, but a further enlargement of the detector system is not foreseen at the present time.
Figure 2.10 shows a simplified block diagram of the DSSC concept. It is based on a new DEPFET active pixel sensor that offers signal compression on the sensor level, fully parallel readout [18] and immediate digitization within the pixel footprint in order to achieve frame rates in the MHz range. Each DEPFET sensor chip (128 x 256 pixels) is connected by bump bonds to eight pixelated mixed-signal readout ASICs (**a**pplication

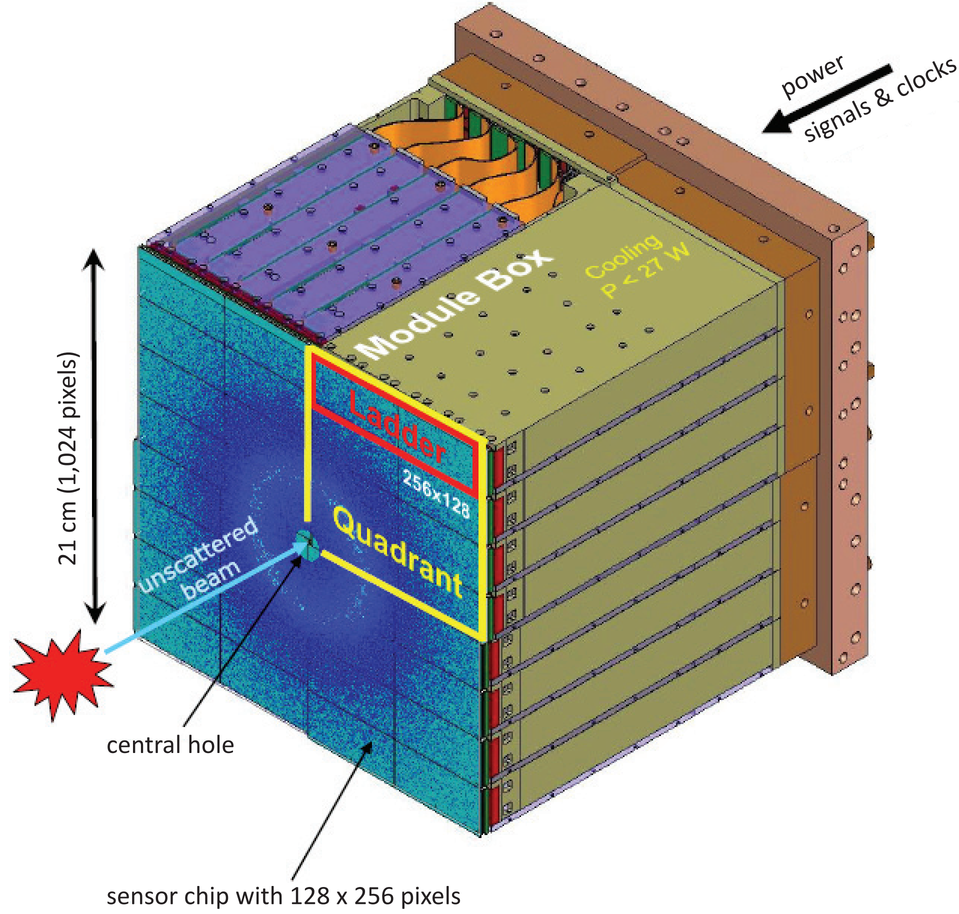

Figure 2.9: *3D view of the full DSSC camera head (1,024 x 1,024 pixels) composed of four quadrants. Each quadrant consists of four ladders and eight monolithic sensors of 128 x 256 pixels each. Due to the geometric arrangement of the quadrants, a central hole is maintained to let the unscattered beam pass through. All power and signal lines go to the rear of the camera head.*

specific **i**ntegrated **c**ircuit) with a format of 64 x 64 pixels. The bump bonding technology enables the 3D integration of DEPFETs and permits the connection of each sensor pixel with its own readout pixel due to the small pitch of only 200 μm and the associated high bump density. For this purpose, a new 64 x 64 readout chip was developed as part of the DSSC project [19]. Each of its 4,096 readout pixels contains the full signal processing chain including a current-to-voltage conversion preamplifier, an analog filter with a trapezoidal weighting function [20], an 8-bit single-slope ADC [21, 22] and an SRAM storage with a capacity of 640 frames per bunch train [23]. The memory should provide enough capacity to store all meaningful frames of a bunch train since the DSSC detector allows the system to overwrite frames in the SRAM that do not contain useful information. For this purpose, the XFEL machine will provide an external veto signal indicating frames that can be discarded. The digital data acquired in the memory is sent off the focal plane via optical links to

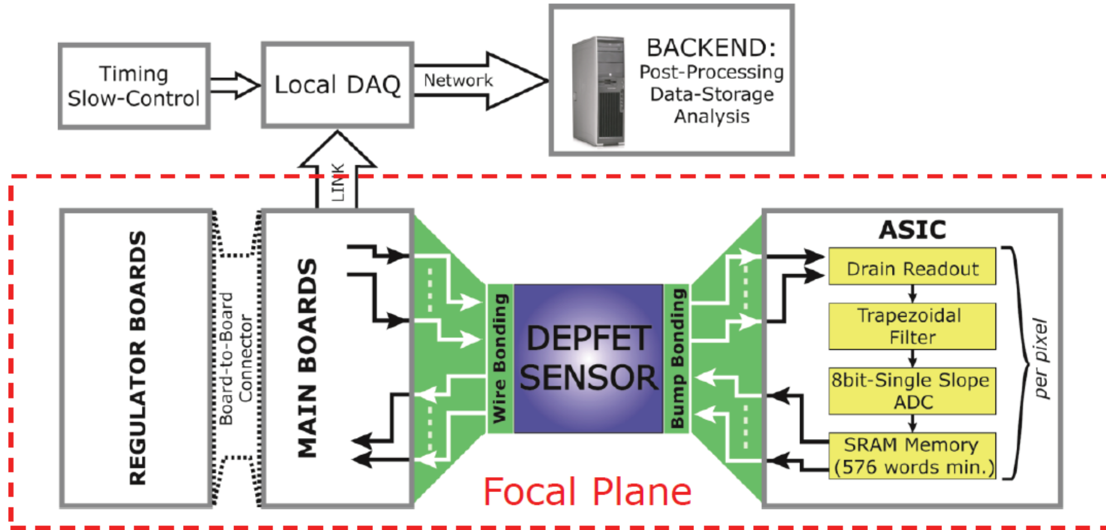

Figure 2.10: *Simplified block diagram of the DSSC detector concept. The sensor is bump bonded to a set of readout ASICs. The ASICs provide analog signal filtering, 8-bit digitization and data storage for every individual pixel.*

the local DAQ system [24] during the 99.4 ms between the bunch trains and temporarily stored there. Subsequently, the data is transferred over the network to powerful server farms for long-term storage and computation-intensive data analysis.

Figure 2.11 shows a drawing of one detector ladder module. Each module consists of a mainboard with two sensor readout chip stacks, four regulator boards and a single I/O board. On the bottom side there are two DEPFET sensor chips (128 x 256 pixels) each bump-bonded to eight readout ASICs. The backside of the ASICs is glued to a ceramic carrier, which in turn sits directly on the mainboard. The ceramic carrier acts as a heat spreader and allows for a temperature gradient over the sensors of a full ladder below 5 K at the foreseen sensor operation temperature of -20°C. All power and signal lines required for the chip stack are on the long side of the ladder by wire bonds between the mainboard and the sensor chip. In particular, this means that all ASIC connections go over the sensor chips.

The mainboard distributes the power and digital signals, and serves as a carrier for the four regulator boards and the I/O board, which are attached perpendicularly by board-to-board connectors.

The regulator boards generate the static and dynamic supply voltages for the DEPFET sensors as well as for the readout ASICs, and have additional electronic components that allow for a power cycling. The DEPFET and the readout ASICs are only active during the 600 μs long bunch trains and switched off during the 99.4 ms long cooling phase of the XFEL machine (compare Figure 2.8). This way the total power consumption within the vacuum can be reduced from a peak power of 10.7 kW down to an average of 400 W. The regulator boards also accommodate big arrays of capacitors to stabilize the static voltages

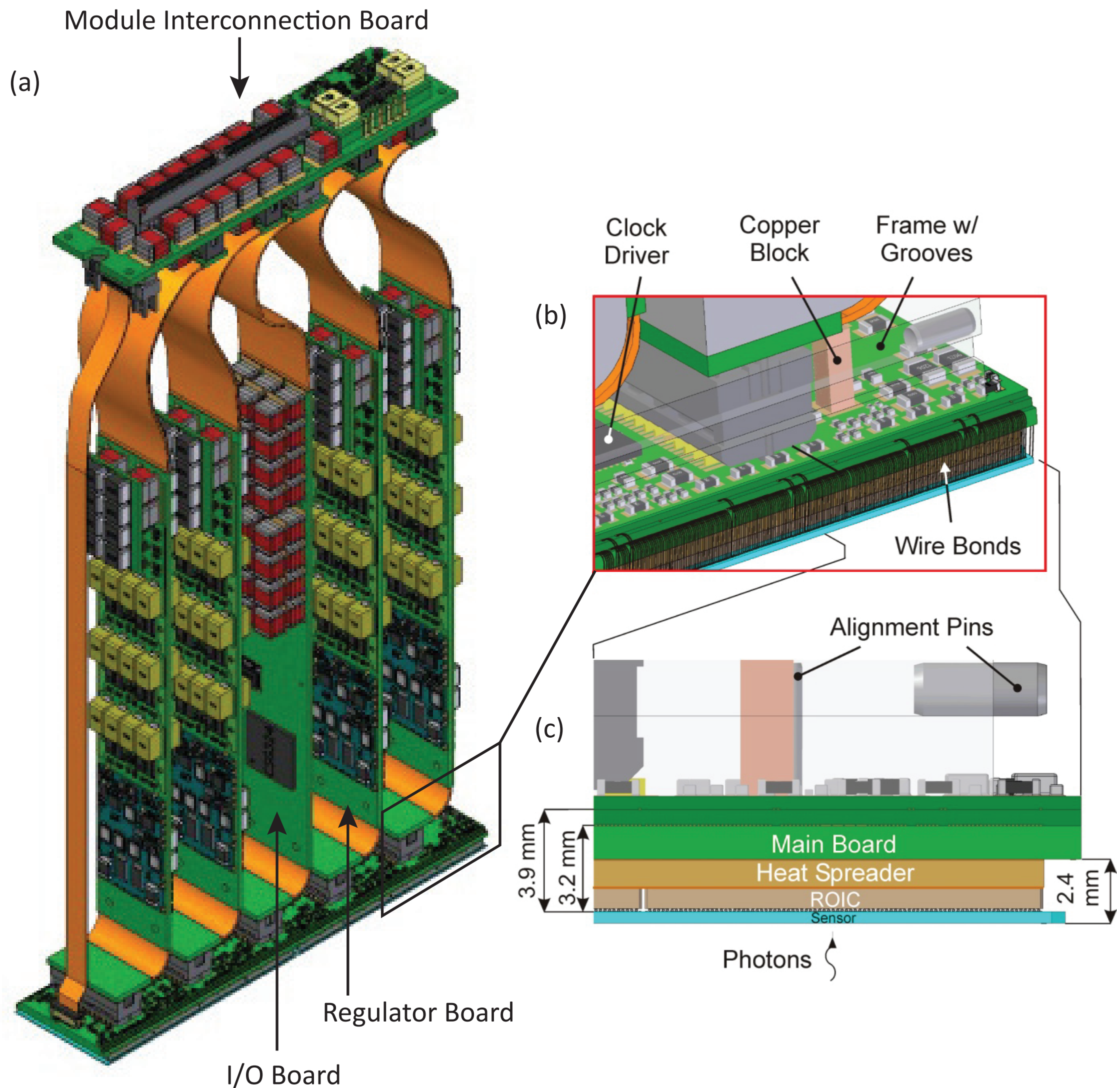

Figure 2.11: *Technical drawing of one "ladder", the smallest subunit of the DSSC detector system. Figure (a) shows the complete ladder with four regulator boards and one I/O board perpendicular to the mainboard. Figure (b) depicts a close-up side view of the mainboard with the wire bonds connecting the mainboard to the DEPFET sensor. Figure (c) illustrates the sandwich structure of the mainboard, the head spreader and the semiconductor chips.*

and to enable fast rise times of a few nanoseconds and constant amplitudes for the clocked voltages over the entire bunch train.
All the digital timing and control signals for power cycling are generated on the I/O board and provided by the module interconnection board on the top in Figure 2.11 (a). Apart from generating the steering signals for regulator boards, the main task of the I/O board is to manage the data stream from the readout ASICs to the DAQ system. It is therefore equipped with a powerful FPGA (field programmable gate array) that receives the measurement data from all 16 readout ASICs of the entire ladder and merges the data

into a single serial output data stream. This can then be transferred via optical links to the DAQ system.
The key component of the detector system is the new DSSC-DEPFET, which features nonlinear amplification and thus provides intrinsic signal compression on sensor level. Besides the DSSC, the LPD and the AGIPD are also based on a fully parallel readout of all sensor pixels in order to achieve the required frame rate of 4.5 MHz. Similar to the DSSC, this is done using bump bonds that connect a sensor chip to a dedicated readout chip. The main difference between the systems is the place and the method of signal compression, which is required to combine the single-photon resolution and the very high dynamic range of several thousand photons per pixel and frame. Both the AGIPD and the LPD have arrays of conventional pin diodes as sensors, whose linear analog output signal is compressed in the readout chip. For the LPD, the analog signal path is fed into three individual amplifier stages which simultaneously process the analog signal with different gains. The AGIPD has indeed only a single amplifier stage, but its gain can be dynamically adjusted to the respective signal level during signal processing.
By contrast, for the DSSC, signal compression for high photon numbers is already implemented on sensor level by the intrinsic properties of the new DSSC-DEPFET. The input capacitance of the DEPFET representing the first amplifier stage is much smaller than in other systems. Consequently, the electronic noise at full speed can be reduced from several hundred electrons to less than 50 electrons r.m.s. for the DSSC. It is thus the only detector system featuring single-photon resolution of low-energy X-rays of 1 keV at the full frame rate of 4.5 MHz. For this reason, the DSSC is foreseen for low energy beamlines at the European XFEL, covering the energy range between 500 eV and 6 keV.
The following chapter will introduce the DEPFET amplifier and discuss the functional principle of the newly implemented signal compression mechanism.

3. DEPFET concept

This chapter presents the basic concept of active pixel sensors based on **de**pleted **p**-channel **f**ield **e**ffect **t**ransistors (DEPFETs). However, because all semiconductor radiation detectors are based on the energy deposition in the detector material, we will first discuss the possible interactions of ionizing radiation with matter before introducing the DEPFET in detail.

3.1. Interaction of radiation with matter

Semiconductor detectors are used for the detection of photons and charged particles like electrons, protons, myons and pions. In order to be detected, these particles have to interact with the detector material. The most important interaction mechanisms of ionizing radiation with a semiconductor are illustrated in Figure 3.1.

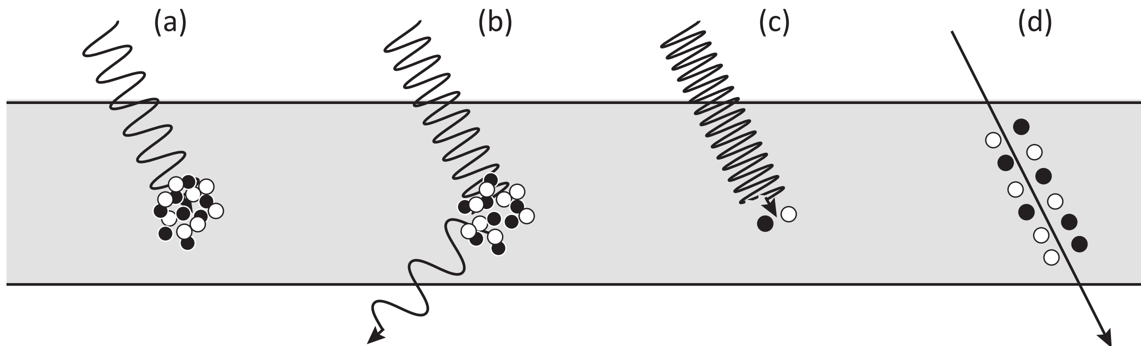

Figure 3.1: *Most important interaction mechanisms of ionizing radiation with matter: (a) photoelectric absorption, (b) Compton scattering, (c) pair production, (d) Coulomb interaction of charged particle.*

3.1.1. Electromagnetic radiation

In general, there are three different interactions for photons: photoelectric absorption, Compton scattering and pair production.

Photoelectric absorption

Photoelectric absorption describes an interaction between a photon and an absorber atom where the photon completely disappears (a). In a semiconductor the photon excites an electron over the band gap and the remaining energy goes into the kinetic energy of the

electron. The minimum required photon energy is therefore defined by the band gap of the material, which in the case of silicon is 1.12 eV corresponding to an optical photon with a maximum wavelength of 1100 nm. For higher primary photon energies, the excited electron dissipates its energy mainly by generating either phonons or additional electron-hole pairs via the Coulomb interaction with other electrons from the valence band (thermalization). Because part of the photon energy is dissipated to the crystal lattice, the average energy required to generate an additional electron-hole pair is 3.65 eV. This value can be considered as constant, but deviations occur for photon energies close to the band gap energy [25]. The statistical fluctuation of the mean number of electron-hole pairs generated is called Fano noise and limits the achievable energy resolution of semiconductor detectors.

Compton scattering

The scattering process of a photon that only transfers a part of its energy is called Compton scattering (b). After the interaction, the scattered photon with less energy and therefore a longer wavelength will continue its path until another interaction process occurs or it leaves the material. The energy lost in the scattering process is transferred to an electron. According to photoelectric absorption this excited electron will thermalize and generate additional electron-hole pairs.

Pair production

For gamma radiation, so-called pair production can occur where the photon is converted into an electron-positron pair (c). Due to momentum conservation, this effect has to take place in the Coulomb field of an atomic nucleus that is absorbing the recoil. Therefore, the minimum required photon energy is the sum of the rest energies of the electron and the positron and the kinetic energy of the recoil nucleus

$$E_\gamma = 2m_e c^2 \left(1 + \frac{m_e}{M_K}\right) \approx 1.022 \text{ MeV} \tag{3.1}$$

where m_e is the mass of the electron, M_K the mass of the recoiling nucleus and c the speed of light. Generally, m_e is much smaller than M_K and thus the second term can be neglected.
According to (a) and (b), additional energy will contribute to the kinetic energy of the electron-positron pair to create further electron-hole pairs during the thermalization process.

Cross sections

The cross sections for the discussed interaction mechanisms depend greatly on energy and materials and vary over several orders of magnitude. The following dependencies can be found in literature:

$$\Phi_{photo} \propto \frac{Z^{4..5}}{E^{-3.5}} \tag{3.2}$$

$$\Phi_{compton} \propto Z \tag{3.3}$$

$$\Phi_{pair} \propto Z^2 \cdot lnE \tag{3.4}$$

where Z is the atomic number of the detector material and E is the photon energy [25, 26]. For silicon, photoelectric absorption dominates up to energies of roughly 50 keV. In the energy range from 50 keV up to 20 MeV it is Compton scattering and for higher energies than those, pair production is the most probable interaction.

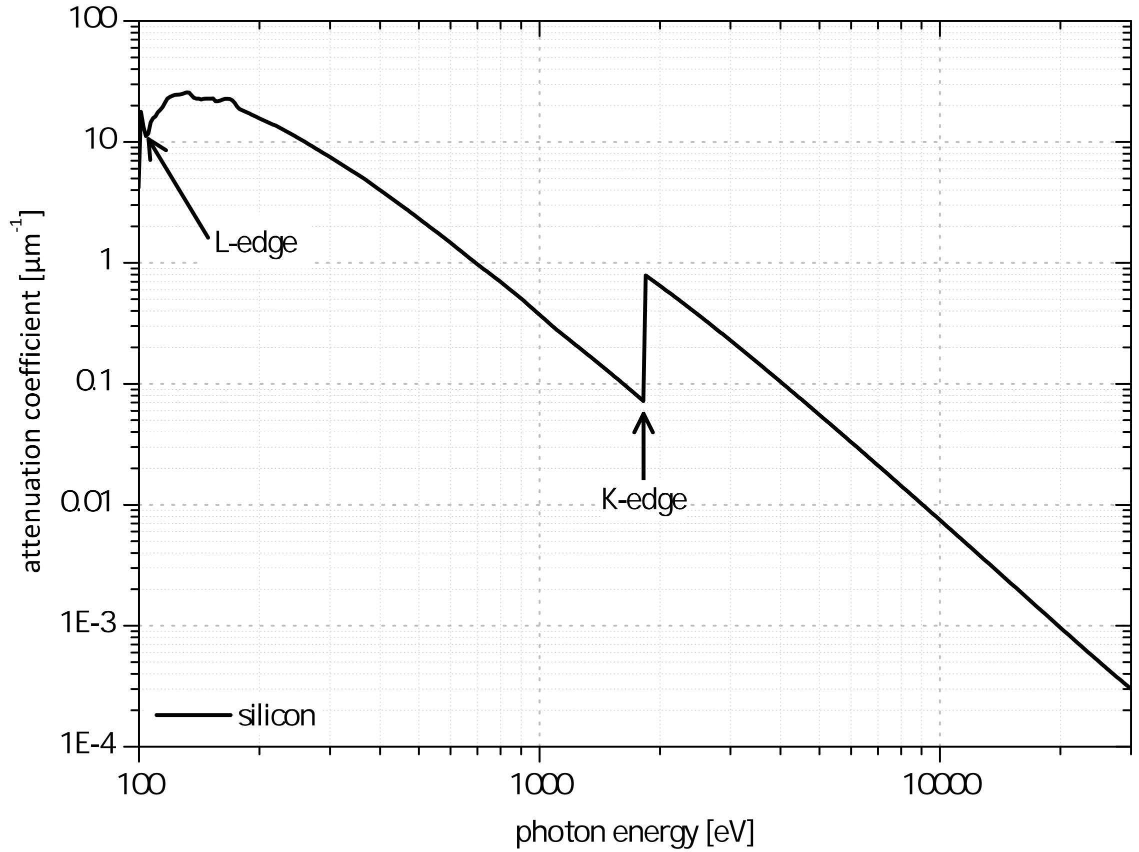

Figure 3.2: *Energy dependence of the attenuation coefficient in silicon for photons in the energy range of 100 eV and 30 keV due to the photo effect [27].*

Considering all of those mechanisms, the attenuation of electromagnetic radiation is described by the Beer-Lambert law

$$I(x) = I_0 \cdot e^{-\frac{x}{\mu}} = I_0 \cdot e^{-x \cdot \alpha} \tag{3.5}$$

where $I(x)$ is the remaining intensity after the transition of an initial intensity I_0 through an absorber material with an absorption length μ and thickness x. The reciprocal value of μ, called the attenuation coefficient α, is shown in Figure 3.2 for silicon in the energy range between 100 eV and 30 keV. The attenuation coefficient decreases as it goes from lower to higher energies. Whenever the energy is higher than the excitation energy of an atomic shell, the attenuation coefficient immediately increases. This behavior can be observed in Figure 3.2 at an energy level of 1839 eV (K-shell of silicon) which is therefore termed the silicon K-edge. For photon energies above the K-edge, α continues to decrease and hence limits the applicability of silicon detectors for the direct measurement of electromagnetic radiation since the detection probability becomes too small. For a wafer thickness of 450 μm, which is the standard thickness of silicon detectors fabricated at the Max-Planck semiconductor laboratory, a detection probability of 99 % can be achieved up to energies of 8 keV.

3.1.2. Particle radiation

Uncharged particles like neutrons interact in direct collisions with the atomic nuclei of the absorber material. This scattering process can be either elastic or inelastic. For elastic scattering, the sum of the energies of the two collision partners before and after the interaction is constant, but atoms can be kicked out of their position and ionize other atoms in their vicinity. For inelastic scattering, part of the energy goes into the excitation of an atomic nucleus, which emits a gamma quantum to return to its ground state. The gamma quantum can again interact with the material by the mechanisms discussed in chapter 3.1.1 while another possibility is neutron capture, where the neutron is absorbed by an atomic nucleus causing radioactive decay. In semiconductors, the cross sections for the described interactions are very small and so other detector types are generally applied.

By contrast, charged particles such as electrons, protons, myons and pions lose their energy mainly through inelastic Coulomb collisions with orbital electrons from the absorber material. The maximum energy per interaction that can be transferred to an electron is generally limited to only a small fraction of the particle energy. Together with the high interaction probability, this leads to a continuous energy loss until the particle is stopped or leaves the detector material.

The mean energy loss in a wide energy range can be described by the Bethe-Bloch equation with additional corrections for low and high energies [26]:

$$-\frac{dE}{dx} = 2\pi N_a r_e^2 m_e c^2 \rho \frac{Z}{A} \frac{z^2}{\beta^2} \left[ln \left(\frac{2m_e \gamma^2 v^2 W_{max}}{I^2} \right) - 2\beta^2 - \delta - 2\frac{C}{Z} \right], \quad (3.6)$$

where

- c light velocity
- r_e traditional electron radius $= 2.817 \cdot 10^{-13}$
- m_e electron mass
- N_a Avogadro's number $= 6.022 \cdot 10^{23}$ mol^{-1}
- I medium excitation potential
- Z atomic number of absorbing material
- A atomic weight of absorbing material
- ρ density of absorbing material
- z charge of incident particle in units of e
- β relativistic speed factor of incident particle $\frac{\mathrm{v}}{\mathrm{c}}$
- γ $\frac{1}{\sqrt{1-\beta^2}}$
- δ density correction
- C shell correction
- W_{max} maximum energy transfer in a single collision

3.2. The DEPFET working principle

A DEPFET (**de**pleted **p**-channel **f**ield **e**ffect **t**ransistor) is an electronic semiconductor device, that uses a special MOS field effect transistor on a fully depleted silicon substrate to detect light and particle radiation. The principle was proposed by J. Kemmer and G. Lutz in 1987 [28]. Like all other semiconductor radiation detectors, the DEPFET is based on charge generation in the detector material via the interactions discussed in the previous section. In order to be detected, the electron-hole pairs generated have to be separated within the detector by the presence of an electric field. For the DEPFET, the principle of sideward depletion, proposed by Gatti and Rehak [29], is used to achieve a full depletion of the silicon bulk and thus to maximize the sensitive detector volume. A schematic of this technique is shown in Figure 3.3.

For the sideward depletion, p^+ contacts are put on both sides of a highly resistive n-type silicon bulk resulting in a pn junction on every side of the wafer. In addition, a highly doped n^+ contact (bulk contact) is placed outside the active area to make an ohmic bulk connection. Both intrinsic space charge regions (a) can be extended by applying a more negative voltage - relative to the bulk contact - to the p^+ contact of the specific diode. For sufficiently high reverse biasing of both diodes the two space charge regions will join and the whole silicon bulk is fully depleted (b).

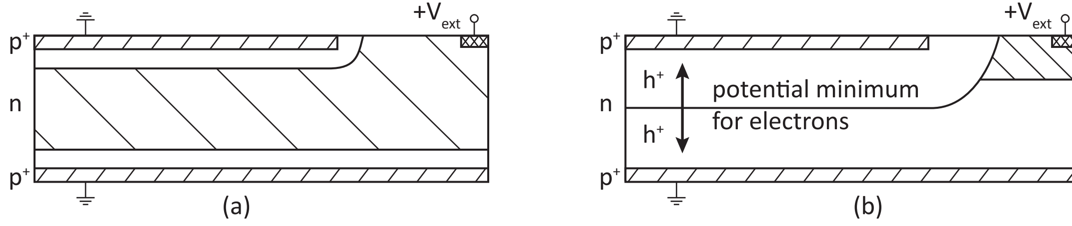

Figure 3.3: *The basic principle of sideward depletion. On both sides of a highly resistive n-type silicon bulk there are p^+ implantations forming two diodes. An n^+ implantation outside of the active volume allows for a bulk contact. The intrinsic space charge regions (a) can be extended by higher reverse biasing of both diodes. For sufficiently positive V_{ext}, both depletion regions touch each other and the bulk is fully depleted (b) (pictures from [30]).*

Taking into account the contact boundary conditions, the potential distribution within the device can be calculated according to the Poisson equation

$$\nabla^2\Phi(\vec{r}) = -\frac{\rho(\vec{r})}{\epsilon_0\epsilon_r} \tag{3.7}$$

where Φ is the electrostatic potential, ρ is the current space charge density, ϵ_0 is the dielectric constant in vacuum, and ϵ_r is the relative dielectric constant for silicon. In case of full depletion and identical reverse biasing of both diodes, it delivers a symmetric potential distribution and a potential minimum for electrons in the middle of the wafer.

In the standard operation of a DEPFET sensor, the front side is kept at a fixed potential and the backside voltage is decreased until the two space charge regions touch each other and the so-called depletion voltage is reached. Figure 3.4 (a) shows the vertical potential distribution within the structure for various bias conditions, assuming a homogeneous n-doping concentration in the bulk. With decreasing backside voltage the space charge region of the backside diode is extended and bulk depletion voltage is reached at V_{dep}. For even more negative backside voltages, the formed potential minimum for electrons is shifted toward the front side but its depth is reduced. In order to compensate for this effect, an additional deep n implantation can be introduced at the front side as indicated in (b). The enhanced donor concentration, according to equation 3.7, results in a stronger bending of the potential and consequently allows for a pronounced and highly confined potential minimum for electrons close to the surface. By tuning the doping distribution you can also adjust the vertical and lateral position and the depth of the potential minimum for electrons.

The basic structure of DEPFET sensor pixels is depicted in Figure 3.5. As necessary for the sideward depletion, the backside consists of a diode used for depletion of the full silicon bulk. Since in the standard operation of a DEPFET sensor the radiation enters the detector through the unstructured backside, the very thin diode is called the entrance window.

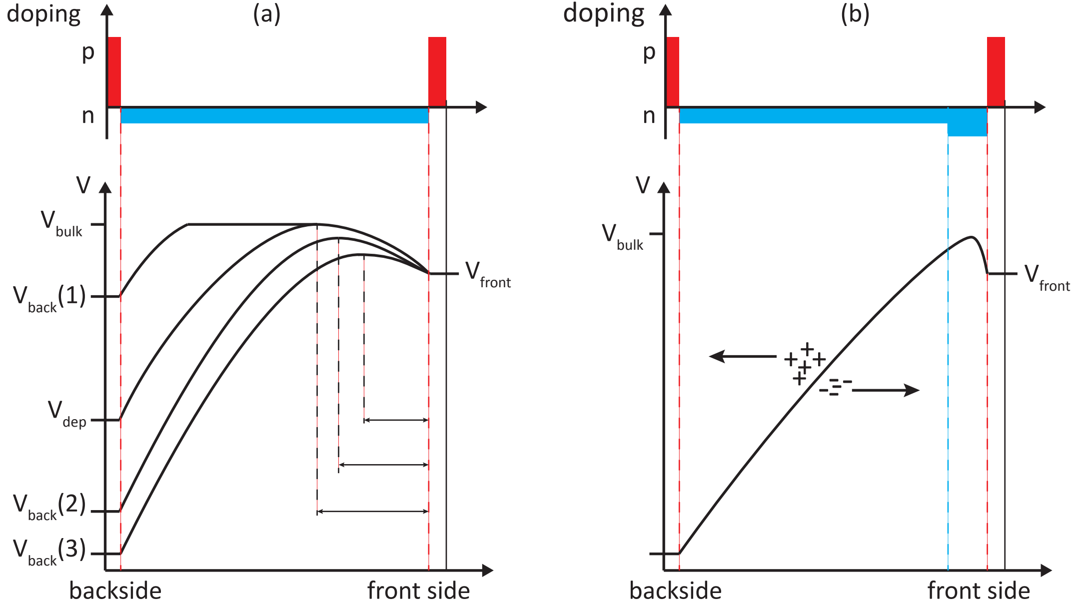

Figure 3.4: *(a) Potential distribution inside a sideward depleted $p^+n^-p^+$ semiconductor structure for asymmetric biasing of the front side and backside diode. After applying a backside voltage more negative than V_{dep} the substrate is fully depleted and a potential minimum for electrons is formed. Further decrease of V_{back} shifts the potential minimum toward the surface and lowers its depth. (b) An increased n-doping concentration close to the front side leads to an improved confinement and enhanced depth of the potential minimum (pictures from [31]).*

On the front side there are two field effect transistors. One is a p-channel field effect transistor comprising the source contact, an external MOS gate and the drain contact in the center. Appropriate biasing and a deep n implantation form a potential minimum for electrons, laterally constricted to the area below the transistor channel. Due to the potential gradient, all electrons generated thermally or by ionizing radiation somewhere in the depleted substrate will be collected in this potential minimum. The stored electrons will induce a mirror charge in the transistor channel and therefore increase the current density in the channel. By measuring the resulting change in the transistor current we can obtain information about the number of stored electrons and thus the energy of the absorbed radiation. Because of the capability to steer the transistor current like an external gate, the potential minimum for electron is called "internal gate". The sensitivity of the transistor current I_D to signal charges Q_{sig} in the internal gate can be calculated according to the analytical DEPFET model proposed by J. Kemmer et al. [32]

$$g_q = \frac{dI_D}{dQ_{sig}} = \sqrt{\frac{2\mu_p I_D}{WL^3C_I}} \tag{3.8}$$

with μ_p being the hole mobility in the transistor channel, W the width, L the length of the transistor channel and C_I the gate insulator capacitance per unit area. Hence, the g_q

depends strongly on the geometry of the transistor - for a standard DEPFET it is in the order of 300 pA per electron. This high amplification can be achieved due to the very small input capacitance of the internal gate, which is in the range of only several tens of fF.

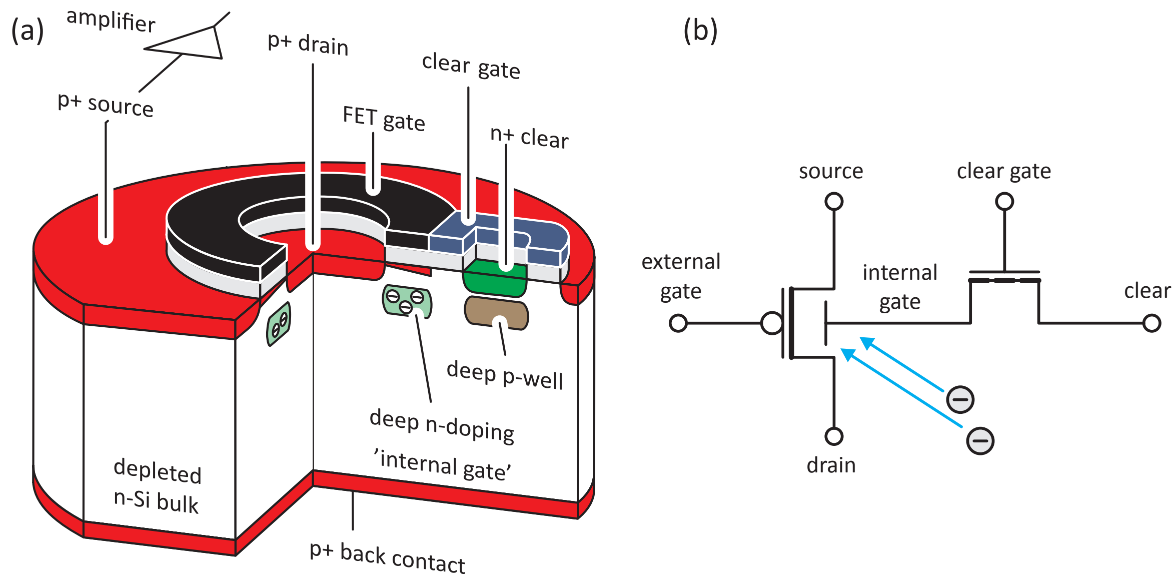

Figure 3.5: *A DEPFET pixel cell (a) and its equivalent circuit (b). The transistor current between source and drain is controlled by the external and internal gates. The charge from the internal gate can be removed by the adjacent nMOS clear structure. The clear gate shields the bulk and the internal gate from the clear contact preventing electron injection as well as charge loss.*

The readout is performed by a comparative measurement of the channel conductivity, once with and once without charge in the internal gate. This so-called correlated double sampling can be implemented either as source follower or as drain current readout. When using the source follower configuration, the source voltage change needed for a constant current through the transistor is measured, whereas for the drain readout the change of the transistor current is determined directly. For the low noise baseline measurement with an empty internal gate, the signal electrons have to be removed from the internal gate by an adjacent clear structure consisting of an n^{+}-doped "clear" contact and a second MOS gate called "clear gate". Together with the internal gate, the clear structure builds an n channel transistor allowing for the complete extraction of signal electrons from the internal gate if a positive voltage is applied to the clear and the clear gate. In order to avoid loss of signal charge into the clear contact as well as the emission of electrons from the clear contact into the internal gate, the clear contact is embedded into a p-doped well that forms a potential barrier for electrons in both directions.

The DEPFET combines detection and amplification within a single device, which provides several outstanding properties:

- Internal amplification without interference-prone connections between sensor and amplifier
- Minimum input capacitance for low noise
- High quantum efficiency for low energies because of irradiation through the homogeneous and thin entrance window on the backside
- High quantum efficiency for high energies because of a fully depleted substrate
- Analog storage in the internal gate allowing for "readout on demand"
- Nondestructive readout of stored information allowing for repetitive readout to reduce the low frequency noise
- Usage as unit cell for 2D active pixel sensors with fill factors of 100 % because of the unstructured, homogeneous, thin entrance window

In addition to its application as an active pixel sensor with an amplifier in each pixel, the DEPFET can also be used as readout node for other detector types like pn-CCDs and silicon drift detectors [33].

3.3. Noise considerations

The achievable energy resolution of a semiconductor radiation detector is limited by overall system noise. The following sections will discuss the physical causes of noise, their dependencies on detector materials and the various operating conditions.

3.3.1. Fano noise

As already mentioned in section 3.1, energy deposition in a semiconductor by ionizing radiation leads to the generation of electron-hole pairs. For silicon, the mean pair generation energy (PGE) is w=3.65 eV, much higher than the band gap because the excitation of phonons transfers part of the energy to the crystal lattice. Since the PGE can be considered to be constant in a wide energy range, the average number of generated electron-hole pairs can be calculated by

$$\langle N \rangle = \frac{E_0}{w} \tag{3.9}$$

with E_0 being the energy deposition in the semiconductor [34].
Due to statistical fluctuations of the generation process, N underlies certain deviations that are described by the Fano statistics. For this purpose, the Fano factor can be defined

as the mean square deviation (variance) of the number of generated electron-hole pairs divided by their mean number $\langle N \rangle$.

$$F = \frac{\langle N^2 \rangle - \langle N \rangle^2}{\langle N \rangle} = \frac{\sigma_{Fano}^2}{\langle N \rangle} = \frac{\sigma_{Fano}^2}{\sigma_{Poisson}^2} \tag{3.10}$$

The Fano factor can be interpreted as an adjustment factor to relate the observed variance to the variance predicted by the Poisson statistics. This is an intrinsic material parameter and has to be as small as possible in order to get low noise and thus good energy resolution. In literature, the value for silicon is commonly specified with F_{Si}=0.115 [35]. However, this value may increase for energies below 1 keV [36–38]. Combining equation 3.9 and 3.10 results in the so-called Fano noise:

$$\sigma_{Fano} = \sqrt{\frac{F \cdot E}{w}} \tag{3.11}$$

Fano noise is an intrinsic property of semiconductor materials and defines the physical limit of the achievable energy resolution of a semiconductor detector system.

3.3.2. Thermal noise

Thermal noise is due to the thermal motion of charge carriers. In a semiconductor the electrons in the conduction band are unbound. Their movement is dominated by electric fields (drift) and gradients in the carrier density (diffusion). This straightened motion is overlaid by random and omnidirectional movement because of the Brownian motion from their thermal energy. Within a transistor, this causes statistically independent fluctuations of the current in the channel, which can be modeled by a noise current source at the drain. Quantum mechanical calculations allow for an analytical determination of its spectral noise-power density. In the typical approximation for a linear device it is given by

$$\frac{d\langle \overline{I^2} \rangle}{df} = \frac{4}{3} k_B \; T \; g_m \tag{3.12}$$

with k_B as the Boltzmann constant, T as the absolute temperature and g_m as the transconductance of the transistor defined as $g_m = \frac{\partial I_{DS}}{\partial U_{GS}}$ [30]. In this approximation the spectral distribution of the thermal noise is independent of the frequency and for this reason generally termed white noise. The quantum mechanical solution includes a cutoff frequency where the spectral noise density drops exponentially and thus guarantees its integrability. Since the bandwidth of semiconductor radiation detectors is limited to frequencies far below the cutoff frequency, the cutoff can be neglected.

3.3.3. 1/f noise

The physical reasons for $1/f$ noise are myriad, many of them are caused by statistical fluctuations in the number of charge carriers and their changing mobility.

For a MOSFET, like the ones used for DEPFET sensors, it is strongly related to the Si-SiO_2 interface where the structure abruptly changes from the crystalline Si to the amorphous SiO_2. This transition leads to unsaturated covalent bindings of silicon atoms called dangling bonds. Usually, dangling bonds are saturated by annealing in a hydrogen atmosphere during the production process - a few will remain, however. If charge carriers in the transistor channel pass a dangling bond they can be trapped, resulting in a reduction of channel conductivity. The probability of this depends on the capturing cross section and on carrier density in the vicinity of the trap. Due to its thermal energy, the trapped charge can be reemitted after a certain delay, thereby leaving the active trap behind. The probability for reemission depends on the energy level of the trap within the band gap, the device temperature, and the electric field conditions (Poole-Frenkel effect).
Similar to thermal noise, the $1/f$ noise can be modeled by a drain current noise with the spectral power density of

$$\frac{d\langle\overline{I^2}\rangle}{df} = \frac{K_F\ g_m^2}{W\ L\ C_{ox}^2}\ \frac{1}{f}. \tag{3.13}$$

The parameter K_F is characteristic for the technology of the production process and is correlated to the existing trap density in the vicinity of the channel. The transistor geometry consists of the gate length L, the gate width W and the capacitance of the gate insulator C_{ox} [30]. Frequency dependence in MOSFETs is approximately $1/f$ and can be derived by assuming various different traps with a continuous distribution of time constants for capturing and reemission.

3.3.4. Shot noise

Shot noise in a semiconductor radiation detector is caused by leakage current in the sensor. Thermally generated leakage current refers to all electron-hole pairs that were not generated as a result of the radiation which should be detected. Generally, it is composed of gate, surface, and bulk leakage current, but for DEPFETs, the bulk leakage current is the most prevalent type.
The excitation probability p of charge carriers over a forbidden energy gap E_{gap} can be approximated by the Boltzmann statistic according to:

$$p \propto e^{-\frac{E_{gap}}{2k_BT}} \tag{3.14}$$

with k_B being the Boltzmann constant and T the device temperature. Generation probability increases exponentially by lowering the E_{gap}, which makes energy levels in the middle of the band gap (deep traps) the most efficient generation centers because they serve as an intermediate state for the excitation of electrons from valence into the conduction band.
Deep traps in the silicon bulk contribute to the volume leakage current and can arise either from impurities in the crystal lattice, crystal defects caused by the production process or from irradiation with massive particles like protons (compare section 3.1.2). In addition,

dangling bonds at the Si-SiO_2 interface also possess energy levels roughly in the middle of the band gap and cause so-called surface leakage current. For a DEPFET sensor, this contribution is negligible because surface generated electrons are removed from the device by dedicated contacts. Taking into account only deep traps, the leakage current can be halved by a temperature reduction of roughly 7 K. To minimize the leakage current also high electric fields close to breakdown field strength have to be avoided in the sensor as they may lead to avalanche effects.
To model shot noise, we take an assumed current source to charge the internal gate with a constant leakage current I_l

$$I_l = \frac{\Delta Q}{\Delta t} = \frac{\Delta N \cdot e}{\Delta t}. \tag{3.15}$$

Here e denotes the elementary charge and ΔN the number of electrons arriving in the internal gate during the time interval Δt.
With statistical fluctuations of the number of arriving electrons $\delta\Delta N = \sqrt{\Delta N}$ the standard deviation of the transistor current can be described by

$$\langle \delta I_l^2 \rangle = \frac{e^2(\delta\Delta N)^2}{\Delta t^2} = \frac{e^2(\Delta N)}{\Delta t^2} = \frac{I_l e}{\Delta t}. \tag{3.16}$$

Spectral noise density can be derived from this, assuming that potential distribution is not changed by any electron previously collected in the internal gate:

$$\frac{d\langle \overline{I_l^2} \rangle}{df} = 2 I_l e. \tag{3.17}$$

It should be pointed out that shot noise especially affects sensor devices with large active volumes where the arriving leakage current in the internal gate is high. These devices have to be cooled in order to reduce shot noise and achieve good energy resolution. However, for large sensors with a lot of small pixels, shot noise will only play a minor role.

3.3.5. Energy resolution

In order to calculate the achievable energy resolution of a semiconductor radiation detector, all noise sources have to be considered, as is done in Figure 3.6 for the drain readout concept. In this case, the information about energy deposition is obtained by measuring the change in the transistor current, which means all noise is modeled using two current noise sources: I_L and I_N. Thermal and 1/f noise are represented by I_N inducing a noise current parallel to the transistor. Leakage current and any involved fluctuations are represented by I_L.
For drain readout, all DEPFET voltages are kept at fixed potentials. For the drain, this is guaranteed by a current buffer that also ensures that the transistor current is not influenced by the electronics outside the sensor. Downstream of the current buffer, the analog current signal is filtered before it can be processed.

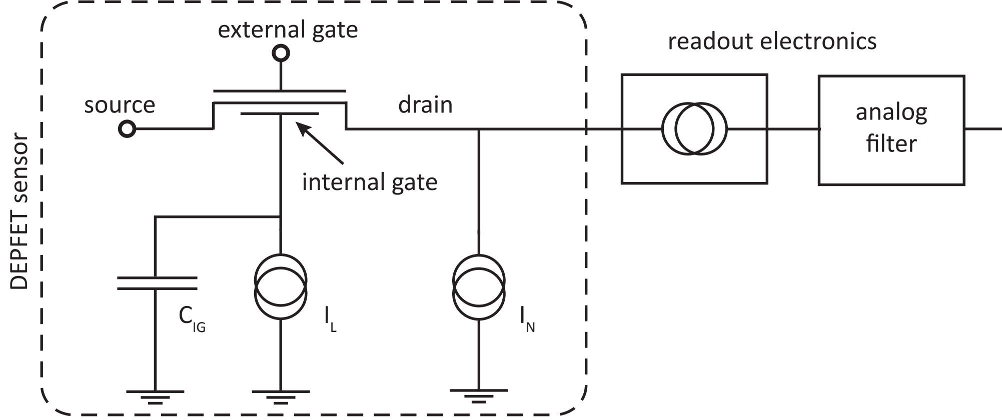

Figure 3.6: *Noise model for drain current readout of a DEPFET sensor. Thermal and* 1/f *noise are modeled by the noise current source* I_N *and the leakage current and any involved fluctuations are represented by* I_L.

To receive the r.m.s. noise value at the output point of the electronics, spectral densities (compare previous sections) have to be integrated over the full bandwidth of the system. According to [39], when applying this to the system shown in Figure 3.6, one gets an electronic noise of

$$ENC^2 = a' A_1 \frac{1}{\tau} \frac{1}{g_q^2} + 2\pi a'_f A_2 \frac{1}{g_q^2} + b A_3 \tau. \tag{3.18}$$

In this notation, noise is shown in terms of equivalent noise charge (ENC), i.e. the number of electrons that has to be collected in the internal gate in order to get a signal equivalent to the r.m.s. noise at the output. The constants A_1, A_2 and A_3 are defined by the shape of the analog filter (weighting function) while τ denotes its specific time constant (shaping time). In addition, $g_q = \frac{\partial I_{DS}}{\partial Q_{IG}}$ represents the amplification of the internal gate and the spectral densities of the individual noise contributions are denoted by the constants

$$a' = \frac{4}{3} k_B \, T \, g_m \qquad \text{(thermal noise)} \tag{3.19}$$

$$a'_f = \frac{K_F \, g_m}{W \, L \, C_{ox}^2} \qquad \text{(1/f noise)} \tag{3.20}$$

$$b = 2 I_l e \qquad \text{(shot noise)} \tag{3.21}$$

To optimize noise performance, the weighting function and the related shaping time have to be adjusted for every specific application. For example, if the detector has large pixels and is operated at high temperatures, the shaping time should be short in order to reduce shot noise. By contrast, thinking of a matrix with small pixels operated at very low temperatures, it may be better to have a longer shaping time to decrease thermal noise.
Finally, the energy resolution ΔE of a semiconductor radiation detector, usually expressed in the Full Width at Half Maximum (FWHM) of the Gaussian peak in the energy spectrum

for a constant energy deposition E_0, is given by

$$\Delta E \approx 2.355 \cdot w \cdot \sqrt{ENC^2 + \frac{F \cdot E_0}{w}}. \tag{3.22}$$

ENC^2 represents the electronics noise and $\frac{F \cdot E_0}{w}$ is Fano noise with w being the pair generation energy and F the Fano factor of the detector material. The factor 2.355 is due to the conversion from standard deviation to the FWHM of a Gaussian peak.
Assuming perfectly noise-free electronics ($ENC^2 = 0$), the achievable energy resolution is defined by the so-called Fano limit ΔE_{Fano}.

3.4. Matrix operation

The DEPFET is often utilized as a unit cell for 2D imaging detectors. The readout of these 2D pixel matrices has been performed row by row until now. Figure 3.7 illustrates the standard interconnection scheme of a DEPFET pixel matrix in the source follower configuration.
Every DEPFET pixel of the 4 x 4 matrix is represented by a simple schematic including the transistor with external (top) and internal gates (bottom). The clear and the clear gate are indicated by a single switch allowing for the extraction of signal charge from the internal gate. These clear switches as well as the external gate contacts are connected in rows to SWITCHER controlling ASICs [40] on both sides of the matrix that provide clocked voltages for the readout sequence. By contrast, the sources are connected in columns to the individual readout input of the so-called ASTEROID readout chip [41, 42] on the bottom side of the matrix. The ASTEROID is a 64-channel shaper/amplifier IC featuring a trapezoidal weighting function for minimum noise, serial analog readout and an integrated shaping sequencer for flexible adjustment of filtering time. All other contacts like the drain or the backside are connected globally to external power supplies.
Using this interconnection scheme, matrix readouts can be performed according to the sequence shown in Figure 3.8. It illustrates the switching sequence of the relevant DEPFET voltages and the two sampling points for correlated double sampling needed to read out a single row of pixels. Signal charge is integrated in the internal gate when the transistor is switched off. For the beginning of the readout sequence, the row under readout is activated when the gate SWITCHER applies a negative voltage to the external gate of the DEPFET. At that moment, the channel conductivity is affected by the signal charge stored in the internal gate. Hence, the following first sampling point is called signal sampling. Analog signals from the transistor sources can be processed in parallel because all active sources are connected to their individual input of the readout chip by the vertical interconnections.

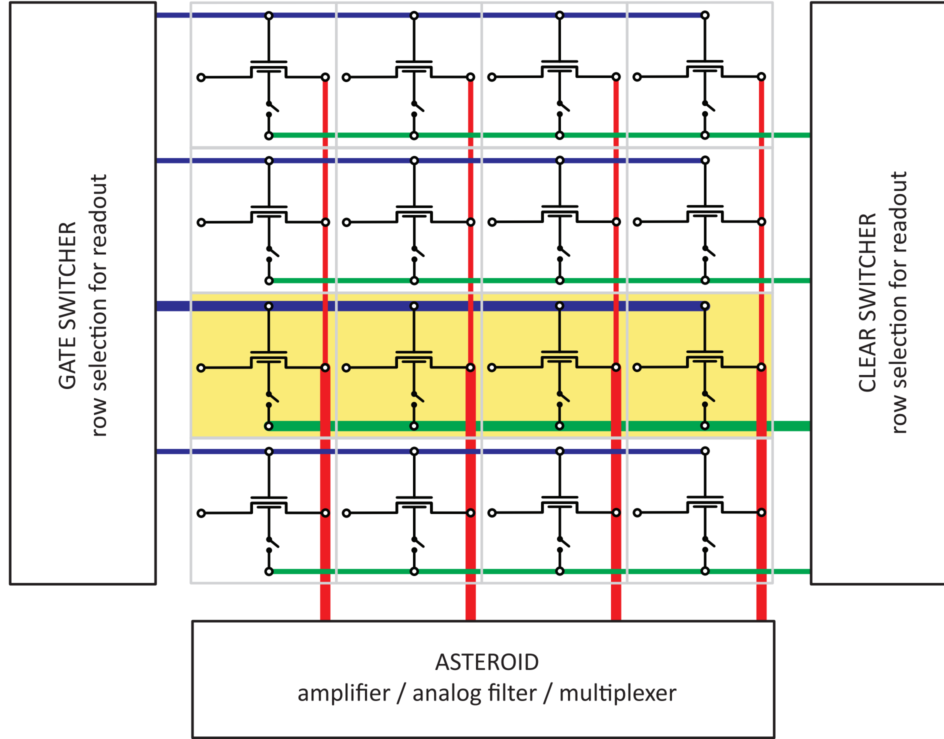

Figure 3.7: *A schematic of the matrix interconnection scheme in source follower configuration. It shows a 4 x 4 matrix with each pixel represented by its simplified equivalent circuit. The drain is connected globally and the sources are connected in columns to the readout ASIC. Row selection is made by the two SWITCHER ASICs, while the readout ASIC performs column parallel readout. The currently active row is colored and the respective connection lines are drawn thick.*

After the signal sampling, all signal charge is removed from the internal gate by applying a positive voltage to the clear (V_{cl}^{on}) and the clear gate (V_{cg}^{on}) via the corresponding clear SWITCHERs.

In order to avoid back emission of electrons into the internal gate, the clear pulse completely envelopes the clear gate pulse. Their temporal overlap, defining the duration of the clear process, has to be sufficiently long to extract all electrons from the internal gate so that the subsequent baseline sampling can measure the channel conductivity with an empty internal gate. The signal difference between the two measurement points containing information on the number of signal charges is usually obtained by a dedicated readout ASIC. These readout ASICs are available for drain current as well as for source follower readout (ASTEROID) and also comprise the analog filter to minimize noise. The simultaneously processed analog signals for the individual sources are subsequently serialized by an internal multiplexer and transferred to an analog-to-digital converter (ADC) and a data acquisition system (DAQ). The last step of the readout procedure is to switch off the active row and select the next row. This line-by-line readout is called rolling shutter mode.

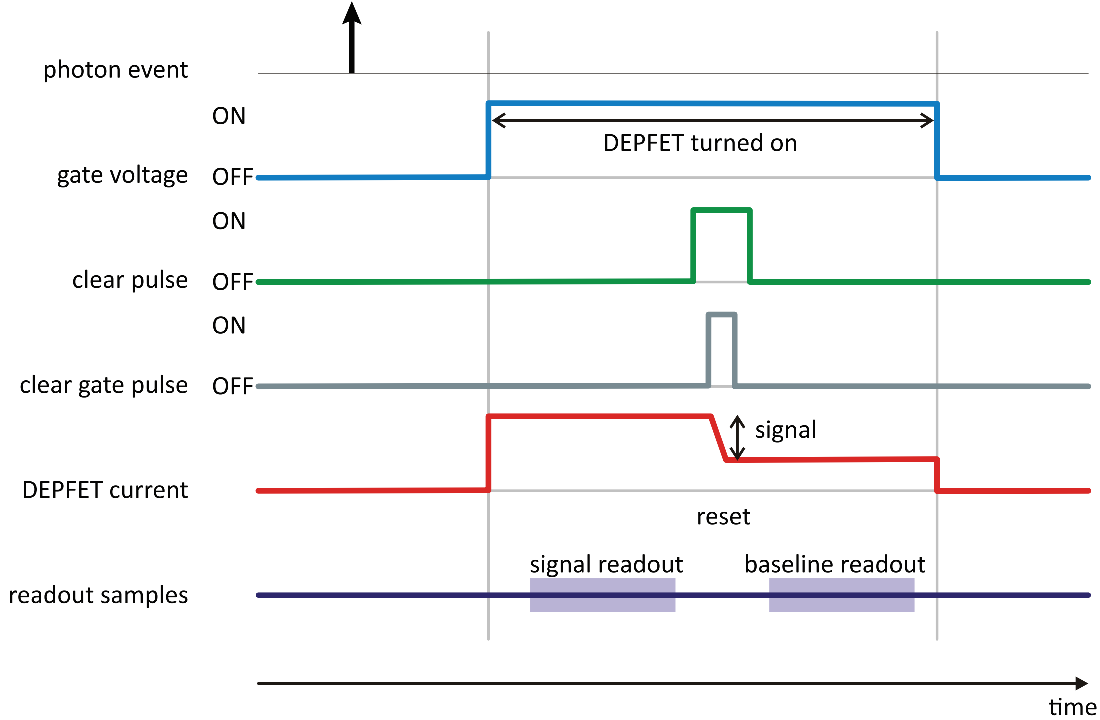

Figure 3.8: *Principle of DEPFET drain current readout. The drain current is measured before and after the clear pulse. The signal corresponding to the charge collected in the internal gate is the difference between the two measurements. The pixel is turned on only during readout and the charge is removed from the internal gate by applying a positive voltage to the clear and clear gate.*

Because the DEPFET is an active pixel sensor with an amplifier in every pixel, the choice of the following row is arbitrary and not restricted to a certain order. This allows for the so-called window mode, where specific sensor areas are read out faster and more often than the rest of the matrix. This can be useful for astronomy applications e.g. the observation of exceptionally bright objects in the field of view requiring very fast readout to avoid the occurrence of several photons within a single readout cycle (pileup).

One example of a large-area DEPFET matrix is shown in Figure 3.9. The sensor comprises 256 x 256 pixels with a pixel size of 75 x 75 μm^2 and therefore an active area of roughly 3.7 cm^2 [43]. On each side of the sensor there are four SWITCHER steering ASICs. The four ASICs on the left side take over the selection of row to be read out, whereas the four ASICs on the right are used for the synchronous reset of the internal gate of the active row. On the bottom side, four ASTEROID readout ASICs are bonded to the sensor, each comprising 64 parallel readout channels. The standard readout time for this setup is about 4 μs per line, limited by the shaping time of the ASTEROID. For the matrix shown, the maximum frame rate f_{max} is derived from

$$f_{max} = \frac{1}{256 * 4\ \mu s} \approx 1\ kHz.$$

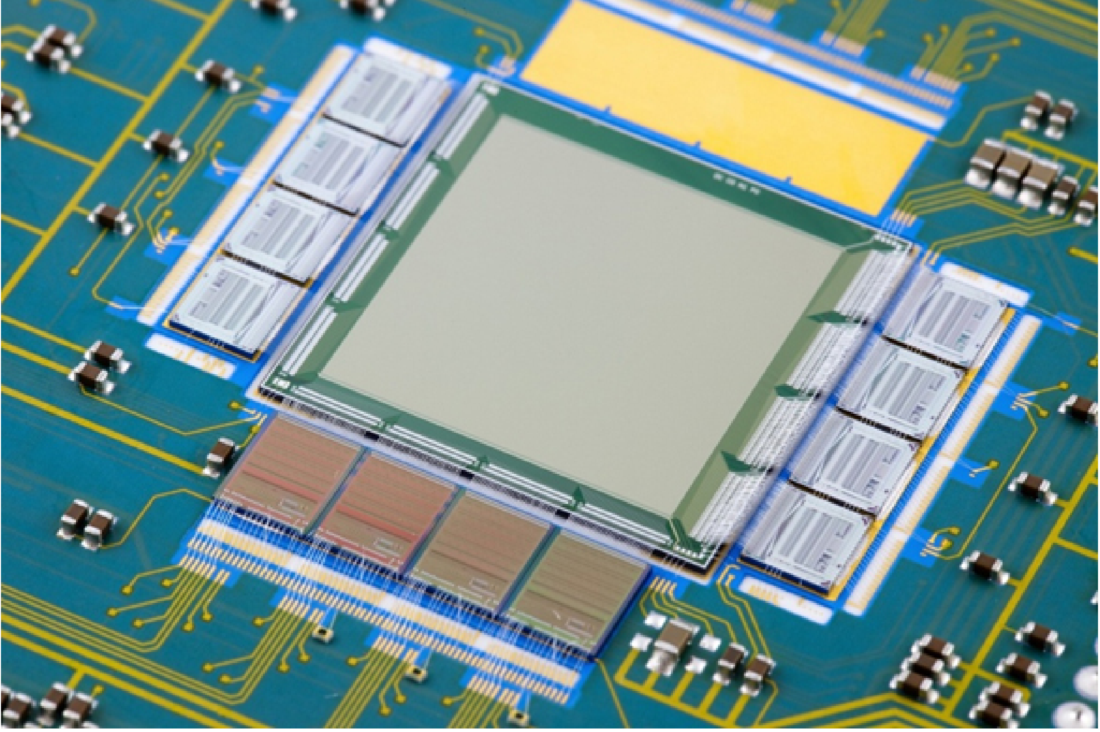

Figure 3.9: *Front side of a DEPFET sensor matrix with 256 x 256 pixels with a pixel size of 75 x 75* μm^2*. On each sides of the sensor four SWITCHER ICs are placed providing the dynamic voltages for the matrix operation. On the bottom side four ASTEROID readout ASICs can be seen.*

In principle, the frame rate can be enhanced by increasing the number of readout nodes. One possibility to achieve this is, for example, to separate the matrix into two hemispheres allowing for the readout in two directions. This option is already foreseen on the ceramic carrier shown in Figure 3.9, where four additional ASTEROIDs can be placed on top of the sensor. Although this increases power consumption and related heat dissipation of the detector, it can still be a beneficial solution for some applications.
The performance of a tested 256 x 256 DEPFET pixel array is shown in Figure 3.10. The DEPFET pixel array allows for spatially resolved X-ray detection with near Fano-limited spectral resolution. Its imaging capability is illustrated in (a) using a silicon baffle in front of the detector to shield the 4.5 keV photons generated with an X-ray tube and a ^{20}Ti target. The number of impinging photons is color-coded and the unshielded areas are clearly visible. The spectroscopic performance of the matrix for backside illumination with an ^{55}Fe source and a device temperature of -40°C is indicated in (b). For single events, i.e., all radiation-induced electrons are collected in a single pixel, the measured energy resolution of the Mn-K$_\alpha$ line at 5.9 keV was 127 eV FWHM ($\Delta E_{Fano} = 117\ eV$). Due to small pixel size, the peak-to-background ratio was only around 1,000, but dedicated analysis algorithms can reconstruct so-called split events - signal electrons induced by a single photon distributed over more than one pixel. This significantly improves the peak-to-background ratio and only slightly deteriorates the energy resolution.

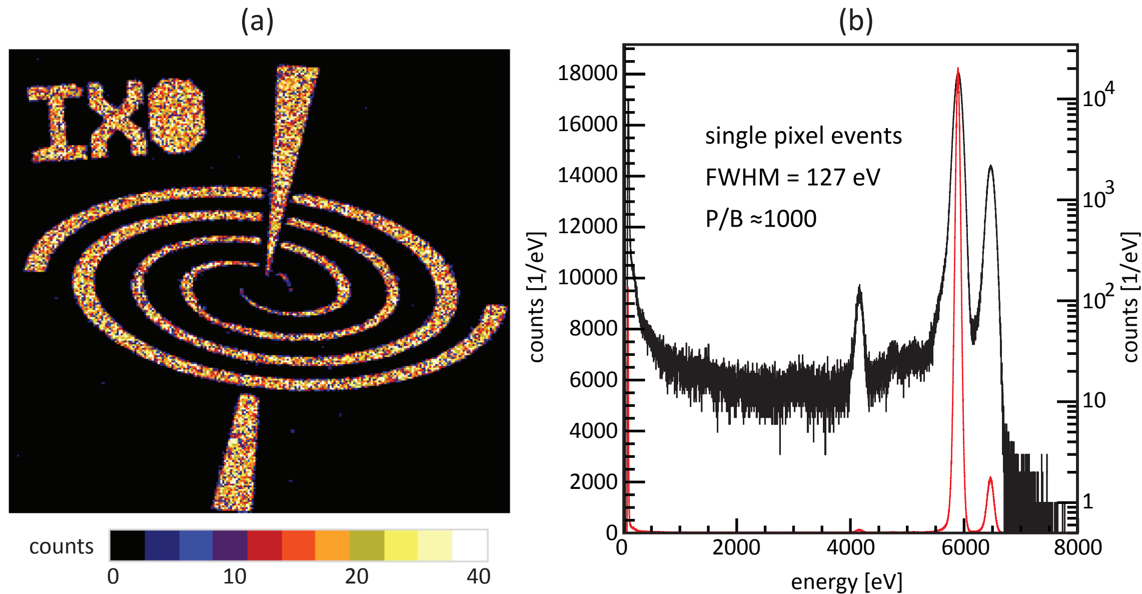

Figure 3.10: *(a) X-ray image obtained with an X-ray generator using a ^{20}Ti target (4.5 keV) and a silicon baffle in front of the detector after 20 min of exposure. (b) ^{55}Fe spectrum in logarithmic (black) and linear (red) scales including all single events recorded over the matrix when it is backside illuminated at -40°C and read out at 300 frames/s. Energy resolution of the Mn-K$_\alpha$ line at 5.9 keV is 127 eV FWHM. Peak-to-background ratio is about 1,000 for a background evaluated at 1 keV [43].*

3.5. Fields of application

The motivation to use DEPFETs as radiation detectors is driven by their unique properties. The technology allows for the realization of large-area devices with excellent homogeneity and the DEPFET itself provides outstanding characteristics. The following compilation is intended to show the current and future areas of application for DEPFET sensors in addition to photon counting at FEL experiments.

Imaging spectroscopy for astronomy applications

The **M**ercury **I**maging **X**-ray **S**pectrometer (MIXS) on board ESA‘s 5th cornerstone mission, BepiColombo, will be the first space instrument using DEPFET-based detectors. This mission will explore Mercury, the closest planet to our sun, and provides a suite of sixteen instruments for the scientific community [44, 45]. BepiColombo will be launched as a composite spacecraft in 2015, and upon arrival at Mercury in 2022 will be separated into two independent orbiters, the Mercury Magnetospheric Orbiter (MMO) and the Mercury Planetary Orbiter (MPO). The MPO will carry eleven instruments, one of them being the MIXS instrument. MIXS will investigate the elemental composition of Mercury’s surface

using X-ray fluorescence (XRF) analysis, a well-known technique that has been successfully deployed by NASA‘s MESSENGER XRS (X-Ray Spectrometer) [46, 47].

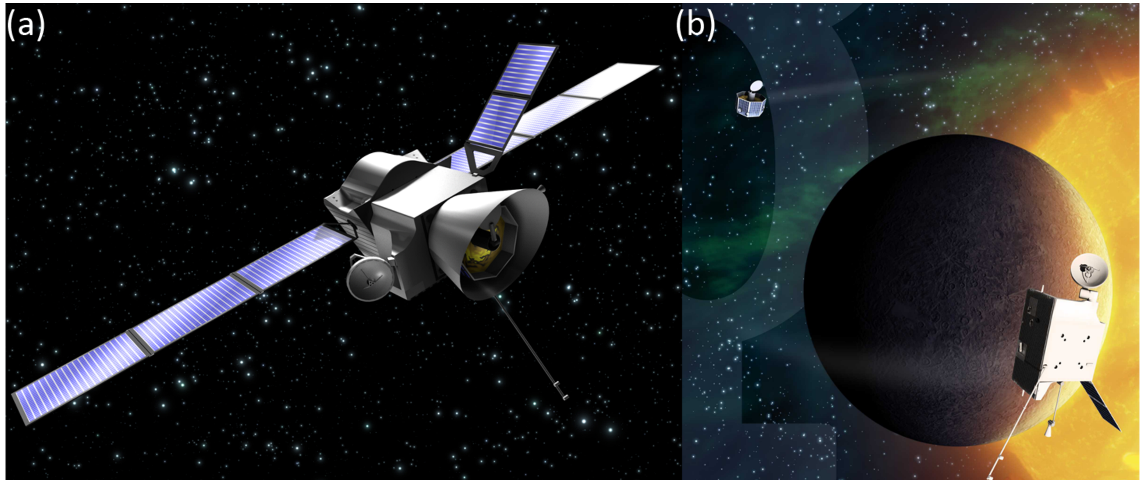

Figure 3.11: *(a) The two BepiColombo orbiters mounted atop the transfer module to form one single-composite spacecraft. (b) After arrival at Mercury, the two orbiters will be separated and the Mercury Planetary Orbiter (MPO) will map the planet while the Mercury Magnetospheric Orbiter (MMO) will investigate its magnetosphere (pictures from [49]).*

The MIXS instrument comprises two identical DEPFET detector modules with complementary optics. One is equipped with a collimator that provides a large field of view and the second will have telescope optics allowing for a spatial resolution of less than 1 km on the surface of Mercury at periherm (closest point) and 4 km at apoherm (farthest point) [48]. Each of the two MIXS DEPFET detector modules consists of 64 x 64 quadratic pixels with a pixel size of 300 x 300 μm^2 covering an active area of 3.69 cm^2. A frame rate of almost 5.9 kHz can be achieved due to the separation of the matrix into two individual hemispheres and the associated doubling of readout channels.

The hostile radiation and thermal environment in Mercury's orbit puts severe requirements on operating temperature and radiation tolerance, but due to its intrinsic radiation hardness, at an energy levels of 1 keV the DEPFET can still provide energy resolution better than 200 eV at mission end, which is required for scientific purposes. Moreover, by embedding the DEPFET into a drift structure, the pixel size can be scaled easily to very large areas. This makes it possible to adjust the detector point spread function to the telescope optics. Both of these things were crucial in the selection of DEPFETs for the MIXS instrument.

More information on MIXS can be found in [50–54]. The MIXS instrument is the first space instrument using DEPFET detectors, but because of their exceptional properties DEPFETs are also foreseen for many other projects in the field of astrophysics [43, 55–58].

Particle tracking in high-energy physics

Unlike to astrophysical applications requiring particularly excellent energy resolution for spectroscopy, the focus in high-energy physics is mainly on spatial resolution.

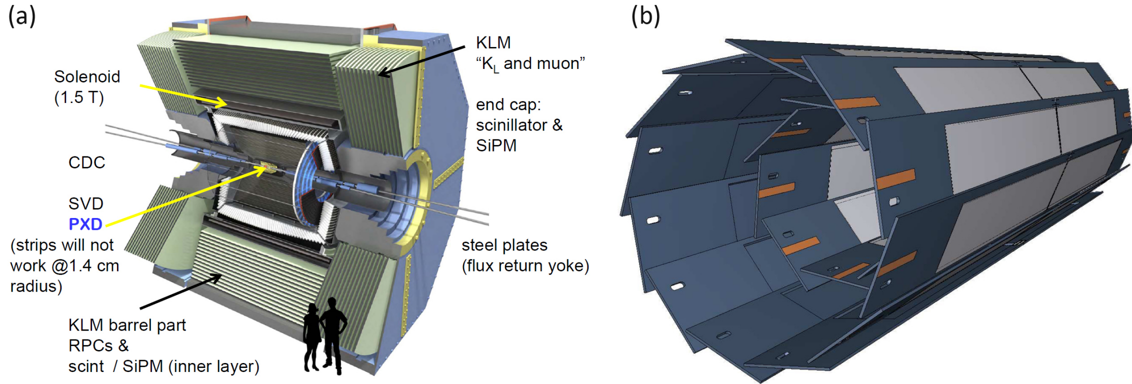

Figure 3.12: *(a) The BELLE2 detector with the pixel vertex detector (PXD), silicon strip detectors (SVD), the central drift chamber (CDC), a barrel-shaped array of Time-Of-Propagation counters (TOP) and the KLM for the detection of K_L^0 mesons and muons. (b) The pixel vertex detector of the BELLE2 detector consists of two cylindrically arranged layers of DEPFET detector modules with eight MPixels (pictures from [59]).*

One example of DEPFETs used in high-energy physics is the BELLE2 experiment at the SuperKEKB collider in Japan. The experiment focuses mainly on the basic understanding of CP violation, which is thought to be responsible for the imbalance between matter and antimatter, and thus for the existence of dark matter.
As usual in high-energy physics, the BELLE2 detector shown in Figure 3.12 consists of several shells of different detector types providing various capabilities (a). The innermost part of the BELLE2 is the so-called pixel vertex detector (b). The high luminosity of the SuperKEKB prevents the use of strip detectors because at a distance of 1.4 cm from the interaction point, occupancy is too high.
Therefore, a DEPFET-based pixel vertex detector will be used that features small pixels with a size of 50 x 50 μm^2 and simultaneously very high frame rates of roughly 50 kHz. To avoid multiple scattering, these DEPFETs are processed on a thinned substrate to minimize the material inside the detector. Although the thinned substrate leads to a reduced amount of signal charge in the detector, the small input capacitance of the DEPFET still guarantees a sufficient signal-to-noise ratio for particle tracking. For these reasons, and because of its intrinsic radiation hardness, a DEPFET-based vertex detector has been considered for the BELLE2 experiment.
Due to the small pixel area there is a high probability that single particles will deposit energy in more than one pixel. By using suitable analysis techniques such as the determination of the center of gravity for energy depositions, a spatial resolution of less then 15 μm and thus much better than the pixel size can be achieved [59]. Other applications in the field of high-energy physics can be found in [60–62].

3.6. Functional principle of new DSSC-DEPFET

In contrast to the spectroscopy and tracking applications previously discussed, the implementation of the DEPFET in FEL experiments makes, among other things, completely new demands on the dynamic range of the detector. Besides the registration of single low-energy X-ray photons, the processing of several thousand photons per pixel per frame should be within the realm of feasibility. Moreover, photon counting capability should not be limited by the detector system but only by the Poisson statistics of the photon generation process in the undulator. A new DEPFET sensor with internal signal compression (DSSC-DEPFET) was developed to meet these requirements.

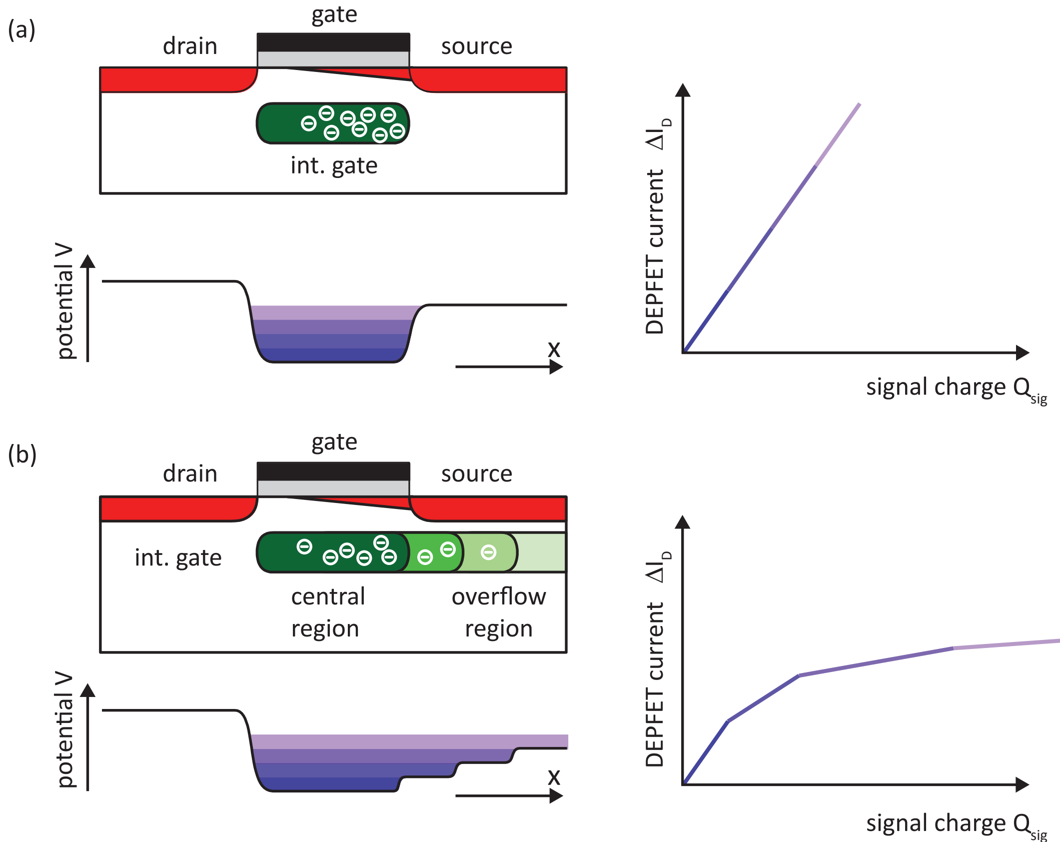

Figure 3.13: *Schematic illustration of the DEPFET with the corresponding potential distribution (left) and the resulting response curve (right) for a spectroscopy DEPFET (a) and a new DSSC-DEPFET (b).*

A spectroscopy DEPFET, as shown in Figure 3.13 (a), has an internal gate located just below the external gate. This leads to an identical steering effect for all signal electrons and thus to a linear relationship between the signal charge and the change of the transistor current.

For the DSSC-DEPFET (b), additional deep n implantations have been introduced that range from the central into the source region. The enhanced n-doping concentration leads to an enlargement of the internal gate below the source, which serves as an overflow region

for electrons. The staggered extension of the implantations into the source region causes a gradient in the n-doping concentration with the maximum being still directly below the transistor channel. Therefore, the location of the absolute potential minimum for electrons does not change compared to the standard DEPFET. Small amounts of signal charge are still stored exclusively in the central region and have a strong steering effect on the transistor current. However, for a higher number of X-rays hitting the pixel, the potential step toward the overflow region will be equalized due to signal electrons partially compensating the positive space charge. Additional signal electrons subsequently spill over into the overflow region under the source. Because only the part of the signal charge which is situated under the channel can modulate the transistor current, amplification for subsequent charge is reduced. Expansion of the internal gate leads consequently to a compression of the output signal of the DEPFET. The resulting relation between signal charge and modulation of the transistor current is only linear for small amounts of charge. The ensuing overflow of signal electrons under the source as well as the associated smaller steering effect leads to a reduction of the response curve gradient, and thus to a nonlinear amplification of the DSSC-DEPFET. The high gain for small amounts of charge allows for the detection of single low-energy X-rays. Processing high numbers of photons is ensured by the overflow region under the source. On the one hand, this increases the charge handling capacity of the internal gate and thus allows for the storage of high levels of charge. On the other hand, related compression of the output signal guarantees that the input range of the readout electronics is not exceeded.
Using DEPFET geometry as well as spatial arrangements and implantation dose, the nonlinear response curve can be adapted to the respective sensor requirements. For example, by enlarging the overflow area the signal compression can be reinforced because only a smaller fraction of the signal charge will be stored in the central region. By introducing a staggered overflow region with several potential steps, as indicated in Figure 3.13 (b), a smooth transition between high and low gain can be attained. The height of each individual potential step is determined by the local change in n-doping concentrations. Together with the area of the overflow segment, the height defines the amount of space charge that has to be compensated before spillover into the next overflow segment begins. Charge handling capacity for each overflow segment can therefore be tuned by adjusting the geometry and dose of the implantations. Hence, within a wide range, the nonlinear response curve of the DSSC-DEPFET can be tailored to the specific requirements of different applications. However, this requires a deep understanding of the device physics and a precise knowledge of the impact of the DEPFET design parameters on its amplification properties. The modeling and improvement of simulation accuracy with regard to nonlinear amplification is therefore one of the crucial issues of this thesis.

4. DSSC-DEPFET prototypes

4.1. Prototype fabrication

The production of DEPFET active pixel sensors comprises about 150 process steps including depositions, etching steps, annealing cycles, implantations and roughly 30 lithography steps. In addition, devices with large areas of several cm^2 are fabricated that in the end need to be free of all defects and should be as homogeneous as possible. Coping with these demands requires a lot of inspection steps to immediately detect technological problems and repeat the process step if necessary. This amount of effort is indispensable to achieve a high yield, but leads to a production time of roughly 18 months. Because of time limitations in the DSSC project, only one prototype run was foreseen, and therefore the development of new DSSC-DEPFET devices was mainly based on numerical device simulations giving a reliable prediction of the device performance in advance. Nevertheless, several different DEPFET designs with a nonlinear gain feature have been developed to obtain a better understanding of the device and recognize possible design issues before starting final sensor production. For this reason, seven DEPFET variants have been designed and fabricated in order to test some aggressively optimized variants but at the same time retain conservative structures to be on the safe side.

As mentioned in chapter 2, the European XFEL requires very high readout speeds up to 4.5 MHz. Hence, DSSC-DEPFET pixels have a hexagonal shape in order to reduce the maximum drift length from the outer rim of the pixel toward the central region of the internal gate and thus minimize the required charge collection time. Moreover, the probability of split events - signal electrons induced by a single photon distributed over more than one pixel - is decreased for hexagonal pixels (compared to quadratic pixels) because the ratio of the circumference to the pixel area is smaller. In order to have at least one hexagonal pixel located in a representative environment, compared to the final pixel matrix, the prototype structures have been realized in seven-cell clusters where the central pixel is surrounded by six neighboring pixels (Figure 4.1 (a)). In this arrangement, comparing spectroscopic measurements of the central and surrounding pixels can identify edge effects of a matrix that are possibly caused by the presence of guard rings close to the pixel.

Also, the size of the prototype structures corresponds exactly to the pixel size in the final DSSC sensor and is 272 μm x 236 μm. Because of the large resulting pixel area, two drift rings have been implemented around the DEPFET in the pixel center. During operation, the drift ring bias becomes more negative with increasing distance to the DEPFET. This

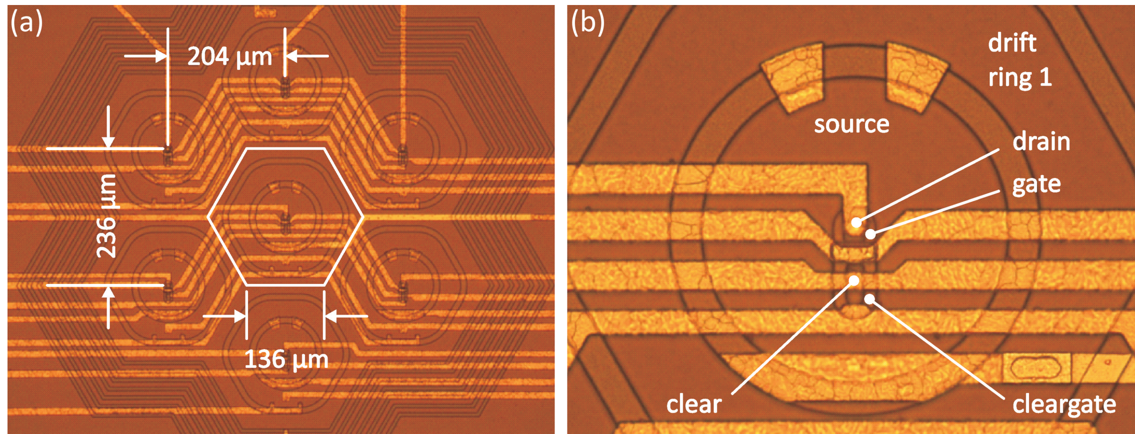

Figure 4.1: *Microphotographs of a DSSC prototype device: seven-cell cluster (a) and a close-up of the central cell's DEPFET (b). The pixel format is identical and the DEPFET layout is similar to the final DSSC device.*

results in a funnel-like potential that guides the bulk electrons toward the internal gate in the pixel center. The drift rings therefore guarantee a complete charge collection in the internal gate and minimize the related time requirements.
Two polysilicon drift gates provide spatial separation for both the drift rings as well as the source from the inner drift ring. The radii of the drift rings are already identical to the final DSSC layout and the layout variations for prototype production mainly refer to the DEPFET amplifier in the pixel center. The production technology and layout of the realized prototype structures will be described in detail in the following sections.

4.1.1. Technology

The first prototypes of DEPFETs with nonlinear amplification have been fabricated within the framework of the multi-project run PXD7. As the technology was dictated by the driving projects of the fabrication, in particular MIXS and IXO [63], only the p^+ implantation of the source in the overflow region (PSON) could be optimized for the DSSC prototypes.
Figure 4.2 illustrates the positioning of the four crucial implantations in the pixel center, which are required to form a potential minimum for electrons under the external gate (central region of the internal gate) and to create an overflow region for electrons under the source. In the region shown there is a homogeneous deep n implantation called NDXN. During operation it is fully depleted and the remaining positive space charge causes an attractive potential for electrons. In addition, three different p implantations partially compensate the NDXN.
The POXN implantation is a high-dose p implantation defining the drain and the contact area at the outer rim of the source. Its deep tails mostly compensate the NDXN so that almost no positive space charge remains. Hence, it laterally restricts the internal gate toward the pixel center as well as toward the inner drift rings at the outside.
Below the external gate there is only the channel implantation, which is used to trim the

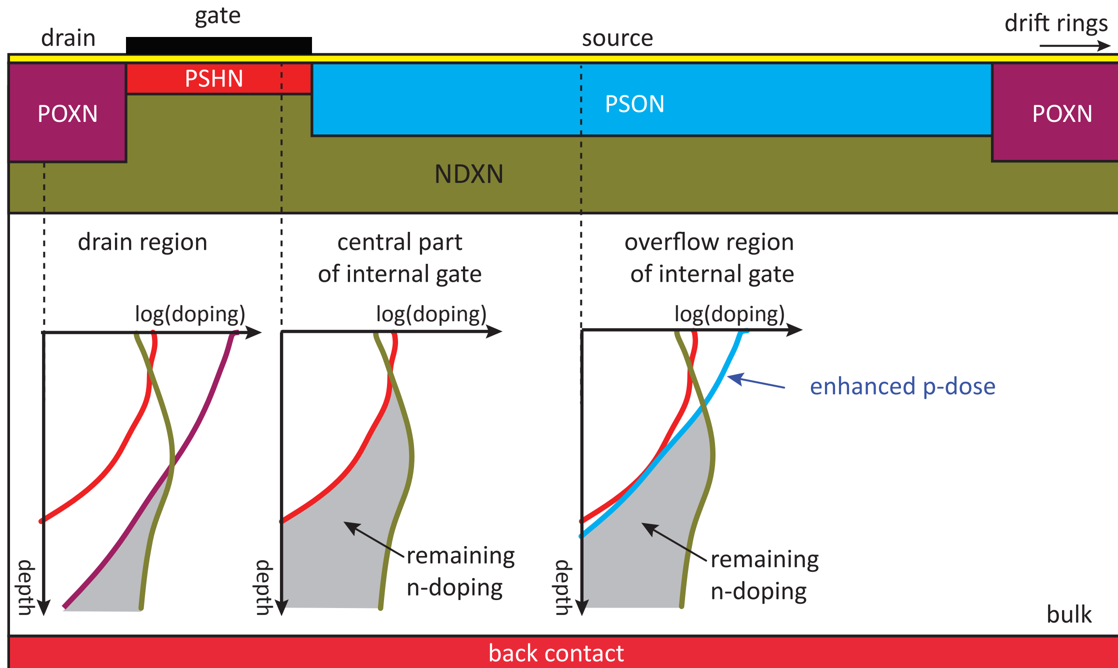

Figure 4.2: *Schematic of the implantation placements within the pixel center. The homogeneous deep n implantation NDXN is partially compensated by the p implantations beyond. The inserts show the 1D doping profiles for different regions on a logarithmic scale. The gray shaded area within each insert indicates the remaining n-doping concentration. The high-dose POXN implant compensates most of the NDXN and thus confines the internal gate. The highest n-doping concentration remains in the gate region due to the shallow, low-dose PSHN channel implant.*

threshold voltage of the transistor. This so-called PSHN is a shallow, low-dose implant resulting in very limited compensation of the NDXN. As the density of positive space charge is consequently highest underneath the external gate, this region exhibits the most attractive potential for electrons and hence forms the central part of the internal gate. Toward the source, this central part is restricted by the onset of the source implantation, termed PSON. Compared to the POXN implant, the PSON is reduced in depth and dose but it partially compensates the NDXN. This causes a reduction of the positive space charge under the source, when compared to the channel region, and thus leads to a potential step at the edge of the two regions of the internal gate. The outcome of the described implantations is a potential distribution as shown in Figure 4.3.

By reducing either the dose or the energy of the PSON implantation, the potential step between the central and the overflow region can be decreased and the onset of signal compression can be shifted toward smaller energies. However, there are two constraints for the PSON implantation. On the one hand, a PSON implantation that is too weak would lead to a resistivity of the source implantation that is too high, thus involving a voltage drop over the source when the DEPFET is on. Because of capacitive coupling of the source implantation to the internal gate, a side maximum in the electrostatic potential

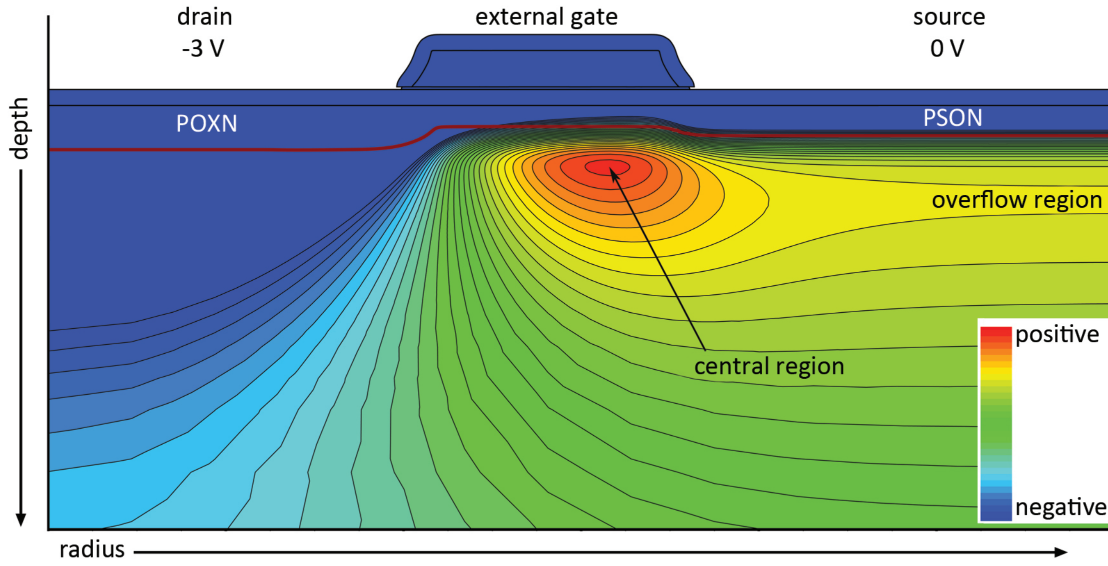

Figure 4.3: *Simulated electrostatic potential for a DSSC-DEPFET prototype in the vicinity of the external gate. The POXN and the PSON implantation form a potential minimum for electrons directly underneath the FET. Due to the negative potential of the drain in the pixel center the potential minimum is not centered with respect to the transistor channel but shifted toward the more positive source.*

can appear in the overflow region and cause an incomplete collection of bulk-generated charge and hence inhibits a proper operation of the DEPFET sensor. On the other hand, a very strong PSON implantation would overcompensate the NDXN, resulting in a linear amplification of the DEPFET even for high signals and making the signal compression unobservable. The process and device simulations shown here were what drove the choice of technological parameters and geometry for the devices. For prototype production the PSON implantation was optimized to achieve a potential step of roughly 1V between the central and overflow regions. For the average gate area of the realized variants this leads to an onset of signal compression at an energy deposition of roughly 100 keV, i.e., 100 X-rays of 1 keV.

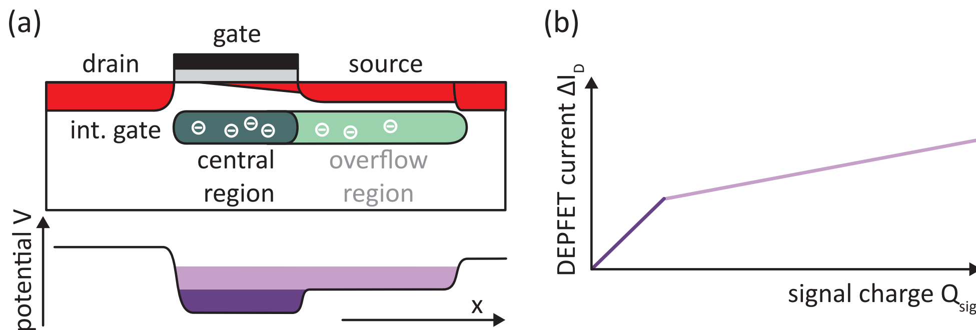

Figure 4.4: *Schematic of implantation placements and electrostatic potential within the internal gate of a DSSC-DEPFET prototype (a). The homogeneous overflow region leads to a basic nonlinear response curve with two different gains (b).*

Figure 4.4 illustrates the basic structure of the DSSC-DEPFET prototypes. Due to the technological constraints of the prototype production, only a homogeneous overflow region could be created. For small signals, all electrons generated accumulate in the central part of the internal gate and thus have a high steering effect on the transistor current.
Once the potential step toward the overflow region is equalized, additional electrons will spread over the entire internal gate causing a compression of the output signal. Due to the homogeneous potential in the overflow region only two different gains and thus only a basic nonlinear response curve could be obtained for the first prototypes. However, they allow for the validation of the general signal compression mechanism and for the study of different layout variants including their impact on amplification properties.

4.1.2. Layout

The DEPFET sensors are processed using a CMOS-like technology comprising two aluminum metalization layers for wiring and two overlapping polysilicon layers for the MOS gates of the DEPFET transistors. The clear gate is implemented in the first (POLY1) and the gate is created by the second polysilicon layer (POLY2), which is deposited after oxidation of POLY1 to have an electrical isolation in between. Therefore, only the POLY2 area with no POLY1 underneath it, defines the area of the FET channel and thus also the area of the central region of the internal gate. Figure 4.5 illustrates the first group of DSSC-DEPFET prototype layouts comprising the CG, SG and NG variant.
These variants have a clear gate completely enclosing the clear contact in its center. The clear structure is used to remove all electrons from the internal gate into the clear contact. In this design, an additional n^+ contact called "the inner substrate" (IS) is required and located in a gap within the p^+-doped inner drift ring of each pixel. The IS serves as a sink electrode for electrons generated at the Si-SiO_2 interface in the nonimplanted regions between the source and the drift rings. Without the IS, surface-generated electrons would contribute to leakage current and limit the maximum voltage difference that can be applied between source/ring1 and ring1/ring2. The combination of clear structure and IS represents the traditional design for DEPFET pixels with drift rings that will, for example, be used in the DEPFET detector system for the MIXS instrument on the BepiColombo mission (see chapter 3.5).

	DEPFET gate			overflow region
variant	$L[\mu m]$	W $[\mu m]$	A_{gate} $[\mu m^2]$	$A_{overflow}$ $[\mu m^2]$
CG	5	36	209.0	4847
SG	3	29	87.0	4812
NG	3	9	27.0	4806

Table 4.1: *Summary of some geometry parameters for the three variants with the traditional clear gate design.*

The gate length L, the gate width W and the resulting gate area A_{gate} as well as the area of the overflow region $A_{overflow}$ are summarized in Table 4.1.
The definition of the gate width of variant CG is not unambiguous because the gate length cannot be defined in the overlap region of the polysilicon layers, i.e., the area between the dashed lines in Figure 4.5. However, this region will not be very attractive for electron due to its proximity to the negative clear gate and hence it is not considered in the gate width W.

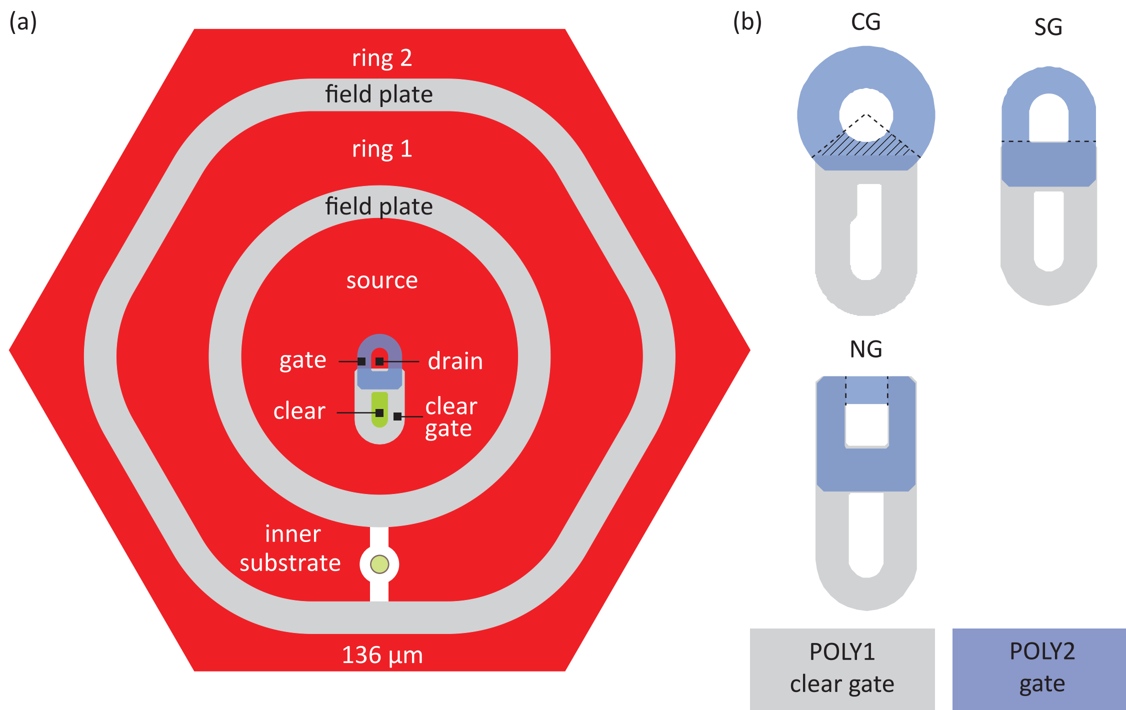

Figure 4.5: *Basic pixel layout of the variants with traditional clear gate design (a). Two drift rings enclose the DEPFET in the pixel center. Electrons generated at the oxide interfaces underneath the drift gates are extracted by the inner substrate contact located in the nonimplanted notch in the inner drift ring. The DEPFET variants in the traditional clear gate design (b): CG, SG and NG.*

The second group of prototype structures comprising the variants DR270, DR180, DR90 and DR60 has a completely different clear gate design and is shown in Figure 4.6. The clear gate is split at the lower end and the clear implantation is extended towards the inner drift ring (a). This completely new design allows the clear structure to extract not only electrons from the internal gate but also surface-generated charge from the regions under the drift gates and move them into the clear contact. The IS can therefore be omitted in the new clear gate design which lowers the number of required contacts per pixel. In large pixel matrices this can be an advantage because it reduces the number of wirings on the sensor and relaxes the layout of the metalization layers.
According to the traditional clear gate design, the main differences between the variants relate to the area of the external gate of the DEPFET. The area scaling is created by

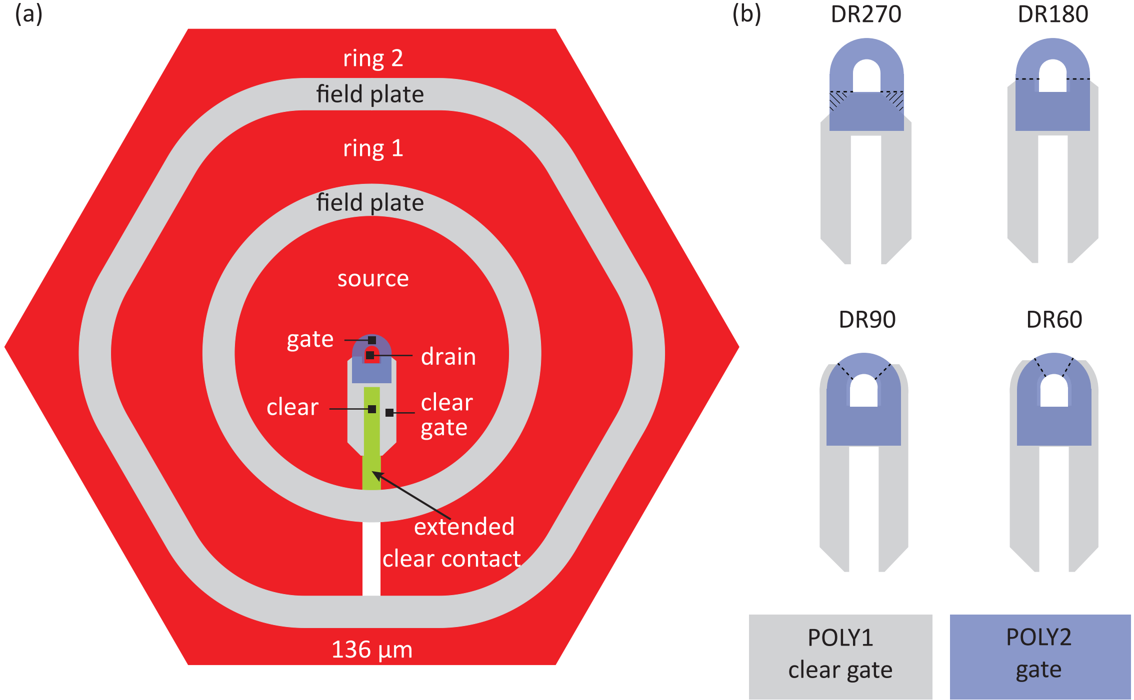

Figure 4.6: *Basic pixel layout of the variants with new clear gate design (a). Two drift rings enclose the DEPFET in the pixel center and the surface generated leakage current from the oxide interfaces underneath the drift gates is drained via the extended clear contact. (b) The DEPFET versions created with various opening angles featuring the new clear structure.*

changing the opening angle of the transistor between 60 and 270 degrees. Table 4.2 summarizes the gate length L, the opening angle of the transistor α, the gate width W and the resulting gate area A_{gate} as well as the area of the overflow region $A_{overflow}$.

Like the CG variant, the gate length of variant DR270 cannot be defined close to the clear gate. However, because of the negative clear gate nearby, the electrostatic potential in this region is reduced and thus only the area between the dashed lines is considered for the gate width W.

	DEPFET gate				overflow region
variant	L [μm]	$\alpha_{transistor}$ [°]	W [μm]	A_{gate} [μm^2]	$A_{overflow}$ [μm^2]
DR270	3	270	25	82.2	5625
DR180	3	180	16	50.7	5625
DR90	3	90	8	27.2	5533
DR60	3	60	5	18.8	5537

Table 4.2: *Summary of some geometry parameters for the four variants exhibiting the new clear gate design.*

4.2. Experimental setup

A new single pixel measurement setup was established for measurements on the DSSC prototype structures. The setup was optimized for operating and characterizing test structures with a wide range of requirements. The test devices are mounted on a 40-pin ceramic carrier allowing for easy connection with a ZIF socket (zero insertion force) on the mainboard and for quick exchange of the device being tested (DUT). A block diagram of the new setup is shown in Figure 4.7.

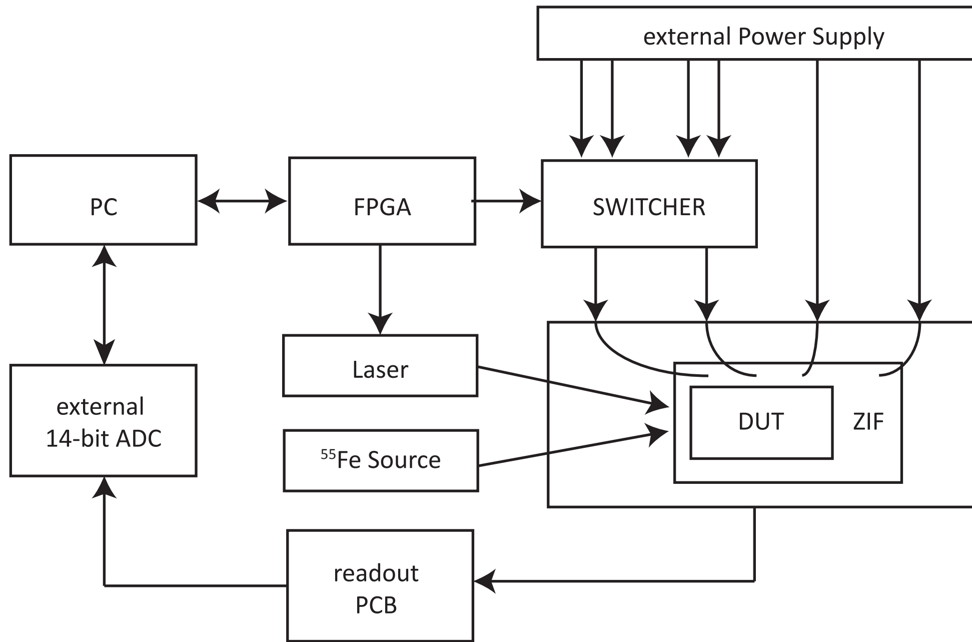

Figure 4.7: *Block diagram of the new measurement setup.*

The required supply voltages for all electronic components and the operation of the DUT are generated by external power supplies and connected to the mainboard, where they are distributed. Static supply voltages are directly connected to a ZIF socket using variable cable connections. The dynamic supply voltages, for example for the clear and the clear gate of the DEPFET, are generated by four dedicated SWITCHER steering ICs [40] located on the mainboard. A SWITCHER has two identical ports, each consisting of two inputs for analog voltages and 64 analog outputs. Controlled by digital signals, the SWITCHER can connect every analog output to one of the two input voltages of the corresponding port and can therefore generate all required clocked voltages for the DUT. The four SWITCHERs can provide eight dynamic voltages allowing for the operation of all available test structures. The analog outputs can also be connected to the ZIF socket by variable cable connections, thereby permitting the use of any pin configurations on the ceramic carrier.
The digital signals for steering the SWITCHERs or triggering other components such as a pulsed laser are generated by an FPGA. By configuring this FPGA, arbitrary measurement sequences of varying complexities can be created. The granularity of the time intervals is defined by the FPGA's 80-MHz clock, which corresponds to time steps of 12.5 ns.

To provide maximum flexibility, an exchangeable readout board has been installed to allow for either a source follower readout using an ASTEROID [41,42] or a discrete drain readout circuit. Because the DSSC-DEPFETs are designed for drain readout, a transimpedance amplifier board as shown in Figure 4.8 was used for all measurements in this thesis.

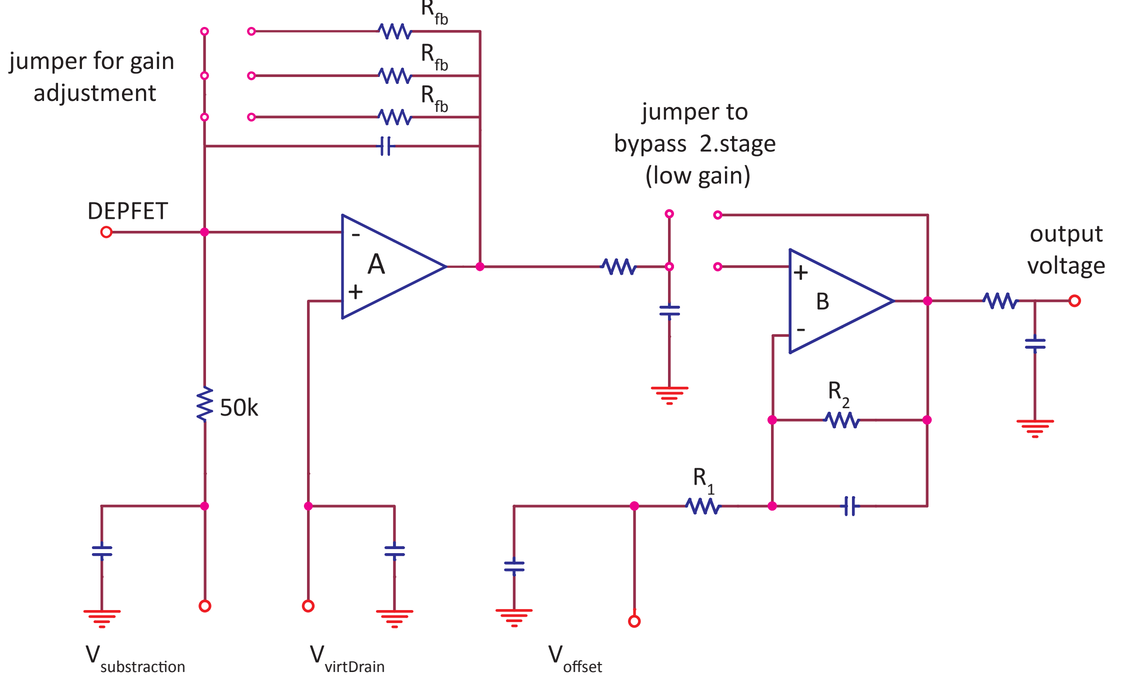

Figure 4.8: *Schematic of the two amplifying stages of the current readout board used for the measurements on the DSSC prototypes.*

In this configuration the DEPFET drain is connected to the negative input of the first op-amp (A) and is kept at a static potential that is adjustable by the external voltage $V_{virtDrain}$. In addition, the DEPFET drain is connected to the $V_{substraction}$ voltage using a resistor. $V_{substraction}$ is more negative than the drain potential and is used to sink the bias current of the DEPFET. Hence, only the DEPFET current due to signal electrons in the internal gate flows over the feedback resistors of the first amplifying stage, and causes a voltage drop across it. Because the first amplifying stage is a transimpedance amplifier, it converts a change of the drain current into a voltage step at the output node of the op-amp (A) according to

$$U = \Delta I_D \cdot R_{fb}. \tag{4.1}$$

Gain from the first amplifying stage can be increased with the feedback resistor and output voltage can either be directly connected to the ADC or further amplified by the second stage. The second amplifying stage is realized as a noninverting amplifier that offers a gain of

$$G = 1 + \frac{R_2}{R_1}. \tag{4.2}$$

Three different readout boards were used for the performed measurements, offering current-

to-voltage gain settings between 50 $\frac{mV}{\mu A}$ and 750 $\frac{mV}{\mu A}$. The analog output voltage from the readout board is digitized by using an external 14-bit ADC with an input range of 2 V providing an ADC conversion factor C_{ADC} of

$$\frac{1}{C_{ADC}} = \frac{2\ V}{2^{14}\ \mathrm{ADU}} = 122\ \frac{\mu\mathrm{V}}{\mathrm{ADU}}. \tag{4.3}$$

Therefore, the overall readout conversion factor C_{ORC} is taken from

$$C_{ORC} = R_{fb} \cdot G \cdot C_{ADC}.$$

For the readout boards used, C_{ORC} varies between 0.41 $\frac{ADU}{nA}$ and 6.1 $\frac{ADU}{nA}$. After digitalization the data is transferred to a PC for storage and offline analysis. Since the readout gain has been optimized for measurements of different prototypes, the resulting digital values measured have always been converted into a drain current change using the overall readout conversion factor C_{ORC}. The drain current change is independent of the setup and hence allows for the comparison of different DEPFET variants.

4.3. Nonlinear response curve

The following section deals with the nonlinear response curve of DSSC-DEPFET prototypes. First, the measurement sequence for determining the nonlinear gain curve using an external laser is presented before the impact of the geometry and the supply voltages on the nonlinear gain curve is discussed on the basis of experimental results and device simulations.

4.3.1. Validation of nonlinear amplification

The characterization of the nonlinear response curve of the DSSC-DEPFET prototypes requires an option to generate a reproducible number of signal electrons in the active volume of the examined pixel. One option is to use a pulsed, optical laser and to illuminate the DEPFET sensors through the irradiation entrance window. Since standard DEPFET sensors are provided with a thin aluminum layer as a light-blocking filter on top of the backside diode, this was omitted for prototype structures in order to avoid the reflection of optical laser light and thus allow for unimpeded penetration into the active volume of the DEPFET sensors.
A red diode laser with an wavelength of 532 nm was used for the measurements. The laser can be pulsed via an external trigger signal coming from the FPGA of the measurement setup (compare section 4.2). The laser generates signal charge at an arbitrary moment in time within a very short time interval. Additionally, the amount of signal charge can be adjusted by the length of the laser pulse and its intensity. Even if the absolute number of signal charges is unknown a priori, it can be determined by comparative measurements

with a radioactive source.
Figure 4.9 illustrates the measurement sequence for scanning the nonlinear detector response using an external laser. The baseline is sampled after a complete removal of signal charge from the internal gate by applying positive voltages to the clear and the clear gate. Subsequently, the DEPFET pixel is exposed repeatedly to short laser pulses that generate signal charge in the active volume. In contrast to irradiation with a radioactive source, charge generation is not localized but evenly spread over the entire pixel area because the laser spot size is several mm^2. Due to the location-dependent charge collection time needed for the collection of the signal charge in the internal gate, the increase of the transistor current is generally slow - for DSSC-DEPFET prototype structures it is several hundred ns. Additionally, the current rise time is extended by the fact that the duration of the laser pulse itself is also in the sub-μs range.

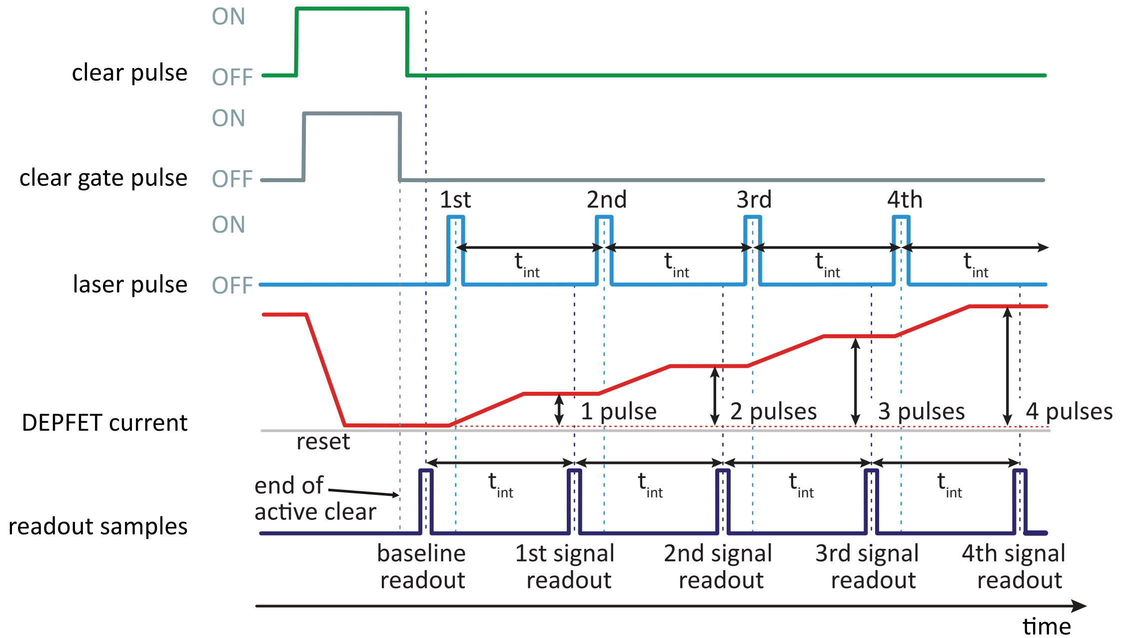

Figure 4.9: *Illustration of the measurement sequence using an external laser to scan of the nonlinear response curve of the DSSC-DEPFET.*

The so-called integration time t_{int}, i.e., the time between two sample points, has to be long enough so that the total charge Q_{laser} generated due to the laser pulse anywhere in the active volume of the pixel under investigation can be completely collected in the internal gate. Another contribution to the signal charge in the internal gate is the leakage current of the pixel area thermally generated within the integration time. Because the leakage current $I_{leakage}$ in a DEPFET is independent on the fill level of the internal gate and thus is constant in time, the accumulated charge ΔQ_{int} in the time interval between two sampling points is given by:

$$\Delta Q_{int} = I_{leakage} \cdot t_{int} + Q_{laser}$$

For DEPFET sensors the leakage current at room temperature is only around 100 pA/cm^2 corresponding for the given pixel size to roughly three electrons within a 10 μs integration time. Because this is generally much less than the laser-generated charge, in Figure 4.9 the DEPFET current is shown to be constant between the complete arrival of the charge due to the last laser pulse and the pulse that follows. However, it is important that the integration time t_{int} is the same for all subsequent laser pulses in order to have a constant contribution from leakage current. This guarantees consistent measurement results even for bright pixels, with a high leakage current due to technology imperfections, and allows for highly precise measurements. If this condition is fulfilled, as shown in Figure 4.9, the number of laser pulses can be increased arbitrarily and the nonlinear response curve can be scanned. The granularity of the scan can be adjusted by the amount of charge generated within the time interval between two sampling points.
Figure 4.10 shows an example of a measurement using 32 laser pulses to scan the nonlinear DEPFET response. As indicated in Figure 4.9, the DEPFET current was sampled after every laser pulse. Each signal difference to the common baseline is represented as an individual spectrum with a single peak. The resulting 32 spectra are color-coded and the DEPFET output signal is given in ADU since the spectra are still uncalibrated.

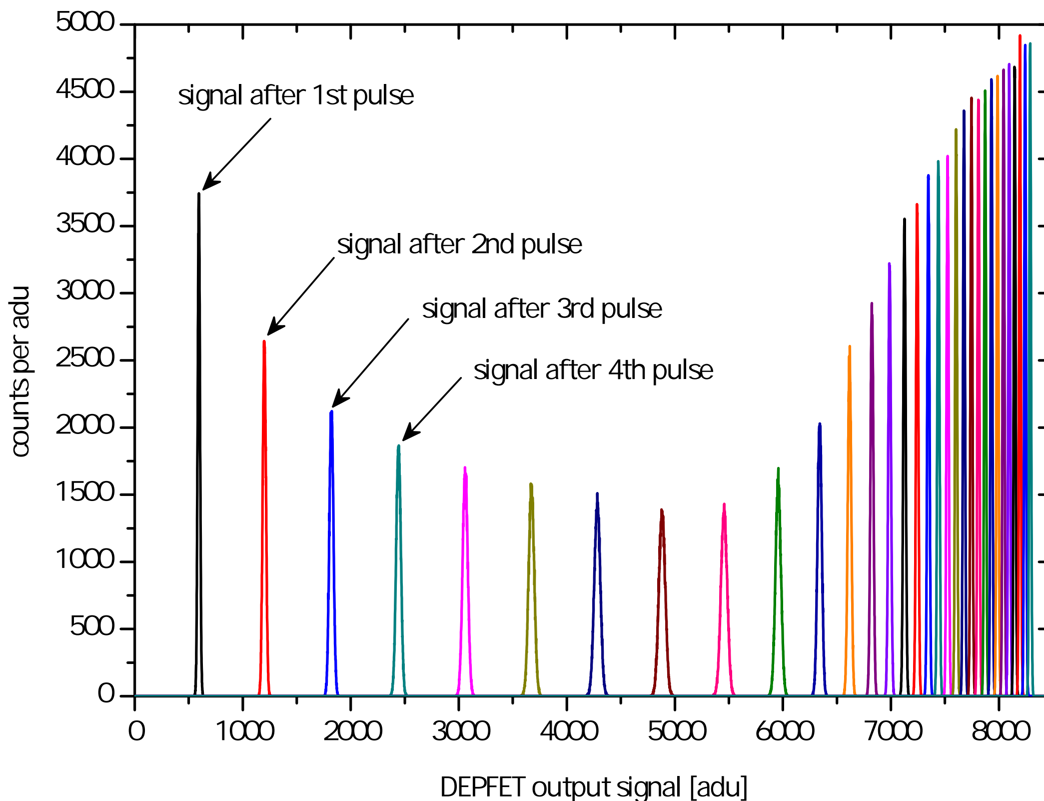

Figure 4.10: *Measured spectra of the irradiation with an external pulsed laser. The different pulses are color-coded and the DEPFET output signal in ADU corresponds to the signal difference between the corresponding signal sampling and the baseline.*

Due to the linear amplification of the DSSC-DEPFET for small energies and the constant number of signal electrons generated within the integration time t_{int} by a single laser pulse and the leakage current, the first nine peaks are distributed equidistantly. For subsequent laser pulses, the signal difference between the peaks is significantly smaller. This transition, shown in Figure 4.10 in the range between 6000 and 7000 ADU, is due to the ensuing overflow of signal electrons under the source and indicates the end of the linear amplification of the response curve.
Due to the Poisson statistics of the photon generation process in the laser, the half width of the peaks increases significantly with the amount of signal charge. As the number of events in each peak is constant, the height of the peaks decreases at first. The initial signal compression of the DSSC-DEPFET also leads to a compression of the half width and thus to a new increase in the peak height.

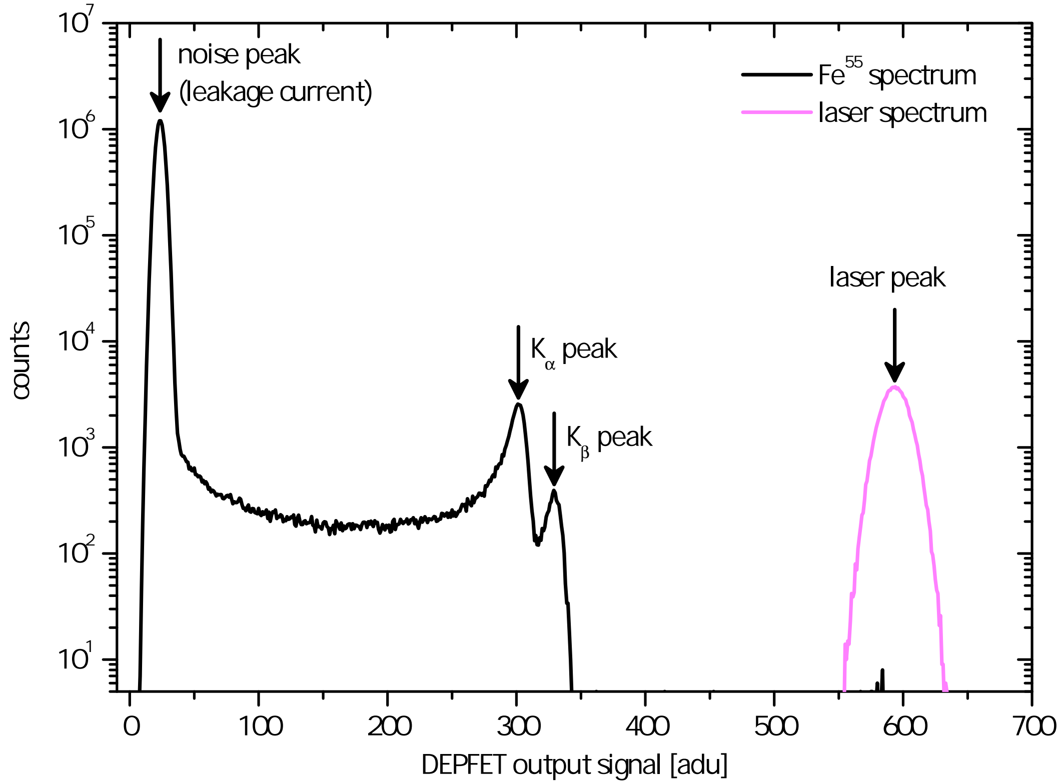

Figure 4.11: *Semi-logarithmic plot of measured spectra for the irradiation with a ^{55}Fe source (black) and with an external laser (magenta).*

The next step in determining the nonlinear response curve is to calibrate the amount of signal charge generated from the laser and the leakage current in the pixel within the integration time. To do this we can refer to the spectrum of the irradiation with an ^{55}Fe source and the spectrum obtained after the first laser pulse. Both spectra are shown in Figure 4.11.
The ^{55}Fe spectrum comprises three pronounced peaks. Due to leakage current within the

integration time of 50 μs the noise peak is located at about S_N=23 ADU. The K_α peak appears at S_{K_α}=302 ADU and the K_β peak at S_{K_β}=330 ADU. Compared to the noise peak, both signal peaks are significantly reduced in the peak height and also in the number of events within the peak. This indicates a small probability that an X-ray photon hits the pixel during a test. Nevertheless, a few pileup events are visible at the double K_α energy at about 582 ADU. From this value, a conversion factor from ADU to the number of signal electrons can be derived by:

$$\frac{N_e(K_\alpha)}{S_{K_\alpha} - S_N} = \frac{\frac{5894\ eV}{3.65\ eV/e^-}}{279\ ADU} = 5.80 \frac{e^-}{ADU}. \tag{4.4}$$

In contrast to the radioactive source, the laser hits the pixel in every readout cycle and therefore no noise peak occurs. The spectrum contains only a single peak at S_L=593 ADU given by the DEPFET output signal due to leakage current and the laser pulse.
According to equation 4.4, the average number of electrons generated between two sampling points can be calculated as follows:

$$N_e = S_L \cdot 5.80 \frac{e^-}{ADU} = 3439. \tag{4.5}$$

Hence, the average amount of signal charge generated during the integration time t_{int} corresponds to a hypothetical photon with an energy of 12.55 keV. This value defines the granularity of the scan of the response curve for the applied measurement sequence. The integrated energy deposition in the pixel after the nth laser pulse since the last clear is thus given by:

$$E_{dep}(n) = n \cdot E_{pulse} = n \cdot 12.55\ keV. \tag{4.6}$$

In order to specify the absolute calibration error, one needs to determine the error of the equivalent energy deposition of one individual laser pulse defined as

$$E_{pulse} = N_e(K_\alpha) \cdot w\ \cdot \frac{S_L}{S_{K_\alpha} - S_N}. \tag{4.7}$$

with $N_e(K_\alpha)$ the number of electrons generated by a K_α photon from a ^{55}Fe source and w being pair-generation energy in silicon. The measured variables are the individual peak positions: S_L for the laser peak, S_{K_α} for the K_α peak and S_N for the corresponding noise peak in the spectrum.
The systematic errors due to the uncertainties of w and of K_α energy, which are precisely known from literature, can be neglected. Since the measurement setup is optimized for high-precision measurements of the nonlinear response curve other systematic errors like nonlinearities of the readout board or the ADC are negligible as well. The dominant contribution to the calibration error arises from the precision of the determination of the three peak positions. These individual errors are statistical and in order to get the absolute calibration error they need to be added quadratically according to:

$$\Delta_{stat}E_{pulse} = \sqrt{\Delta S_L{}^2\left(\frac{\partial E_{pulse}}{\partial S_L}\right)^2 + \Delta S_{K_\alpha}{}^2\left(\frac{\partial E_{pulse}}{\partial S_{K_\alpha}}\right)^2 + \Delta S_N{}^2\left(\frac{\partial E_{K_{pulse}}}{\partial S_N}\right)^2}. \quad (4.8)$$

The partial derivatives in equation 4.8 are as follows:

$$\frac{\partial E_{pulse}}{\partial S_L} = n \cdot N_e \cdot w \, \frac{1}{S_{K_\alpha} - S_N} \quad (4.9)$$

$$\frac{\partial E_{pulse}}{\partial S_{K\alpha}} = n \cdot N_e \cdot w \, \frac{-S_L}{(S_{K_\alpha} - S_N)^2} \quad (4.10)$$

$$\frac{\partial E_{pulse}}{\partial S_N} = n \cdot N_e \cdot w \, \frac{S_L}{(S_{K_\alpha} - S_N)^2} \quad (4.11)$$

The laser peak as well as the noise peak have roughly a Gaussian shape and compared to the peak height the background is very low - or in the case of the laser not present at all. This allows for precise positioning of the peaks and therefore both ΔS_L and ΔS_N are very small and can be estimated to be ± 0.3 ADU. The main contribution to the calibration error comes from the determination of the K_α peak position of the ^{55}Fe source. Due to the high background and the related asymmetric peak shape, an accurate positioning is more difficult which leads to much higher uncertainties and a ΔS_{K_α} of roughly ± 2 ADU. An absolute calibration error of

$$\Delta E_{pulse} = 92 \; eV \quad (4.12)$$

can be obtained when using these values. For the given E_{pulse}, this corresponds to a relative error of below 1%. For finer granularity in the scan, this relative error will become larger as the absolute errors for the peak positions stay constant.

The last step in obtaining the nonlinear response curve is determining the exact position of all 32 laser peaks with regard to their output signals. Plotting these values against the corresponding energy deposition in the pixel we get a response curve as shown in Figure 4.12 for a single pixel in a seven-cell prototype cluster in the SG geometry.

In order to characterize the nonlinear response curve it is useful to calculate its first two derivatives as shown in the insert of Figure 4.12. The 1st derivative represents the slope and therefore also the charge-to-current amplification of the internal Gate of the DEPFET, typically labeled as g_q. Up to an equivalent energy deposition of roughly 90 keV, the g_q stays constant at 560 pA/e$^-$ before it drops steeply. For high energies, the g_q converges against a value below 50 pA/e$^-$ but still no constant value is reached at the end of the investigated energy range up to 420 keV.

Another parameter that can be extracted from the 1st derivative is the so-called compression factor of the nonlinear response curve C_{comp} defined as

$$C_{comp} = \frac{g_q^{lin}}{g_q^{comp}}. \quad (4.13)$$

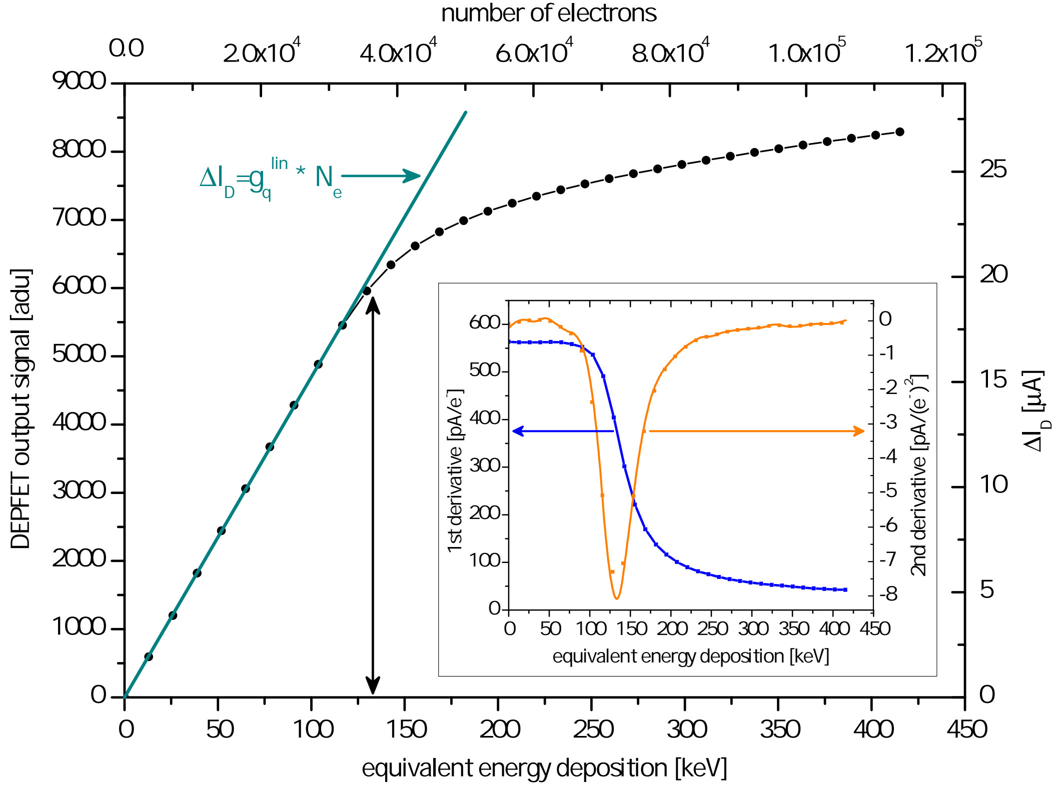

Figure 4.12: *Measured nonlinear response curve of one pixel in a seven-cell cluster in SG geometry. The insert depicts its first two derivatives. The 1st derivative (blue) corresponds to the amplification of the DEPFET and the minimum of 2nd derivative (orange) is used to define the onset of signal compression.*

It describes the ratio between the amplification for small energies g_q^{lin} and that for high energies g_q^{comp}. Even if the amplification is strongly energy dependent, g_q^{comp} generally refers to the value it converges against for high energies, which makes it possible to specify an energy-independent value for C_{comp}.

The second derivative of the response curve characterizes its bending. The minimum of the second derivative is used within the framework of this thesis to determine a mathematically unambiguous definition of the onset energy for the signal compression E_{kink}.

parameter	value
g_q^{lin}	560 pA/e$^-$
g_q^{comp}	45 pA/e$^-$
C_{comp}	12
E_{kink}	133 keV

Table 4.3: *Extracted figures of merit for the nonlinear response curve shown in Figure 4.12.*

In principle, other definitions would also be possible but the minimum of the second derivative occurs precisely when the potential distribution of the internal gate shows the

most significant change in terms of the area of the isoelectric potential minimum for signal electrons. For the given example, the figures of merit are listed in Table 4.3.

4.3.2. Measurements on layout variants

For optimizing the nonlinear response curve of DSSC-DEPFETs it is essential to know how the device performance depends on the pixel layout. For this reason, all variants have been tested and their characteristics have been investigated in detail. As far as possible, all available DSSC-DEPFET prototypes have been operated with standardized supply voltages in order to improve the comparability between the nonlinear gain curves for different layouts - even if the optimal spectroscopic performance could not be attained for all variants. The impact of the individual operation voltages on the amplification properties is discussed in section 4.3.3.

	variant						
parameter	CG	SG	NG	DR270	DR180	DR90	DR60
V_{DS} [V]	-3.0	-3.0	-3.0	-3.0	-3.0	-3.0	-3.0
V_{GS} [V]	-3.4	-3.1	-1.4	-3.4	-3.8	-2.1	-2.0
I_D [μA]	100	100	4	100	100	8	7
V_{CL}^{high} [V]	17.5	17.5	20.0	17.5	17.5	17.5	17.5
V_{CL}^{low} [V]	2.5	2.5	2.5	2.5	2.5	2.5	2.5
V_{CG}^{high} [V]	5.0	5.0	6.5	5.0	5.0	5.0	5.0
V_{CG}^{low} [V]	-2.5	-2.5	-2.5	-3.5	-3.5	-3.5	-3.5
V_{R1} [V]	-15.0	-15.0	-15.0	-15.0	-15.0	-15.0	-15.0
V_{R2} [V]	-25.0	-25.0	-25.0	-25.0	-25.0	-25.0	-25.0
V_{BC} [V]	-100	-100	-100	-100	-100	-100	-100

Table 4.4: *Overview of the relevant DEPFET operation parameters used for the measurements of different layout variants. The shown voltages are referred to the DEPFET source potential.*

Table 4.4 summarizes the drain current as well as all relevant supply voltages applied to the prototypes during irradiations with an radioactive ^{55}Fe source or an external pulsed laser.

The gate voltage V_{GS} has been adjusted to a drain current of roughly $I_D \approx 100$ μA in order to compensate for variations of the width and length of the DEPFET gates for the different layout variants and thus to allow for the analysis of the internal amplification of each structure. Since the DEPFET is in the on-state, a conductive layer of freely moving holes is located underneath the external gate forming the transistor channel and shielding the internal gate from the negative potential of the external MOS gate. As a result, potential distribution beneath the transistor channel, which is responsible for the nonlinear detector response, is independent on gate voltage as long as the transistor is switched on. Measurements as well as device simulations have confirmed this behavior.

As shown in Table 4.4, there are three deviations from the standard voltage set:

- V_{CG}^{low} has been decreased for the new variants with the open clear gate structure compared to the traditional variants in order to strengthen the potential barrier encapsulating the clear contact and thus reduce the loss of signal charge during the integration phase.
- V_{CL}^{high} and V_{CG}^{high} have been increased for the NG variant to enhance its clear capability.
- I_D has been reduced for devices with small gate widths (NG, DR60 and DR90) in order to limit the voltage drop within the source implantation. This is due to its finite sheet resistance and the high current density close to the channel.

4.3.2.1. Traditional variants

Figure 4.13 shows the measured nonlinear response curves of all individual pixels for a single seven-cell cluster of the NG, SG and CG variant. Each curve is obtained with the measurement procedure described in the previous section: a scan of the detector response with an increasing number of laser pulses and an absolute energy calibration with an ^{55}Fe source.
The curves for different variants are well separated since the onset energy of signal compression is lowered by the reduction of the gate area. This is due to the smaller volume of the central portion of the internal gate and the related decrease in its charge handling capacity. All variants show pixel-to-pixel inhomogeneities of up to 10% [64]. For representative specifications all measured curves have been analyzed separately and the extracted parameters are averaged for each variant. Table 4.5 summarizes the gate area A_{gate}, the onset energy of signal compression E_{kink}, the charge handling capacity of the central portion of the internal gate per gate area C_{IG}, and the measured sensitivity of the internal gate in the linear region $g_q^{measured}$.

	L	W	A_{gate}	E_{kink}	C_{IG}	$g_q^{measured}$	g_q^{theory}
variant	[μm]	[μm]	[μm^2]	[keV]	[$e^-/\mu m^2$]	[pA/e$^-$]	[pA/e$^-$]
NG	3	9	27.0	39.5	401	247	196
SG	3	29	87.0	134.1	422	540	546
CG	5	36	209.0	670.8	879	227	(227)

Table 4.5: *Overview of the gate area A_{gate}, the onset energy of signal compression E_{kink}, the charge handling capacity of the internal gate per gate area C_{IG}, and the measured and theoretical sensitivity of the internal gate $g_q^{measured}$ and g_q^{theory} for the NG, SG and CG variant.*

For the variants SG and NG, the average capacity of the central portion of the internal gate per gate area is roughly 400 e$^-$/μm^2. The significantly higher charge handling capacity for the CG variant of 879 e$^-$/μm^2 shows that the kink energy does not simply scale with the

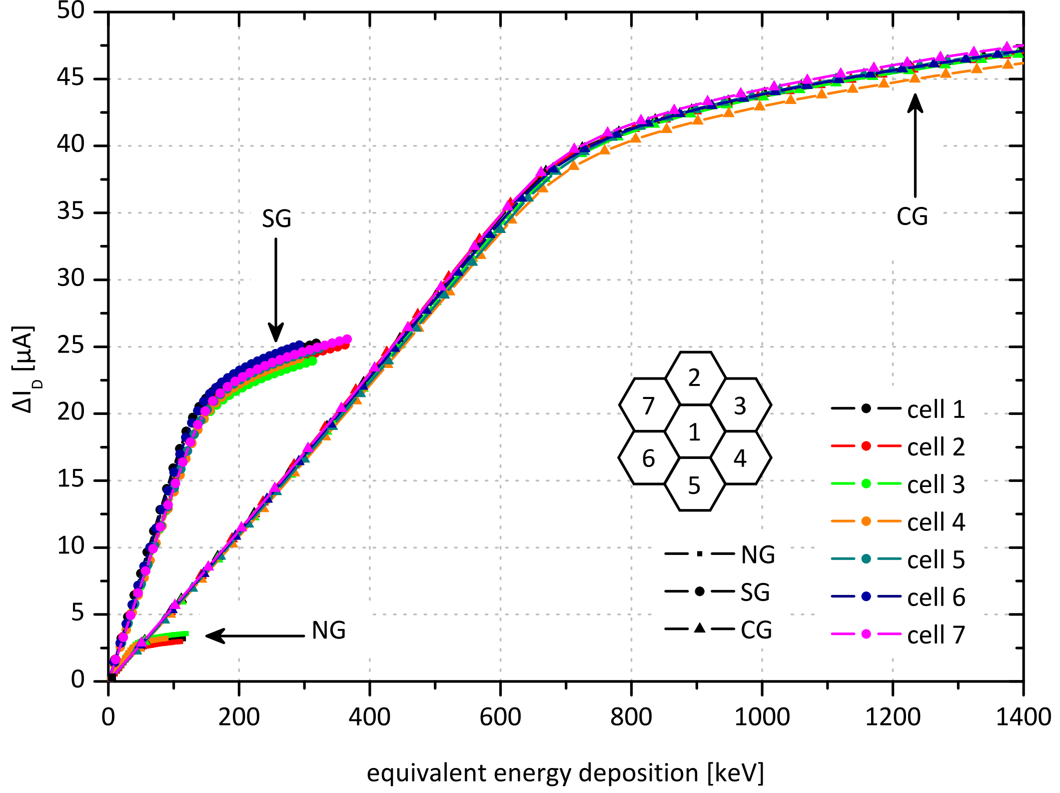

Figure 4.13: *Nonlinear gain curves measured for DSSC prototypes with traditional clear gate design using a series of calibrated laser pulses. The symbols in the curves mark the individual laser pulses and the different symbols represent various layout variants. The curves for individual pixels of the seven-cell clusters are color-coded.*

gate area. The increased gate length of 5 μm deepens the internal gate's potential valley and thus increases the potential step between the central part and the overflow region of the internal gate, which leads to delayed overflow of the signal electrons in the source region.

The charge transconductance of the internal gate g_q, i.e., the sensitivity of the transistor current I_D to signal charges Q_{sig}, can be calculated based on the analytical DEPFET model proposed by J. Kemmer et al. [32].

$$g_q = \frac{dI_D}{dQ_{sig}} = \sqrt{\frac{2\mu_p I_D}{WL^3 C_I}} \tag{4.14}$$

Here μ_p denotes the hole mobility in the transistor channel, W the width, L the length of the transistor channel and C_I the gate insulator capacitance per unit area.
The capacitance of the DEPFET's gate insulator can be modeled as a series circuit of plate capacitors matching the capacitance of oxide and nitride.

$$\frac{1}{C_{ins}} = \frac{1}{C_{ox}} + \frac{1}{C_{nit}} \tag{4.15}$$

$$C_{ox/nit} = \epsilon_r \cdot \epsilon_o \cdot \frac{A}{d} \tag{4.16}$$

An insulator capacitance of C_{ins}=1.76 $\cdot 10^{-4}$ $\frac{\mathrm{F}}{\mathrm{m}^2}$ can be calculated for PXD7 production using the relative dielectric constants ϵ_{ox}=3.9 for silicon dioxide and ϵ_{nit}=7.5 for silicon nitride.
Hole mobility in the transistor channel is required in order to demonstrate device performance scaling with the gate dimensions and test the model from equation 4.14 against measured data. Mobility depends strongly on doping concentration and trap density at the Si-SiO_2 interface. Because these technology-dependent parameters are a priori unknown, hole mobility has to be determined from measurement results and is considered to be constant for all devices in PXD7 production. Based on equation 4.14 and the g_g value measured for the CG variant, we can derive a hole mobility of $\mu_p = 80\ \frac{cm^2}{Vs}$. Compared to literature, this value is much smaller than the bulk mobility of holes in silicon ($\approx 450\frac{\mathrm{cm}^2}{\mathrm{Vs}}$), but it seems plausible since the doping concentration in the channel is roughly $1 \cdot 10^{17}\frac{1}{\mathrm{cm}^3}$ [65] and the maximum current density is close to the Si-SiO_2 interface exhibiting a higher trap density compared to the bulk.
The theoretical values for internal gate transconductance g_g^{theory} resulting from this hole mobility are shown in Table 4.5. The agreement with measured values is very good for the SG variant, but deviations of more than 20 % occur for the NG version even if the reduced drain current is considered. These deviations from the analytical model may be caused either by the linear geometry of the NG transistor or by the very small gate width.

4.3.2.2. New variants

Figure 4.14 shows the nonlinear response curves of representative seven-cell clusters in each of the four variants with the open clear gate structure. Similar to above, the kink between the linear and the compression region occurs at higher accumulated energy for large gate devices.
The average capacity of the internal gate per unit area is in the range of 360 to 440 $\mathrm{e}^-/\mu\mathrm{m}^2$. The capacity of the DR180 variant is comparable with the SG variant and it shows up that a reduction of the gate width not only decreases the absolute E_{kink} but also the area-normalized charge handling capacity C_{IG} of the internal gate (see Table 4.6). This gate width dependence indicates upcoming 3D effects, which will be investigated in detail by 3D device simulations in the following sections. This also explains the low C_{IG} of 364 $\mathrm{e}^-/\mu\mathrm{m}^2$ measured for the DR270 variant.
Like for the traditional variants, the analytical model of equation 4.14 can be applied to calculate the sensitivity in the linear region. A good agreement with the measured values is obtained for large gate devices and a relative error of less than 15% is achieved for the DR270 and DR180 variants conducting a current of 100 μA. However, prediction

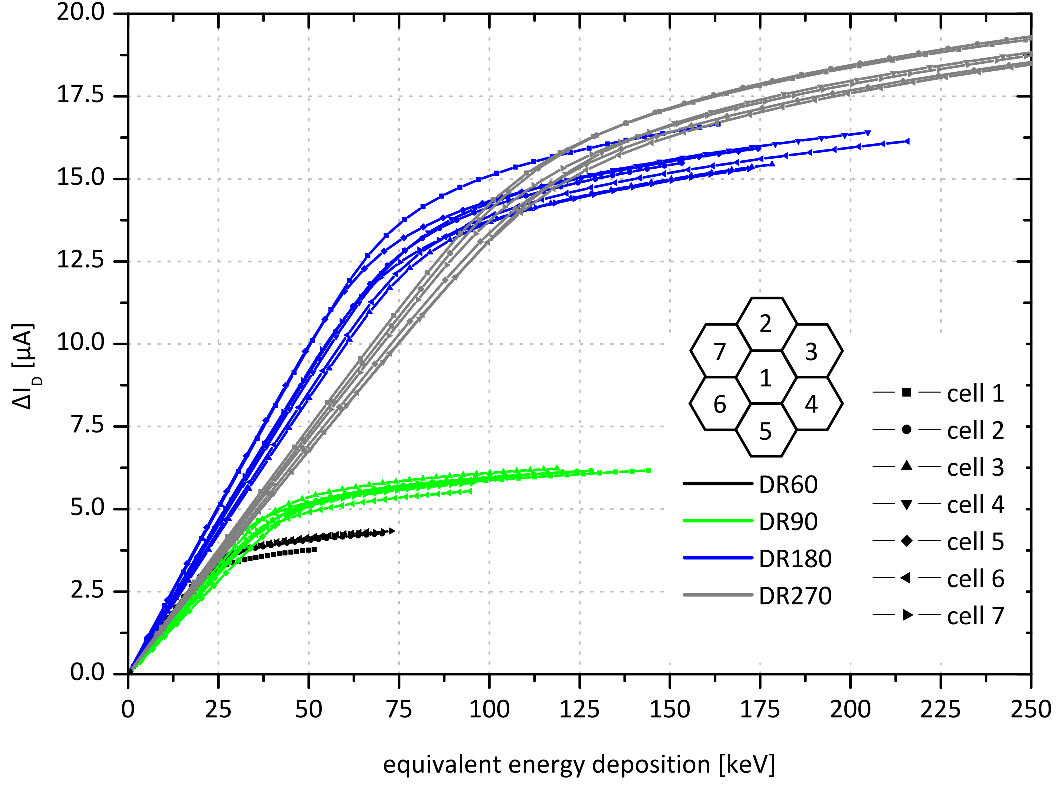

Figure 4.14: *Nonlinear gain curves measured on DSSC prototypes with open clear gate structure using a series of calibrated laser pulses. The symbols in the curves mark the individual laser pulses and the variants are color-coded. The curves for individual pixels of a seven-cell clusters are indicated by different symbols.*

accuracy becomes worse for smaller gate widths, and the relative error already exceeds 50% for the DR60 variant. It should be noted at this point that the biggest discrepancies occur for variants that exhibit a very small gate widths (DR60, DR90 and NG) and that are operated at a reduced drain current of much less than 100 μA. This again indicates upcoming 3D effects that are not included in the simplified analytical model and hence limit its applicability.

	L	W	A_{gate}	E_{kink}	C_{IG}	$g_q^{measured}$	g_q^{theory}
variant	$[\mu m]$	$[\mu m]$	$[\mu m^2]$	[keV]	$[e^-/\mu m^2]$	[pA/e$^-$]	[pA/e$^-$]
DR60	3	5	18.8	24.9	363	526	348
DR90	3	8	27.2	38.3	386	433	294
DR180	3	16	50.7	81.3	439	662	735
DR270	3	25	82.2	109.3	364	500	588

Table 4.6: *Overview of the gate area A_{gate}, the onset energy of signal compression E_{kink}, the charge handling capacity of the internal gate per gate area C_{IG}, and the measured and theoretical sensitivity of the internal gate $g_q^{measured}$ and g_q^{theory} for the variants with open clear gate structure.*

4.3.2.3. Comparison with simulations

As mentioned in section 4.1, DEPFET production time is roughly 18 months and therefore numerical simulations play a crucial role in device development. Measurements from the first prototypes allow for a validation of the process and device simulations, especially for the nonlinear response curve. Simulations have been performed using Synopsys TCAD (Technology Computer-Aided Design), which provides a comprehensive suite of numerical semiconductor simulation tools for both 2D and 3D simulations [66]. This includes the simulation of the fabrication process as well as device simulations to investigate electrical device properties during operation.
Both 2D and 3D simulations have been performed as part of this thesis. However, the extensive computational effort for 3D simulations required a three-step approach to calculate the nonlinear response curve, which comprises an initial 2D simulation and two additional correction steps. The approach is illustrated in Figure 4.15 and its basic procedure will be discussed in the following.

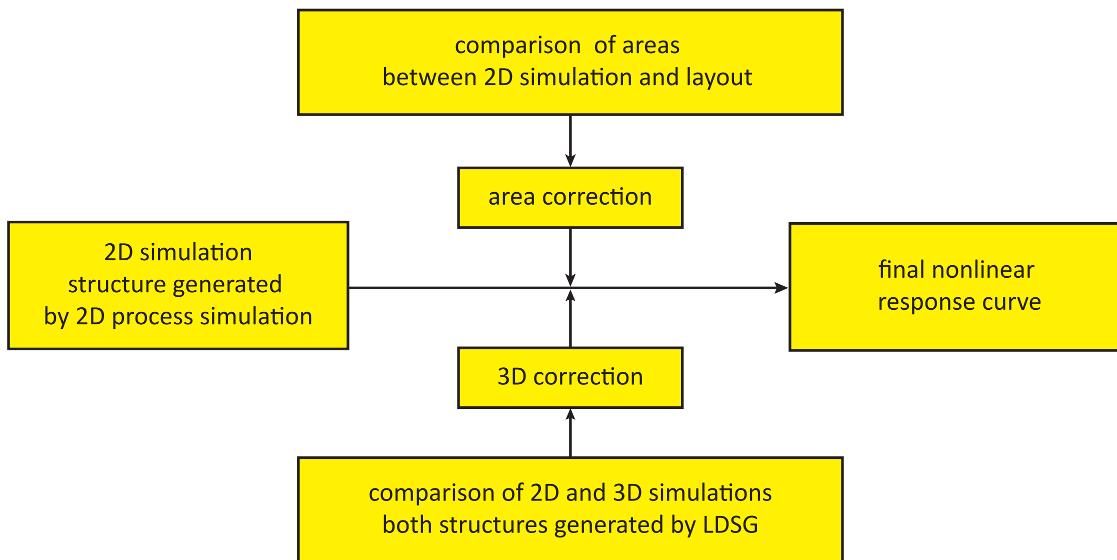

Figure 4.15: *Illustration of the simulations performed to calculate the nonlinear response curve. Two corrections are applied to the result of the cylindrically symmetrical 2D simulation in order to arrive at the final response of the DSSC-DEPFET. The first correction simply involves different sizes of the central region and the overflow region in the simulation and in the real device. The second correction involves 3D effects resulting from the nonideal rotation symmetry of the DEPFET, which influence potential distribution of the internal gate.*

First of all, we assume the DEPFET has a circular shape and perform a 2D simulation. A process simulation including all fabrication steps such as depositions, etchings, implantations and annealing cycles generates a two-dimensional structure of the DEPFET. This provides us with a very reliable prediction of the doping profiles, not just for the unstructured regions but also for the boundaries of the implantation areas generated by

photoresist or by polysilicon covering the silicon during the implantations. Two corrections are then applied after the cylindrically symmetrical 2D device simulation determines the nonlinear response of the DSSC-DEPFET.
The first correction has to do with the different areas of the central and overflow regions of the internal gate in the simulation and in the real device. The charge amount stored in the central portion and the overflow regions of the internal gate is thus scaled down by the ratio between the gate and the overflow area of the full circular structure and the real device. This approximation assumes that the potential distribution is correctly modeled in the 2D simulation, and consequently the capacity of the different regions of the internal gate simply scales with the considered area. For example, the DR180 variant featuring only one half of the full circular gate structure is assumed to exhibit only half the charge handling capacity of the central region extracted from the 2D simulation. The scaling factors for the central portion S_G and for the overflow region S_{OF} are summarized in Table 4.7 for all available variants.

	A_{gate}			A_{of}		
variant	layout	simulation	ratio S_G	layout	simulation	ratio S_{OF}
NG	27.0	105.6	3.911	4806	6781	1.41
SG	87.0	105.6	1.214	4812	6781	1.41
CG	209.0	238.8	1.143	4847	6619	1.37
DR60	18.8	94.2	5.011	5537	6807	1.23
DR90	27.2	94.2	3.463	5533	6807	1.23
DR180	50.7	94.2	1.858	5625	6807	1.21
DR270	82.2	94.2	1.146	5625	6807	1.21

Table 4.7: *Overview of the scaling factors S_G for the central region and S_{OF} for the overflow region of the internal gate for all layout variants. The scaling factors are defined as the ratio of the area considered in the simulation and the area in the real device.*

Assuming a homogeneous current density in the channel, this simple area correction can also be applied to the drain current influencing internal gate transconductance g_q (compare equation 4.14). Since the gate length is correctly modeled, the area scaling corresponds to a scaling of the gate width. The simulated drain current refers to the full circular structure, meaning a device like the DR180 variant with just a half gate circle, will only conduct half the current. This scaling has to be considered in advance in order to emulate the same current density in the channel like in the real device conducting 100 μA.
As the measurements have already shown, however, device properties do not simply scale with the gate area or width. In order to increase simulation accuracy and predictability of the device properties, the full 3D geometry has to be taken into account in a second correction step. Therefore, 3D simulations of the DEPFET structure have been introduced within the framework of this thesis, but a 3D simulation of the full fabrication process was not applicable as the computational effort was too high. Instead, the DEPFET structure

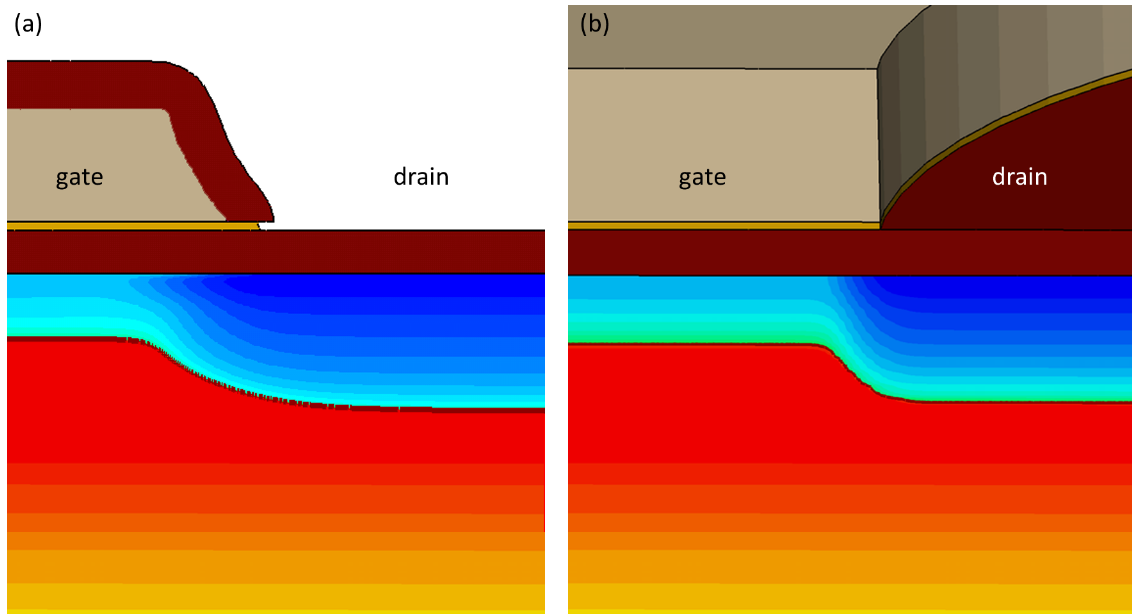

Figure 4.16: *Comparison of the doping profiles at the transition from the gate to the drain contact generated by 2D process simulations (a) and by LDSG for a 3D structure (b). Deviations of the color-coded doping concentration only occur at the implantation boundary.*

has been created using **l**ayout-**d**riven **s**tructure **g**eneration (LDSG) in which 2D masks directly exported from a layout program are used to grow layers of various materials on top of a silicon bulk to, for example, generate the MOS structure of the gate and the clear gate. Beyond layer generation, 1D doping profiles can be placed perpendicular to the 2D masks and thus emulate 3D implantations. The required 1D doping profiles can be extracted from process simulations or from measurements like SIMS (Secondary Ion Mass Spectrometry). The drawback of this approach is illustrated in Figure 4.16. The left side shows the result of a 2D process simulation whereas the right plot depicts a 3D structure generated by LDSG.
The example shows the transition from the DEPFET gate towards the drain contact. The p^+ drain implantation (POXN) is masked by the polysilicon MOS gate. Both structures are identical in the region of the homogeneous implantation. Differences only appear at the edges of an implantation. The realistic, rounded polysilicon shape is a result of the simulated etching processes and does not occur in the 3D structure, but it is relevant for the process simulation because it covers the drain implantation. Instead of an abrupt transition, the covering layer that the implantation penetrates gets thicker and thicker leading to a doping profile that moves towards the surface before it becomes completely shadowed by the MOS structure. However, the shape of the covering layers does not influence the doping profiles in the 3D structure at all since they are simply placed within the silicon. A Gaussian or error function with adjustable parameters is used for the transition from the implanted to the nonimplanted region. This allows us to primitively emulate the

underdiffusion of dopant atoms under covering layers, which leads to a fading of the 1D implantation profile, as shown in Figure 4.16 (b). The doping profile does not bend toward the surface and thus the underdiffusion is not realistically modeled. In case of the DEPFET gate this may change, for example, the effective gate length of the transistor, which limits accuracy when simulating the nonlinear detector response. As a result, and because a 3D process simulation was not applicable, the influence of the full geometry was investigated by comparing 2D and 3D simulations with both structures generated by LDSG to preclude the impact of differing doping profiles. A detailed description of the entire simulation procedure (Figure 4.15) will be given in the following sections.

4.3.2.4. 2D simulations with area correction

For a 2D simulation of the nonlinear response curve, a 2D cut is made through the device as depicted in Figure 4.17. It starts at the pixel center with the drain contact, includes the internal gate under the DEPFET gate and the overflow region under the source, and ends at the outer pixel rim in the center of the second drift ring. The figure shows only the top part of the corresponding 2D doping profile used as input data in the 2D device simulations. The simulation covers a radius of 120 μm and a device depth of 180 μm.

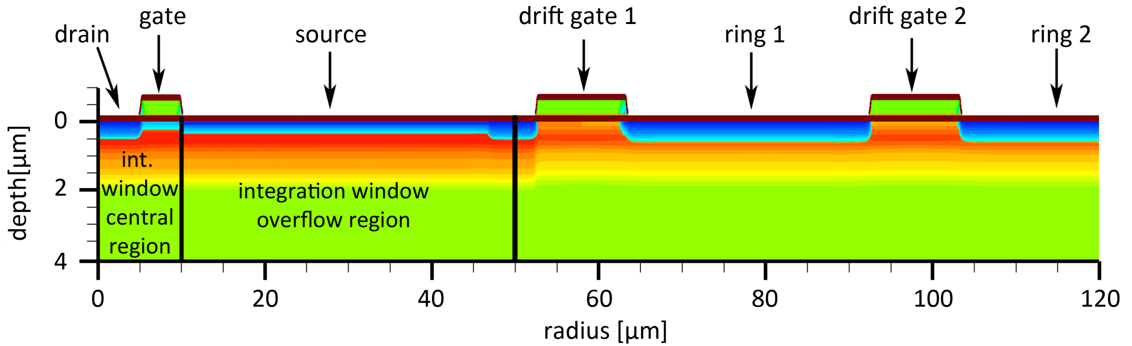

Figure 4.17: *2D structure generated by process simulation including pixel topology and implantations within the silicon and serving as input data for 2D device simulations. The picture shows only the top part of the 180 μm deep structure. The two black boxes mark the integration windows for signal charge stored in the central part (left) and the overflow region (right) of the internal gate for later scaling of the response curve.*

The first step of the device simulation is to establish the initial situation before charge generation, i.e., biasing of all contacts with voltages corresponding to the measurements and full depletion of the internal gate. Initially, the supply voltages are ramped up consecutively in a quasi-static simulation. During this procedure, the gate voltage needs to be adapted to achieve a current density in the transistor channel that corresponds to the real device. For example, during measurement the SG variant has been operated with a transistor current of $I_D^{meas} = 100\ \mu A$ with an empty internal gate. To achieve consistency in the simulations for a full circular structure, the following baseline transistor current has to be set via the

gate voltage in the simulation:

$$I_D^{sim} = I_D^{meas} \cdot S_G \tag{4.17}$$

The next step is to deplete of the internal gate. However, this is not easily achieved since the cylindrical structure does not have an n^+ contact to dump free electrons. The only way out is to manually modify the occupation probability of energy levels in the detector material, which in semiconductors is described by the Fermi-Dirac statistic

$$f_{FD}(E) = \frac{1}{1 + e^{\frac{E-E_F}{k_b T}}} \tag{4.18}$$

with E as the potential of the energy level, k_b as the Boltzmann constant, T as the device temperature and E_F as the so-called Fermi level. By decreasing E_F far below conduction band potential, the occupation probability of the conduction band with electrons can be reduced to zero. This situation corresponds to a fully depleted device and is a prerequisite for the simulation of the nonlinear response curve.

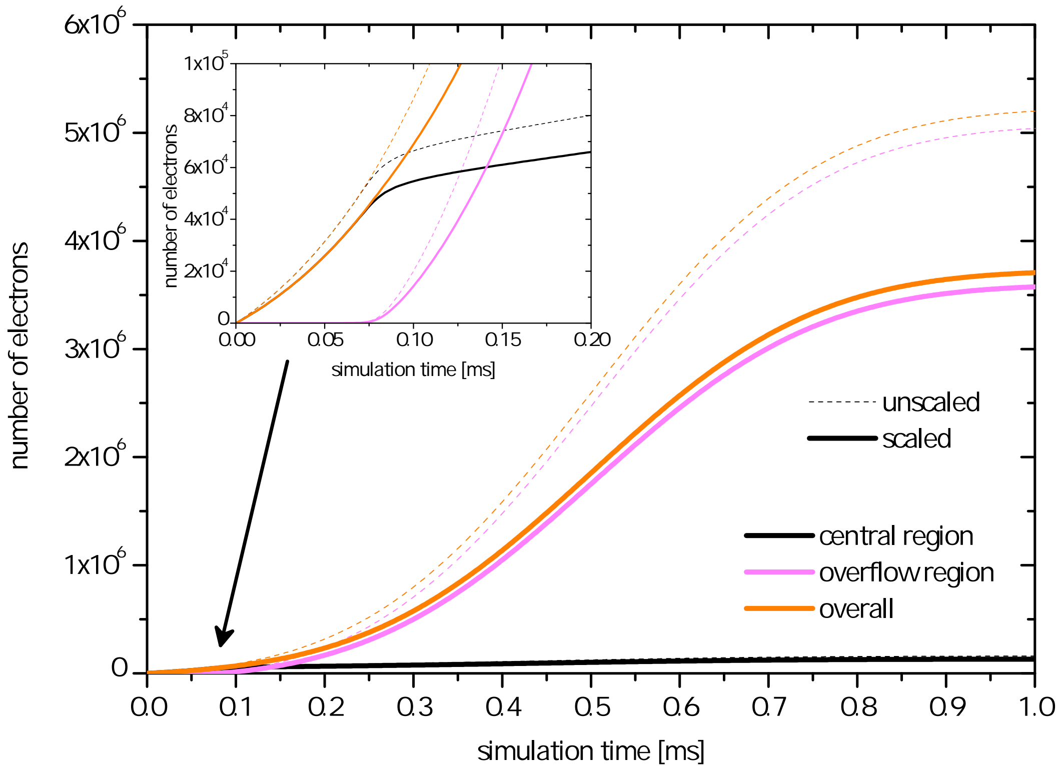

Figure 4.18: *The temporal evolution of overall charge generation and its distribution over the central and overflow regions of the internal gate. The insert shows an enlarged view of the first 200 μs. During the first 70 μs all charge is stored in the central region before the electrons spill over into the overflow region causing a compression of the DEPFET output signal. The dashed lines show unscaled simulation results and the solid line shows the consequences of the area scaling in the case of an SG variant.*

The last step is the simulation of drain current change due to charge generated in the internal gate. Since in a quasi-static simulation, the device always stays in electrical equilibrium, the internal gate would be immediately filled up again with electrons once the Quasi-Fermi potential is not fixed anymore. For this reason, determining the nonlinear response curve requires transient simulations. The covered time range is 1 ms and the time characteristics of the charge generation rate has a Gaussian shape with a FWHM of $\sigma_{\mathrm{FWHM}} = 200\ \mu$s and a maximum at t = 500 μs. The charge is generated underneath the external gate at a depth of 3 μm resulting in a very fast settling time of the generated charge in the ns range. Combined with very slow charge generation rates, this guarantees almost perfectly settled charge distribution at all times. This kind of simulation is not intended to reflect the real process of charge generation and collection, but it provides an instrument to control internal gate filling in order to obtain the nonlinear response curve. Two integration windows, indicated in Figure 4.17, are defined so the simulated charge can be scaled to the corresponding charge in the real device. This enables us to determine the number of electrons in each window, taking into account the full circular geometry. The temporal evolution of the charge generation process during the simulation is illustrated in Figure 4.18.

During the first 70 μs, all generated electrons accumulate in the central part of the internal gate before the electrons begin to enter the outer integration region, indicating the onset of signal compression. Once this effect has started, additional charge is mainly collected in the overflow region and the number of electrons in the central part only increases very slowly.

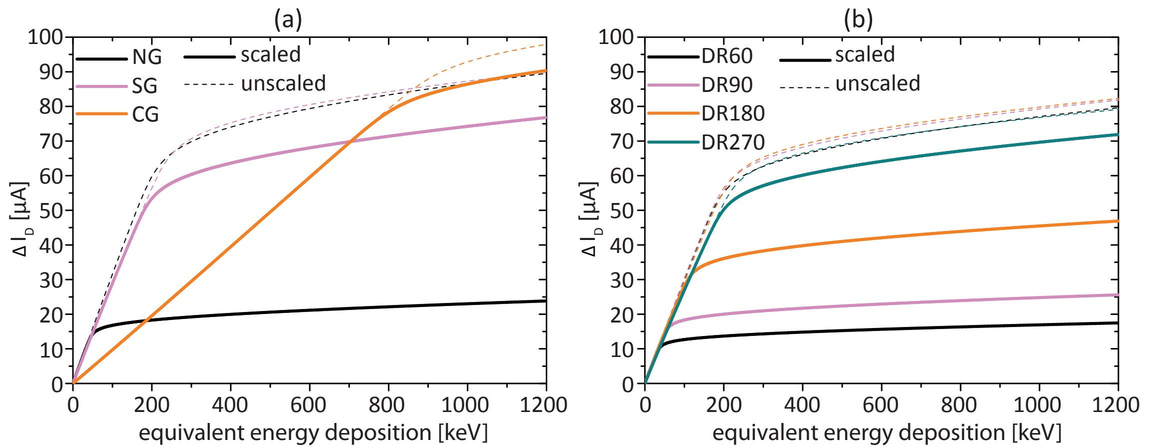

Figure 4.19: *Comparison between the unscaled response curves directly obtained by 2D simulations and the curves scaled with S_G and S_{OF} in order to compensate for the pure area difference between the simulation and the real device. The traditional variants are shown in (a) and the new variants in (b).*

The simulated response curve of the DEPFET becomes obvious when the DEPFET output signal is plotted as a function of the overall generated charge. In order to take the area correction into account, the drain current and the charge in the internal gate are scaled with

the factors given in Table 4.7. Figure 4.19 shows the unscaled and then scaled DEPFET characteristics obtained by 2D simulation for all layout variants.
When the scaling factor S_G is applied to the charge in the central region and the drain current, and the scaling factor S_{OF} is applied to the charge in the overflow region of the internal gate, it has two effects on the curves. On the one hand, the smaller the gate area of the real device gets, the more the kink energy E_{kink} is shifted toward lower energies. As for all prototypes the gate area is smaller than in the 2D simulation, the unscaled curves always bend at higher accumulated energies. On the other hand, a reduced gate area enhances the compression factor since the fraction of charge stored directly below the transistor channel is decreased.
By contrast, the sensitivity of the internal gate g_q^{lin} for small amounts of signal charge stays constant because in the linear region both the charge and the current axis are compressed with the common factor S_G.

	kink energy [keV]		
variant	2D simulation	measurement	ratio
NG	53.5	39.5	1.354
SG	186.5	134.1	1.391
CG	773.3	670.8	1.153
DR60	37.0	24.9	1.486
DR90	54.3	38.3	1.418
DR180	103.3	81.3	1.271
DR270	170.8	109.3	1.563

Table 4.8: *Overview of the kink energy E_{kink} determined by 2D simulations and measurements for all available variants. The simulation values are scaled from the circular shape to the gate area of the real device using S_G.*

Table 4.8 provides a summary of extracted kink energies E_{kink} and their deviations from measurement data for all variants. The deviations range from 15% for the CG to 56% for the DR270 variant. This indicates that the impact of the layout on the nonlinear response curve goes beyond the influence of the pure gate area. The following section deals with 3D simulations in order to not only investigate the impact of 3D effects on device properties but also to compensate for them.

4.3.2.5. 3D corrections

This section contains a comparison of 2D and 3D simulations allowing to quantify the impact of the real layout on the detector response. In order to anticipate the effect of deviant doping profiles at the implantation boundaries (compare Figure 4.16), structure generation for both simulations has to follow the same procedure. Since the 3D process simulation is not suitable because of excessive computational demands, both the 2D and

the 3D structures are done using LDSG: 1D doping profiles are placed within the silicon and the underdiffusion of dopant atoms at the implantation boundaries is modeled with a mathematical function defining the fading of the 1D profiles. The nonlinear response curves were then simulated for all available variants taking into account the supply voltages of the measurements summarized in Table 4.4.
The 2D device simulations have been performed according to the procedure described in the section above. The resulting response curve is scaled afterward with the scaling factors from Table 4.7.
By contrast, the 3D simulations include all contacts necessary for the full operation of the DEPFET, i.e., the clear and the clear gate are also covered, allowing for the extraction of free electrons from the device and thus the full depletion of the silicon bulk. Figure 4.20 shows the top part of the 3D structure for the SG variant generated by LDSG.

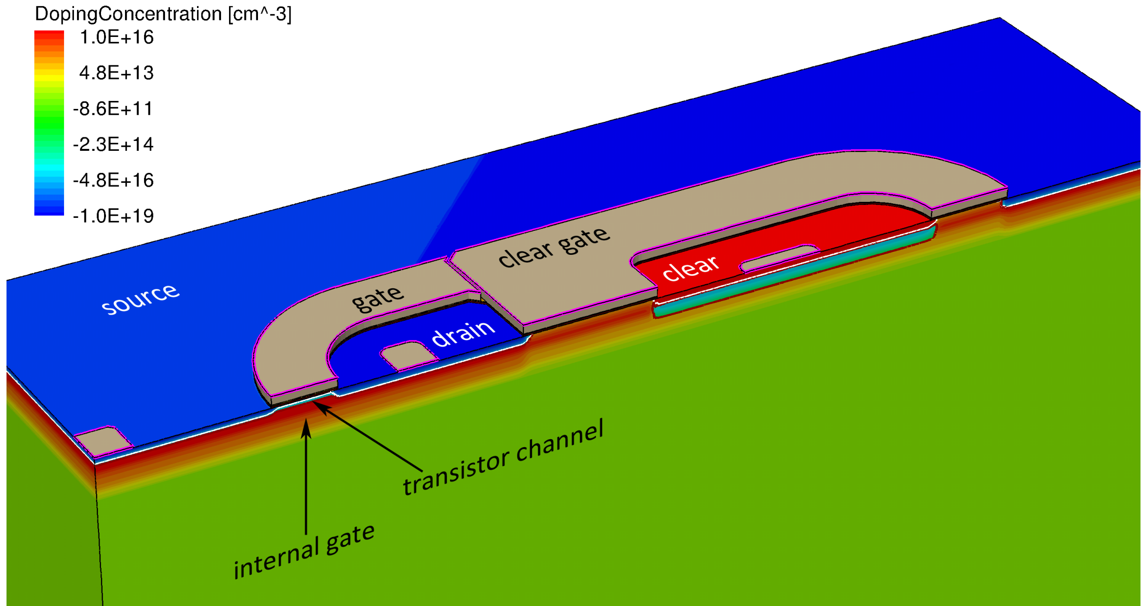

Figure 4.20: *Three-dimensional structure of the SG variant generated by LDSG. The horizontal plane covers an area of 16 x 60* μm^2 *and the device depth is 50* μm. *The doping concentration is color-coded.*

The simulation takes advantage of the symmetry of the DEPFET and thus comprises only one half of the DEPFET. All outer boundaries are treated with reflective conditions, a so-called ideal Neumann boundary:

$$\epsilon \nabla \Phi + \vec{P} = 0 \tag{4.19}$$

where ϵ is the dielectric constant in silicon, Φ the electrostatic potential and $\vec{P}$ the polarization of the material. In particular, this implies that streamlines of the electric field terminate perpendicular to the surface of the boundary and that there is neither an

electron nor a hole current flowing through that surface:

$$\overrightarrow{J_n} \cdot \hat{n} = 0 \tag{4.20}$$
$$\overrightarrow{J_p} \cdot \hat{n} = 0 \tag{4.21}$$

The structure covers an area of only 16 x 60 μm^2 in the pixel center. This precludes the simulation of the compression factor since not the full overflow region is considered but it minimizes the number of required grid points and the related calculation time.
Similar to the 2D simulations, quasi-static simulations are used to raise DEPFET supply voltages to the values given in Table 4.4. Subsequently, a 300 ns long transient simulation of a realistic clear pulse was performed. A V_{CG}^{high} of +7 V and a V_{CL}^{high} voltage of +20 V have been applied for 270 ns in order to extract all electrons from the device. Because of the small size of the considered overflow region, 270 ns are more than sufficient to accomplish a complete clear process. For the final simulation of the response curve, charge is generated according to the 2D simulations at a depth of 3 μm directly underneath the external gate, leading to a charge settling time in the ns range. The overall simulation time was 1 ms and the charge generation rate had a Gaussian shape with a maximum at t = 500 μs and a FWHM of $\sigma_{\mathrm{FWHM}} = 300$ μs. Since the 3D simulation delivers a response curve of only one half of the DEPFET, the 3D curve also has to be scaled, but in this case both the transistor current and the charge in the internal gate just have to be multiplied by a factor of two.
Figure 4.21 shows a comparison between the response curves obtained by 2D and 3D device simulations for all variants. Since the overflow region is only partially considered in the 3D structure, the slope of the response curves in the compression region is much steeper because more electrons are stored directly underneath the transistor channel. Nevertheless, the simulations show for all variants that the kink in the 3D curves occurs at smaller accumulated energies.
The reason for this becomes apparent in Figure 4.22 (a) showing the electrostatic potential in absence of electrons on a horizontal cut through the device in the depth of the internal gate for the SG variant. The potential distribution along a cut through the transistor channel depends on the position of the cut. In particular, this means that the potential is not constant perpendicular to the channel. Instead, it becomes increasingly negative toward the clear gate. This reduces the effective gate area and leads to an overflow of signal electrons under the source for smaller accumulated energies than it is expected from 2D simulations considering only the pure effect of the gate area. The potential distribution along the transistor channel in the depth of the internal gate is depicted in Figure 4.22 (b) for the cuts marked in (a). In the center of the pixel, the curves show a negative electrostatic potential of roughly -1.2 V due to negative drain voltage. Furthermore, the potential in the overflow region is also almost identical for both curves because the doping profiles and the source voltage are the same. However, small deviations occur since the source is only connected via a small contact hole and the location-dependent current flowing through the

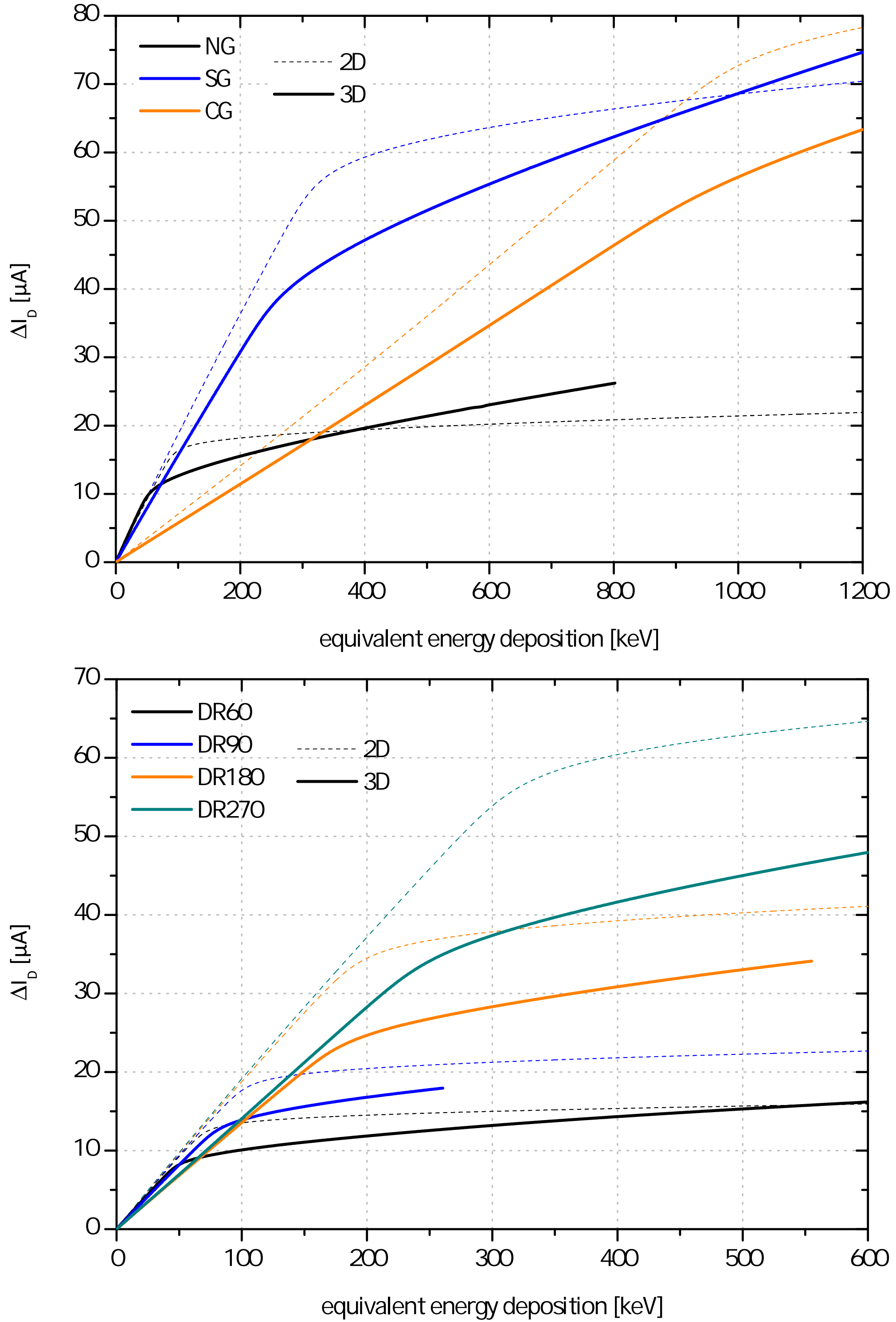

Figure 4.21: *Comparison of nonlinear response curves for traditional (top) and new (bottom) variants obtained by 2D and 3D device simulations. Both input structures are generated by LDSG allowing us to isolate the impact of the noncylindrical symmetry of the DEPFET on the nonlinear response. The different variants are color-coded. The dashed lines indicate the 2D results and the continuous lines are the 3D results.*

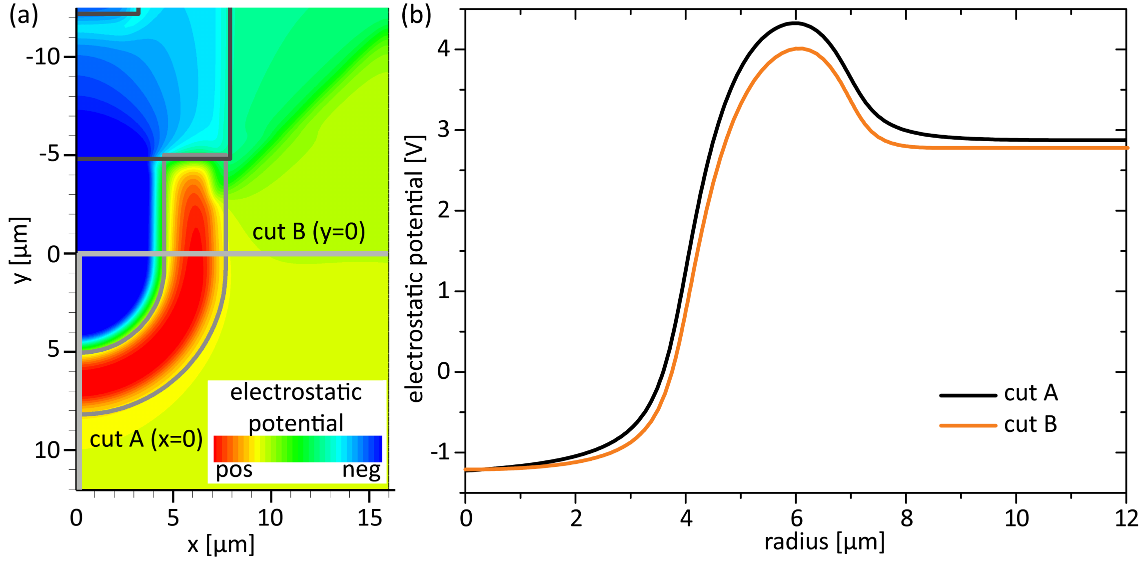

Figure 4.22: *(a) Potential distribution on a horizontal cut through the 3D DEPFET structure of the SG variant at a depth of the 0.75 µm, where the potential maximum of the internal gate is located. The position of the gate and the clear gate located at the top of the silicon bulk are indicated by gray lines. (b) Potential distribution along the two cuts illustrated in (a) through the internal gate.*

implantation causes a voltage drop due to its finite sheet resistance. In particular, this means that the source potential, coupled to the overflow region below, depends on the position within the source implantation. This effect can be suppressed either by a reduction of the source current or by lowering the sheet resistance of the source implantation. Of course, both cannot be regarded as free parameters, but they are subjected to operation and fabrication considerations.

By contrast, the height of the potential maximum located directly underneath the external gate is clearly lowered for shorter distances to the clear gate. In addition, the shape of the gate at the position of cut B is no longer circular, but linear. This enhances the impact of negative drain potential in the center and leads not only to a reduction of electrostatic potential in the internal gate but also to a shift of the radial position of the maximum toward the source.

Cut A is farthest from the clear gate and thus closest to cylindrical symmetry. This cut features the highest potential step in the 3D simulation, which means the number of electrons fitting in the central region of the internal gate is reduced in the 3D simulation. This also becomes apparent in Table 4.9, which summarizes the onset energy of signal compression E_{kink} for all variants extracted from the 2D and 3D simulations.

The ratio of E_{kink} for both simulation methods - S_{3D} - quantifies the impact of real geometry on charge handling capacity of the central part of the internal gate. The smallest deviations occur for the CG and the DR180 variants, which exhibit a large gate width and the highest similarity to a circular DEPFET gate. In order to include the observed 3D effects in the nonlinear response curve we can define an effective scaling factor for the gate

area

$$S_G^{eff} = \frac{A_{gate}^{simulation}}{A_{gate}^{layout}} \cdot S_{3D} = S_G \cdot S_{3D}. \tag{4.22}$$

This approximation implies that only part of the central region of the internal gate is used to store electrons before the spillover under the source begins. Scaling the nonlinear response curve with the factors S_G^{eff} and S_{OF} takes into account both the pure area correction as well as 3D effects. It has to be pointed out that the 3D correction factors S_{3D} technically have to be determined individually for every layout and each set of operation parameters. Since this requires prohibitive computational effort, the impact of the layout on the detector response has only been tested under standard operating conditions and the impact of DEPFET supply voltages (see section 4.3.3) has only been studied for the SG variant.
The clear gate is also coupled to the overflow region of the internal gate, but the reduction of electrostatic potential is restricted to only a very small part in the direct proximity of the clear structure. The impact on the compression factor is therefore very limited and 3D effects can be neglected for the effective overflow area.

4.3.2.6. Conclusion

Simulation of the nonlinear response curve of a DSSC-type DEPFET requires precise knowledge of the doping profile within the complete device as well as some attention to the entire 3D structure. It has been shown that process simulations including all fabrication steps deliver more realistic doping profiles at the implantation boundaries than layout-driven structure generation. Consequently, a desirable full 3D simulation flow would comprise both process and device simulations. Although the DSSC-DEPFET pixel is mirror-symmetric, at least one half of the pixel has to be included in the simulation in order to determine the nonlinear response curve over the full energy range. Due to the enormous computational effort required, however, this procedure is currently not applicable. Instead, 2D process and device simulations were performed where cylindrical symmetry is

	kink energy [keV]		
variant	2D simulation	3D simulation	ratio S_{3D}
NG	90.5	51.0	1.775
SG	308.5	245.0	1.259
CG	970.5	909.5	1.067
DR60	69.5	48.0	1.448
DR90	100.5	79.0	1.272
DR180	188.5	172.0	1.096
DR270	309.0	236.0	1.309

Table 4.9: *Overview of the kink energy E_{kink} determined once with 2D and once with 3D simulations for all available variants. The deviations between both results indicate the impact of real geometry compared to a circular shape of the DEPFET gate.*

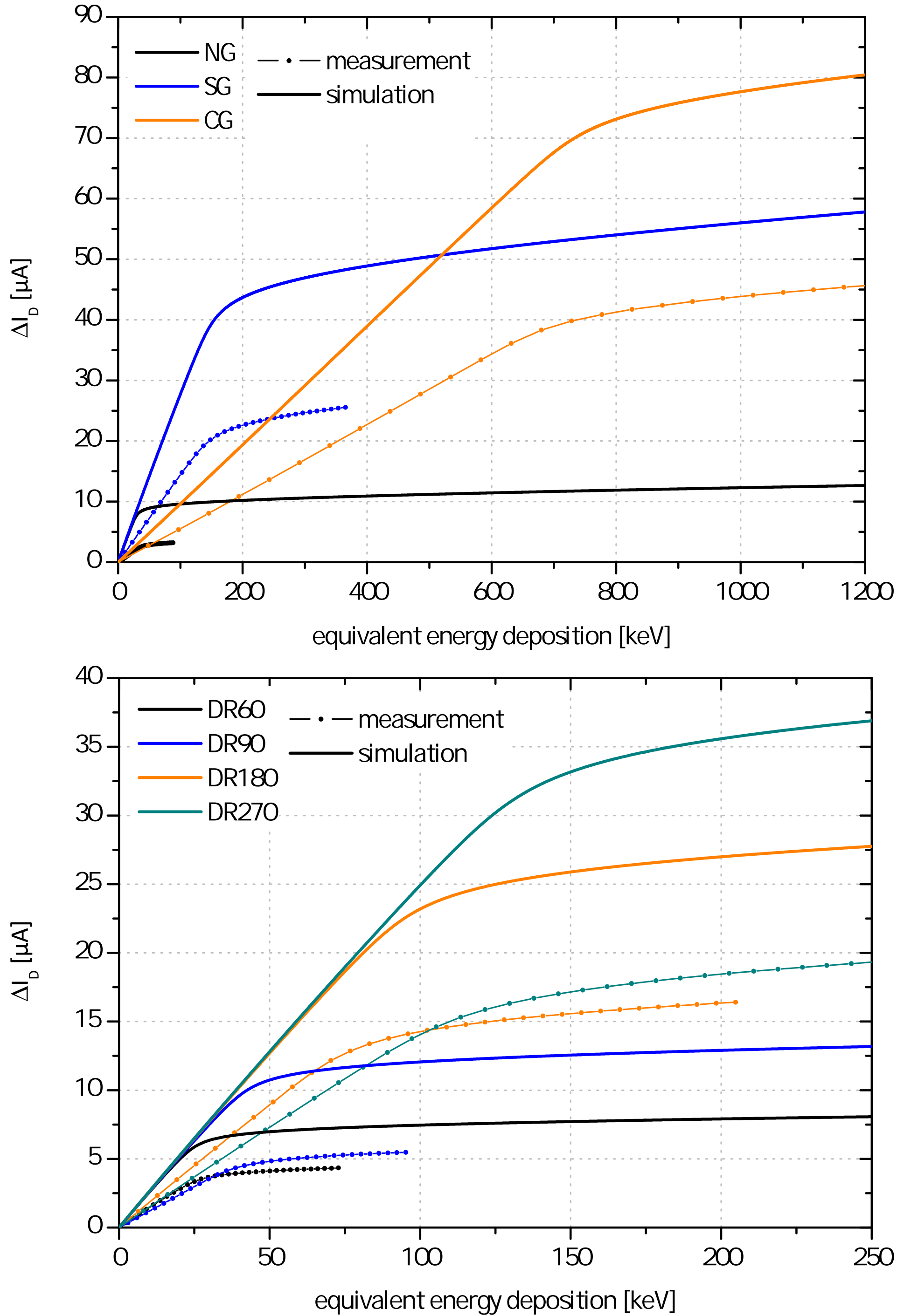

Figure 4.23: *Comparison of the nonlinear response curves for the classical variants (top) and the novel variants (bottom) obtained from measurements and simulations considering both the pure area as well as the 3D correction. The symbols mark the measurement points for a representative pixel of the according variant. The agreement between measurement and simulation is rather poor for the charge transconductance g_q due to the unknown hole mobility in the channel but is very good for the kink energy E_{kink} being the most important design parameter of the DSSC-DEPFET.*

assumed and two previously discussed corrections were applied to the result. The simulated nonlinear response curves with both introduced corrections are depicted in Figure 4.23 together with the measurement results for the traditional and the new variants.
We see big deviations between the simulation and the measurements for the slope of the curves in the linear region. The sensitivity of the drain current to signal charge in the internal gate is overestimated in the simulation. One possible explanation relates to the hole mobility in the channel illustrated in Figure 4.24.

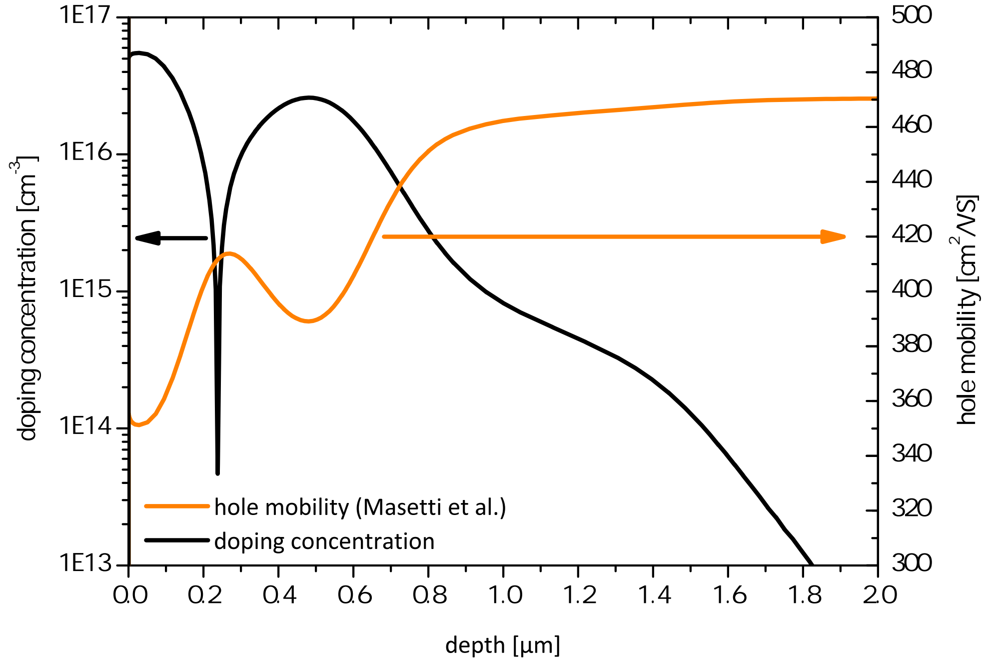

Figure 4.24: *Hole mobility and doping concentration extracted from the simulation on a cut perpendicular to the transistor channel. The mobility varies with the doping concentration according to the analytical model proposed by Masetti et al. [67].*

The black curve shows the doping concentration on a cut through the channel perpendicular to the Si-SiO_2 interface. The channel implantation is located close to the surface and the *pn* junction is at a depth of roughly 250 nm. The peak below belongs to the deep *n* implantation of the internal gate. The orange curve depicts hole mobility including a doping dependence based on the model proposed by Masetti et al. [67]. Hole mobility reaches its minimum of $\mu_\mathrm{p} = 350\ \frac{\mathrm{cm}^2}{\mathrm{Vs}}$ in the region close to the surface, where maximum current density exists. This value is still much higher than the average hole mobility $\mu_\mathrm{p} = 80\ \frac{\mathrm{cm}^2}{\mathrm{Vs}}$ extracted from the measurements, but the differences may be due to mobility degradation at the interface caused by additional scattering centers that were not taken into consideration. Since equation 4.14 says that the sensitivity of the internal gate is directly proportional to the square root of hole mobility, the observed deviations of roughly a factor two, can be explained. However, further optimizations of the mobility models have been dispensed because absolute current values are anyway calibrated in the detector system.

The main focus of simulations regards the onset energy of signal compression because this defines the dynamic range of the DSSC detector system. Table 4.10 summarizes both measured and simulated kink energies for all prototypes. The deviations range from 25% for the NG to below 2% for the DR60 variant.

	kink energy [keV]		
variant	measurement	simulation with corrections	deviations
NG	39.5	29.8	0.754
SG	134.1	146.8	1.095
CG	670.8	723.5	1.079
DR60	24.9	25.3	1.016
DR90	38.3	42.3	1.104
DR180	81.3	93.8	1.154
DR270	109.3	129.0	1.180

Table 4.10: *Overview of the kink energy E_{kink} determined by measurements and 2D simulations for all available variants. The simulation values take into account both the pure area as well as the 3D correction.*

The specific effects of the two correction to this very good agreement are illustrated in Figure 4.25.

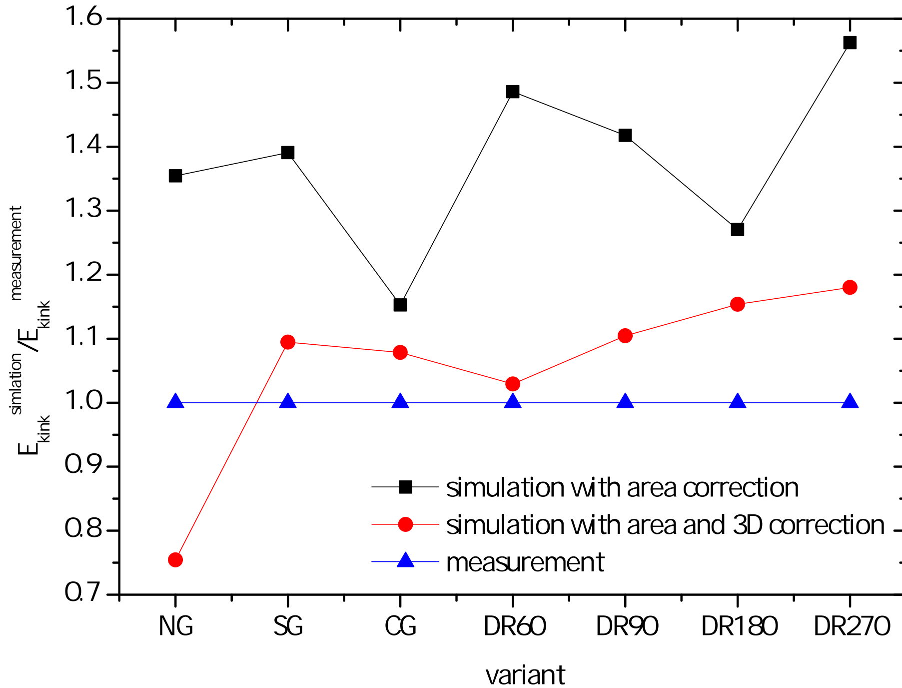

Figure 4.25: *Deviations of the onset energy of signal compression from measurement results for simulations with and without considering the 3D correction.*

The curve without corrections is not shown because, especially for small gate devices, the deviations are very high, for example 740% for the DR60 variant. By considering

only the area correction, discrepancies can be limited to less than 60% and generally the values become smaller for large gate devices where 3D effects play only a minor role. The DR270 variant is an exception since the high-dose source implantation (POXN) is directly bordering the external gate at roughly 1/3 of the gate width, as illustrated in Figure 4.26.

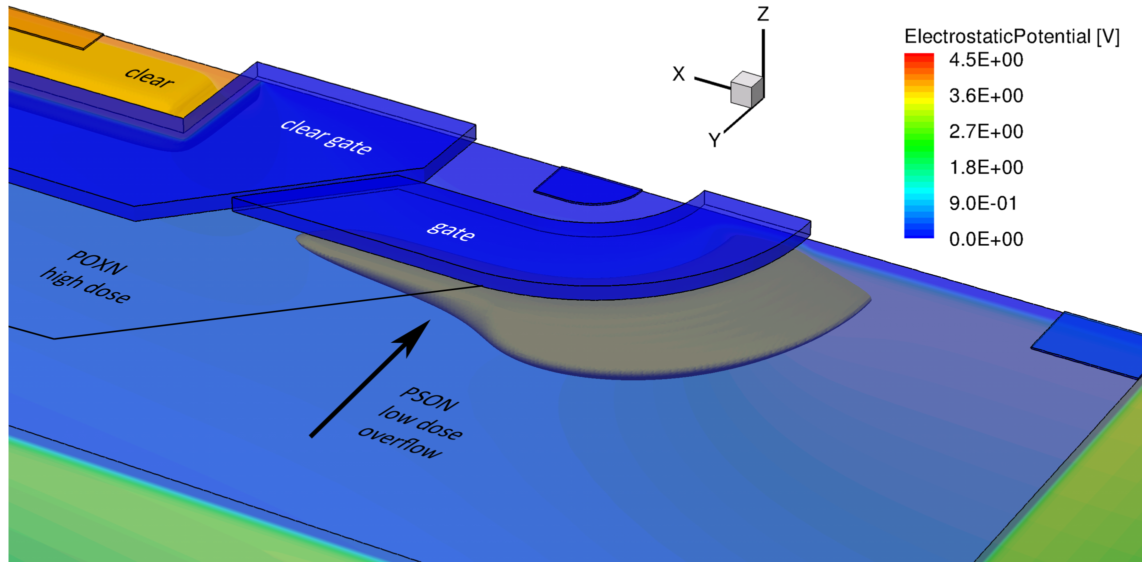

Figure 4.26: *3D potential distribution simulated for the DR270 variant with empty internal gate. The detail shows the isosurface at a potential of 3.3 V directly under the external gate. The black line represents the shape of the high-dose source implantation (POXN). Due to the direct adjacency of the POXN to the external gate, the isosurface is compressed and thus the volume of the internal gate is decreased.*

This proximity lowers electrostatic potential in the associated part of the internal gate and thus reduces charge handling capacity of the internal gate. The effect is not considered in the 2D simulation, leading to the higher discrepancy for the pure area correction but at the same time the 3D correction has a stronger impact. For all other variants the 3D correction gains influence for smaller gate devices since edge effects become more dominant. Apart from the NG variant, kinks in the measured curves occur systematically for smaller energies, indicating that the modeled doping profiles do not perfectly match the real device. That could in turn lead to a higher potential step between the central and the overflow region and thus to a delayed overflow of signal electrons under the source. The exception of the NG variant is most likely due to the linear shape of the gate and the assumed cylindrical symmetry in the 2D simulations, which limit the applicability of the corrections. It has to be pointed out that the DR180 and DR270 variant are the only ones sensitive to misalignment of the POXN implantation. As discussed above, a POXN implantation adjacent to the gate reduces charge handling capacity of the internal gate. If the POXN mask is misaligned, it causes a smaller or bigger contact area, which either weakens or enhances the effect. For all other variants, crucial implantations for charge handling capacity of the internal gate (PSON and POXN) are self-aligned because in the pixel center

they are only masked by the MOS structure of the DEPFET gate. This excludes an impact of misalignment on the onset energy of signal compression for those variants. The effect of misalignment is not part of in the simulation, which may be the reason why the highest discrepancies for circular gate geometries are observed for DR180 and DR270 variants. Nevertheless, simulations that take into account both the area and the 3D corrections show very good agreement with the measurements, validating the applicability of the simulation approach and allowing for the optimization of the nonlinear response curve of future DSSC-DEPFET devices.

4.3.3. Variation of DEPFET supply voltages

To operate large-area devices with a high number of DSSC-type pixels, there are three main issues regarding global supply voltages that have to be investigated:

- Do fluctuations of the bulk doping concentration, which can be emulated by a change of the backside voltage, have any impact on the functionality of the pixels?
- What are the consequences of a reduction in clear gate low voltage during the 2,700 flashes of one burst due to the discharge of capacitors in the electronics?
- How can the nonlinear response curve be adjusted by the drain voltage?

The change in DEPFET amplification due to the clear low voltage is negligible, since the capacitive coupling is too weak. Furthermore, high levels of the clear and clear gate are only applied during the reset of the internal gate and therefore have no impact on the detector response - if a complete removal of signal charge can be guaranteed. Also, as long as the transistor is switched on, gate voltage does not change the potential distribution in the internal gate. Hence, only the impact of the backside, the clear gate low, and the drain voltage are investigated below.

4.3.3.1. Backside voltage

The DSSC detector will be composed of 32 monolithic sensor chips each with a format of 6.2 x 3.0 cm^2. Radial bulk doping variations of roughly 10% have been observed over a single wafer for previous productions of similar devices using the silicon float-zone substrate material with an extremely low n-doping concentration of $1 \cdot 10^{12}$ cm^{-3}. Due to the large chip size, comparable fluctuations are expected in final sensor production for one monolithic sensor chip comprising 128 x 256 pixels. Doping fluctuations cause a local change in bulk depletion voltage. Changing the backside voltage can compensate for this in single pixels but it does not work in DSSC devices that provide a large number of pixels operated with a global backside. Nevertheless, it has to be ensured that the backside voltage is higher than the depletion voltage of any pixel in the matrix so that pixel functionality is maintained.

Depletion of the DEPFET is mainly done via the backside diode, which is basically a single-sided abrupt *pn* junction. The width of its space charge region can be calculated based on

$$W_D = \sqrt{\frac{2\epsilon_0\epsilon_{Si}(V_{BC} - \Psi_{bi})}{eN_d}}. \tag{4.23}$$

with ϵ_0 as the dielectric constant in vacuum, ϵ_{Si} the relative dielectric constant in silicon, V_{BC} the voltage applied to the backside diode, Ψ_{bi} the built-in potential, e the elementary charge and N_d the donor concentration in the silicon bulk [65]. Depletion voltage is reached if the space charge layers from the backside and the front side touch each other. Since the impact of doping fluctuations on the width of the depletion region of the front side is negligible, the width of the depletion region of the backside diode has to be kept constant. In particular, this means that 10% more negative backside voltage can emulate a 10% increase of bulk doping concentration.

Figure 4.27 shows the nonlinear response curve of a DSSC-type pixel in the SG variant for backside voltages between -80 and -150 V. The depletion voltage for the examined pixel is

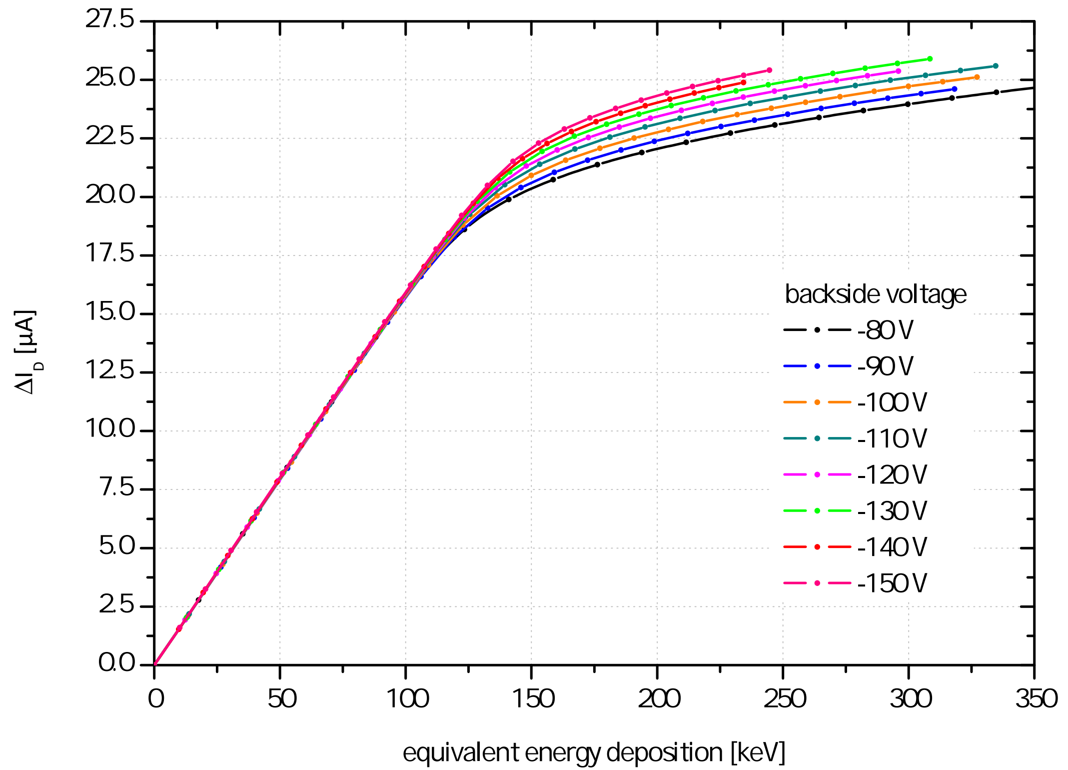

Figure 4.27: *Measured nonlinear response curves for a single pixel in the SG variant for backside voltages between the depletion voltage of -80 V and -150 V. The amplification for small signals g_q^{lin} stays unchanged but kink energy E_{kink} is shifted toward higher accumulated energies for more negative backside voltages.*

reached at -80 V. The observed 10% fluctuations of bulk doping concentration within one device, based on equation 4.23, result in depletion voltage deviations of less than 10 V. Therefore, the expected fluctuations of the bulk depletion voltage are significantly exceeded

by the tested voltage range from -80 V to -150 V.

The decrease of the backside voltage does not change the stray capacitances of the internal gate and as a result, sensitivity g_q^{lin} of the DSSC-DEPFET for small signals stays constant. However, a slight shift of kink energy E_{kink} toward higher accumulated energies shows up for more negative backside voltages. This can be explained by differing coupling strengths between the internal gate and the transistor channel and source implantation. The DSSC-DEPFET structure and the relevant capacitive couplings of the internal gate are illustrated in Figure 4.28. The potential of the backside V_b and the source V_s as well as the potential

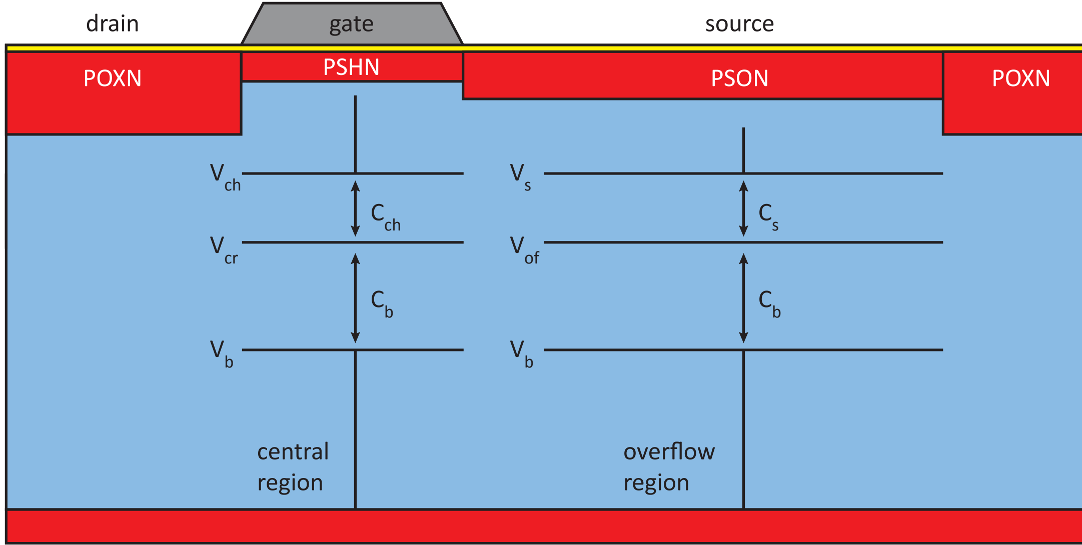

Figure 4.28: *Illustration of the relevant couplings in the internal gate towards the channel C_{ch}, the source C_s, and the backside C_b.*

within the channel V_{ch} are provided by external supply voltages. Potential distribution of the internal gate can be calculated by solving the Poisson equation taking into account the given boundary conditions. This multidimensional problem can only be solved numerically. Nevertheless, changes in the electrostatic potential of the floating internal gate due to a variation in backside voltage can be estimated for a fully depleted device. Therefore, capacitive coupling strength between the central region and the transistor channel C_{ch} and between the overflow region and the source C_s have to be taken into account. Furthermore, coupling the entire internal gate with the backside C_b also has to be considered.Changes of the electrostatic potential in the central region ΔV_{cr} and in the overflow region ΔV_{of} of the internal gate due to shifts of the backside voltage ΔV_b can be calculated as follows:

$$\Delta V_{cr} = \Delta V_b \cdot \frac{C_b}{C_b + C_{ch}} \tag{4.24}$$

$$\Delta V_{of} = \Delta V_b \cdot \frac{C_b}{C_b + C_s} \tag{4.25}$$

Based on this, the following calculations can be made to arrive at the variation of the

potential step ΔV_{step} between the central and overflow regions directly connected to the onset energy of signal compression:

$$\Delta V_{step} = \Delta V_{cr} - \Delta V_{of} \quad (4.26)$$

$$\Delta V_{step} = \Delta V_b \cdot C_b \left(\frac{1}{C_b + C_{ch}} - \frac{1}{C_b + C_s} \right) \quad (4.27)$$

Table 4.11 summarizes the depth of the initial depletion region d_{dep} in the p implantation and the depth of the potential maximum d_{pm} of the internal gate for the central as well as overflow regions. The values are taken from device simulations under standard operating conditions. Coupling strength is enhanced for smaller vertical distances between the beginning of the space charge region and the position of the potential maximum.

parameter	central region	overflow region
d_{dep} [μm]	0.05	0.23
d_{pm} [μm]	0.69	1.15
$d_{pm} - d_{dep}$ [μm]	0.64	0.92

Table 4.11: *Overview of the depth for the initial space charge region d_{dep} and the depth of the potential maximum d_{pm} as well as their vertical distance for the central and overflow regions of the internal gate. All values are taken from device simulations.*

It turns out that the coupling strength C_{ch} is higher than C_s. In particular, this means that V_{cr} is less influenced by the backside voltage variation compared to V_{of}. For more negative backside voltages, this leads to an increase of the potential step between the central and overflow regions and thus to higher charge handling capacity in the central part of the internal gate, resulting in the observed shift of onset energy of signal compression toward higher energies. This effect also becomes apparent in the simulated nonlinear response curves. However, the performed measurements show that the device stays functional for a very wide range of backside voltages that correspond to bulk doping fluctuations of a factor of almost two - much more than expected for the final devices. The differences in amplification properties are limited and can be compensated by a dedicated pixel-by-pixel calibration procedure [68].

4.3.3.2. Clear gate voltage

During each burst of the European XFEL, which contains 2,700 X-ray flashes with a maximum repetition rate of 4.5 MHz (compare chapter 2), the detector is in the on-state and in the time between the flashes almost all supply voltages stay unchanged. The only exceptions are the clear and clear gate because they have to be switched for the reset of the internal gate. Because the capacitance of these contacts is quite high and more than 2,700

switching cycles with voltage swings of several volts have to be performed within 600 μs, the power is mainly provided by big arrays of capacitors. Each switching discharges the capacitors and leads to a slight reduction of the high and low levels of the clear and clear gate voltages with respect to ground.

The high levels are only applied to the DEPFET when the internal gate is being reset and therefore do not influence its amplification properties. Lowering of the high levels extends the time required to extract all electrons from the internal gate. However, this can be compensated by increasing the initial high levels so that a complete clear process is ensured within the available time interval even for the last flash of an XFEL burst. The amplification properties of the DEPFET only depend on the low-level voltages applied to the device during the integration and readout phase. In that respect, the clear low voltage can also be neglected as long as back emission of electrons into the internal gate does not occur - the surrounding clear gate prevents its impact on potential distribution in the internal gate. By contrast, the clear gate itself directly overlaps with the external gate. Due to capacitive coupling, its bias condition therefore influences the internal gate potential. Figure 4.29 shows the resulting change in the nonlinear response curves for clear gate low voltages V_{CG}^{low} between -1 V and -5 V measured for a DSSC-type DEPFET in the SG variant.

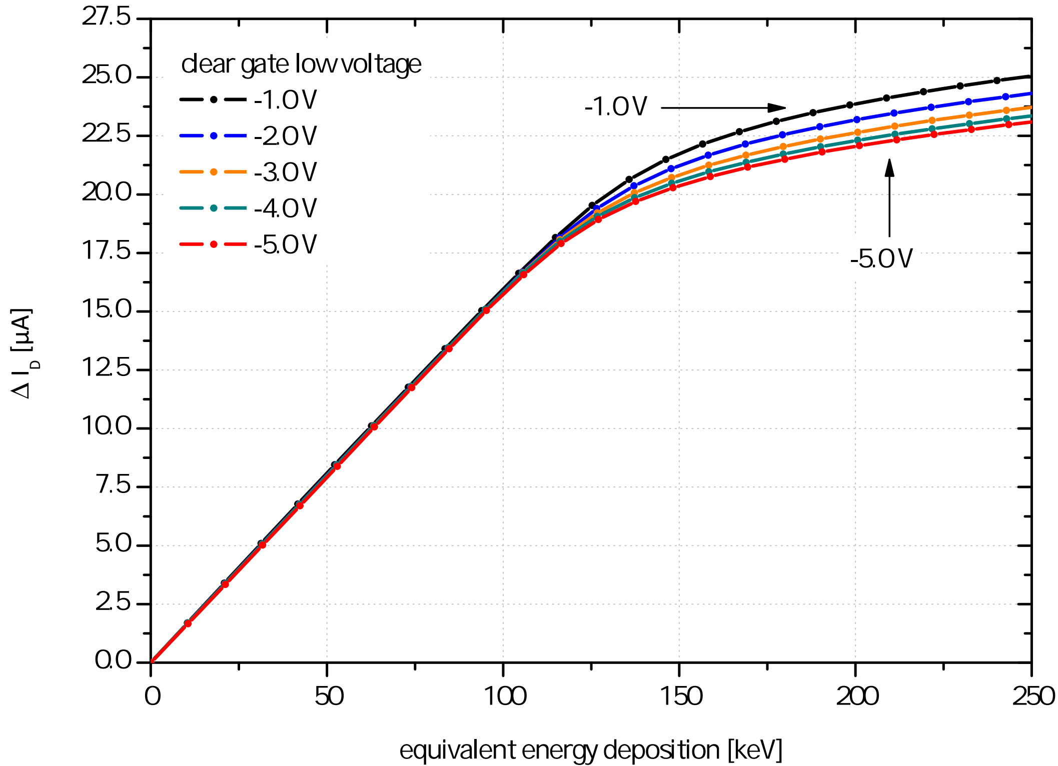

Figure 4.29: *Measured nonlinear response curves for a single pixel in the SG variant for clear gate low V_{CG}^{low} voltages in the range from -1 V to -5 V. The amplification for small signals g_q^{lin} stays unchanged but kink energy E_{kink} is shifted toward smaller accumulated energies for more negative clear gate voltages.*

The sensitivity for small signals g_q^{lin} is independent of the clear gate low voltage but kink energy shifts to higher energies for more positive clear gate low voltages.

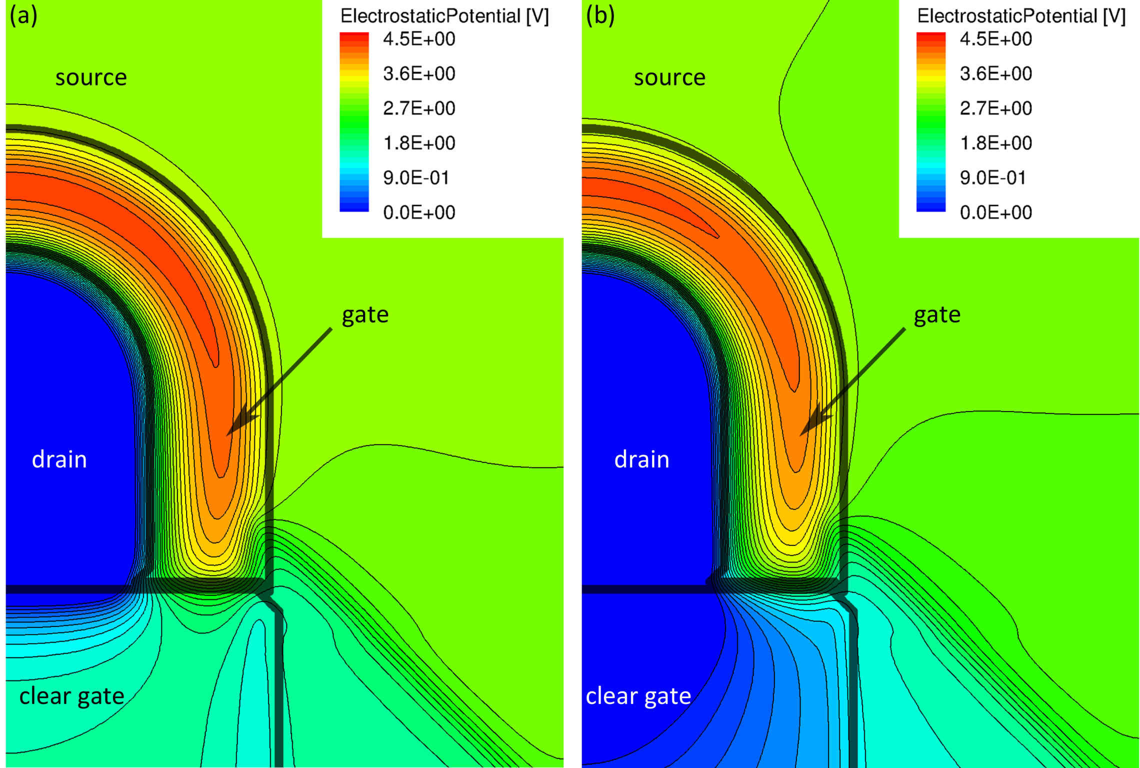

Figure 4.30: *Simulated electrostatic potential on a horizontal cut through a DSSC-DEPFET at a depth of 0.7 μm for the SG variant. The two plots illustrate the change in potential distribution due to a variation of the clear gate low voltage from -1 V (a) to -5 V (b).*

Figure 4.30 shows horizontal 2D cuts through a 3D-simulated DSSC-DEPFET in the SG variant. The depicted cuts represent the electrostatic potential for clear gate voltages of -1 V (a) and -5 V (b) at a depth of 0.7 μm below the Si-SiO_2 interface, where the potential maximum of the internal gate is located. The simulation reveals that the position of the potential maximum along the direction of the transistor channel remains the same. Independent of the clear gate voltage, small signal charges are always collected at the same location and the resulting stray capacitances do not change. The resulting sensitivity for small signals g_q^{lin} is therefore independent of the clear gate low voltage. This is in agreement with Figure 4.29.

By contrast, due to capacitive coupling the absolute electrostatic potential in the central part of the internal gate is decreased for more negative clear gate voltages. This leads to a reduction of the potential step between the central and overflow regions and thus to an earlier onset of signal compression in terms of accumulated energy. The coupling strength of the clear gate to the internal gate as well as the related shift of kink energy all depend on DEPFET geometry. On the one hand, a larger contact area between the (internal) gate

and the clear gate facilitates a fast and complete clear process but on the other hand it enhances the impact of the clear gate low voltage on the nonlinear response curve. Even if the strength of this effect is limited due to the weak coupling, it can lead to measurement errors, which depend on the primary photon energy of the XFEL, the actual nonlinear response curve of the DSSC-DEPFET sensor, and the observed photon intensity. In order to avoid these measurement errors the supporting capacitors for the clear gate low voltage have to be sufficiently large to limit their discharge and thus to suppress a change of the nonlinear response curve. If this is not feasible, the dependence of the detector response from the clear gate low voltage has to be considered by a dedicated calibration procedure.

4.3.3.3. Drain voltage

As shown in the previous sections, the impact of supply voltages on the nonlinear response curve depends on capacitive coupling of the floating internal gate to the surrounding electrostatic potentials. The coupling of the central region is strongest toward the channel, followed due to their direct vicinity by the source and the drain contact. Because the drain voltage defines both the potential within the drain implantation as well as in the channel, it has a large impact on the detector response.

Figure 4.31 shows the measured nonlinear response curves for drain voltages between -2.0 V and -5.5 V. For each curve the gate voltage V_{GS} has been adjusted to a drain current of 100 μA, allowing for the comparison of small signal amplification g_q^{lin}.

More negative drain voltages cause a strong increase of the small signal amplification. Figure 4.32 illustrates the potential distributions on a 1D cut from the drain to the overflow region of the internal gate simulated for the SG variant for drain voltages between -2 V and -5 V. The cuts are located at a depth of 0.7 μm, where the absolute potential maximum of the internal gate is reached. For more negative drain voltages, the potential maximum is pushed away from the drain resulting in a stricter confinement of the internal gate and a reduction of the stray capacitance toward the drain region. This way, a mirror charge of a signal electron is induced in the transistor channel rather than in the drain. In the case of the SG variant, a change of the drain voltage from -2 V to -5 V (see Figure 4.31) enhances the small signal amplification g_q^{lin} roughly by a factor of two.

Furthermore, a more negative drain voltage compresses the internal gate enough to be comparable to a reduction of the gate length. The consequences are lowered absolute electrostatic potential in the central region and at the same time a reduction of the potential step toward the overflow region. The strength of this effect can change depending on the geometries of the external and internal gates. A short gate length and a weak curvature of the gate increase the impact of drain voltage on the nonlinear response curve. For the illustrated SG variant the strongest change in potential occurs close to the clear gate. Due to the linear shape of the external gate in this region the impact of the central drain is enhanced compared to the circular shape far away from the clear gate. The reduction of the electrostatic potential decreases charge handling capacity in the central part and therefore

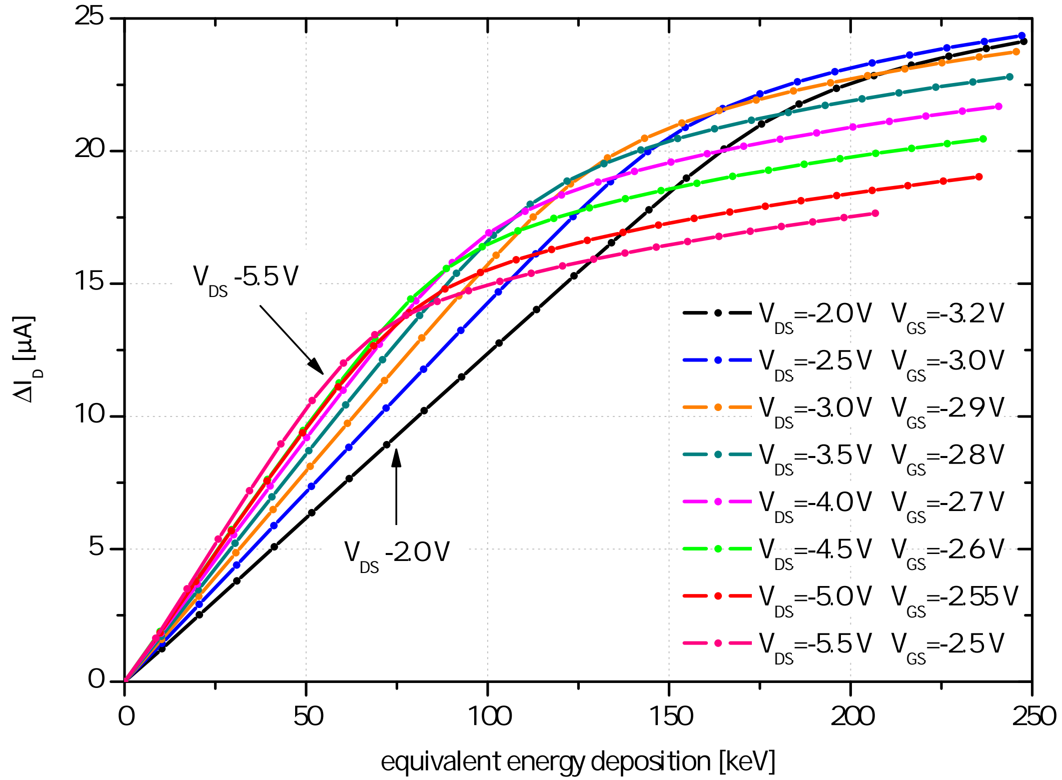

Figure 4.31: *Measured nonlinear response curves for a single pixel in the SG variant for drain voltages V_{DS} between -2 V and -5.5 V. For comparability reasons the gate voltage V_{GS} has always been adjusted to a drain current of $I_D = 100\ \mu A$. For more negative drain voltages the amplification for small signals g_q^{lin} is increased and the kink energy E_{kink} is shifted toward smaller accumulated energies.*

shifts the onset of signal compression toward smaller accumulated energies. Within the investigated range of the drain voltage from -2 V down to -5.5 V the kink energy is shifted by a factor of almost five.

The basic shape of the nonlinear response curve is defined by the geometry and technology applied in DEPFET production, which has to be fixed at a certain point in the fabrication process. The controllability of the nonlinear response curve using the drain voltage is therefore an important feature because it allows to adjust the amplification properties of the DSSC-DEPFET within certain boundaries even after production. This can be very useful in the case of a change in the primary photon energy in the XFEL. Let's assume a DEPFET sensor is customized for linear amplification ranging up to an equivalent energy deposition of 120 keV, which corresponds to 40 photons each with an energy of 3 keV. In this case a reduction of primary photon energy down to 500 eV would lead to linear amplification for the first 240 photons. The resulting dynamic range would be drastically decreased because the sensor provides a linear response for almost all available 256 bins of the 8-bit ADC, making the advantage of nonlinear DEPFET amplification obsolete. The adaptation of the response curve via the drain voltage allows us to control onset energy for

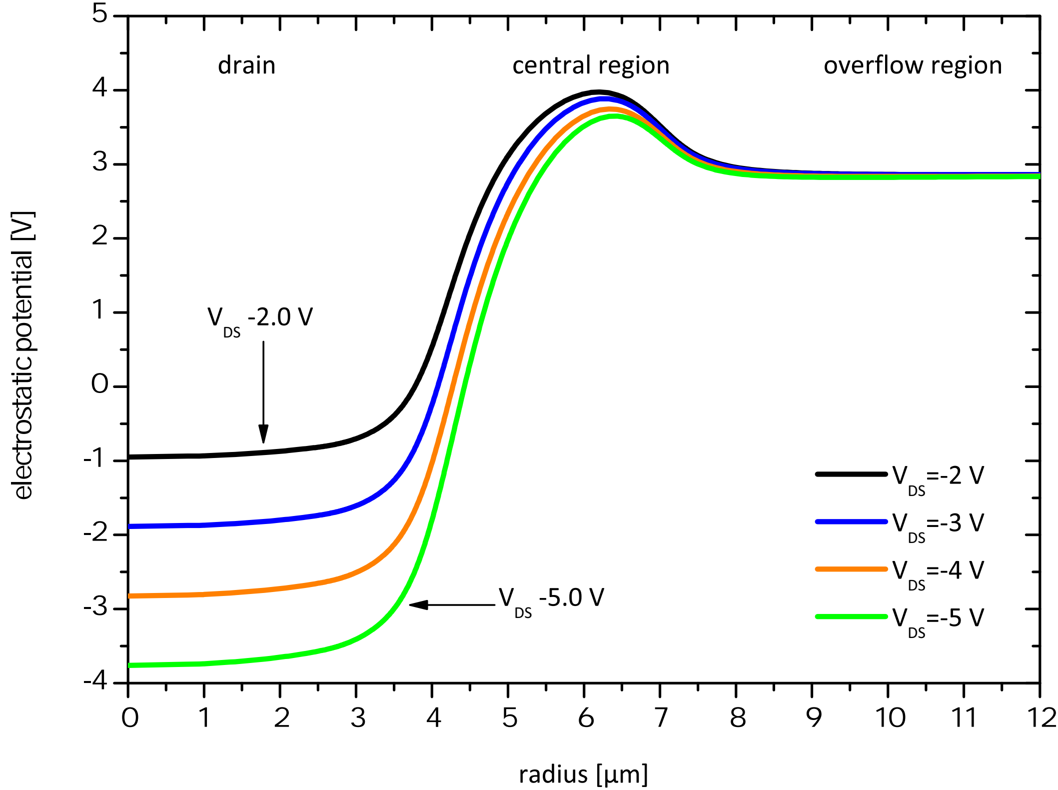

Figure 4.32: *Simulated electrostatic potential on a horizontal cut through a DSSC-DEPFET in SG geometry at a depth of 0.7* µm*. The plot illustrates the change in potential distribution due to a drain voltage change from -2 V to -5 V.*

signal compression in order to cope with different photon energies and thus guarantees the high dynamic range of the DSSC detector system.

4.4. Internal charge injection

In section 4.3.3 we discussed calibration of the nonlinear response curve using an external pulsed laser. Although this procedure is well suited for laboratory-based studies of available prototype structures, it is not applicable for a full DSSC detector. On the one hand, each prototype has only seven cells so measuring the individual pixel characteristics can be performed successively. On the other hand, the radiation entrance window of these structures has been fabricated without aluminum on top in order to allow unimpeded penetration of optical light into the active volume of the DEPFET. By contrast, the final DSSC-DEPFET sensors will be provided with a lightproof aluminum layer on top of the entrance window as a filter for optical light with an average attenuation of 10^{-6}. This is necessary to avoid spoiling the X-ray signal with optical stray light from surrounding experimental instrumentation such as optical lasers used for pump-and-probe experiments. In addition, the DSSC detector will comprise one million pixels making a certain degree of parallelization of the calibration procedure mandatory since the required time for calibration

should be minimized. In order to cope with these boundary conditions, calibrating the DSSC detector would require an external pulsed laser with an optical peak power of several kWs. Handling such lasers and distributing light evenly to the pixels under calibration would be very challenging and costly. Additionally, most of the light produced would be reflected from the aluminum layer and it would have to be ensured that this intense stray light does not damage any other equipment in the vacuum chamber. The applicability of external lasers for the in-situ calibration of a DSSC detector system is therefore very limited.

Another way of generating charge that could theoretically be used for measuring nonlinear response curves is the leakage current within the active volume of the pixels. Indeed, this method has already been verified for prototype structures. Due to the low leakage current of less than 100 pA/cm^2 at room temperature, and with the given DSSC pixel size, a time of roughly 100 ms is required to generate a charge equivalent to an energy deposition of 100 keV. At the DSSC operating temperature of -20°C this would take several seconds because leakage current $I_{leakage}$ depends exponentially on device temperature T according to

$$I_{leakage} \propto T^{3/2} \cdot e^{-\frac{E_{gap}}{k_B T}} \tag{4.28}$$

with E_{gap} as the energy of the band gap and k_B as the Boltzmann constant [65]. Depending on primary photon energy, the dynamic range of a DSSC detector goes up to energy depositions of several MeV. Thermal generation of the amount of signal charge needed for calibration would take many seconds. During this time the system has to be at least partially in the on-state, which is impossible due to the high power consumption of the DSSC detector and its limited thermal budget (compare section 2.4).

The third option for generating charge for calibration purposes is to inject signal electrons via n-doped contacts within each pixel. In principle, either the clear or the inner substrate contact can be utilized.

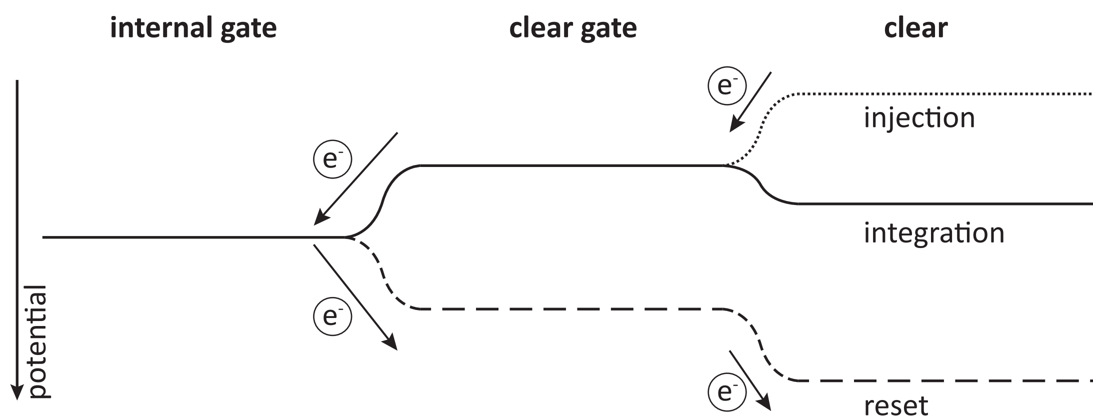

Figure 4.33: *Simplified view of potential distribution on a cut from the internal gate to the clear contact during the integration phase (solid line), the clear process (dashed line) and the electron injection from the clear into the internal gate (dotted line).*

The clear contact is located in the center of the pixel and in the direct vicinity of the internal gate. Figure 4.33 illustrates a simplified scheme of the potential distribution on a cut from the internal gate to the clear contact for all operating conditions. The solid line depicts the situation during the integration phase. The clear gate forms a potential barrier for electrons in order to avoid charge transfer between the clear and the internal gate. The dashed line represents the clear process when electrons are extracted from the internal gate. The potential gradient facilitates the drift of electrons from the internal gate into the clear contact. If the drift direction is to be inverted, a distribution as indicated by the dotted line has to be enforced. Besides the high and low levels of the clear this would necessitate an additional injection level. Since the available SWITCHERs do not support three-level switching, two SWITCHERs have to be connected sequentially to provide all required clear levels for DEPFET calibration.

Apart from this technical issue, which can be solved on an engineering level, a fundamental problem arises from the change in internal gate potential due to collected signal charge. For larger signal charges, internal gate potential becomes more negative since the remaining positive space charge is diminished. Due to capacitive coupling, this may also involve a decrease in floating potential under the clear gate and a less forward biasing of the injecting clear diode. Consequently, the charge amount of a single injection pulse is reduced for higher fill levels of the internal gate. It is expected that this limits the reproducibility of the injection pulses required for a highly precise calibration and thus makes the clear contact inappropriate for the calibration procedure. For this reason, the use of the inner substrate contact for calibration purposes is preferred and is discussed in detail in the following sections.

4.4.1. Charge injection using the inner substrate contact

As described in chapter 4.1.2 the inner substrate (IS) contact is placed in a nonimplanted notch in the inner drift ring. Its genuine function is that of a sink electrode for electrons generated at the oxide interfaces in the nonimplanted regions between the source and the drift rings. Without the IS, surface-generated electrons would contribute to the leakage current and limit the maximum voltage difference that can be applied between source/ring1 and ring1/ring2. A 3D simulation of a simplified device was performed in order to illustrate its functional principle. The 3D structure and the actual doping profiles are depicted in Figure 4.34.

The structure includes half of the overflow region with a clear contact in the center. The clear is encapsulated by a clear gate comparable to a standard DEPFET and allows for the reset of the internal gate. Since the simulation focuses only on IS contact operation, the DEPFET gate and thus the central part of the internal gate are omitted. Like in the real device, a high-dose p implantation (POXN) is placed at the outer rim of the overflow region to separate the internal gate from the drift ring. To maintain electrical isolation between the source and the drift ring, this low resistive p implantation is discontinued

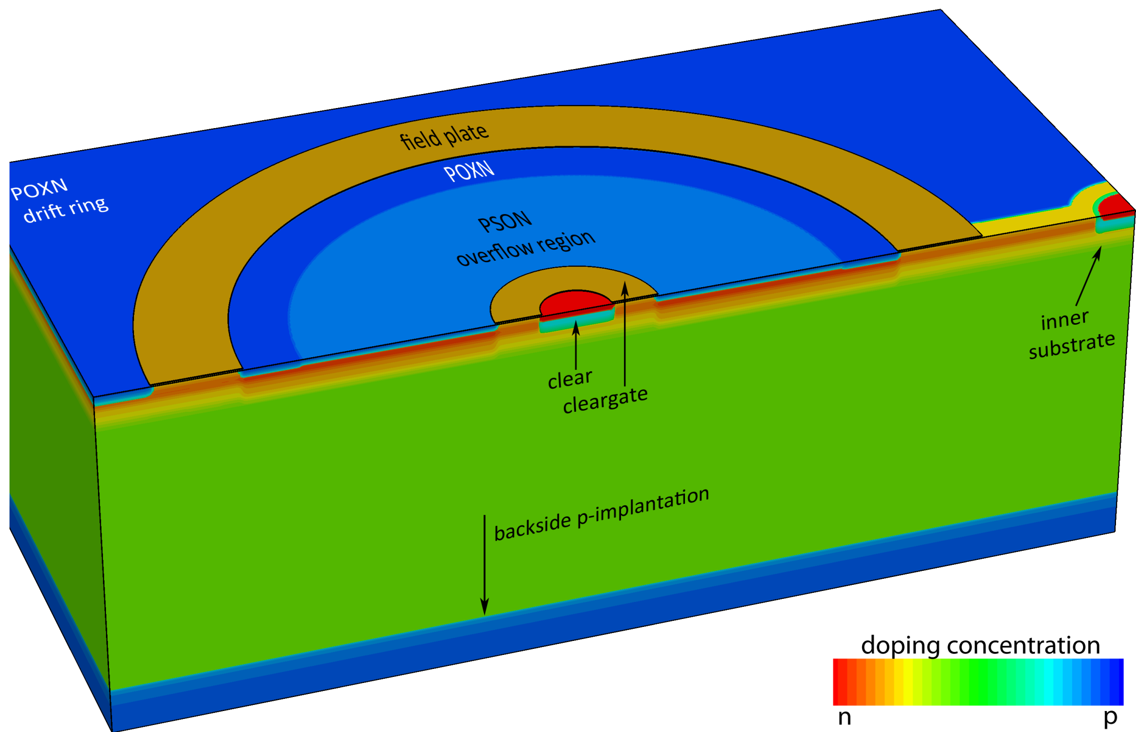

Figure 4.34: *Three-dimensional structure of the simplified test device utilized to simulate the internal charge injection. The color code illustrates doping concentrations with n-doping in red and p-doping in blue. The structure comprises the IS contact, a drift ring, a half circle of the inner field plate, the overflow region and a small clear contact to fully deplete the internal gate.*

underneath the field plate. The IS is placed within the drift ring and consists of a high-dose n implantation embedded in a p-doped well in order to prevent the loss of signal charge. The IS is connected to the field plate region by a narrow channel without POXN implantation to avoid a potential barrier for electrons.

To minimize the simulation area and run the simulation within a reasonable computation time, the radius of the field plate is reduced relative to the real DSSC layout, which certainly has an impact on absolute electrostatic potentials in the device. In particular, the potential under the field plate and in the overflow region of the internal gate is decreased since the enhanced curvature of the MOS gate increases the influence of the negative ring voltage on the potential distribution. Apart from this, the main working principle of the IS remains the same.

The resulting potential distribution within this 3D structure during the integration phase of the DEPFET is shown in Figure 4.35. The clear structure is deactivated and thus the internal gate (overflow region) is the most attractive region for electrons. At the outer rim of the source, the POXN implantation forms a potential barrier for electrons toward the field plate region, which means signal charge cannot escape from the internal gate once it has arrived. It also prevents surface-generated leakage current from the field plate region from entering the internal gate and eliminates its contribution to the signal charge. As a

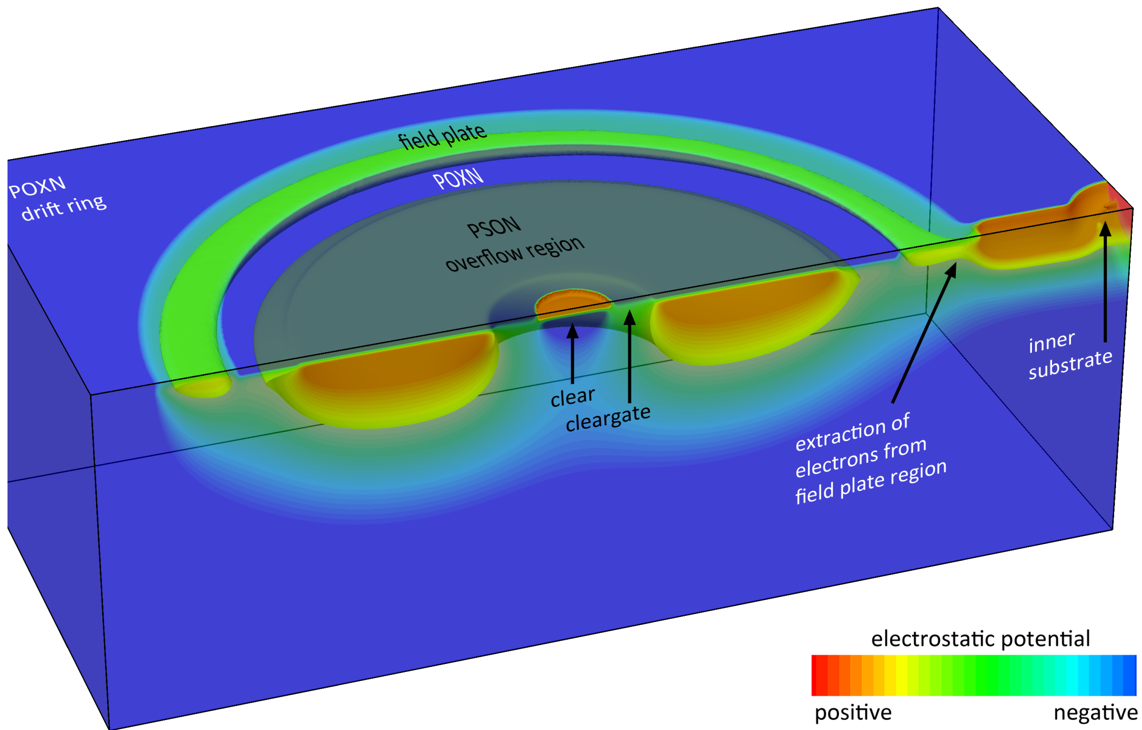

Figure 4.35: *Simulated electrostatic potential in the test device during the integration phase of the DEPFET. The equipotential surfaces indicate the potential barrier between the internal gate and the field plate region. Electrons generated on the surface below the field plate are extracted from the field plate region by the positively biased IS contact.*

result, charge accumulates under the MOS gate and is extracted from the device via the IS, which features the most positive potential within the local potential valley.

Since the electrical field induced by the IS is only present in its direct vicinity, the charge transfer under the field plate is mainly based on diffusion. This limits the velocity of electron extraction and results in an equilibrium of their generation and extraction, which in turn means that there are some electrons under the field plate at all times. The IS ensures, however, that the available amount of charge is insufficient to compensate the potential barrier toward the overflow region and thus prevents thermally-generated electrons from entering the internal gate. This situation has to be created in order to successfully inject electrons from the IS into the internal gate.
Electrons can be injected by decreasing IS voltage and biasing the IS diode in a forward direction. Initially, the local potential valley under the field plate is filled up with electrons compensating the current space charge. At a certain fill level the potential barrier towards the internal gate is lowered enough so that injected electrons can spill over into the internal gate where they can be used for calibration purposes.

Figure 4.36 illustrates the simulated potential distribution on a 2D cut through the device at a depth of 0.65 μm 20 ns after the beginning of the injection phase. At this moment, the injected electrons have just entered a small part of the field plate region and the potential

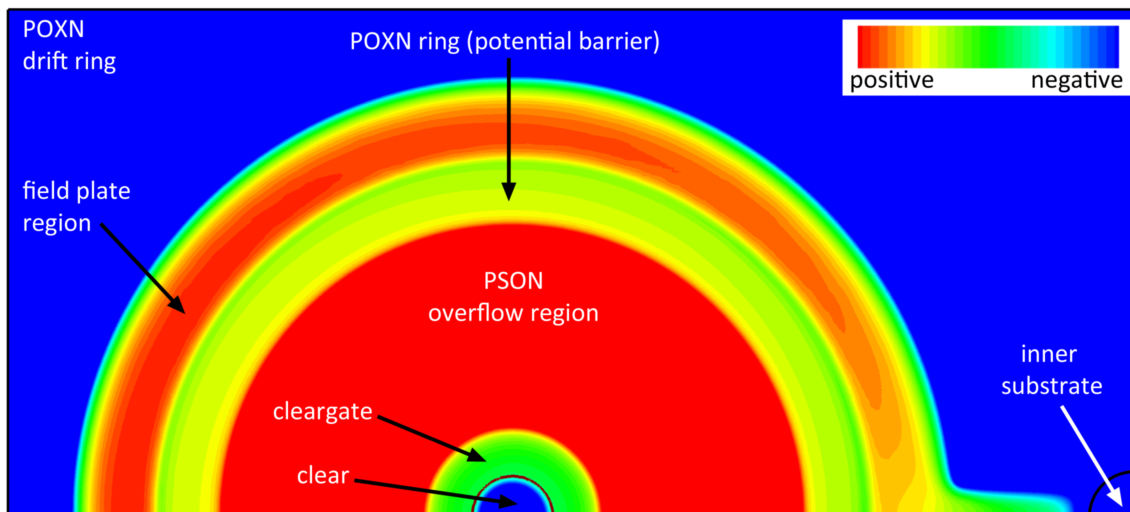

Figure 4.36: *Simulated electrostatic potential on a horizontal cut through the test device at a depth of 0.65 μm 20 ns after the injection voltage is applied to the IS contact. The POXN ring at the outer rim of the source forms a potential barrier between the overflow region and the field plate region. This barrier is lowered in the vicinity of the IS due to injected electrons.*

barrier toward the internal gate is only reduced in the vicinity of the IS contact. The main part of the field plate region is still fully depleted and the potential barrier is comparable to levels during the integration phase. This indicates that the filling process is transient and the resulting spillover of electrons into the internal gate will not be homogeneous from all directions. Instead, it will start close to the IS and for longer injection pulses the region where the spillover occurs will be extended. This also applies for higher injection amplitudes, which enhance the velocity of the diffusion process under the field plate due to stronger gradients of electron density. A time sequence for a 200-ns-long injection pulse starting from a fully depleted field plate region can be found in Appendix B
The simulation shows us how complex this transient process is, but it cannot provide any quantitative results. That would require modeling the real DSSC device geometry, which is still not possible since the computation is prohibitively time-consuming.
The number of electrons arriving in the internal gate from a single injection pulse N_{inj} is given by

$$N_{inj} = \frac{\int_0^{t_{inj}} I_{inj}(t)\, dt}{e} - N_{fpr} \tag{4.29}$$

with e as the elementary charge, I_{inj} as the injection current at the IS contact, t_{inj} as the duration of the injection pulse and N_{fpr} as the number of injected electrons remaining in the field plate region and not entering the internal gate.
The IS contact can be seen as a simple diode but the analytical determination of the corresponding injection current is complex because only the n-doped contact is directly connected and the p-doped well is floating. The potential of the floating p-well is defined by capacitive coupling to the surrounding potentials and by the degree of depletion related

to the history of the device operation. In the case of electron injection, all available holes recombine almost instantaneously, but with the injection of electrons the electrostatic potential under the field plate decreases along with that of the floating p-well. Therefore, the filling process leads to a transient reduction of the injection current until static potential distribution is established.

The number of injected electrons remaining in the field plate region N_{fpr} is even more complex to specify. In the case of a quasi-static fill-up, N_{fpr} is defined by the size of the field plate region and the current potential barrier toward the internal gate. Once the potential barrier is compensated, all additionally injected electrons will spill over into the internal gate. For injection pulses in the sub-μs range, the fill-up is a dynamic process. This means even if the spillover has begun locally, only some of the additional electrons injected will enter the internal gate but others will continue filling up the field plate region. Another aggravating circumstance is that if the temporal spacing between two injection pulses is too short, not all electrons are extracted from the field plate region before the subsequent injection pulse takes place. Those remaining electrons will partially compensate the positive space charge under the field plate, which locally decreases the potential barrier toward the internal gate. In this case N_{inj} is enhanced for higher prefill levels of the field plate region with electrons at the beginning of the injection.

It must be pointed out here that the so-called "prefill" level is in fact a locally inhomogeneous electron distribution. It depends on the duration and amplitude of the previous injection pulse and on the last electron extraction process. Even if all contributing effects can only be described qualitatively, the newly introduced measurement sequence presented in the following section is able to provide an identical prefill level for all injection pulses and hence to guarantee reproducible amounts of injected signal charge.

4.4.2. Measurement sequences

Figure 4.37 shows the readout sequence used to determine the nonlinear pixel response with the IS contact as an internal source for signal charge. The procedure is similar to the external pulsed laser method described in section 4.3.1.

At the beginning of the sequence, the internal gate is reset by applying a positive voltage pulse to the clear and the clear gate. Immediately after the reset, no electrons are present in the internal gate and the baseline is sampled. Then injection pulses identical in width and amplitude are applied. After each injection pulse, the DEPFET current is sampled. Since between the injection pulses no clear action is performed, the signal charge accumulates in the internal gate and increases with each injection. The injection pulses and individual readouts are equally distributed in time and their temporal spacing is indicted by t_{int}. Between the injections and the subsequent readout there is an offset in time t_{off}. The injected electrons reach the internal gate and find their equilibrium distribution during t_{off}.

The number of signal charges N_{IG} arriving in the internal gate between readouts consists

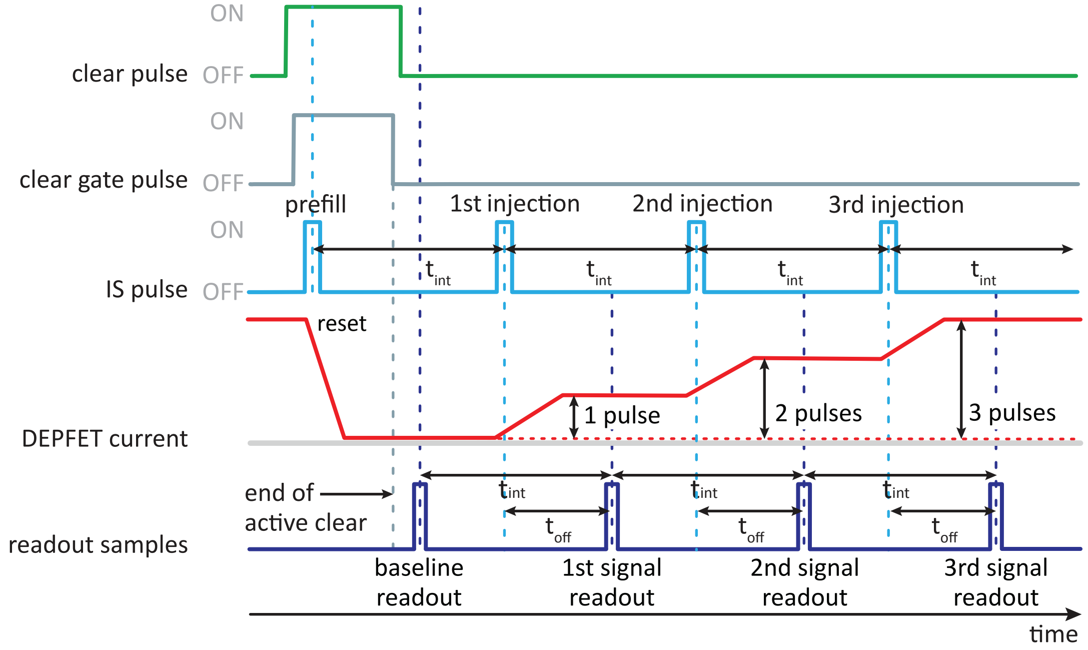

Figure 4.37: *Illustration of the measurements sequence for scanning the nonlinear response curve of a DSSC-DEPFET using internal charge injection via the IS contact. The baseline is sampled after a clear pulse. Then alternating injection pulses are applied and the resulting DEPFET output signal is sampled. The "prefill" pulse during the clear phase guarantees an identical prefill condition of the field plate region for all injections and thus ensures a reproducible injection strength.*

of two components: the electrons generated thermally within the active volume of the DEPFET pixel $N_{leakage}$ and the electrons injected by one IS pulse N_{inj}.

$$N_{IG} = N_{leakage} + N_{inj} \tag{4.30}$$

Both contributions have to be constant in order to create reproducible steps of signal charge. For $N_{leakage}$ this is achieved via uniform temporal spacing between the readouts that define the integration time of the present leakage current. For a stable N_{inj} not only the width and the amplitude of the voltage pulses but, as discussed in the previous section, also the prefill level of electrons in the field plate region has to be the same at the beginning of each injection. If the time interval between two injections t_{int} is too short the charge distribution in the device does not reach a state of equilibrium in the sense that the field plate region is depleted of electrons. In this case, the prefill level depends on the duration and amplitude of the previous injection and on the last electron extraction process. Due to the repetitive sequence, the prefill level for the second and all subsequent injection pulses is the same. In order to provide identical conditions for the first pulse as well, an additional prefill pulse identical in width and amplitude has to be applied during the clear. That way the potential pocket under the field plate is filled while all electrons that overcome the

potential barrier and reach the internal gate are removed by the clear contact.
Measurements have shown that without prefill, N_{inj} for the first pulse is systematically smaller than for subsequent injections. The deviation can easily exceed 25% whereas with the measurement sequence shown above, only statistical fluctuations on a per mill level were observed.
Table 4.12 summarizes the typical ranges for all relevant sequence parameters including t_{off}, t_{int}, t_{inj} and the voltage level of the IS during injection V_{inj} used for the measurements.

parameter	range
t_{off}	10 μs
t_{int}	12 μs
t_{inj}	50 ns up to 500 ns
V_{inj}	-0.4 V up to +0.4 V

Table 4.12: *Summary of the parameter ranges for t_{off}, t_{int}, t_{inj} and the voltage level of the IS during injection V_{inj} used for the performed measurements.*

Usually 24 injection pulses were applied within a single sequence cycle, which corresponds to a sequence duration of roughly 350 μs. Most of the time is dedicated to ensuring the complete collection of injected charge in the internal gate (t_{off} and t_{int}). The sequence can definitely be shortened for the DSSC detector since the charge collection of the final sensor will be much faster. Additionally, the same calibration accuracy can be achieved with much less measurement points using dedicated fit algorithms. A detailed discussion of this can be found in [69].

4.4.3. Validation of the internal charge injection

In order to validate the internal charge injection method, the newly introduced measurement sequence was used to determine the nonlinear response curve of a DSSC prototype pixel in the SG variant. The DEPFET output spectra for an increasing number of injection pulses was recorded by cycling the sequence 10^5 times.
Figure 4.38 (a) depicts the obtained spectra for injection pulses with a duration of t_{inj}=160 ns and an injection voltage of V_{inj}=+0.17 V. The resulting amount of electrons sent to the internal gate by a single injection pulse corresponds to an energy deposition of 23.6 keV. All 24 spectra show a symmetrical Gaussian peak shape comparable to the external laser method, which illustrates the stability of the injection pulses and allows for a precise determination of the peak position by using a Gaussian fit. Figure 4.38 (b) shows the nonlinear response curve for the internal injection and external laser methods. Both were derived using the calibration procedure discussed in section 4.3.1. The deviation between the two curves is on the per mill level, which demonstrates the similarity of the methods.
In order to assess the applicability of internal charge injection for all conceivable response

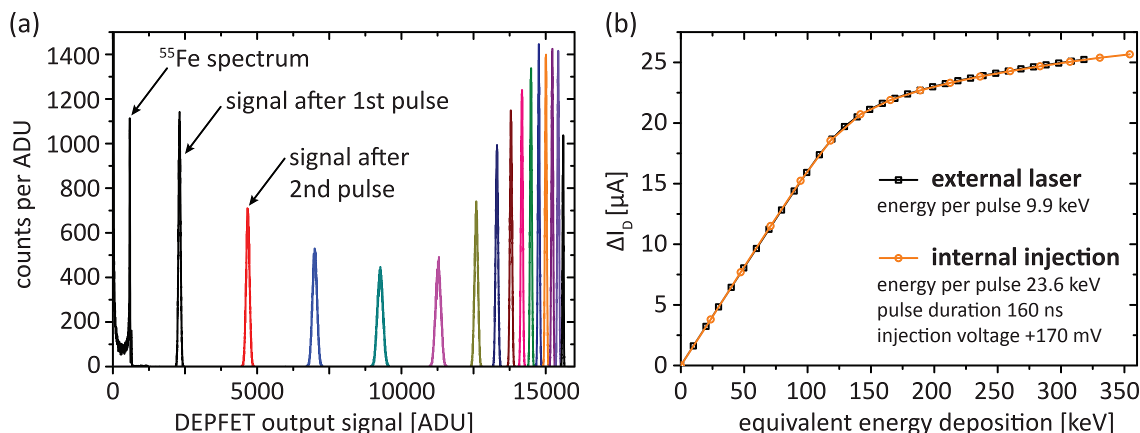

Figure 4.38: *(a) DEPFET output spectra measured for an increasing number of internal injection pulses using the new developed measurement sequence. (b) Nonlinear response curves for a single DSSC pixel in the SG variant under standard operating conditions determined once by the internal injection and once by the external laser method. The deviation between the two calibration methods are on the per mill level.*

curves, however, the granularity of the scan must be adjustable. Therefore, a set of measurements was performed with varying durations and amplitudes of the voltage pulse at the IS contact. All other timing parameters of the sequence such as t_{int} and t_{off} were unchanged, as were the remaining supply voltages.

Figure 4.39 illustrates the equivalent energy deposition per injection pulse as a function of its voltage amplitude. The color-coded curves represent the tested pulse durations between 50 ns and 250 ns and the symbols indicate the tested injection voltages. Since the internal charge injection is based on a forward-biased diode, the equivalent energy deposition per pulse shows exponential dependence on the injection voltage V_{inj}. Since the y-axis is not normalized to the pulse duration, an enhanced arch in the curves can be observed for longer injections. Equation 4.29 already indicated that shorter injection pulses require a more negative V_{inj} to obtain an equal number of injected electrons in the internal gate.

Figure 4.40 illustrates the equivalent energy deposition as a function of the pulse duration for constant V_{inj}. This corresponds to vertical cuts through the curves depicted in Figure 4.39. Although individual curves comprise no more than three measurement points due to the coarse grid of the tested pulse durations, a nonlinear dependence shows up. In the case of a quasi-static fill-up of the field plate region the electron current sent to the internal gate would be constant in time once the spillover has started. This would result in a linear relationship between N_{inj} and the injection time t_{inj}. The measurements therefore clearly confirm that the fill-up is a transient process. To generate a qualitative explanation of this dependence, the injection process was simulated taking into account the measurement sequence discussed in the previous section. In the simulations t_{int} has always been set to 5 μs to guarantee a consistent extraction process for electrons from the field plate region between the injections. The simulated electron density on a horizontal 2D cut through the

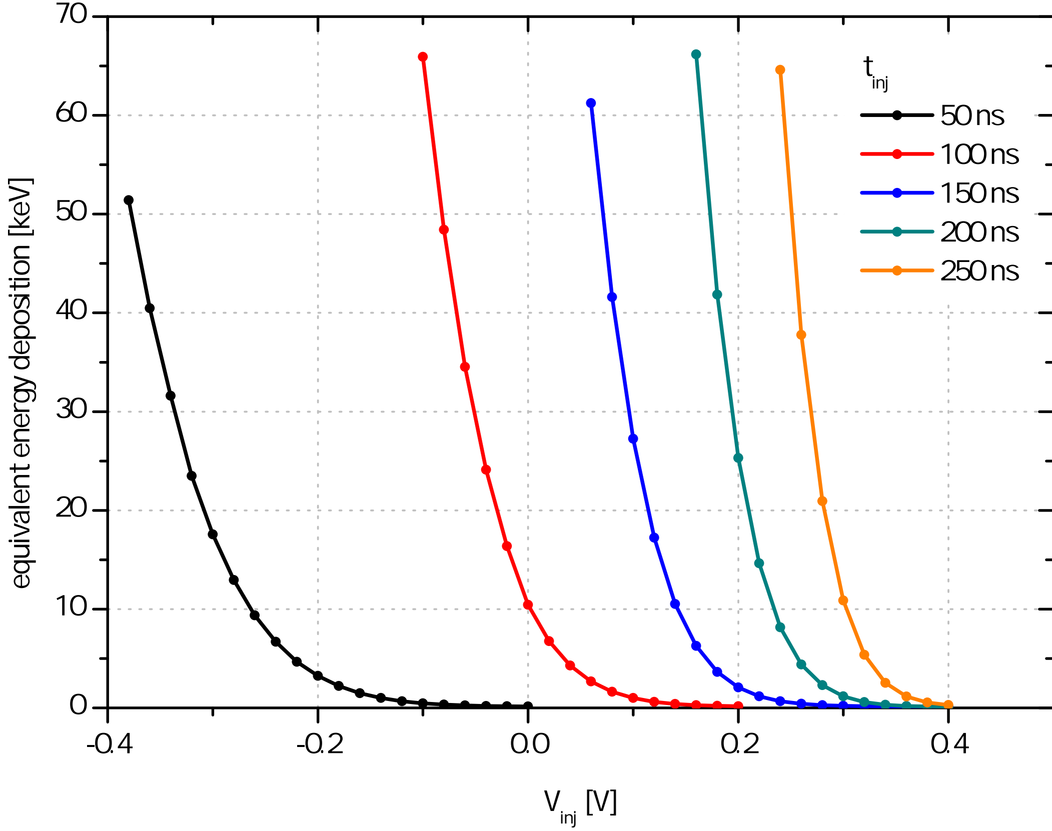

Figure 4.39: *Equivalent energy deposition per injection as a function of the amplitude of the voltage pulse applied to the IS. The tested pulse durations between 50 ns and 250 ns are color-coded and the symbols mark the tested injection voltages.*

test device is shown in Figure 4.41 for pulse durations of 100 ns (a) and 300 ns (b).

The plots on the left illustrate the prefill level at the beginning of the first injection. It is enhanced for the longer pulse (b) because more charge enters the devices and remains there after the extraction phase, which is too short for a full depletion of the field plate region. Therefore, fewer electrons have to be spent to refill the gap between the source and the drift ring before the spillover begins.

This consequence shows up 70 ns after the injection voltage is applied to the IS. For both pulses the spillover began locally, close to the IS, and first electrons reached the internal gate. However, due to the higher prefill level for the longer injection pulse (b), the region where electron density could facilitate the overflow of electrons into the internal gate is extended compared to (a). At the end of the injection pulse (right plots) this effect becomes even more apparent. With increased injection times the electrons access a larger area under the field plate. The region where the spillover takes place starts localized but extends with the injection time. Even if the injection current I_{inj} is constant in time, the fraction of charge that reaches the internal gate becomes more dominant.

The combination of the discussed phenomena leads to a more than linear increase of the equivalent energy deposition with t_{inj}. However, for very long pulses the injection will reach

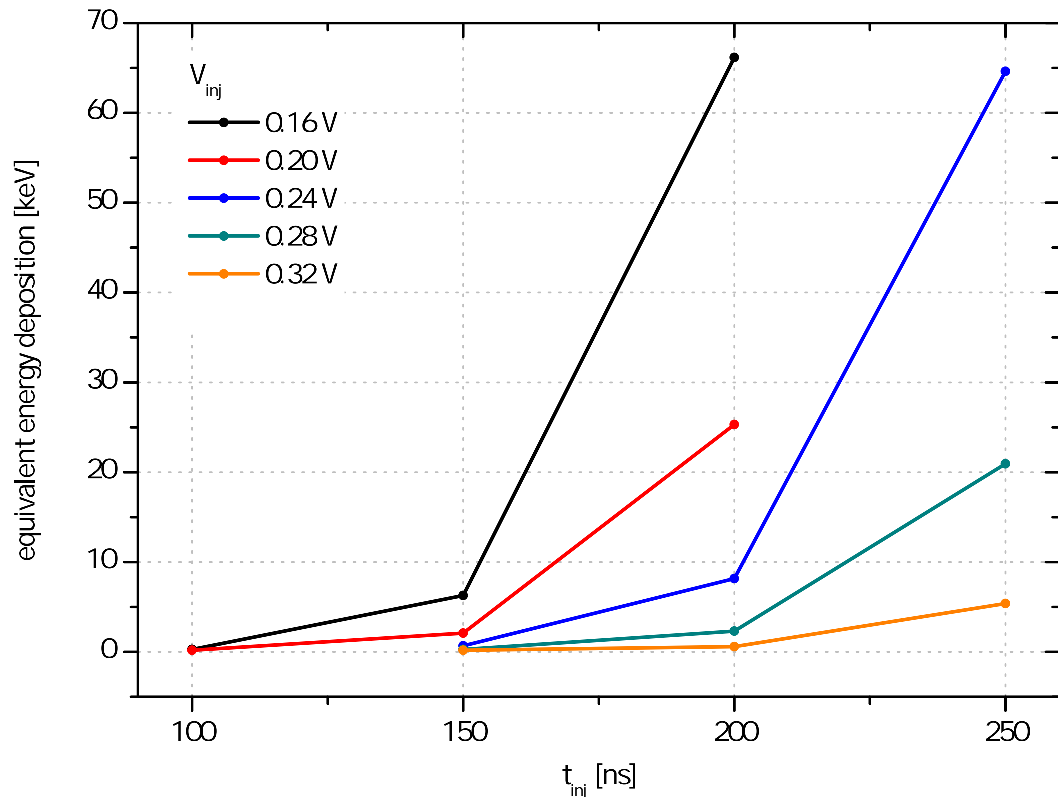

Figure 4.40: *Equivalent energy deposition per injection as a function of the pulse duration t_{int} for injection voltages between 0.16 V and 0.36 V.*

a state of equilibrium and a linear relation should appear. For the tested pulse durations up to 500 ns this behavior was not yet observed. Further experiments are necessary to specify the exact dependence here. On the one hand, a finer and wider measurement grid for the pulse durations is required to facilitate a result while on the other hand further 3D device simulations have to be performed considering the layout of the real DSSC pixel. However, this goes beyond the scope of this thesis and is not required for the application of internal charge injections for purposes of calibration.

The measurements clearly prove that the internal charge injection mechanism works over a wide range of operating parameters. They also demonstrate that this calibration technique will be able to handle the inevitable threshold variations for the onset of charge injection over a large-format array of DSSC sensor pixels which are caused by technological fluctuations during the fabrication. The new technique will therefore allow for the in-situ calibration of the DSSC detector without the need to remove the detector from the beamlines. However, its applicability for large-area sensors still has to be investigated and confirmed. Possible challenges may arise in the distribution of injector pulses with the necessary stability over a large number of pixels.

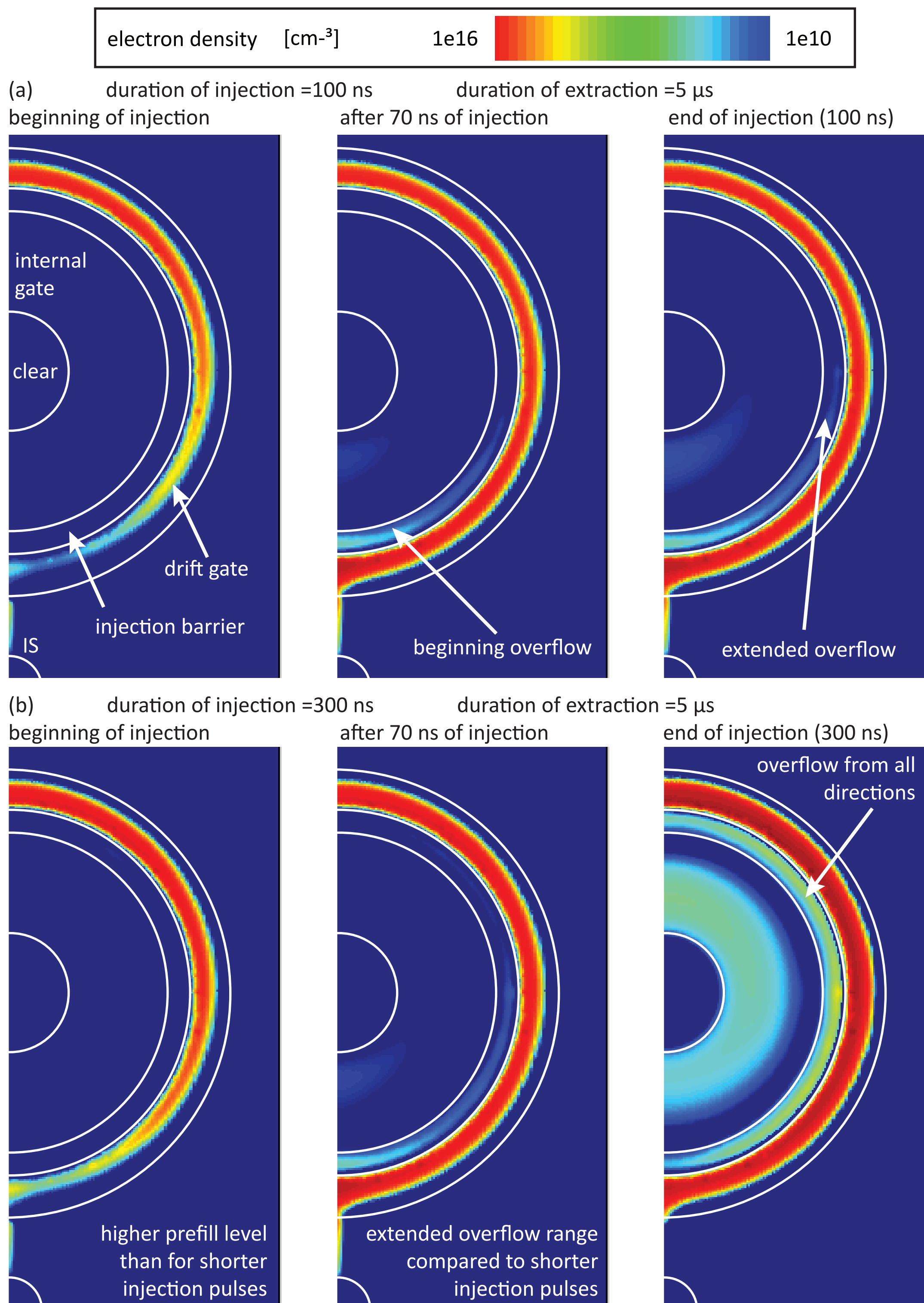

Figure 4.41: *Simulated electron density on a horizontal cut through the device at a depth of 0.8 µm at the beginning of the first injection (left), 70 ns afterwards (center) and at the end of the pulse (right). The simulation has been performed for pulse durations of 100 ns (a) and 300 ns (b) and an extraction time of 5 µs.*

5. Design of final DSSC sensors

The first DEPFET prototypes featuring nonlinear amplification were designed with the aim of confirming the basic mechanism of analog signal compression. As presented in the previous chapter, they also allowed for comprehensive studies of the device and thus contributed significantly to a better understanding of the physical processes involved. Nevertheless, these structures have been fabricated on a multiproject level and the technology was a compromise to meet the requirements for different applications. This resulted in the three main limitations of the DSSC-DEPFET prototypes:

- limited radiation hardness
- slow charge collection speed
- a basic nonlinear response curve with only one compression level

This chapter demonstrates how these limitations can be eliminated with dedicated production technology and presents the expected performance of the final DSSC sensors.

5.1. Radiation hardness

In the DSSC application at the European XFEL, the DEPFET will have to cope with extremely high radiation levels. Assuming a primary photon energy of 12 keV and a 500 μm thick silicon sensor, a worst-case scenario delivers a total absorbed radiation dose of 1 GGray (=100 Grad) over three years of operation [70]. This section will initially give an overview of the damaging mechanism with results of radiation hardness tests of DEPFETs fabricated using the standard technology. Then the radiation hardening measures will be discussed along with the overall improvements that were achieved.

5.1.1. Damaging mechanism

The main degradation effect of DEPFETs due to X-ray photons is based on the charge generation in the gate oxides. Whenever X-rays penetrate an oxide they can ionize atoms and create electron-hole pairs. As long as the kinetic energy of the resulting electrons and holes is sufficiently high, they will in turn excite additional electron-hole pairs. This cascade effect is only stopped by the lack of kinetic energy of the charge carriers involved. For silicon dioxide, on average 18 eV is required for a single excitation process [71].
After being generated, the electron-hole pairs can immediately recombine or they can

separate, either by their thermal movement or by the presence of an electric field. Taking into account electron-hole pair generation, the specific hole density that escapes this initial recombination process n_h is given by [72]

$$n_h = D \cdot t_{ox} \cdot g_0 \cdot f(E_{ox}). \tag{5.1}$$

Here D denotes the total absorbed radiation dose, t_{ox} the oxide thickness and g_0 a material-dependent parameter corresponding to the initial charge pair density per rad of dose ($g_0^{SiO_2}$=8.1 $\cdot$ 10^{12} pairs/cm^3 [72]). The term $f(E_{ox})$ represents the so-called hole yield - the fraction of generated holes that do not recombine with an electron. This is a monotonic function that increases with the electric field strength since the field speeds up the separation process of the electron-hole pair and shortens the available time for recombination [73].
In case of an existing electric field in the oxide, the electron and the hole will start moving in opposite directions immediately after their generation.

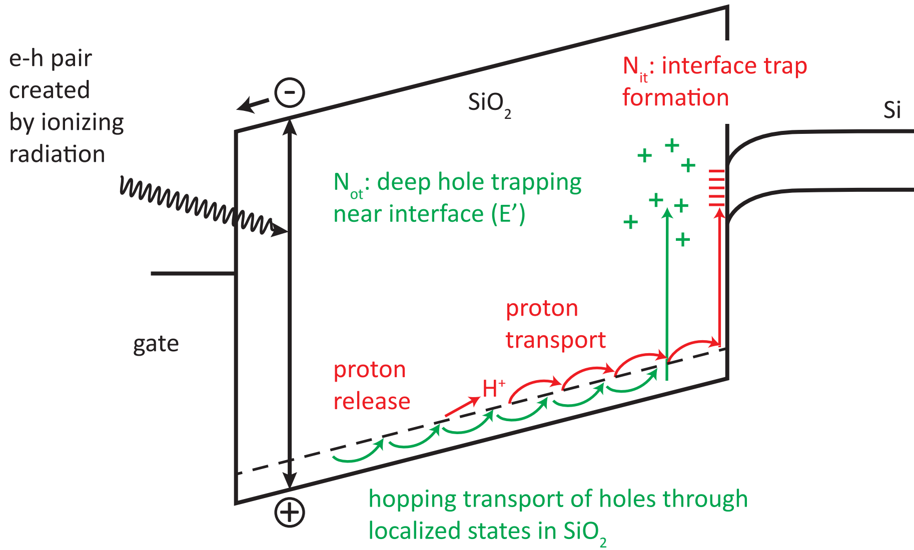

Figure 5.1: *Band diagram of the MOS structure for positive gate biasing. Radiation induced electron-hole pairs are separated by the electric field in the oxide. While approaching the* Si-SiO$_2$ *interface the hole can get trapped within the oxide or cause interface traps [74].*

For positive gate biasing, as illustrated in Figure 5.1, the electrons drift toward the gate interface. Due to their high mobility, most are swept out of the oxide within several picoseconds [75, 76]. By contrast, hole transport is directed towards the Si-SiO$_2$ interface and is much slower since it is based on hopping through localized states [74]. While approaching the interface the holes can either get trapped within the oxide - forming oxide-trapped charge - or they can cause interface traps by various mechanisms.
Hole trapping in the oxide occurs mainly in a 5-20 nm thin layer above the Si-SiO$_2$ interface. In this region there is an increased density of oxygen vacancies due to the outdiffusion of oxygen in the oxide [77]. Furthermore, the lattice mismatch causes a large number of strained Si-Si bonds, which can easily capture a passing hole. In this case the hole can

recombine with an electron of the covalent bond forming a so-called E' center [78–80] according to:

The hole-capture cross section close to the interface depends strongly on the device fabrication defining the number of available traps. For radiation-hardened oxides, trap density is minimized and the capturing probability can be decreased down to a few percent compared with more than 50% for radiation soft oxides [74].
In addition to the oxide-trapped charge, radiation-induced holes can also cause interface traps. The microscopic formation process of these traps is still under investigation and many models based on various mechanisms have been proposed. An overview of them can be found in [81]. One commonly known mechanism is based on hydrogen atoms (protons) that are likely released as holes move through the oxide or as holes are trapped near the Si-SiO_2 interface. The protons also migrate to the interface, where they can crack weak Si-H bonds and react to the molecular hydrogen. The remaining dangling bonds of the involved silicon atoms can subsequently act as an interface trap [74, 82] enhancing 1/f-noise (compare section 3.3.3) and reducing hole mobility in the channel. Since the DSSC does not focus on spectroscopy but on photon counting, the consequences of the higher noise only becomes apparent in cases of massive degradation.
For the DSSC, an acceptable irradiation level is limited by the overall positive charging of the gate insulator. Although the interface traps are amphoteric, which means that they can be neutral, positively or negatively charged, the positive charge state dominates in the case of the p channel transistor of the DEPFET. For an increasing radiation dose, the oxide- and interface-trapped charge will accumulate and result in a positively charged oxide. This leads to a threshold voltage shift in the transistor to more negative gate voltages according to

$$\Delta V_{th} = \frac{-1}{C_{ox} t_{ox}} \int_0^{t_{ox}} \rho_{ot,it}(x) x \, dx \tag{5.2}$$

with C_{ox} as the oxide capacitance per unit area, t_{ox} as the oxide thickness and $\rho_{ot,it}$ as the density of oxide- and interface-trapped charge [74].
Since hole trapping probability is not homogeneous in the oxide but highest close to the interface, we see that threshold voltage shift is dependent on gate voltage, as shown in Figure 5.2.

The highest oxide and interface trap density and thus the largest trapping probability is located close to the Si-SiO_2 interface. For positive gate bias, the holes migrate toward this region and the buildup of positive oxide charge is favored. While applying negative gate voltage, the holes drift toward the gate and the lower trapping probability inhibits the accumulation of positive oxide charge. Minimum flatband voltage shift is obtained at a zero-field condition in the oxide. In this case the discussed hole yield is minimal since the separation process of excited electron-hole pairs is decelerated and the initial recombination

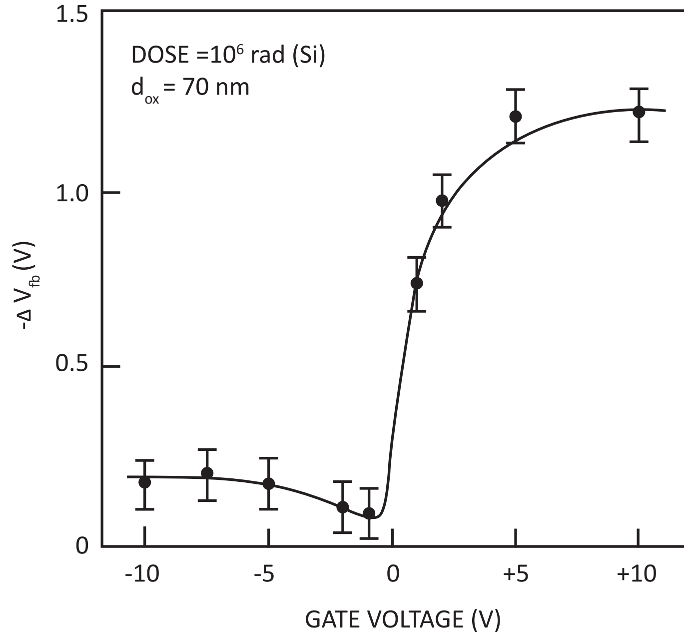

Figure 5.2: *Measured flatband voltage shift as a function of the applied gate voltage. The MOS structure with a gate oxide thickness of 70 nm was exposed to a total radiation dose corresponding to 1 Mrad in silicon. Minimum flatband voltage shift occurs at a zero-field condition in the oxide. For negative gate voltages the holes migrate to the gate-*SiO_2 *interface and* $-\Delta V_{fb}$ *is slightly enhanced. For positive gate voltages the holes drift toward the* Si-SiO_2 *interface with the highest hole trap density and* $-\Delta V_{fb}$ *increases strongly before a saturation effect arises [83].*

probability is enhanced. Furthermore, the movement of charge carriers in the oxide is omnidirectional and electrons will consequently also pass by holes, that have already been trapped. This leads to the recombination of some fraction of trapped holes and reduces the present amount of positive oxide charge.

In addition to hole trapping probability, the positive charge in the oxide also is defined by the absolute number of radiation-induced electron-hole pairs. Assuming a constant absorption rate of X-rays in the oxide, the number of electron-hole pairs generated depends linearly on the gate oxide thickness. If the distribution of trapped holes in the oxide further does not change, flatband voltage shift for a certain amount of trapped holes also decreases linearly with the gate oxide thickness. Taking both considerations into account, one can derive a square-law dependence of radiation-induced flatband voltage shift, as indicated in Figure 5.3 by the dashed line [84–86]. The depicted symbols mark measurement results for MOS capacitors irradiated at 80 K.

The experimental data obtained for oxide thicknesses above 20 nm fit quite well the theoretical model. For thinner oxides, the tunneling process of electrons from the silicon into trapped-hole states in the oxide becomes more and more dominant and the flatband voltage shift decreases sharply, limiting the applicability of the simplified model.

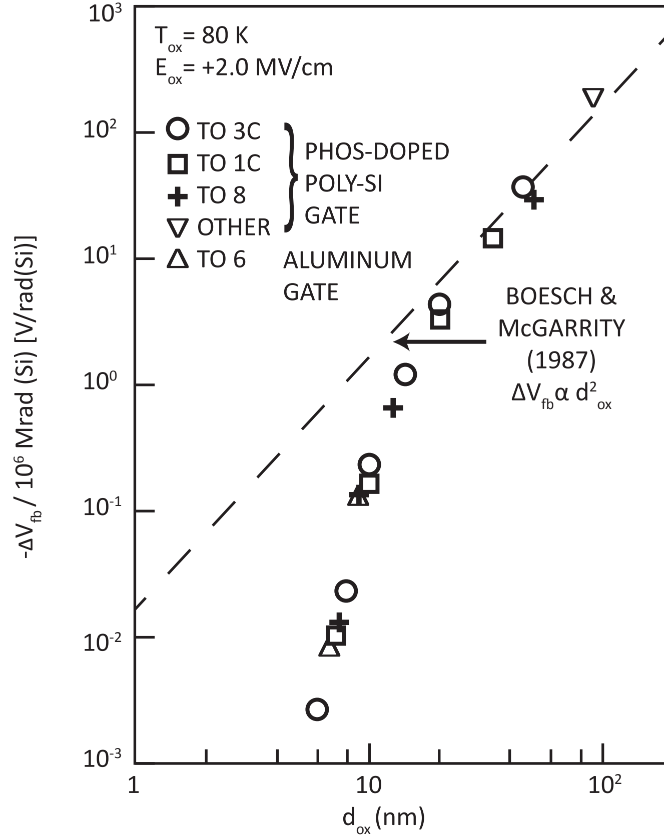

Figure 5.3: *Double logarithmic plot of the flatband voltage shift per Mrad of dose as a function of the gate oxide thickness for MOS capacitors irradiated with* Co^{60} *at 80 K. The theoretical model describing the increase of* $-\Delta V_{fb}$ *with* d_{ox}^2 *is represented by the dashed line and the symbols indicate measurement results. Deviations from the theoretical model show up for gate oxide thicknesses of less than 20 nm, when tunneling processes set in [87].*

In principle, the DEPFET can cope with a threshold voltage shift and a readjustment of the gate and clear gate voltages can compensate for that. However, in FEL applications of the DSSC, the radiation patterns on the detector will be very inhomogeneous. Some FEL experiments, mainly those focusing on crystalline targets, can cause very intense and localized Bragg peaks on the detector. In other applications a water jet is used to bring biological targets into the beam and the scattering of X-rays on the water molecules produces a bright and concentric ring on the detector around the primary beam. The shift in the flatband voltage due to radiation-induced oxide charges will therefore also be very inhomogeneous. Since supply voltages for the DSSC detector are common for big sensor areas (64 x 64 pixels), the gate and clear gate voltages are not adjustable for individual pixels.

The acceptable radiation level is therefore limited by the maximum threshold voltage spread of all MOS gates within a single sensor block, still allowing for the unconditional operation of all pixels. The admissible threshold voltage spread has to be determined individually for the DEPFET and the clear transistor.

Limitations for the DEPFET gate

For a nonirradiated DSSC detector, the common gate voltage for an area of 64 x 64 pixels is tuned to a mean transistor current of 100 μA. For previous DEPFET productions the drain current dispersion was about 10% [50] due to inevitable technological fluctuations. After some operating time at the XFEL there will be some pixels exposed to a high radiation dose while other pixels will not be irradiated at all. Positive charge in the gate insulator reduces drain current with increasing radiation levels and, for a certain dose, some pixels are even completely switched off if the gate voltage is kept constant. In order to avoid insensitive detector areas, a more negative gate voltage has to be applied. At this point it has to be taken into account that a reduction in drain current also worsens the signal-to-noise ratio and hence detection capability for single photons. The minimum reasonable drain current is therefore given by the primary photon energy of the XFEL, and whether single-photon detection is required or not. For further considerations, a minimum drain current of 50 μA is assumed. The adjusted gate voltage is connected to big sensor areas also comprising nonirradiated pixels, which will consequently conduct much more current than initially foreseen. It has to be ensured here that the readout electronics are able to sink the higher drain current. In the latest version, the readout ASIC can deal with a maximum baseline drain current of 300 μA.
For the DSSC-DEPFET gate, the acceptable radiation level is therefore limited by the fact that the baseline drain current of all pixels within a sensor block of 64 x 64 pixels has to be in the range of 50 μA to 300 μA.

Limitations for the clear transistor

The genuine function of the clear gate is to form a potential barrier for electrons between the clear and the internal gate, which suppresses charge transfer between the two regions. Due to X-ray irradiation of the sensor and the related positive charging of the oxide, the region under the clear gate becomes more attractive for electrons. This weakens the potential barrier and facilitates the loss of signal charge from the internal gate into the clear contact as well as the back emission of electrons in the opposite direction, depending on the applied bias. In order to remedy both effects, the clear gate voltage has to be decreased. For nonirradiated pixels, it will come to an inversion condition below the clear gate as soon as the required gate voltage is too negative. In this case the clear gate transistor forms a parasitic current path from the drain toward the source. The additional current is not steered by signal charge in the internal gate and thus does not have a benefit - it only charges the input range of the electronics. Moreover, there is no potential barrier for the holes under the clear gate toward the back contact and consequently the inversion also results in a hole current to the backside. Both additional hole current paths increase the power dissipation in the sensor and have to be prevented. Given the discussed boundary conditions, inline measurements on the final sensors have shown that the expected width of the operation window for the clear gate voltage is in the order of 5 V.

5.1.2. Results of irradiation test using standard technology

A precursor experiment already investigated the suitability of standard DEPFET technology in extremely intense photon beams like the ones expected at the European XFEL. For this

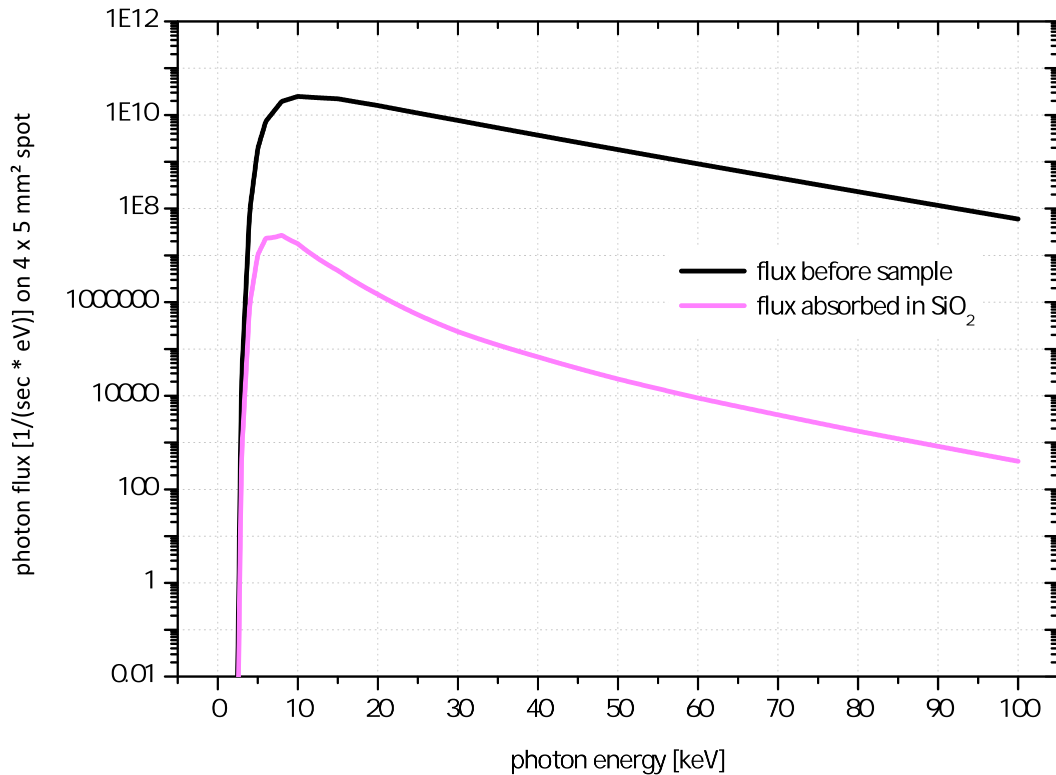

Figure 5.4: *The black curve depicts the measured primary DORIS F3 photon flux for a beam spot size of 5 x 4* mm^2 *as a function of the energy for a synchrotron current of 100 mA. The blue curve illustrates the calculated flux absorbed in the oxide of the test samples for front side illumination, assuming a homogeneous oxide layer in the beam spot.*

purpose DEPFET test samples with thick gate insulators representing standard DEPFET technology were processed and irradiated at the F3 beamline of the DORIS synchrotron. The spectrum at the F3 beamline shown in Figure 5.4 is white with a peak energy of 10 keV and an FWHM of 16 keV.
The photon flux is proportional to the synchrotron current, which typically varies between 90 mA and 140 mA. At a synchrotron current of 100 mA the integrated photon flux hitting an area of 5 x 4 mm^2 is $5 \cdot 10^{14}$ ph/sec. Due to the given gate insulator thickness and the front side illumination of the samples, total flux absorbed in the gate insulator of an identical area was $2 \cdot 10^{11}$ ph/sec, corresponding to a dose rate of 38 kGy/sec or 3.8 Mrad/sec. In the following, all given dose values refer to the energy deposition inside the gate oxide layer.
It was foreseen to irradiate in dose steps of three per decade with small initial values (100 krad, 200 krad, 500 krad, 1 Mrad, 2 Mrad, ...). A chopper wheel was thus going to be inserted into the beam to reduce the dose rate to more convenient values. However, due to

the failure of the chopper wheel motor, the samples were irradiated at a high dose rate with larger initial values (several Mrad) of up to several 100 Mrad to few Grad in the final phases.

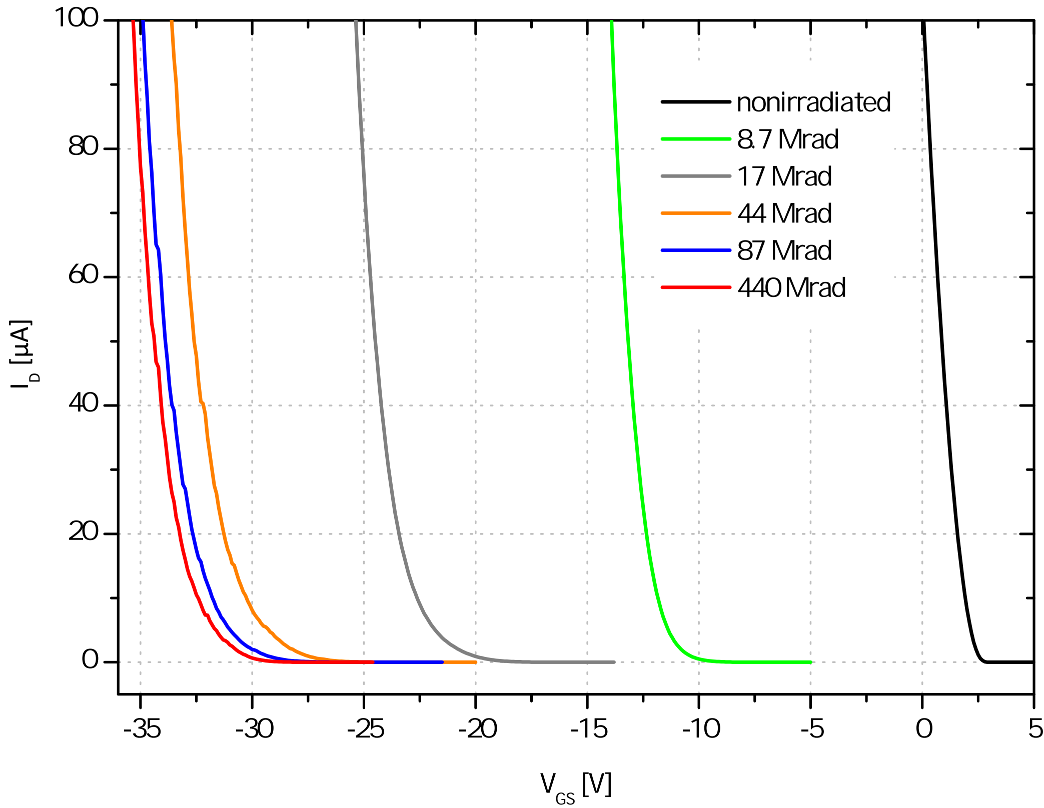

Figure 5.5: *Measured transfer characteristics of a depletion-type PMOS transistor fabricated using standard DEPFET technology with a gate length of 5 µm and a gate width of 50 µm for different irradiation levels. For a radiation dose of 440 Mrad the threshold voltage shift exceeds 30 V [88].*

For dosimetry, the photocurrent of a calibrated diode was measured and translated into a dose rate value. The dose rate value was put into relation with the synchrotron current and the proportionality of dose rate and synchrotron current was assumed.
The samples were mounted on ceramic carriers and thermally connected to a heat sink at a positive temperature above the dew point as the whole setup was in air. The sample temperature during irradiation could not be controlled nor monitored. Sample characteristics were measured using an I-V setup close to the beamline and the typical time for interim sample characterization between two irradiation cycles was 10 to 20 min.
Figure 5.5 shows the transfer characteristics of one of the irradiated p channel field effect transistors (FETs) with a gate length of 5 µm and a gate width of 50 µm. The FET features a channel implantation and is representative of the DEPFET transistor. Like all other samples, the transistor survived and still has measurable and analyzable characteristics. However, the measurements show a threshold voltage shift exceeding 30 V for a dose of

440 Mrad and the measured threshold voltage shift does not scale linearly with the total dose. Instead, it increases steeply to roughly 50 Mrad and for higher doses some kind of saturation behavior appears.
Due to the broken chopper wheel motor the dose before the first measurement (8.7 Mrad) caused a threshold voltage shift that cannot be compensated by the DSSC readout electronics. Therefore, the acceptable radiation dose for the given DSSC boundary conditions cannot be determined from these irradiation tests. To improve and precisely specify the radiation hardness of the DSSC detector, the irradiation tests were repeated with new test devices fabricated using a dedicated technology.

5.1.3. Results of irradiation test with thinned gate insulators

An another batch of DEPFET representative test structures was produced in order to improve DSSC radiation hardness. The gate oxide was thinned down with respect to the standard DEPFET technology in order to minimize absorption probability for X-ray photons and thus reduce the resulting hole density in the gate insulator. Additionally, the channel implantation (PSHN) was optimized by technology and device simulations to obtain zero-field conditions in the oxide at the foreseen DSSC drain current of 100 μA. Both measures are known from literature and have been discussed above (compare Figure 5.3 and 5.2).
The test samples fabricated with thinned gate insulators have been irradiated at the F4 beamline of the DORIS synchrotron. According to the first irradiation campaign, the intense white beam of the DORIS ring (Figure 5.4) was used, but in order to reduce the high photon flux, aluminum absorbers of different thicknesses were placed in front of the samples. This method dampened the dose rate from 14 Mrad/s down to 1 krad/s, which also allowed for irradiation steps below 1 Mrad.
Dosimetry was done by a thermo-luminescence dosimeter as well as by measuring the photocurrent of a diode during irradiation. The results of both redundant methods were consistent.
For irradiation under realistic conditions the samples were mounted inside a vacuum box so that the DUT could be cooled down to the foreseen DSSC operating temperature of -20°C. Active cooling regulation kept the temperature constant even during very intense irradiations. Using vacuum feed-throughs, the device was connected to the outside in order to bias the devices during irradiation and perform in-situ measurements on the mounted structure.
The irradiations were again focused on PMOS transistors with and without channel implantation to represent the gate and the clear gate of the DEPFET. Each transistor type is available in eight different technology versions covering various gate insulators. All variants were irradiated in steps up to a dose of 100 Mrad and the device characteristics have been measured several times per decade of the absorbed dose value.
Below we show the measured transfer characteristics of the two representative transistor

types for various radiation levels and the maximum tolerable radiation dose will be derived individually for the gate and the clear gate. Both transistors are not fabricated in the most radiation hard technology, but in the same technology that was selected for the production of the final DSSC sensor. This technology represents the best compromise of radiation hardness and the resulting technological risks associated with thinning the gate insulator. The lower risks ensure an indispensable high yield for the large-area DSSC devices.

Results for the DEPFET transistor

Figure 5.6 shows the transfer characteristics of a depletion-mode transistor representing the DEPFET gate with a gate length of 5 μm and a gate width of 50 μm.

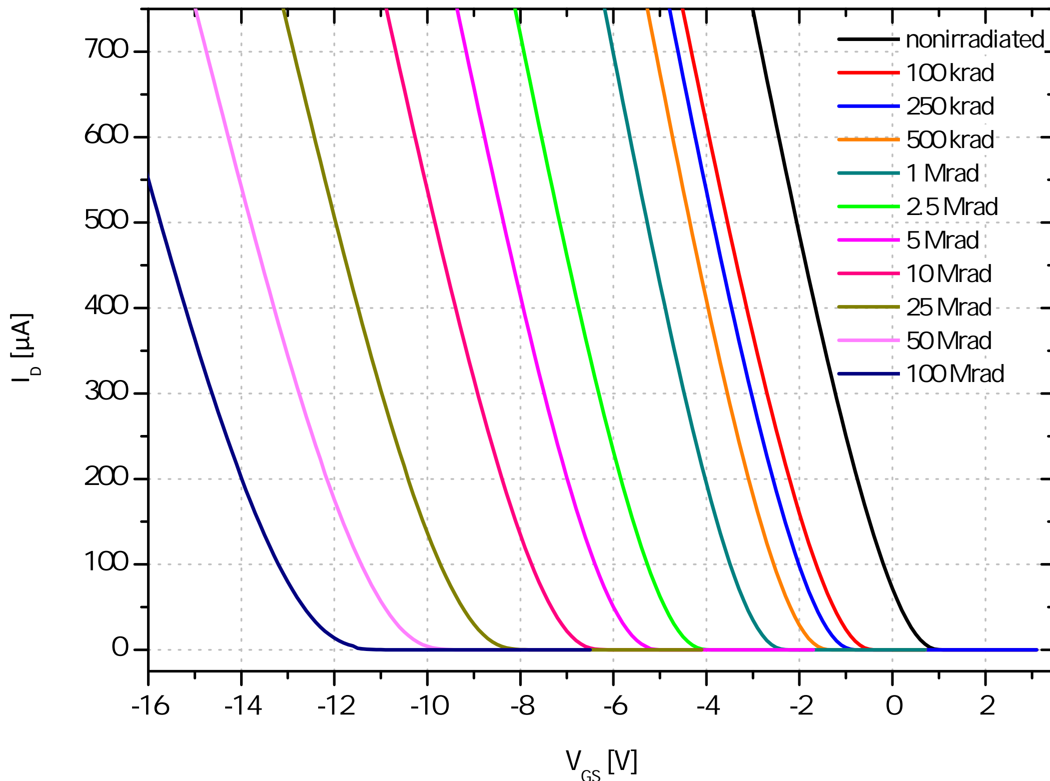

Figure 5.6: *Measured transfer characteristics of a depletion-type PMOS transistor fabricated in DSSC-DEPFET technology with a gate length of 5* μm *and a gate width of 50* μm *for different irradiation levels.*

During irradiation the gate voltage was kept constant at 0 V. In this case the expected drain current of the nonirradiated DSSC-DEPFET in the DSSC gate geometry is roughly 100 μA. Since the gate voltage for the DSSC detector decreases with the accumulated radiation dose, the applied gate voltage of 0 V is in any case more positive than in the XFEL's application, which makes the irradiation tests a sort of worst-case measurement.

The measured gate voltage shift for a resulting drain current of 100 μA was less than 15 V for an irradiation dose of 100 Mrad. Previous irradiations of identical test structures using standard DEPFET technology with a thick gate oxide showed threshold-voltage shifts beyond 30 V at comparable dose values. The irradiations of the new test devices were performed under biasing and at a device temperature of -20°C. Although these realistic conditions are more adverse, the thinner gate insulator led to an improvement of more than 50%.

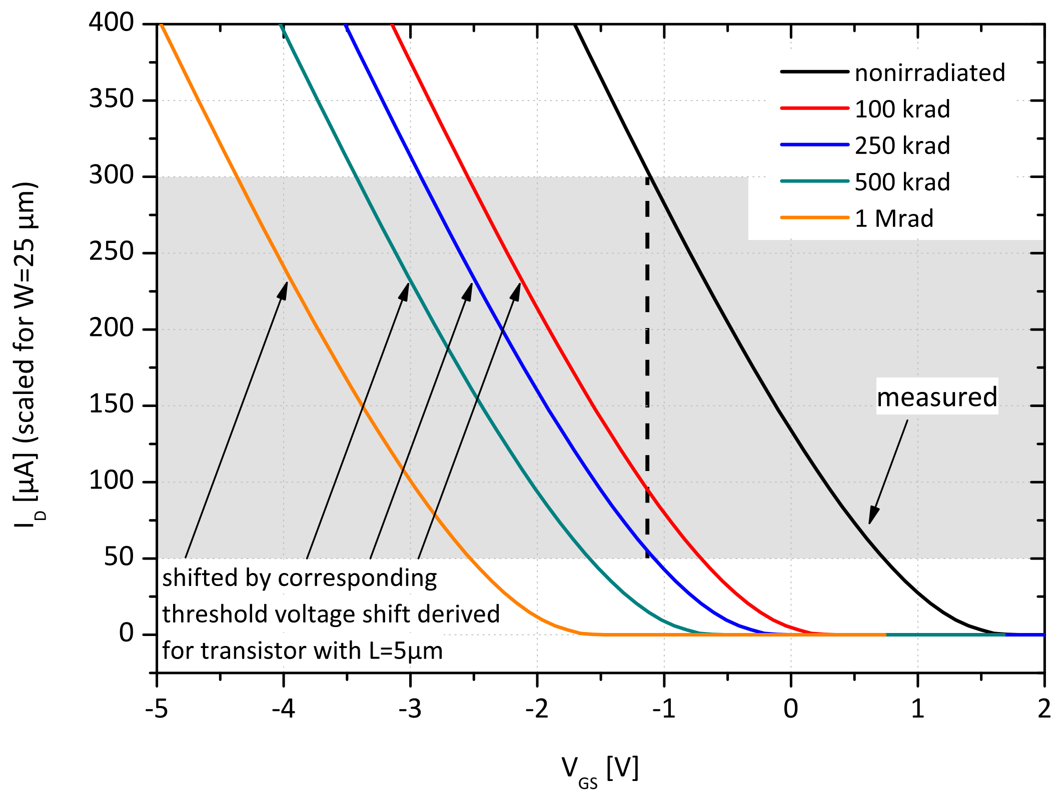

Figure 5.7: *Transfer characteristics measured for a nonirradiated depletion-type PMOS transistor fabricated using DSSC-DEPFET technology with a gate length of 3.5* μm *(black). The drain current shown is scaled down to a gate width of 25* μm*. The characteristics for increasing irradiation levels are generated by shifting the black curve by the corresponding threshold voltage shift measured for a transistor with a gate length of 5* μm*. The gray area indicates the acceptable input range of the readout electronics.*

Determining an acceptable radiation dose for the gate in the DSSC application requires consideration of the gate dimensions. The DEPFET gate selected for the DSSC detector has a gate length of 3.5 μm and a gate width of 25 μm. Assuming a homogeneous current density in the channel, the drain current measured can easily be scaled with the channel width. By contrast, gate length has an impact on the shape of the transfer characteristics as it changes the g_m of the transistor. Although transistors with gate lengths of 3.5, 4, 5,

7.5 and 10 μm have been irradiated together on the same sample, the dosimetry used only applies to the transistor with the 5 μm gate length because it is located in the center of the chip and beam intensity drops toward the outside. The only way to derive the maximum acceptable radiation dose for the DEPFET gate is to determine threshold voltage shift from the curves depicted in Figure 5.6 and then transfer that to the transistor with a gate length of 3.5 μm. This procedure is feasible in a first order approximation since the threshold voltage shift due to ionizing radiation is independent of the gate length. However, degradation of the interface is neglected, which would lead to a lowering of the g_m due to the reduction of hole mobility in the channel.
The black curve in Figure 5.7 depicts the transfer characteristics measured for a nonirradiated depletion-type PMOS transistor fabricated using DSSC-DEPFET technology with a gate length of 3.5 μm. The drain current indicated has been divided by a factor of two in order to scale the gate width of the transistor from 50 μm down to 25 μm. The characteristics for increasing irradiation levels are generated by shifting the black curve by the corresponding threshold voltage shift measured for a transistor with a gate length of 5 μm.
The region highlighted in gray indicates the allowed drain current for the DEPFETs in the DSSC detector ranging from 50 to 300 μA. The measurement shows that the maximum tolerable radiation level is around 250 krad. In this case the gate voltage has to be decreased by 1.9 V to keep the drain current for irradiated pixels above 50 μA while nonirradiated pixels will still conduct less than 300 μA. By extending the input range of the readout electronics to higher drain currents, the gray area and thus the acceptable radiation dose for the DEPFET transistor can be further increased.

Results for the clear transistor

The irradiations of clear transistors were also performed under a constant gate bias of 0 V. The transfer characteristics measured for an enhancement-mode transistor representing the clear FET are depicted in Figure 5.8 for different radiation levels. The transistor features a gate length of 5 μm and a gate width of 50 μm. A threshold voltage shift of 13 V can be measured for the final dose of 100 Mrad, which is 2 V less than observed for the depletion-type transistor. This is due to technological boundary conditions allowing for a thinner insulator below the clear gate than underneath the gate, which results in increased radiation hardness even if the enhancement transistor is not designed for zero-field conditions in the oxide. As already mentioned, the width of the operating window for the clear gate is expected to be 5 V for the final DSSC sensors and a comparable threshold voltage shift for the clear transistor can be observed for an integrated radiation dose of 500 krad. Therefore, the acceptable radiation dose of the DSSC-DEPFET is limited by the gate and can be set at 250 krad.

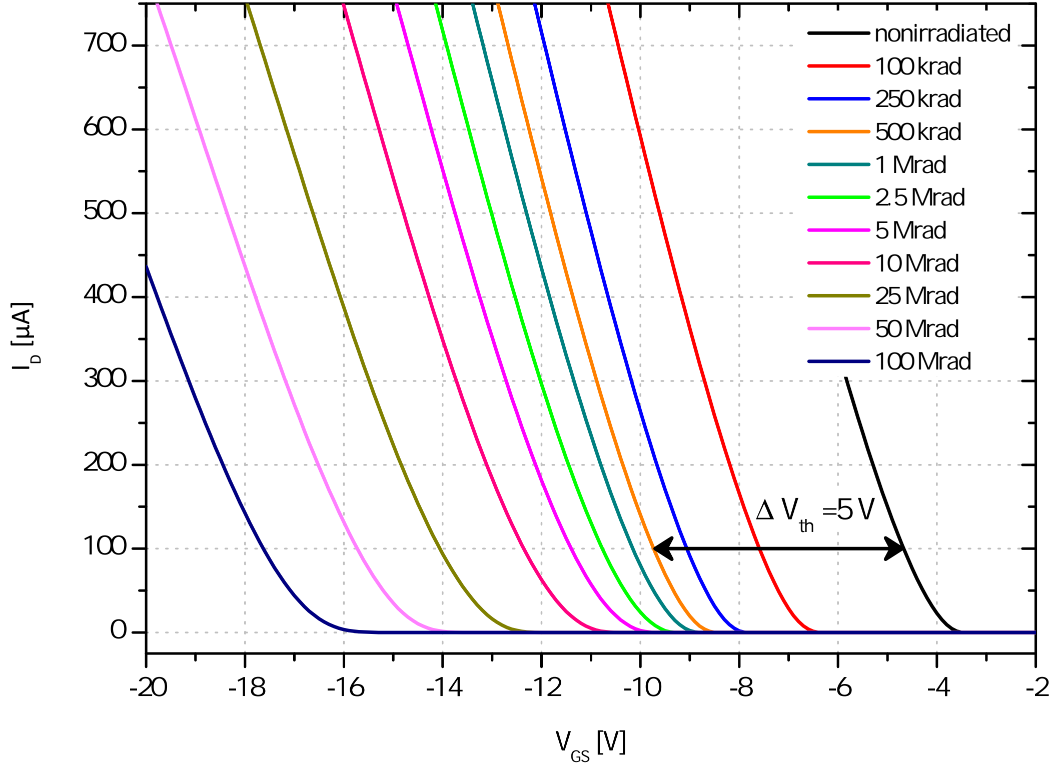

Figure 5.8: *Measured transfer characteristics of a enhancement-type PMOS transistor fabricated in DSSC-DEPFET technology with a gate length of 5 μm and a gate width of 50 μm for different irradiation levels. The tolerable threshold voltage shift of 5 V is reached at a radiation dose of 500 krad.*

5.1.4. Conclusion

Limits for the DEPFET operation have been derived from the characteristics measured, assuming the worst-case scenario, that in a real experiment the sensor will be irradiated unevenly, i.e., some pixels get most of the intensity while others remain nonirradiated. For the clear gate, a limitation arose from its operating window, which is assumed to have a width of 5 V. For the DEPFET gate the limitation is taken from the dynamic range of the readout ASIC, which is assumed to allow a minimum/maximum current of 50 μA and 300 μA, respectively. As shown in the previous section, the boundary conditions for the gate restrict the tolerable radiation dose for the DSSC-DEPFET to 250 krad.

Figure 5.9 shows the transfer from the absorbed dose to the acceptable number of photons per pixel as a function of photon energy. For low photon energies, radiation hardness is not an issue since the photons enter the detector through the radiation entrance window on the backside and the self-shielding effect of the silicon bulk limits the dose absorbed by the gate oxide on the front side. For photon energies above 6 keV, the silicon bulk becomes more and more transparent allowing the photons to reach the active front side. For this reason, the tolerable number of photons hitting a single pixel decreases sharply before it reaches a local minimum at about 17 keV. For even higher energies, the absorption probability

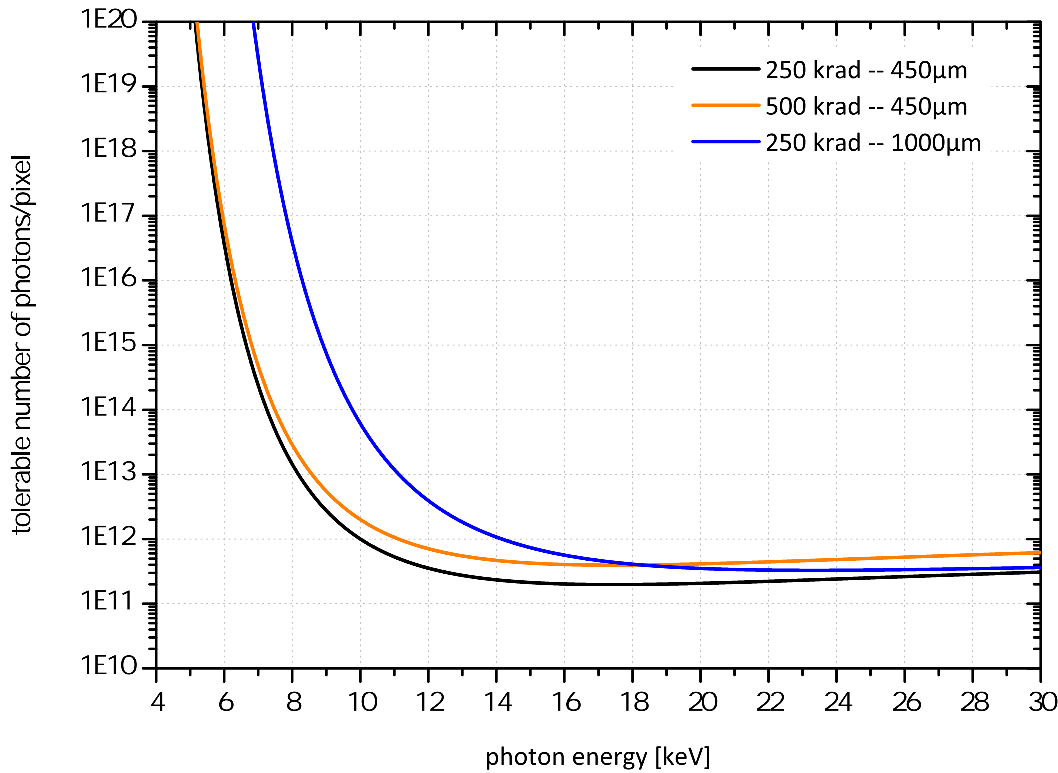

Figure 5.9: *Acceptable number of X-ray photons per pixel as a function of the energy. Due to backside illumination of the DEPFET sensor and the self-shielding effect of the 450 μm thick silicon bulk the DSSC detector is almost insensitive to X-rays up to 6 keV. For higher photon energies, the silicon bulk becomes transparent and radiation tolerance decreases sharply. For energies above roughly 17 keV, the progressive reduction of photon absorption probability in the gate oxide leads again to a slight enlargement of the acceptable photon number.*

of photons in the gate insulator is further reduced and the tolerable number of photons increases again slightly.

In order to guarantee the unrestricted applicability of the DSSC detector, the energy range has to be limited to less than 6 keV. In this scenario, the permitted radiation dose will never be reached in three years of operation, even for the enormous photon flux of the European XFEL. Nevertheless, the DSSC can also be used for the higher energies if the experimental conditions ensure that the tolerable number of photons per pixel is not exceeded.

As indicated in Figure 5.9, it is also conceivable that an extension of the energy range can be achieved, for example by increasing bulk thickness. Using a 1-mm-thick silicon substrate, the energy range could be expanded up to roughly 8 keV. However, this would require a complete redesign of the sensor since the dimensions of the edge structures - especially the guard rings - have to be increased. Another option would be to pre-irradiate of the full DSSC detector to several hundred krad. As already mentioned, the threshold voltage of the transistors does not shift linearly with the radiation dose. The fastest shift for low doses could be generated by homogeneous pre-irradiation. Up to now, this option

has not been evaluated in detail because it is technically very challenging to achieve the required homogeneity over the full DSSC detector area of 500 cm^2, and the associated risks are too high.

In addition, annealing concepts proposed in literature have not yet been investigated, since they are technically not feasible given the present thermal design. Furthermore, mechanical stress due to thermal cycles can lead to damages in the complex interconnection systems between the sensor, the readout ASICs and the mainboards. These issues have to be investigated in detail as soon as the first ladder prototype is available because the recovery of the positive oxide charge could provide significant potential for radiation hardening.

Apart from the DEPFET, DSSC detector radiation tolerances can also be improved by enlarging of the dynamic range of the readout ASICs. In the best case, only the operating window of the clear gate would dictate limits and, in the present configuration, the acceptable dose could be enhanced up to 500 krad (compare Figure 5.9).

5.2. Readout speed

The European XFEL will provide ultra-short X-ray flashes with a maximum repetition rate of 4.5 MHz. The full readout cycle has to be implemented within the corresponding 220 ns between two flashes. Figure 5.10 illustrates the time scheme foreseen for the 4.5 MHz operation of the DSSC detector.

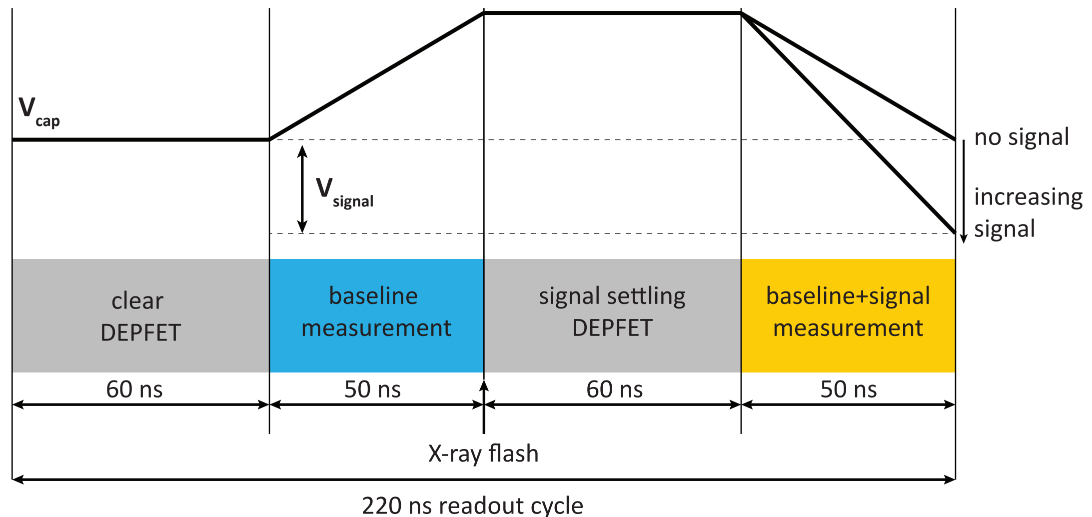

Figure 5.10: *Time scheme of a DSSC readout cycle for a 4.5-MHz operation. The internal gate is cleared and the baseline drain current is integrated on a capacitor in the analog filter of the readout chip before the X-ray flash hits the detector. In the first 60 ns after the flash, signal electrons have to settle before the drain current discharges the capacitor. The charging voltage V_{signal} of the capacitor after the readout contains information about the energy deposition in the pixel.*

Initially, 60 ns are allocated for a complete reset of the internal gate and due to the nonlinear gain curve it is essential that no electrons remain in the internal gate, since this would result in reduced charge handling capacity in the central part of the internal gate and a shift in the onset energy for signal compression toward smaller energy depositions. Baseline drain current is measured after the clear pulse. To do this, the drain current flows into the readout ASIC where the current path is split, and most of the drain current is compensated by a constant current source. Only a small fraction is fed into the analog filter and integrated on a capacitor for 50 ns. After integration, the X-ray flash hits the detector and the electrons generated in the DEPFET sensor immediately start to migrate toward the internal gate. Again, a time interval of 60 ns is allocated for electrons to settle in the sensor before the drain current is measured again. The actual drain current that is not compensated by the constant current source is therefore used to discharge the capacitor in the analog filter according to the baseline measurement for 50 ns. The resulting charging voltage of the capacitor V_{signal} contains data about the signal-induced drain current increase and, for a known response curve, data about energy deposition in the pixel after the last clear pulse.
For small photon energies, the readout chip gain, respectively the resulting charging voltage of the capacitor, has to be enhanced either by reducing the capacitance of the integrating capacitor or by extending the integration phases. By minimizing of the clear and the charge settling time of the DEPFET, the available time span for the readout can be extended, and the possible gain range can be increased. In order to facilitate all gain settings required for obtaining both single-photon detection and high dynamic range for photon energies above 500 eV, the charge collection time in the DEPFET has to be less than 60 ns. A detailed discussion of the expected DSSC detector performance for different readout speeds and photon energies between 500 eV and 12 keV can be found in [15].

contact	applied voltage [V]
source	0
drain	-3
gate	-2
inner drift ring	-12.5
outer drift ring	-25
backside	-120

Table 5.1: *Summary of the voltages applied to the DEPFET pixel during the transient simulation of charge collection speed.*

Transient 2D device simulations have been performed in order to optimize sensor design for maximum operating speed. These simulations included the same radial slice through a single pixel, which was already used to simulate the nonlinear response curve. The simulation area starts at the drain in the pixel center and ranges 120 μm to the outer

drift ring at the pixel boundary. It covers the full bulk thickness of 450 μm, considers the foreseen DSSC device temperature of -20°C and assumes cylindrical symmetry. The voltages applied during the simulation are summarized in table 5.1.

When the transistor is switched off, the internal gate potential can be steered by the gate voltage because of capacitive coupling. For a more positive gate voltage, the floating internal gate becomes more attractive for electrons and the charge collection can potentially be sped up. In the DSSC application, the DEPFET transistor is switched on whenever X-rays hit the detector. Thus, the internal gate becomes more negative since it is capacitively coupled to the negative potential in the transistor channel. Consequently, the source, drain and gate voltages in the simulation have been tuned to keep the DEPFET transistor in the on-state. This leads to realistic potential distribution and excludes the possible reduction of charge collection time as a result of internal gate potentials being too positive. Drift voltages have been set to the maximums that can be applied - before in the given prototype technology - the punch-through between source/ring1 and ring1/ring2 sets in. Figure 5.11 (a) shows the simulated potential distribution in the entire device for a backside voltage of -120 V.

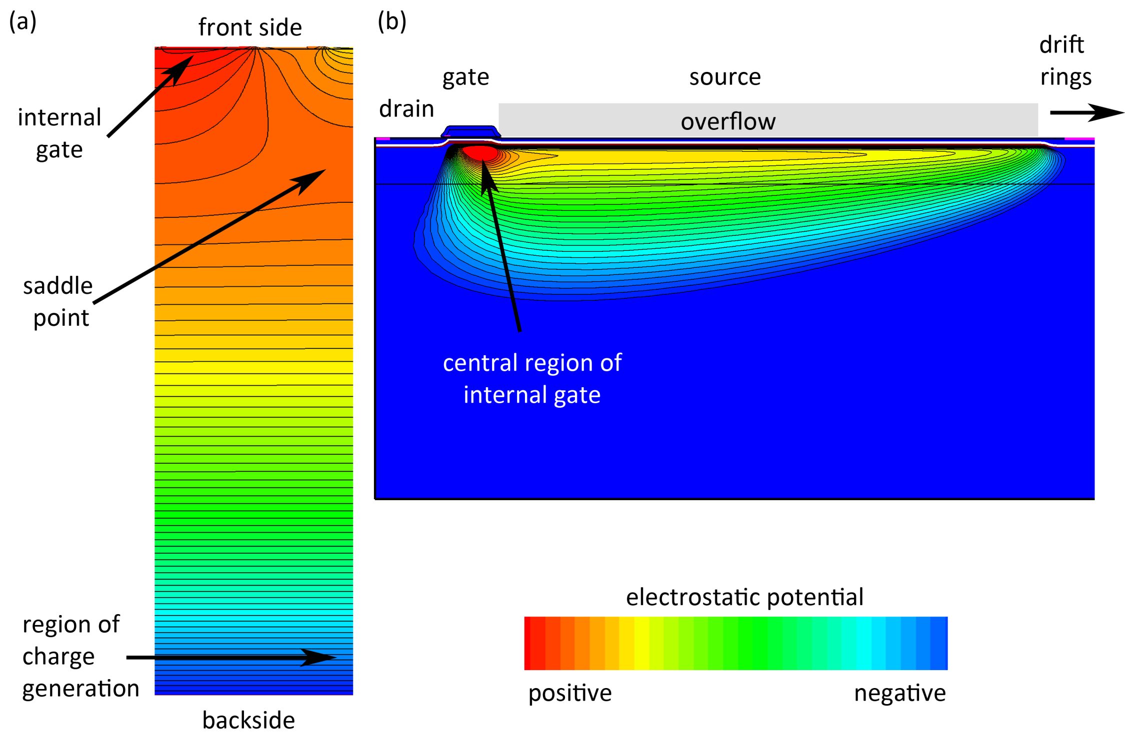

Figure 5.11: *Simulated potential distribution on a radial slice through a DEPFET in the SG variant fabricated using standard technology. The slice comprises the drain, the gate, the source and the two drift rings as well as the field plates in between. The full simulation region covering the full wafer thickness of 450 μm is depicted in (a) and a detailed view of the internal gate region close to the active front side is shown in (b).*

The maximum charge collection time prevails for photons absorbed at both the outer rim of the pixel and close to the radiation entrance window. In this case, the radiation-induced electrons have to overcome the highest possible distance toward the internal gate. For the simulation, a homogeneous electron density is generated within 1 ns in a box ranging from 110 to 115 μm with respect to the pixel center and located at a depth between 440 to 445 μm. Due to the cylindrical symmetry, this is equivalent to a torus-shaped charge cloud in the device comprising 1,615 electrons. That corresponds to the charge generated by absorbing an Mn-K_α photon.

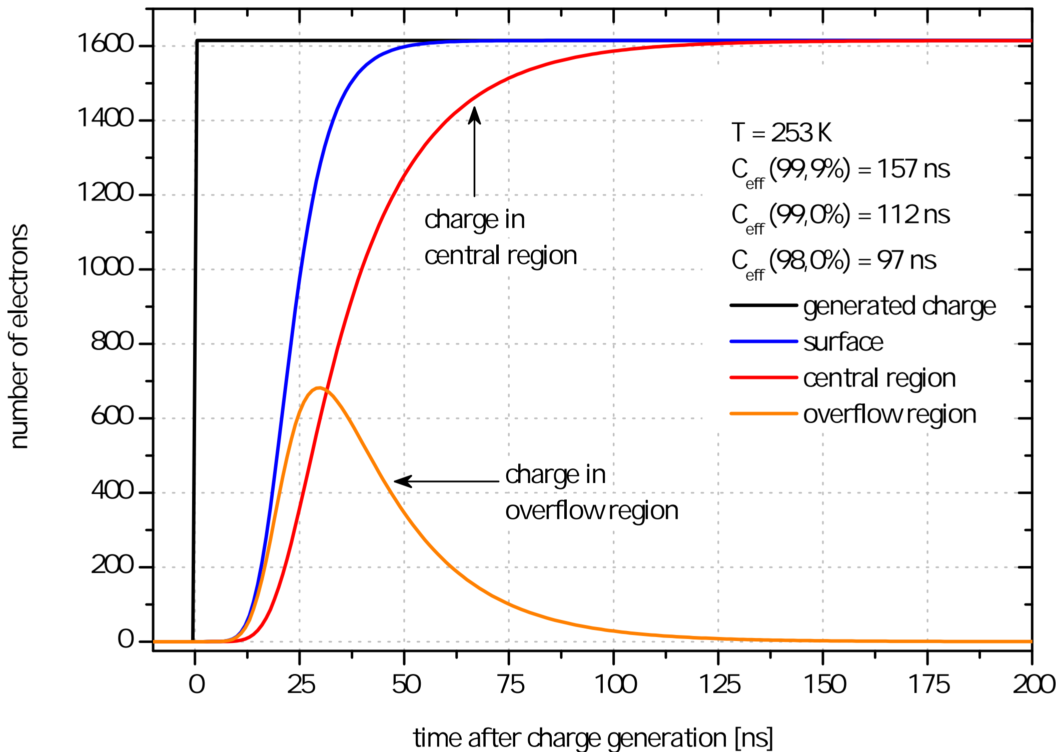

Figure 5.12: *Simulated temporal evolution of a charge cloud comprising 1,615 electrons as a function of the time after its generation. The simulation covers the full wafer thickness of 450 μm and the nonlinear DEPFET corresponds to the SG variant fabricated using standard technology. After 48 ns, 99% of the generated electrons have entered the surface region but due to the diffusion-based charge redistribution in the overflow region it takes 157 ns before 99.9% have finally reached the central region of the internal gate.*

After being generated, the electrons move perpendicular to the equipotential lines. Hence, due to interference from depletion in the drift ring region and the backside they will initially drift toward the saddle point at the outer pixel rim at a depth of roughly 80 μm. The electrons are then directed toward the source by negative drift ring potentials, where they enter the overflow region of the internal gate. As indicated in Figure 5.11 (b), electrostatic potential in the overflow region of the internal gate is almost constant. Further electron transport toward the central region is therefore mainly based on diffusion, which signifi-

cantly reduces the electron velocity. Two specific integration windows have been defined in order to visualize the temporal evolution of charge transfer in the device. One comprises the central part and the other the overflow region of the internal gate.
Figure 5.12 illustrates the amount of charge located in each window as a function of the time after generation. Due to the presence of an electric field in the bulk it takes only 48 ns until 99% of the generated electrons have reached the internal gate region. However, the subsequent diffusion-based transport from the overflow region into the central part of the internal gate is very slow and thus dominates the overall charge collection time. With increasing number of electrons collected in the central region, the prevailing concentration gradient in the overflow is decreased and the diffusion process is in turn slowed down. Consequently, it lasts 97 ns before 98% of the generated electrons enter the central part, but 157 ns to achieve 99.9%. This simulation clearly shows that the constant electrostatic potential in the overflow region under the source represents a limiting factor for charge collection time.
In order to eliminate this bottleneck, two additional deep n implantations have been introduced for final sensor production, as illustrated in Figure 5.13 (a). These n implantations are primarily used to tailor of the nonlinear characteristics of the DEPFET, as will be discussed in detail in section 5.3. Both implantations range from the drain in the center of the pixel to the overflow region under the source. Their staggered expansion into the source region results in a segmentation of the overflow region. Figure 5.13 (b) shows the resulting electrostatic potential in the case of a fully depleted device. For smaller radii, the higher n-doping concentration enhances the current positive space charge, making the central part of the internal gate more attractive for electrons. At the implantation boundaries, the concentration gradient induces a lateral drift field that is directed toward the internal gate and supports the charge transfer within the overflow region.
In order to identify the potential acceleration of charge collection due to the additional implantations, the transient device simulation was repeated for the structure depicted in Figure 5.13. The charge is considered individually for each of the three overflow segments. For comparability reasons the supply voltages have been kept unchanged, the only exception being the gate voltage adapted to keep the transistor in the on-state. Therefore, the potential distribution in the silicon bulk is not modified and the simulation only shows the improvement from segmenting of the overflow region. Figure 5.14 depicts the evolution of the charge cloud obtained as a function of the time after its generation. Once again, due to the unchanged electric field conditions in the bulk, the charge transfer of 99% of the electrons into the surface region takes roughly 48 ns. However, the lateral drift field introduced accelerates the redistribution of charge within the overflow region considerably. Consequently, charge collection efficiency of 99.9% is already achieved after 66 ns and the simulations indicate that the staggered overflow region reduces the collection time by roughly a factor 2.4.

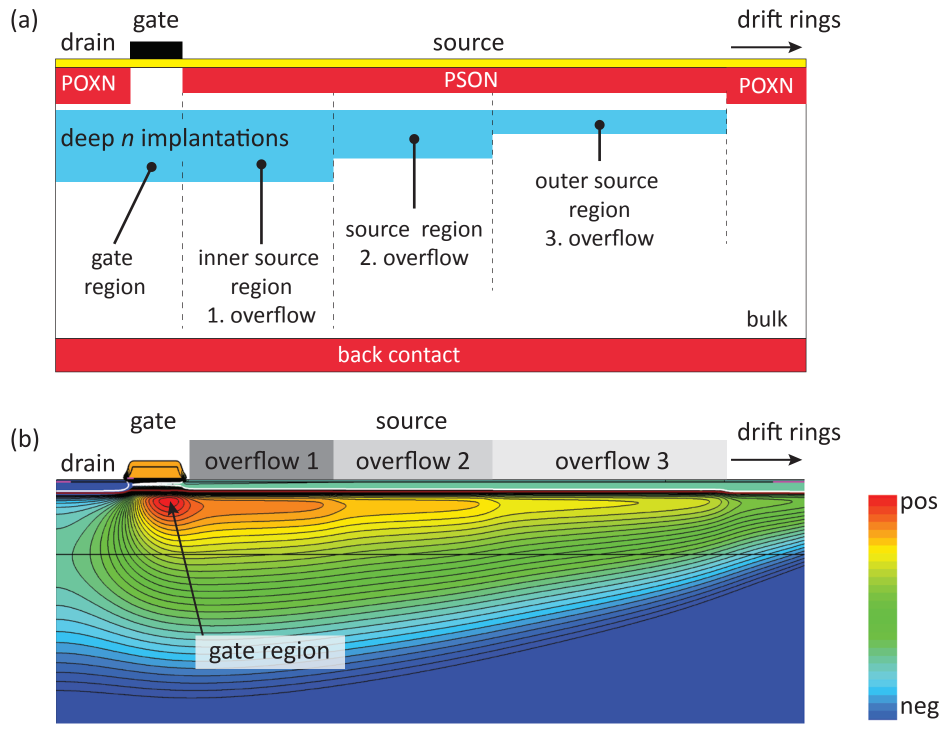

Figure 5.13: *(a) Schematic cross section of the nonlinear DEPFET optimized for high readout speeds. Two additional deep n implantations split the overflow region into three parts. (b) Simulated potential distribution in the top part of the device. Potential steps are formed at the boundaries of the additional implantations and the previous diffusion-based charge transport toward the gate region is accelerated by the induced lateral electric field.*

Furthermore, Figure 5.14 shows that under these bias conditions most electrons enter the internal gate in the second overflow region. Although the introduced lateral drift field speeds up charge transfer through the first overflow into the gate region it still takes almost one-third of the overall collection time. For optimum bias conditions, the negative potentials of the backside and drift rings will guide the electrons directly underneath the transistor channel. As the given ring voltages cannot become more negative without punch-through between the source and the drift rings, the only solution is to apply a more positive backside voltage. By doing so, the impact of the negative ring potentials can be extended into the silicon bulk, leading to an earlier and stronger redirection of the electrons towards the pixels center. On the one hand, this reduces charge collection time as the electrons enter the internal gate closer to the center. On the other hand, more positive backside voltage decreases the current electric field strength in the bulk and thus reduces electron drift velocity in the bulk. The two effects are in competition and the only way out is to apply more negative ring voltages. Hence, a new drift ring design was developed and implemented in the final DSSC sensors. Simulations show that a maximum voltage difference of 35 V between source/ring1 and ring1/ring2 can be applied before punch-through occurs. The new design broadens the operating window of the drift

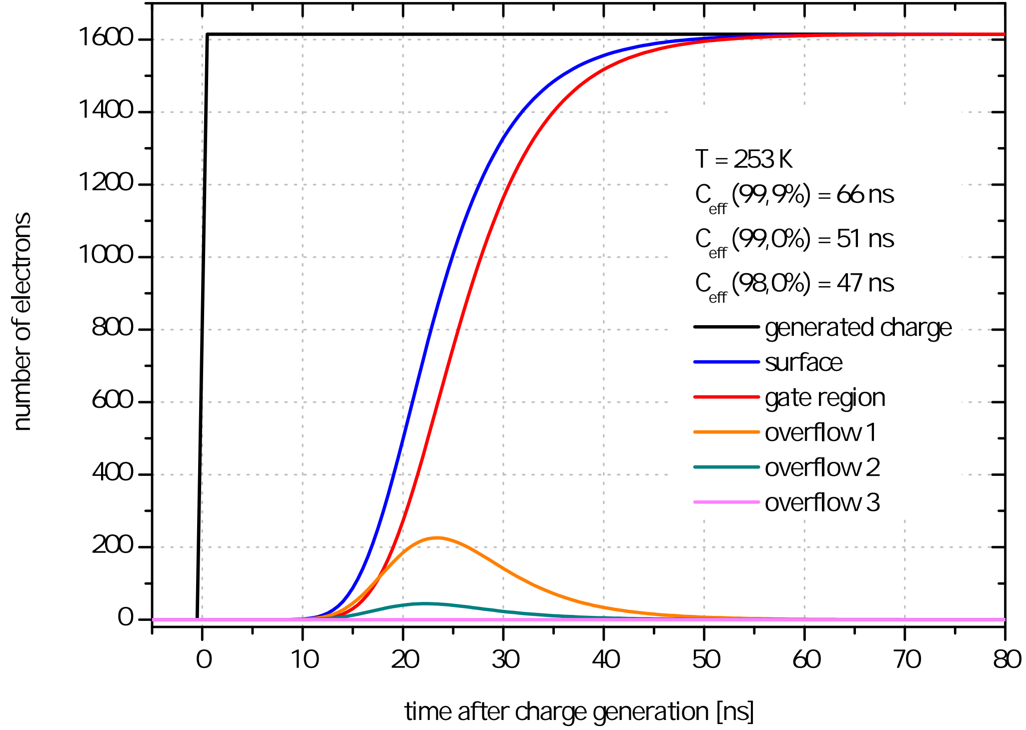

Figure 5.14: *Temporal evolution of a charge cloud as a function of the time after its generation, simulated for the DEPFET structure shown in Figure 5.13. The simulation again covers the full wafer thickness of 450 μm and the same voltages as with the previous simulation using the standard technology. Accordingly, it takes 48 ns before 99% have entered the surface region but the new lateral drift field introduced to the overflow region allows for charge collection efficiency of 99.9% after just 66 ns. The charge collection time has been sped up by a factor of 2.4.*

structures and facilitates a potential distribution that guides signal electrons close to the transistor channel even for the very negative backside voltages necessary for high drift fields.

Figure 5.15 shows the result of a transient simulation of charge collection for a homogeneous overflow region, for a staggered overflow region with comparable biasing, and for the final DSSC-DEPFET with drift ring voltages of -30 V and -60 V and a backside voltage of -180 V. For the DSSC-DEPFET, charge transfer to the active front side is accelerated and 99% of the electrons have reached the surface in just 24 ns. This is due to the higher drift field in the silicon bulk caused by the more negative backside voltage. Although the assumed ring voltages are very conservative and more electrons enter the internal gate in the overflow region, the charge collection time for 98% collection efficiency in the central region can again be reduced by 39% down to 29 ns compared to the lower drift voltages.

It has to be pointed out that this simulation represents the worst-case scenario, and generally the collection of signal charge generated closer to the pixel center will be much faster. The results indicate that for optimized biasing of the drift rings and the backside, a charge collection time of less than 30 ns can be achieved for 98% of the generated charge,

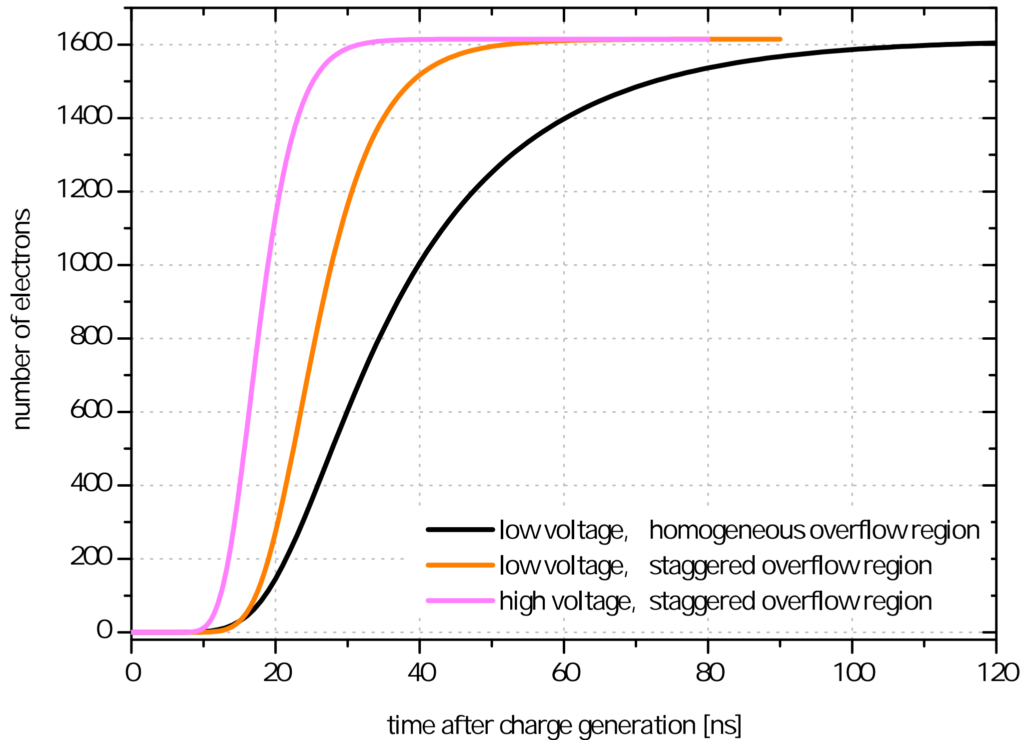

Figure 5.15: *Amount of signal charge in the central region of the internal gate as function of the time after charge generation. For prototypes, a charge collection efficiency of 98% is achieved in 97 ns. By segmenting of the overflow region, the redistribution of electrons within the internal gate is sped up, resulting in a charge collection efficiency of 98% after 47 ns. By using the advanced drift ring design and higher backside voltages the charge collection time is shorted to 29 ns.*

which is enough for photon counting applications.

However, the full DSSC sensor comprising 128 x 256 pixels will only provide global backside and global outer ring voltage. Voltage at the inner ring will only be adjustable in blocks of 64 x 64 pixels and even if the expected bulk doping fluctuations are lower than 10% they will preclude optimal biasing of all pixels at once. For pixels with lower bulk doping, the global backside voltage will be too negative and the electrons will enter the internal gate in the overflow region, instead of the central region. In pixels with higher bulk doping concentration, the current electric field strength in the top part of the device is reduced, which lowers the drift velocity of the signal electrons. However, sensitivity analyzes show that due to the newly introduced staggered overflow region backside voltage variations of 10% can be managed, and a charge collection time of less than 60 ns can be attained for all pixels on a single chip. Furthermore, they indicate that a change in overflow segmentation due to a variation of the radii of the additional n implantations does not considerably affect charge collection speeds as long as no large regions without lateral drift fields occur. This allows us to utilize the additional deep n implantations in the overflow region to tailor the DEPFET amplification properties, as discussed in the following section.

5.3. Design of final nonlinear response curve

One of the key features of the DSSC detector is nonlinear amplification in the DEPFET. The high gain for small energy depositions permits the detection of individual low-energy photons, and signal compression for large energies extends the dynamic range of the detector to several thousand photons per pixel and frame. Although nonlinear DEPFET amplification limits single-photon detection capabilities for high photon numbers, it still allows for better energy resolution than the natural fluctuations of photon distribution caused by Poisson noise ($\Delta N = \sqrt{N}$) in the FEL process.
The first DEPFET prototypes exhibiting nonlinear amplification were aimed at confirming the overall signal compression mechanism. They have therefore been fabricated using standard technology and only one additional implantation has been introduced for the source (PSON). This basic technology results in constant potential in the overflow region, and the realizable nonlinear response curve provides only two different gains. Although the onset energy of signal compression can be controlled by DEPFET geometry and the PSON implantation, as discussed in detail in chapter 4, this is insufficient for the requirements of the DSSC detector system. If the onset energy of signal compression is too low, the smaller signal-to-noise ratio will limit single-photon detection capability, and if it is too large the high gain will reduce the dynamic range of the detector system.
Within the framework of final sensor production, the advanced technology comprising two additional deep n implantations offers further opportunities for tailoring DEPFET amplification properties once compression has started. The new tuning options for the gain curve are discussed in the following section.

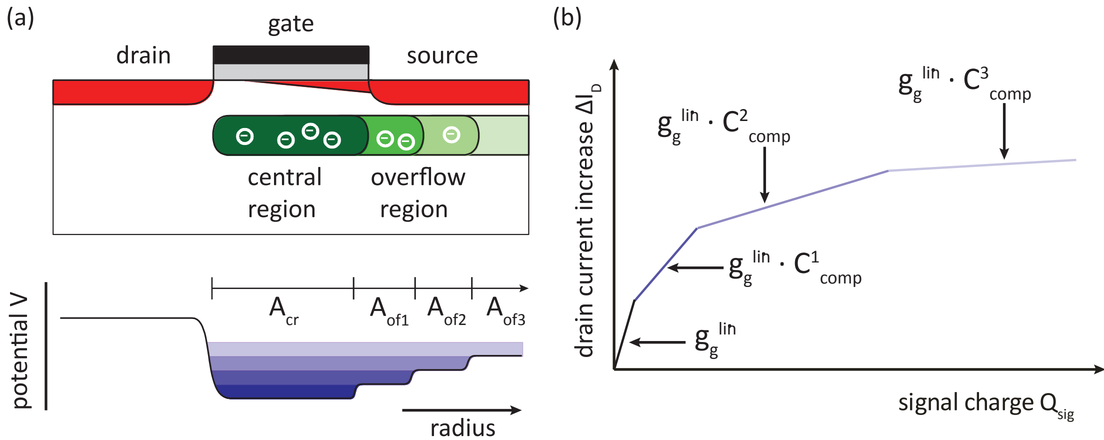

Figure 5.16: *(a) Schematic structure and electrostatic potential in the internal gate of a DSSC-DEPFET with two additional deep n implantations. The areas of the central region and the individual overflow regions are indicated by A_{cr} and A^i_{of}. (b) Nonlinear response curve for a DSSC-DEPFET featuring three overflow regions.*

Figure 5.16 is a schematic of implantation placements and electrostatic potential on a radial cut through a DSSC-DEPFET (a) as well as of the resulting nonlinear response

curve (b). In contrast to the prototype fabrication, the overflow region is staggered by two deep n implantations causing a graduation of electrostatic potential. This does not affect the amplification of the DEPFET as long as all signal electrons fit into the central region. However, in the case of initial electron spillover under the source, the charge spreads only into the first overflow region until the signal charge in turn compensates the next potential step toward the subsequent one. This way the equipotential area where signal electrons accumulate is extended step by step. As a result, the previously introduced compression factor defined as

$$C_{comp} = \frac{g_q^{lin}}{g_q^{comp}}, \tag{5.3}$$

that is, the ratio of the DEPFET amplification for small signals g_q^{lin} and that for high signals g_q^{comp}, has to be determined individually for every fill level of the internal gate with a different number i of overflow segments involved. Assuming a homogeneous electrostatic potential within each overflow segment and an abrupt potential step in between, C_{comp}^i can be derived from the areas of the gate region A_{cr} and of the k-th overflow region A_{of}^k based on

$$C_{comp}^i = \frac{A_{cr} + \sum_{k=1}^{i} A_{of}^k}{A_{cr}}. \tag{5.4}$$

The compression factor is increased with a larger number i of accessible overflow segments. As the area of the source stays unchanged, the compression factor observed in the prototypes can only be achieved if electrons spill over into all three overflow segments. So minimum as well as maximum amplification is still defined by DEPFET geometry and the size of the entire overflow region, as was the case for the prototypes. The staggered overflow region just smooths the response curve by introducing intermediate gains.

Geometry of additional n implantations

These intermediate gains can be adjusted by the geometric arrangement of additional deep n implantations, as illustrated in Figure 5.17.

Enlarging the area of the corresponding overflow segment reduces the fraction of signal charge stored directly underneath the transistor channel and enhances the compression factor according to equation 5.4. At the same time, the larger overflow segment equally increases charge handling capacity in the overflow segment, i.e., the amount of space charge that has to be compensated in order to equalize the potential step towards the subsequent overflow region. As a consequence, a larger segment area not only reduces DEPFET gain but also extends the energy range to which the respective gain applies. However, it does not shift the onset of electron spillover with respect to the drain current increase ΔI_D because the amount of signal charge stored in the central region remains the same.

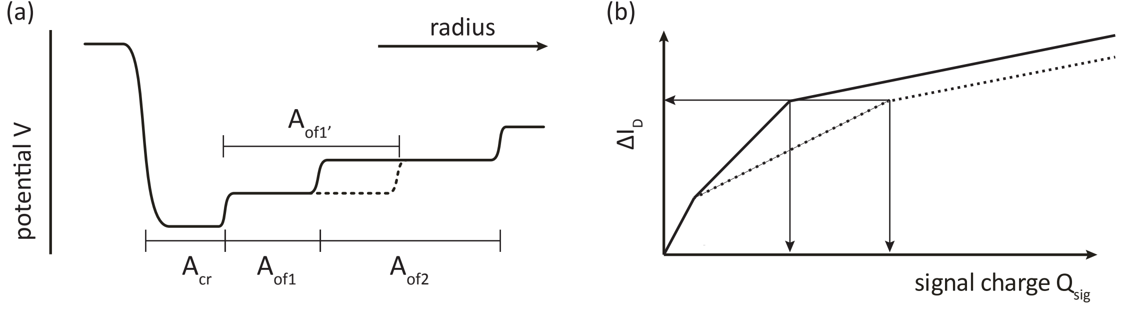

Figure 5.17: *(a) Schematic diagram of internal gate potential within a DSSC-type DEPFET featuring two overflow segments. The dashed line indicates an enlarged implantation region of the additional deep n implantation and a larger area of the overflow segment A^1_{of}. (b) The resulting nonlinear response curve for the two variants. For a larger area A^1_{of} (dashed line), the first compression region shows reduced gain and an extended energy range.*

Doping due to additional n implantations

In terms of electrons, charge handling capacity in the i-th overflow segment is taken from

$$C^i_{of} = A^i_{of} \cdot \Delta d^{i \to i+1}_{donor} \tag{5.5}$$

with $\Delta d^{i \to i+1}_{donor}$ as the difference of the integrated donor area density between the i-th and the i+1-th overflow segments. The present donor area density is defined by the n doping concentration that is not compensated by the source implantation (PSON). In the case of a fully depleted device, a lower donor concentration leads to less positive space charge and more negative potential, which is less attractive for electrons. The dashed line in Figure 5.18 (a) illustrates the change in electrostatic potential in the internal gate due to a reduction of donor concentration in the second overflow region.

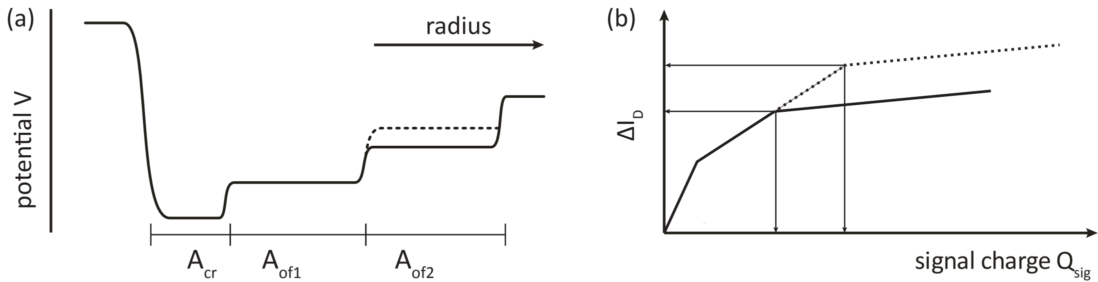

Figure 5.18: *(a) Schematic diagram of internal gate potential in a DSSC-DEPFET. The dashed line indicates a reduced n-doping concentration in the outer overflow region, leading to a higher potential step between the 1st and the 2nd overflow segment. (b) The resulting nonlinear response curve for the two variants. Although the gains remain the same, the increased potential step extends the energy range of the first compression region.*

The lower donor concentration decreases positive space charge and leads to a higher po-

tential step between the two overflow regions. As indicated in (b) this has no impact on compression factors since charge splitting between the central part and the overflow segments remains the same. However, more space charge has to be compensated to equalize the potential step between the 1st and the 2nd overflow region, which extends the energy range of the first compression region. In addition, ΔI_D at beginning spillover into the 2nd overflow region is enhanced as well, because more electrons are stored in the central part due to the higher potential swing.

Conclusion

Optimizing sizing as well as implantation parameters for the additional deep n implantations allows us to adjust the gain independent of the energy range of the compression regions. In general, this facilitates customization of the nonlinear detector response for the specific demands of various experiments. However, due to the wide range of applications for the DSSC detector, the nonlinear response curve has been tuned in order to satisfy the requirements of photon energies between 500 eV and 6 keV concurrently.

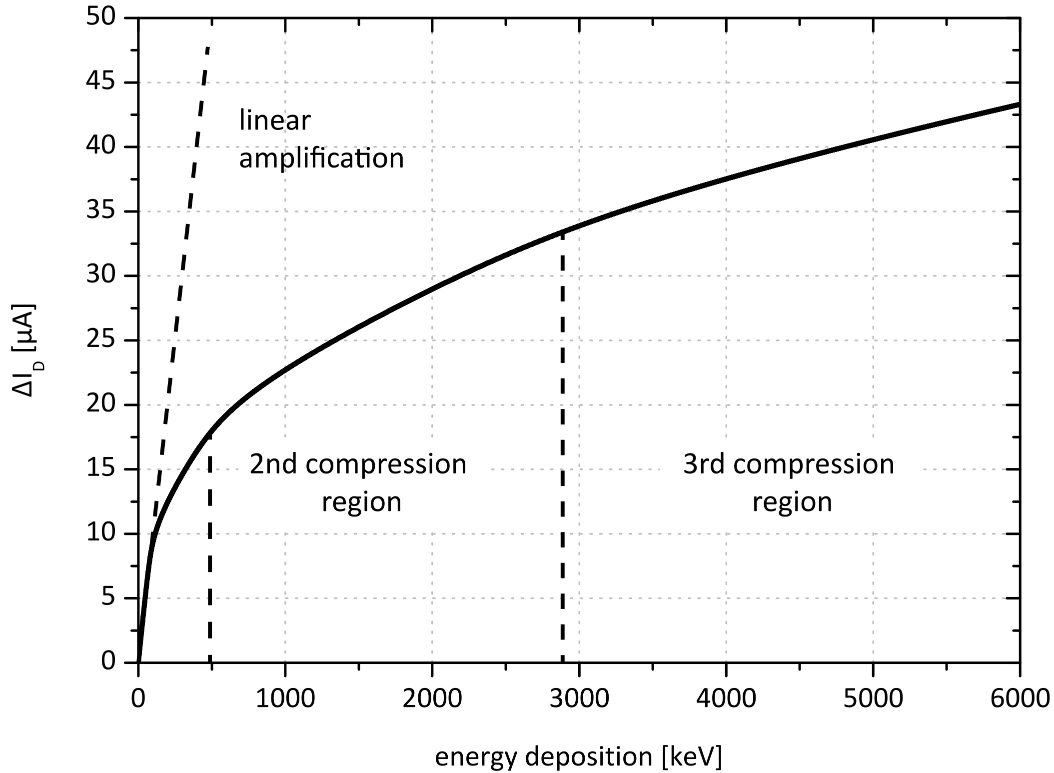

Figure 5.19: *Simulated nonlinear response curve for the final DSSC-DEPFET fabricated using optimized technology for a drain voltage of -3 V.*

Figure 5.19 depicts the expected response of the final DSSC-DEPFET. It has been simulated according to the procedure discussed in chapter 4.3.2.3 including the area and 3D corrections. The structure considers the advanced technology with improved radiation hardness and

high-speed readout capabilities. For a source drain voltage of V_{DS}=-3 V, the linear region with high amplification goes up to an energy deposition of 80 keV. The energy range and the expected compression factors for the three compression regions are summarized in table 5.2.

region	energy range [keV]	C_{comp}
linear region	0-80	1
1st compression region	80-470	≈ 7
2nd compression region	470-2880	≈ 20
3rd compression region	≥ 2880	≈ 55

Table 5.2: *Simulated parameters of the expected pixel response for the final DSSC-DEPFET fabricated using optimized technology. The compression factor C_{comp} indicates the ratio of amplification in the first linear region and amplification in the respective compression region.*

Due to technological fluctuation during the fabrication process, some deviations in the actual detector response are expected with possible reasons being variations in implantation doses, layer thicknesses or structure sizes. Although process quality is constantly monitored during the production, these fluctuations are unavoidable. Therefore, the response curve of the final DSSC-DEPFET was tailored in such a way that it can sustain these unpredictable deviations over a wide spectrum without degrading the dynamic range of the detector system. For the prototypes discussed in chapter 4, the simulations systematically predicted a roughly 10% higher onset energy for signal compression than was measured for the real devices. As soon as the first final DSSC-DEPFETs are available, measurements of the detector's response will again allow for a quantitative verification of the simulations. This information will provide the basis for further studies of the fluctuations in the actual production process as well as for future adaptations of the DSSC-DEPFET.

6. Summary

The European X-ray free electron laser (XFEL) is a research facility currently under construction in Hamburg. Starting in 2015, it will deliver ultra-short and coherent X-ray pulses with a maximum repetition rate of 4.5 MHz. These extremely bright flashes will exhibit unprecedented brilliance that is at least six orders of magnitude grater than state-of-the-art synchrotron sources. The European XFEL will unleash completely new opportunities for a wide range of basic research covering biology, chemistry, physics and material science.

In order to benefit from the exceptional properties of the facility, new 2D detector systems with single-photon detection capability, high dynamic range and a maximum frame rate of 4.5 MHz will be required. The DSSC (DEPFET Sensor with Signal Compression) is one of three detector systems currently under development and focuses on the low-energy X-ray range between 500 eV and 6 keV. The DSSC is based on a DEPFET active pixel sensor with nonlinear gain, i.e., high gain for small signals to allow for the detection of single low-energy X-rays and reduced gain for high signals to extend the dynamic range to several thousand photons per pixel and frame. Despite the lower gain for large signals, energy resolution of the DSSC will in any case be better than the natural Poisson noise of the photon generation process in the FEL.

Not only were initial DSSC-DEPFET prototypes realized as part of this thesis, but a new test setup was also built and dedicated measurement techniques were developed in order to capture and asses the new properties of the devices. This included the evaluation of suitable measurement routines, the determination of proper operating conditions and the defining of noteworthy figures of merit for nonlinear response curves, all of which enable the comparison of different curves. In summary, the signal compression mechanism has been verified successfully, based on this conceptual part of the thesis. Furthermore, the nonlinear response curves of seven-cell clusters of different layout variants have also been measured, and the scalability of the onset energy of signal compression with gate geometry has been proven.

Since the operation of large arrays of DSSC-DEPFETs within the DSSC detector system puts severe requirements on the homogeneity of the sensors, we investigated the device properties given varying supply voltages. These measurements were intended to determine the operating windows for the DSSC-DEPFET during use and it was shown that the devices work in a very wide range of conditions. The DSSC-DEPFETs will therefore be able to cope with technological inhomogeneities that are inevitable on big sensor arrays. Moreover, the experiments also demonstrated the adjustability of DEPFET amplification using drain

voltage. Even after production this unique feature allows for the optimization of the nonlinear response curve for various photon energies and therewith for the maximization of the dynamic range of the detector system.

Device simulations play a crucial role in the development of DSSC-DEPFETs and before the start of this thesis a coherent physical model of the DSSC detector amplifier structure was missing. Indeed, a comparison of measured onset energy of signal compression with values derived from 2D device simulations revealed discrepancies of up to 60%. What's more, increased deviations for smaller gate dimensions indicated 3D effects that cannot be modeled by 2D simulations. Therefore, an advanced simulation approach was developed based on a combination of 2D and newly introduced 3D device simulations. The 2D approach facilitates detailed discretization and includes a simulation of the fabrication process in order to improve modeling for doping profiles. The 3D simulation allows for quantitative analysis of changes in amplification properties due to the noncylindrical symmetry of a DEPFET. Combining 2D and 3D simulations significantly improved overall accuracy. It also enhanced the predictability of amplification properties, especially for the small gate geometries required to achieve signal compression for small energy depositions in the sensor. This new simulation approach will therefore be an indispensable tool for optimizing DSSC-DEPFETs for future applications focusing exclusively on low-energy photons. For the first time, the 3D simulation also enabled the visualization of 3D effects within a DEPFET sensor. This significantly contributed to the understanding of all involved physical processes during sensor operation.

Based on these findings and the improvements in device modeling derived within this thesis, production technology for the next generation of DSSC-DEPFETs has been optimized to the demands of the European XFEL. Thinning gate insulators improved radiation hardness by more than a factor of two and the impact of two additional deep n implantations on the detector performance was thoroughly studied. It has been shown that these implantations not only speed up the charge collection but also smooth the response curve and allow for the customization of DEPFET amplification properties. In fact, the simulations indicate that the next generation of DSSC-DEPFETs will provide very fast charge collection times of less than 60 ns, and that the shape of the response curve allows for single-photon detection as well as for a dynamic range of several thousand photons per pixel and frame for photon energies between 500 eV and 6 keV. However, this has to be verified experimentally as soon as the final devices are available.

Despite the continuous monitoring of the DEPFET fabrication process, small fluctuations are unavoidable in implantation doses, layer thicknesses or structure sizes, for example. These fluctuations will lead to an individual nonlinear response curve for each sensor pixel and in order to compensate for this, a pixel-based calibration of the DSSC detector system is required. To this end, a new method of internal charge injection has been developed within the framework of this thesis. It is based on pulsed forward biasing of a small diode integrated in each pixel and it does not require additional hardware in order to allow for a

fast, pixel-by-pixel, in-situ calibration of all pixels at once. The excellent accordance with test charge generation by external irradiation demonstrated the functionality of the internal charge injection mechanism and its insensitivity to device inhomogeneities. Furthermore, the internal charge injection can be used for quick "health checks" for the entire detector system. For these reasons, the new technique will be the baseline calibration method for the final DSSC detector system.

This thesis has addressed all relevant aspects of the DSSC-DEPFET sensor development and therefore provides a comprehensive basis for the application of DEPFETs with nonlinear amplification in the experimental environment of the European XFEL. Moreover, the improved simulation models also enable the fast and reliable customization of amplification properties for other photon counting applications in future free electron laser experiments.

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B. IS injection

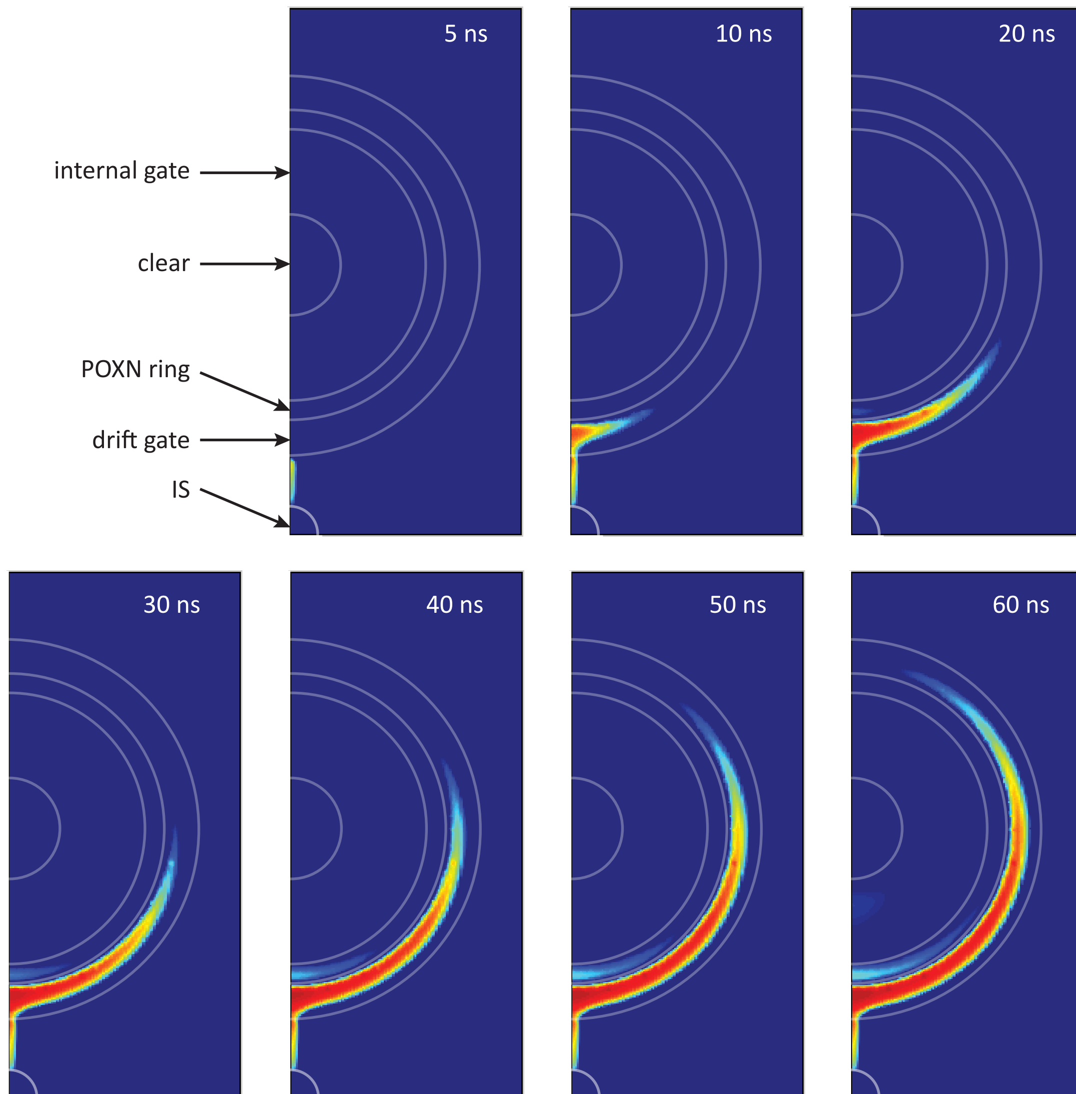

Figure B.1: *Simulated electron density on a horizontal cut through the test device depicted in Figure 4.34 at a depth of 0.8* μm *during IS injection. The time sequence starts from a fully depleted device and shows the electron distribution as a function of the injection time.*

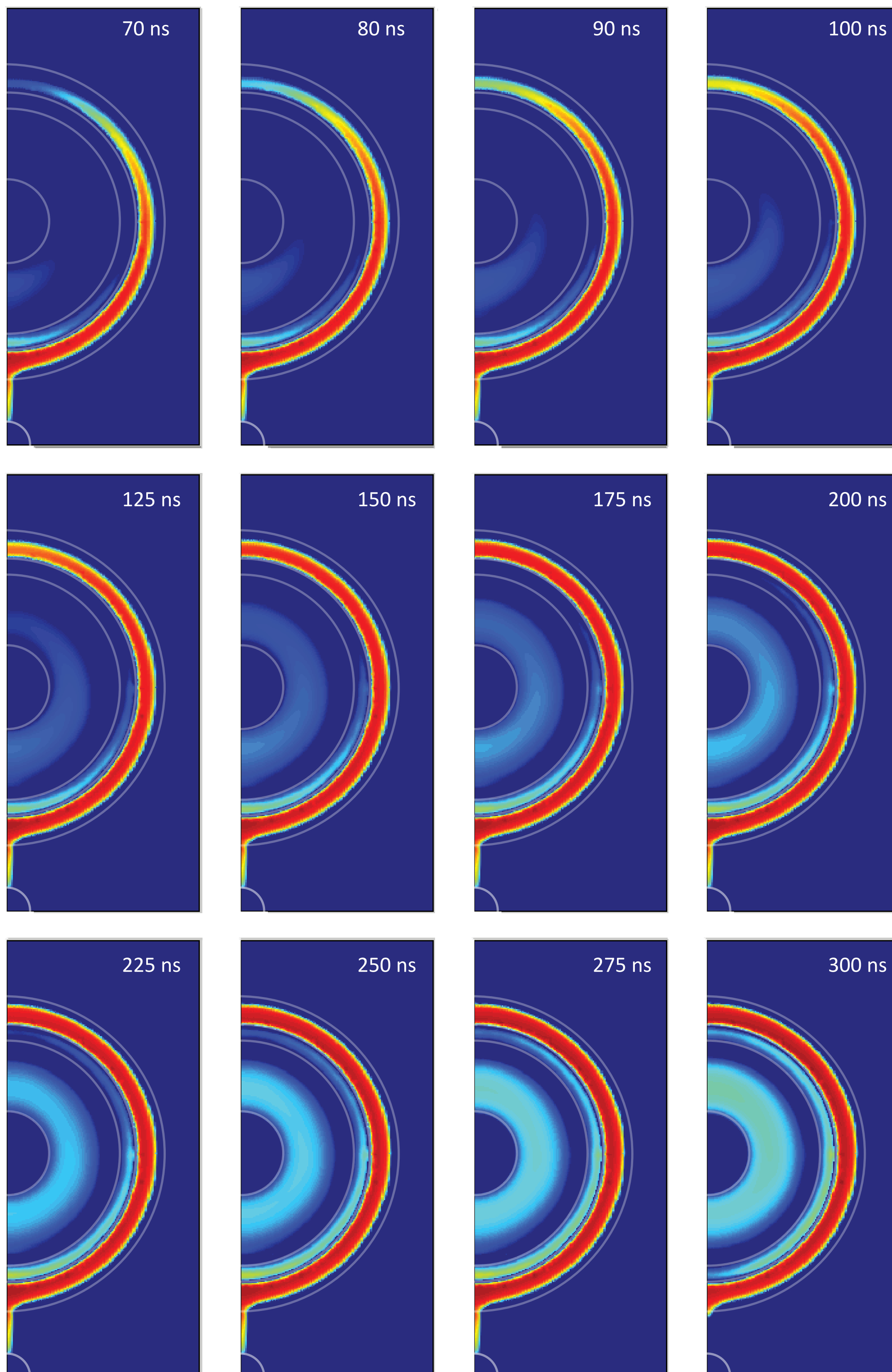

Figure B.2: *Simulated electron density on a horizontal cut through the test device depicted in Figure 4.34 at a depth of 0.8 μm during IS injection. The time sequence shows the electron density between 70 ns after the beginning and the end of injection. At t=300 ns a positive voltage is applied to the IS and electrons are extracted from the device.*

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