Technische Universität München
-
Max-Planck-Institut für Physik

Radiation Hardness Studies for DEPFETs in Belle II

Andreas Ritter

Vollständiger Abdruck der von der Fakultät für Physik
der Technischen Universität München zur Erlangung des
akademischen Grades eines

Doktors der Naturwissenschaften (Dr. rer. nat.)

genehmigten Dissertation.

Vorsitzende: Univ.-Prof. Dr. Nora Brambilla
Prüfer der Dissertation:

1. Hon.-Prof. Allen C. Caldwell, Ph.D.
2. Univ.-Prof. Dr. Stephan Paul

Die Dissertation wurde am 28.11.2013 bei der Technischen Universität München
eingereicht und durch die Fakultät für Physik am 17.2.2014 angenommen.

Technische Universität München
Max-Planck-Institut für Physik

Radiation Hardness Studies for DEPFETs in Belle II

Andreas Ritter

28.11.2013

Betreut durch Prof. Allen Caldwell

Abstract

The study of CP violation requires dedicated detectors and accelerators. At KEK, the High Energy Accelerator Research Organization located in Tsukuba, Japan, an upgrade of the present accelerator KEKB and its detector is in progress. For this new Belle II detector, a new vertex system will be installed, consisting of a silicon strip detector (SVD) and a pixel detector (PXD). The PXD exhibits eight million pixels, each of them made of Depleted p-channel Field Effect Transistors (DEPFETs).
During the operation of Belle II various machine- as well as luminosity-related background processes affect the device performance of the DEPFET through radiation damage. As a Metal-Oxide-Semiconductor (MOS) device, the DEPFET is affected by ionizing radiation damage as well as by damages to the silicon bulk itself.
The major part of the radiation damage has its origin in the creation of electrons and positrons near the interaction point. Therefore, the hardness factor of electrons of relevant energy was investigated in this work. With this quantity the damage by electrons could be compared to the damage inflicted by neutrons. Neutron irradiations were performed with DEPFETs and related silicon material. The effects of leakage current increase and type inversion were studied.
As the electron hardness investigation indicates, the bulk damage done to the DEPFET is small in comparison to the impact on the silicon dioxide layer of the device. Ionizing radiation results in a build-up of oxide charge, thus changing the device characteristics. Especially the threshold voltage of the DEPFET is shifted to more negative values. This shift has to be compensated during the operation of Belle II and is limited by device and system constraints, thus an overall small shift is desired.
The changes in the device characteristics were investigated for the two gate electrodes of the DEPFET with respect to their biasing and production related issues. With an additional layer of silicon nitride and a proper type of oxidation the influence of the alterations are minimized. For the evaluation DEPFET equivalent devices were utilized. Recommendations for the final production could thus be made.
The thesis is continued with a discussion on surface damage annealing and a proposed model for the ionizing radiation damage in Metal-Nitride-Oxide-Semiconductor (MNOS) devices. A suitable model helps by predicting the radiation damage in the DEPFET, facilitating design considerations for the production of the device. The model is based on an electric field dependent charge yield in the oxide and nitride insulator with subsequent trapping of the resulting electrons and holes.
An estimation for the expected signal performance of the DEPFET in Belle II as well as the behavior to inhomogeneous irradiation in the PXD conclude this work.

Zusammenfassung

Das Erforschen der CP Verletzung verlangt nach geeigneten Beschleunigern und Detektoren. Am KEK, der Hochenergie- und Beschleunigerforschungsorganisation in Tsukuba, Japan, findet ein Upgrade des bestehenden Beschleunigers KEKB und seines Detektors statt. Ein Vertexsystem wird für den neuen Belle II Detektor installiert, welches aus einem Siliziumstreifendetektor (SVD) und einem Pixeldetektor (PXD) besteht. Der PXD verfügt über acht Millionen Pixel, von denen jeder einzelne aus einem Depleted p-channel Field Effect Transistor (DEPFET) aufgebaut ist.

Während der Betriebsdauer von Belle II beeinflussen verschiedene Beschleuniger- und Luminositätsbasierende Untergründe das Verhalten des DEPFET. Als ein Bauteil welches auf dem Metal-Oxide-Semiconductor (MOS)-Übergang basiert, wird der DEPFET durch ionisierende Strahlung im Oxid, wie auch durch Strahlung im Silizium selbst geschädigt.

Die Hauptquelle der Strahlung hat ihren Ursprung in der Erzeugung von Elektronen und Positronen nahe dem Wechselwirkungspunkt. Daher wurde der Härtefaktor von Elektronen im relevanten Energiebereich untersucht. Mit dieser Größe kann der Schaden welcher von Elektronen verursacht wird mit denen von Neutronen verglichen werden. Neutronenbestrahlungen wurden an Siliziummaterial durchgeführt, welches zum Material des DEPFETs vergleichbar ist und die Effekte von Leckstromzunahme und Typinvertierung untersucht.

Wie die Erforschung der Härte von Elektronen zeigt, ist der Schaden im Sliziumsubstrat des DEPFETs durch sie im Vergleich zum Schaden in der Siliziumdioxidschicht des Bauteils gering. Ionisierende Strahlung führt zu einem Aufbau positiver Ladungsträger im Oxid und verändert dadurch die Bauteileigenschaften. Diese Veränderungen wurden für die zwei Gateelektroden des DEPFETs untersucht. Berücksichtigt wurden hierbei produktionsspezifische Fragestellungen, wie die Menge an Siliziumnitrid und die Wahl des Oxidationsverfahrens, als auch das Verhalten aufgrund unterschiedlicher elektrischer Potentiale. Zu diesem Zweck wurden Bauteile verwendet, welche zum DEPFET äquivalent sind. Damit konnten Empfehlungen für die finale Produktion gewonnen werden.

Die Arbeit wird mit einer Diskussion über das Ausheilen von Strahlenschäden und einem vorgestellten Modell zur Beschreibung der Auswirkung ionisierender Strahlung in Metal-Nitride-Oxide-Semiconductor (MNOS) Bauteilen fortgesetzt. Ein geeignetes Modell der Strahlenschäden in MNOS Bauteilen kann die zukünftige Design- und Entwicklungsphase neuerer Strukturen erleichtern. Es basiert auf der Ladungsträgerausbeute in beiden Isolatorschichten mit anschließendem Einfangen der resultierenden Elektronen und Löcher.

Eine Abschätzung des zu erwartenden Signalverhaltens des DEPFETs in Belle II, sowie das Verhalten aufgrund inhomogener Bestrahlung schließen diese Arbeit ab.

Contents

1. Introduction **1**

2. The Belle II Project **5**

2.1. Particle Physics Motivation . . . 5
2.1.1. C-, P-, T-Operations and CP-Violation . . . 5
2.1.2. Flavor Physics . . . 6
2.1.3. Unitarity Triangle . . . 7
2.1.4. Time Dependent CP Violation . . . 9
2.1.5. Entangled State for B Mesons . . . 10
2.1.6. Measurement of CP Violation . . . 11
2.2. Belle II Detector . . . 12
2.2.1. Pixel Detector (PXD) . . . 13
2.2.2. Silicon Vertex Detector (SVD) . . . 14
2.2.3. Central Drift Chamber (CDC) . . . 14
2.2.4. Particle Identification at End-Caps (ARICH) . . . 14
2.2.5. Particle Identification along the Barrel (PID, TOP) . . . 15
2.2.6. Electromagnetic Calorimeter (ECL) . . . 15
2.2.7. Kaon and Muon Detection (KLM) . . . 15
2.3. The Pixel Detector (PXD) . . . 16
2.3.1. Layout . . . 17
2.3.2. Electronics . . . 18
2.4. Radiation Background at Belle II . . . 19
2.4.1. Touschek Effect . . . 19
2.4.2. Four-Fermion Final State Radiation . . . 20
2.4.3. Radiative Bhabha and Neutron Flux . . . 21
2.4.4. Synchrotron Radiation . . . 23
2.4.5. Summary . . . 23

3. Semiconductor Physics and Devices **25**

3.1. Introduction to the DEPFET . . . 25
3.2. Metal-Oxide-Semiconductor Capacitor . . . 26
3.2.1. Design of a MOS Capacitor . . . 26
3.2.2. Ideal MIS/MOS Capacitor . . . 27
3.2.3. Surface Space-Charge Region . . . 30
3.3. Metal-Oxide-Semiconductor Field Effect Transistor . . . 33
3.3.1. Introduction . . . 33
3.3.2. Current-Voltage Characteristic . . . 34
3.3.3. Threshold Voltage . . . 36
3.3.4. Output Characteristics . . . 36

3.3.5. Subthreshold Region . . . 37
3.4. DEPFET . . . 38
3.4.1. Sidewards Depletion . . . 39
3.4.2. Working Principle . . . 41
3.4.3. Current-Voltage Characteristic of a DEPFET . . . 42
3.5. Gate Controlled Diode . . . 43
3.5.1. Layout . . . 44
3.5.2. Mode of Operation . . . 45
3.6. Fabrication and Processing . . . 49
3.6.1. Silicon Dioxide . . . 49
3.6.2. Silicon Nitride . . . 50
3.6.3. Interface Trap Annealing . . . 51

4. Radiation Damage in Semiconductor Devices 53
4.1. Bulk Damage . . . 53
4.1.1. Lattice Distortions . . . 53
4.1.2. Manifestation of Defects . . . 54
4.1.3. The NIEL Scaling Hypothesis . . . 54
4.2. Oxide Damage . . . 56
4.2.1. Microscopic View on Interface Traps . . . 56
4.2.2. Microscopic View on Oxide Traps . . . 59
4.2.3. Influence of Oxide Thickness . . . 61
4.2.4. Radiation Hardness of Wet and Dry Oxide . . . 62
4.2.5. Gate Length Dependent Radiation Damage . . . 63
4.2.6. Influence of Gate Potential . . . 65

5. Experiments on Bulk Damage 69
5.1. Electron Irradiation and Hardness Factor . . . 69
5.1.1. Experiment . . . 69
5.1.2. Analysis . . . 70
5.2. Neutron Irradiations . . . 72
5.2.1. Type Inversion . . . 73
5.2.2. Increase in Detector Noise . . . 74
5.3. Summary and Conclusions . . . 79

6. Experiments on Interface Traps 81
6.1. Interface Trap Distribution from MOS Capacitor Measurements . . . 81
6.1.1. Measuring Technique . . . 81
6.1.2. Measurements . . . 85
6.1.3. Results and Discussion . . . 87
6.2. Interface Trap Density from MOSFET Measurements . . . 92
6.2.1. Calculation of Changes in Interface Trap Density . . . 92
6.2.2. Measurements of MOSFETs . . . 93
6.2.3. Results of Interface Trap Changes . . . 93
6.2.4. Influence of Interface Trap Density on Transconductance . . . 98
6.3. Interface Trap Extraction from GCD Measurements . . . 100
6.3.1. Interface Trap Density . . . 100

6.3.2. Measurement Procedure . . . 103
6.3.3. Results and Discussion . . . 104
6.4. Conclusions . . . 109

7. Experiments on Oxide Damage 111
7.1. Introduction . . . 111
7.1.1. Influence of Gate Voltage Shifts . . . 111
7.1.2. Influence of Clear Gate Voltage Shifts . . . 112
7.1.3. Design/Production Options for the DEPFET . . . 112
7.2. Measurement Methods for the Threshold Voltage . . . 115
7.2.1. Saturation Mode . . . 116
7.2.2. Linear Mode . . . 116
7.2.3. DUT Description . . . 116
7.3. Threshold Voltage Shift Studies for the Gate . . . 118
7.3.1. Biasing Schemes for the Gate . . . 118
7.3.2. Measurements and Results . . . 119
7.3.3. Summary/Conclusions for the Gate . . . 125
7.4. Threshold Voltage Shift Studies for the Clear Gate . . . 125
7.4.1. Biasing Schemes for the CLG . . . 125
7.4.2. Measurements and Results . . . 127
7.4.3. Summary/Conclusions for the Clear Gate . . . 131
7.5. Summary . . . 131

8. Surface Damage Annealing 133
8.1. Introduction . . . 133
8.1.1. Tunnel Annealing . . . 134
8.1.2. Thermal and Bias Annealing . . . 136
8.2. Room Temperature Annealing . . . 136
8.2.1. Comparison of Annealing Behavior . . . 136
8.2.2. Interface Trap Annealing - Latent Build-Up . . . 144
8.3. Elevated Temperature Annealing . . . 146
8.3.1. Description of Experiment . . . 146
8.3.2. Results of Transistor Annealing . . . 146
8.3.3. Results of GCD Annealing . . . 147
8.4. Impact on PXD/Belle II . . . 147

9. Proposed Model for Radiation Damage in MNOS Devices 153
9.1. Motivation for a Model of Radiation Damage in MNOS Devices . . . 153
9.2. Charge Yield and Trapping . . . 154
9.3. Applied Voltage and Resulting Electric Field . . . 155
9.3.1. Potential for the Clear Gate . . . 155
9.3.2. Potential for Gate . . . 156
9.4. Fitting of Data . . . 156
9.5. Model Parameters . . . 157
9.6. Comparison of Prediction and Data . . . 158
9.7. Summary and Conclusion . . . 162

10. Estimations of the DEPFET Performance in Belle II 169
10.1. Expected DEPFET Signal Performance . . . 169
10.1.1. Introduction . . . 169
10.1.2. Required Internal Amplification . . . 169
10.1.3. Noise Overview . . . 170
10.1.4. Tolerable Temperature . . . 170
10.1.5. Detector Efficiency . . . 171
10.2. Influence of Inhomogeneous Irradiation . . . 172
10.2.1. Motivation . . . 172
10.2.2. Impact on the PXD . . . 174
10.2.3. Drain Current Scenarios . . . 178
10.3. Summary . . . 185

11. Summary and Outlook 187

A. Irradiation Facilities 191
A.1. X-Ray Irradiation at the Karlsruhe Irradiation Center . . . 191
A.2. Electron Irradiation - Synergy Health . . . 192

B. Measurement of MOSFETs 193
B.1. DUT Overview MOSFETs . . . 193
B.2. Threshold Voltage . . . 194
B.2.1. Threshold Voltage from Input Characteristics in Saturation Mode . . . 194
B.2.2. Threshold Voltage from Input Characteristics in Linear Mode . . . 194
B.3. Subthreshold Swing . . . 196
B.3.1. Extracting the Subthreshold Swing from Saturation Measurements . . . 196
B.4. Transconductance . . . 197
B.4.1. Extraction of Transconductance from Input Characteristics . . . 197
B.4.2. Errors on Transconductance . . . 197

C. CV Measurements of MOSCAPs 199
C.1. DUT Description . . . 199
C.2. Measurement Corrections . . . 199

D. Measurements of GCDs 203
D.1. Overview of GCDs . . . 203

E. Model Parameters 205

F. Acronyms 207

Chapter 1.

Introduction

In the past decades, the Standard model of elementary particle physics (SM) has proven to be extremely successful. However, some observations like the dominance of matter vs. anti-matter in the universe cannot be readily explained. This asymmetry in the genesis of baryons requires three criteria to be met, first formulated by Sakharov [1] in 1967 (republished 1991). These Sakharov conditions state:

1. Violation of the baryon number $\mathcal{B}$.
2. Violation of C and CP symmetry.
3. No thermal equilibrium.

The first point is evidently a necessary starting point. In order to have more baryons to be generated the proper conservation quantity has to be violated. This can be represented via ([2])

$$X \rightarrow Y + B, \tag{1.1}$$

in which X and Y are particles with $\mathcal{B}_{X,Y} = 0$ and B represents the excess of Baryons ($\mathcal{B} > 0$). However, in the SM this quantity is conserved and such a process was up to now not observed.

The second condition states that a process under charge-conjugation symmetry C, which would result in equal production rates for baryons and anti-baryons, has to be violated, thus reaction rates Γ are

$$\Gamma(X \rightarrow Y + B) \neq \Gamma(\overline{X} \rightarrow \overline{Y} + \overline{B}). \tag{1.2}$$

Also the CP process must be violated. The particle X may decay into two left-handed or right-handed quarks according to

$$X \rightarrow q_L q_L, \tag{1.3}$$
$$X \rightarrow q_R q_R. \tag{1.4}$$

Thus, if C and CP were a symmetry of nature equal production rates via

$$\Gamma(X \rightarrow q_L q_L) + \Gamma(X \rightarrow q_R q_R) = \Gamma(\overline{X} \rightarrow \overline{q}_L \overline{q}_L) + \Gamma(\overline{X} \rightarrow \overline{q}_R \overline{q}_R) \tag{1.5}$$

would prevent an asymmetry between baryons and anti-baryons.

The third statement must be fulfilled to prevent an inverse reaction rate of equation 1.1, which would be in effect in a thermal equilibrium. Thus, the condition

$$\Gamma(Y + B \rightarrow X) = \Gamma(X \rightarrow Y + B) \tag{1.6}$$

would restore the baryon asymmetry.

In the frame of the SM great efforts have been put into the study of CP violating effects. Nevertheless, the measured and predicted rates cannot account for the observed matter/anti-matter asymmetry in the universe. However, the information is still not complete and dedicated experiments have been and are going to be built in order to shed some light into this elusive aspect.
Collaborations of particle physicists have been formed for this endeavor and resulted in successful experiments such as BaBar[1] or LHCb[2]. One of those aforementioned experiments is the upgrade of the Belle experiment towards Belle II, which focuses on the study of the decays of generated $B^0/\overline{B}^0$ pairs. CP violating effects can e.g. be observed if particle and anti-particle end up in the same final state. Since their lifetimes and especially the difference in their lifetimes is very small, high precision detector components are required for measurements in this system.
The accelerator structure creates a boost of the system which translates the difference in their lifetimes into a spatial distance of their decay vertices. The reconstruction of the vertices is made possible by precision vertex detector instruments. The first in line is the Pixel Detector (PXD), consisting of Depleted p-channel Field Effect Transistor (DEPFET) pixels. The DEPFET has many advantages such as an intrinsic amplification and low noise, which makes it the detector of choice for the PXD. Yet, as a silicon semiconductor device it suffers from the radiation generated in the interaction point and from other radiation background processes in the detector environment.

The major part of the radiation damage has its origin in the luminosity-related creation of electrons and positrons at the interaction point. These low energetic particles traverse the DEPFET, causing on their way both damage to the bulk and to the oxide layer of the device. This layer, common in all Metal-Oxide-Semiconductor (MOS) devices, is affected twofold.
One aspect is the build-up of positive charge at the interface, leading to different device characteristics such as a change in the threshold voltage. This is influenced by the type of oxide and may be compensated partially by an additional layer of silicon nitride. The other aspect is the creation of interface traps, which manifest as additional noise of the device.
Bulk damage on the other hand is caused by a distortion in the crystal lattice, altering the properties of the silicon itself. The damage is observed e.g. by an increase in leakage current and in a change of doping concentration.

In this work all three aspects of the radiation damage, i.e. oxide trapped charge, interface traps, and bulk damage, are investigated. Production parameters, such as the type of oxidation and nitride layer thicknesses are studied in order to find optimal operation conditions for the DEPFET in the Belle II experiment. With such optimized device parameters a longer lifetime of the DEPFET in the radiation environment can be expected.
The annealing of defects is also investigated since dose rates in the final experiment are considerably smaller than the ones used for irradiation experiments in this thesis.
A model for the behavior of the radiation induced threshold voltage shift due to ionizing

[1] `http://www-public.slac.stanford.edu/babar/default.aspx`
[2] `http://lhcb-public.web.cern.ch/lhcb-public/`

radiation is presented at the end of this work. It is accompanied by estimations for the DEPFET with respect to the integrated luminosity, such as detector noise and different device/system behavior caused by inhomogeneous irradiation profiles.

Chapter 2.

The Belle II Project

CP violation is an important part in the standard model and is a key to the matter/antimatter asymmetry in our universe. The study of it evolved from the first occurrence in the kaon system to the study of CP violations of neutral B mesons. Dedicated accelerators and detectors were developed for this endeavor. The already successful particle detector Belle [3] is now being upgraded towards Belle II.
Starting from a particle physics point of view, CP violation is reviewed briefly, then the intended Belle II detector is presented. The Pixel Detector (PXD), i.e. the detector closest to the interaction point and consisting of Depleted p-channel Field Effect Transistor (DEPFET) pixels, is closer examined. The layout of this subdetector is presented in this chapter, as well as the various radiation background components which are responsible for the radiation damage of the DEPFET pixels.

2.1. Particle Physics Motivation

This section is a brief introduction into the field of particle physics and CP violation. Further reading on this matter can be found in [4, 5, 6].

2.1.1. C-, P-, T-Operations and CP-Violation

Symmetries play an important role in modern physics. Each continuous symmetry operation which leaves a system invariant corresponds to a conservation law (Noether's Theorem [7]). In this way the translation of time corresponds to the conservation of energy and the translation of coordinates $\mathbf{x} \rightarrow \mathbf{x}'$ to the conservation of momentum.
In addition to the continuous symmetries, the Standard model of elementary particle physics (SM)[1] also relies on discrete symmetry operations. Important discrete symmetries are charge conjugation C, parity transformation P, and time reversal T.
The effect of the charge conjugation operator C on a wave function of a particle $|\Psi\rangle$ alters this state into its antiparticle by changing all relevant quantum numbers (not only electric charge),

$$C\,|\Psi\rangle = |\overline{\Psi}\rangle\,. \tag{2.1}$$

A parity operation inverts space coordinates with respect to the origin,

$$P\,|\Psi(\mathbf{x})\rangle = |\Psi(\text{-}\mathbf{x})\rangle\,. \tag{2.2}$$

[1] Since the SM has many developers a historical review on the achievements of particle physicists is given in [8]

E.g. it leaves the spin of a particle unaffected ($\mathbf{s} \xrightarrow{P} \mathbf{s}$), and due to a change in momentum $\mathbf{p} \xrightarrow{P} \mathbf{-p}$, the angular momentum $\mathbf{l} \xrightarrow{P} \mathbf{l}$ is not changed as well. In this way vectors can be distinguished into polar vectors V, which change their sign under a P operation, and into axial vectors A which are invariant under P transformation.
The time reversal operator T simply mirrors the time of a system,

$$T\,|\Psi(t)\rangle = |\Psi(-t)\rangle\,, \tag{2.3}$$

leaving the space coordinates unchanged $\mathbf{x} \xrightarrow{T} \mathbf{x}$, but particles now move backwards $\mathbf{p} \xrightarrow{T} \mathbf{-p}$.

Those discrete symmetry considerations are necessary in physics since it can be shown quite generally that every system has to be invariant under the combined transformation of CPT, following the laws of quantum field theory. Since only the combined operations of C, P, and T are invariant it is possible that e.g. parity transformations are violated (like in weak interaction) when the two other operations combined (C and T) restore the system. In this way, CP violation is possible if the time reversal operation T is also violated. The first evidence of CP violation was found in 1964 by Cronin, Fitch, and Christenson et al. [9] and the following sections will describe this property of the SM in more detail.

2.1.2. Flavor Physics

The SM describes the interaction of particles by three different forces, the Electromagnetic (EM), the weak[2] and the strong force. The forces are represented via the exchange of force carrier particles among leptons and quarks. The latter can be represented in three different generations and each of the six quarks has a quantum number called *flavor*. Figure 2.1 shows a summary of the available elementary particles.

The flavor quantum numbers are conserved in EM and strong interactions, but are violated in weak interactions (i.e. changing one quark into another). The weak force carrier couples to the eigenstate of the weak isospin which is rotated to the eigenstate of the quark flavor. Originally introduced by Cabbibo in 1963 [11] for $n = 2$ quark generations, the idea of rotation was generalized for $n = 3$ generations by Kobayashi and Maskawa in 1973 [12]. The formalism involves a unitary matrix V to transform the flavor eigenstates $|q\rangle$ into the weak eigenstates $|q'\rangle$,

$$\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \begin{pmatrix} d \\ s \\ b \end{pmatrix}. \tag{2.4}$$

The elements V_{ij} of the complex CKM-Matrix represents the coupling strength of the quark i converting to a quark j. In this case the electric charge changes and therefore the interaction is mediated via the W Bosons of the weak force.
The elements of the matrix are not entirely free. E.g. the sum of one row i is constrained by

$$\sum_{j=1}^{n} |V_{ij}|^2 = 1, \tag{2.5}$$

meaning that the sum of all up-type quarks (u,c,t) coupling to the down type quarks is universal. Another constraint on the matrix is the unitarity condition.

[2] which can be combined with EM to an electroweak force

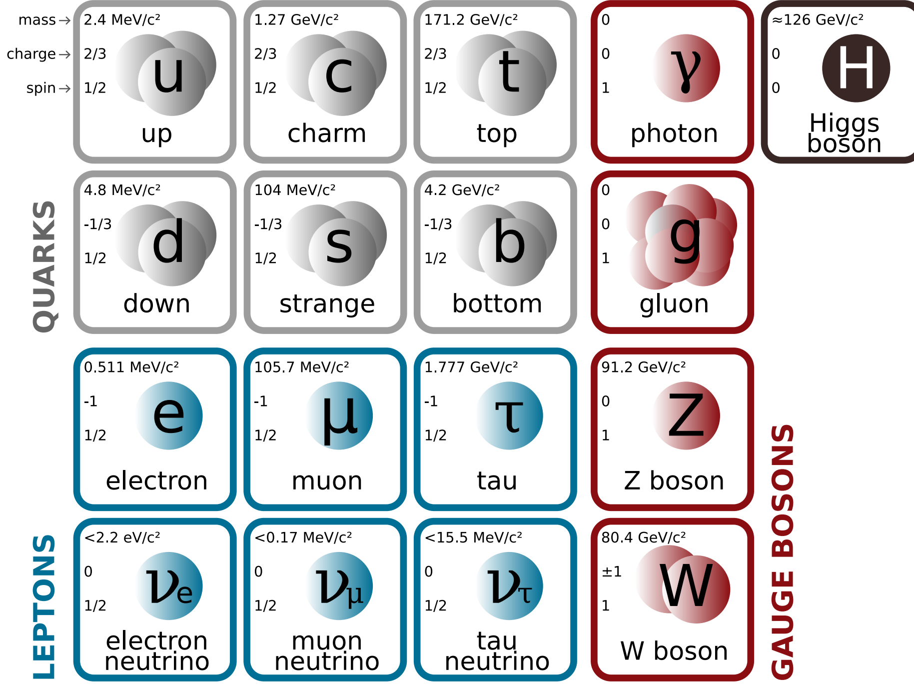


Figure 2.1.: Elementary particles of the standard model, after [10].

2.1.3. Unitarity Triangle

For the conservation of probability, the CKM-Matrix has to be unitary. This will lead to a set of equations, which have to satisfy

$$V_{ik}^{*} V_{ij} = \delta_{kj}. \tag{2.6}$$

This condition results for the case of $k = 2$ and $j = 1$ into the equation

$$V_{us}^{*} V_{ud} + V_{cs}^{*} V_{cd} + V_{ts}^{*} V_{td} = 0. \tag{2.7}$$

In the kaon system the transition in the Feynman graphs (cf. figure 2.3) is made possible via the exchange of u, c and t quarks to the d and s quarks (and appropriate anti-quarks) of the kaon. From measurements in this system more information can be get on the matrix elements of equation 2.7.
Equation 2.6 can be interpreted as a triangle in complex space, but since the third term $V_{ts}^{*} V_{td}$ in equation and 2.7 is very small, the triangle is nearly flat, indicating almost no CP violation in the kaon system[3].
On the other hand, the sides of the triangle in the B system,

$$V_{ub}^{*} V_{ud} + V_{cb}^{*} V_{cd} + V_{tb}^{*} V_{td} = 0, \tag{2.8}$$

are of similar lengths, which makes this system an ideal test candidate. A good test for the SM is if the unitarity conditions of equation 2.6 hold true, i.e. if the triangle is closed.
An up-to-date picture of the triangle is shown in figure 2.2. The sides of the triangle have been normalized by $V_{cb}^{*} V_{cd}$, thus this side is going from (0,0) to (1,0).

[3] If no imaginary part existed, the triangle would be flat and no CP violation present.

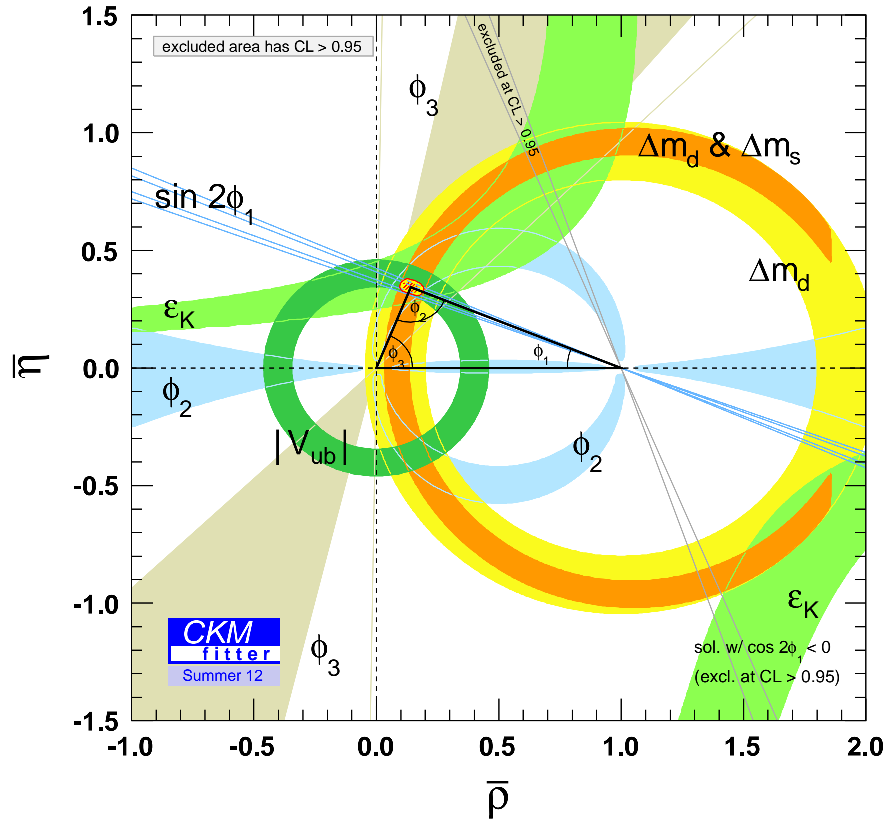


Figure 2.2.: Up-to-date picture of the unitarity triangle. The closeness is still not ensured, as can be seen by the indication on top of the triangle. *Updated plot from* [13].

2.1.4. Time Dependent CP Violation

Neutral Meson Mixing

In the kaon system a transition from K^0 into $\overline{K}^0$ was observed. The transition process is explained in leading order in the Feynman box diagrams 2.3. The situation in the B^0 system, figure 2.4, is similar. Both systems are able to oscillate between particle and anti-particle, which is called *flavor mixing*.

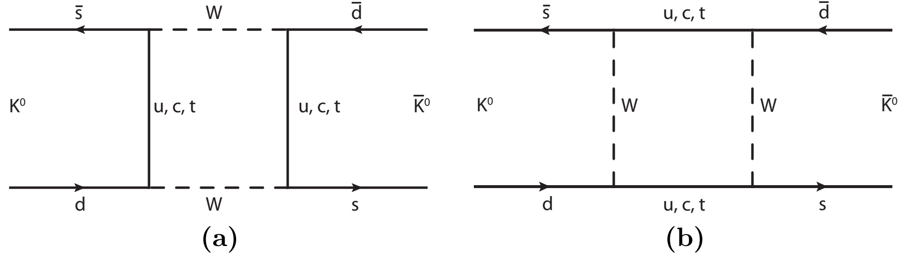


Figure 2.3.: Feynman diagram for the oscillation of K^0 to $\overline{K}^0$.

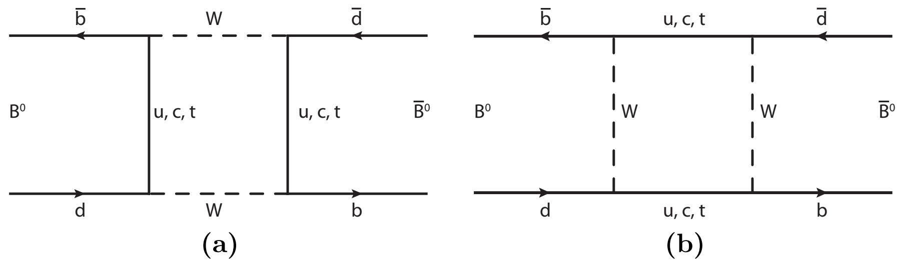


Figure 2.4.: Feynman diagram for the oscillation of B^0 to $\overline{B}^0$.

The (lighter and heavier) mass eigenstates of the B-mesons can be described as linear combinations of particle and anti-particle,

$$|B_L\rangle = p\,|B^0\rangle + q\,|\overline{B}^0\rangle \tag{2.9}$$

$$|B_H\rangle = p\,|B^0\rangle - q\,|\overline{B}^0\rangle\,, \tag{2.10}$$

in which p and q are constants. These eigenstates can, in contrast to the kaon system, hardly be distinguished. However it is possible to measure an amplitude $\mathcal{A}$ to the same final state $|f\rangle$ via the transition T,

$$\overline{\mathcal{A}}_{CP} = \langle f|\,T\,|\overline{B}^0\rangle \tag{2.11}$$

$$\mathcal{A}_{CP} = \langle f|\,T\,|B^0\rangle\,. \tag{2.12}$$

The two states of the B system oscillate into each other. Thus, in order to predict which state can be observed at a given moment in time t, one needs to solve the evolution of the oscillation process. From equations 2.9 and 2.10 a state B^0 at a moment $t = 0$ is given by

$$|B^0\rangle = \frac{1}{2p}(|B_L\rangle + |B_H\rangle). \tag{2.13}$$

Time evolution of light and heavy Bs can be expressed by

$$|B_L(t)\rangle = e^{-im_L t} \cdot e^{\Gamma_L t/2} |B_L\rangle = e^{-im_L t} \cdot e^{\Gamma_L t/2}(p\,|B^0\rangle + q\,|\overline{B}^0\rangle) \tag{2.14}$$

$$|B_H(t)\rangle = e^{-im_H t} \cdot e^{\Gamma_H t/2} |B_H\rangle = e^{-im_H t} \cdot e^{\Gamma_H t/2}(p\,|B^0\rangle - q\,|\overline{B}^0\rangle), \tag{2.15}$$

where m_L and m_H are the masses of light and heavy B's and Γ_L and Γ_H are their decay width. This leads to a time evolution for B^0 with

$$|B^0(t)\rangle = g(t)\left[\cos\left(\frac{\Delta m t}{2}\right)|B^0\rangle + i\frac{q}{p}\sin\left(\frac{\Delta m t}{2}\right)|\overline{B}^0\rangle\right], \tag{2.16}$$

with $\Delta m = m_H - m_L$ and $g(t) = e^{-i\frac{m_H+m_L}{2}t} \cdot e^{\Gamma t/2}$. The difference in the decay width Γ of the heavy and lighter B can be neglected since the time difference is very small, which was confirmed by calculations based on the box diagrams in figure 2.4.

2.1.5. Entangled State for B Mesons

From the EM interaction of $e^+ + e^- \rightarrow \gamma$ a short-lived bound state of bottonium is created, the $\Upsilon(4S)$. The short-lived meson decays almost instantaneously with a probability of $\approx 1/3$ into a pair of neutral $B^0/\overline{B}^0$ mesons.
From the quantum numbers of the initial photon, $J^{PC} = 1^{--}$, the system of the two Bs has to be in an $L = 1$ state, because $S = 0$[4].
Since parity is conserved in EM and strong interaction, the total wave function of the two Bs exhibits a negative parity. Choosing a coordinate system where one B is located at **x** and the other at **-x** results in

$$|\Psi_B\rangle = \frac{1}{\sqrt{2}}\left(|B_1(\mathbf{x})B_2(\mathbf{-x})\rangle - |B_1(\mathbf{-x})B_2(\mathbf{x})\rangle\right). \tag{2.17}$$

Applying the parity operator on this system,

$$P\,|\Psi_B\rangle = \frac{1}{\sqrt{2}}\left(|B_1(\mathbf{-x})B_2(\mathbf{x})\rangle - |B_1(\mathbf{x})B_2(\mathbf{-x})\rangle\right) \tag{2.18}$$

$$= (-1)\,|\Psi_B\rangle \tag{2.19}$$

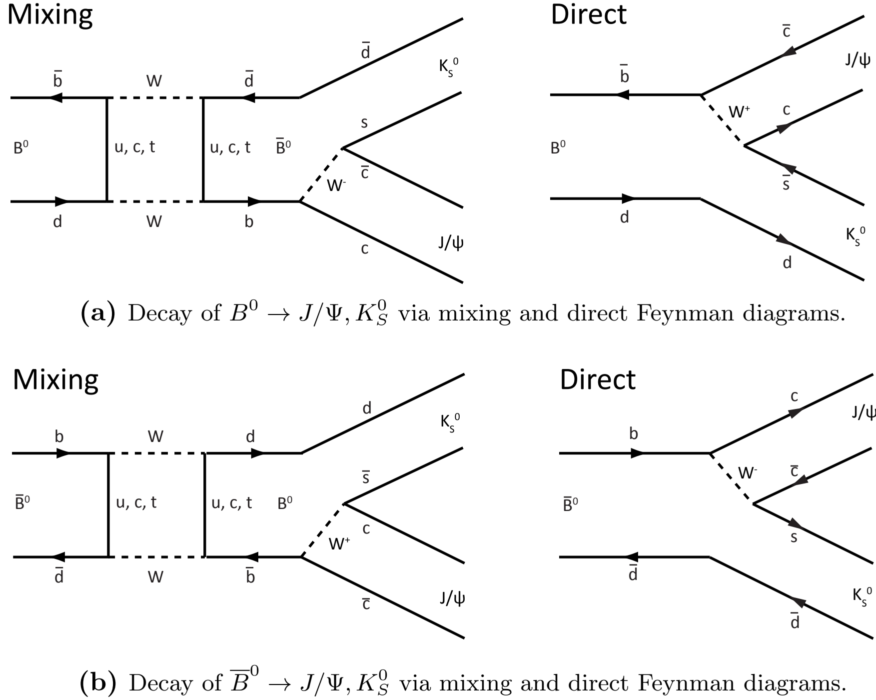
switches the space coordinates and yields the parity quantum number of the photon.

The state of the B system is determined by the asymmetric wave equation 2.17, in which for B_1 and B_2 the time evolution of equation 2.16 for B^0 and the appropriate equation for $\overline{B}^0$ can be inserted.
In section 2.1.4 it was shown that the neutral B meson can oscillate into its own antiparticle (equation 2.16). Therefore it is possible to assume a time t' at which two identical B^0B^0 or $\overline{B}^0\overline{B}^0$ mesons arise. However, identical bosonic particles would require, according to Bose-Einstein statistics, a symmetric wave function. Yet, as long as the wave function $|\Psi_B\rangle$ does not collapse (i.e. a measurement takes place or one of the B mesons decays) the wave function is still antisymmetric. Thus, the entangled state $|\Psi_B\rangle$ is kept and the two B mesons can only oscillate orthogonally [14].

[4] If the two fermions in the B meson would couple to a spin 1 particle additional energy would be needed for a B^*.

2.1.6. Measurement of CP Violation

One way to perform a CP violation measurement is if particle and anti-particle end up in the same final state. A representation of this issue is depicted in figure 2.5a for B^0 and in figure 2.5b for $\overline{B}^0$, with the special case for $|f\rangle = |J/\Psi, K_S^0\rangle$. Not all contributing Feynman



(a) Decay of $B^0 \rightarrow J/\Psi, K_S^0$ via mixing and direct Feynman diagrams.

(b) Decay of $\overline{B}^0 \rightarrow J/\Psi, K_S^0$ via mixing and direct Feynman diagrams.

Figure 2.5.: Feynman diagrams for the decay of B^0 and $\overline{B}^0$ into the same final state J/Ψ and K_S^0.

diagrams for the same final state $|f\rangle$ are represented in figure 2.5. E.g. one of the oscillation (cf. figure 2.4) is missing.
Instead of decay amplitudes (equation 2.11 and 2.12) decay rates in the form of

$$\Gamma(B^0 \rightarrow f) = |\mathcal{A}_{CP}|^2 \tag{2.20}$$

$$\Gamma(\overline{B}^0 \rightarrow f) = |\overline{\mathcal{A}}_{CP}|^2 \tag{2.21}$$

are measured. Since these small numbers are hard to compare, the figure of merit is the asymmetry

$$a_{CP} = \frac{\Gamma(B^0 \rightarrow f) - \Gamma(\overline{B}^0 \rightarrow f)}{\Gamma(B^0 \rightarrow f) + \Gamma(\overline{B}^0 \rightarrow f)} \tag{2.22}$$

between the decay rates.

The short lifetime of B^0 mesons in the order of $\approx 1.5\ ps$ does not allow a direct time measurement between B^0 and $\overline{B}^0$. However, the asymmetric energy of the SuperKEKB accelerator (Low Energy Ring (LER) with 4 GeV and High Energy Ring (HER) with 7 GeV) leads to a boost of the system, enhancing the lifetimes of the particles by the Lorentz factor γ, creating a distance ΔL between the two decay times.

With the production of entangled initial states, cf. equation 2.17, flavor oscillation can be handled. Figure 2.6 shows the decay of an entangled $B\overline{B}$ state into J/Ψ and K^0_S. The semileptonic decay designates the *tagged* B-meson. At this time the flavor is fixed due to the charge of the lepton. The tagged B meson is either $B^0/\overline{B}^0$ and the other (*reconstructed*) B-meson is in the opposite state $\overline{B}^0/B^0$ and now free to oscillates on its own until it decays, too.

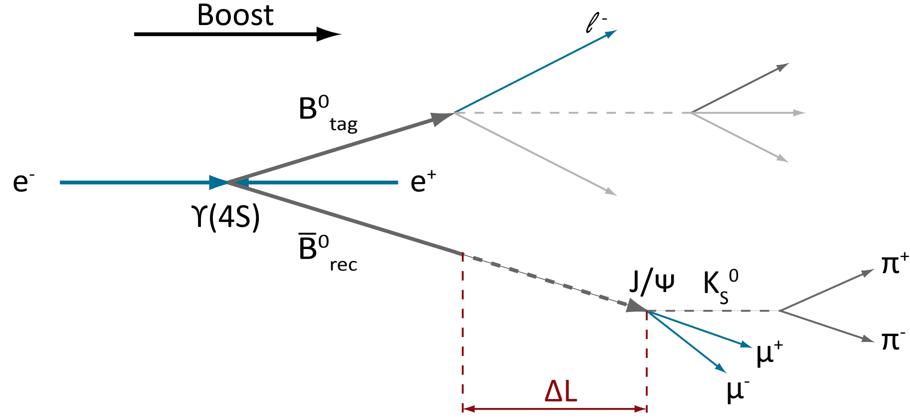


Figure 2.6.: Decay of $B^0\overline{B}^0$ into $J/\Psi K^0_S$. The charge of the lepton in the tag side is entangled to the charge of the reconstructed $\overline{B}^0$.

With a precise measurement of the two decay vertices, the distance of the decay ΔL is translated back into a lifetime difference $\Delta\tau$ between particle and anti-particle. In order to reconstruct such small differences and to study the effects of CP violation an enormous effort is put into the construction of dedicated accelerators and detectors. In fact a preciser measurement of spatial difference between the two vertices implies preciser information on the CKM -Matrix elements and therefore on CP violating effects.

2.2. Belle II Detector

The oscillation from B^0 into its antiparticle makes great demands on possible measurements, i.e. detectors with dedicated properties for this endeavor. The study of CP violation was amongst others conducted with the Belle experiment at the KEKB accelerator in Tsukuba, Japan. This experiment was concluded on June 30, 2010.
The Belle II detector is the new measuring device at the SuperKEKB accelerator. The asymmetric electron/positron collider will operate at an energy of 10.58 GeV[5] and is the successor of KEKB.
The main purpose of Belle II is the study of CP violation in the B system and it is based on the Belle detector. Since several machine parameters have changed for the upgrade of KEKB to SuperKEKB the new detector itself has to cope with new requirements. One crucial part is the increase in luminosity up to $\mathcal{L} = 8 \cdot 10^{35} cm^{-2}s^{-1}$. Besides an increase in available events, this will, amongst others, increase the occupancy, size of transferred data stream,

[5] Other energies are possible in order to operate at other resonances.

and radiation levels as well.
An illustration of the intended detector is shown in figure 2.7. In the subsequent sections the planned detector components are explained, based on [15]. Further reading can be found in [16, 17].

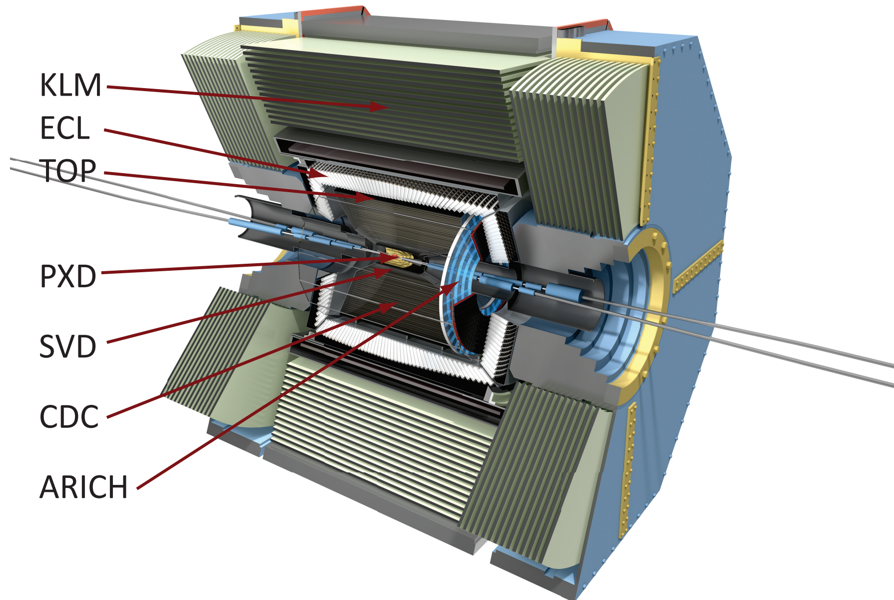


Figure 2.7.: Layout of the intended Belle II detector.

With the expected data set the uncertainties in the unitarity triangles can be reduced further, decay channels can be analyzed more precisely and, via higher order Feynman contributions, hints for new physics can manifest. An illustration of a sensitive process is given in figure 2.8. Calculations of the SM processes can be, dependent on the decay, very precise. Probing of such channels in experiments allows a comparison of the theoretical predictions and observed data. Discrepancies therein can be explained via processes which are beyond the SM, e.g. with supersymmetry (SUSY). Further reading can be found e.g. in [18, 19].

2.2.1. Pixel Detector (PXD)

The PXD is the detector which is closest to the interaction point. Its layout is described in detail in section 2.3. Besides tracking of "normal" hits, the PXD recognizes in addition the crossing of pions with low transverse momentum p_t. These particles with energies in the range of $40\ MeV \lesssim E_\pi \lesssim 75\ MeV$ deposit very high charge into the detector and are barely visible in the following subdetectors. In order to facilitate tagging (cf. section 2.1.6 for details) this data of the PXD can become useful.

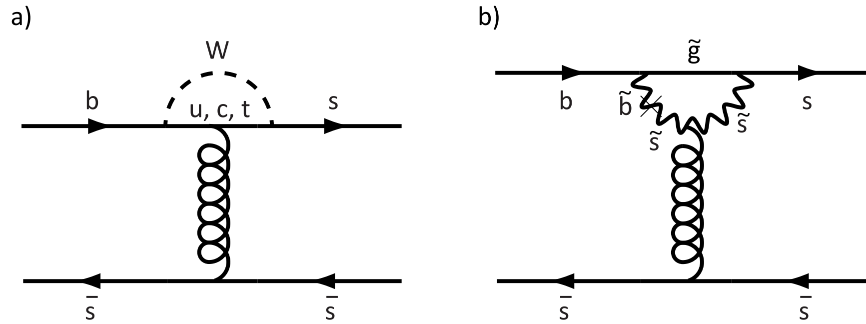


Figure 2.8.: Penguin diagrams in which new physics can manifest. A SM process is shown in a), while b) shows a contribution from a SUSY extension in which $\widetilde{b}$ and $\widetilde{s}$ squarks as well as gluinos ($\widetilde{g}$) participate (*after [19]*).

2.2.2. Silicon Vertex Detector (SVD)

The Silicon Vertex Detector (SVD) is composed of four layers of double-sided silicon strip detectors. Its main purpose is to measure the tracks of charged particles together with the PXD and the Central Drift Chamber (CDC) (see section 2.2.3) for the reconstruction of the two decay vertices of B-mesons. In this way the detectors work together very closely. Since the overall data amount of the PXD would be too large due to background, the CDC and SVD report extrapolations of their tracks to the PXD where so-called Regions of Interests (ROIs) are defined. Hits in such regions are to be read-out later, depending on trigger signals.
In addition, the combination of the two silicon based detectors leads to a so called Vertex Detector (VXD), since software considerations for tracking are in most cases applicable to both.

2.2.3. Central Drift Chamber (CDC)

Consisting of more than 14,000 wires the CDC plays a crucial role in the design of Belle II. In addition to its main purposes, i.e. the reconstruction of charged particle tracks and measurements of E/p, it also serves for particle identification via the energy loss in the gas mixture. In addition, the CDC can provide trigger signals for charged particles to which other subdetectors can react or participate in the analysis.
Most of the wires are arranged in z direction (axial) in order to measure the transverse momentum, whereas the other wires (stereo) are slightly tilted by an angle of $\sim \pm 50\ mrad$.[6] This provides information for the polar angle Θ of the tracks.

2.2.4. Particle Identification at End-Caps (ARICH)

For Particle Identification (PID) Cherenkov radiation is used. This radiation is emitted whenever the velocity of a charged particle v exceeds the velocity $c' = c/n$ of electromagnetic waves in a medium with refractive index n and speed of light c. The light is emitted in a

[6]angle depends on the layer

cone and the opening angle ($= 2\Theta_{ch}$) is dependent on the velocity:

$$\cos\Theta_{ch} = c'/v = 1/\beta n. \tag{2.23}$$

By reconstructing this angle and knowing the refractive index of the medium the momentum over mass can be extracted.
In Belle II this is realized in the end-caps via an aerogel, which serves as a radiator for the particles, coupled to Hybrid Avalanche Photo Detector (HAPD). This detector consists of a Photomultiplier Tube (PMT) with an Avalanche Photo Diode (APD) read-out. The aerogel itself is highly transparent so that photon loss inside the material is suppressed (scattering or absorption). The cone of the Cherenkov radiation is visible as an ellipsoid on the position detectors (formed by the PMTs and APDs) from which a reconstruction of the cone is possible. This setup forms the Aerogel Ring Image Cherenkov Detector (ARICH).
With this detector an identification of kaons and pions is possible. Differently from Belle, where only a binary read-out of the two particles took place, in Belle II the ARICH will have additional information (i.e. β) on the particle.

2.2.5. Particle Identification along the Barrel (PID, TOP)

The PID in $r\Phi$-direction also relies on the emittance of Cherenkov radiation. First, a radiator material converts the transition of a particle into Cherenkov light which itself is transported in the medium. The light in this radiator is reflected internally until it reaches the read-out nodes at the end. These consist of wavelength shifter and Micro Channel Plate (MCP)-PMTs. The fast data acquisition of $\sim 40\ ps$ for the MCP-PMTs is necessary since the arrival time of Cherenkov radiation due to pions is $\sim 100\ ps$ earlier than the light from the slower kaons [20]. The two particles can be discriminated via this time gap due to the different impinging angle of the particles. This forms the Time-of-Propagation (TOP) detector.

2.2.6. Electromagnetic Calorimeter (ECL)

The calorimeter in Belle II consists of thousands of CsI(Tl) crystals. Electrons and photons deposit nearly all their energy into these crystals via bremsstrahlung and pair production and create electromagnetic showers. On the other hand, heavier charged particles like muons and pions deposit only a fraction of their energy into the Electromagnetic Calorimeter (ECL). This feature, in combination with the E/p result from the CDC, is used to precisely identify electrons. The read-out of these crystals is done with PMTs.

2.2.7. Kaon and Muon Detection (KLM)

Further outside of the solenoid the Kaon and Muon Detector (more precisely: K_L^0, μ-Detector) (KLM) is located. It consists of a sandwich structure of iron plates in combination with Resistive Plate Chambers (RPC). Besides providing a return path for the magnetic field, the iron plates serve as interaction material for muons and K_L^0. The muon and the showers from K_L^0 exit the iron plates and traverse the RPCs. This detector is based on the principle of a plate capacitor with high voltage on each side and a gas mixture within. Whenever a particle from the shower traverses the plates it ionizes the gas atoms and the electric field accelerates the created electrons and ions. The electrons initiate more ionization and the electric field in this area breaks down since the charge from the two plates now

flows along the trajectory of the particle. This break-down is then picked up by sensor strips which are placed orthogonally on each side of the RPC, so that a location of this event is possible.
To distinguish between muons and K_L^0 one uses the fact that as a neutral particle the K_L^0 does not leave a track in the CDC, whereas the tracks from the CDC can be extrapolated to find possible muon hits in the KLM. In addition, the decay of K_L^0 leaves a broad shower contrary to the signal of muons.

2.3. The Pixel Detector (PXD)

With its asymmetric beam energies the SuperKEKB accelerator translates the difference in the decay time of B- and $\overline{B}$-mesons into a difference of the decay length via the boost of the system. The crossing angle of 83 $mrad$ of the beams and their energies lead to a relativistic velocity of

$$\beta = \frac{|\mathbf{p}_{CMS}| \cdot c}{E_{CMS}} = \frac{|\mathbf{p}_{e^+} + \mathbf{p}_{e^-}| \cdot c}{E_{CMS}} \approx \frac{3.03}{10.58} \approx 0.286, \tag{2.24}$$

and to a Lorentz factor of

$$\gamma = \frac{1}{\sqrt{1-\beta^2}} \approx 1.0438. \tag{2.25}$$

Thus the decay difference due to their lifetime τ is given by

$$\Delta L = \beta\gamma\tau c \approx 137\ \mu m \tag{2.26}$$

In order to reconstruct this difference in the decay vertices precise vertex reconstruction is needed.
Placing tracking detectors closer to the interaction point is a worthwhile goal for better reconstruction. Yet, the occupancy of the detectors increases drastically in this way. The use of pixel detectors is inevitable since standard strip detectors would suffer from their ambiguities. In addition strip detectors rely on the principle of a depleted diode for signal generation. This means, in order to increase the signal height thicker detectors would have to be used in addition with electronics for amplification, which would require additional cooling equipment. Such bulky detectors would lead to multiple scattering of particles crossing them, which would affect the information gained from detectors sitting further outside of the interaction point.
The DEPFET technology provides integrated amplification allowing a considerable reduction in absorber thickness. For the Belle II detector a thickness of 75 μm is envisaged which corresponds to an equivalent thickness of 0.21 of the radiation length X_0[7]. In addition, the DEPFET itself only dissipates power when switched on but is sensitive also in the off state. Thus only marginal power of 0.5 W per half module (only DEPFETs) has to be cooled away via air stream, allowing cooling equipment to be placed outside the acceptance region where most of the heat-generating Application-Specific Integrated Circuits (ASICs) sit.
A Computer-Aided Design (CAD) drawing of the PXD is shown in figure 2.9, the working principles of a DEPFET are described in section 3.4.

The PXD consists of two layers. Each of them is made of so-called half ladders. A schematic is depicted in figure 2.10. The thin silicon bulk (active area) of a half ladder

[7] including additional material like Application-Specific Integrated Circuits (ASICs), bump bonds, etc.

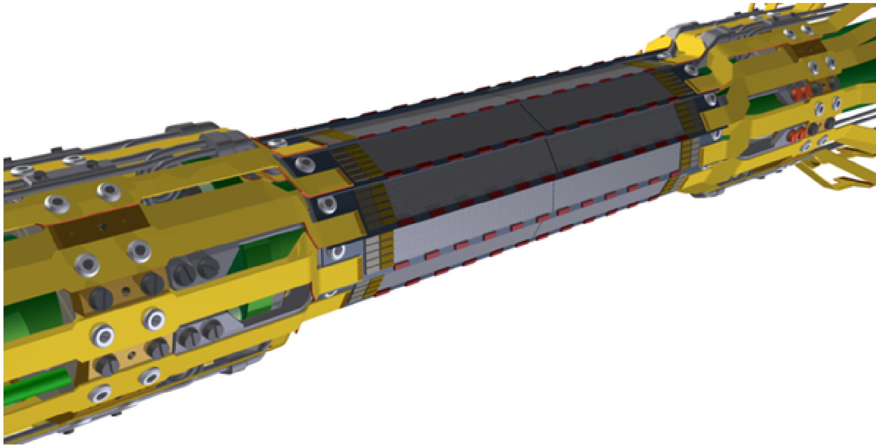


Figure 2.9.: Technical design drawing of the PXD with Kapton cables (yellow) attached. The detector is already mounted on the beam pipe (green) and only the outer layer is visible. *CAD drawing by K.-H. Ackermann.*

contains 768x250 DEPFET pixels. They are controlled by *Switchers* (see section 2.3.2), sitting on the thicker balconies of the modules.
At the end of each module (i.e. a half ladder), on thick silicon, the read-out ASICs are located. They consist of the Drain Current Digitizer (DCD) (cf. section 2.3.2), which samples the drain current and digitizes it, and the Data Handling Processor (DHP) (cf. section 2.3.2), which is mainly responsible for zero suppression.

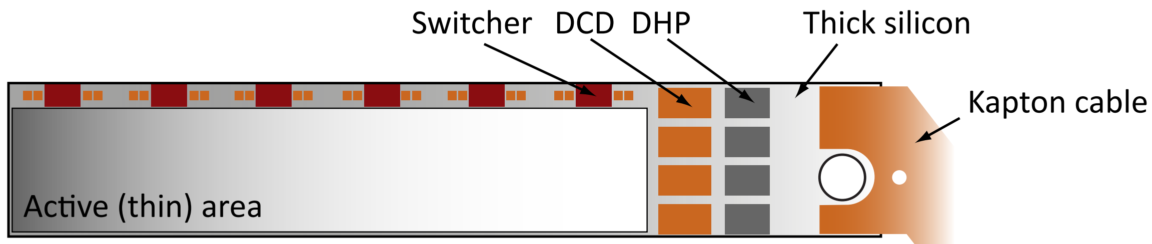


Figure 2.10.: Schematic of a half ladder (module) of the PXD. The Kapton cable is truncated in the drawing.

The PXD is placed close to the beam pipe, only 1.4 *cm* (2.2 *cm*) separates the inner (outer) layer from the interaction point. This will result in good vertexing but considerable radiation damage has to be taken into account. Chapter 4 is dedicated to the impact of radiation on semiconductor devices, while section 2.4 deals with the various radiation sources the PXD will have to face.

2.3.1. Layout

The PXD is organized in two layers surrounding the beam pipe. A short overview of its parameters is presented in table 2.1. Two of the abovementioned modules are glued together via ceramic inlays so that they form a complete ladder. Each half of them is read out at the

end of the active area (end-of-stave) located outside the acceptance region.

	Inner Layer	**Outer Layer**
# Ladders	8	12
Sens. Length	90 mm	123 mm
Radius	1.4 cm	2.2 cm
Appr. Pixel Size	50x50 μm^2	50x75 μm^2
# Pixels	1536(z) x 250($R - \Phi$)	1536(z) x 250($R - \Phi$)
Thickness	75 μm	75 μm
Frame/Row Rate	50 kHz/10 MHz	50 kHz/10 MHz

Table 2.1.: Properties of the PXD.

2.3.2. Electronics

Switcher

On each half ladder several switcher chips are mounted at the thick balconies. The task for them is twofold: First, to switch between the on- and the off-state of the DEPFET. This is performed via switching between two voltages for the DEPFET gate. Second, the Switcher performs a clear operation of the DEPFET also via switching between two voltages, thus a clear pulse is applied.
The mode of operation is realized in a rolling shutter mode for switching on rows of the DEPFET matrix. Due to the module design four rows are switched on and read out at the same time, while the rest of the DEPFET matrix is in the off state. The Switcher delivers fast voltage pulses up to a $\sim 20\ V$ difference between gate on/off (clear low/high). The short pulse of the clear is capacitively coupled to the clear gate, thus facilitating the clear process.

DCD

The DCD samples the drain current with the use of an 8-bit Analog-to-Digital Converter (ADC). In addition to the resolution of the ADC, a global current sink removes the constant part of the drain current from the DEPFETs. This makes it possible to max out the available ADC range for the signal. An individual 2-bit current source for each of the 256 channels is available to take static pedestal fluctuations of the current into account, which e.g. can originate from the device spread due to production or inhomogeneous irradiation (cf. section 10.2 for a more in-depth discussion of inhomogeneous irradiation and DCD properties).

DHP

Data handling of the digital domain is the task of the DHP. It is responsible for the correction of pedestal fluctuations and common mode noise. Additionally it reduces the amount of data via zero suppression of non-hit pixels/clusters and assigns time stamps to the event. Transmitting is done via kapton cables on a trigger request.
Moreover, the DHP handles slow control signals for the DCD and the Switchers.

2.4. Radiation Background at Belle II

The DEPFET gets irradiated during the operation of Belle II by various kinds of radiation. In the following the main components contributing to the background are pointed out and are reviewed closely. The estimation of radiation levels was done as a collaboration effort and is still under investigation. At the moment considerable inhomogeneous radiation along z is expected. Due to the fact that the simulations are still ongoing definite numbers cannot be stated. However, present simulation results indicate a similar situation to Belle. Section 10.2 will have a closer look on this issue.

2.4.1. Touschek Effect

The Touschek effect is a kind of intra beam scattering [21], but whereas normal scattering just leads to an diffusion of the beam profile, the Touschek effect is a single scattering event between the transverse momentum p_x of two particles and the longitudinal direction p_s (see picture 2.11).

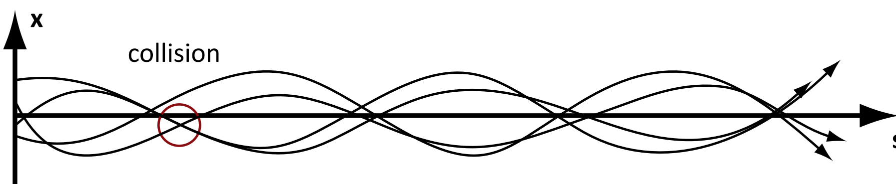


Figure 2.11.: Sketch of particles flowing along the beam line (after [22]). In one bunch a collision between two particles takes place.

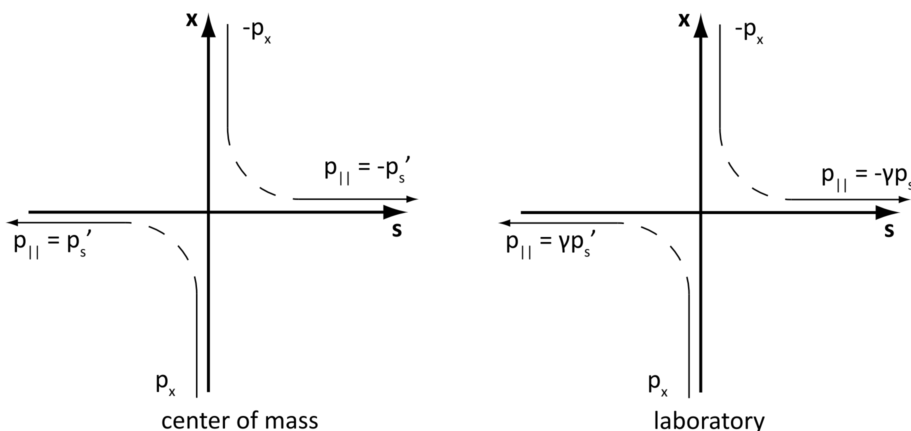


Figure 2.12.: Collision of two particles, left side in the rest frame, right side in the laboratory frame (after [22]). In general, after the collision the particles will have a momentum in both directions. In the laboratory frame the longitudinal momentum is enhanced by γ.

By Lorentz transformation after the scattering event one particle is enhanced by the relativistic factor γ and the other one is slowed down (see second picture 2.12). This leads to the loss of these two particles since such high momentum alterations cannot fit into the acceleration structure (cavities, focusing magnets, etc.) anymore. The loss rate of particles

is

$$R_{Touschek} \propto \frac{N}{E^3\sigma}, \tag{2.27}$$

where E is the energy, N the number of particles in a bunch and σ the beam size [23]. Since the LER exhibits a small beam energy of 4 GeV and nano beam optics will result in a small beam size with a high density of particles, the Touschek effect cannot be neglected in Belle II.
The loss happens everywhere along the beam line but especially near points where the bunch densities are increased and more scattering events are probable. Near the interaction region the scattered electrons or leptons contribute to the radiation background and, of course, can create fake events.

2.4.2. Four-Fermion Final State Radiation

The dominant background process is the four-fermion final state radiation. In this process, see e.g. figure 2.13 for one of the dominating diagrams, the crossing electrons and positrons both emit a photon, which leads in the end to a four-fermion final state. Since the mass of electrons is considerably lower than that of muons, the resulting final state will most likely consist of two electrons and two positrons. The background has a cross-section of $\mathcal{O}(10^7\ pb)$

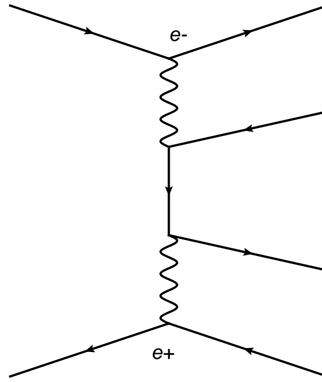


Figure 2.13.: Feynman diagram of the dominant four-fermion final state radiation.

and with increasing luminosity the background will increase as well.
The simulation of this background is found in detail in [24], whereas in this section only a brief summary will be stated. The energy distribution and dose estimates for the PXD are complicated due to the processes which take place after the Quantum electrodynamic (QED) generation of additional fermions. To estimate the impact of the process, the detector geometry (PXD as well as Belle II) has been simulated referring to a design as close as possible to the final one.
The energy distributions of electron/positron pairs hitting the PXD is determined by the QED process and the magnetic field of Belle II. In fact it can happen that particles cross the PXD multiple times (*curlers*) and deposit increasingly more energy into the semiconductor. Also, the magnetic field reduces the amount of particles for the second layer of the PXD, which then is less affected by this radiation background. The energy distribution of electrons/positrons reaching the PXD is shown in figure 2.14 and 2.15.
The simulation of the background was done using the Monte Carlo (MC) generators *KoralW*

[25] and *Berends, Daverveldt, Kleiss (BDK)* [26]. Both generators describe the physics very well at low energies, yet at higher energies BDK proved to be more accurate [27] and in accordance with measurements at Belle.
A short summary is given by table 2.2 for the two layers, with the timescale of a Snowmass year (smy) $= 10^7\ s$ at full luminosity $\mathcal{L} = 8 \cdot 10^{35} cm^{-2} s^{-1}$. In this way one smy corresponds to an integrated luminosity of 8 ab^{-1}.

Layer	Fluence $(e^+e^-/(smy\ cm^2))$	Fluence $(e^+e^-/(ab^{-1}\ cm^2))$	Avg. En. (MeV)
1	$4 \cdot 10^{13}$	$5 \cdot 10^{12}$	4
2	$2 \cdot 10^{13}$	$2.5 \cdot 10^{12}$	6

Table 2.2.: Electron/positron flux and energy from four-fermion final state radiation in the PXD, given for a smy at full luminosity.

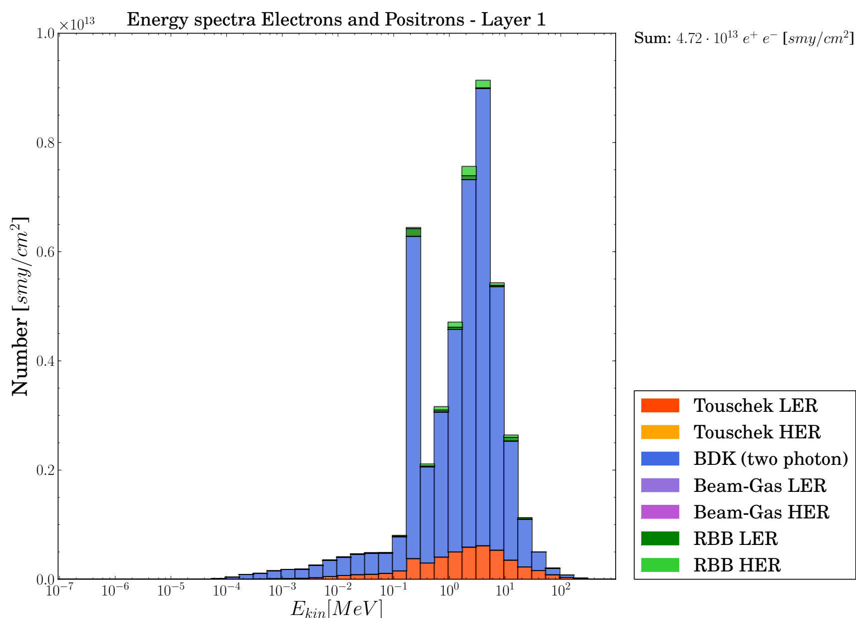


Figure 2.14.: Energy spectrum of electrons and positrons crossing the first layer of the PXD. The amount of four-fermion final state radiation is indicated by the item BDK (two photon) in blue. For comparison other background sources are listed as well. RBB contributes as well as Touschek from the LER, while the HER can be neglected. The mean energy for the first layer is $\approx 4\ MeV$. *Courtesy of Moll [24].*

2.4.3. Radiative Bhabha and Neutron Flux

Neutrons as source of radiation damage for the DEPFET/PXD originate from Radiative Bhabha (RBB) scattering near the interaction point. Losing energy in the beam does not only imply a loss of particles for the accelerator, but especially near the the detector a *backscattering* can take place. The scattered e^- (or e^+) can hit heavy materials (e.g. a

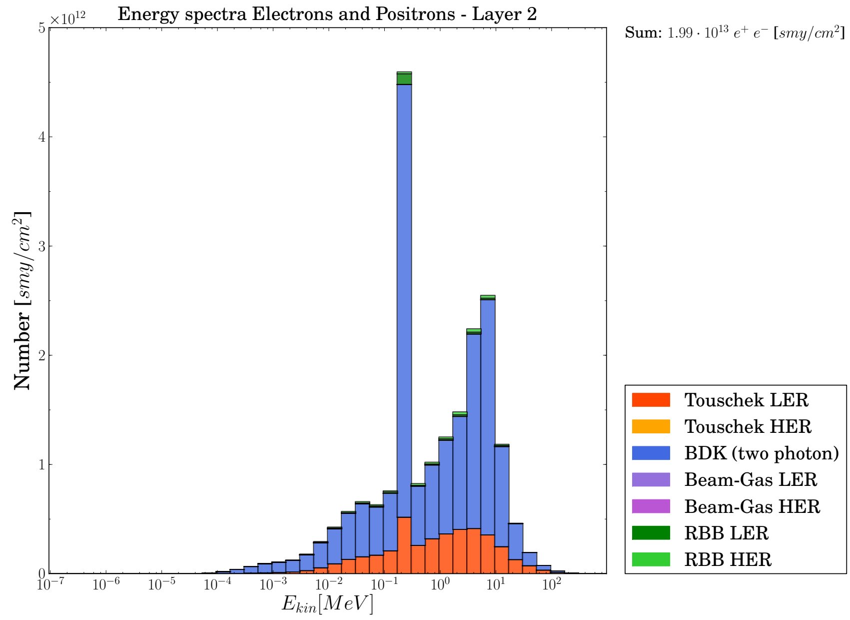


Figure 2.15.: Energy spectrum of electrons and positrons crossing the second layer of the PXD, with a mean energy of ≈ 6 MeV due to curlers. The amount of four-fermion final state radiation is indicated by the item BDK (two photon) in blue. For comparison other background sources are listed as well. RBB contributions, as well as Touschek contribute only to a small amount to the distribution. Beam-gas events can be neglected. *Courtesy of Moll [24]*.

quenching magnet) on its way downstream under a flat angle. From this scattering event a neutron shower is generated and some fraction of it is backscattered into the detector. Simulations of this process show only a small neutron fluence due to the flat angle for the PXD and the damage due to this source of background can be neglected [28].
In total a (pure) neutron fluence of $\Phi_n \approx 8 \cdot 10^{10}\ cm^{-2}smy^{-1}$, i.e. $\Phi_n \approx 10^{10}\ 1/(cm^2ab^{-1})$, for the PXD can be expected [29][8].

2.4.4. Synchrotron Radiation

Synchrotron Radiation (SR) is inevitable in a circular accelerator structure. However with the design of the Interaction Region (IR) the impact of SR can be minimized. At the moment simulations on this issue are ongoing and no final result has been presented yet. Current investigations show that only one module is affected by SR, whereas an average occupancy of 0.14 ± 0.02 % was found for the PXD [30].
This number has to be compared to the occupancy, which arises from the 4-fermion final state radiation of $\approx 0.8\%$ in the first layer. At present it is expected that SR will contribute to the radiation dose only with a marginal increase.

2.4.5. Summary

The various background processes affect the PXD in several ways. With the exception of pure neutrons traversing the detector, each other process will induce surface damage in the DEPFET (cf. section 4.2). Neutrons and especially the traversing electrons and positrons will affect the behavior of the DEPFET bulk (cf. section 4.1). Table 2.3 shows a summary of the expected radiation damage.

Background Type	Influence	Occ. L1	Occ. L2	Dose rate L1 kGy/ab^{-1}	Dose rate L2 kGy/ab^{-1}	Neutr. L1 $n/(ab^{-1}cm^2)$	Neutr. L2 $n/(ab^{-1}cm^2)$
Touschek (LER)	Surface/Bulk	0.10%	0.07%	0.25	0.125	-	-
4-Fermion	Surface/Bulk	0.80%	0.20%	2.25	0.5625	5.00E10	2.50E10
Rhad. Bha-Bha	(Surface)/Bulk	0.03%	0.01%	<0.125	<0.125	-	-
Synchrotron	Surface	0.40%	0.05%	-	-	-	-
Neutrons (all Sources)	Bulk	-	-	-	-	1.00E10	1.00E10

Table 2.3.: Overview of the influence of the various background radiation processes. Occupancy, dose rate and neutron levels are referred to layer 1 (L1) and layer 2 (L2) of the PXD.

[8] smy is referred to full luminosity

Chapter 3.

Semiconductor Physics and Devices

The radiation damage in Belle II will alter the characteristics of the DEPFET. Therefore this device is briefly explained which is followed by a more thorough discussion of the devices and physics on which the DEPFET is based upon.
The MOS interface is of basic importance since all surface damage effects induced by radiation manifest in this region. The simple yet powerful device is the Metal-Oxide-Semiconductor Capacitor (MOSCAP) whose working principle most of the devices in this study depend on.
The discussion is followed by a review of the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). This device is used in this work to study effects which will occur in the DEPFETs due to the radiation environment of Belle II. Subsequently the DEPFET and its properties are presented in more detail.
The chapter is closed with a discussion on Gate Controlled Diodes (GCDs), which are used as a diagnose device for the extraction of interface trap density.

3.1. Introduction to the DEPFET

The DEPFET was proposed by Kemmer and Lutz in [31] and a first working device was presented in [32]. Since the DEPFET is the sensor of choice for the PXD in Belle II, its properties are explained here shortly, while the device is revisited in section 3.4 for a closer look at its characteristics.
The working principle of a DEPFET is based on a MOSFET combined with a charge storage mechanism. Ionizing radiation generates electron-hole pairs (ehps) in the bulk of the DEPFET, illustrated in figure 3.1. The voltages, applied at the various contacts of the DEPFET, lead to a drift of those charge carriers. Holes are removed via the backside, whereas electrons drift to the charge storage. This charge storage is called *internal gate* and is realized by an additional n implantation below the channel of the topside MOSFET.
There the stored charge acts upon the current which is flowing in the transistor. By increasing this current from I_1 to I_2 they make a signal, which is proportional to the energy deposition of the ionizing radiation, visible. A clear mechanism takes care of removing those electrons from the internal gate. After removal the current value is back to its nominal value. A read-out is then usually done in the following way:

1. Sample drain current with some amount of charge in the internal gate I_2.
2. Remove stored charge via the clear process.
3. Sample drain current with empty internal gate I_1[1].

[1] In Belle II a slightly different read-out scheme is utilized. Pedestal currents are stored digitally and only a

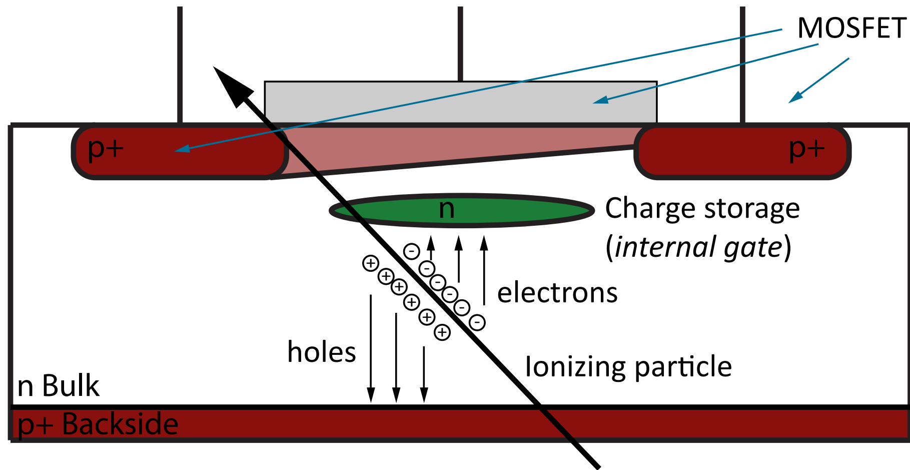


Figure 3.1.: Working principle (charge collection) of a DEPFET. An ionizing particle generates ehps, holes drift to the backside and electrons to the charge storage.

4. Calculate signal current $I_{sig} = I_2 - I_1$.

As aforementioned, the DEPFET is based upon a MOSFET structure. Thus, a closer look on this underlying device (section 3.3) together with the physics of the MOSCAP (section 3.2) is necessary.

3.2. Metal-Oxide-Semiconductor Capacitor

The MOS capacitor is a striking device for many applications concerning the qualification of semiconductor production processes. The simplicity of this device is the key to various kinds of analysis. All other MOS devices are based on its physics.
In this work its use as a device is restricted to the qualification of the insulating layer and modifications therein induced by radiation damage. Therefore a brief description of the working principle is given in this section, while experimental techniques are presented in section 6.1.1. A comprehensive discussion on both topics can be found in the work of Nicollian and Brews [33].

3.2.1. Design of a MOS Capacitor

In principle, the device can be considered as a plate capacitor. A schematic representation is given in figure 3.2. The device consists of a conducting plate which is called *gate* and is usually fabricated either with aluminum or doped polycrystalline silicon. The other electrode of the capacitor is the silicon bulk itself, which can be doped in various concentrations.
An insulating layer separates these two electrodes and due to the dielectric nature of the insulation, a plate capacitor is formed. Generally, this structure is known as a Metal-Insulator-Semiconductor (MIS) capacitor.
For the devices examined in this work, the insulating layer was made of silicon dioxide in

single sampling takes place.

combination with a thin layer of silicon nitride. For this double insulating layer the term *oxide* is used synonymously.

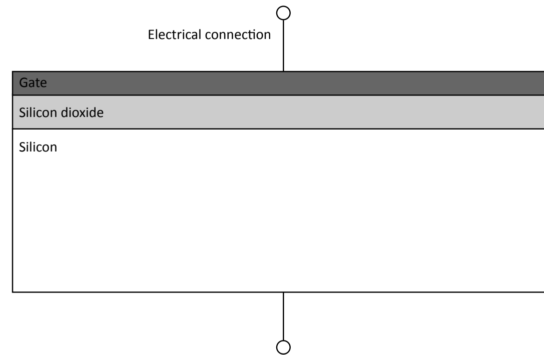


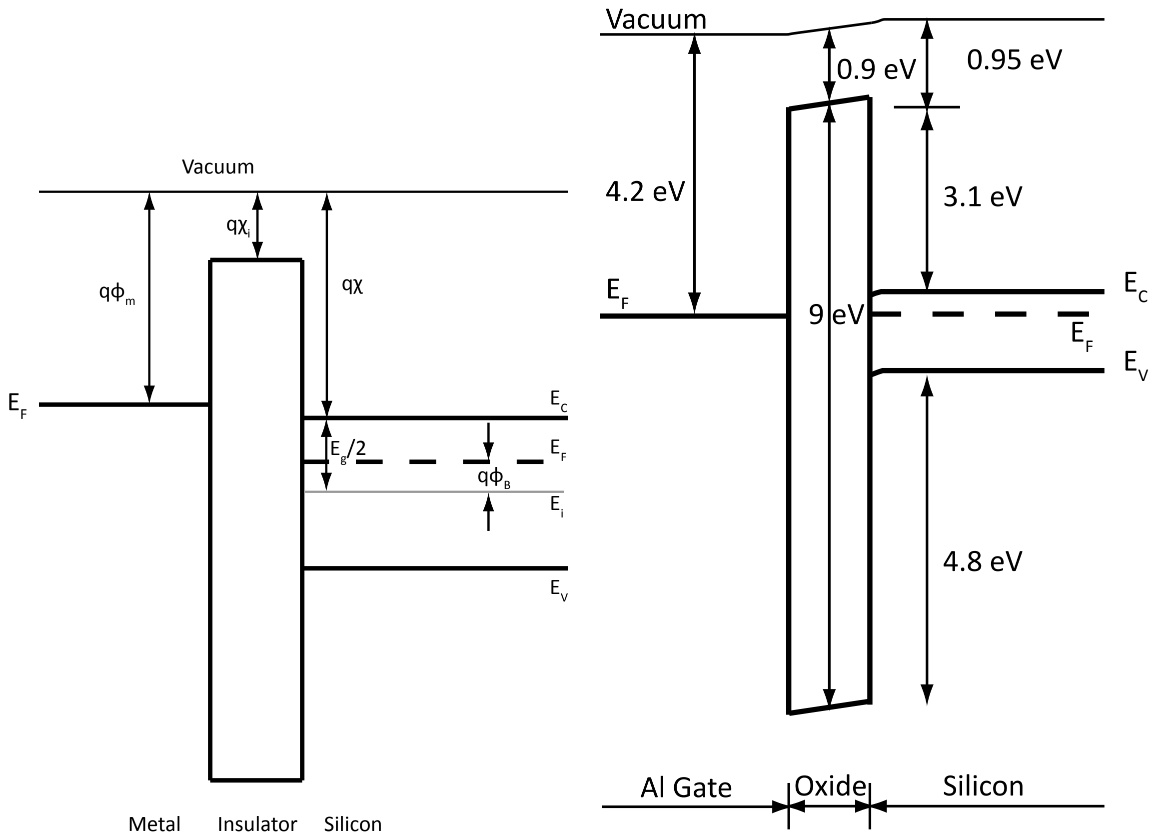
Figure 3.2.: Schematic illustration of a MOS capacitor. The insulation is realized by an SiO_2 layer. Often this is a two layer composition of SiO_2 and Si_3N_4. The gate area is large in comparison to that of a MOSFET, when used as a diagnose device.

3.2.2. Ideal MIS/MOS Capacitor

In figure 3.3a a basic energy band representation of a MIS system is given. As the insulator blocks the current flow, the Fermi potentials in the semiconductor and in the metal do not need to be the same.
DEPFETs are produced on an n-doped silicon bulk, therefore the following discussion is limited to this doping. Highly n-doped polysilicon exhibits similar characteristics as aluminum, thus the aluminum gate can be replaced with a polysilicon layer of appropriate doping. Polysilicon has certain advantages during production which makes it the preferred technology for transistor gates. However, contacts for bond wires or the routing on the chip are done in aluminum.
The use of polysilicon might result in slightly different band bending since the work function depends on the doping concentration. Band bending due to a metal gate, i.e. aluminum, can be seen in figure 3.3b, where the work function $q\Phi_{Al} = 4.2\ eV$ of aluminum causes this effect. Figure 3.3a shows an energy band representation in which work functions and electron affinity are perfectly aligned.

By applying a voltage to the gate contact (and setting the silicon as grounding), the charge carrier density at the interface silicon/insulator can be controlled. The amount of charge carriers depends on the doping of the silicon adjacent to the insulator. In the subsequent paragraphs an n-doping is assumed.
If the voltage is positive enough, electrons drift to the surface and accumulate there. This *accumulation* case can also be visualized in the band diagram, see e.g. figure 3.4a. The Fermi level remains constant, which results in a band bending of the surface edge of the conduction band and, due to the fixed bandgap, also of the valence band.

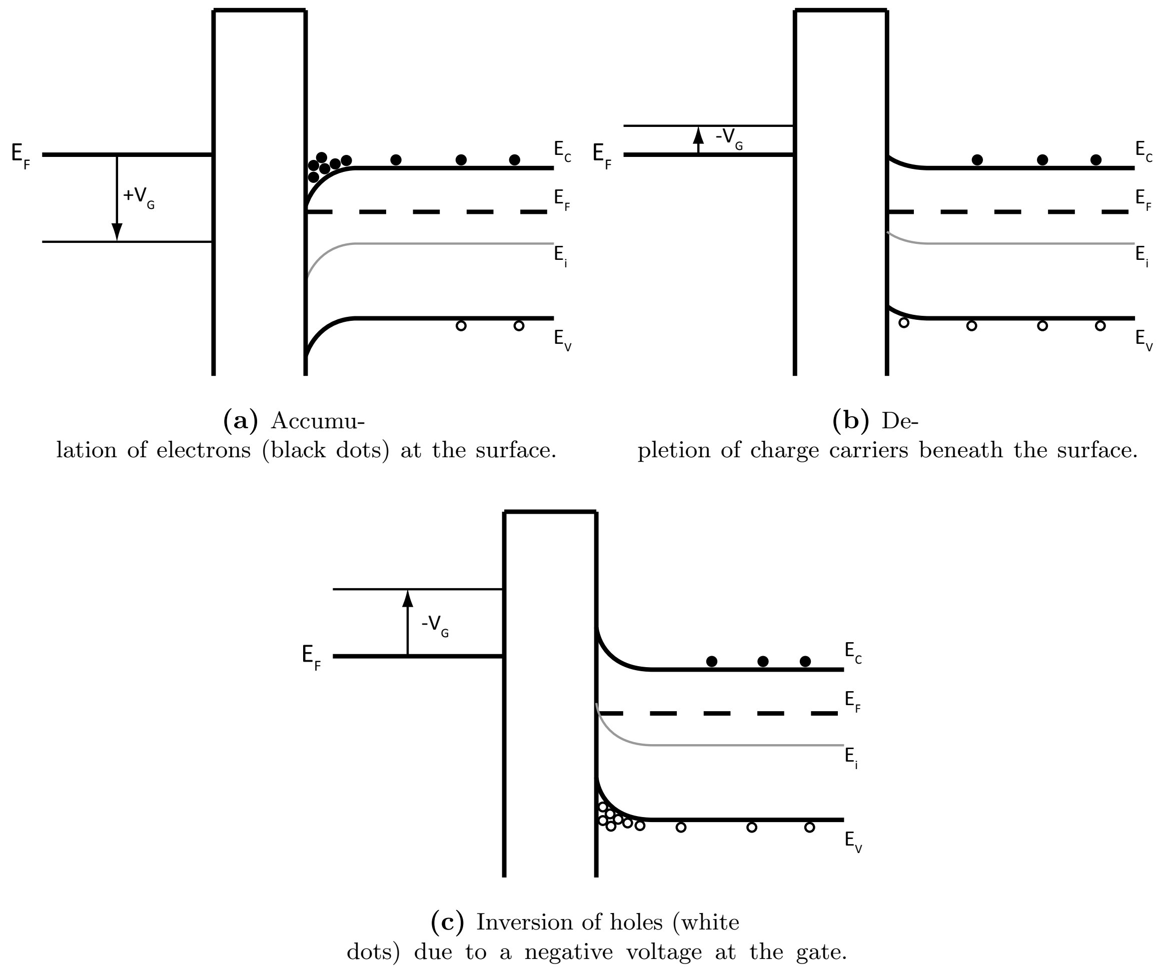
By reducing the gate voltage, a point where no band bending occurs and the charge density is given by normal doping relations can be reached. This is called the flat-band case.
When lowering the gate voltage further towards more negative values, the electric field repels the majority carriers from the surface but is still too positive to attract significant minority charge. The surface is now in *depletion* (figure 3.4b).



(a) Band diagram of an ideal MIS transition. The Fermi level in the metal does not coincide with the one in the semiconductor. A flat-band case is established by a perfect match of the electron affinity χ and the work function Φ.

(b) Band diagram of a typical MOS system. Due to the work-function of aluminum of 4.2 eV the Fermi levels are nearly the same and only little band bending occurs.

Figure 3.3.: Energy band diagrams of MIS/MOS systems.



(a) Accumulation of electrons (black dots) at the surface.

(b) Depletion of charge carriers beneath the surface.

(c) Inversion of holes (white dots) due to a negative voltage at the gate.

Figure 3.4.: Energy band diagrams for MOS capacitors in several states. A variable gate voltage V_G alters the band bending of the n-doped silicon.

Eventually, the voltage is negative enough to attract minority carriers. The surface is now *inverted* (3.4c) with holes.

3.2.3. Surface Space-Charge Region

Energy-Band Representation of a MOS Capacitor

As a consequence of the capacitive coupling from the silicon to the gate electrode, the band bending depends on the applied voltage. Having a closer look at the surface (figure 3.5), the band bending, which influences the electron and hole density, can be described with a potential

$$\Psi(x) = -\frac{E_i(x) - E_i(\infty)}{q}, \tag{3.1}$$

where q is the elementary charge and E_i is the intrinsic energy level ([34]). At the surface, this potential assumes the value $\Psi(0) = \Psi_S$.
The potential Φ in the system is defined as the distance to the Fermi potential E_F

$$q\Phi(x) = E_F - E_i(x), \tag{3.2}$$

where far away from the surface the bulk potential $\Phi(\infty) = \Phi_B$ is found. The bulk potential $\Phi_B > 0$ is given (with the Boltzmann constant k_B, the temperature T and the intrinsic carrier density n_i) by

$$\Phi_B = k_B T \ln\left(\frac{N_D}{n_i}\right) \tag{3.3}$$

and is located above the intrinsic level E_i for slightly n-doped wafers with doping concentration N_D.

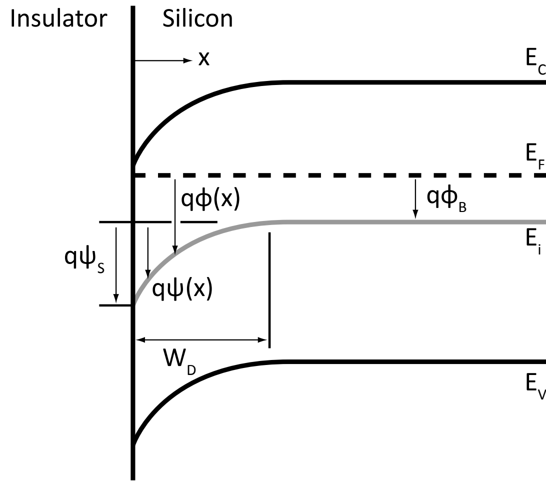


Figure 3.5.: Illustration of the energy levels of MOS capacitor. A positive voltage on the gate leads to an energy-band bending at the surface of Ψ_S. Farther away from the surface the potential $\Psi(x)$ reduces to zero. W_D denotes the maximum depletion width, when the surface potential is in the range $-\Phi_B < \Psi_S < 0$.

The sign convention from Nicollian and Brews [33] is used throughout this work. This means electron energy increases in the up direction, and an arrow in a band diagram pointing

up denotes negative potential.
With the help of Ψ, the cases given in figure 3.4 can be distinguished more clearly.
In accumulation, the bands are bent down, the arrow of Ψ also points in this direction, therefore:

1. $\Psi_S > 0$ accumulation.
2. $\Psi_S = 0$ flat-band condition.
3. $-\Phi_B < \Psi_S < 0$ depletion.
4. $-2\Phi_B < \Psi_S < -\Phi_B$ weak inversion.
5. $\Psi_S < -2\Phi_B$ strong inversion.

External Voltage and Gate Capacitance

When applying a voltage V_G to the gate contact, this voltage divides into two parts. The first one V_i appears over the sheet capacitance of the insulator C_i, whereas the second part is responsible for the band bending.

$$V_G = V_i + \Psi_S \tag{3.4}$$

with V_i determined by the electric field $\mathcal{E}_i$ and the thickness of the insulator d

$$V_i = \mathcal{E}_i d = \frac{|Q_S|d}{\epsilon_i} = \frac{|Q_S|}{C_i}, \tag{3.5}$$

where Q_S is the charge per unit area on the capacitor and $\epsilon_i(= \epsilon_r\epsilon_0)$ is the permittivity of the insulator, composed of the vacuum permittivity ϵ_0 and the material dependent relative permittivity ϵ_r.
Depending on the applied voltage, the counter electrode of the system may change. A way of understanding this effect is visualizing the capacitor as a series combination of two capacitors (see e.g. figure 3.6), where

$$C = \frac{C_i C_D}{C_i + C_D} \tag{3.6}$$

is the total sheet capacitance and C_D the voltage dependent depletion-layer capacitance.

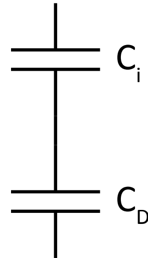


Figure 3.6.: Electrical representation of the MIS capacitor. The insulating capacitance C_i remains constant, where on the other hand C_D depends on the surface potential Ψ_S.

For the following discussion, especially for the extraction of interface trap properties, it is useful to define dimensionless potentials

$$u(x) = \frac{q\Phi(x)}{k_B T} \tag{3.7}$$

and

$$v(x) = \frac{q\Psi(x)}{k_B T}. \tag{3.8}$$

These quantities are defined analogously to the surface potential with $u(0) = u_s$ and $v(0) = v_s$ and $u(\infty) = u_B$ and $v(\infty) = 0$.
To find a proper analytical form for the voltage dependent capacitance of the system, it is necessary to look at the surface charge and its potential. The appropriate relation is Poisson's equation

$$\frac{d^2\Phi}{dx^2} = -\frac{\rho(x)}{\epsilon_{Si}}. \tag{3.9}$$

The charge distribution $\rho(x)$ in the silicon is given by all charge carriers

$$\rho(x) = q[N_D - N_A + p(x) - n(x)], \tag{3.10}$$

where $p(x)$ is the hole density and respectively $n(x)$ the electron density. N_D and N_A are donor and acceptor concentrations.
Applying the above constraints $\Phi(\infty) = \Phi_B \rightarrow \rho(\infty) = 0$ ensures charge neutrality at the end of the bulk. With the dimensionless potentials one finds

$$\frac{d^2u(x)}{dx^2} = \frac{1}{L_D^2}(\sinh u(x) - \sinh u_B), \tag{3.11}$$

where L_D is the Debye length

$$L_D = \sqrt{\frac{\epsilon_{Si} k_B T}{2q^2 n_i}}. \tag{3.12}$$

Solving equation 3.11 leads to a rather complicated electric field F_S at the surface. The derivation of the field is given in many textbooks on semiconductor physics (e.g. in [33] or [34]). The charge at the surface Q_S is then given by Gauss' law

$$Q_S = \epsilon_{Si} F_S. \tag{3.13}$$

The behavior of the charge in the MOS capacitor due to an external voltage (Direct Current (DC) and Alternating Current (AC)) and therefore the differential capacitance of the system is elucidated in detail in section 6.1.1 where measuring techniques for MOS capacitors are discussed.

Depletion-Layer Capacitance

For the purpose of determining the electric field in the insulator during depletion the following considerations are useful. In case of depletion, and also for weak inversion, the surface potential is in the range of $-2\Phi_B < \Psi_S < 0$. This leads to an easier term for the space-charge density (e.g. see [34])

$$Q_S \approx \sqrt{2\epsilon_{Si} q N_D \Psi_S} = qW_D N_D, \tag{3.14}$$

in which W_D represents the depletion width. In this case, the width as a function of applied voltage V is given by

$$W_D = \sqrt{\frac{\epsilon_{Si}^2}{C_i^2} + \frac{2\epsilon_{Si}V}{qN_D}} - \frac{\epsilon_{Si}}{C_i}. \tag{3.15}$$

The depletion capacitance C_D can then be estimated by using the plate capacitor model again, thus

$$C_D = \sqrt{\frac{\epsilon_{Si}qN_D}{2\Psi_S}} = \frac{\epsilon_{Si}}{W_D}. \tag{3.16}$$

3.3. Metal-Oxide-Semiconductor Field Effect Transistor

3.3.1. Introduction

The current-voltage characteristic of a MOSFET relies on the plate capacitor model discussed in section 3.2. Figure 3.7 shows a cross-section through a MOSFET.

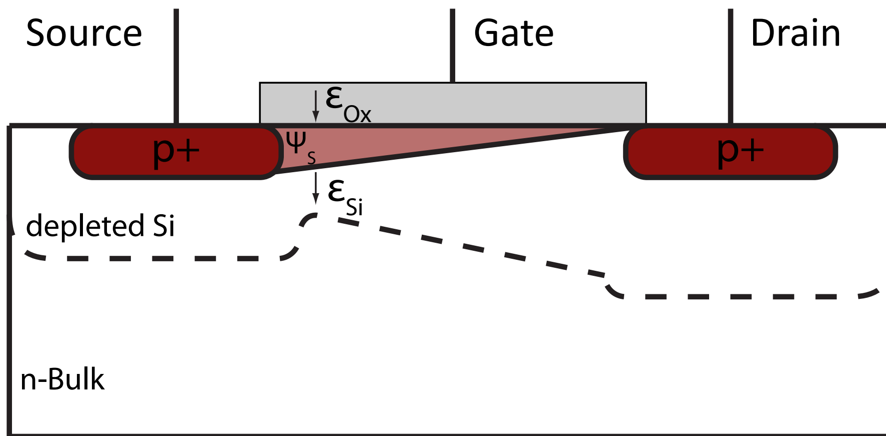


Figure 3.7.: Cross-section along the channel of a MOSFET. Depicted are the main contacts (drain, source and gate) as well as the depleted region if a channel is established, the electric fields $\mathcal{E}$ and the surface potential Ψ_S.

The gate voltage sets the surface beneath the insulator into the previously discussed charge cases:

1. accumulation.
2. depletion.
3. inversion.

The discussion in this section is limited to MOSFETs with an n-doped bulk and p-doped drain and source. However, with the appropriate changes in electric charge and potentials the characteristics for opposite MOSFETs can be derived. In addition, instead of a general sheet capacitance C_i, a more specific insulator, silicon dioxide, with its sheet capacitance C_{ox} is used.

During accumulation the transistor is in the off-state and currents are blocked by a *pn*-junction either at the drain or at the source side. At the transition between depletion and inversion a marginal current flows in this subthreshold region, see section 3.3.5 for details. At inversion, a conducting channel of holes enables a current flow from source to drain.

3.3.2. Current-Voltage Characteristic

In this section the current-voltage characteristic of the MOSFET is presented. Information on the physics of the MOSFET can be found e.g. in [34] and many other textbooks. The presented derivation follows [35].

The surface charge density in the channel Q_C is given according to the charge-sheet model by the electric fields $\mathcal{E}_{Ox}$ and $\mathcal{E}_{Si}$,

$$\mathcal{E}_{ox}\epsilon_{ox} = \mathcal{E}_{Si}\epsilon_{Si} - Q_C. \tag{3.17}$$

The fields depend on the applied gate potential V_G, the bulk voltage V_{Bulk} and the flat-band voltage V_{FB} (in which different work-functions Φ_{ms} and initial oxide charges are incorporated), as well as the doping concentration N_D. Equation 3.17 can be solved via

$$\begin{aligned} Q_C &= \mathcal{E}_{Si}\epsilon_{Si} - \mathcal{E}_{ox}\epsilon_{ox} && (3.18)\\ &= \left[\frac{-qN_D}{\epsilon_{Si}} d_{Si}\epsilon_{Si}\right] - [(V_G - V_{FB} - \Psi_s)/d_{ox}\epsilon_{ox}] && (3.19)\\ &= [-qN_D d_{Si}] - [(V_G - V_{FB} - \Psi_s)C_{ox}] && (3.20)\\ &= -[\sqrt{2qN_D\epsilon_{Si}(V_{Bulk} - \Psi_s)} + (V_G - V_{FB} - \Psi_s)C_{ox}]. && (3.21) \end{aligned}$$

In equation 3.21 the depletion depth d_{Si} in silicon is used (cf. also equation 3.38 for a depletion width originating from an abrupt *pn* junction).
A voltage V_D at the drain enables a current flow, but introduces an additional electric field $\mathcal{E}(y)$, which is orthogonal to the field in the gate (direction x), in the channel. Figure 3.8 illustrates this issue. Due to the lateral electric field the surface potential depends on the position in the channel, becoming

$$\Psi_s(y) = V_C(y) - 2\Phi_B, \tag{3.22}$$

in which V_C is the channel potential. At the source side ($y = 0$) the potential is zero and at the end of the channel it assumes the drain voltage value, thus

$$\begin{aligned} V_C(0) &= 0 && (3.23)\\ V_C(L) &= V_D. && (3.24) \end{aligned}$$

The current flowing from source to drain I_{DS} in a MOSFET of gate length L and gate width W is given by

$$\begin{aligned} I_{DS} &= -v(y)Q_C(y)W && (3.25)\\ &= -\mu_p\mathcal{E}(y)Q_C(y)W && (3.26)\\ &= -\mu_p W\frac{dV_C}{dy} \cdot [\sqrt{2qN_D\epsilon_{Si}(V_{Bulk} - V_C(y) + 2\Phi_B)} && (3.27)\\ &+ (V_G - V_{FB} - V_C(y) + 2\Phi_B)C_{ox}]. \end{aligned}$$

Hereby the drift velocity $v(y)$ depends on the electric field according to

$$v(y) = \mu_p \mathcal{E}(y), \tag{3.28}$$

in which a constant hole mobility μ_p is assumed.

The continuity equation enforces a constant current with respect to y, thus the relation

$$I_{DS} = \frac{1}{L} \int_0^L I_{DS}\, dy \tag{3.29}$$

holds true. Equation 3.29 leads then to a current of

$$I_{DS} = \frac{W}{L}\mu_p \int_0^{V_D} [\sqrt{2qN_D\epsilon_{Si}(V_{Bulk} - V_C + 2\Phi_B)} \tag{3.30}$$

$$+ (V_G - V_{FB} - V_C + 2\Phi_B)C_{ox}]dV_C$$

$$= -\frac{W}{L}\mu_p C_{ox}\{\left(V_G - V_{FB} + 2\Phi_B - \frac{V_D}{2}\right) V_D \tag{3.31}$$

$$- 2/3\frac{\sqrt{2qN_D\epsilon_{Si}}}{C_{ox}}\left[(V_{Bulk} - V_D + 2\Phi_B)^{3/2} - (V_{Bulk} + 2\Phi_B)^{3/2}\right]\}.$$

By decreasing the drain voltage, more and more charge of the bulk is depleted at the drain side, leading to a pinch-off point at the channel (cf. figure 3.8). A further decrease of V_D beyond the establishing of the pinch-off leads to a spatial shift of the pinch-off towards the source side. The channel length is hereby reduced to L', but I_{DS} becomes independent of V_D in this saturation region.

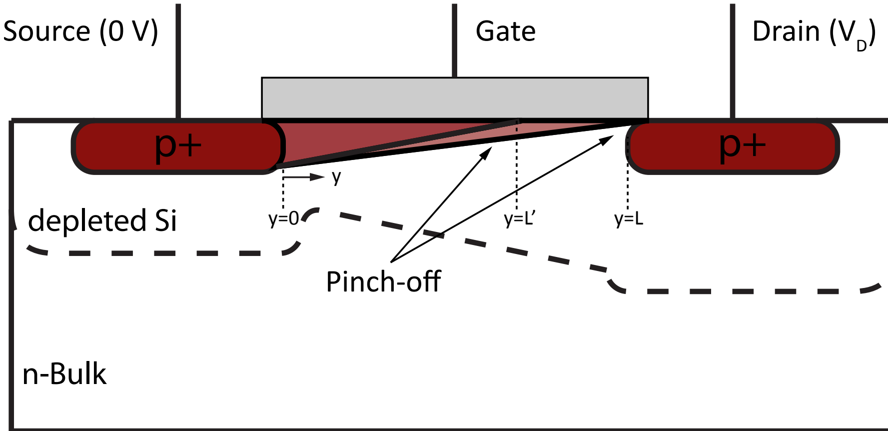


Figure 3.8.: Illustration of a MOSFET with V_D at saturation, thus a pinch-off at the drain occurs. Decreasing V_D further leads to a spatial shift of the pinch-off and depletes the region near the drain deeper.

The pinch-off condition at this location is equivalent to $\Psi_s = V_D - 2\Phi_B$ and "zero" channel charge, $Q_C = 0$. Thus, with equation 3.21 the saturating drain voltage is given by

$$V_{D_{sat}} = V_G - V_{FB} + 2\Phi_B$$

$$+ \frac{qN_D\epsilon_{Si}}{C_{ox}^2}\left[1 + \sqrt{1 + 2\frac{C_{ox}^2}{qN_D\epsilon_{Si}}(V_{Bulk} - V_G + V_{FB})}\right]. \tag{3.32}$$

The discussion of I_{DS} with respect to a change in V_D is continued in section 3.3.4. Another aspect of the channel behavior, i.e the threshold voltage, shall be discussed previously.

3.3.3. Threshold Voltage

An important quantity is the threshold voltage V_{th} at which the transistor starts to form a channel. Setting the surface potential in equation 3.21 to $\Psi_S = -2\Phi_B$ (onset of strong inversion) and the surface charge density in the channel to $Q_C = 0$ leads to

$$V_{th} = V_{FB} - 2\Phi_B + \frac{1}{C_{ox}}\sqrt{2qN_D\epsilon_{Si}(V_{Bulk} + 2\Phi_B)}. \tag{3.33}$$

To find the proper current flowing from source to drain, equation 3.32 is inserted into equation 3.31, leading to

$$I_{D_{sat}} = I_D(V_{D_{sat}}) = -\frac{W}{L}\mu_p C_{ox}\frac{V_{D_{sat}}^2}{2}, \tag{3.34}$$

with a saturation voltage for the drain

$$V_{D_{sat}} = V_G - V_{th}. \tag{3.35}$$

Hereby, the bulk voltage effects were absorbed into the threshold voltage.

By plotting a $\sqrt{I_{D_{sat}}}(V_G)$ curve, the threshold voltage can easily be extracted via a fit to the now linear slope, where the intersection with the voltage axis is V_{th} [36].

A major effect of ionizing radiation in MOS devices is the shift of the threshold voltage towards negative values (cf. section 4.2 for more details). This is due to the fact that positive charge is accumulated in the SiO_2 close to the channel. The external gate voltage has to overcome this charge and depending on the amount of charge Q_{ox} and the oxide capacitance C_{ox} the shift in voltage is given by[2]

$$\Delta V_{th} = \frac{Q_{ox}}{C_{ox}}. \tag{3.36}$$

This is one of the crucial radiation damage issues the DEPFET will have to face in the Belle II experiment. Shifts due to the accumulated charge can be measured not only with a MOSFET. MOSCAPs also detect the shift as a change in the flat-band voltage V_{FB}. Also, GCDs work as measuring devices because the additional charge manifests as a shift in the onset of depletion (see section 3.5 for more details).
Further remarks, experiments and results on the issue of oxide trapped charge Q_{ox} are presented in chapter 7.

3.3.4. Output Characteristics

The output characteristics of a MOSFET indicate the relation between the drain voltage V_D and the drain-source current I_{DS}. A typical behavior is illustrated in figure 3.9.

In the linear mode only a moderate voltage is applied at the drain contact; in this thesis in most cases $V_D = -0.5\ V$. From a small voltage at the gate an inversion layer of holes is

[2] Here the influence of interface traps and oxide trap distribution in the insulator is neglected.

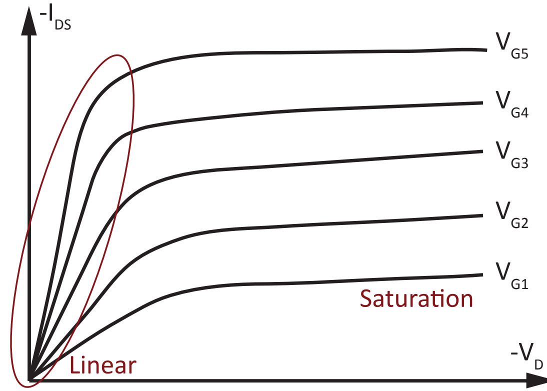


Figure 3.9.: Sketched output characteristics of a MOSFET. The linear region describes the fast increase of the drain-source current I_{DS} at low drain voltages V_D, while the saturation describes the flat region at higher drain voltages. Ideally, in saturation I_{DS} should not depend on V_D.

formed. The resulting channel acts as an resistor for the drain-source voltage, which is then, due to Ohm's law, visible as the linear increase in the output characteristics.
If the amount of the drain voltage is decreased further, charge carriers are depleted near the drain region (cf. figure 3.8). Eventually when the charge is near zero a pinch-off of the channel occurs. This is also visible in the output characteristics as an end of the transition region (sometimes also called *nonlinear region*).
An increase of $|V_D|$ further results in a fixed drain-source current, thus *saturation* is reached. The pinch-off point moves towards the source end of the channel, ensuring the fixed I_{DS}. However, as the effective channel length is shortened hereby a small influence of V_D to I_{DS} remains. This behavior may become important when considering short channel effects such as Drain-Induced Barrier Lowering (DIBL) (cf. section 3.3.5).

3.3.5. Subthreshold Region

Exponential Behavior of Drain Current

Below the threshold of a transistor, the interface is in depletion or in weak inversion. Figure 3.10 shows a cross-section through the source-gate-drain region in thermal equilibrium; the Fermi potential is steady. A small barrier for holes φ flowing from source to drain is induced at the source.
If now a voltage is applied to the drain (and the gate potential is still negligibly small, figure 3.11), the potential at the drain end is lowered for holes, but they still need to overcome the barrier φ at the source.
This leads to an exponential behavior of the drain current, as it is shown e.g. by [37] and [34],

$$I_D \approx \frac{W\mu_p}{L\beta^2} \cdot c \cdot e^{\beta\Psi_s}, \tag{3.37}$$

with the factor $\beta = \frac{q}{k_B T}$. The quantity c is given by dopings and charge concentrations. A gate voltage will have a direct impact on barrier height, since it influences the surface

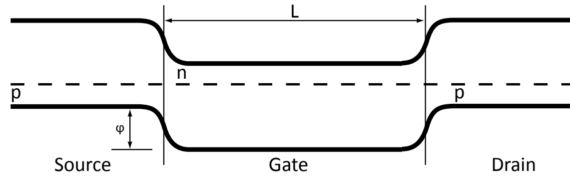


Figure 3.10.: Band diagram of the source-gate-drain (*p*-*n*-*p*) region in thermal equilibrium.

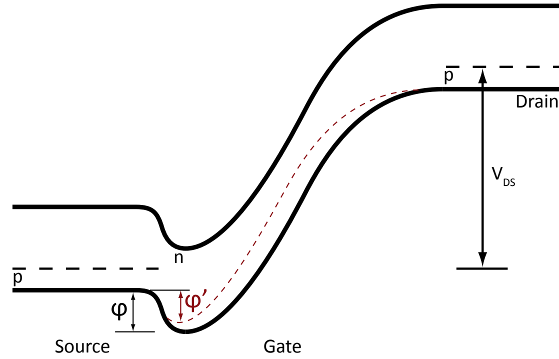


Figure 3.11.: Negative voltage applied at the drain. Once holes have overcome the induced barrier φ at the source they drift to the drain. A voltage at the gate controls this subthreshold current additionally by lowering/increasing the barrier φ at the source. A strong negative voltage V_D may influence the barrier height additionally, thus reducing it to φ'.

potential Ψ_s.

Drain-Induced Barrier Lowering

If the gate length L of the MOSFET is short enough, the potential at the drain end can influence the barrier height φ and reduce it to φ' (see e.g. figure 3.11). Lowering the barrier increases the flow of charge carriers from the source, therefore even in saturation the drain current depends on the drain voltage V_D. This short-channel effect is known as Drain-Induced Barrier Lowering (DIBL). The smaller the gate length L, the more influence the drain voltage exhibits. When increasing the amount of drain voltage further, the two depletion regions from source and drain may connect and a punch-through is established (cf. section 3.4.3).

3.4. DEPFET

The DEPFET is a unique device for radiation detection since it combines the amplification properties of a MOSFET with the charge collection efficiency of a fully depleted bulk. Due to the fact that the sensor itself exhibits an inherent amplification (cf. section 3.4.3), the absorption/detection material, i.e. silicon, can be made very thin. In the PXD the DEPFET is only 75 μm thick.
The charge collection mode via the depleted bulk can be done in an off state of the transistor,

thus leading only to a marginal power dissipation of the device. The bulk depletion is realized via a sidewards depletion and explained in the following section 3.4.1.

3.4.1. Sidewards Depletion

Having a device with two *pn*-junctions on both sides and a bulk contact, it it possible to deplete the bulk from each junction separately. The junction depth d_{Dio} of a single diode with an abrupt doping profile (in which the dopant concentration of acceptors N_A and donors N_D is simplified with $N_A >> N_D$) is given by

$$d_{Dio} = \sqrt{\frac{2\epsilon_{Si}}{qN_D}(V_{bi} + V_{rev})}, \tag{3.38}$$

in which V_{bi} is the built-in voltage of a diode of the order of $\sim 0.5\ V$ and V_{rev} the reverse biasing potential applied to the diode.
When depleting from both sides, the total bulk thickness can be depleted with a lower (total) voltage than with just one junction. This concept of sidewards depletion was first introduced by Gatti and Rehak [38] in 1984 and is essential for the DEPFET. The concept of sidewards depletion in a DEPFET is illustrated (idealized) in figure 3.12.

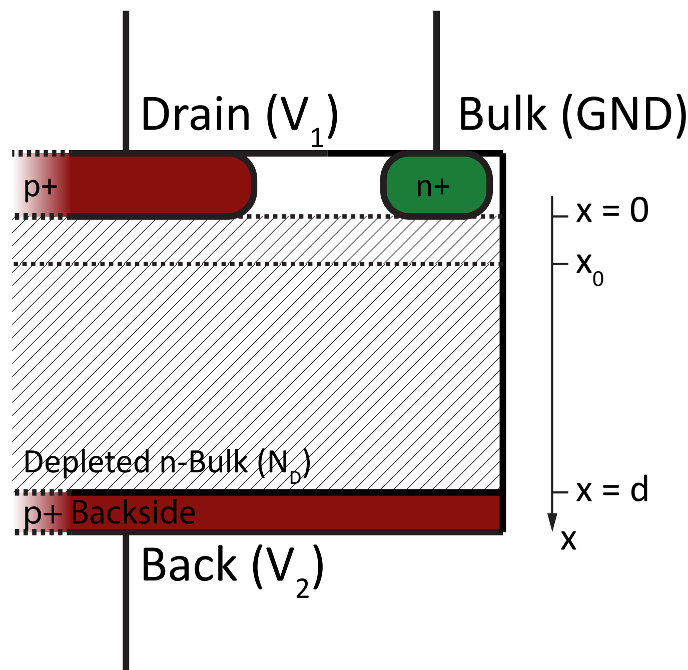


Figure 3.12.: Idealized sidewards depletion in a DEPFET. The bulk is depleted via the topside *p*+ regions, i.e. drain/source, and the backside *p*+ implantation. The bulk is set as grounding in this example, while it is set to a positive voltage in a real DEPFET.

The shape of the depleted potential is given by Poisson's equation

$$\Delta\Phi = -\frac{\rho(\mathbf{x})}{\epsilon_{Si}}. \tag{3.39}$$

Following the one-dimensional approach of the MOS capacitor leads to equation

$$\frac{d^2\Phi}{dx^2} = -\frac{qN_D}{\epsilon_{Si}}, \tag{3.40}$$

in which N_D is the doping concentration of the depleted bulk. Boundary conditions are set by

$$\Phi(0) = V_1 \tag{3.41}$$
$$\Phi(d) = V_2 \tag{3.42}$$

where V_1 and V_2 are the voltages at the top and back side.
With the given boundaries a common solution is found by

$$\Phi(x) = -\frac{1}{2}\frac{qN_D}{\epsilon_{Si}} \cdot x^2 + \left(\frac{V_2 - V_1}{d} + \frac{1}{2}\frac{qN_D}{\epsilon_{Si}}d\right) \cdot x + V_1. \tag{3.43}$$

An illustration of the potential is shown in figure 3.13.

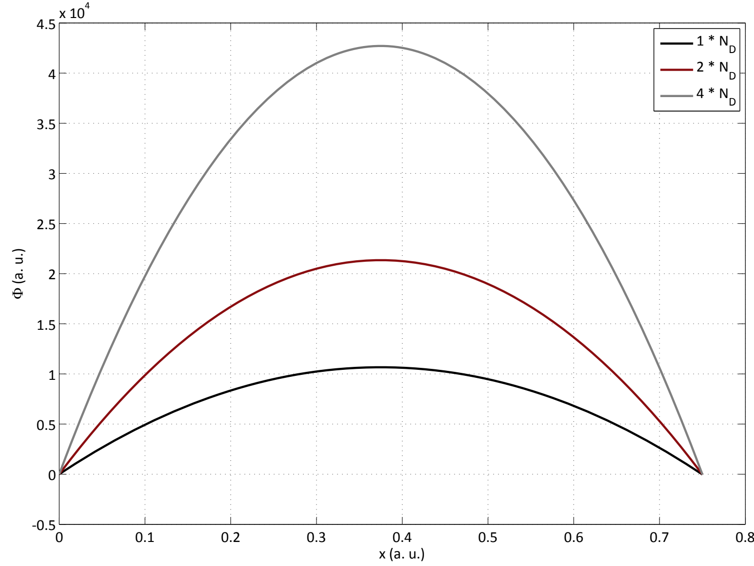


Figure 3.13.: Sidewards depletion potential with three different bulk dopings N_D. The voltages V_1 and V_2 determine end-points, while N_D controls curvature and potential depth (cf. equation 3.43).

The potential minimum given by $\frac{d}{dx}\Phi(x) = 0$, is located at

$$x_0 = \frac{d}{2} + \frac{\epsilon_{Si}}{qN_D}\frac{V_1 - V_2}{d}. \tag{3.44}$$

Together with the bulk doping the location of minimum can be shifted via the control voltages. In the DEPFET a sufficiently negative backside biasing in combination with an additional doping below the channel forms this minimum for electrons.

3.4.2. Working Principle

The concept of sidewards depletion in combination with an additional n implantation below the gate of a MOSFET creates the aforementioned charge storage in section 3.1. This space charge region (scr) acts upon the holes in the channel similar to the gate of the MOSFET, thus justifying the name *internal gate*. Since the charge has to be removed from the internal gate during operation, the removing *clear* region has to be placed close by. Figure 3.14 shows a cross-section through a DEPFET pixel cell. Orthogonally to the channel region (source-gate-drain) the clear and the surrounding *clear gate* are shown.

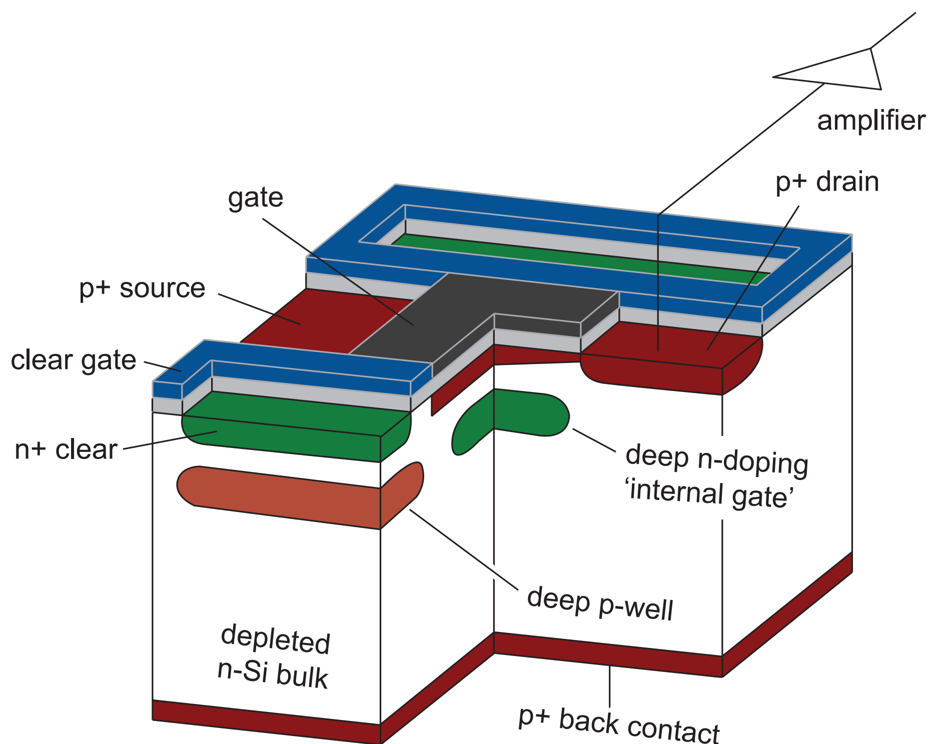


Figure 3.14.: Schematic illustration of a typical DEPFET pixel cell.

The clear exhibits a $n+$ doping concentration which would make it even more attractive for electrons than the internal gate, but a p-implantation shields the clear in order to hinder signal electrons from drifting to the $n+$ clear contact instead of the internal gate. The clear gate in combination with this deep p implantation forms a barrier consisting roughly of $n_{int.gate}/n_{bulk} - p_{shield} - n_{clear}$, similar to the one shown in figure 3.10. The height of the barrier can be controlled with the potential on the clear gate.
By applying a sufficiently positive voltage to the clear, a punch-through to the internal gate is established and the charge therein removed. The layout of the device facilitates the clear process by capacitively coupling the clear gate to the clear contact, thus temporarily lowering the barrier for the stored electrons.

3.4.3. Current-Voltage Characteristic of a DEPFET

DEPFET Equations

One of the key features of the DEPFET is its integrated amplification via the internal gate. From this scr to neighboring contacts like drain, source and channel a capacitive coupling is present. Lying close to the channel, the induced charge Q_{ind} therein, being opposite in sign to the signal charge Q_{sig}, is given by a fraction f of it, thus ([35])

$$Q_{ind} = fQ_{sig}. \tag{3.45}$$

This effect is similar to a change in the external gate voltage by $\Delta V = fQ_{sig}/C_G$, with the gate-channel capacitance

$$C_G = WLC_{ox}. \tag{3.46}$$

The drain current from equation 3.34 is altered with a new saturation voltage for the drain

$$V_{D_{sat}} = \frac{fQ_{sig}}{C_G} + V_G - V_{th}. \tag{3.47}$$

Important parameters for the DEPFET are the overall transconductance g_m and the charge amplification of the internal gate g_q, given by

$$g_{m_{sat}} = \frac{\partial I_{D_{sat}}}{\partial V_G} = -\frac{W}{L}\mu_p C_{ox} V_{D_{sat}} = \sqrt{\frac{2W\mu_p C_{ox}}{L} \cdot (-I_{D_{sat}})} \tag{3.48}$$

$$g_{q_{sat}} = \frac{\partial I_{D_{sat}}}{\partial Q_{sig}} = -\frac{W}{L}\mu_p f \frac{C_{ox}}{C_G} V_{D_{sat}} = f\sqrt{\frac{2\mu_p}{WL^3 C_{ox}} \cdot (-I_{D_{sat}})}. \tag{3.49}$$

From these two equations, a simple relationship for g_q can be concluded

$$g_q = g_m \frac{f}{C_G}. \tag{3.50}$$

Design decisions for DEPFETs are partly based on the important equation 3.49. Reducing oxide thickness to improve radiation hardness (cf. section 4.2) results in a loss of g_q as the oxide capacitance is increased. One way to increase the charge amplification is to reduce the channel length L, thus compensating the loss caused by thinner oxides.

DEPFET Backside Biasing

In a device with two *pn*-junctions like a bipolar transistor or a DEPFET, it may happen that the depletion regions of the two junctions begin to touch each other. When applying high enough negative voltages on the *p*-sides of a *pnp* device, each junction starts to grow and eventually they touch each other leading to a potential *punch-through* through the structure. As in the case of field emission, the charge carriers have to overcome a barrier. The situation is similar to the subthreshold region of a MOSFET (cf. section 3.3.5), where holes drift to the drain contact once they have overcome the barrier height φ.

In order to establish a drift field in the bulk of the DEPFET a sufficiently negative potential on the backside has to be applied. Since the backside is on the thinned silicon part of the

module with only 75 μm thickness and therefore very brittle, applying a bond wire would be a risky operation. In addition, for such an application a metalization of the backside would be needed.
Instead the DEPFET technology uses the punch-through effect. A $p+$ contact is placed at the surface (figure 5.8), outside the DEPFET region. A sufficiently high negative voltage (e.g. $-60\ V$) is applied at the top side and punches through the bulk reaching the back side. There the overall $p+$ backside implantation forms a conductive layer from which the depletion of the remaining bulk originates. Further information can be found e.g. in [39].

DEPFET Read-Out

The DEPFETs are organized in the way of a matrix. The Switcher (section 2.3.2) switches clear and gate voltages. Table 3.1 shows more details about these voltages.

Notation	Typical value (V)	Description
V_{Clear}^{on}	14...18	Used for charge removing
V_{Clear}^{off}	4	Used during charge collection
V_{Gate}^{off}	2	Used during charge collection
V_{Gate}^{on}	-5...-3	Used during read-out and clear process

Table 3.1.: Voltages applied at the DEPFET matrix via Switchers. The detailed voltage depends on the layout of the DEPFET.

The read-out works in a rolling shutter mode due to the Switcher. Hereby one row is enabled and the drain current of that row is transported parallelly (columns) to the DCD where the current is *sampled*. After that, a *clear* process takes place. In Belle II the next row is enabled and the process starts again. This sample-clear process is called *single sampling* since the subtraction of stored baseline currents is performed in the digital domain of the PXD.
Usually, when time is not of the essence a second sampling for the baseline current is performed after the clear. The resulting sample-clear-sample process (cf. section 3.1) is called Correlated Double Sampling (CDS).

3.5. Gate Controlled Diode

A GCD is used to investigate the quality of the Si/SiO_2 interface. It is built in such a way that it measures the current which is generated from interface traps (cf. section 4.2.1). Such a "current" is also generated in the DEPFET beneath the clear gate as it is operated in depletion. Since nearly all electrons present in the bulk of the DEPFET will drift to the internal gate, the surface generated electrons and their noise will also be observed in addition to a signal charge.
Therefore GCDs offer a relatively fast and easy way to determine this quality. However, a disadvantage of this device and its measuring procedure is that, unlike in MOS capacitors (cf. section 3.2 and section 6.1), the interface trap distribution as a function of energy in the bandgap cannot be extracted.

3.5.1. Layout

GCDs fabricated in the Halbleiterlabor der Max-Planck-Gesellschaft (HLL) exist in several configurations, but they all are based on the following design scheme:
On the slightly *n*-doped wafer a boron implantation is made in such a way that the *p*-doped region (denoted as *p+*) has the form of a tree (e.g. see figure 3.15 and figure 3.17, where the branches are depicted). There is a gate structure between the branches of the *p*-region. Gate and *p+* are in the middle of the device. The gate controls the MOS interface from inversion to accumulation. The *p+* contact is kept at a fix reverse potential, measuring the total current flowing through the device.
The whole device is surrounded by an additional diode, the *p+ outer ring*. The negative voltage on this contact inhibits leakage current originating from the outside of the gate area or from the rest of the Device Under Test (DUT), see e.g. figure 7.3.
This is combined with a guard ring, which is set to accumulation so that interface traps are saturated under this MOS contact. This way it is ensured that the measured contents are effectively reduced to the region defined by the inner diode and the gate structure.
A typical layout of a gate controlled diode can be seen in figure 3.15.

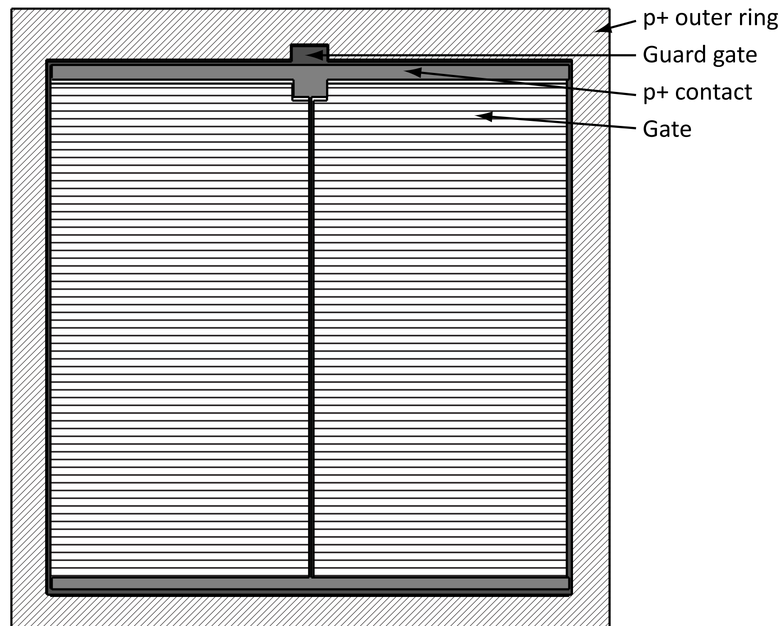


Figure 3.15.: Schematic layout of a typical gate controlled diode at the HLL. The gates are realized as horizontal ribbons in the middle. The *p+* contact runs from the top bar along a vertical one until it widens at the bottom again, contact is done by a bond wire to the top nose. Guard gate surrounds the GCD and *p+* outer ring shields the device from outside leakage currents.

There are several types of gate controlled diodes on the wafers for the Thin-Oxide (TO) Project. One characteristic is the structure of the polysilicon layer. It comes in two varieties, a fine ribbed version with a bar and gap thickness of 6 μm and a thicker version with width of 93 μm and a gap of 7 μm. However, for the calculation of the gate area, it is necessary to take the effect of under etching and under diffusion into account. This leads to a size

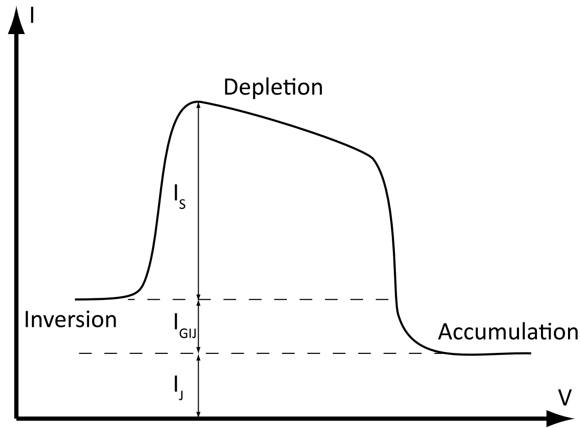


Figure 3.16.: Typical current of a gate controlled diode. The gate voltage controls the situation of the interface (accumulation, depletion, inversion).

reduction of 0.75 μm at each polysilicon edge.
The important gate area and other parameters are listed in table 3.2 and table D.1.

Type	$p+$ strip width (μm)	Gate strip width (μm)	Gate area (cm^2)	Gate area (corr.) (cm^2)
Fine	6	6	$4.589 \cdot 10^{-2}$	$4.055 \cdot 10^{-2}$
Coarse	7	93	$8.128 \cdot 10^{-2}$	$8.055 \cdot 10^{-2}$

Table 3.2.: Design properties of GCDs.

3.5.2. Mode of Operation

The internal $p+$ strips are constantly biased in reverse mode (with a positive bulk potential V_{Bulk}), therefore they collect all the charge generated in the scr.

Accumulation

Beginning with figure 3.17, the MOS contact is biased into accumulation, hereby attracting electrons from the bulk, which passivate interface traps. The measured current in the diode is just the basic current generated in the junction I_J (equation 3.56). The origin of this current is the thermal generation of charge carriers in the scr of the diode. To prevent light-induced generation the DUT has to be kept in the dark during measuring time.
The scr extends only due to the reverse bias voltage and the built-in potential V_{bi}. The width is given by equation 3.58. A trend of the current (from accumulation to inversion) is depicted in figure 3.16.

Depletion

The voltage on the gate strips is operated into depletion (figure 3.18). Formerly attracted electrons are now forced away from the interface. This results in unpassivated interface

traps, which now become generation active. The surface generated current I_S contributes to the normal current I_J in addition to the wider (induced) scr, generating I_{GIJ}.
The surface current I_S is given by

$$I_S = qGA_G, \tag{3.51}$$

with the surface generation rate per area G and the area under the gate A_G.
When assuming a homogeneous distribution of interface traps throughout the forbidden bandgap, the surface generation rate can be calculated via ([40, p. 804])

$$\begin{aligned} G &= \sigma_n \sigma_p v_{th} D_{it} n_i \int \frac{dE_{it}}{\sigma_n \exp(\frac{E_{it}-E_i}{k_B T}) + \sigma_p \exp(-\frac{E_{it}-E_i}{k_B T})} && (3.52) \\ &= \sigma v_{th} \pi k_B T D_{it} n_i && (3.53) \\ &= s_g n_i, && (3.54) \end{aligned}$$

where $\sigma = \frac{1}{2}\sqrt{\sigma_n \sigma_p}$ is an effective capture cross-section of the capture cross-sections σ_n, σ_p for electrons and holes and D_{it} is the average interface trap density. Besides the intrinsic charge carrier density n_i the thermionic velocity v_{th} also impacts on the capture probability. With the surface generation velocity

$$s_g = \sigma v_{th} \pi k_B T D_{it} \tag{3.55}$$

equation 3.54 can be written in shorter way.
By measuring the surface generated current I_S, the important figure of merit s_g can be deduced, which is sufficient to evaluate the quality of the interface. However, to compare the results gained from GCDs with those from MOS capacitors and MOSFETs, the interface trap distribution D_{it} has to be calculated. Section 6.3.1 deals with the arising problem of the effective capture cross-section.

Inversion

Changing the gate voltage further, the inversion case is reached (figure 3.19). The attracted holes passivate the generation active interface traps, thus inhibiting I_S. Only the sum of the junction current I_J and the gate induced junction current I_{GIJ} can be measured.

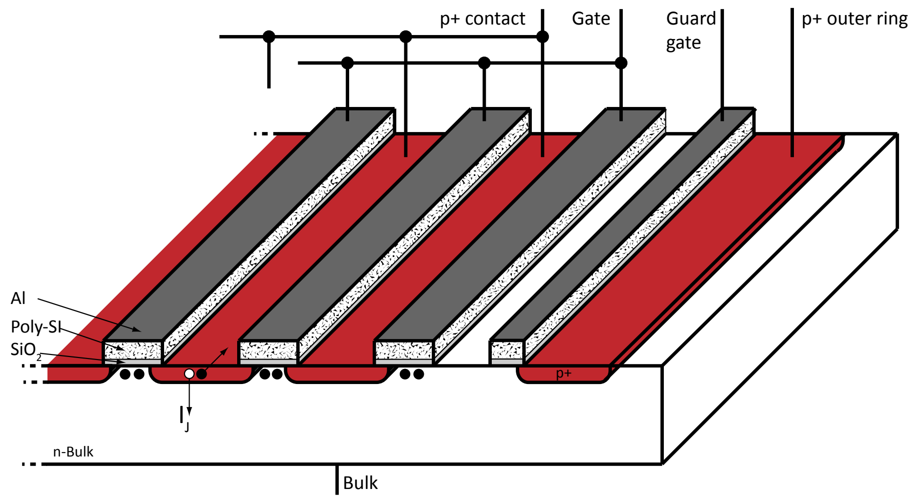


Figure 3.17.: Gate controlled diode in accumulation. A positive voltage on the gate ensures passivation of interface traps by electrons (black dots). The measured current at the $p+$-contact is I_J originating from the pn-junction.

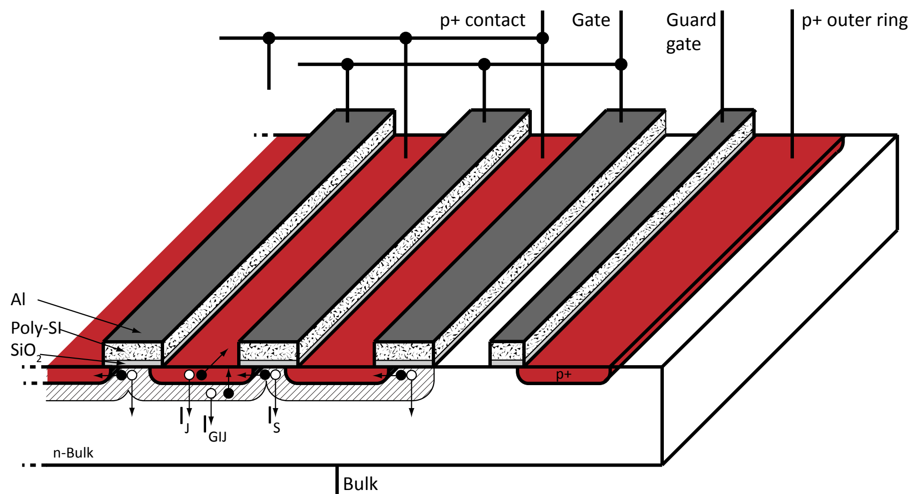


Figure 3.18.: Gate controlled diode in depletion. The junction of the pn-transition widens resulting in an increased gate induced current I_{GIJ}. In addition, as the surface is depleted from charge carriers, it becomes generation active, increasing the current by I_S.

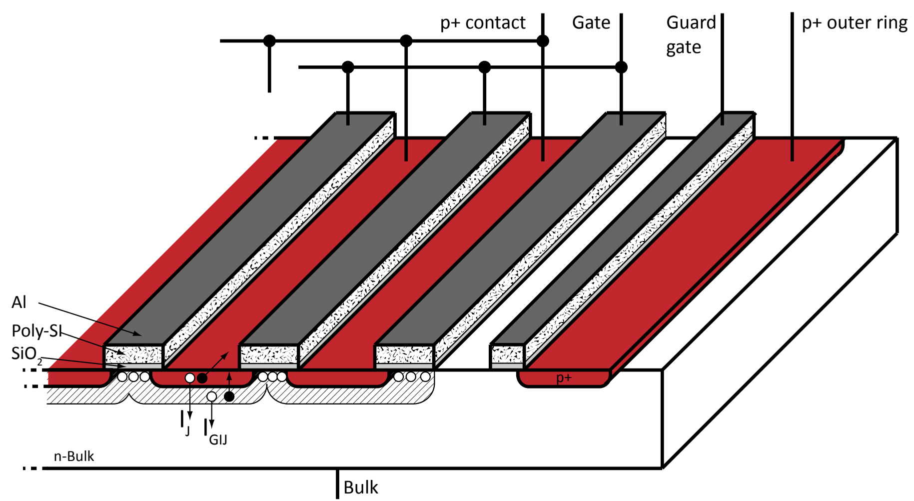


Figure 3.19.: Gate controlled diode in inversion. The surface is passivated by holes, interface traps do not contribute to the measured current. However, the negative potential keeps the widened junction, thus I_{GIJ} still contributes.

Basic Equations

Since the intrinsic level is taken as a zero reference, the equations given by [41] can easily be adapted by switching acceptor type with donor type. There are three important currents for a gate controlled diode, one of them is the abovementioned I_S for the surface current during depletion (equation 3.51).
From the junction generated current

$$I_J = \frac{qn_i W_J A_J}{\tau_{g,J}} \tag{3.56}$$

and the gate induced current

$$I_{GIJ} = \frac{qn_i W_G A_G}{\tau_{g,G}} \tag{3.57}$$

two quantities can be extracted. One is the lifetime in the bulk, given by $\tau_{g,J}$, the other the lifetime in the gate region $\tau_{g,G}$.
The various widths can either be measured or calculated, using

$$W_{G,inv} = \sqrt{\frac{2\epsilon_{Si}(V_{Bulk} + 2\Phi_B)}{qN_D}} \tag{3.58}$$

and

$$W_J = \sqrt{\frac{2\epsilon_{Si}(V_{Bulk} + V_{bi})}{qN_D}}. \tag{3.59}$$

N_D is the doping concentration in the bulk and in equation 3.58 $\Psi_S = 2\Phi_B$ (equation 3.3) is used, as it is typical for strong inversion.

3.6. Fabrication and Processing

This section provides a brief review over important aspects of the fabrication of the gate insulator. In order to produce a DEPFET more than 90 process steps are necessary, thus a detailed explanation would be beyond the scope of this thesis.
A large part of the radiation damage from which the DEPFET is affected has its origin and location in this insulating layer. It consists of a moderately thick layer of silicon dioxide on top of the silicon followed by a thin layer of silicon nitride.

3.6.1. Silicon Dioxide

Silicon dioxide in semiconductor technology is typically used as an insulator. The insulator is grown on top of the wafer silicon. An appealing picture of silicon dioxide is given in [34], which explains the chemical constitution of silicon dioxide in the following (ideal) way. On a single-crystal of silicon (the wafer) exists a thin layer (approximate thickness of one atom layer) of non-stoichiometric silicon dioxide, followed by strained layer SiO_2 and then the remaining strain-free amorphous SiO_2.
SiO_2 can be grown in a thermal oxidation process at elevated temperatures. The two main processes are described below, whereas matters of radiation hardness of the two can be found in section 4.2.4.

Dry Oxidation

The wafer is put into a clean furnace (i.e. a quartz tube). While heating up to $\sim 1050\ °C$ the silicon reacts with the oxygen of the forming gas (a mixture of nitrogen and oxygen) in the following way

$$Si + O_2 \rightarrow SiO_2. \tag{3.60}$$

Typically, the interface Si/SiO_2 of such a dry oxidation has a very good quality. Due to the very high temperatures the SiO_2 is stoichiometric and possesses a high density ([42]).

Wet Oxidation

In this process, steam is passed into the quartz tube and the following reaction takes place

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2. \tag{3.61}$$

Usually, this process is referred to as *wet* oxidation. It can be processed at lower temperatures, e.g. at $\sim 950\ °C$ and the oxidation is faster than in the dry case.

3.6.2. Silicon Nitride

Properties

Silicon nitride Si_3N_4 is a chemical compound which is used in semiconductor industries for several reasons:

1. It is a very good diffusion barrier against contaminations such as sodium ions and it can block even hydrogen.

2. A deep (or buried) barrier for oxygen can be formed. During fabrication of semiconductor devices, an oxidation of a polysilicon layer may be desired. While the oxidation at the surface takes place, oxygen atoms may diffuse through the polysilicon and an undesired oxidation process happens in the polysilicon. This diffusion process is inhibited by a nitride layer.

3. It acts as an etch mask during fabrication of semiconductor devices. Etchants can act against the common used SiO_2 but do not react with Si_3N_4.

4. It smooths out rough surfaces, which are common when e.g. using polysilicon. Silicon nitride exhibits a conformal deposition, i.e. the reaction rate is determined by the offered surface. In this way, dangerously high electric fields, which may lead to isolation breakdowns, are reduced.

5. It has an influence on radiation hardness (see section 7.1.3 for details).

Considering technological aspects such as diffusion or etching masks, clearly, a moderate thick nitride layer is favored. However, as Si_3N_4 exhibits a large dielectric constant of 7.4 (vs. 3.9 of SiO_2) and the capacitance of the insulation layer affects device performance and radiation hardness, a compromise has to be found. In addition, even though Si_3N_4 acts as a good etch mask, it is hard to remove such layers in the fabrication process. Thus a thick nitride layer has also its disadvantages.

Nitride Deposition

Silicon nitride can be deposited by a wide variety of methods. A common method, and used for the devices in this work, is Low-Pressure Chemical Vapor Deposition (LPCVD). At elevated temperatures of $700\ ^\circ C - 800\ ^\circ C$ dichlorosilane and ammonia lead to a deposition of Si_3N_4 on the wafer by ([43])

$$3SiH_2Cl_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2. \tag{3.62}$$

3.6.3. Interface Trap Annealing

Quite often a silicon atom at the interface Si/SiO_2 does not find suitable binding partners for all its electrons and an orbital of the atom is not saturated. These Dangling Bonds (DBs) can be passivated by applying the wafers to a flow of forming gas (a mixture of nitrogen and hydrogen) at elevated temperatures. In this way the hydrogen atom reacts with the DB and passivates it according to

$$Si\cdot\ + H \rightarrow Si - H. \tag{3.63}$$

This process becomes important when considering the radiation hardness of the oxide layer in respect to interface traps (see section 4.2.1 for more details).

Chapter 4.

Radiation Damage in Semiconductor Devices

Radiation damages in semiconductors can be distinguished into two kinds. First, the traversing particle affects the crystal lattice of the semiconductor which leads to defects therein. Such bulk defects manifest via additional states in the bandgap and, on device level, with a change of electrical behavior.
Second, ionizing radiation generates ehps in the device. Whereas this effect is desired in the bulk of a semiconductor device, it is the origin of increased trapped oxide charge and interface traps in gate insulators.
In this chapter, both effects are discussed as they occur in DEPFET related materials (i.e. silicon, silicon dioxide and silicon nitride) with an emphasis on oxide damage.

4.1. Bulk Damage

4.1.1. Lattice Distortions

This section gives a short overview of the procedures which take place in the silicon bulk. The works of Srour et al. [44] and Moll [45] present extensive information in this field.
Briefly outlined, a particle traversing a solid body loses energy both through ionization and through displacement of atoms in the crystal lattice. Whereas ionization plays a major part in surface defects (see section 4.2), this section deals with the distortions in the solid.
When an atom in the solid is hit by a traversing particle, this atom is displaced from its original site in the crystal and thus leaves a vacancy behind. In addition to the initial particle, this Primary Knock on Atom (PKA) moves through the crystal lattice, dislocates further atoms and also loses energy via ionization.
By these mechanisms different kinds of crystal defects are produced, i.e. vacancies and interstitials. If these two are located close to each other they are called Frenkel pairs. At the end of their paths, the energies of the atoms have been reduced in such a way that defects lie very close to each other, not only forming Frenkel pairs but instead a dense agglomeration of point defects, known as clusters. An overview (in tabular form) on various kinds of defects which can arise in solids is given by Bridges et al. [46].
To dislocate a silicon atom from its lattice site the binding energy in the lattice of $E_{th} \approx 25\ eV$ needs to be overcome. For the formation of a cluster defect an energy of $E_{th} \approx 5\ keV$ is needed. However, the momentum of the incoming particle must not be neglected, therefore electrons, which are the main background in Belle II, have to have an energy of $E_{th} > 260\ keV$ for point defects and $E_{th} \approx 8\ MeV$ for clusters.
Vacancies are very mobile at room temperature and move through the lattice trying to find more stable defect configurations such as divacancies. This process of converging to a stable crystal modification is known as *annealing*, and takes place with all kinds of defects.

Movement and defect formation are strongly time and temperature dependent and behave (simplified) in an Arrhenius way, therefore it is important to keep track of time and temperature.
For experimental usage it is convenient to suppress annealing via cold temperature and perform a defined heat cycle in order to compare different DUTs. Typically a heat treatment of 80 min at 60 $°C$ is chosen, which corresponds to an annealing time of 20 days at room temperature. Measurement and handling time of the DUT $\mathcal{O}(h)$ are then negligible.

4.1.2. Manifestation of Defects

Lattice distortions in silicon devices manifest via additional energy states in the forbidden bandgap. How visible the defects are on the level of an electric device depends on their concentration, electron/hole capture cross-section and the location of the energy state in the bandgap [47].
Three kinds of manifestations can be distinguished:

1. Defects very close to the middle of the bandgap act as generation/recombination center. This will lead to an increase in thermally generated currents via Shockley-Read-Hall recombination. The issue of higher leakage currents and resulting noise is presented in section 5.2.2.

2. Removal/creation of dopants is visible as additional energy states near the band edges. This can be divided into four parts: acceptor creation/removal and donor creation/removal. It has been shown that acceptor creation and donor removal are the dominant processes leading generally to a change in effective doping concentrations and eventually to an alteration of n-doped silicon into p-doped, known as type inversion. Section 5.2.1 deals with this issue.

3. Defects can also act as trapping centers for holes and electrons. Thereby they reduce charge collection efficiency and thus increase noise. In section 5.2.2 the specific punch-through noise which is introduced by trapping centers is examined closer.

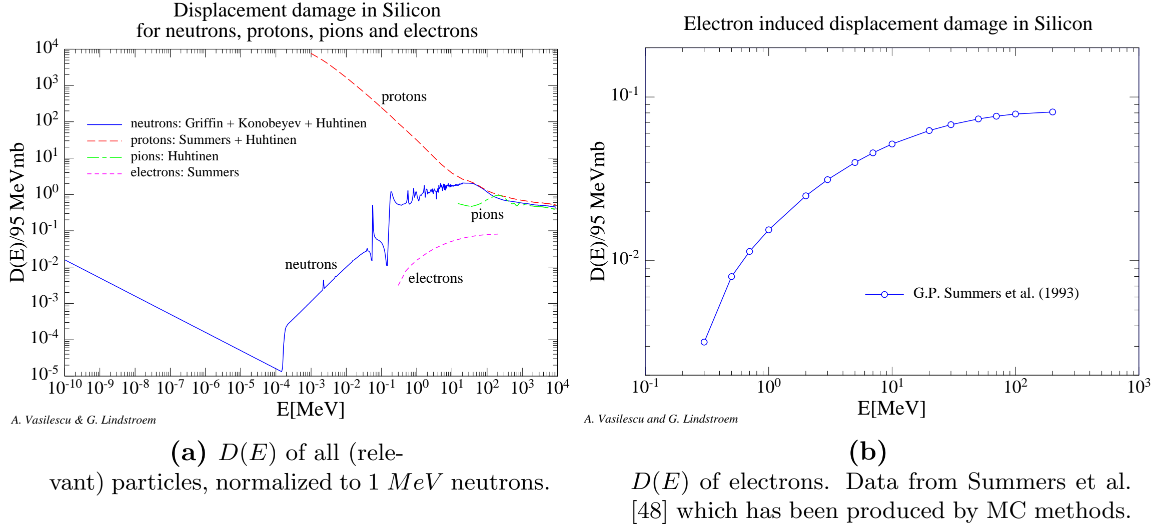
4.1.3. The NIEL Scaling Hypothesis

The effects of bulk damage are similar with all damaging particles - lattice distortions and ionization. This leads to the question if there is a way to express and scale the damage done to the bulk just by the type and energy of the incoming particle. The Non Ionizing Energy Loss (NIEL) hypothesis is based on this assumption.
The idea behind is that the damage is determined by the energy transferred to the atom and that this damage, or more precisely the displacement damage cross-section D, behaves linearly with the energy of the particle. In order to compare the damage done by different particles, D has been normalized to neutrons of 1 MeV energy

$$D(E_n = 1\ MeV) = 95\ MeV\ mb. \tag{4.1}$$

Taking the NIEL hypothesis to be valid, different fluences of particles Φ can be compared to each other via a hardness factor κ to the neutron equivalent fluence Φ_{eq}

$$\Phi_{eq} = \kappa \cdot \Phi. \tag{4.2}$$



(a) $D(E)$ of all (relevant) particles, normalized to 1 MeV neutrons.

(b) $D(E)$ of electrons. Data from Summers et al. [48] which has been produced by MC methods.

Figure 4.1.: Displacement damage cross-sections, taken from [49].

The hardness factor is determined by the damage related cross-section and the energy spectrum $\phi(E)$ of the particle fluence

$$\kappa = \frac{\int D(E)\phi(E)dE}{D(E_n = 1MeV) \cdot \int \phi(E)dE}. \tag{4.3}$$

Equation 4.3 is sometimes cumbersome to use and/or the spectrum of the particles used for irradiations is not entirely known. Assuming a monoenergetic spectrum $\phi(E) = \phi_0\delta(E - E_0)$, κ reduces to

$$\kappa = \frac{D(E_0)}{D(E_n = 1MeV)}. \tag{4.4}$$

Figure 4.1a shows an overview of the damage related cross-sections by various particles. As mentioned in section 2.4.2, electrons are the main background in Belle II and due to the magnetic field of the detector most of them have an energy of $\sim 4\ MeV$ in Layer 1 and about $\sim 6\ MeV$ in Layer 2 (cf. table 2.2).

Figure 4.1b is a close-up of electrons and at this energy

$$D(E_e = 6\ MeV) = 0.045\ (95MeVmb) \tag{4.5}$$

can be expected. Using the simplified equation 4.4, a hardness factor $\kappa = 0.045$ has to be taken into account.

Irradiation studies on silicon have been undertaken in form of huge collaboration efforts. Different particles at different energies as well as different doped silicon wafers have been investigated in order to shed some light in the parameter space which one has to deal with in this field. The *RD50* group[1] carries the work of the successful ROSE collaboration (RD48, e.g. [50]) on towards detectors for very high luminosity colliders. However, studies for the impact of low energy electron irradiation are scarce since in general the investigation

[1] `http://rd50.web.cern.ch/rd50/`

is focused on parameters more relevant for the Large Hadron Collider (LHC). This made measurements in the Belle II parameter range necessary. Dittongo et al. [51] showed the measured hardness of electrons at 900 MeV was four times less than expected from simulated data. Also, in [52] are discrepancies shown at $\sim 2\ MeV$.
Measurements of electrons in the relevant energy regime (10 MeV instead of 4 MeV respectively 6 MeV) and on appropriate silicon resistivity are undertaken, as part of the present work, to clarify this issue. These measurements are presented in section 5.1.
The NIEL scaling hypothesis is a useful tool when developing detectors for harsh radiation scenarios, however, one has to be careful by depending solely on this hypothesis, as the abovementioned discrepancies for electrons and for protons in [53] have shown.

4.2. Oxide Damage

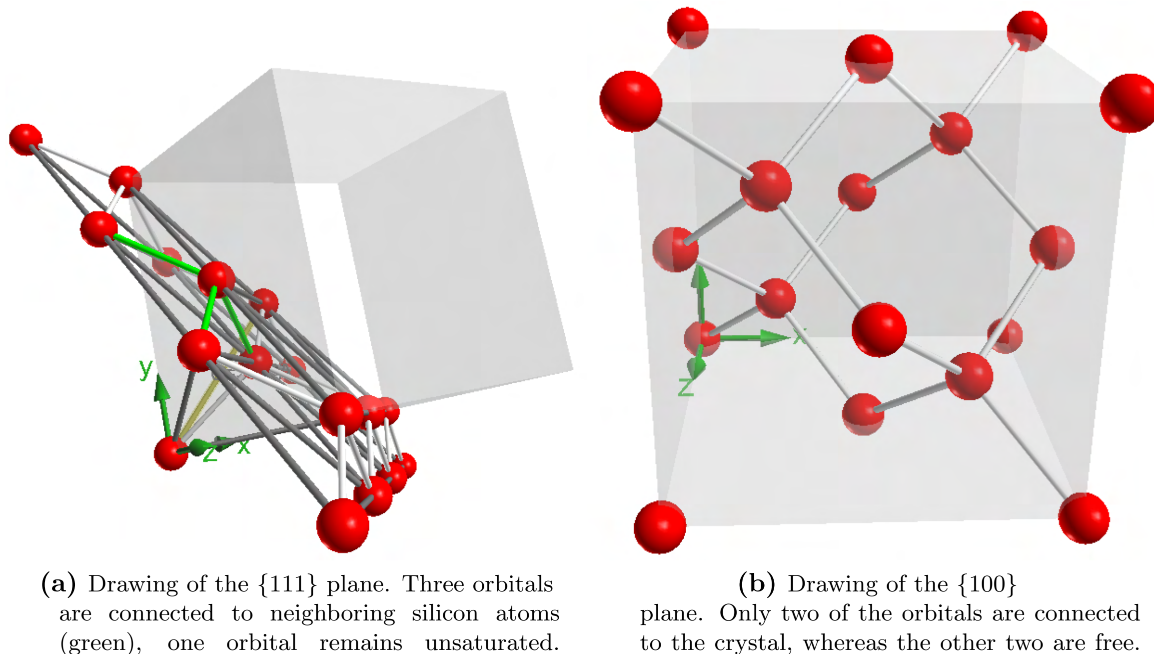
4.2.1. Microscopic View on Interface Traps

At the interface between Si and SiO_2 not every silicon atom finds a binding partner. Therefore an unused electrical binding reaches to the other side of the interface.
Depending on the oxide production process (see section 3.6.1), SiO_2 layers of different qualities are built. A good quality oxide is one which exhibits no pinholes and a low density of interface traps.
These traps originate from the different "lattice constants"[2] of silicon and silicon dioxide [54]. Figure 4.2a shows the silicon lattice cut at the {111} plane. One [sp^3]-orbital can connect to the oxide (not shown) on the other side, whereas the three other orbitals are positioned to silicon atoms in the lattice. Usually the orientation of a wafer is done at the {100} plane. A graphical representation is shown in figure 4.2b. Clearly, it is possible that two orbitals reach out from the interface.

These unsaturated bindings are called Dangling Bonds (DBs) and they can assume the electrical charge states: $-, 0, +$. Due to this behavior DBs are called amphoteric, because they can act donor- as well as acceptor-like. DBs are the physical representation of interface traps.
The DB type described above is called P_b and is the main source for interface traps [56]. The microscopic nature of interface traps was first studied by Nishi [57] on {111} silicon, using Electron Paramagnetic Resonance (EPR).
With silicon, which is cut for the {100} plane, the situation is a bit more complicated, since it is possible that two different DBs reach out from the interface. These defects are classified as P_{b0} and P_{b1}. By applying the EPR technique, Poindexter [58] was able to identify the defect level P_{b0} as the same defect which occurs at the {111} silicon, i.e. P_b.
Later on, the EPR technique was improved and gathering of defect information is now broadly done with this technique, well described in [59].

With insights into the microscopic nature of interface traps, one can assume the following model: Ionizing radiation creates electron-hole pairs in silicon dioxide. As holes hop through the oxide, they release hydrogen ions (see figure 4.5, [60]) from hydrogen containing oxide defects (D'H) along their path. If water molecules are present at interstitial sites, they con-

[2] since SiO_2 is of amorphous nature speaking of lattice constants is technically not correct. However, on short-range order the analogy to a periodical lattice can be used.



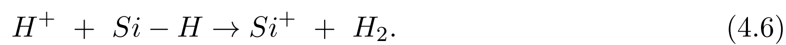
(a) Drawing of the {111} plane. Three orbitals are connected to neighboring silicon atoms (green), one orbital remains unsaturated.

(b) Drawing of the {100} plane. Only two of the orbitals are connected to the crystal, whereas the other two are free.

Figure 4.2.: Silicon interface and orientation along {111} and {100} direction. Produced with [55].

tribute to the H^+ release [61].
Protons are very mobile and move preferably to the biggest crystal defect, i.e. the interface between Si and SiO_2. However, it is also possible that the proton moves along the interface due to the energetic barriers of Si or SiO_2.
When the H^+ arrives at the interface, as illustrated in figure 4.3, it can become either directly trapped at a trap precursor or depassivate a $Si - H$ bond (see e.g. [62, 63]).
These bonds are present in most semiconductor devices. During production DBs are passivated with forming gas. The therein contained hydrogen bonds to the open binding and passivates it (cf. section 3.6.3).

Some authors argue (e.g. [64], [60]) that neglecting a hydrogen anneal might be a better way to increase the radiation hardness. Thereby a formation of additional interface traps could be prevented. However, Schwank et al. [64] only consider changes in the gate potential due to interface trap increase ΔV_{it}. It well may be that the overall trap density was already high with devices from a low H_2 anneal and the increase in V_{it} due to irradiation was therefor smaller. Devices with a high H_2 concentration initially exhibit a low interface trap concentration, which rises quickly after irradiation leading to a higher ΔV_{it}.
The depassivation according to Rashkeev et al. [62] follows



$$H^+ \; + \; Si - H \rightarrow Si^+ \; + \; H_2. \tag{4.6}$$

The dimeric hydrogen moves quickly out of the crystal and the positively charged silicon can acquire an additional electron from the bulk and forms a DB.
Although other models were proposed, e.g. by Fleetwood et al. [65], the cycling of interface traps via an electric potential is a strong argument for equation 4.6. Nevertheless, the build-up of interface traps can be quite complicated and occurs partially retarded. This effects is

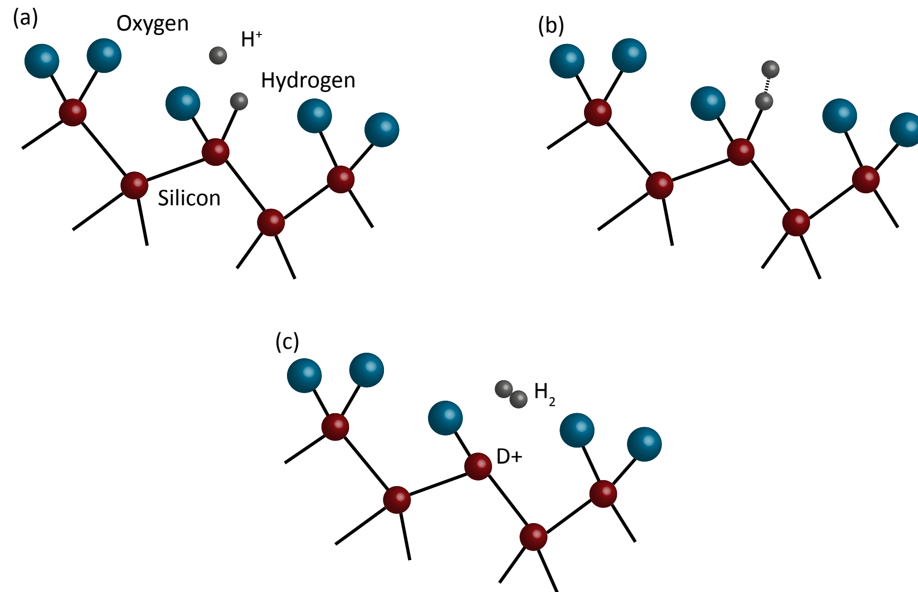


Figure 4.3.: Illustration of the formation of the P_b interface trap. Protons reach the interface (a), where they react with the hydrogen from a passivated DB (b). The dimeric hydrogen diffuses out and leaves a charged defect D+ behind (c). This defect then may react further with electrons from the silicon (after [62]).

known as *latent interface trap build-up*, and was shown by Fleetwood et al. [65]. The latent build-up is most probably due to the fact of hydrogen diffusion through the crystal lattice [66].
The information on interface traps is not yet complete, e.g. Capan et al. [67] show neutron irradiated MOS capacitors, where a stretch-out of Capacitance-Voltage (CV)-curves and hence additional interface traps are visible. In addition, they did not find a shift in the CV curve, however Lenahan and Conley J. F. [59] show an interaction between P_b and the oxide trap E' (cf. section 4.2.2).

Although EPR can give quite an insight into the nature of interface traps, for most applications it is sufficient to know where these traps are located energetically in reference to the silicon bandgap. Most laboratories use capacitance-voltage scans (see section 3.2 and 6.1.1 for details) to determine the interface trap density $D_{it}(E)$ ([56], [58], [68]).
A convenient way to look at the interface trap distribution is presented by Sze and Ng [34]. As interface traps are of amphoteric nature the distribution can be divided into two groups, one consists of acceptor states, the other of donor states. This issue is illustrated in figure 4.4.

The combined distribution D_{it} exhibits a neutral energy level E_0. Up to this level, the distribution is neutrally charged. If the Fermi level is higher (lower) than E_0 a negative (positive) net charge occurs.

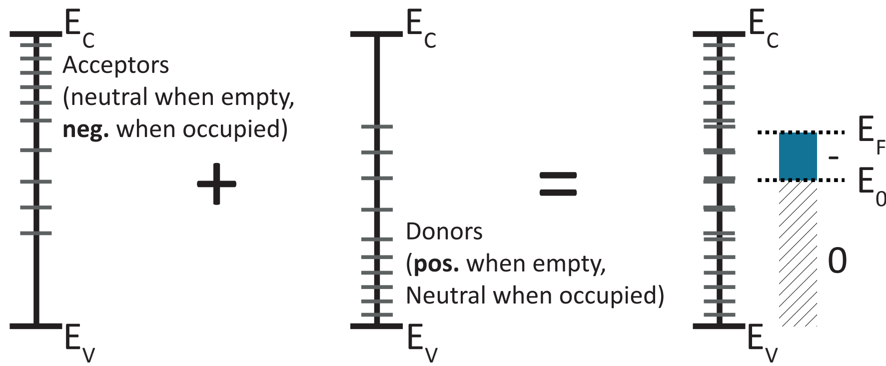


Figure 4.4.: Composition of the interface trap distribution in the bandgap. E_0 is a zero charge energy level, the total charge is determined by the Fermi level E_F.

4.2.2. Microscopic View on Oxide Traps

When silicon dioxide is exposed to ionizing radiation, ehps are created in the insulator. This process takes place as long as the energy of the generating radiation is higher than $\approx 18\ eV$.

Charge Transport

Once electrons and holes are created they start to move in the oxide. This is due to diffusion and, in most cases, also due to an electric field. Electrons are rather mobile in SiO_2 and are swiftly swept out of the isolator. Holes on the other hand have a mobility several orders of magnitude lower, i.e. $\mu_{e_{SiO_2}} = 20\ cm^2/(V \cdot s)$ vs. $\mu_{h_{SiO_2}} = 2 \cdot 10^{-7}\ cm^2/(V \cdot s)$ at 300 K [69].
The hole transport is to some degree (short-term effect) independent of the applied field [66]. However, an electric field pointing towards the Si/SiO_2 interface (see figure 4.5) enhances the movement of holes in this direction (long-term effect).
Due to their electric charge they locally distort the crystal lattice. This combination of lattice and charge carrier is known as polaron [70]. Because of their interaction with the lattice, holes move through SiO_2 via “polaron hopping”.

Charge Yield

Depending on the particle, a more or less dense column of ehps is formed along the trajectory of the traversing particle. As discussed above, electrons will quickly separate from holes, however an initial recombination will always take place. If there is no electric field present in the gate oxide, recombination of a vast amount of the created charge is possible. Therefore only a small number of holes remain in the oxide, which can then be trapped later on.
The scenario changes in the presence of an electric field. This hinders recombination and therefore increases the charge yield of holes and electrons by separating them. The number of “surviving” holes is given by

$$N_h = f(\mathcal{E}_{ox}) g D d, \tag{4.7}$$

where f is the charge yield depending on the electric field in the insulator, g a material constant defining the initial amount of generated charge pairs ($g_{SiO_2} = 8.1 \cdot 10^{12} cm^{-3} rad^{-1}$),

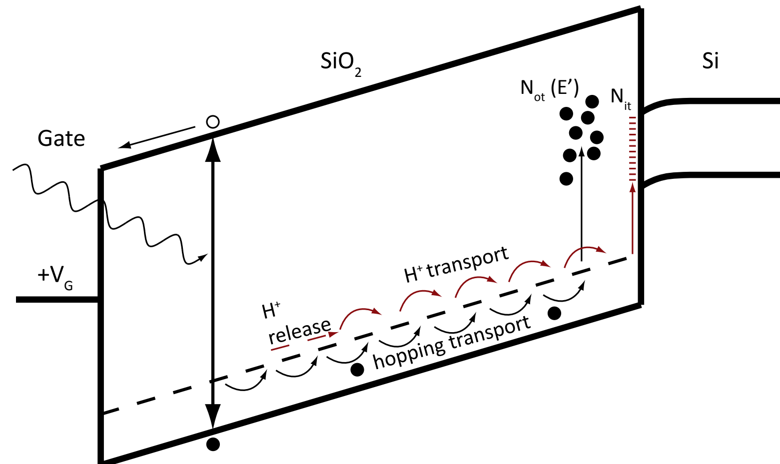


Figure 4.5.: Schematic representation of a MOS energy band diagram with positive potential at the gate. Ionizing radiation creates ehps. Electrons (white dots) are removed swiftly and holes (black dots) move via polaron hopping to defect precursors at the interface, releasing protons on their way.
Protons themselves also move to the interface, where they react with passivated dangling bonds and form interface traps (after [60]).

D is the dose and d the thickness of the isolator [71]. This idea is revisited later on in section 9.2 in which a model for the observed radiation damage is proposed.

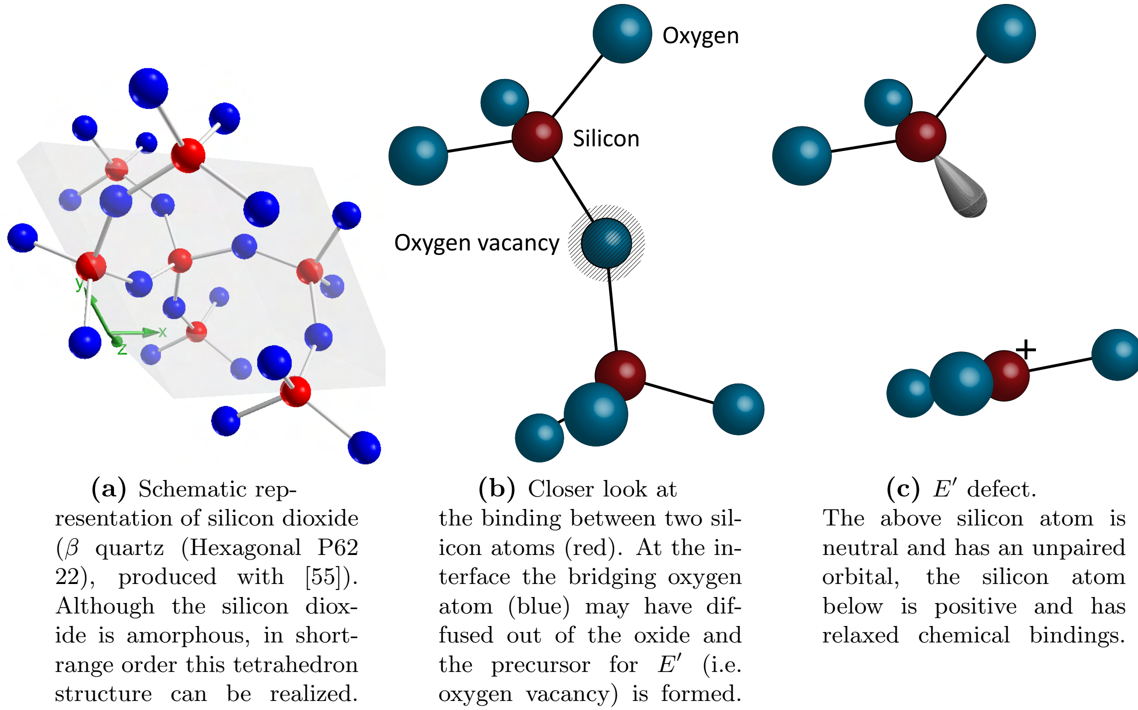
Oxide Traps

Generated holes can be trapped at defect sites near the Si/SiO_2 interface. Lenahan and Dressendorfer [72] investigated the microscopic nature of radiation induced trapped charge in their work. Via CV-measurements they determined the trapped charge and with EPR[3] measurements they estimated the concentration of a trivalent silicon defect, designated as E'[4]. The concentration of both measurements harmonized well, and it is now agreed that in fact E' centers are identical to the trapped charge.
Later on their work was refined, e.g. by [73], who broke down the E' center into E'_γ and E'_δ. Yet, all defects are based on an oxygen vacancy in the oxide and excess oxygen interstitials in the underlying silicon. These vacancies tend to be formed via out diffusion of oxygen from the SiO_2 into the underlying silicon.
Figure 4.6a shows a representation of the short-range order of the silicon dioxide and figure 4.6b zooms in on two silicon atoms. These figures illustrate how it may happen that at the stressed interface the bridging oxygen atom is missing and an electron binding from Si to Si is established. This is the classical precursor of the E' defect, and due to its origin in the crystal lattice it is highly dependent on processing and fabrication.
If there is a hole in the vicinity of the stressed binding between these two silicon atoms, it may happen that the binding gets broken. One of the silicon atoms is then neutrally charged and has an unsaturated $[sp^3]$-oribtal, whereas the other atom is positively charged (figure

[3]sometimes also called Electron Spin Resonance (ESR)
[4]a short overview on defect-labeling is given in [46]

4.6c)

$$Si - Si + h \rightarrow Si^{+} + Si. \tag{4.8}$$



(a) Schematic representation of silicon dioxide (β quartz (Hexagonal P62 22), produced with [55]). Although the silicon dioxide is amorphous, in short-range order this tetrahedron structure can be realized.

(b) Closer look at the binding between two silicon atoms (red). At the interface the bridging oxygen atom (blue) may have diffused out of the oxide and the precursor for E' (i.e. oxygen vacancy) is formed.

(c) E' defect. The above silicon atom is neutral and has an unpaired orbital, the silicon atom below is positive and has relaxed chemical bindings.

Figure 4.6.: Silicon dioxide and E' defect at the interface.

4.2.3. Influence of Oxide Thickness

The damage done in the gate insulator origins in principle from deposited energy in the silicon dioxide. This energy creates additional charge in the insulator, which is proportional to the dose.
The absorbed dose is given for photons via the Beer-Lambert law

$$D_{abs} \propto (1 - e^{-\mu d}), \tag{4.9}$$

where μ is a material absorption constant and d is the thickness of the oxide. For small values of d, equation 4.9 is linear in d.
Other radiation sources, i.e. ionizing particles, lose energy in the small layer of SiO_2 also linear with the thickness d.
As described in section 4.2.2, one of the manifestations of trapped oxide charge is the threshold voltage shift ΔV_{th}, given by the additional charge Q_{ox} and the capacitance C of the gate. The abovementioned mechanisms lead to a quadratic thickness dependence of the threshold voltage shift, first from the amount of trapped charge, and second from the thickness dependent capacitance

$$\Delta V_{th} = \frac{\Delta Q_{ox}}{C} \propto d^2. \tag{4.10}$$

As one can see in [74], the quadratic dependence is realized up to a minimum of $d \approx 20\ nm$. The shift in flat-band voltage deviates progressively below this value. It is assumed that electrons tunnel from the silicon into the oxide, neutralizing the trapped charge. The tunnel probability increases fast, and the shift nearly drops to zero for very thin gate oxides $\mathcal{O}(nm)$. In modern MOS technology, gate oxides are made in this order of magnitude to comply with the scaling rules of ongoing miniaturization, resulting in oxides which are intrinsically radiation hard.
However, the quadratic dependence relies on several assumptions, e.g. a uniform generation of charge within the oxide, which is likely true for positive fields from the gate electrode to the interface, whereas zero fields tend to show a linear behavior in ΔV_{th} [75].
Also, assuming trapping centers located directly at the interface may lead to a simple capacitance model, which can be sufficient, however taking other trap configurations in the oxide into account can also lead to a more linear behavior, such as found in [76].

Already at the beginning of design considerations of DEPFETs for Belle II, it was clear that thick oxides, which were used e.g. for the production run PXD 5, would never meet the requirements necessary for a radiation harsh environment. The question on a maximum tolerable shift in threshold voltage is difficult to answer. A hard limit is set by the Switcher (cf. section 3.4.3), which can handle $\sim 20\ V$ between gate and clear, thus a crucial quantity is the difference between V_{Gate}^{on} and V_{Clear}^{on} [77, 78].
Another critical constraint is given by the difference in gate to clear gate voltage. Those two voltages are routed on top of each other on the final chip and are isolated to each other by a layer of SiO_2. If the difference is too high, a break-down can occur, rendering parts of the module useless. However, at the moment a definite voltage on the final devices cannot be given. Yet from previous productions it is known that a voltage difference of $\sim 20\ V$ should not be exceeded.
In [75] some DUTs were measured which exhibited thinner oxides. A first high dose irradiation was carried out, shown in figure 4.7, and led to the confirmation that thinner oxides in combination with a nitride layer are very promising. A specific production run with emphasis on insulator parameters variations became necessary.

4.2.4. Radiation Hardness of Wet and Dry Oxide

This section deals with questions mostly concerning oxide trapped charge and their technological dependence. A short overview of production issues is given in section 3.6.1.
Radiation hardness of a device depends on many parameters. One of the production dependent questions is whether to use dry or wet oxides for fabrication. The precursor of oxide trapped charge is in most cases an oxygen vacancy at the interface. Clearly, the more precursors are at the interface the more likely it is that generated charge in the oxide will be trapped therein. Thus, reducing the amount of precursors is a good way of hardening the oxide.
In [79] a systematical study was undertaken for finding relevant process parameters. The work focused, amongst other issues, on the question of dry and wet oxidation. Aubuchon [79] showed that for a irradiation dose of 1 $Mrad(Si)$ with ^{60}Co and negative gate biasing, a dry oxidation leads to smaller shifts in V_{FB} than wet oxidation.
Process dependent radiation hardness was also found in the work of [72], where five differently processed MOS capacitors were exposed to 10 $Mrad$. With $+20\ V$ at the gate electrode, a

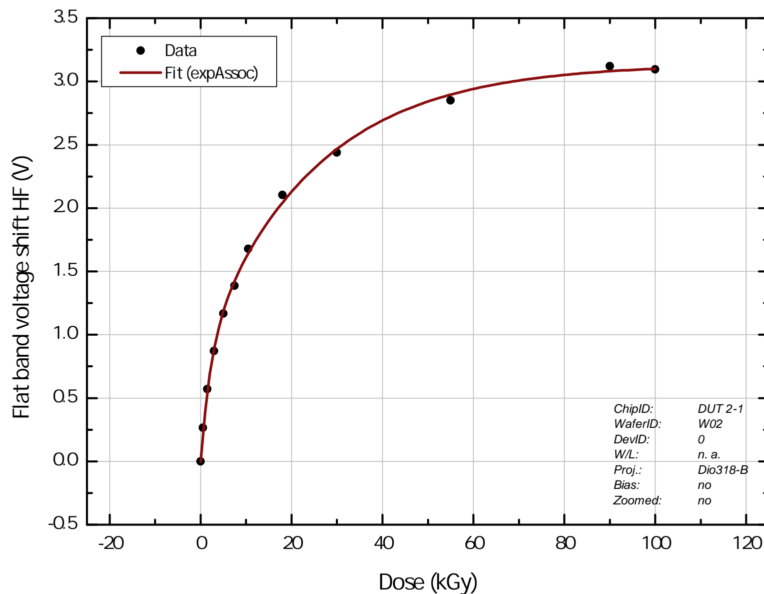


Figure 4.7.: Shift in flat-band voltage from a high frequency CV-measurement. The DUT was taken from the production run *DIO-318B* (see also table C.1 for an overview of all MOSCAP DUTs). The last measurement point is a bit lower than the previous one, this is due to a short amount of room temperature annealing ($\approx h$) after the irradiation.

difference of factor four in the E'-concentration (which is in principal oxide trapped charge) could be extracted.
The work of Schwank and Fleetwood [80] investigated process dependent radiation hardness further and emphasized on post-oxidation annealing temperatures of MOS capacitors. They showed a relaxed scenario for oxide trapped charge with $T_{anneal} \leq 875\ °C$. For higher temperatures, a fast increase in ΔV_{FB} was found and attributed to the grain size of the polycrystalline gate electrode. However, the temperature in the fabrication process is subject to several restrictions.
The diffusion of oxygen from the SiO_2 layer into the silicon is clearly influenced by temperature (cf. section 4.2.2), thus the higher the temperature the more E' precursors are likely to be present. Wet oxidation is usually performed at lower temperatures, which may lead to better radiation hard oxides. E.g. wet oxidation in this work contained anneal temperatures of $\approx 950\ °C$ and in case of radiation hardness a reduction would have been favored.

4.2.5. Gate Length Dependent Radiation Damage

A closer look on device parameters reveals a connection between the amount of threshold voltage shift ΔV_{th} vs. dose and gate length/size. Figure 4.8 exemplary shows that for a smaller gate length L the threshold voltage shift is less in comparison to the shift in those transistors with longer gates. The effect visible here is increased when looking at V_{th} values which were extracted in the saturation mode of the MOSFET. The data in figures 4.8 and 4.9 was estimated in the linear region, ensuring that short-channel effects such as DIBL do not manifest.
However, the connection between gate length L and the amount of $\Delta V_{th}(D)$ is not as present in each device as it is e.g. in L04 (figure 4.8). There are devices which exhibit a turnaround

in this issue. Table 4.1 shows an overview of the devices from the TO project. For doses higher than this turnaround value smaller gate lengths tend to be nearly every time in favor of small $\Delta V_{th}(D)$. If the dose is below the turnaround point, the behavior is reversed. In table 4.1 the effect is also quantized and divided into parts located left and right (TL/TR) on the chip. In several cases a different bias scheme was applied during irradiation at the two common gate contacts (cf. table B.1 for details).
Figure 4.9 shows an example of this issue in which the DUT E05 exhibits a turnaround at $\approx 3.5\ kGy$.

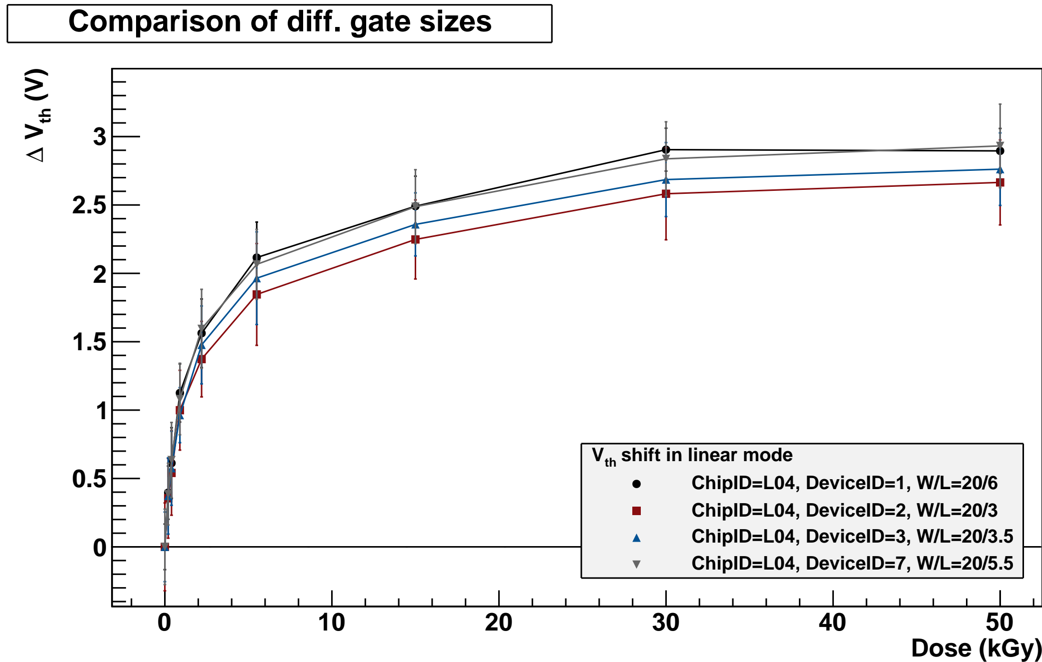


Figure 4.8.: At the DUT L04 a smaller ΔV_{th} can be observed for smaller gate lengths. Gate bias during irradiation was fixed at $-2.5\ V$.

The reason for the dependency on gate size is not quite clear. Although directly comparable devices to the DEPFET technology do not exist, in [81] p-channel MOSFETs from a radiation hard Silicon-Nitride-Oxide-Semiconductor (SNOS) process were investigated. Those devices may be compared to the devices in this study. They exhibit a higher shift in V_{th} for smaller gate length up to a dose of 10 kGy. However, in [81] the effect is very small and in the order of $\lesssim 4$ %. With a Complementary Metal-Oxide-Semiconductor (CMOS) process they observed a bigger dependency on gate length at 50 kGy, yet there the gate length was often below 2 μm. In [82] no evidence was found on devices which exhibit a polysilicon gate, whereas on devices which exhibited a $TiSi_2$ polycide gate the effect could be observed. In [82] gate size dependency could be attributed to a gate size dependency of interface traps, which arises probably due to mechanical stress of the gate insulator.
Another observation was made in [83], where the authors argue that a shorter gate length exhibits worse shifts in threshold voltage than longer gates. However the maximum dose in the study of Djezzar et al. [83] did not exceed 4 kGy.
With the devices which exhibit a turnaround effect observed in this study the effects of [81] and [83] can be confirmed, however an explanation for the observed process is difficult. Ar-

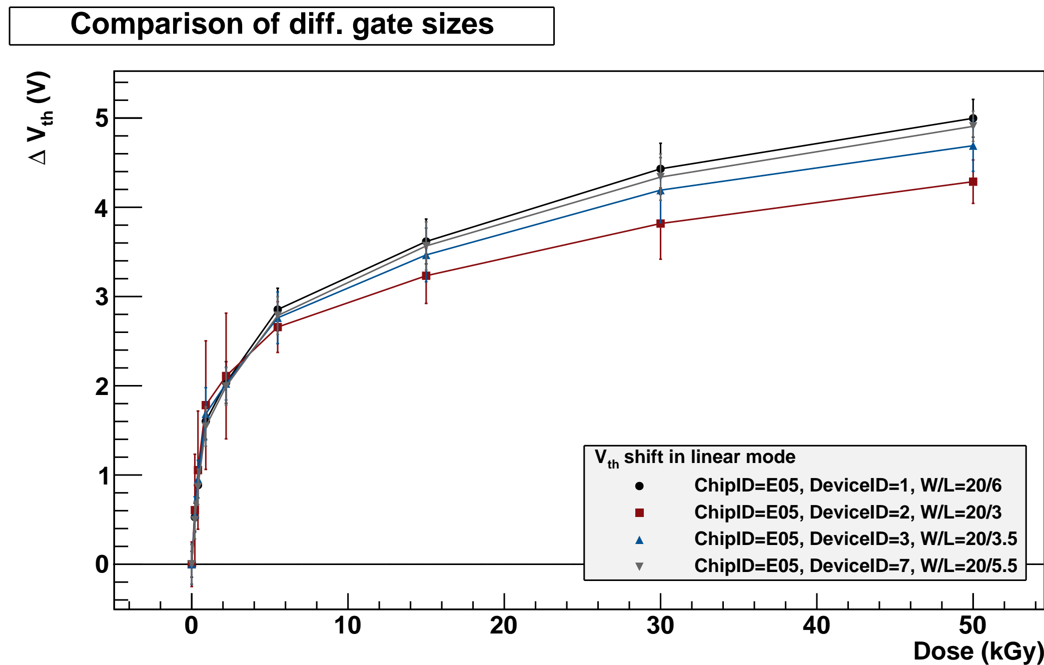


Figure 4.9.: In the range of $D \lesssim 3.5\ kGy$ a larger shift for smaller gate lengths can be observed. At the turnaround smaller gate lengths exhibit a smaller shift in threshold voltage. The gate bias of the DUT E05 was kept constantly at $+2.5\ V$.

guments which rely on additional mechanical stress for shorter gates and therefore increased trapping of holes cannot explain the turnaround effect. In addition, there are devices which behaved contrary to the ones of [81] and [83] and always exhibit better performance of shorter gates.

At the moment no conclusive explanation can be given on this issue, however differences may result due to a different biasing of the DUTs, although a distinct pattern cannot be observed.

As a relief in the matter of DEPFETs for Belle II the gate length design decision is not driven by radiation hardness since the effect is small, but instead the decision is dependent on the desired g_q (equation 3.49). The issue of radiation damage dependent on gate length may arise again when considering DEPFETs with very small gate length for high amplification/low power dissipating applications.

4.2.6. Influence of Gate Potential

The gate potential influences the amount of radiation damage in the insulator twofold:

1. The resulting electric field affects the charge yield of ehps in the insulator (cf. section 4.2.2).

2. The resulting ehps undergo a drift motion controlled by the electric field.

In this sense, the physical cause is the electric field instead of the gate potential. However, it is convenient to state gate voltage since this quantity can be easily handled in the laboratory. Quite generally it is observed that a positive voltage at the gate leads to increased V_{th} shifts.

ChipID	Dose Max. (kGy)	Effect at TL ($mV/\mu m$)	Effect at TR ($mV/\mu m$)	Description
A07	100	160	260	ΔV_{th} lower for smaller L
E04	50	182	232	ΔV_{th} lower for smaller L
E05	50	316	454	ΔV_{th} lower for smaller L, after turnaround at 3.5 kGy
E07	50	493	424	ΔV_{th} lower for smaller L
G03*	100	37	48	ΔV_{th} lower for smaller L, after turnaround at 2 - 10 kGy
G16*	100	124	115	ΔV_{th} lower for smaller L, after turnaround at 2 kGy
I03	100	187	435	ΔV_{th} lower for smaller L, (except for L = 3 m, turnaround at 7,5 kGy)
I04	50	186	267	ΔV_{th} lower for smaller L
J04	50	184	355	ΔV_{th} lower for smaller L
J15	100	142	240	ΔV_{th} lower for smaller L
L03*	100	31	36	ΔV_{th} lower for smaller L, after turnaround at 30 kGy
L04	50	189	154	ΔV_{th} lower for smaller L
L16*	100	58	66	ΔV_{th} lower for smaller L, after turnaround at 1,5 kGy
N04	50	194	200	ΔV_{th} lower for smaller L, after turnaround at 10 kGy
N05	50	245	369	ΔV_{th} lower for smaller L, after turnaround at 5 kGy
N07	30	209	157	ΔV_{th} lower for smaller L

Table 4.1.: Overview of DUTs in linear mode, where gate size influence differences in ΔV_{th}. The effect was calculated using the maximum difference in ΔV_{th} at the dose maximum and dividing it by the difference in gate length. TL/TR represent left and right hand side of TO devices (seven MOSFETs each), since the sides sometimes exhibit different gate biasing conditions (cf. table B.1). Devices with an asterisk are gate equivalent devices and exhibit MOSFETs with long gates, thus the effect is small.

In this case, not only the charge yield is high, but also the holes drift to the trap precursors at the SiO_2/Si interface. Figure 4.10 shows this issue exemplary and compares well with equivalent plots shown in Ma and Dressendorfer [74].

Since the DEPFET exhibits an internal gate the question of a resulting electric field in the

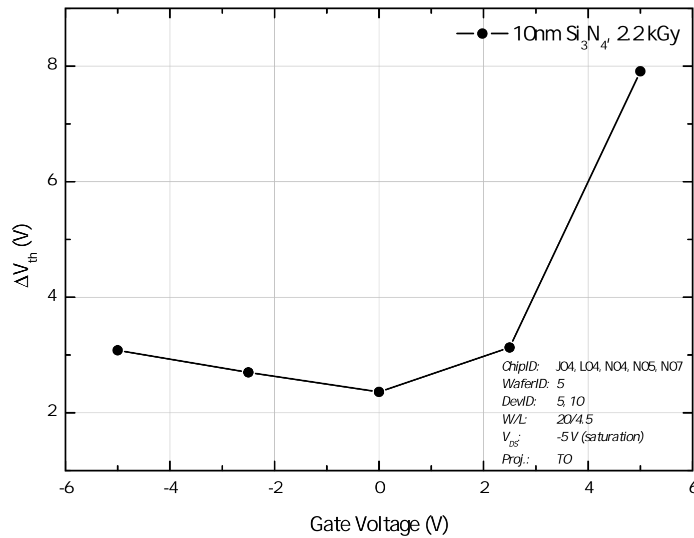


Figure 4.10.: Influence of gate potential on radiation damage.

insulator is not trivial to answer. The internal gate prevents the accumulation of majority carriers beneath the gate electrode, which results for positive voltages in a zero electric field condition. A more detailed look into this issue is presented in section 9.3.

Chapter 5.

Experiments on Bulk Damage

The main source for radiation damages in the DEPFET consists of electrons and positrons of low energy. In contrast to the LHC at which heavy and vast amounts of particles impinge on the silicon in the tracker, the device parameters of the DEPFET should only be marginally altered due to changes in the silicon bulk because of the reduced particle spectrum at Belle II. However, as the first amplification stage of the detection signal in the detector is the detector itself, already small changes are amplified and may therefore be visible.
Since there are only MC data for the displacement damage cross-section of electrons in the energy range expected at Belle II, the first section of this chapter is dedicated to the estimation of the radiation hardness factor of this main background. The second section deals with the changes of the detector material. The expected fluence of particles was simulated with neutrons. The focus lies on leakage current increase, type inversion and noise performance.

5.1. Electron Irradiation and Hardness Factor

The main contribution to the damage done to the silicon bulk is caused by the traversing of electrons from the 4-fermion final state radiation (cf. section 2.4.2). The damage mechanism in the silicon bulk is explained in section 4.1 and the various types of background radiation in section 2.4, while table 2.2 reminds of relevant parameters in assessing radiation test scenarios.
As already mentioned in section 4.1.3 some publications have brought up concerns about NIEL scaling and found estimated values for the damage function gained from MC simulations as too high. A closer look on the damage caused by electrons in the relevant energy regime was necessary.

5.1.1. Experiment

In the experiment diodes with a resistivity of 100 Ωcm were used. They exhibited a thickness of 50 μm and on each chip four different types of diodes were located. A photograph of a sample is shown in figure 5.1. Although the resistivity of the tested diodes does not match with the intended resistivity of the DEPFET modules of $\Omega_{res} = 400\ \Omega cm$ in Belle II, the results obtained with such devices are still valid as a comparison measurement (cf. results in equation 5.8 and 5.9) and previous studies have shown, e.g. [45].
As an irradiation facility the electron accelerator from Synergy Health Radeberg GmbH [84] was used (see also section A.2). This machine delivers a homogeneous beam of 10 MeV electrons to the targets. The DUTs were placed on a carrier of a band-conveyor which then moved the unbiased DUTs under the beam several times, until the desired dose was

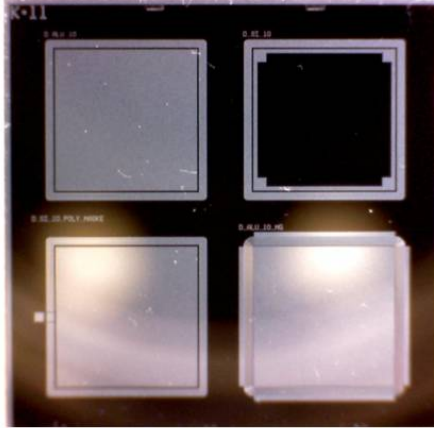


Figure 5.1.: Photograph of a diode test chip. Four different diodes are located on the chip and differ in way of contacting and guard ring design.

accumulated. The dose was measured with an alanine dosimeter close to the DUTs. The irradiation protocol states a mean error on this measurement of ~ 5.5 %. An impression of the irradiation procedure is given in figure 5.2. Table 5.1 summarizes the DUTs and the dose.

#	ChipID	Desired dose (kGy)	Achieved dose (kGy)
1	M09	4.2	2.8
2	J12	26	28.8
3	I05	52	57.6
4	I12	78	86.4

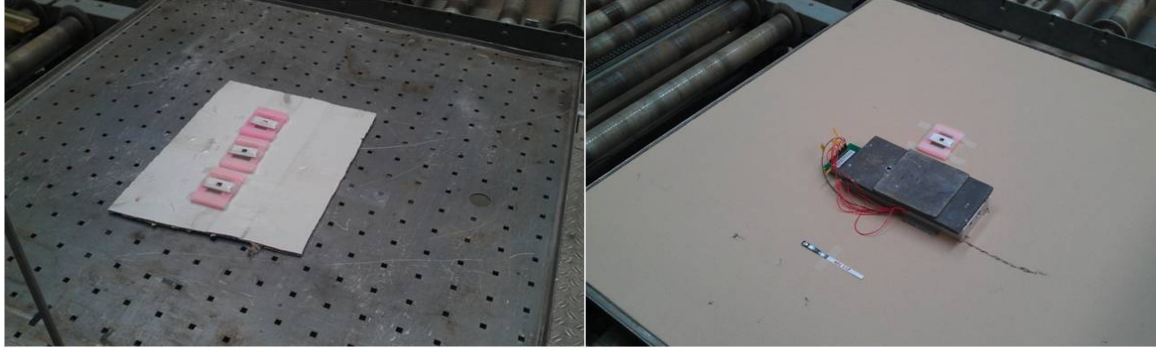
Table 5.1.: Chips and dose from the electron irradiation.

5.1.2. Analysis

Measurements

The characterizations of the DUTs were performed using Current-Voltage (IV) and Capacitance-Voltage (CV) scans. With the CV method the depletion voltage of the diode can be ascertained. Hereby the reverse bias of a diode is increased until all the volume is depleted. Assuming a parallel design of the diode, a steady decrease in the capacitance is measured until a minimum is reached. From a $1/C^2(V)$ plot a sharp bend at the onset of bulk depletion can be extracted and states the depletion voltage V_{Depl} (see e.g. also equation 5.5).
In addition, the current at V_{Depl} of the IV scan was taken as a reference mark. The volume of the diode is given by the area (ensured by a proper potential on a guard ring) and the thickness of the device. As temperature and light have an impact on charge generation, measurements were performed in a dark box and the temperature was noted and later corrected for all DUTs via equation 5.1,

$$I_{T_R} = I_T \cdot (\frac{T_R}{T})^2 exp(-\frac{E_g}{2k_B}[\frac{1}{T_R} - \frac{1}{T}]), \tag{5.1}$$



(a) Chips
J12, I05, I12 bonded on ceramic boards, which are placed on a carrier of a band-conveyor.

(b) Diode
M09 was run parasitically with a DEPFET hybrid (placed under lead plates) through the machine. A dosimeter is placed on the left.

Figure 5.2.: Electron irradiation at Synergy Health.

with T as the measured and T_R as the reference temperature. In this case, $T_R = 20\ °C$ was chosen.
The following measurement equipment was used for the characterizations:

- For IV scans a Keithley KT4200 SCS was utilized.
- For CV scans an LCR meter from Agilent of type 4284A measured the capacitance while the KT4200 SCS supplied the DC sweep voltage.

Prior to irradiation a pre-characterization took place. After the irradiation, the DUTs were kept cool to hinder thermal annealing. In order to compare the DUTs to a common standard, the devices were annealed in a thermal chamber with 60 $°C$ for 80 minutes. This corresponds to a room temperature storage for about 20 days. A more detailed explanation on the measurement procedure is given in [39].

Leakage Current Increase

The increase in leakage current of the devices is shown in figure 5.3. The slope of the increase α_{el} "[...]is a very good damage parameter for the measurement of hardness factors of high energetic particles or radiation fields" [45]. The value of $\alpha_{el} = (4.2 \pm 0.1) \cdot 10^{-19} \frac{A}{cm}$ obtained from measurements is compared with the reference increase of neutrons $\alpha_n = (3.99 \pm 0.03) \cdot 10^{-17} \frac{A}{cm}$. This leads to a hardness factor of

$$\kappa_{Exp_{10MeV}} = \frac{\alpha_{el}}{\alpha_n} = (1.05 \pm 0.03) \cdot 10^{-2} \tag{5.2}$$

for the measured electrons.

MC simulations (cf. figure 4.1b) predict values for the displacement damage cross-section. At a given energy of 4 MeV a $\kappa_{MC_{4MeV}} \approx 0.04$ can be determined (cf. equation 4.4). The measurement of 10 MeV electrons revealed a much safer experimental hardness factor. In addition, since the occurrence of cluster effects in the silicon bulk is suppressed below

electron energies of 8 MeV, a much safer operation than anticipated for DEPFETs in Belle II can be deduced.
With a fluence of $4 \cdot 10^{13} e^+e^-/(smy\ cm^2)$ for the first layer of the PXD, an equivalent NIEL fluence of

$$\Phi_{eq} = 4 \cdot 10^{11} n_{eq}/(smy\ cm^2)[= 5 \cdot 10^{10}\ n_{eq}/(ab^{-1}\ cm^2)] \tag{5.3}$$

can be calculated[1]. This is much lower than regions at which type inversion occurs (cf. section 5.2.1). The issue of resulting shot-noise due to the increased leakage current is

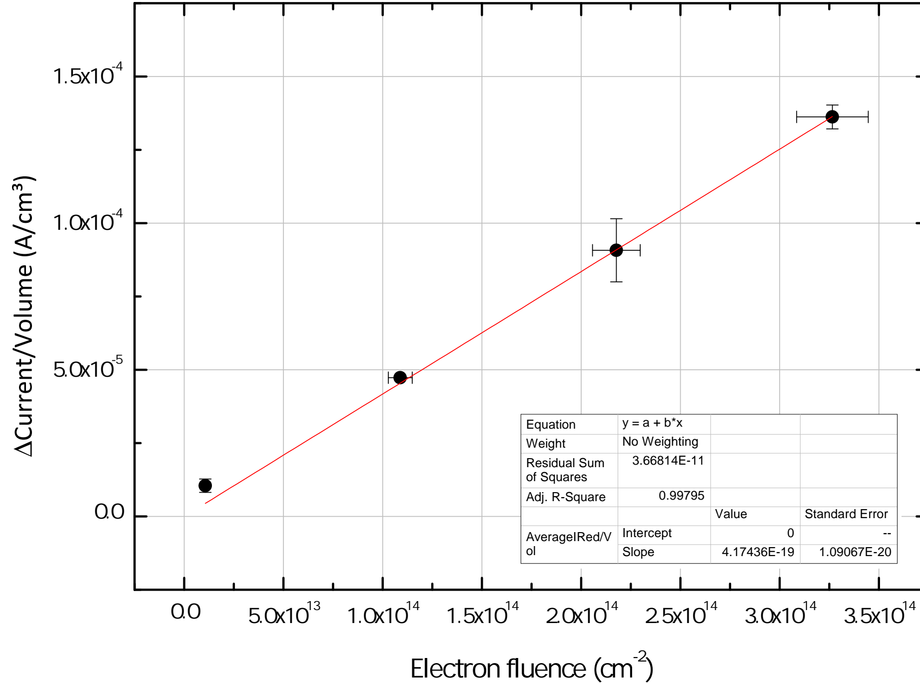


Figure 5.3.: Increase of leakage current in diodes irradiated with 10 MeV electrons. The uncertainty on dose is given by the dosimeter as 5.5 % and the error bars in on the leakage current represent the standard deviation of the diode samples on the chip. At a fluence of $\approx 1 \cdot 10^{14}\ 1/cm^2$ only one diode worked.

discussed in section 5.2.2.

5.2. Neutron Irradiations

The results and studies presented in this section were conducted by Petrovics [39] in his master thesis. In this work a brief summary on the matter of bulk damage studies with neutrons is given. A more thorough discussion on this issue can be found in his work.
Two effects of bulk damage are important considering the radiation hardness assessment of DEPFETs for Belle II:

1. Type inversion, i.e. the n doped regions of the silicon undergo a transition to p doped regions.

2. Increase in thermally generated leakage current → increase in detector noise.

[1] assuming $\kappa_{10MeV} = \kappa_{4MeV}$

5.2.1. Type Inversion

Introduction

As briefly explained in section 4.1.2, type inversion occurs due to crystal defect build-ups during/after irradiation. Particles of energies high enough to overcome the lattice binding in the silicon crystal create a PKA which then in addition creates bulk defects. Defects, such as vacancies, interstitials or impurities manifest as additional states in the silicon bandgap. The DEPFET in the Belle II experiment exhibits a depleted bulk during operation. This non-equilibrium condition results in a lack of free charge carriers, thus their concentration is negligibly small ($n \approx p \approx 0$). Due to this condition, states can only emit charge carriers in contrast to trapping which is a rare process because no charge carriers are available for trapping. However, at high fluences of radiation a considerable leakage current in detectors is present. Charge carriers from such a current *can* be trapped and emitted later on.
States near the band edges have a high emission rate $\mathcal{E}$ into the appropriate band, given by ([35])

$$\mathcal{E}_{n,p} = \sigma_{n,p} \cdot v_{th_{n,p}} \cdot n_i \cdot e^{\pm \frac{E_t - E_i}{k_B T}}, \tag{5.4}$$

with the capture cross-section $\sigma_{n,p}$ of electrons/holes of the state, the thermal velocity $v_{th_{n,p}}$ of the charge and E_t as the energy level of the trap in the bandgap. E.g. a trap located close to E_C will in most cases be empty and thus positively charged.
In this way, the radiation induced defect can alter the effective space charge N_{eff} and create/remove donors and acceptors. Changes in the scr are manifested in a change of the depletion voltage V_{Depl}, necessary to deplete the bulk of charge carriers

$$V_{Depl} = \frac{q}{2\epsilon_{Si}} d^2 |N_{eff}| - V_{bi}. \tag{5.5}$$

Here, d is the thickness of the bulk and V_{bi} the built-in potential of the diode, which is in almost any case negligible ($V_{bi} \approx 0.5\ V$).
Experiments have shown that of the four possible processes donor removal and acceptor creation are the two dominant ones. Since the bulk of the DEPFET consists of n-doped silicon a reduction of the effective doping concentration should be visible.

Measurements and Results

Measurements were conducted using diodes with a resistivity of 400 Ωcm, which is the designated DEPFET resistivity in Belle II. Irradiations were performed at the JSI TRIGA Reactor in Ljubljana (Slovenia) [85]. After irradiation the devices were kept cool until the irradiated devices were measured in the HLL, where a defined annealing cycle of 80 min at 60 $°C$ was performed.
The measurement procedure of neutron irradiated diodes is similar to the aforementioned procedure of electron irradiated diodes (cf. section 5.1.2). Equation 5.5 relates the extracted depletion voltage at a certain fluence to a effective doping concentration.

Figure 5.4 shows the measured depletion voltage together with an appropriate fit of the change in effective doping,

$$N_{eff}(\Phi) = N_{D,0} e^{-c\Phi} - N_{A,0} - b\Phi, \tag{5.6}$$

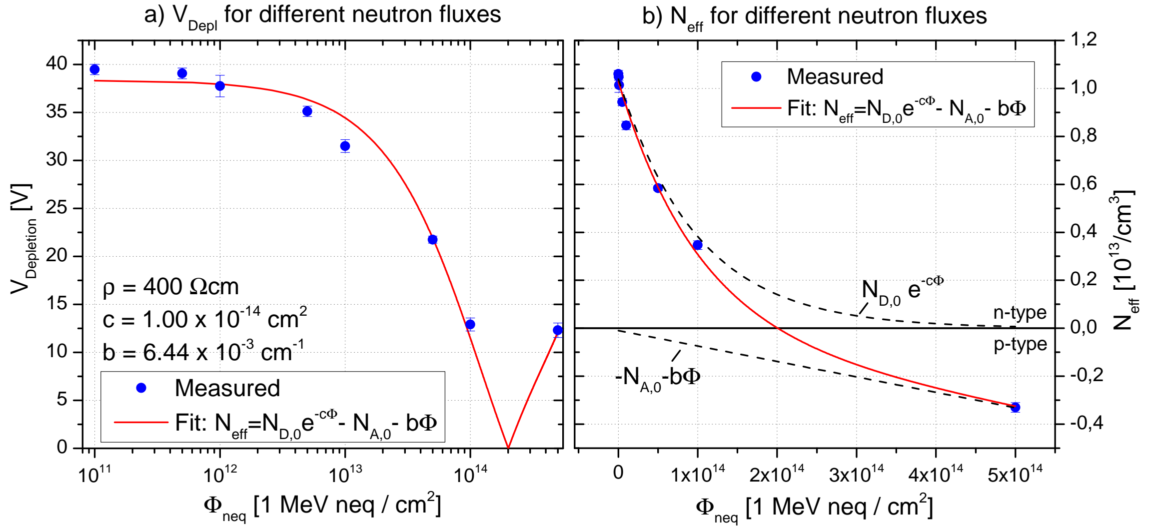


Figure 5.4.: Change in depletion voltage and effective doping concentration for 400 Ωcm. The point of inversion can be clearly seen via the fit (red) of the data (blue). *Taken from [39].*

using b for the creation of acceptors and c for the removing of donors. From the fit the point of type inversion Φ_{ti} can be extracted to be

$$\Phi_{ti} = 2 \cdot 10^{14} \frac{1MeV\ neq}{cm^2}. \tag{5.7}$$

Although the electron/positron fluence is quite high in the first layer of the PXD, type inversion will not occur for the DEPFET modules in Belle II. The hardness factor gained from electron irradiations reveals only a small damaging impact of low energetic electrons on the silicon bulk and the neutron studies show an onset of type inversion at much higher fluences than will be available at Belle II.

5.2.2. Increase in Detector Noise

Overview

The noise which is present in the DEPFET consists of several types and sources. Relevant sources are:

1. Shot noise
   a) Noise from surface generated current at interface traps (section 6.3.3).
   b) Noise from bulk generated leakage current (section 5.2.2).
2. Low frequency or 1/f noise
   a) Flicker noise in the conducting channel.
   b) Punch-through biasing noise (section 5.2.2).

The noise which originates from the bulk, i.e. through leakage current and punch-through are discussed in this section, while Flicker noise in the channel can be neglected due to the fast read-out procedure.

Leakage Current and Shot Noise

Leakage current originates from states close to the middle of the bandgap. Such states exhibit optimal emission and capture rates of electrons and holes, thus producing a current. For the measurements of the leakage current increase diodes and DEPFETs were used. The extraction of leakage currents of diodes at their depletion voltage is explained in the above section, while the extraction of leakage currents with DEPFET devices is explained in the following.
A multichannel oscilloscope card was attached to the DEPFET matrix, measuring the increase of drain current of eight pixels with respect to time. The internal amplification g_q was measured with an ^{55}Fe source. In order to find the appropriate voltages for the optimal operation point of the DEPFET additional laser scans were performed. Hereby a laser illuminated the matrix to provide signal charge in the internal gate. Then the signal due to this charge was evaluated with respect to different voltages, such as clear gate voltage, drift, backside voltage etc. The leakage current could be determined with the known pixel volume and the increase in drain current with respect to time at the optimal operation point.
The irradiation and pre-measurement procedure (thermal annealing) is similar to the above-mentioned in section 5.2.1. The current, as it is highly temperature dependent, had to be adjusted to a reference temperature of $T_R = 20\ °C$ via equation 5.1. Detailed measurement procedures are given in [39].
Figure 5.5 shows the increase in leakage current per fluence.

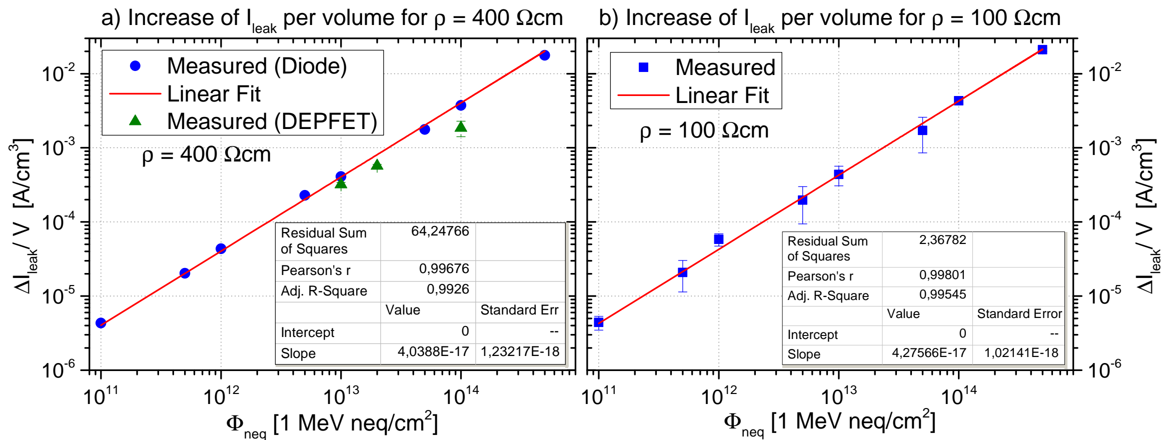


Figure 5.5.: Leakage current increase of silicon material with two different resistivities (100 Ωcm and 400 Ωcm) after neutron irradiation. *Taken from [39].*

From previous experiments, e.g. [45], a dependency on the detector resistivity was not expected and this could be confirmed in this study. The increase in leakage current was determined to be

$$\alpha_{400\ \Omega cm} = (4.04 \pm 0.12) \cdot 10^{-17} \frac{A}{cm} \tag{5.8}$$

and

$$\alpha_{100\ \Omega cm} = (4.28 \pm 0.1) \cdot 10^{-17} \frac{A}{cm}. \tag{5.9}$$

An overview of the measured leakage currents of DEPFETs is given by table 5.2.

Neutron fluence $\left(\frac{1\ MeV\ neq}{cm^2}\right)$	$1 \cdot 10^{13}$	$2 \cdot 10^{13}$	$1 \cdot 10^{14}$
$I_{leak}/V\ (A/cm^3)$	$(3.2 \pm 0.2) \cdot 10^{-4}$	$(5.7 \pm 0.3) \cdot 10^{-4}$	$(1.85 \pm 0.44) \cdot 10^{-3}$
$I_{leak}/pixel$ (pA)	61.1 ± 4.2	107 ± 5.3	348 ± 81.6
$e^-/RO/pixel\ (\#)$	7361 ± 506	12891 ± 638	41807 ± 9831
Shot noise/RO/pixel (ENC)	$85.8\pm^{2.9}_{3.0}$	$113.5\pm^{2.8}_{2.8}$	$204.5\pm^{22.8}_{25.6}$

Table 5.2.: Overview of leakage current and noise due to bulk damage. For the read-out (RO) time 20 μs together with a pixel volume of $V_{pixel} = 50 \cdot 50 \cdot 75\ \mu m^3$ was assumed ([39]).

The increase in leakage current means also an increase in shot-noise, i.e. fluctuations in the amount of electrons reaching the internal gate. A figure of merit concerning the noise in a detector is the Signal-to-Noise Ratio (SNR). The higher this ratio is, the better the signal can be recognized above the noise background. Typically, the signal in a particle detector is referred to the amount of charge created by a particle called Minimum Ionizing Particle (MIP).
A MIP deposits energy in silicon according to the Bethe-Bloch equation. However, the thinner the absorber, the more skewed the Landau distribution of the deposited energy is. Therefore for very thin absorbers such as the PXD the Bethe-Bloch equation had to be adapted to yield the most probable value for $\frac{dE}{dx}$ instead of the average value. Figure 5.6 shows the energy distribution together with the marked most probable value for 500 MeV pions in slices of silicon of different thickness.

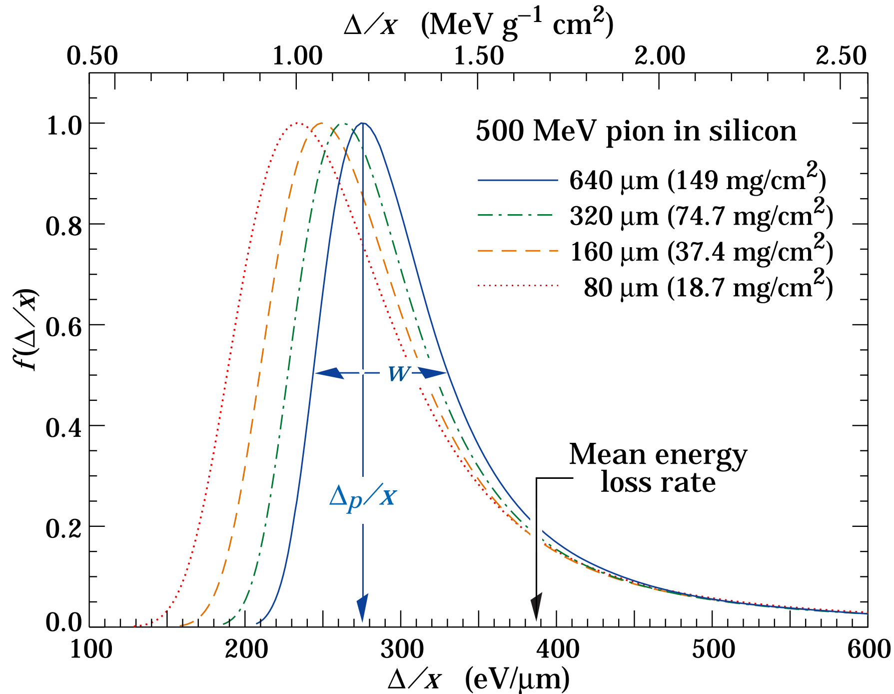


Figure 5.6.: Energy distribution for 500 MeV pions in silicon for different thicknesses [86].

As the PXD exhibits a thickness of 75 μm the most probable energy deposition is roughly

230 $eV/\mu m$. Together with the ehp creation energy of 3.6 eV the total amount of generated charge S can be calculated. The electrons thereof drift to the internal gate and are thus detected. It is convenient to state the amount of noise in Equivalent Noise Charge (ENC), so that noise and signal can be compared easily.
The intrinsic variance of the charge is given by [35]

$$< \Delta S^2 >= F \cdot S, \tag{5.10}$$

with the Fano factor $F = 0.115$. Thus, for the signal of a MIP in the PXD,

$$S = (4792 \pm 22)\ e^- \tag{5.11}$$

can be assumed.
To the amount of electrons in equation 5.11 all noise sources contribute. The shot noise contribution due to the increased leakage current is shown in figure 5.7 for a pixel in layer 1 of the PXD. This is a conservative estimate, the electron fluence in the second layer is considerably lower.

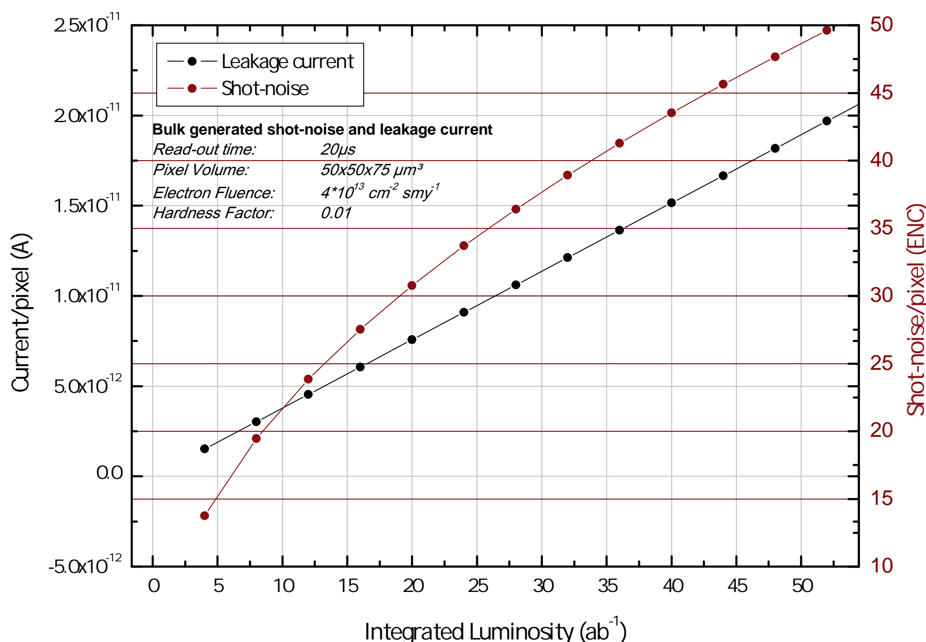


Figure 5.7.: Expected shot-noise and leakage currents vs. integrated luminosity of electron/positron induced radiation damage in the bulk. A hardness factor of $\kappa = 0.01$ is assumed.

Punch-through Biasing and Noise

One of the key features of the DEPFET is the fully depleted bulk. This is ensured via a $p+$ backside implantation and an appropriate voltage in the range of e.g. 30 V for a sensor thickness of 75 μm. At this thickness, silicon is very brittle and a safer way for biasing the backside is a punch-through (cf. also section 3.4.3) bias via the topside, instead of using a bond wire on the backside.

Figure 5.8 shows the edge region of the DEPFET. With a voltage of e.g. $-60\ V$ a punch-through to the backside is established, in such a way that this potential is set to $\approx -30\ V$.

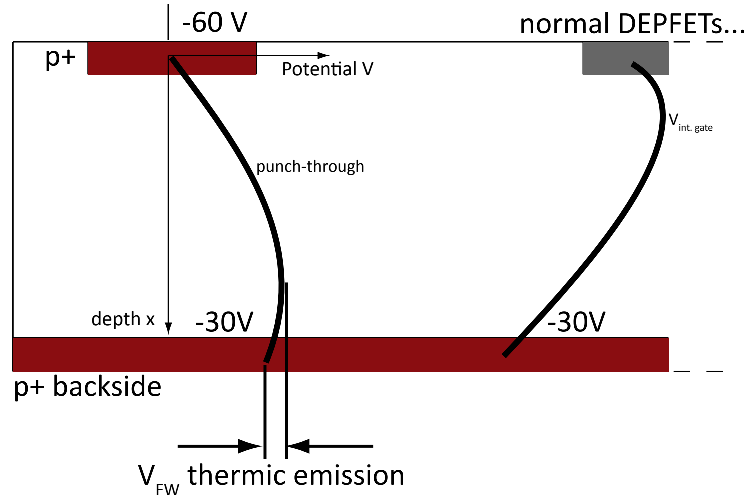


Figure 5.8.: Cut along the biasing structure of a DEPFET. On the topside a negative voltage is applied, which then is conducted to the backside of the silicon via punch-through. The height of the barrier V_{FW} is modulated by trapped charge due to radiation and will effect the channel potential via the normal depletion (potential curve on the right-hand side). In case of severe punch-through noise an additional metal layer could have been implemented at the backside, which would act as huge capacitor plate.

This depletion voltage leads then to the typical potential curve for the internal gate, as it is shown on the right-hand side of the drawing.
As the punch-through effect has to deal with the barrier from the backside contact to the bulk (denoted by V_{FW}) a stochastical emission of charge (holes) can be observed. The energy of the holes is distributed according to the Boltzmann distribution and higher energetic holes can overcome the barrier.
With increasing radiation levels more and more trap sites in the bulk are produced. When a charge carrier gets trapped in the path of the punch-through (and especially at the barrier location) and is later stochastically emitted, a typical increase in $1/f$ noise can be observed. The trapped charge carrier modulates the normal barrier height V_{FW}. Assuming an increase in V_{FW} will lead to additional holes behind the barrier. Later on, when the trapped charge becomes free, the barrier is reduced and a flush of holes moves into the punch-through path.

The issue of punch-through biasing noise was brought up by measurements for the Collider Detector at Fermilab (CDF) [87], and for the A Toroidal LHC Apparatus (ATLAS) detector at LHC [88]. To investigate this issue for the Belle II radiation scenario the abovementioned irradiated DEPFETs were studied additionally with a punch-through biasing. This was conducted via selectively switching the backside biasing from the punch-through mode to the normal backside biasing.
Measurements were then performed on a subset of the DEPFET matrix using a multichannel oscilloscope card and a designated measuring setup called Mini-Matrix System (MiMa) [89]. Amongst other methods a Fast Fourier Transformation (FFT) analysis was conducted. The resulting Power Spectral Density (PSD) is shown in figure 5.9. Even for high fluences no additional noise contribution due to punch-through is visible, which makes this biasing mode an excellent choice for the DEPFET in Belle II. One can omit the risk of bonding a wire to

the backside of the modules which would (most likely) increase the overall yield of available modules for the PXD.

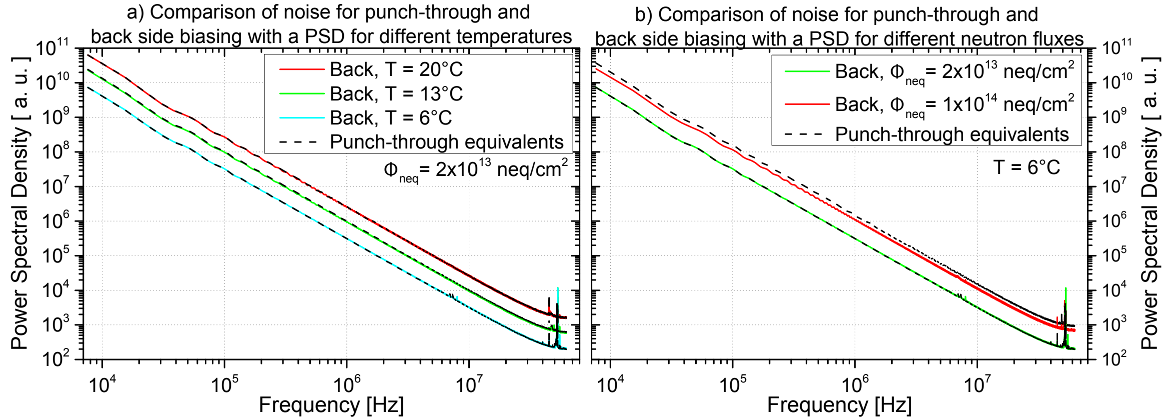


Figure 5.9.: PSD of DEPFETs after neutron irradiation. No change from normal biasing mode vs. punch-through mode can be observed in (a). The parallel shift in (b) may account for a thermal difference. Clearly, the overall reduction of temperature reduces not only the thermal generation but also reduces thermal movement of charge carriers. Thus a total reduction of noise is observed, because the constant thermal noise over all frequencies is reduced. Taken from [39].

5.3. Summary and Conclusions

In this work the hardness factor of electrons with 10 MeV is investigated. The resulting factor of $\kappa \approx 0.01$ means a considerable reduction in equivalent neutron fluence for the PXD, especially in the first layer. The total amount of damage will be most likely less than predictions by this hardness factor since cluster effects arise at the measured 10 MeV but are scarce at the expected energy of 4 MeV in the first layer.
Type inversion was studied with diodes in [39] and found to occur at a fluence of $\Phi_{ti} = 2 \cdot 10^{14} \frac{1MeV\ neq}{cm^2}$. With the new scaled equivalent fluence from electron irradiations type inversion is not an issue for the DEPFETs in Belle II.
The increase in detector noise due to bulk effects, i.e. leakage current and punch-through noise, was studied. While for the low frequency noise of the punch-through mode no additional effect was ascertained, the shot-noise due to leakage current increases. However even at a reference temperature of $T_R = 20\ °C$ the noise is still small and poses no threat to the operation in the experiment. Lowering the temperature would reduce the noise and could be a remedy if the SNR in the experiment is too weak, although already the procedure of cooling the detector to room temperature is quite challenging.

Chapter 6.

Experiments on Interface Traps

The purpose of studying interface traps for DEPFETs lies in their manifold appearance in the device. Interface traps act as an additional capacitance parallel to the semiconductor depletion layer capacitance. Due to their amphoteric nature they are emptied and filled each time the surface undergoes a charge transition, e.g. depletion $\rightarrow$ inversion. The charge load of interface traps is mirrored in the charge load of the gate. Thus the switching speed of the DEPFET is reduced, which is visible as a degradation of the subthreshold swing. A further aspect is the decrease of the transconductance g_m. The mobility of the charge carriers in the channel is reduced by additional scattering at traps near the SiO_2/Si interface.
Another aspect of interface traps is the continuous creation of charge at the surface during depletion. While this is utilized in the determination of interface traps via GCDs, in the DEPFET this effect increases the noise of the device because the created electrons my travel to the attractive internal gate and contribute to the signal electrons.
A deeper insight of interface traps can be gained with the use of MOS capacitors. This device allows a detailed look at the distribution of traps in the band gap, while from other devices (e.g. GCDs) only a rough average interface trap density can be extracted.

6.1. Interface Trap Distribution from MOS Capacitor Measurements

6.1.1. Measuring Technique

Introduction

The principal design and equations of a MOS Capacitor are given in section 3.2. There are three different methods for the extraction of interface trap properties. Two of them rely on a theoretical CV curve and all are based on the same measuring technique, which is to superpose an alternating voltage above a slowly varying DC voltage. The DC voltage is related to a DC change in the surface potential Ψ_s, which scans the band gap of the MOS capacitor from accumulation into inversion.
The small AC voltage (and its frequency) is used by the measuring device to calculate the capacitance from the capacitive reactance. In addition, depending on the frequency, interface traps can be charged or emptied by the AC change. The method relies on the fact that in a low frequency case (LF), interface traps follow the AC voltage and are visible, whereas a high frequency (HF) is too fast for them.
This section is based on the work of Nicollian and Brews [33], who provide detailed information about the measurement procedure. Pahlke [90] and Wei [75] have also studied the effect of ionizing radiation on MOS capacitors. They used high quality HLL wafers and

encountered problems with small minority charge carrier generation.

Theoretical CV Curve at High Frequencies

When applying an alternating voltage on the gate of a MOS capacitor, the surface charge and the charge in the silicon bulk reorganize themselves to the new field.
In accumulation and depletion the capacitance arises mostly from the flow of majority carriers (i.e. electrons, in this work) into the depletion layer. The crucial time constant is the dielectric relaxation time of

$$\tau_D = \Omega_{res}\varepsilon_{Si}, \tag{6.1}$$

which is for most resistivities Ω_{res} small enough to follow AC voltages in the frequency range up to 1 MHz. Minority carriers are of less importance in the above cases because of charge carrier concentration $n > p$.
However, in inversion minority carriers determine the CV relation. Minority carriers follow the applied AC voltage as long as their relaxation time τ_R is small enough, compared to the period of the voltage. As τ_R can be quite large in silicon (and especially in the high grade material of the HLL), only with very low frequencies a "true" LF-CV curve can be obtained. These minority carriers can be generated either by light or by thermal excitation. To ensure a proper measurement, which is influenced only by the silicon and silicon dioxide properties and also is a reproducible measurement, a light-tight casing was used during the measurement. This leaves only thermal generation mechanism for the minority carrier concentration. As described in section 4.1.2 bulk trap centers in the middle of the band gap act as optimal Shockley-Read-Hall-Generation centers, which is typical for low quality material and/or bulk damage. The wafers used for the TO project were high quality Float-Zone (FZ) wafers. Measurements in the inversion case are extremely difficult; in most cases even impossible. The charge generation rate can often reach $\mathcal{O}(min)$.
For this reason, only the upper half band gap during accumulation and depletion could be reasonable extracted.

For a theoretical CV curve one has to take a closer look at the inversion layer. The inversion layer charge is not affected by the AC voltage, but instead the additional voltage is (at the transition from depletion → inversion) compensated by a change in the depletion layer width. Also the inversion layer thickness has to change to take the altered electric field in the depletion layer into account.
When the inversion layer gets narrower, holes have to fill the states in the valence band to a deeper level to compensate for the still constant hole charge. Such a change can be realized by allowing the Fermi potential to have an alternating level superposed. By this method the capacitance in the HF case can be found via a similar approach as described in section 3.2.3. The method is to calculate the hole density in inversion due to an alternating Fermi level (described in detail in [33]), then to apply Poisson's equation and to integrate from the bulk to the silicon surface in order to get the dimensionless electric field v. With $Q_D = \varepsilon_{Si}\frac{dv}{dx}$ and differentiating the charge partially to potential v_S at the surface

$$C_D = \varepsilon_{Si}\frac{\partial}{\partial v_S}\left(\frac{dv}{dx}|_{x=0}\right), \tag{6.2}$$

the semiconductor capacitance is calculated.
However, the resulting equation for C_D is still too complicated for practical use. During

the transition from strong inversion to weak inversion the redistribution effect of minority carriers is small and one can simplify C_D to

$$C_D = C_{FB}(e^{-v_s} - 1)F^{-1}(v_S, u_B). \tag{6.3}$$

Here, C_{FB} denotes the flat-band capacitance, given by

$$C_{FB} = \frac{\varepsilon_{Si}}{L_D} \tag{6.4}$$

and F

$$F = 2^{1/2}\,\mathrm{sgn}(v_S)(-(v_s + 1) + e^{v_S})^{1/2} \tag{6.5}$$

is the dimensionless electrical field.

For a closed form of the CV curve, which is valid for all voltages, equation 6.3 is used for accumulation, depletion and weak inversion. For strong inversion equation 6.3 is matched to a constant value. The optimal matching point L in the dimensionless potential is given by

$$e^{v_L - 2u_B} = v_L - 1 \tag{6.6}$$

$$v_L \approx 2.1u_B + 2.08. \tag{6.7}$$

However, due to the high quality material of the used wafer, measurements in inversion are difficult since minority carriers from thermal generation are suppressed. Therefore, as the (strong) inversion case cannot be reached, the use of the matchpoint is not considered in this work.

Extraction of Interface Trap Densities from CV Measurements

Interface traps are visible in a CV measurement via two effects:

1. More gate bias is needed to sweep the CV curve from accumulation into inversion (and vice versa), this results in a stretch-out of the CV curve.
2. Interface traps contribute to the measured capacitance.

A small change in gate charge dQ_G is countered without interface traps by a change in the surface charge dQ_S, so $dQ_G + dQ_S = 0$. When interface traps are present, the change in gate charge is also countered by a change in interface trap occupation, thus $dQ_G + dQ_S + dQ_{it} = 0$. Therefore the change in dQ_S will be smaller, resulting in a smaller change of $d\Psi_S$. This means that a higher gate bias swing is needed to tune the interface from accumulation into inversion, thus a stretch-out of a CV curve can be observed.
The model of the MOS capacitor is now extended to incorporate interface traps. The picture of a series capacitance (figure 3.6) changes to figure 6.1, where an additional capacitance arises from the occupation of interface traps.

Figure 6.1 is represented by

$$C_{LF} = (C_D + C_{it})\frac{C_i}{C_i + C_{it} + C_D}. \tag{6.8}$$

Equation 6.8 already implies the LF characteristic, that is to say that the capacitance C_{it} depends on the AC frequency. Only an interface trap level, which can capture a charge within

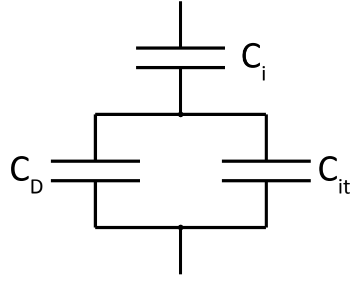


Figure 6.1.: MOS capacitor with interface traps. These result in an additional capacitance parallel to the silicon depletion capacitance.

a period of the AC voltage, contributes to the measured capacitance. For high frequencies less traps contribute and $C_{it}(f \to \infty) = 0$. However, the slowly changing DC voltage will always ensure that traps are occupied to this level. Therefore, at high frequencies only stretch-out is observed in CV measurements. In this case, the HF capacitance is given by

$$C_{HF} = \frac{C_D C_i}{C_D + C_i}. \tag{6.9}$$

Three possible measurement approaches for the determination of interface trap densities rely on the equivalent circuit diagram of figure 6.1:

1. Comparison of a theoretical HF-CV curve with a measured HF curve (stretch-out based).
2. Comparison of a LF-CV curve and extraction of C_{it} with the help of a calculated (theoretical) curve.
3. Comparison of both measured HF- and LF-CV curves.

From all CV techniques C_{it} can be determined. The relation of the trap distribution D_{it} to the capacitance is given by

$$C_{it}(\Psi_S) = qD_{it}(\Phi_S), \tag{6.10}$$

taking into account a total interface trap density, which in reality consists of acceptor- and donor-like traps (cf. figure 4.4)

$$D_{it}(\Phi_S) = D_{it}^a(\Phi_S) + D_{it}^d(\Phi_S). \tag{6.11}$$

However, with the CV measurement the trapping characteristic, implied by equation 6.11, cannot be revealed and only the total interface trap density can be extracted.

Combined HF and LF Technique

The technique is based on both HF and LF measurement. With the HF measurement, the result is a stretched-out curve and the capacitance is given by 6.9.
In the next step a LF measurement is performed. Using equation 6.8 and 6.9 leads to an expression for the interface trap capacitance

$$C_{it}(V_G) = \left(\frac{1}{C_{LF}(V_G)} - \frac{1}{C_i}\right)^{-1} - \left(\frac{1}{C_{HF}(V_G)} - \frac{1}{C_i}\right)^{-1}. \tag{6.12}$$

Gate Voltage and Surface Potential

In order to use equation 6.10, the interface trap capacitance from equation 6.12 needs to be converted to a function of surface potential Ψ_S. This can be done via a theoretical HF-CV curve $C_{HF}^{theo}(\Psi_S)$ and a measured $C_{HF}^{exp}(V_G)$ curve. Comparing the same capacitance values from both graphs, illustrated in figure 6.2, a direct relationship $\Psi_S(V_G)$ is established. This relation is used to get a $C_{it}(\Psi_S)$ curve, and with the help of equation 6.10 the interface trap density D_{it} is correctly positioned.
$C_{HF}^{theo}(\Psi_S)$ is taken from equation 6.3, with respect to the area of the capacitor, and taking into account the voltage divider with the insulator capacitance (see figure 3.6 and equation 3.6).

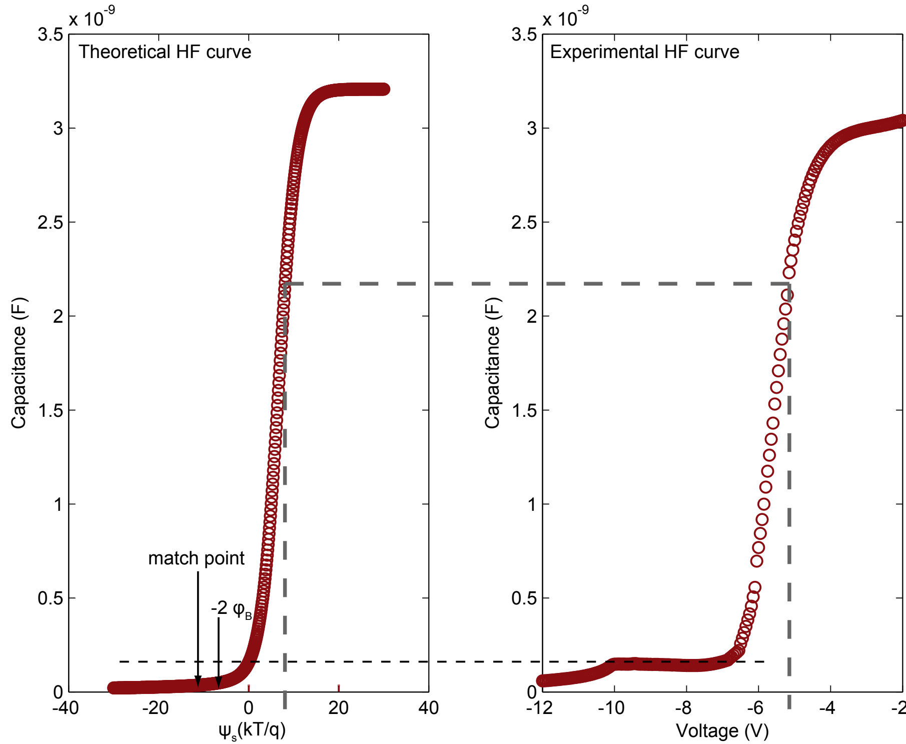


Figure 6.2.: Matching of a theoretical CV curve to an experimental one. The matchpoint is denoted in the theoretical curve, but since the point is below the onset of strong inversion and minority carriers cannot be generated as fast as they are needed in this case, the discussion is limited to the range of weak inversion → accumulation.

6.1.2. Measurements

Measurement details are discussed in this section. For detailed background information, e.g. about used frequencies and DUT descriptions cf. appendix C. The device for the extraction of the capacitive reactance was a Agilent 4284A precision LCR meter operated in the $Z - \Theta$ mode. The DC sweep voltage was supplied by a Keithley 487 Picoammeter/Voltage Source.

Convention of Potentials

With the method explained in section 6.1.1 the interface trap distributions can be extracted. The trap density is given as a function of the surface potential with respect to the Fermi level

$$\Phi_s = \Psi_s + \Phi_B. \tag{6.13}$$

The conduction band edge E_C is located at $\Phi_{s_{EC}} = 0.56\ eV$.

Device Overview and Oxide Capacitance Discrepancies

The measurements were carried out in the HLL and at the X-ray irradiation facility in Karlsruhe. As the measurement of these devices is technically complicated and time consuming, only coarse scans over several doses were performed, while MOSFETs from the same DUTs were measured in finer dose intervals. Table C.3 gives a short overview of used devices.
Although there are some deviations from the nominal thickness (see table C.2) of nitride and oxide, these deviations cannot explain the difference between calculated and measured capacitance. However, since silicon nitride was deposited in a two step process the interpretation of measurement data may be altered due to the second interface. For the extraction of interface traps, and especially for the mapping of the theoretical to the experimental HF curve, the measured (maximum) oxide capacitance was used in order to get a consistent interface trap density picture.

Frequencies for Capacitance Measurement

To obtain a "true" HF curve, higher frequencies are desirable because then the measured capacitance is (more) free of contributing interface traps. However, the phase shift Θ in this case tends to be very small and the measurement data for the extracted capacitance gets vague.
One possible remedy is to increase the AC voltage of the LCR meter to obtain higher signal values for the calculation of the impedance. However, the DC voltage sets the measured region at the band gap of the MOS interface. A too high amplitude of the alternating voltage would lead to a more coarse scan of this region. For this reason a probing amplitude of $V_{AC} = 50\ mV$ was chosen.
In addition lower frequencies as the used 20 Hz for the LF case would result in a more detailed interface trap capacitance. In the 20 Hz case interface traps contribute within capture/emission times of one half period ($= 25\ ms$).

Fermi Pinning

A problem arises if the scan speed of the DC voltage is too fast. In this case, it may happen that the surface potential remains fixed at the current trap level until this level is charged, therefore the capacitance measurement returns a constant value. This effect is known as Fermi pinning (see e.g. [54], [67]) and would have been a critical issue in this work in case minority carriers were needed due to band bending at the interface (i.e. inversion).
However, the impact of this error is small, since already in the derivation of the theoretical

capacitance the region from inversion into strong inversion has been neglected. Therefore only a reduced picture of interface traps in the upper half of the band gap can be extracted.

6.1.3. Results and Discussion

Measurement Results

For all the possible nitride thicknesses of the TO project (10, 20, 40 and 60 nm), an interface trap distribution could be extracted. However due to the lack of minority carriers and Fermi pinning results are only given at a surface potential $\Phi_s \gtrsim 0.1\ eV$.
At the beginning of the irradiation campaign the devices were put to a same dose sequentially, e.g. DUT1 from $0\ kGy \rightarrow 0.5\ kGy$ and then DUT2 to this same step and so on. This leads to a small room temperature annealing for the devices while another DUT is irradiated. For the device Q12 the procedure deviates at the point of $15\ kGy$, at which all following dose steps were consecutively applied.
Figure 6.3 shows the distribution of a MOSCAP with 10 nm nitride thickness. A change from the final dose to the last annealing measurement ($\Delta t \approx 30\ d$) is barely visible on this logarithmic scale.

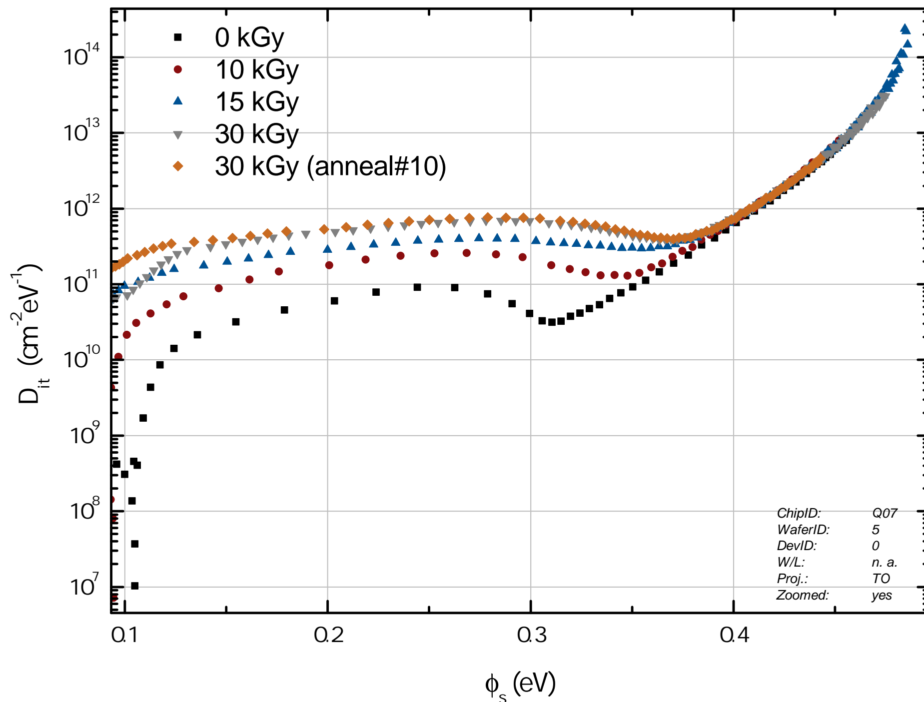


Figure 6.3.: Interface trap distribution of Q07 ($10\ nm\ Si_3N_4$). The plot shows a detail of $\Phi_s \gtrsim 0.1\ eV$, lower parts of the band gap could not be extracted due to lack of minority carriers. The orange data (anneal#10) corresponds to a room temperature annealing of $t_{RT} \approx 30\ d$. A slight increase during annealing near the middle of the band gap is visible.

Figure 6.4 shows the evolution of interface traps during $30\ d$ of annealing. Most of the annealing happens in the first few days. During room temperature annealing an effect called *latent interface trap build-up* takes place. Whereas most of the fixed oxide charges are visible instantaneously during irradiation, interface traps arise time-delayed. The data shown in

figure 6.4 (exemplary from DUT Q07) indicates that most of the latent build-up happens near the middle of the band gap, while close to the conduction band edge only small increases are visible.

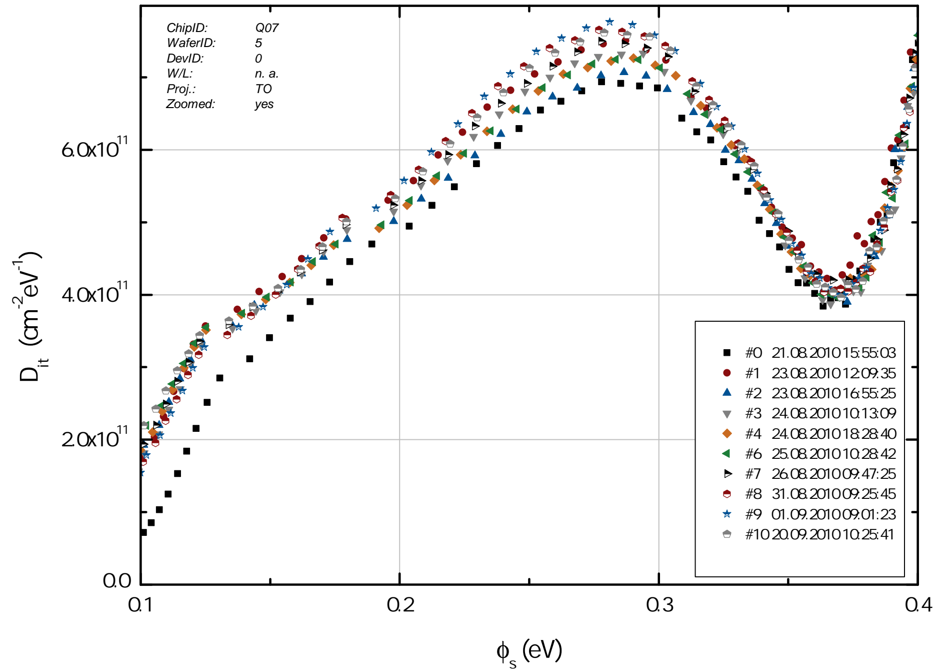


Figure 6.4.: Annealing during room temperature of Q07 after the final dose of 30 kGy. Latent interface trap build-up is shown mainly at $0.1\ eV \lesssim \Phi_s \lesssim 0.3\ eV$. Near E_C only a marginal increase takes place. The local maximum of the distribution is located at $\Phi_s \approx 0.28\ eV$.

In contrast to the Q07 device, the capacitor B07 with 20 nm silicon nitride exhibits a slightly higher interface trap distribution, shown in figure 6.5. The shape of the curve is similar to that of Q07. The local maximum of the distribution is located at $\Phi_{s_{B07}} \approx 0.29\ eV$, in comparison to $0.28\ eV$ of the capacitor Q07.

The evolution of increasing interface trap density of the 60 nm silicon nitride capacitor B12 is shown in figure 6.6.

The 40 nm DUT was irradiated up to 115 kGy, the interface trap distribution during the irradiation is shown in figure 6.7 and, on a linear scale, in figure 6.8. The measured capacitance (or more precisely the measured impedance Z and the phase shift Θ) was unstable when approaching the accumulation case for higher doses. In addition the matching to a theoretical curve increased the noise of the trap distribution. Yet despite the noisy data there is a clearly visible shift in the local maximum with dose towards the conduction band edge.

While the peak is barely visible at 30 kGy the peak height rises strongly together with the dose.

Nitride Dependency and Local Maxima

Although the B12 device exhibits the thickest silicon nitride of all studied capacitors its interface trap density is not at a maximum, as figure 6.9 indicates. In this comparison at

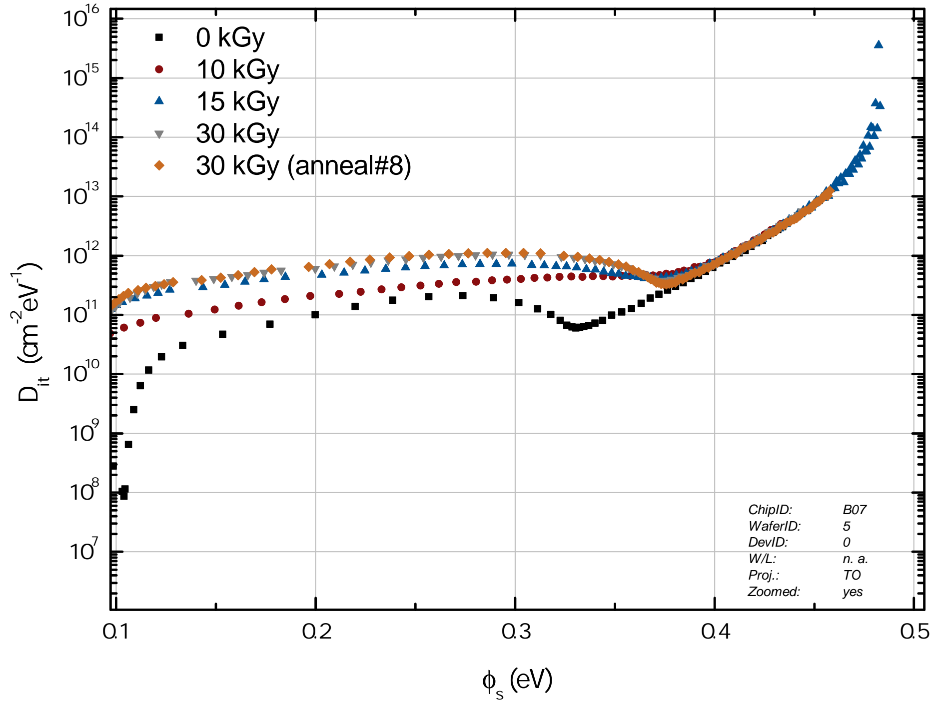


Figure 6.5.: Interface trap distribution of B07 (20 nm Si_3N_4). The orange data (anneal#8) corresponds to a room temperature annealing of $t_{RT} \approx 30$ d.

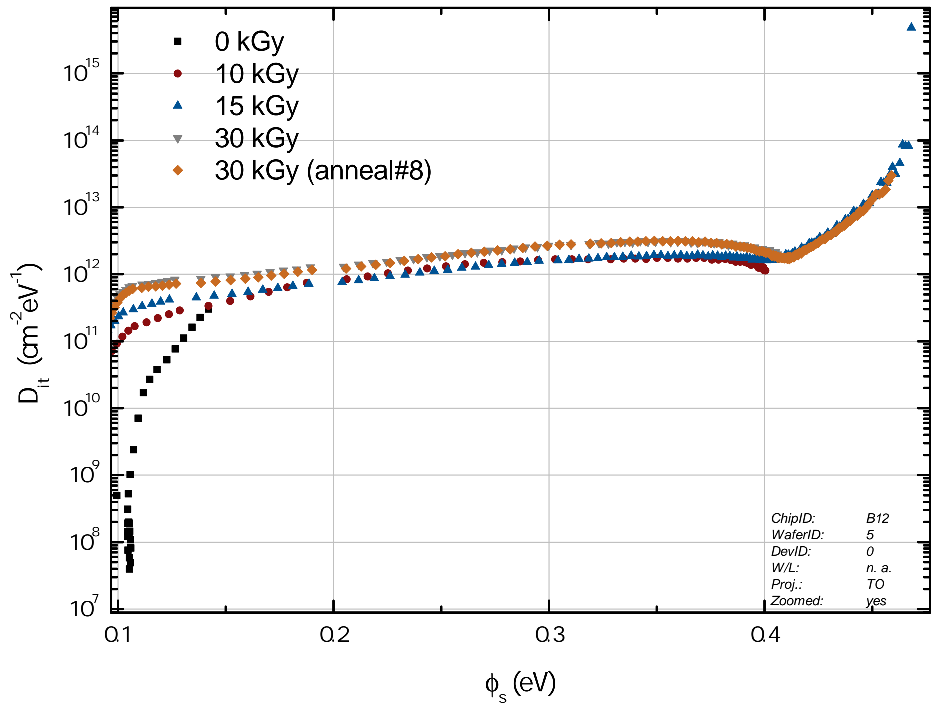


Figure 6.6.: Interface trap distribution of B12 (60 nm Si_3N_4). The anneal data (anneal#8) shown corresponds to a room temperature annealing of $t_{RT} \approx 30$ d.

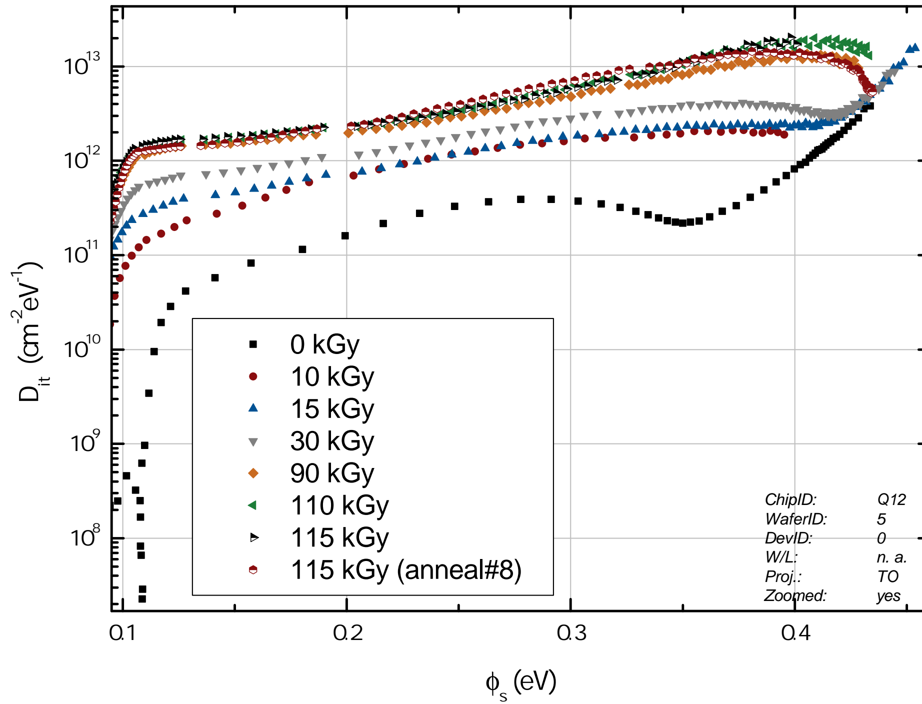


Figure 6.7.: Interface trap distribution of Q12 (40 nm Si_3N_4). The anneal data shown corresponds to an annealing of $t_{RT} \approx 29$ d.

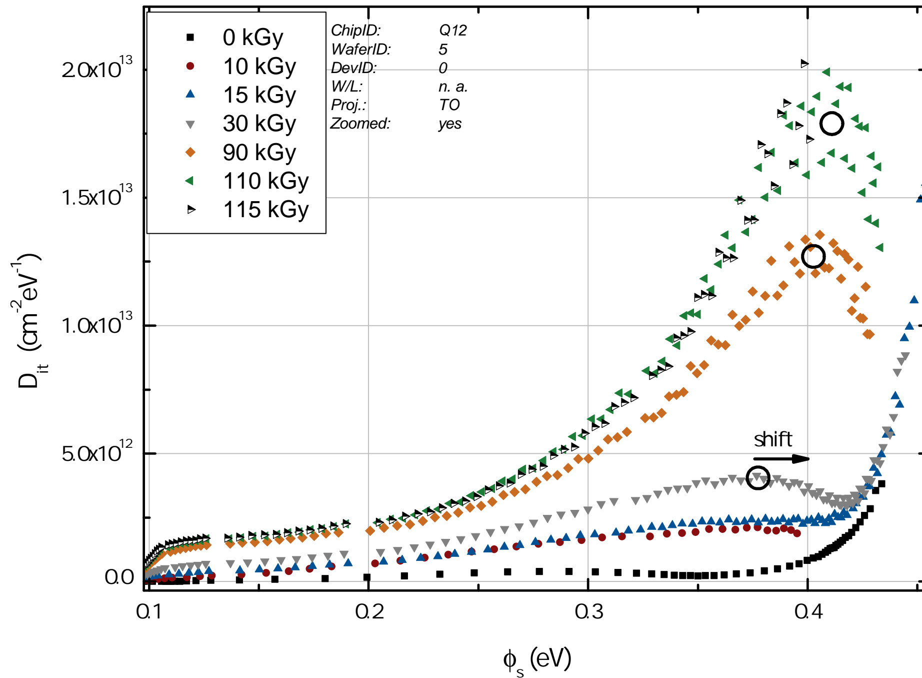


Figure 6.8.: Interface trap density of Q12. A shift of the local maximum towards the conduction band edge of the 40 nm nitride capacitor can be observed. At higher doses the measurement of the capacitor towards accumulation was unstable, resulting in a noisy extraction of the distribution.

30 kGy no clear dependency on nitride thickness can be concluded. A small thickness seems to be in favor of a low trap distribution, but the comparison of 40 nm and 60 nm nitride counters this assumption. In addition the position of local maximum tends to depend also on the nitride thickness.

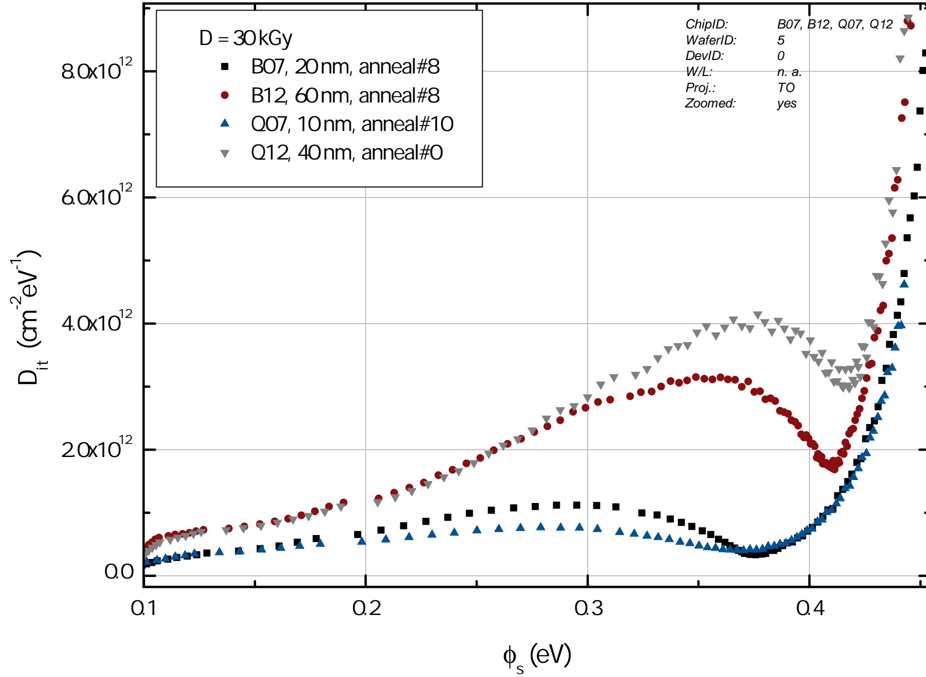


Figure 6.9.: Comparison of four DUTs with different nitride thicknesses after a final dose of 30 kGy. There is no clear dependency on nitride thickness visible, in addition the location of the local maximum is different between the two thinnest and two thickest devices.

Table 6.1 summarizes the location of the peak for the DUTs at a dose of 30 kGy.

	B07	B12	Q07	Q12
$\Phi_{s_{peak}}$ (eV)	0.29	0.35	0.28	0.37

Table 6.1.: Position of local maximum after 30 kGy.

The explanation of this behavior is difficult. The positions of local maxima are described in literature, e.g. Gerardi et al. [56] found the position of the combined signal of P_{b_0} and P_{b_1} roughly 0.3 eV below the conduction band edge. Thoan et al. [68] found two peaks in their D_{it} distribution. One of them is close to valence band edge, while the other is located 0.27 eV below E_C.
In comparison to the maxima of the capacitors studied in this work, these other local maxima are located at $\Phi_{s_{Gerardi}} = 0.26\ eV$ respectively at $\Phi_{s_{Thoan}} = 0.29\ eV$. These positions correspond well with the positions of the maxima of the devices with a small nitride thickness (10 and 20 nm) and can therefore be attributed to classical P_b interface traps (cf. table 6.1) as it is described in section 4.2.1.
However, the other position of the peak distribution is difficult to attribute. One possible explanation is that, as the signal of P_b is a superposition of P_{b_0} and P_{b_1}, so could the peak

at $\Phi_{s_{peak}} \approx 0.36\ eV$ as well be a superposition of a typical P_b interface trap defect and another, to the author unknown, defect. When this defect concentration increases, the superpositioned distribution would shift towards the unknown defect, as it is visible for Q12 in figure 6.8. The data so far would suggest an origin related to nitride deposition (yet not only on nitride thickness) and dose. If thicker nitride layers were demanded in future devices a more in-depth investigation into this issue may be in order. The extraction of interface trap distributions in the upper part of the band gap with HLL devices is shown to be possible and a typical interface trap defect is confirmed to be present in the TO production.

The extraction of interface trap properties of MOSCAPs is no trivial task. The LF measurement was conducted with a probing frequency of 20 Hz. Therefore such a measurement never is a measurement where *all* traps contribute, however the capture/emission time of non-contributing traps would have to be quite large. In addition, the HF measurement was conducted mainly with 100 kHz although the LCR meter can deliver higher frequencies. The reason for this was the decrease of the capacitive reactance of the system with increasing frequencies. Differences in Z and Θ were small in higher frequencies so in order to have a reliable signal the frequency was decreased. In this sense, the HF measurement is still polluted with interface traps. Additionally as the experimental CV curve is matched to a theoretical (interface trap free) one, a small mismatch can take place if different frequencies are used. This effect can be seen e.g. at the difference of irradiated DUTs in comparison to the ones at 0 kGy, where a lower frequency was used.
In order to access the lower band gap of the devices one could possibly place a $p+$ region near the capacitor to serve as a hole reservoir from which minority carriers can be drawn in case of inversion as it is used in charge-pumping measurements of MOSFETs (information on charge-pumping can be found in [91] and [92]).

6.2. Interface Trap Density from MOSFET Measurements

6.2.1. Calculation of Changes in Interface Trap Density

By plotting the drain current I_D in a semilogarithmic plot vs. the gate voltage V_G, the subthreshold swing S can be extracted. This quantity gives information about how fast the drain current is switched on/off, precisely the change in gate voltage in order to decrease the current by one order of magnitude.
The mechanism of the drain current in the subthreshold region is mentioned in section 3.3.5. Here, a closer look on the influence of the gate voltage to the surface potential is necessary.

The theory of the MOS capacitor (see section 3.2.3) describes how the voltage over the total capacitance is divided (equations 3.4 and 3.5). Neglecting fixed oxide charges and other influences to V_{FB}, the gate voltage divides by

$$V_G = \Psi_s + \frac{\sqrt{2\varepsilon_{Si} q N_D}}{C_{ox}}. \tag{6.14}$$

The change in gate voltage is then given by

$$\frac{dV_G}{d\Psi_s} = \frac{C_{ox} + C_D}{C_{ox}}, \tag{6.15}$$

where the depletion capacitance C_D is described in the range of depletion/weak inversion by equation 3.16.

The subthreshold swing S is given by the change in gate voltage for the drain current (equation 3.37)

$$S = ln10 \frac{dV_G}{d(lnI_D)} = ln10 \frac{dV_G}{d(\beta \Psi_s)}. \tag{6.16}$$

Substituting equation 6.15 into equation 6.16, results in

$$S = ln10 \frac{k_B T}{q} \frac{C_{ox} + C_D}{C_{ox}}. \tag{6.17}$$

When taking the additional capacitance C_{it} due to interface traps into account, equation 6.17 must be modified by

$$S = ln10 \frac{k_B T}{q} \frac{C_{ox} + C_D + C_{it}}{C_{ox}}. \tag{6.18}$$

The swing from equation 6.18 is especially useful when determining the change in interface trap densities ($D_{it} = q^2 C_{it}$)

$$\Delta D_{it} = \frac{C_{ox}}{ln10 q k_B T} \cdot (S_{irrad} - S_0). \tag{6.19}$$

Acquiring all the necessary quantities in equation 6.18 is often quite tedious, whereas for equation 6.19 only temperature and the oxide sheet capacitance need to be known. More details on the extraction of the subthreshold swing can be found in appendix B.3.

6.2.2. Measurements of MOSFETs

With the aforementioned technique the swing is extracted from each device. Since the amount of data is too extensive to show in this work a reduction is necessary. In the following diagrams the subthreshold swing was averaged from either all 14 MOSFETs or from the right and left side of the DUT. Figure 7.3 shows a typical design of a DUT. The transistors are organized in an inverse “U”-shape around the central device (designated with DeviceID = 0). Starting from the left side the transistors are labeled in their DeviceID from 1-7 and from the middle to the right 8-14. The separation/mirroring in the device layout into two groups made it possible to apply two gate voltages during irradiation.
The swing is extracted using a linear fit in the semilogarithmic plot and from the slope the change in V_G needed for one order of magnitude can be calculated. The errors of the fit were propagated to the swing and later on to the change in interface trap density.
In the calculation of the change in interface trap density (equation 6.19) a temperature of $20°C$ and the designed sheet capacitance was used (cf. table B.1).
Further information on measurement and irradiation procedure can also be found in section 7.2.

6.2.3. Results of Interface Trap Changes

In figure 6.10 the results from 10 nm and 20 nm silicon nitride devices are shown. Most of the DUTs were biased with different gate voltages in order to simulate the different regions

from the Clear Gate (CLG) (cf. section 7.4.1 for biasing schemes of the CLG). The creation of interface traps depends as well as the oxide trap charge E' on the electric field present in the insulator. The released protons should drift more efficiently to the SiO_2/Si interface if a positive voltage is applied.
In figure 6.10 such an effect is visible[1]. The devices which exhibit a fixed gate bias of 5 V during irradiation show roughly double the interface trap increase than the devices with the lowest bias of $-5\ V$. This trend is nearly universal with the one exception of DUT N04 at 35 kGy (figure 6.10a). The dip in this data cannot be sufficiently explained, however at this step the DUT was irradiated over night and a small annealing of roughly 2 hours took place until the measurement was started.

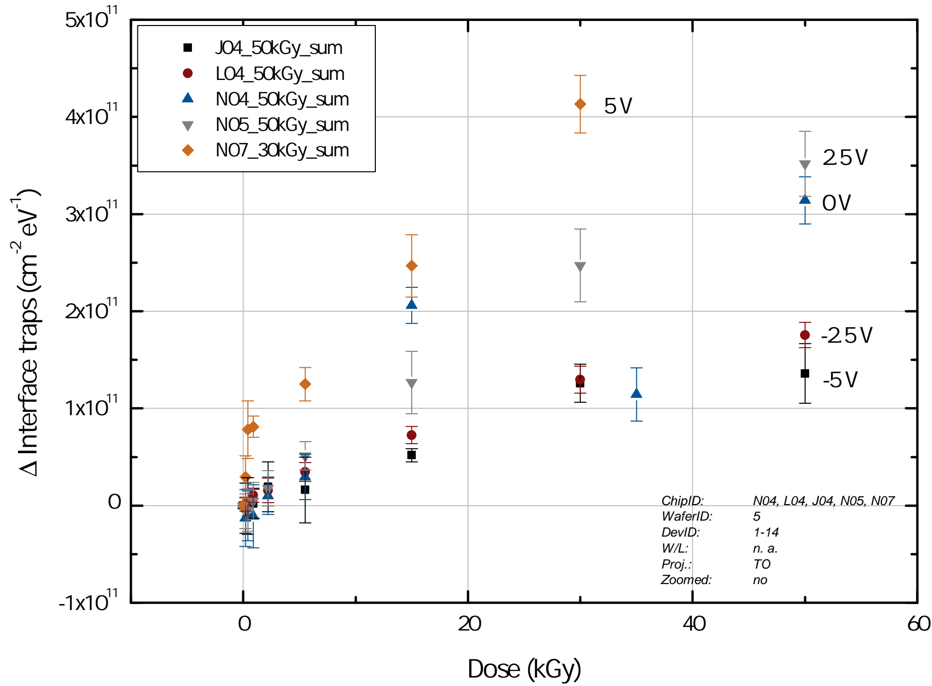
The increase in D_{it} is similar in both nitride thicknesses, although the 10 nm devices performs slightly better. The study of voltage dependency focused mainly on 10 nm and 20 nm thick silicon nitride devices. However a few irradiations were performed with 40 nm devices, shown in figure 6.13. From this data no clear correlation between nitride thickness and ΔD_{it} can be derived.
However at low doses a slight decrease in trap density is visible. This behavior is similar to the extracted transconductance $g_m(D)$ (cf. section 6.2.4), in which a small improvement is visible at the beginning of irradiation. Yet it is disputable if the trap density decreases in reality. From the increased E' centers it may happen that the holes in the channel are forced away from the interface. In this buried channel the scattering at the interface is reduced, which would manifest as an increase in g_m and a decrease in trap density. At higher doses the trap density would be too large that the effect of a buried channel device can manifest.

In the study for the CLG several voltages were applied at the gates during irradiation. The results are shown in figure 6.11 for both relevant nitride thicknesses. The acquired data supports the model of released protons in the interface as the source of interface traps. A clear dependency on gate voltage is visible. The more positive field is present, the more interface traps are created.

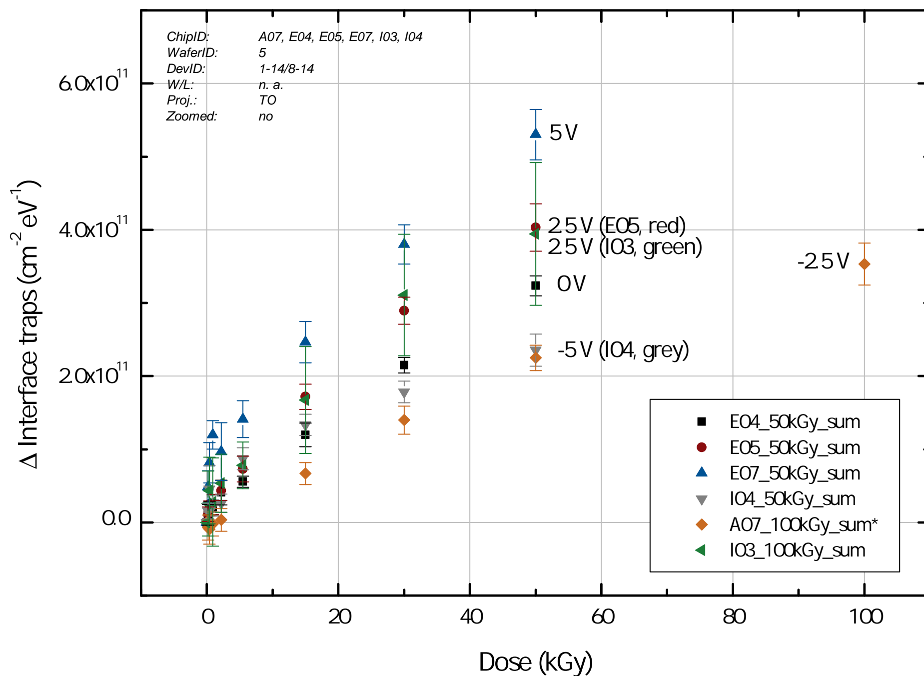
Another important scenario has been tested for the 20 nm and 40 nm devices as it was clear, that, from a technological point of view, thicker nitrides were preferred. The interface at the CLG has to be adapted continuously to the threshold voltage shift to ensure a sufficient barrier for the internal gate to the Clear.
Figure 6.12 compares for 20 nm nitride thickness constant and adaptive biasing. In most cases the adaptive biasing shows less increase in interface traps and only in few cases it is nearly the same. The same behavior can be observed in the 40 nm devices, shown in figure 6.13. With the data at hand, the adaptive biasing, which is in addition the more realistic scenario, is favorable in reducing interface trap generation.

An investigation over all nitride thicknesses was conducted for gate equivalent devices. The change in interface trap density is shown in figures 6.14 and 6.15. From both figures an universal correlation in D_{it} increase to nitride thickness can be deduced (at least for higher doses). This is in accordance to the data shown above from CLG structures in which the 10 nm showed less increase than the 20 nm nitride thickness devices.
The inlet in figure 6.14 shows a zoom into low doses. At this point the data behaves erratically, which likely occurs due to latent interface trap build-up and small irradiation

[1] the negative data point in figure 6.10b arises from one bad swing extraction at 5.5 kGy of A07, DeviceID = 13 and can therefore be ignored.

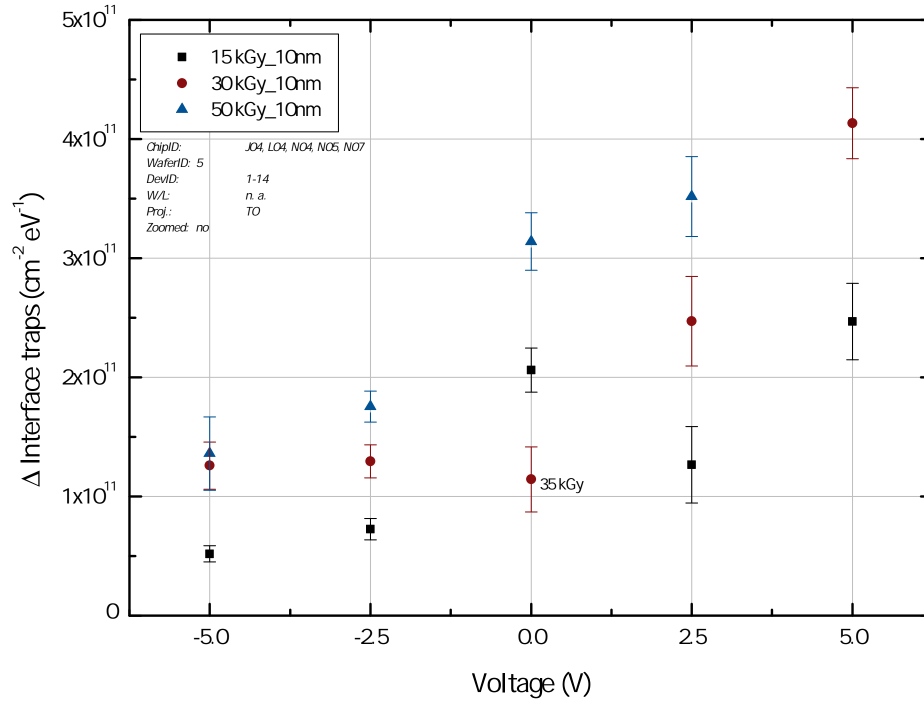


(a) Increase in interface trap density from 10 *nm* thick silicon nitride via the subthreshold technique from MOSFET measurements.

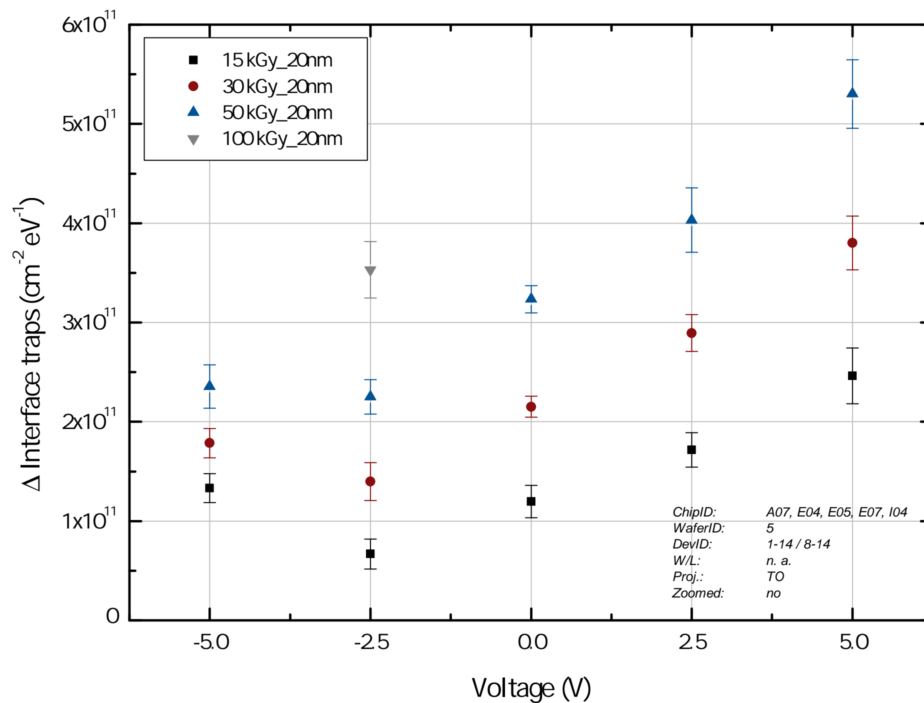


(b) Increase in interface trap density from 20 *nm* thick silicon nitride via the subthreshold technique from MOSFET measurements.

Figure 6.10.: Comparison of interface trap densities from 10 *nm* and 20 *nm* nitride. The voltage labeling refers to a fix bias at the gate during irradiation.



(a) Increase in interface trap density from 10 nm thick silicon nitride. Data point at (0 V, 30 kGy) is actually at (0 V, 35 kGy).



(b) Increase in interface trap density from 20 nm thick silicon nitride.

Figure 6.11.: Increase in interface trap density from CLG equivalent test structures of the TO project. A clear correlation between increase in D_{it} and applied gate voltage during irradiation is visible.

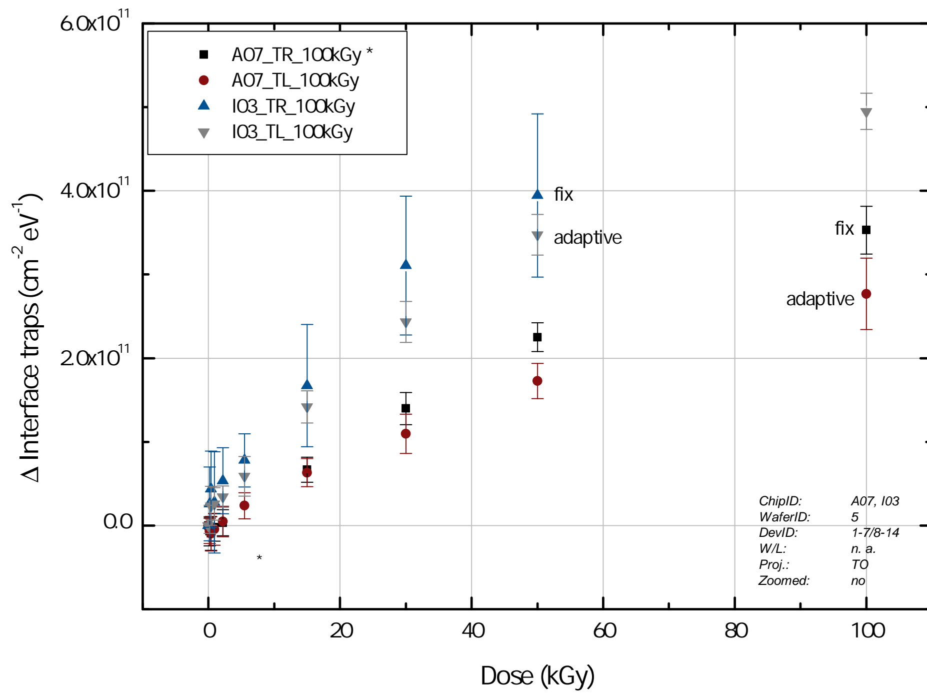


Figure 6.12.: Comparison of adaptive and fix biasing with 20 nm thick silicon nitride.

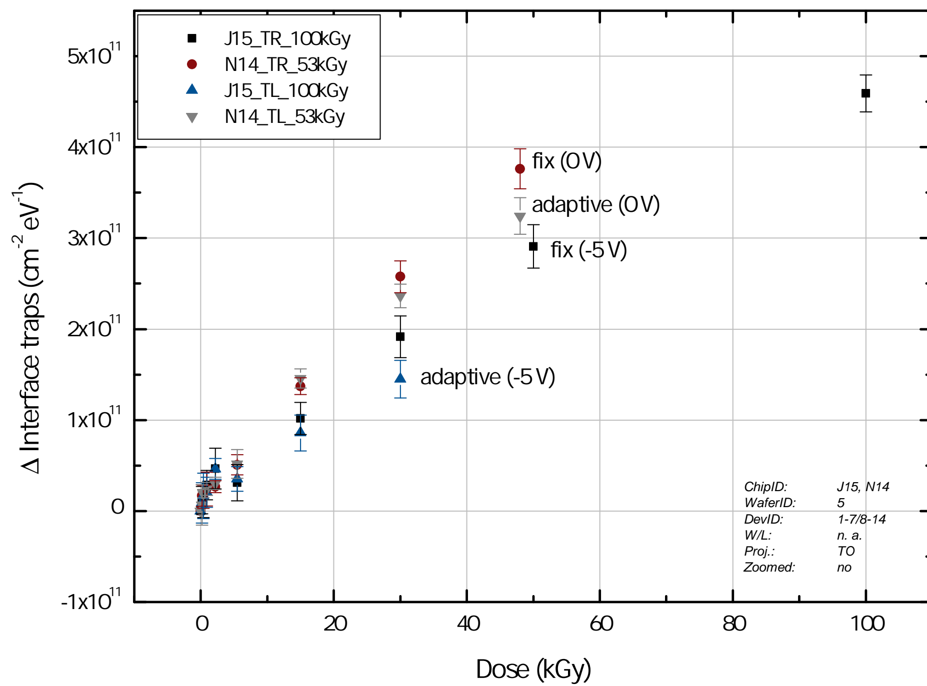


Figure 6.13.: Comparison of adaptive and fix biasing with 40 nm thick silicon nitride.

intervals. Concerning the interface trap density from MOSFET measurements a nearly overall observation is a slight reduction at low doses. Such an observation can clearly be seen in the inlet for the 10 nm device. However, from corresponding measurements with GCDs or MOSCAPs such a reduction is not visible. Most likely this reduction can be attributed to the buried channel effect (see above). Yet, such low doses will be reached quickly in the final experiment, thus this effect plays only a marginal role.

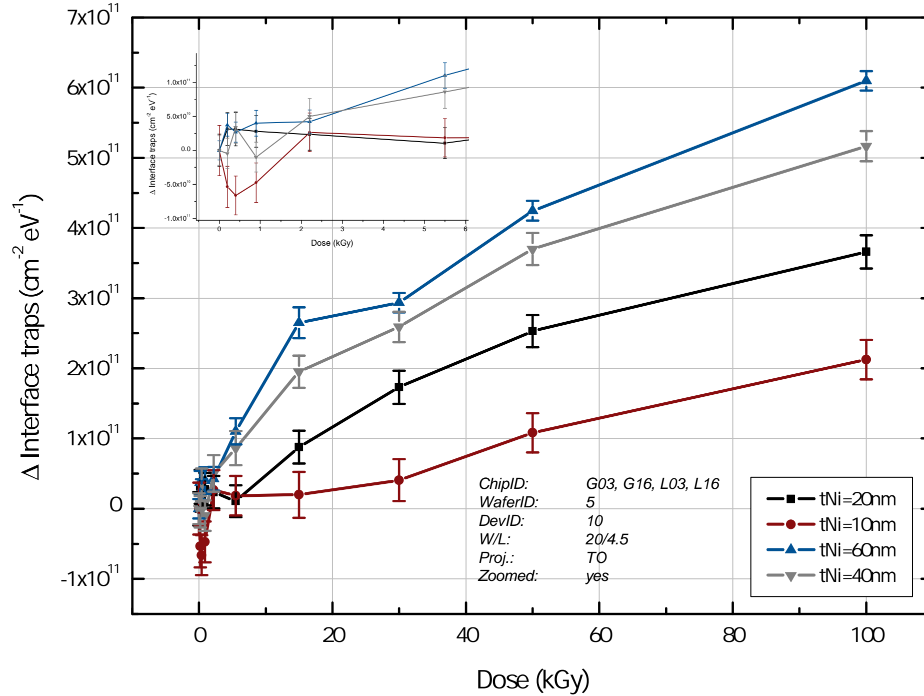


Figure 6.14.: Changes in interface trap density from gate equivalent structures. The inlet shows the behavior at low doses.

In figure 6.15 the change in D_{it} is shown with the gate bias as an additional parameter. Besides the fixed gate bias of $+2\ V$ during irradiation the other gate bias has been adapted. Different to the adaption from CLG devices the adaption is stopped at zero volts (confer also section 7.3.1 on biasing schemes). While from CLG devices the adapted ones show a lesser increase in trap density, the situation with gate equivalent devices is inverted. Yet, the adaption is, depending on gate capacitance, stopped more or less at low doses. At this point the drift for generated holes in the oxide is reduced and less traps are generated. The difference between the two biasing schemes is marginal and the difference to the CLG structures can be attributed to the early stop.

6.2.4. Influence of Interface Trap Density on Transconductance

Besides causing other effects, interface traps can manifest in a change in the MOSFET transconductance g_m (cf. equation 3.48). The traps act on the charge carrier mobility μ via[2]

$$\mu = \frac{\mu_0}{1 + \alpha_{it} N_{it}}, \tag{6.20}$$

[2]assuming the change due to oxide traps to be negligible

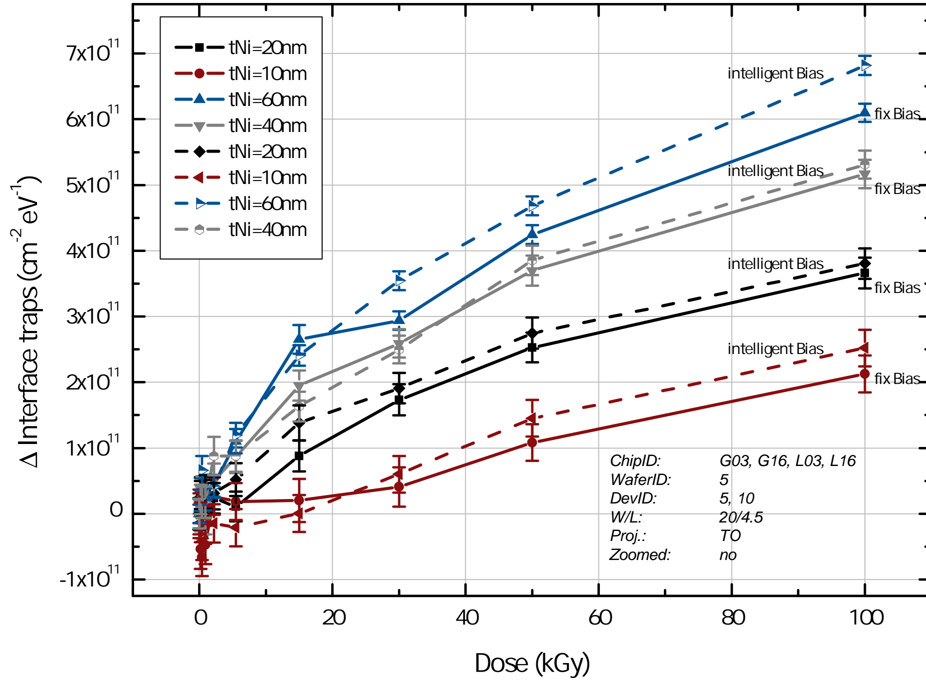


Figure 6.15.: Interface trap density changes with respect to fix ($+2\ V$) and intelligent ($+2\ V \rightarrow 0\ V$) gate bias. Since the adaption is stopped at low doses the difference is only marginal.

in which N_{it} is the total amount of interface traps in units of $1/cm^2$ and α_{it} a constant determined experimentally to be $35 \cdot 10^{12}\ cm^2$ ([93]). The transconductance of the MOSFET is an important parameter since the internal amplification g_q of the DEPFET is directly related via equation 3.50.
The data presented in this section is extracted from the TO project. The devices shown[3] exhibit a gate length $L = 4.5\ \mu m$ and were irradiated with a fixed gate bias during irradiation. The g_m was estimated at a drain current of $I_{DS} = 100\ \mu A$ and since the capacitive coupling of the gates of the thinner devices is larger, the transconductance is also higher compared to the 20 nm devices. However, small deviations due to production induced spread have to be considered. The spread can be seen in the zoomed figure 6.17b at $D = 0\ kGy$.

The data for devices with 10 nm nitride, figure 6.16, corresponds well with the interface trap increase gained from the behavior of the subthreshold swing. The devices which were irradiated with a negative gate bias show a smaller decrease in g_m than the devices with a positive voltage.
With the thicker nitride configuration of 20 nm (see figure 6.17) the clear dependency on gate bias during irradiation is distorted up to medium doses, originating from the DUT I04 with a zero gate bias. Except this data, the situation is comparable to the thinner nitride devices. However, the different behavior for the the two devices which were both irradiated with $+2.5\ V$ and the similar behavior at low doses of A07 ($-2.5\ V$) cannot be readily explained. A possible explanation is the fact that after irradiation a difference in the short-annealing time is present. Shaneyfelt et al. [94] showed that directly after irradiation

[3] DeviceID = 10

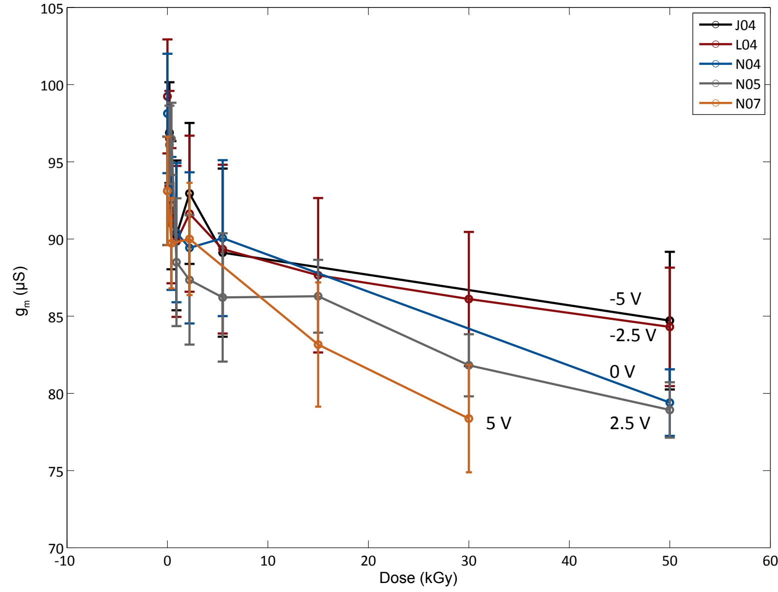


Figure 6.16.: Transconductance of 10 nm nitride MOSFETs. The parameter is the fix gate bias during irradiation for the CLG equivalent transistors.

the build-up of traps takes time and even time differences on a short-scale $\mathcal{O}(min)$ do have already an effect.
A small increase in g_m (figures 6.16 and 6.17), visible also as a decrease in the subthreshold swing extracted interface trap density D_{it}, can be observed up to a low dose of 2 kGy. Although Awazu et al. [95] have found reductions of the interface trap center P_b in a dose range up to 150 kGy, the reduction in the devices in this study show this behavior only for small amounts of radiation. A more possible explanation attributes this effect to a buried channel behavior (cf. section 6.2.3).
A typical decrease in the g_m depends on gate bias and nitride thickness. The figures presented above give detailed information on this issue, a rough decrease of ≈ 15 % can be taken into account after 100 kGy of irradiation.

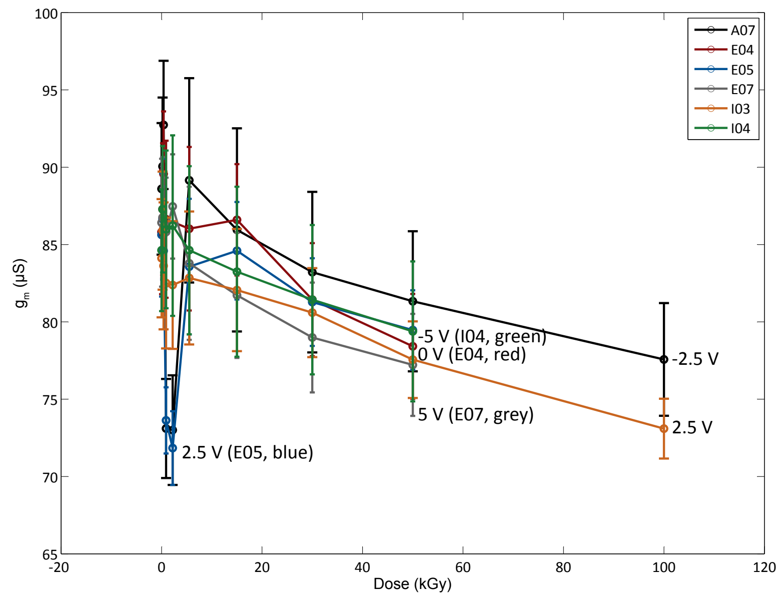
6.3. Interface Trap Extraction from GCD Measurements

6.3.1. Interface Trap Density

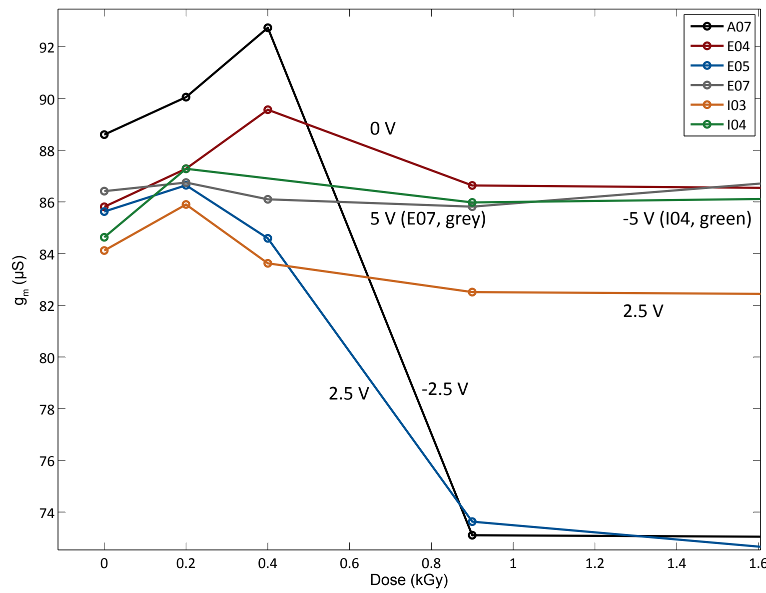
The GCD offers an easy access to the surface generated current. For details of theory and principal operation of a GCD cf. section 3.5. Perhaps the most important parameter of a GCD is the surface current I_S (equation 3.51) and, derived from this quantity, the surface generation velocity s_g (equation 3.55).
The interface trap distribution is given directly proportional to s_g by

$$D_{it} = \frac{s_g}{\sigma v_{th} \pi k_B T}. \tag{6.21}$$

However, the effective capture cross-section is disputable.



(a) Extracted transconductance at $I_{DS} = 100\mu A$.



(b) Zoom of figure 6.17a into low doses (error bars omitted).
A small increase in g_m is visible, possibly due to a buried channel behavior.

Figure 6.17.: Transconductance of 20 nm nitride MOSFETs. The parameter is the fix gate bias during irradiation for the CLG equivalent transistors.

Uncertainties on the Effective Capture Cross-Section

Several groups have undertaken measurements to evaluate the capture cross-sections for electrons and holes σ_n, σ_p. However, as the interface is strongly fabrication dependent, one can find several references in literature.
Basic work on the Si/SiO_2 interface was conducted by Nicollian and Goetzberger [96], who state numbers still used up to now on capture cross-sections (e.g. Becker et al. [97] used $\sigma = 2.5 \cdot 10^{-16} cm^2$, based on Nicollian and Brews [33]). Depending on crystal axis orientation and fabrication, σ_p, σ_n span the range of $[2 \cdot 10^{-17} cm^2, 2 \cdot 10^{-14} cm^2]$.
Jupina and Lenahan [98] studied the effect of radiation induced traps at the interface and used for an effective capture cross-section $\sigma = 4 \cdot 10^{-16} cm^2$ for a MOSFET operated as a gate controlled diode.
Saks [99] measured $\sigma_n = 1.25 \cdot 10^{-16} cm^2$ and $\sigma_p = 1.5 \cdot 10^{-16} cm^2$ with charge-pumping on low interface trap devices. Previously, Saks and Ancona [100] showed measurements, where they extracted $\sigma_p \approx 1 \cdot 10^{-16} cm^2$ and a rather large range for $\sigma_n \approx [3 \cdot 10^{-15} cm^2, 1 \cdot 10^{-13} cm^2]$. However, they claim that this value seems unrealistically large and may be based on a single set of devices rather than a "typical" device.
A more recent work was conducted by Lenahan et al. [101], with a focus on the capture cross-section of P_{b_1} in comparison to P_{b_0}. Both types showed a realistic behavior of the effective $\sigma \approx 1 \cdot 10^{-16} cm^2$.
Table 6.2 summarizes the different cross-sections. It is clear that from such a wide range of

Author	Year	Reference	σ_n (cm^2)	σ_p (cm^2)	σ (cm^2)
Nicollian and Goetzberger	1967	[96]	$2 \cdot 10^{-14}$	$2 \cdot 10^{-17}$	$2 \cdot 10^{-17}$
Becker et al.	2000	[97]			$2.5 \cdot 10^{-16}$
Nicollian and Brews	1982	[33]			e.g. $2.5 \cdot 10^{-16}$
Jupina and Lenahan	1989	[98]			$4 \cdot 10^{-17}$
Saks	1997	[99]	$1.25 \cdot 10^{-16}$	$1.5 \cdot 10^{-16}$	
Saks and Ancona	1990	[100]	$\approx 10^{-15} - 10^{-13}$	$1 \cdot 10^{-16}$	
Lenahan et al.	2002	[101]			$1 \cdot 10^{-16}$

Table 6.2.: Summary of capture cross-sections for electrons and holes in literature. The range of the parameters varies heavily in publications.

capture cross-sections the error on D_{it} from equation 6.21 cannot be determined satisfiably. Therefore for the device the cross-section independent surface velocity s_g and the surface current density per area j_S will be stated. From the current density it is only a small step to the relevant noise contributions of depleted surfaces of the DEPFET during operation.

Avalanche Injection at High Gate Voltages

In section 3.5 the shape of the current vs. gate voltage was explained. However, in measured data, e.g. figure 6.18, a difference to a "typical" curve (figure 3.16) can be seen.
Beginning with accumulation (positive voltage) there is a visible decrease from a high current, which is already more than the surface generated current I_S. This is attributed to an avalanche breakthrough at the $p+$ contact, indicated in figure 6.19. Especially at the edge

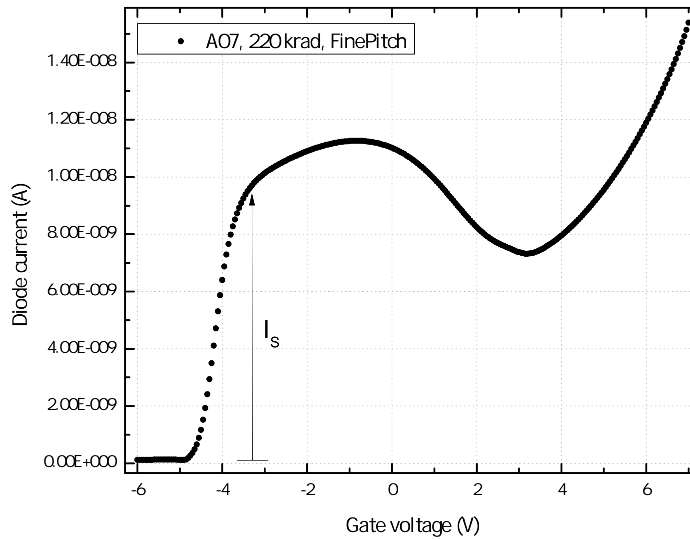


Figure 6.18.: Avalanche breakthrough visible in accumulation in the diode current of a GCD. Extraction of I_J is disputable with such a device. However, extraction of I_S is possible.

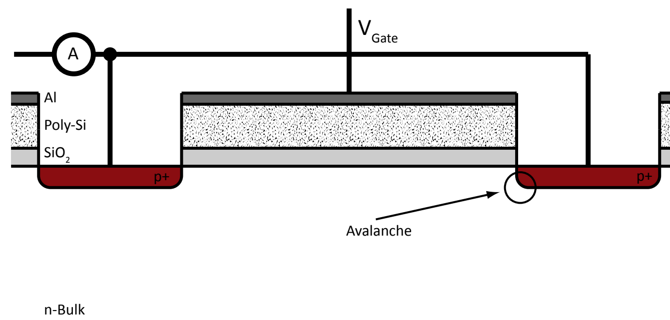


Figure 6.19.: Cross-section of a GCD through gate branches. The potential difference between the bulk and the $p+$ contact may lead to an avalanche breakthrough. With high positive gate voltages charge carriers below the insulator are located on a higher potential and break through more easily.

of the implantation high electric fields may arise, which lead to an increase in current. At this location the potential of charge carriers beneath the gate contact correspond to the applied gate voltage. The potential difference leads to a high band bending in the semiconductor, thus charge multiplication via impact ionization takes place.
Analysis of I_J in accumulation from devices which exhibit such a behavior is difficult and in this work the analysis is limited to the current I_S, which can still be extracted at the onset of inversion.

6.3.2. Measurement Procedure

The diode, consisting of the n bulk and the $p+$ regions, is biased in reverse. The gate voltage is controlled from accumulation into inversion. Appropriate biasing of guard rings into accumulation and the p guard (ring) into reverse bias ensures a definite area/volume

from which the current measured in the GCD is drawn. Figure 6.20 shows a schematic illustration of this procedure. The gate, bulk, $p+$ outer ring, and $p+$ contact were connected

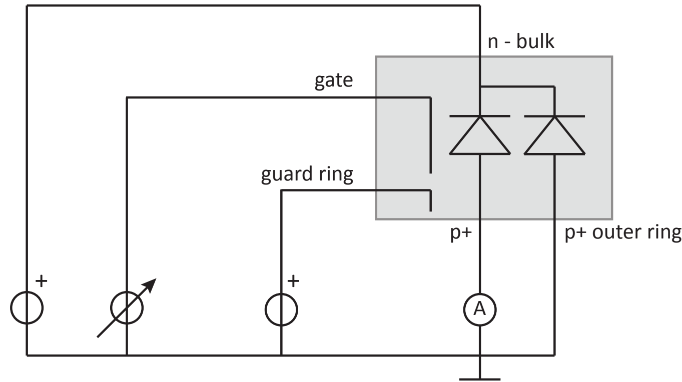


Figure 6.20.: Schematic illustration of the GCD measurements procedure. The outer diode ($p+$ outer ring) together with the guard ring ensures a definite volume of the GCD, while the contact at the bulk is biased in reverse. The ammeter measures the current due to a sweep in the gate voltage.

to a Keithley 4200-SCS with a pre-amplified current measurement for the reverse diode current. The guard ring contact was biased using a Toellner TOE-8842 power supply.
An overview of the GCD devices, their biasing and properties[4] is given in section D.1.

6.3.3. Results and Discussion

The devices in this study were measured with a reverse bias of 2 V to 4 V. An exemplary plot of reverse diode current vs. gate voltage can be seen in figure 6.21.

From this data the surface generated current is extracted and the surface velocity s_g is calculated. Figure 6.22 shows a first observation regarding s_g, which is proportional to the interface trap density (equation 6.21).

Surface Generated Current and Gate Area

The surface generated current should behave in a proportional way to the gate area of the GCD according to equation 3.51. However, the data shown in figure 6.23 indicates that although the gate area of the coarse pitch devices of $A_{coarse} \approx 8.055 \cdot 10^{-2} cm^2$ is nearly twice as large as $A_{fine} \approx 4.055 \cdot 10^{-2} cm^2$ the surface current does not scale with the area.

A possible explanation of this behavior is based on the fact that between the $p+$ strips no electrical drift field is present (cf. figure 6.19 and figure 3.18 for a cross-section of a GCD). Therefore the generated charge has to diffuse to the read-out strips. Along the lateral surface path of the diffusion current the charge carriers therein can be trapped by interface traps, thus preventing *new* generation of charge at this location.
At the edge of the gate strips the generated charge is removed via the potential of the $p+$ contact. This ensures continuous generation at the edges. In the middle of the gates the

[4]The J04 unirradiated data was accidentally overwritten and was copied from N05

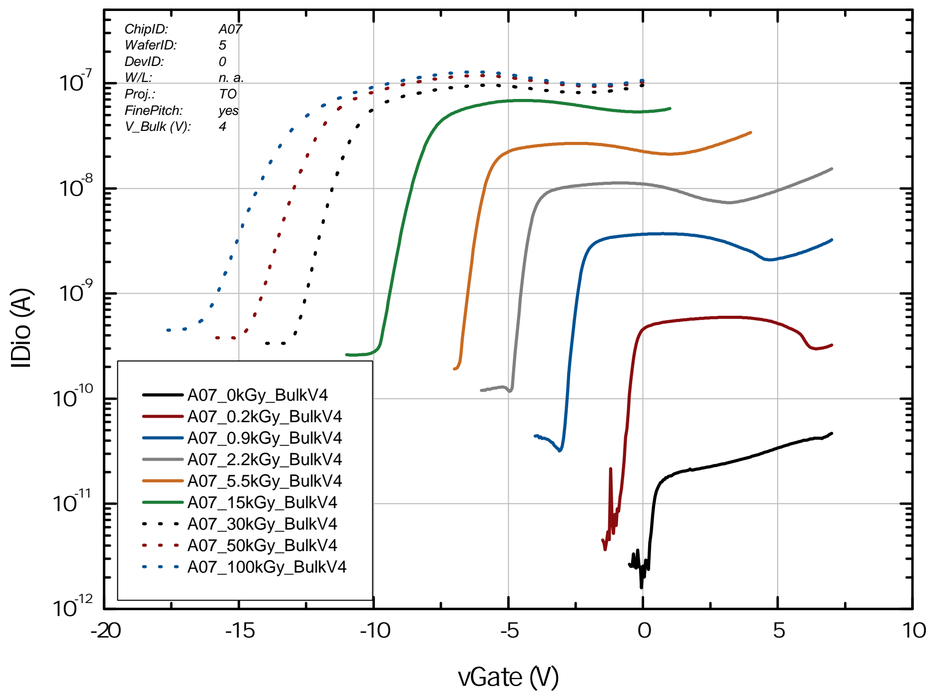
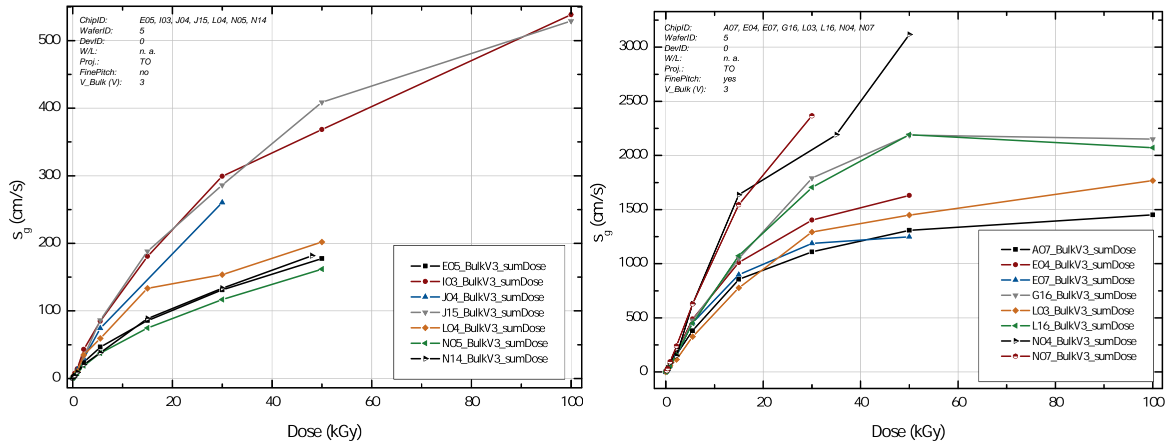


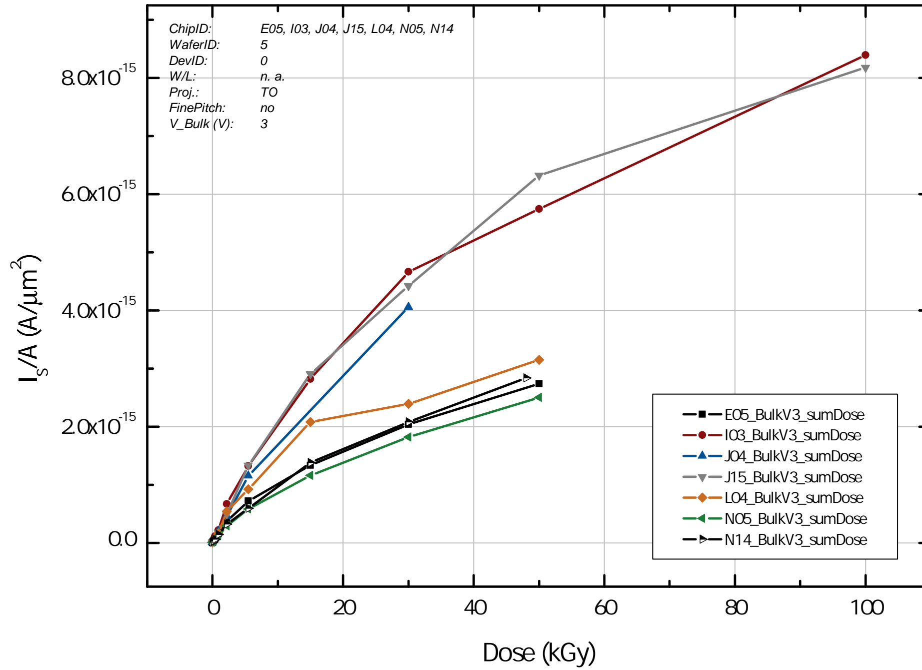
Figure 6.21.: Diode reverse current of the GCD from A07. Besides the increase in the surface generated current a shift in the gate voltage for the onset of depletion is also visible.



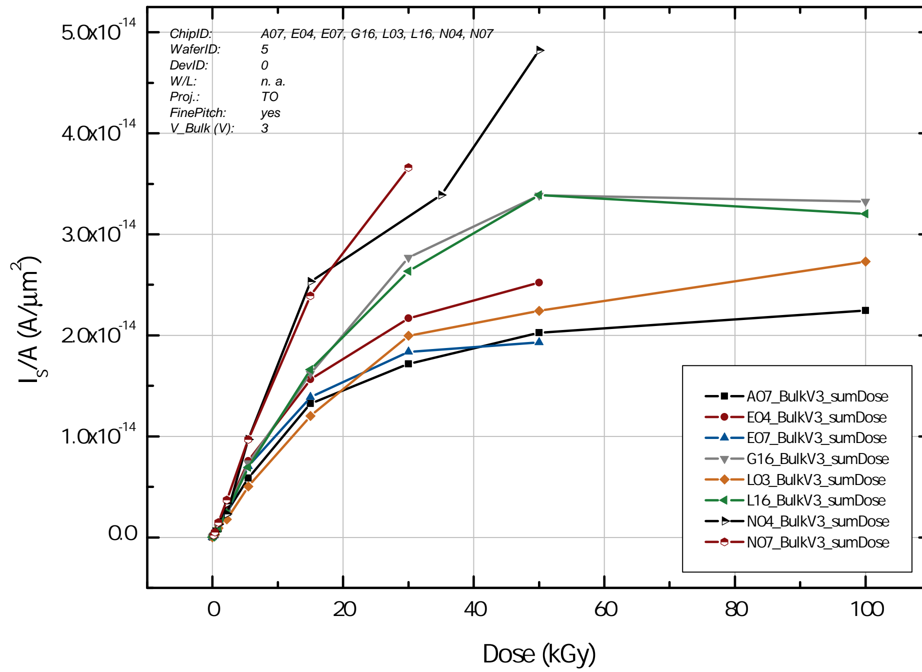
(a) These DUTs exhibit a **coarse** pitch between the diode strips. The gate area is larger than for the fine ribbon structure.

(b) GCDs with a **fine** pitch and ribbon structure between the $p+$ strips.

Figure 6.22.: Comparison of coarse and fine pitch GCDs. The measured surface current and therefore s_g is considerably larger in the fine pitch versions than in the DUTs with a coarser pitch.



(a) Reverse diode current density per unit area. The gate size of the coarse devices is considerably larger than that of the fine pitch devices.



(b) The reverse diode current density per unit area of the fine pitch GCDs.

Figure 6.23.: Comparison of surface generated currents between coarser and finer pitch GCDs.

charge is hardly removed. The smaller the gate strips are the better is the charge removal beyond the gate. In this sense the surface current I_S (and calculated properties thereof) from fine gate ribbon devices is more reliable than from coarser gate areas. Table 3.2 shows the difference in the two GCD layouts. From these parameters it is evident that from the fine strip version more surface current is measured.
In light of this argument, one has to be careful when relying on information from literature which disregards this aspect.

Behavior of Surface Current

In the presentation of $j_S = I_S/A$ in figure 6.23 several groups of data are visible. A concise explanation on this behavior is difficult. From the fine structured devices the GCDs of N04 and N07 show the most current. A look into the GCD properties in table D.1 reveals that theses devices exhibit the thinnest nitride thickness of 10 nm, although the biasing is different.
The GCDs from G16 and L16 depart from the rest for a dose > 30 kGy. They exhibit 60 nm, respectively 40 nm, of nitride and received the same biasing during irradiation. The remaining devices show considerably less current, however L03 exhibits also a 10 nm nitride thickness.
The overview regarding the coarse GCDs is similarly confusing. A group consisting of I03, J04, and J15 exhibits considerably more current density than the other devices. However the nitride thicknesses there is also mixed.
At this stage no clear explanation can be given on the different behavior of I_S. The DUTs studied in this work are too few to draw a concise conclusion. It well may be that a grouping visible in the figures of 6.23 here turns out to be a spread over all devices. In this sense further investigations which scan the available parameter space (biasing, dopings, nitride thicknesses, etc.) would be needed in order to formulate final statements.

Noise

The important figure of merit is the additional noise in the DEPFET one can expect after a certain point of irradiation. The CLG will be in depletion during operation in Belle II, thus the surface of this contact will be generation active. The area of one DEPFET pixel can be estimated from the layout. The design of a DEPFET from the production run PXD 6 is exemplary shown in figure 6.24. The CLG area of one DEPFET from this design is $A_{CLG} = 3.625 \cdot 10^{-6} cm^2$. Taking a conservative route in the calculation of noise one needs to use data extracted from a fine structured GCD since its gate width is comparable to the CLG. Exemplary the current density from A07 and N04 is used in the calculation. The result is shown in figure 6.25.

The temperature dependency of the surface generated current and (derived thereof its noise) is given by the dependency of the surface generation velocity of equation 3.55. Assuming the other factors besides T to be constant a change in the velocity due to a change in the vicinity of the room temperature of $293K$ (=20 $°C$) is negligible.

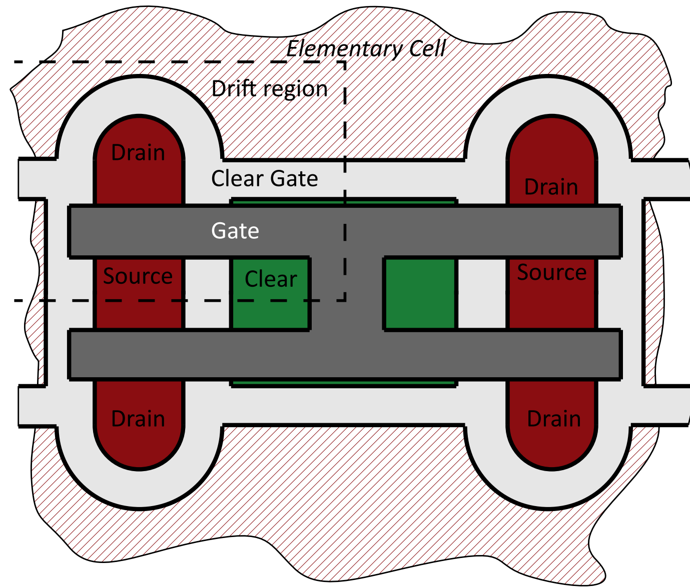


Figure 6.24.: Four DEPFETs from PXD 6. The dashed line indicates the "elementary" cell of one device.

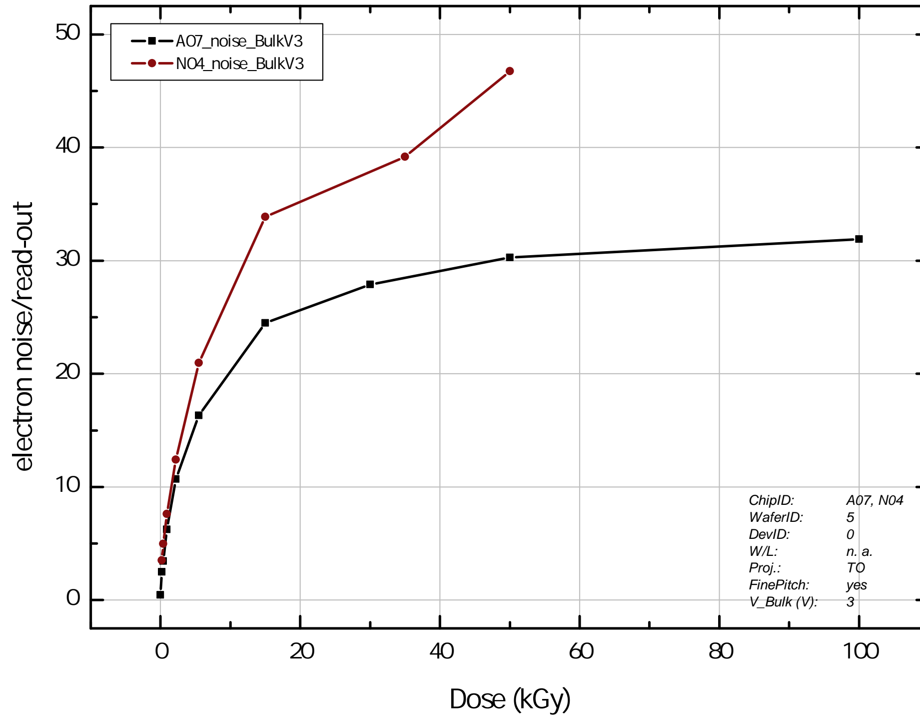


Figure 6.25.: Electron noise of fine structured GCDs during a read-out cycle of $t_{RO} = 20\ \mu s$.

6.4. Conclusions

Three different devices are used to study the interface trap distribution of the TO project. Measurements with MOSCAPs reveal detailed information about the distribution throughout the band gap although the measurement technique is quite complicated and time consuming. The measurements presented in this chapter confirmed the existence of a typical interface trap defect P_b to be present in the TO devices. Capacitors with nitride thicknesses of 40 nm and 60 nm showed a yet unconfirmed trap signal. From the data shown in section 6.1 it is clear that the major interface trap increase takes place slightly above the intrinsic level E_i, i.e. $0.1\ eV \lesssim \Phi_s \lesssim 0.35\ eV$.

MOSFETs on the other hand reveal impacts of interface traps directly on device parameters. Whereas the subthreshold swing is used to determine the change in interface trap density after irradiation, the transconductance g_m is an important parameter for the DEPFET, since the internal amplification g_q is proportional to g_m. The small improvement after low doses of the transconductance may be attributed to a buried channel behavior. However, this benefit is undone with increased scattering at the interface at higher doses. A decrease in g_m of $\approx 15\%$ has to be taken into account after 100 kGy for TO (or similar) devices[5].

The GCD technique usually offers a fast and clean access to interface traps. However, as this study revealed, the design of the device is especially important. Finer gate structures suffer less from diffusion effects under the gate strips and show considerably more surface generated current. Therefore the extraction of interface trap density has been omitted since such a statement would hardly be reliable. However, as the fine GCD structures are close to the intended Belle II DEPFET dimensions for the CLG, the surface current from such devices is used to estimate the additional noise one can expect due to interface traps in the internal gate. Depending on the electric field in the insulator of the CLG more or less noise is created by the generation active defects. After 50 kGy a typical noise contribution ranges from 30 e^- up to 47 e^- per read-out cycle.

[5] depending on nitride thickness and biasing during irradiation

Chapter 7.

Experiments on Oxide Damage

During the operation of Belle II several background radiation processes (cf. section 2.4) generate ehps in the insulation layer of the gate and the clear gate of the DEPFET. One of the main processes taking place is the trapping of holes in silicon dioxide. Due to their low mobility the generated holes remain as trapped oxide charge Q_{ox} in the insulator, especially located very close to the SiO_2/Si interface (see also section 4.2 for a more in-depth discussion of the radiation damage process).
The crucial effect in which Q_{ox} manifests on device level is the shift of threshold voltage V_{th} in the DEPFET. In this way, the clear gate is treated similarly to a transistor's gate although it is not operated in the sense of a classical MOSFET.
These shifts in the PXD will have to be adjusted during the operation of Belle II in order to ensure a proper operation point of the DEPFET. For a safer operation in the experiment several design options, i.e. type of oxide and the amount of silicon nitride, are investigated to minimize the effects of the shift in the threshold voltages.
The investigations in this chapter focus on the device behavior itself. Effects which arise due to an inhomogeneous irradiation of the PXD are covered in section 10.2.

7.1. Introduction

The trapped oxide charge (mostly due to E' center defects) shifts the reference level of the MOS interface. The investigation is therefore split into the two parts of the DEPFET, namely gate and clear gate.
The shifts of these reference levels are affected by design and production issues, i.e. type of oxidation and the amount of silicon nitride. These levels are synonymously referred to as threshold voltage V_{th} since MOSFETs, which are equivalent to the gate and clear gate, are used as DUTs.

7.1.1. Influence of Gate Voltage Shifts

The gate voltage of each ladder of the PXD is connected to the DEPFET matrix via Switchers. Each Switcher is supplied with a gate-on and a gate-off voltage. During the lifetime of Belle II those voltages have to be adjusted continuously or at least in reasonable intervals, due to the ionizing radiation induced shift in V_{th}. The adaption ensures a proper conduction and off-state of the connected DEPFET matrix part.
The upper limit on these switching voltages is given by the voltage tolerance of the Switcher which is $\sim 20\ V$. As already mentioned, DEPFETs from previous productions utilized thick oxides and therefore exhibited high shifts in the threshold voltage ΔV_{th} (cf. also section 4.2.3). With these devices the operation with Switchers would have become difficult. One

aim in this study therefore is a parameter scan of available design/production options (cf. section 7.1.3) of the DEPFET in order to stay well below this hard limit.

7.1.2. Influence of Clear Gate Voltage Shifts

The issue with accumulated charge in the CLG is different from the abovementioned shifts in the gate threshold voltage. The bulk beneath the clear gate (when operated with appropriate bias) acts as a barrier for signal electrons in the bulk of the DEPFET and for the electron reservoir in the clear.
The height of the barrier is controlled by the clear gate voltage. The behavior of the DEPFET during charge collection mode and clear mode is influenced amongst others also by the clear voltage. A detailed discussion can be found in e.g. [102, 39].
If the potential of the clear gate is too negative, accumulation of holes occurs, leading to a parasitic channel between drain and source, while the "normal" channel below the gate is still switched off. Besides the issue of a wrong signal detection, the current flowing beneath the clear gate might be, due to the large "width" of the CLG, so high that the amplifying and digitizing circuits next in the read-out line get overloaded.
On the other hand, while the barrier is too low due to a more positive voltage at the clear gate, electrons are not separated anymore between the bulk of the DEPFET and the clear region. Depending on the clear voltage, signal charge from the bulk can either disappear into the clear, or electrons from the clear are emitted into the bulk and are treated as signal charge (so-called *back emission*).
The barrier height can be treated as a certain reference voltage of the CLG transistor, such that Q_{ox} leads to a shift in this voltage. As the reference level can be chosen freely, a good value is the threshold voltage of this transistor. In this study, clear gate equivalent transistors were investigated and the shift in the measured V_{th} should be interpreted to the effects mentioned above.
Another issue are intra-pixel variations. The amount of oxide trapped charge depends on the electric field over the insulator and the CLG exhibits several interfaces to neighboring potentials. Figure 7.13 shows an illustration of a possible DEPFET design with relevant voltages. Due to the various cross-sections along the CLG region, parts of a pixel are stronger affected by radiation than others. E.g. the region to the drift is exposed to more damage than the region to the source. Thus, given the abovementioned effects and one common clear gate voltage, the barrier in one region is too high and on another one it is too low. Finding a common operation point for the CLG voltage is not a trivial task. Determining device/design parameters which ensure minimal differences in ΔV_{th} along the pixel for such a common voltage is one goal of this study.

7.1.3. Design/Production Options for the DEPFET

The two design options for the DEPFET production for Belle II studied for this work are:

1. the thickness of a silicon nitride layer deposited on top of the silicon dioxide layer and

2. the type of SiO_2 to be used in the production of the DEPFET.

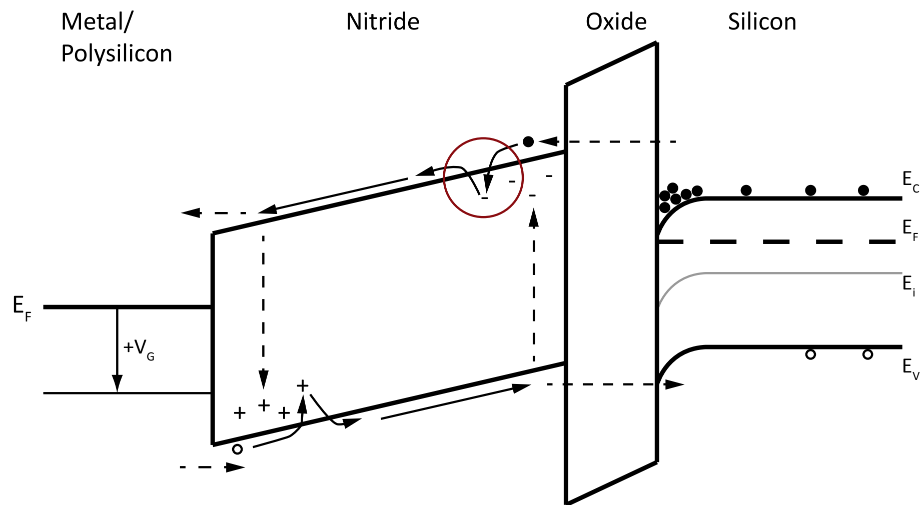
Nitride Layer

The effect of an additional nitride layer on the radiation hardness was investigated first by Newman and Wegener [103] with Metal-Nitride-Oxide-Semiconductor (MNOS) devices. There, an improvement in comparison to pure MOS devices was observed, i.e. a smaller shift in V_{th} with respect to dose. Ionizing radiation creates ehps in silicon nitride as well as it does in the oxide or silicon bulk. For it is an insulator, charge transport in the silicon nitride is suppressed. Conduction through the nitride (of $\sim 20 - 70$ nm thickness) is controlled by trapped charge therein (cf. figure 7.1 for a graphical representation). The rate of ionization of those traps determines the "current flow" across the insulator. The electric field over the insulator facilitates the Frenkel-Poole emission of a trapped charge by lowering the barrier on one side along the field of the Coulomb trap, making a tunneling process of the trapped charge more likely (cf. figure 7.1b). This model is generally accepted. However, other models which are based on phonon assisted processes may also be valid (e.g. in [104]).

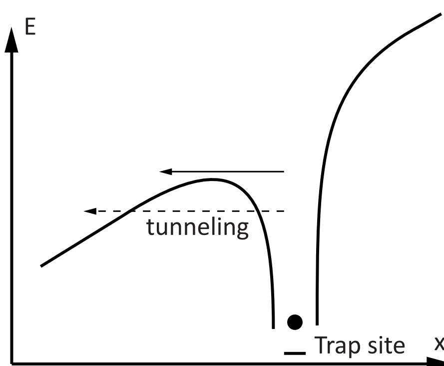
The migration of a charge is stopped until a (meta-) stable defect is reached. Studies concerning the influence of those additional traps onto radiation hardness of MNOS devices were done e.g. by Cricchi and Barbe [105]. At the nitride-oxide interface a small barrier exists, leading to a halt in the "conduction" of charge carriers through the insulators. Due to this stop, trapping at defect sites sitting close to the oxide-nitride barrier is more likely.
Traps in silicon nitride have several possible energy locations. Krick et al. [106] showed that a typical defect in silicon nitride acts similarly to a DB defect in silicon. Thus its charge can be +/0/-, depending on occupation. In addition, no crystal reorganization takes place in the insulator when altering the charge state of the defect. The properties of this defect are subjected amongst others to the growth conditions during production of the semiconductor devices, e.g. such as the temperature during the deposition of silicon nitride ([107]).
As charge carriers can enter the nitride in various ways, the trap distribution and especially the occupation of traps depend on the nitride layer thickness ([108, 109]).
A trivial prediction of the behavior of an MNOS structure to radiation exposure cannot be given, since some of the traps in the silicon nitride are of amphoteric nature and the charge state of traps depends also on thickness. Thus detailed investigations with devices which exhibit a layout as close as possible to the desired devices are necessary.
Takahashi et al. [110] have shown that it is possible to achieve a zero threshold voltage shift with respect to ionizing dose with an MNOS structure of appropriate thicknesses. In their study they utilized a slanting etching method for device manufacturing, making a vast amount of the silicon nitride thickness parameter space accessible. Positive charges in the oxide were "canceled" by electron traps in the silicon nitride.
However, such a zero shift condition occurs only at a certain dose value; for the DEPFETs in the final experiment an overall smaller shift of the threshold voltage is desirable. In order to investigate this issue, several devices with different nitride layer thicknesses are studied. Yet, the deposition of silicon nitride is not always advantageous. Jin et al. [111] have shown that the recombination rate of the typical P_b interface trap increased after a LPCVD of silicon nitride, which increases the noise due to higher surface generated currents (cf. section 6.3.3).

Silicon Dioxide Type

The influences of different types of silicon dioxide shall here be mentioned only briefly and for the sake of completeness, as an in-depth discussion of this matter can be found in the



(a)
Graphical representation of an MNOS structure. The positive voltage $+V_G$ on the gate sets the structure into accumulation. The electric field assisted emission of traps is indicated by the red circle, a close-up thereof is shown in in figure 7.1b.



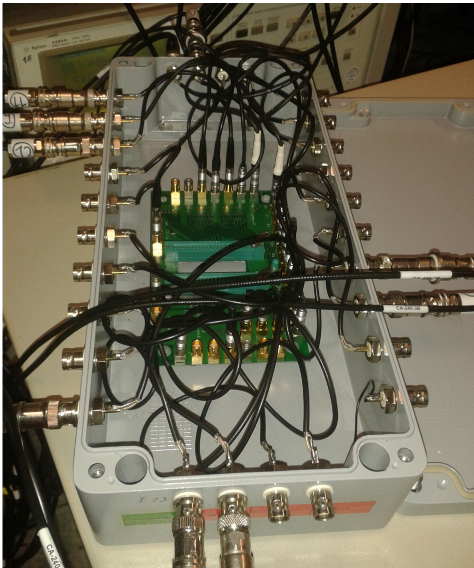
(b)
Frenkel-Poole emission of a trapped charge carrier. The lowering of the barrier on one side due to the electric field facilitates this process.

Figure 7.1.: Conduction through silicon nitride, after [104].

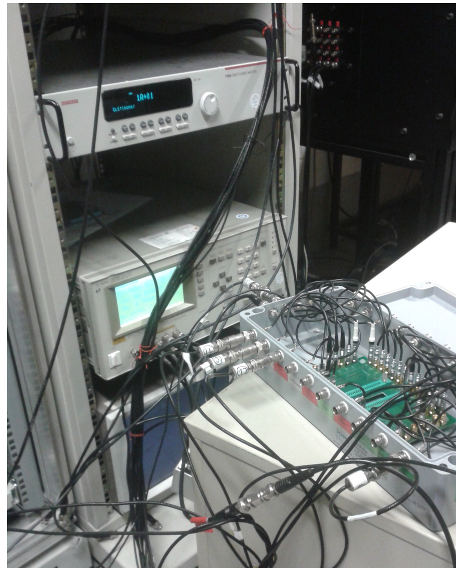
earlier sections 3.6.1 and 4.2.4. Most of this work concentrates on devices from the TO production, where a dry oxidation process was used. However, some devices from the PXD 6 production, fabricated with a wet oxidation process, were also studied.

7.2. Measurement Methods for the Threshold Voltage

The extraction of the threshold voltage V_{th} can be performed both in the linear mode and in saturation (cf. section 3.3.4). Both methods rely on the input characteristic data of $I_{DS}(V_G)$, i.e. the drain-source current and the gate voltage.
Voltage and current were measured with a Keithley 4200 SCS in combination with a switching matrix card mainframe Keithley 708B and an installed semiconductor matrix card of type 7072. The semiconductor chip with the various transistors was attached to a ceramic carrier, which was then placed into a Zero Force Injection (ZIF) socket on a Printed Circuit Board (PCB).
From this board Lemo 00 connectors enabled the use of small coaxial cables to Bayonet Neill Concelman (BNC) connectors, which are located outside the measuring box. The box provides additional electrical shielding as well as the shielding from light which would otherwise alter the measurement. The BNC connectors of the box were attached via adapters to Triax cables to the abovementioned measurement equipment. Figure 7.2 shows pictures of the measurement setup.
X-ray irradiations of the devices were conducted at the Karlruhe Irradiation Center (cf. appendix A.1).



(a) Measurement box. In the center the DUT can be inserted into a ZIF socket. Lemo 00 cables are attached to the BNC adapters in order to provide access from outside the box.



(b) Measurement setup. On the bottom of the rack is the Keithley 4200 SCS, above of it is the LCR meter and on the top side the matrix card with its mainframe.

Figure 7.2.: Measurement setup in the laboratory of the HLL. During irradiation campaigns the setup was transported to the sites of the radiation facilities.

7.2.1. Saturation Mode

The threshold voltage in saturation is given by equations 3.33 and 3.34. In the experiment the drain-source current I_{DS} is measured with respect to the gate voltage V_G. The MOSFET is hereby operated in saturation mode, i.e. with an applied drain voltage of $V_D = -5\ V$.
If the square root of the current $\sqrt{I_{DS}}$ is now plotted against V_G a linear relationship can be observed (see equation 3.34). A linear fit into this region reveals the threshold voltage in saturation $V_{th_{sat}}$ at the intersection with the V_G axis. A more detailed description is presented in the appendix B.2.1.

7.2.2. Linear Mode

The extraction of the threshold voltage in the linear region has some advantages over the aforementioned extraction in saturation. E.g. the change in channel length due to the pinch-off point location and short-channel effects such as DIBL (section 3.3.5) can be neglected. Only a moderate drain bias is applied, i.e. in most cases $V_D = -0.5\ V$. The drain current I_{DS} is measured with respect to the gate voltage V_G. In the data from the derivation

$$g_{m_{lin}} = \frac{\partial I_{DS}}{\partial V_G} \tag{7.1}$$

a maximum can be observed. A tangent to this data point in the input characteristic indicates the threshold voltage V'_{th} at the intersection of the V_G axis. This value has to be modified with the applied drain voltage V_D in order to determine the threshold voltage in linear mode

$$V_{th_{lin}} = V'_{th} - 1/2 \cdot V_D. \tag{7.2}$$

This method is also known as Extrapolation in the Linear Region (ELR) [36]. More details on this method can be found in the appendix B.2.2.

7.2.3. DUT Description

Layout of TO Devices

Production of DEPFETs can be quite time consuming due to the vast amount of production steps, such as implantations, wafer bonding and thinning. Therefore special test structures were developed to avoid those obstacles. In addition, the concentration on test structures allowed parameter variations like nitride thickness, gate length, GCD pitch, etc.
Each chip of the TO-production is identified by a unique number. In table B.1 additional information on MOSFET types is given. A typical layout is shown in figure 7.3. The chip is roughly 6 x 6 mm^2 in size and bonded to a 40 pin ceramic carrier.

Layout of PXD 6 Devices

Test structures from the PXD 6 production run differ from those from the TO project. E.g. they exhibit an additional polysilicon layer but no common biasing contacts or embedded test structures such as MOSCAPs or GCDs. This results in a non-trivial attaching of bond wires to the structures, nevertheless representative devices are accessible. In figure 7.4 a layout of the PXD 6 chips is presented.

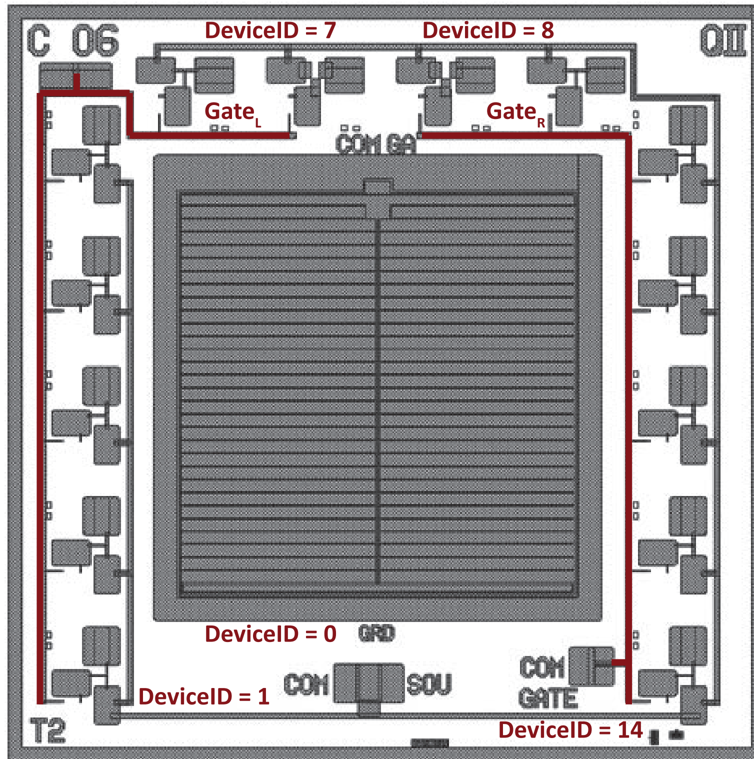


Figure 7.3.: Layout of a typical TO chip. 14 MOSFETs surround a central device, like a GCD (here) or a capacitor. Each side (L/R) of the chip can be biased with a common gate contact.

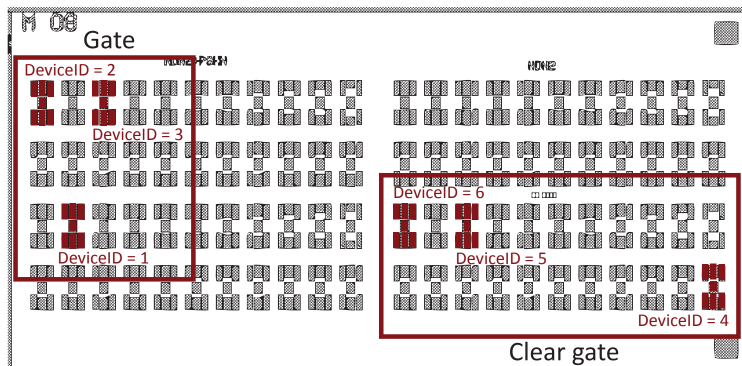


Figure 7.4.: Layout of PXD 6 test structures. In contrast to TO devices no common gate contacts are present. MOSFETs which are usually selected are designated in red.

7.3. Threshold Voltage Shift Studies for the Gate

7.3.1. Biasing Schemes for the Gate

During the Belle II experiment the DEPFETs will be most of the time in an off state. Only for read-out purposes the channel in the transistors will be switched on. This results in a duty cycle D of

$$D = \frac{t_{on}}{t_{off}} = \frac{100\ ns}{19.9\ \mu s} \approx 0.5\%. \tag{7.3}$$

Therefore the DUTs in this study were irradiated only in the off state.
The gate voltage during operation of Belle II has to fulfill several requirements. E.g. the channel has to be clearly shut off during disuse in order to minimize power dissipation. Therefore a positive voltage at the gate is needed, as the threshold voltage of DEPFETs is typically at $\sim 0\ V$. However, as the radiation damage accumulates in the device, V_{th} is shifted to negative voltages. Thus an adaption is possible to reduce the gate voltage. When stopping the adaption process at $V_G = 0\ V$ an optimal scenario of preventing further radiation damage may be achieved (cf. section 9.3).
In this study the gate devices were irradiated with a fixed gate potential of $V_G = +2\ V$ and with an adaptive mode (called *gate adaptive* or *intelligent bias*). In this mode the irradiation starts also with $+2\ V$ at the beginning (i.e. $0\ kGy$) but then the gate voltage is adapted according to the (estimated) threshold voltage shift of each dose step. At the dose step in which the voltage would have to be set to negative values the adaption is stopped and V_G is set to zero volt. Figure 7.5 illustrates this issue.

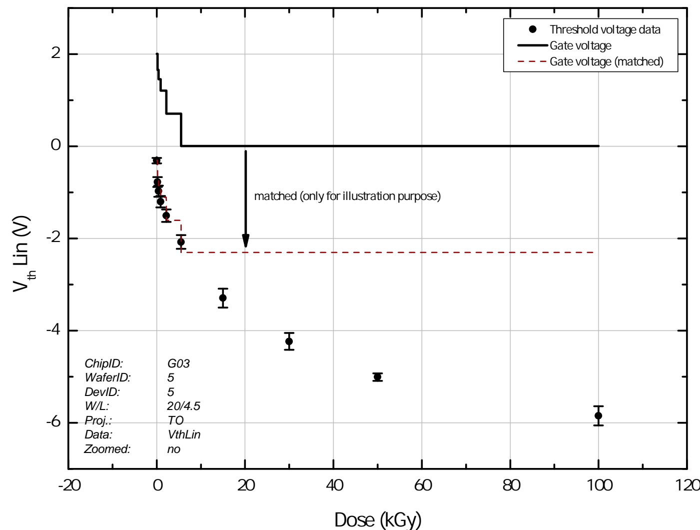


Figure 7.5.: Gate adaptive mode of V_G during irradiation. The adaption is stopped at zero volt. Since the threshold voltage could not be extracted during irradiation campaigns thoroughly the adaption had to be done to an estimated value. The red dashed line shows that this method is quite successful.

Another issue, which is only mentioned briefly in this work, is the study of the so-called *gated mode* of the DEPFET. During the injection of charge into the rings of SuperKEKB some of the newly injected charges are off-orbit. This results in a continuous loss of particles,

in which the bunches are damped further and further (also called cooling) the longer the charges stay in the rings. However, collisions and trespassing of such noisy bunches results in an undetermined amount of charge in the internal gate of the DEPFETs. The off-orbit particles may hit the beam pipe, collimators, etc. and can hereby generate electromagnetic showers. This background interferes with the normal charge collection mode of the DEPFET. The solution is to blind the internal gate for the trespassing time of those noisy bunches. As the internal gate potential follows the external gate voltage, the potential minimum for electrons in the DEPFET bulk can be located on a higher level. Thus the already stored electrons from good events would have to overcome a higher barrier to reach the clear. In addition the alternative electrode, i.e. the clear, is made more attractive with a more positive voltage than usual, i.e. by applying the $V_{clear_{HI}}$ voltage, which is usually applied for the clear process during read-out. This results in a charge removal of electrons from the bulk but leaves the stored charge in the internal gate from previous (good) collisions unaffected. Therefore a study was necessary which focussed on higher gate voltages than normal (cf. section 7.3.2). Further reading on this issue can be found e.g. in [112, 113].

7.3.2. Measurements and Results

Influence of Nitride Thickness

In the frame of the TO project several nitride thicknesses were deposited on top of the thin SiO_2. The influence of the various thicknesses is shown in figure 7.6. From this data a better performance for thin nitride thicknesses can be observed. A lower shift in V_{th} can be expected due to a higher gate capacitance, additionally the amount of oxide charge is smaller[1] as one can see in table 7.1. The irradiation was performed with a fixed gate bias of $V_G = +2\ V$, simulating an off state of the DEPFET.

ChipID	DoseMax kGy	$\sim \Delta V_{th}$ V	t_{ox} nm	t_{ni} nm	Sheet Capacitance F/cm^2	Sheet charge Q_{ox} C/cm^2
L03	100	3.6	85	10	$3.83 \cdot 10^{-8}$	$1.38 \cdot 10^{-7}$
G03	100	5.1	85	20	$3.62 \cdot 10^{-8}$	$1.85 \cdot 10^{-7}$
L16	100	8.8	85	40	$3.26 \cdot 10^{-8}$	$2.87 \cdot 10^{-7}$
G16	100	9.4	85	60	$2.97 \cdot 10^{-8}$	$2.79 \cdot 10^{-7}$
12U	100	8	90	30	$3.27 \cdot 10^{-8}$	$2.61 \cdot 10^{-7}$

Table 7.1.: Comparison between threshold voltage shift at the dose maximum and resulting oxide charge.

Figure 7.7 shows an irradiation of PXD 6 structures with a fixed gate voltage of $V_G = +2\ V$. The DUT 12U on wafer 12 was produced utilizing a dry oxidation process. The oxide of 12U exhibits a thickness of $t_{ox} = 90\ nm$ which is only marginally thicker than the $t_{ox} = 85\ nm$ of TO devices. Together with the already quite thick nitride layer of $t_{ni} = 30\ nm$ a $\Delta V_{th} \approx 8\ V$ can be observed after 100 kGy. This is close to the value from TO devices (figure 7.8) which exhibit shifts of 8.8 V and 9.4 V for 40 nm and 60 nm.
From this data a small nitride layer is favored in terms of low threshold voltage shifts. Taking

[1] Hereby only the projection of the charge to the SiO_2/Si interface is taken into account. No spatial information is extracted.

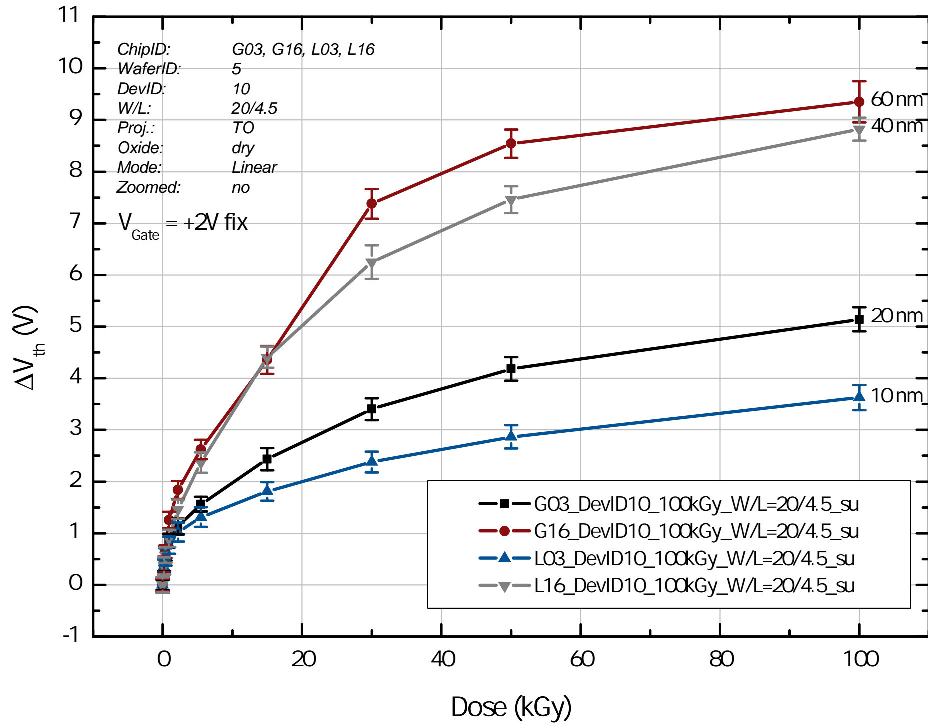


Figure 7.6.: Threshold voltage shift with respect to dose for TO devices. The data originates from DUTs whose gate lengths $L = 4.5\ \mu m$ are close to the final production value for the PXD. The smaller the nitride thickness, the better the performance to ionizing radiation.

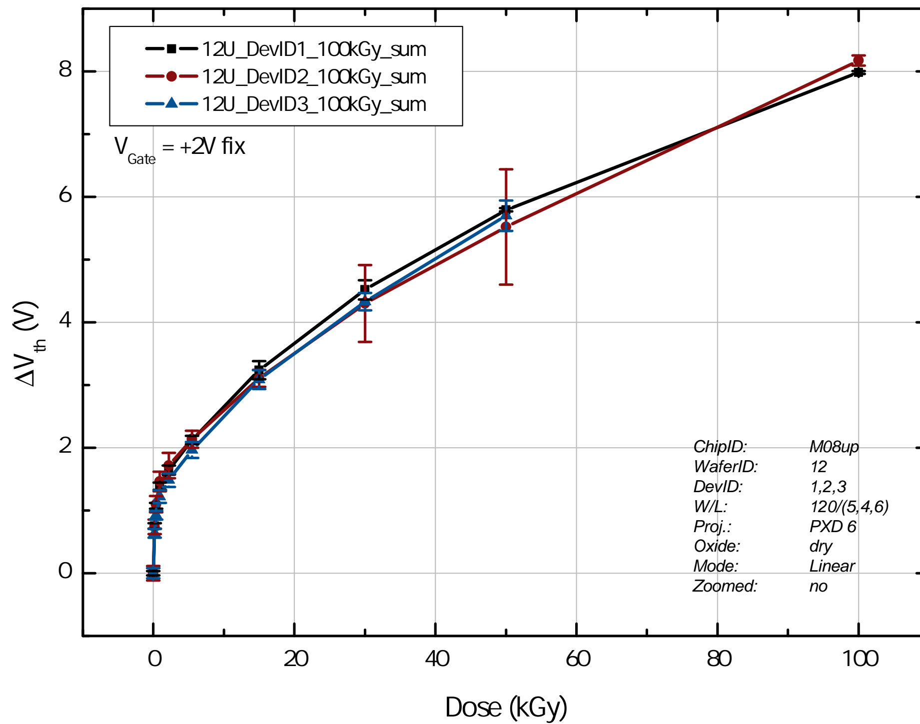


Figure 7.7.: Threshold voltage shift of three test structure from PXD 6. The wafer of this DUT exhibits a dry oxide.

the changes of the gate capacitance into account, a smaller (net) amount of charge is trapped in the insulator (see table 7.1).
A slight drawback in the interpretation of the data are the different production methods of the TO and PXD 6 project. In the TO project the oxide was already produced to its nominal thickness, while for the PXD 6 production an initially thicker oxide was grown which was then thinned down later. Also the nitride layer in the TO production was deposited twice except for the 10 nm thickness, while at PXD 6 only a single deposition took place. As aforementioned, the production steps may have a considerable impact on radiation hardness, so that the devices must not generally be compared. However, the data listed in table 7.1 indicates a good agreement on the issue of nitride thickness influence.

Influence of Gate Bias

The gate bias has to be adapted in the Belle II experiment (cf. section 7.3.1), therefore a gate adaptive biasing scenario was conducted during irradiation experiments. Figure 7.8 shows the effect of this biasing method on the threshold voltage shift with reference to $V_G(0\ kGy) = +2\ V$.

Figure 7.8.: Comparison between a fixed gate bias and a gate adaptive biasing scenario. For each nitride thickness with a fixed gate bias the corresponding DUT shows a larger shift in V_{th}.

From this data it is clear that this adaption mode has a negative effect with respect to device performance in a radiation environment. However, the effect is small and for devices with a 10 nm or 20 nm nitride thickness the effect is in the order of $\sim 0.5\ V$. Only for devices which already exhibit large shifts, i.e. 40 nm and 60 nm, the effect is considerably

higher.

The influence of the gated mode on the transistor performance was studied with the DUT 06U from the PXD 6 production. It exhibits a wet oxide and was irradiated with a gate voltage of $V_G = +5\ V$ which was then sequentially lowered to zero volts (cf. section 7.3.1). The shift of V_{th} with respect to dose is shown in figure 7.9a. After 100 kGy the threshold voltage was shifted by $\sim 7.3\ V$.
In this way, the gate adaption mode shows a worse performance in case of radiation hardness than with a fixed gate potential of $+2\ V$, as can be seen in the comparison of figure 7.9b.

Clearly, a lower threshold voltage shift with respect to dose would be in favor. However, the trade-off is between a moderate increase in the radiation induced threshold voltage shift and a considerably long dead time in the order of 20 % for the detector during trespassing of noisy bunches ([114]). Thus, figure 7.9a shows a realistic estimation of the threshold voltage shift with respect to dose which one can assume for the DEPFETs in Belle II.

Influence of Oxide Type

The choice of the oxidation method during production influences the radiation hardness of a device considerably. Therefore test devices from the production run PXD 6 which exhibit a wet oxide were subjected to X-ray irradiation. The shift in threshold voltage was determined after certain dose steps. In figure 7.10 a performance of such a device is shown.

This device also exhibits a nitride thickness of 30 nm but shows considerably lower voltage shifts than devices from a dry oxidation process (compare table 7.1). As aforementioned, production processes influence the radiation hardness. However, in figure 7.11 a comparison of two DUTs of the PXD 6 production, which share most of the production steps, is shown. A lower shift due to X-ray irradiation can be observed for the wet oxidation process.

In figure 7.12 several devices are compared to each other:

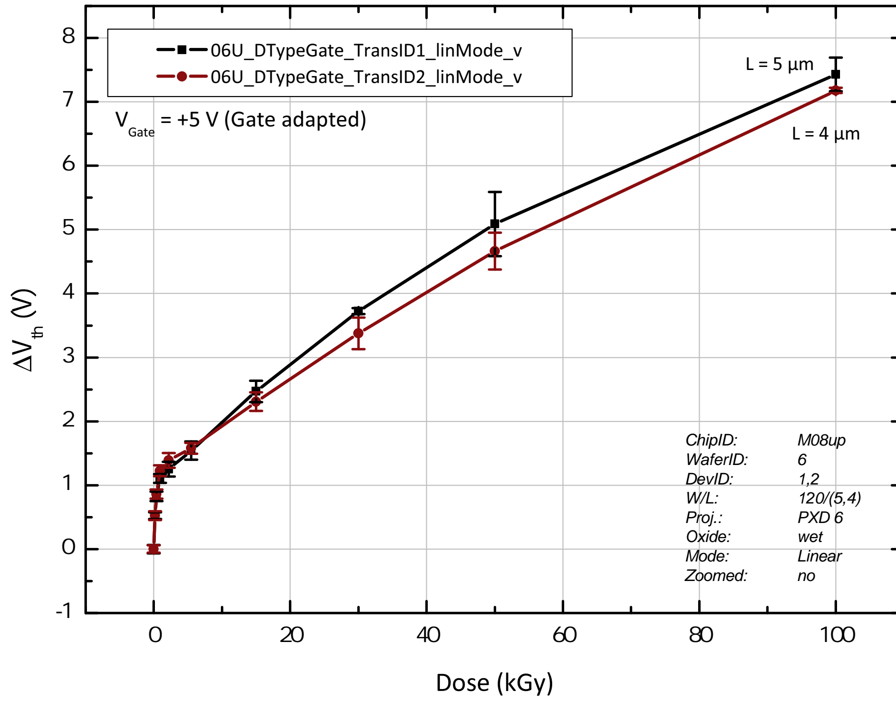
1. Dry oxidation data with a focus on nitride thickness variation from the TO project.

2. PXD 6 data from a dry oxidation process (DUT 12U).

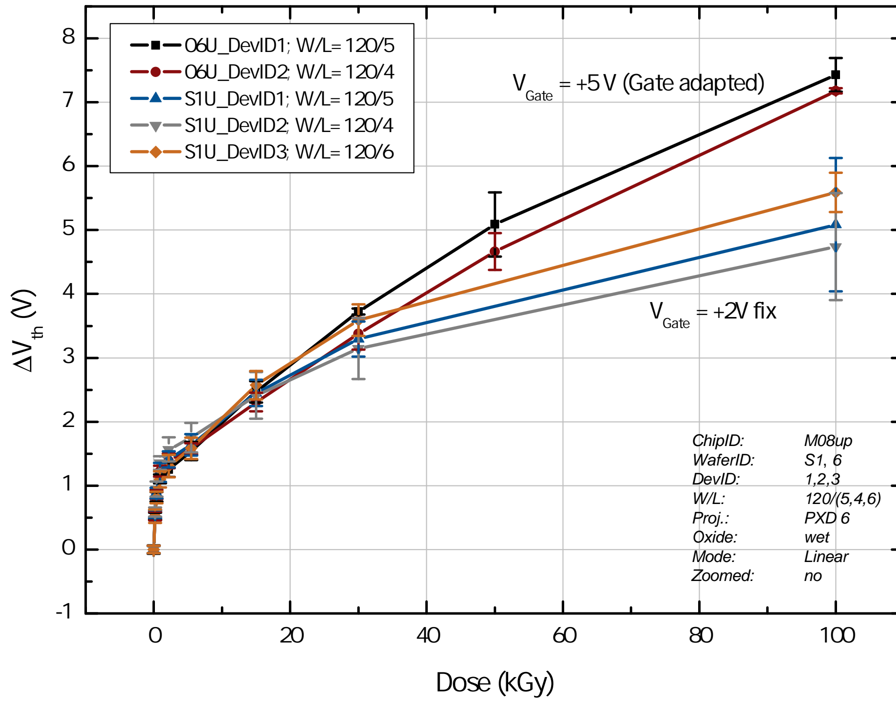
3. Wet oxidation data of the device S1U from the PXD 6 production.

While the dry oxidation device from PXD 6 (12U) fits in the order of nitride thickness influence, a far better behavior in terms of radiation hardness can be seen from the DUT S1U.

As a conclusion for the study of device parameters for gate equivalent devices a wet oxidation is clearly in favor when dealing with radiation hardness. In addition the thicker nitride exhibits mechanical/electrical advantages, in fact it smoothes out the surface leading to lesser occurrences of high electric fields. These high electric fields might cause a breakdown of the insulator.
The gate biasing method would be in favor of a fixed gate potential, however the issue of noisy bunches requires a higher gate adaptive voltage which results in a higher shift of the threshold voltage.



(a) ΔV_{th} of the DUT 06U. The devices were subjected to a gate adaptive biasing scenario. The high gate voltage of $+5\ V$ originates from the study for the gated mode (see section 7.3.1).



(b) Comparison of a fixed biasing scenario and a gate adaptive mode. The high gate voltage of $V_G = +5\ V$ simulates the gated mode of the DEPFET in the Belle II experiment.

Figure 7.9.: ΔV_{th} with respect to dose and different gate biases during irradiation.

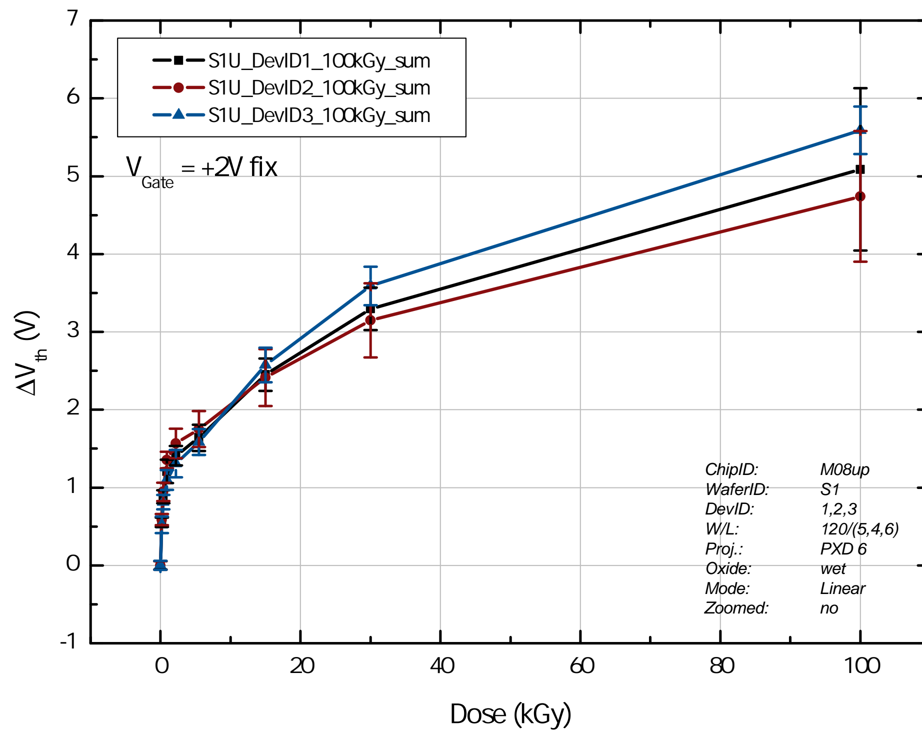


Figure 7.10.: Threshold voltage shift of three MOSFETs from the DUT S1U. These devices exhibit a wet oxide and show a maximum value of $\Delta V_{th} \approx [4.5\ V, 5.5\ V]$ after a dose of 100 kGy.

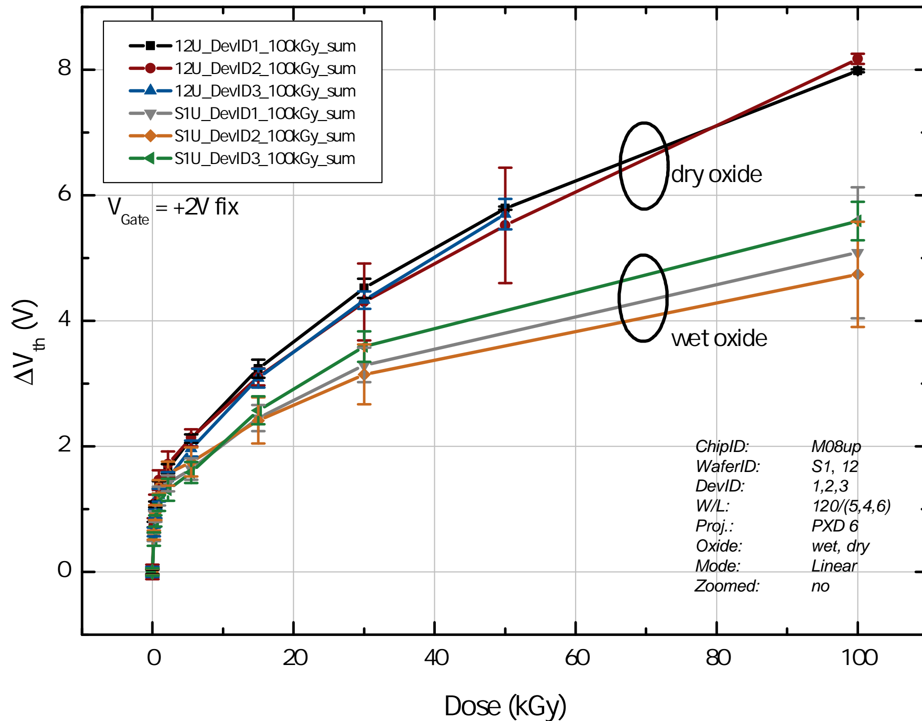


Figure 7.11.: Comparison between dry oxidation (12U) and wet oxidation (S1U). Although the wet oxidation devices show a dependency on gate length the threshold voltage shift is considerably lower with such devices.

7.3.3. Summary/Conclusions for the Gate

The study of threshold voltage shifts of the gate covered many parameters. The nitride layer thickness was investigated and an overall good performance, i.e. low threshold voltage shifts, could be found for devices which exhibit a 10 nm or 20 nm thickness.
In addition to the devices from the TO project, several DUTs from PXD 6 were irradiated and measured. Those devices were produced either with a wet or dry oxidation process for the gate insulator and a better performance for the wet oxides could be observed, despite - or perhaps because of the fact - that they exhibit a nitride thickness of 30 nm. Devices from the TO production showed a considerable shift with a thickness of 40 nm.
Besides of production related questions, i.e. oxide and nitride, several biasing schemes were evaluated. While a fixed gate bias of +2 V showed the best characteristics, only a slightly negative behavior could be observed for a +2 V gate adaptive biasing. However, the SuperKEKB injection scheme requires a gate adaptive biasing of +5 V, which in terms of radiation hardness is less favorable.

7.4. Threshold Voltage Shift Studies for the Clear Gate

7.4.1. Biasing Schemes for the CLG

Biasing schemes for the CLG are different from those for the gate. Figure 7.13 shows a typical design of the DEPFET. The clear gate itself has many intersections with neighboring

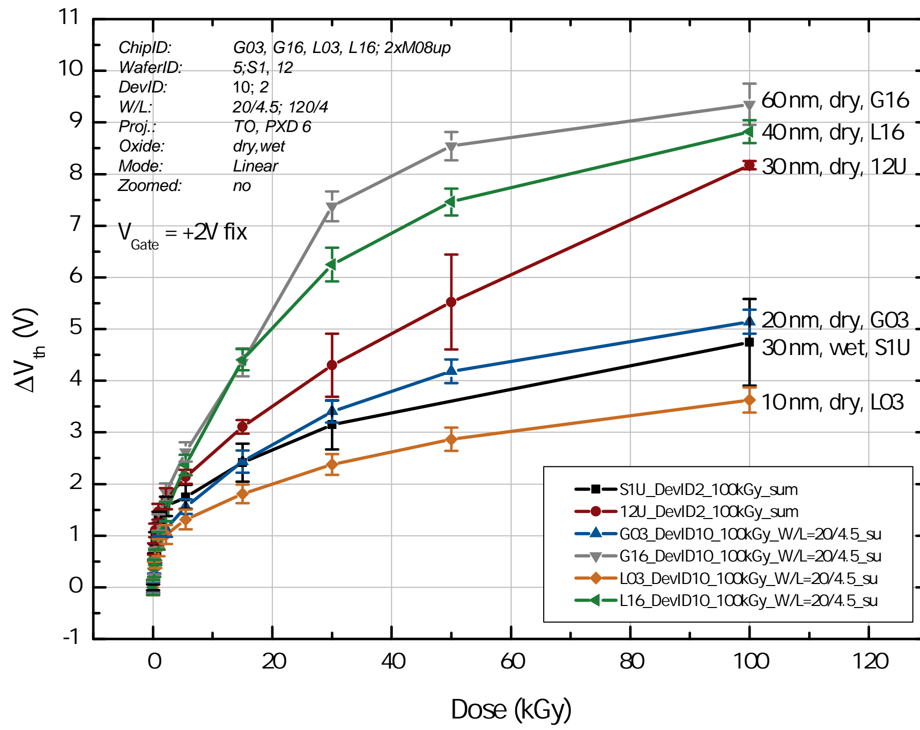


Figure 7.12.: Overview of threshold voltage shifts with a fixed gate bias of $V_G = +2\ V$. The wet oxidation (DUT S1U) shows a good performance, although the device L03 (10 nm) is slightly better.

contacts. Depending on the kind of contact (e.g. drain, clear) several potential differences arise. The difference ranges from $+5.5\ V$ (clear gate to the drift region) to $-6.5\ V$ (CLG to the clear). Thus not only the dependency of the threshold voltage from the dose is necessary for radiation assessments but also the dependency on the electric field/voltage. In this study the range was narrowed down to $[-5\ V, +5\ V]$ in steps of $2.5\ V$. More negative voltages can be neglected as data from literature indicates, e.g. Ma and Dressendorfer [74] provide a collection of material.

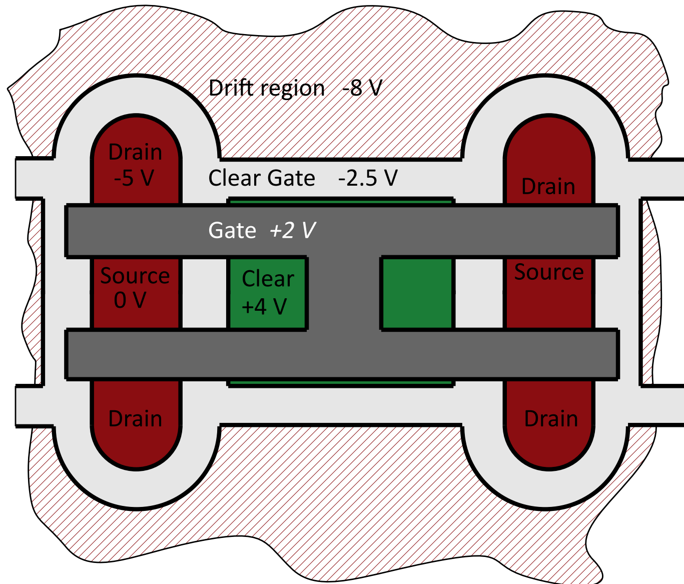


Figure 7.13.: Illustration of a layout of four DEPFETs in a compact design option. The voltage on the CLG has various counter electrodes which leads to an intra-pixel variation of the clear gate behavior.

In addition, adaptive biasing scenarios were conducted. The clear gate acts as a barrier for the electron between bulk and clear. Effects of unappropriated CLG voltages can range from a loss in signal efficiency up to a back injection of charge carriers (cf. section 7.1.2). Especially the region of the CLG next to the drift region is subjected to high voltage shifts. In order to prevent an unintended behavior of the DEPFET due to the radiation induced shift of the clear gate potential, the voltage of the CLG has to be adapted continuously during operation, which makes such studies necessary. The adaption for the CLG studies in this work was done in the same way as for the gate (described in section 7.3.1), with the exception that the gate bias is always adapted and not stopped at zero volt.

7.4.2. Measurements and Results

The investigation of the threshold voltage shift of the gate revealed a good performance for nitride layer thicknesses of 10 nm and 20 nm. Thus, the clear gate study focuses on these two values.

Figure 7.14 shows the behavior of several DUTs which were subjected to X-ray irradiation and exhibit a 10 nm nitride layer thickness. An overall small threshold shift with respect to

dose can be observed, however a fast increase in ΔV_{th} is visible for a fixed gate biasing of $V_G = +5\ V$.

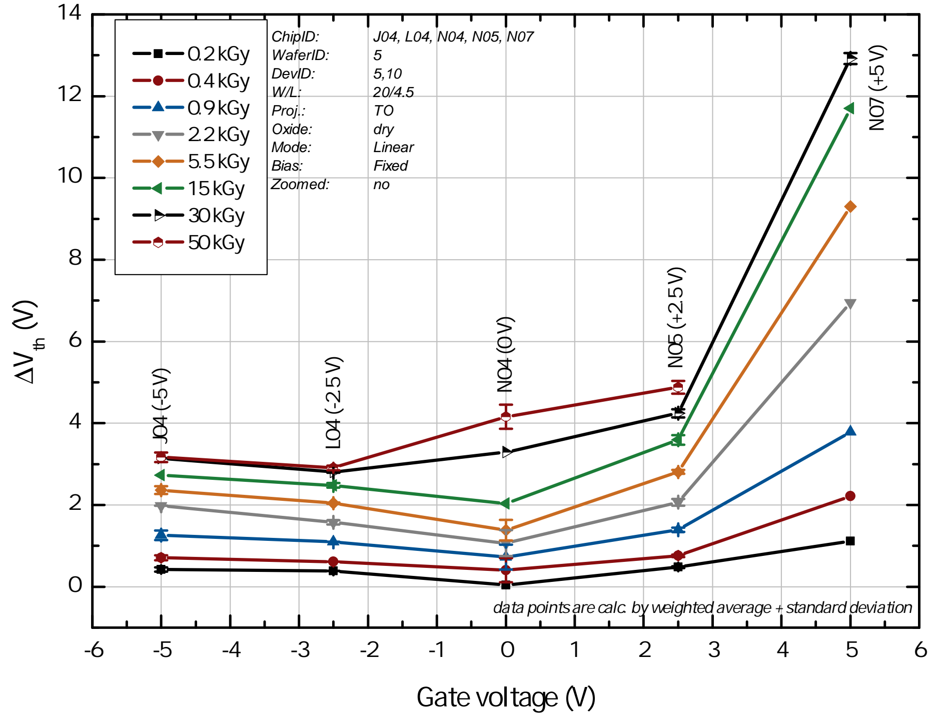


Figure 7.14.: Threshold voltage shift of clear gate equivalent test structures after certain dose steps. On the horizontal axis the fixed gate voltage during irradiation is depicted. Error bars represent the standard deviation to a weighted average of two V_{th} values. The MOSFETs exhibit a gate length of 4.5 μm and a nitride layer of 10 nm thickness.

The situation for the 20 nm is similar, as can be seen from figure 7.15. However, the crucial shift at $V_G = +5\ V$ is different. The DUT E07 exhibits a shift of

$$\Delta V_{th}(50\ kGy)_{20\ nm} \approx 9.5\ V, \tag{7.4}$$

which is considerably lower than the value of the DUT N07 of

$$\Delta V_{th}(30\ kGy)_{10\ nm} \approx 13\ V. \tag{7.5}$$

Thus, contrary to the results of the gate equivalent devices, a moderately thick nitride layer is favorable.

In order to avoid intra-pixel variations the shift in threshold voltage with respect to gate biasing ought to be in the same magnitude. Table 7.2 summarizes the values of threshold voltage shifts and the spread $\mathcal{S}$ to the median voltage. The spread with respect to the median is also shown in figure 7.16 for 30 kGy and 50 kGy. In this comparison the devices with 20 nm fare better than the ones with 10 nm, especially after 50 kGy.

The clear gate voltage has to be adapted to the threshold voltage shifts which occur during the operation of Belle II. The results are shown together with a fixed biasing in figure 7.17.

In the negative region of V_G an enhanced radiation damage can be observed as well as a reduction in the positive V_G region. The positive voltage is the main source of the spread in the threshold voltage. Thus, a reduction of the spread $\mathcal{S}$ may be possible.

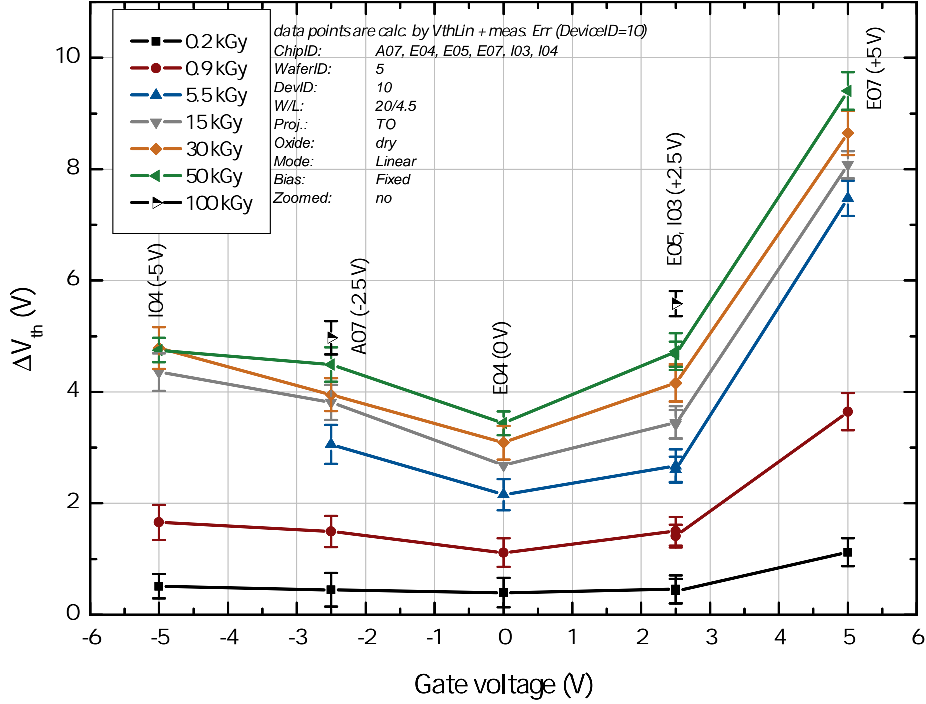


Figure 7.15.: Threshold voltage shifts of devices which exhibit a 20 nm nitride layer thickness. One MOSFET of the clear gate equivalent test structures is shown together with the measurement error on the V_{th} extraction in linear mode. At +2.5 V two different DUTs are shown.

	$\Delta V_{th}(V)$	$\mathcal{S}(V)$	$\Delta V_{th}(V)$	$\mathcal{S}(V)$	$\Delta V_{th}(V)$	$\mathcal{S}(V)$	$\Delta V_{th}(V)$	$\mathcal{S}(V)$
t_{Ni} Dose	10 nm 30 kGy	10 nm 30 kGy	10 nm 50 kGy	10 nm 50 kGy	20 nm 30 kGy	20 nm 30 kGy	20 nm 50 kGy	20 nm 50 kGy
$V_G(V)$		**3.29**		**3.66**		**4.16**		**4.72**
-5	3.14	-0.15	3.17	-0.50	4.79	0.62	4.75	0.03
-2.5	2.80	-0.49	2.91	-0.76	3.95	-0.21	4.49	-0.23
0	3.29	0.00	4.16	0.50	3.09	-1.08	3.44	-1.29
2.5	4.24	0.95	4.88	1.22	4.16	0.00	4.72	0.00
5	12.92	9.63	-	-	8.65	4.49	9.40	4.68

Table 7.2.: Overview of the threshold voltage after 30 kGy and 50 kGy and its spread $\mathcal{S}$ to the median (in bold).

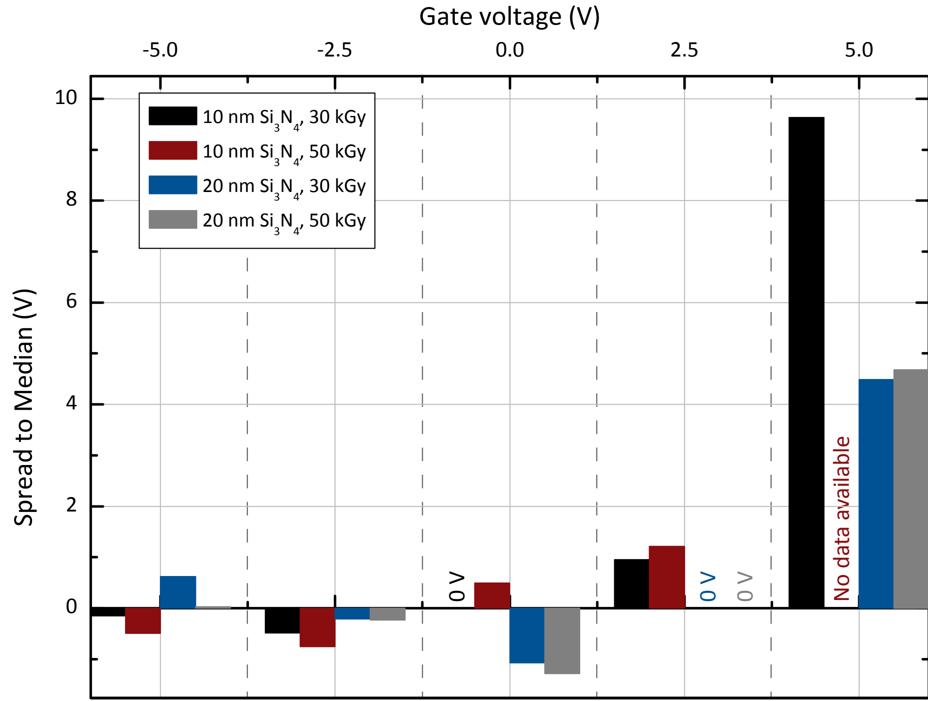


Figure 7.16.: Spread $\mathcal{S}$ of the clear gate threshold voltage shifts. The spread is calculated as the difference to the median value of one data set, e.g. differences of $\Delta V_{th}(V_G)$ of the 10 nm, 30 kGy data.

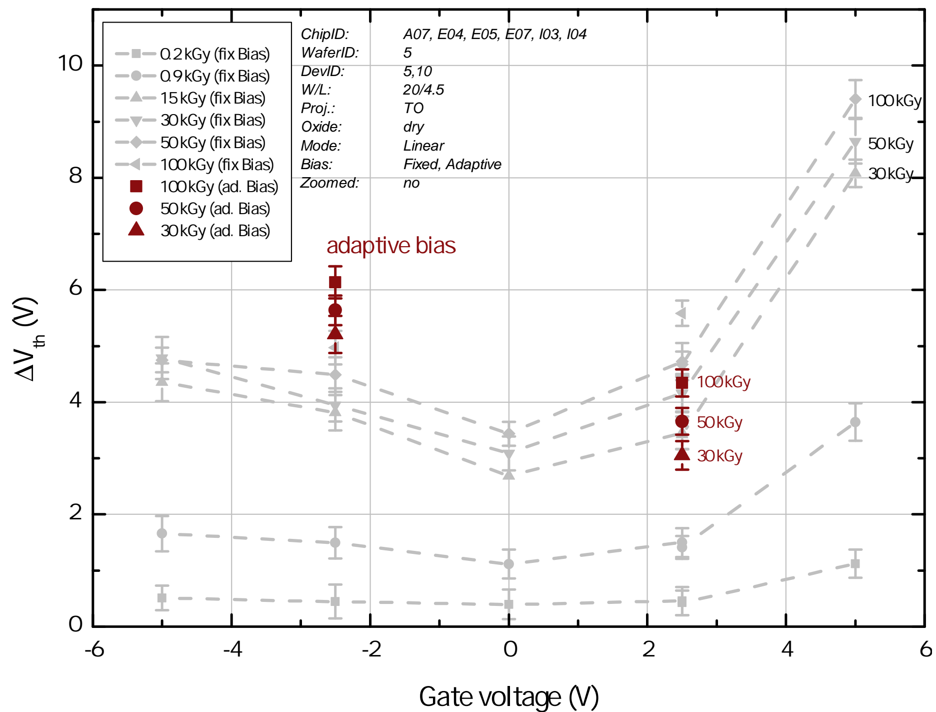


Figure 7.17.: Comparison between adaptive biasing (red) and fixed biasing (grey).

7.4.3. Summary/Conclusions for the Clear Gate

Due to the layout of the DEPFET several potential cross-sections to neighboring contacts arise, resulting in different electric fields in the CLG. In this section this influence of applied electric field/voltage was investigated. Several DUTs were irradiated with different gate biases. The threshold voltage shift with respect to the voltage parameter space was studied with two different nitride thicknesses from the TO project.
It could be shown that devices with a moderately thick nitride layer of 20 nm performed better than the comparison group which exhibits a thickness of 10 nm.
This is contrary to the results of section 7.3, at which gate structures of a 10 nm nitride layer thickness showed the least threshold voltage shifts.
In order to reduce the spread $\mathcal{S}$ of the voltage shifts, a reduction of the voltages of critical neighboring contacts within the DEPFET pixel (i.e. drift and drain) is desirable. In [39] a parameter scan of the drift voltage was performed and a reduction seems feasible.

7.5. Summary

In this chapter the threshold voltage shift of several DUTs is investigated. The thickness of the nitride layer in an MNOS device is of major interest. For the gate of a DEPFET a Si_3N_4 thickness of 10 nm is recommended. However, the nitride parameter affects also production related issues such as the smoothing of surfaces via the conformal deposition of nitride, in which a thicker deposition is desired. The use of a wet oxidation process in the fabrication of DEPFETs in combination with a moderately thick layer of 30 nm proves to be a good combination.
The clear gate has, contrary to the results from gate test structures, a better performance with a thicker layer of nitride. 20 nm instead of 10 nm is the thickness of choice to reduce the voltage spread due to other potentials of the DEPFET, such as drain or drift. This spread can also be reduced further by lowering the amount of drain and especially drift voltage. Such investigations were performed in [39] and shown to be feasible.
The biasing of similar devices in the studies for the gate and clear gate revealed the important influence of the electric field in the insulator for the behavior of the device to ionizing radiation. Most models, e.g. in [115, 74], rely on the fact of a finite trap precursor density. At higher doses the probability of finding a remaining trap precursor for the holes in the oxide decreases, such that a saturation of the threshold voltage is visible. However, similar devices in this study were different only in the biasing of the gate (see especially section 7.4 for the clear gate). Nearly all showed a saturation of $\Delta V_{th}(D)$ at higher doses, yet at different levels of ΔV_{th}. Thus it is a fair assessment that the trap precursor density is still sufficient and the origin of saturation lies elsewhere. A model for the radiation damage in MNOS devices, based on other assumptions, is proposed in chapter 9.

Chapter 8.

Surface Damage Annealing

The annealing of surface damage depends on several variables. Amongst them are time, temperature and bias. Interface traps can be annealed with the use of hydrogen, like it is done with forming gas during production. Since temperature affects crystal organization an effect on interface trap density is present. However, without elevated temperature and/or hydrogen incorporation only marginal changes in the interface trap density can be observed. In the following the discussion is focussed on the annealing of trapped oxide charge, interface trap annealing is mentioned briefly. Charge removal, or more precisely neutralization, occurs to a large part via tunneling of electrons from the semiconductor. Two different models of this time dependent process are compared and results on the fraction of anneal charge are presented.
Results after room temperature and elevated temperature annealing are shown besides a brief introduction into the annealing mechanism.

8.1. Introduction

DUTs which were measured for this thesis exhibit a negative shift in threshold voltage after irradiation. Therefore it can be readily concluded that positive charge is accumulated in the insulator and a huge fraction of the charge is probably located close to the Si/SiO_2 interface (see section 4.2 for explanation).
Figure 8.1 shows an idealized trap distribution of oxide trapped charge close to the interface.

The removal of a classical E' defect is the neutralization of the trap site with an electron, thus restoring a neutral charge of the two SiO_2 tetrahedrons. This annealing is possible via

1. tunneling of electrons to defects sitting spatially very close to the interface or
2. generation of charge pairs in the insulator itself and electron participation at defect sites.

Although a clear distinction between those two cannot be made (e.g. temperature has an effect on tunneling), in the following section a closer look at the physics of tunnel annealing is attempted.
An important aspect of annealing is that it is (up to a certain fraction) temporary, as shown by Schwank et al. [117]. They switched the biasing during elevated temperature annealing and could restore a considerable fraction of the defects believed to be annealed. Further studies showed that a more complex picture on atomic level was needed and eventually Lelis et al. [118] proposed a dipole model in which the tunneling electron does not remove the trapped hole but instead populates the remaining p-orbital at the neutral silicon (see e.g.

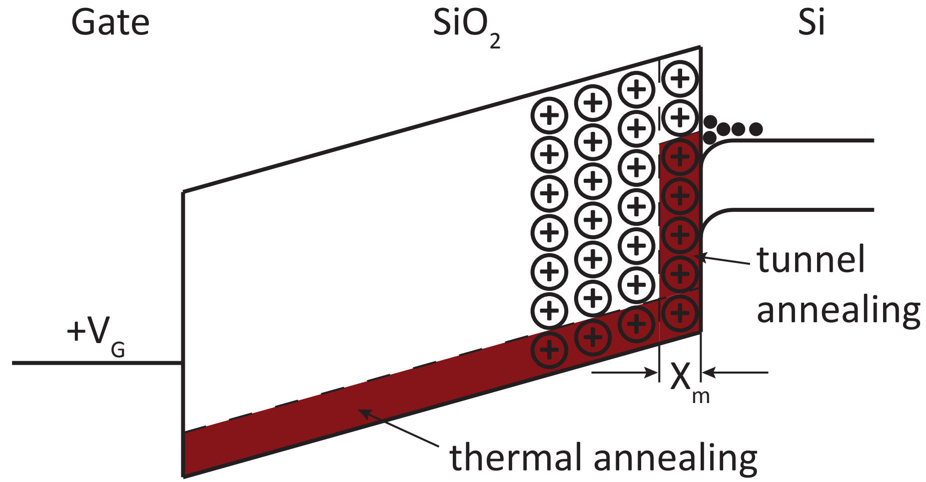


Figure 8.1.: Idealized distribution of trapped oxide charge. Electrons from the conduction band edge can anneal defects close to the interface within a typical distance x_m. Thermally generated ehps in the oxide can take part in the annealing process up to a certain energy level, after [116].

figure 4.6c). Only if the two silicon atoms are close to each other a *true* annealing, at which the binding between them is restored, can take place.

8.1.1. Tunnel Annealing

Defect sites in the SiO_2 sitting close to the interface can be neutralized with tunneling electrons from the silicon conduction band. However, this mechanism anneals only the fraction of defects which also have an appropriate energy level within the SiO_2 (see e.g. figure 8.2). Tunneling will lead to a fast decrease in accumulated oxide trapped charge with respect to time, yet as the tunnel probability decreases the annealing takes longer and longer until eventually a stable configuration is reached.
One explanation is to describe a tunneling front of annealing that can be expressed via the depth $x_m(t)$ in SiO_2 to which for a given time all oxide trapped charges up to this depth have been annealed [119].
Since the tunnel probability decreases exponentially, the depth can be explained by

$$x_m(t) = \frac{1}{2\beta} \ln\left(\frac{t}{t_0}\right), \tag{8.1}$$

with the tunnel barrier height parameter β and t_0 as a reference time. The amount of annealed traps can be extracted if a trap distribution $n(x)$ is assumed. E.g. a fast decrease beyond the interface is given by

$$n(x) = n_0 e^{-\lambda x}, \tag{8.2}$$

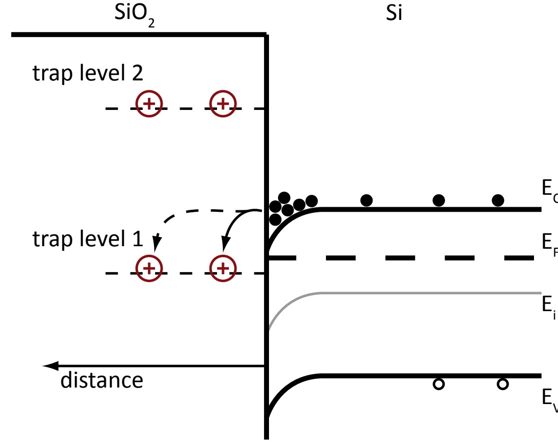


Figure 8.2.: Energy band diagram of the SiO_2/Si interface; for simplification only two energy trap levels are shown. Positive oxide charge traps are located spatially and energetically different in the oxide. Trap sites close to the silicon conduction band can be easily annealed via tunneling electrons (trap level 1). As the probability for finding a tunneling electron decreases exponentially with distance, parts of the trapped charge remain. Charge in higher traps (level 2) cannot be annealed. An elevated temperature is necessary to lift electrons to the appropriate level.

in which λ^{-1} is the characteristic trap depth and n_0 the trap normalization [75]. The amount of annealed traps $N(t)$ is calculated via

$$N(t) = \int_0^{x_m(t)} n(x)dx \tag{8.3}$$

$$= -\frac{n_0}{\lambda}\left[\left(\frac{t}{t_0}\right)^{\frac{-\lambda}{2\beta}} - 1\right]. \tag{8.4}$$

For changes in the amount of annealed charge $\Delta N(t)$

$$\Delta N(t) = N(t) - N(0) = -\frac{n_0}{\lambda}\left[\left(\frac{t}{t_0}\right)^{\frac{-\lambda}{2\beta}}\right] \tag{8.5}$$

can be simplified further. According to [120], taking the anneal front to be small in comparison to the thickness of the oxide t_{ox}, i.e. $x_m << t_{ox} \Rightarrow \lambda \to 0$, equation 8.5 modifies to

$$\lim_{\lambda\to 0} \Delta N(t) = \frac{n_0}{2\beta}\ln\left(\frac{t}{t_0}\right). \tag{8.6}$$

Under this assumption, the change in the threshold voltage/flat-band voltage with respect to time is then given by

$$\Delta V_{th}(t) = -\frac{q t_{ox}}{\epsilon_{SiO_2}} \cdot \frac{n_0}{2\beta}\ln\left(\frac{t}{t_0}\right), \tag{8.7}$$

which was observed in experiments [121, 60].
However, the above statements rely on several assumptions, like the behavior of the tunneling front x_m in equation 8.1 from McLean et al. [119] and also on the trap distribution $n(x)$ in

the oxide in equation 8.2. If one of the two assumptions is not entirely correct deviations from the logarithmic model are possible, as it is pointed out e.g. in Oldham et al. [120].
In the studies of Wei [75] a exponential behavior of annealing vs. time was fitted with considerably accuracy, assuming a different trap distribution. Thus, a comparison of the two different approaches is necessary.

8.1.2. Thermal and Bias Annealing

Several processes profit from elevated temperatures, so that the term "thermal annealing" might be misleading. Elevated temperature increases the amount of available ehps both in the silicon bulk and also in the oxide. Only the electrons in the oxide perform a pure thermal annealing by reaching defect sites up to a certain energy level as it is indicated in figure 8.1. Besides the increase in electron concentration in the silicon, elevated temperature enables annealing of trap sites which are located energetically higher than at room temperature (illustrated in figure 8.2). However the barrier height between Si/SiO_2 of 3.1 eV will not be overcome by temperature alone.
The use of a positive potential at the gate contact may lead to a tilt in the energy band diagram so that electrons can tunnel into energetically higher traps. Also, it increases the available amount of electrons in the conduction band due to the MOS interface. The DEPFET in the final Belle II experiment will exhibit all kinds of different electric fields in the clear gate insulator while the gate on the other hand will mostly be in a zero field condition. Therefore no special bias annealing study was conducted within this work and the devices annealed unbiased.
A third influence, i.e. photo generation of ehps in Si and SiO_2, is not discussed in this thesis. Although the DUTs were not entirely sealed from solar radiation they were not especially exposed, thus this topic can be omitted.

8.2. Room Temperature Annealing

8.2.1. Comparison of Annealing Behavior

Annealing of MOS Capacitors

In section 8.1.1 a logarithmic dependency of the flat-band voltage with respect to time was proposed. In figure 8.3 four MOSCAPs were evaluated with this assumption and although the overall fit characteristic results are not entirely good a common slope for the devices Q07, Q12 and B12 can be observed. The device B07, which exhibits a 20 nm nitride thickness, shows a smaller slope. A lower trap distribution density n_0 might be a reason for this observation (cf. equation 8.7).
As a comparison the four devices were also subjected to an analysis of the form

$$V_{FB}(t) = A(1 - e^{-t/\tau}), \tag{8.8}$$

referring to a model in which a certain fraction of trapped oxide charge is in tunneling distance and can be annealed away.
This analysis performs very well as can be seen in figure 8.4. For the lifetime of the traps τ two groups can be estimated. Q07 and Q12 anneal faster with $\tau \approx 50$ h and for B07 and B12 a much longer lifetime of $\tau \approx 85$ h is visible.

When comparing the two different model approaches of figure 8.3 and figure 8.4 a better performance of the exponential fit can be deduced.

However, a comparison of the total fraction of annealed charge reveals an interesting connection. The fraction f is given by the the relation of the shift at time t to the total shift,

$$f = \frac{V_{FB}(t) - V_{FB_{unirrad}}}{V_{FB}(t=0) - V_{FB_{unirrad}}}. \tag{8.9}$$

In figure 8.5 the flat-band voltage after the irradiation was set to one and would be zero if all the accumulated charge had been annealed away. From this point of view nearly all the capacitors anneal in the same way, except for the DUT B07. This device exhibits a faster anneal rate than the others, yet at the maximum anneal time the difference is only in the order of 5 %.

Another puzzling feature of all the devices which are shown in figure 8.5 is the common reverse annealing peak at $\sim 80\ h$. Such an effect can be attributed to device annealing rebound mechanisms as they were first reported by Schwank et al. [117] (cf. section 8.1). Even with zero bias voltage at the gate some small fractions of reverse annealing were observed but the overall trend in the annealing mechanism was not changed (see e.g. [122, 123, 66]).

Annealing of MOS Transistors

The annealing of MOSFETs is similar to the annealing of a MOS capacitor. For CLG studies the transistors were subjected to a gate bias during irradiation. The electric field in the device does not determine the spatial occupation of traps in the first place, but rather influences charge yield and timing response after irradiation pulses ([66]). However, the electric field does have an impact on the hole transport and depending on the dose rate an annealing during irradiation cannot be neglected. If a gate bias is present, the electron/hole concentration at the interface will influence the annealing response of the device.

Figure 8.6 shows the fraction anneal of devices with a 10 nm nitride thickness subjected to a gate bias during irradiation.

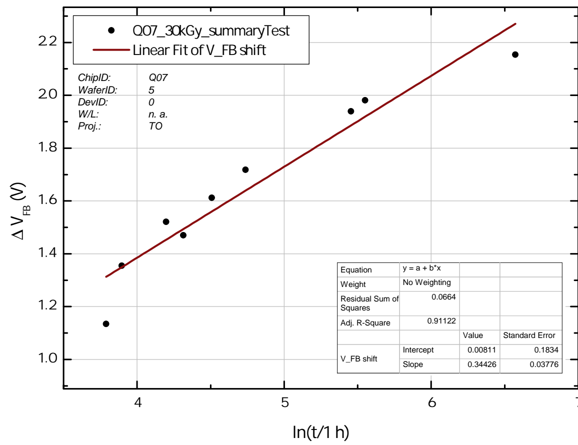
A clear dependency on the applied gate bias during irradiation cannot be deduced. A hypothesis may be that under zero bias up to positive bias the traps closer to the interface are occupied, which then results in a faster anneal. The positive potential during irradiation may have resulted in a small annealing during irradiation, so that traps close to the interface were already neutralized at the end of irradiation. Thus later on a slower annealing of devices with $V_G = 2.5\ V$ and $5\ V$ can be observed.

During irradiation, negative gate bias already hinders the hopping electrons from reaching the traps close to the interface, which results in poor tunnel annealing.

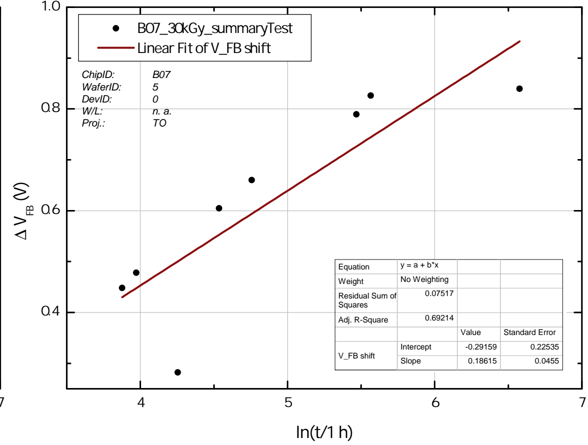
This hypothesis is somewhat contradicted by the results with devices which exhibit a 20 nm nitride layer. The resulting fraction anneal is shown in figure 8.7.

The device E04 with $V_G = 0\ V$ during irradiation seems to perform better than the complementary device N04, cf. figure 8.6. However, the devices E05 and E07 perform in a similar way as the devices with the lower nitride thickness, supporting the hypothesis.

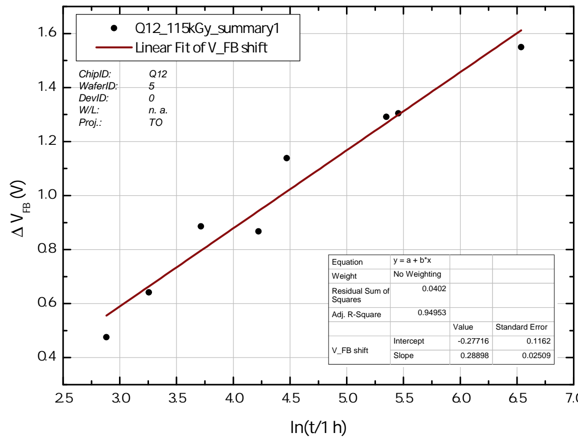
From the data at hand no decisive conclusion can be drawn in the issue of pre-bias depending annealing. Additional measurements, especially with devices with a zero gate bias, would be needed.



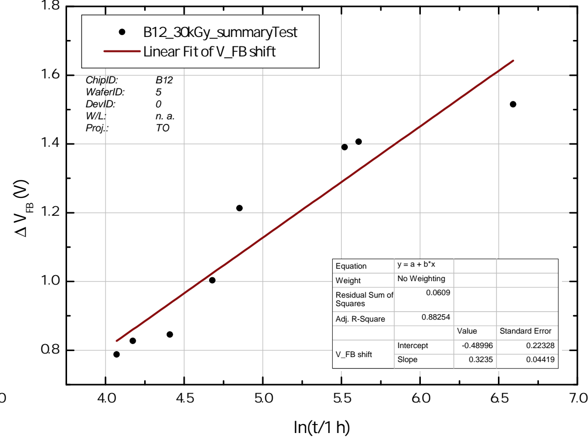
(a) Annealing of Q07 (10 nm of Si_3N_4). The fit seems reasonable, however long annealing times are not described very well.



(b) Annealing of B07 (20 nm of Si_3N_4). The model does not agree very well with the data, especially for long annealing times.

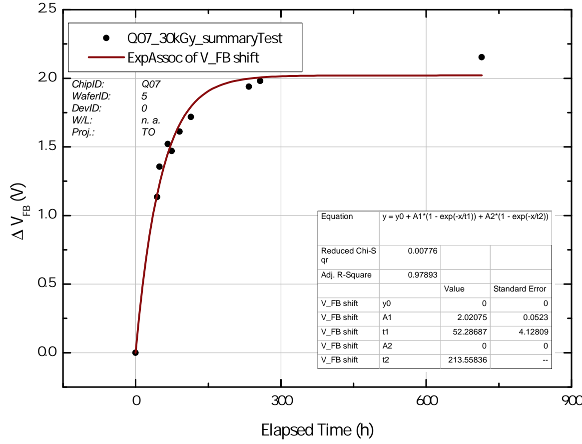


(c) Annealing of Q12 (40 nm of Si_3N_4). The data of this capacitor is well described by the ln dependency.

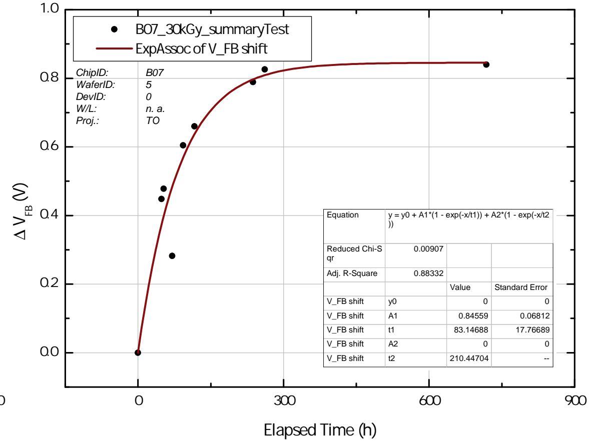


(d) Annealing of B12 (60 nm of Si_3N_4). Overall no good agreement between the suggested ln dependency and the data.

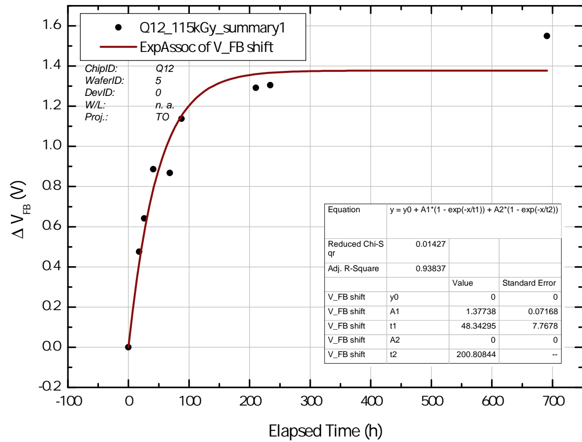
Figure 8.3.: Overview of the annealing amount in MOSCAPs. Each data set was fitted with an $V_{FB}(\ln(t))$ dependency.



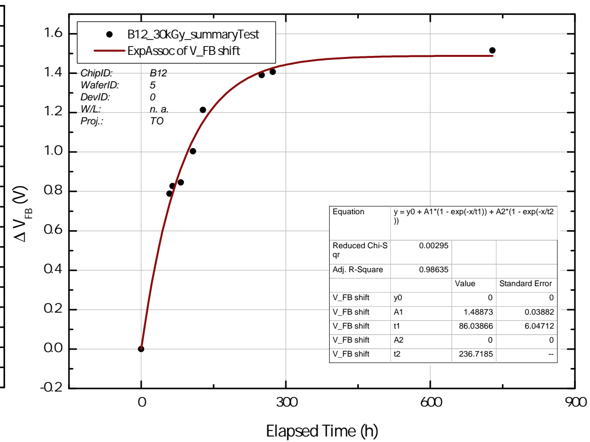
(a) Annealing of Q07 (10 nm of Si_3N_4). Data after long annealing is not accounted very well.



(b) Annealing of B07 (20 nm of Si_3N_4). Besides the data at $\sim 80\ h$ an excellent agreement between fit and data can be observed.



(c) Annealing of Q12 (40 nm of Si_3N_4). The data after $\sim$ 700 h of room temperature anneling is not described well with the fit.



(d) Annealing of B12 (60 nm of Si_3N_4). Overall fit and data are in good congruence.

Figure 8.4.: Overview of the annealing amount in MOSCAPs with an exponential behavior of the annealed flat band voltage $\Delta V_{FB}(t)$.

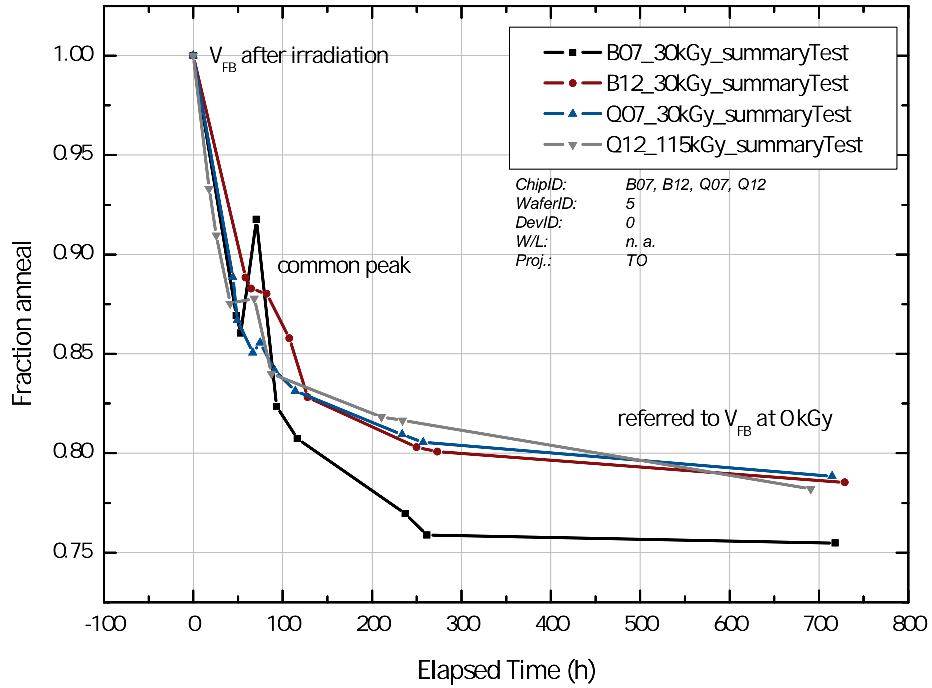


Figure 8.5.: Fraction anneal of MOS capacitors. The scaling of the vertical axis is normalized to the value of V_{FB} after the maximum dose and $t = 0$ (i.e. = '1'). A total anneal of accumulated charge would result in a '0' value (see also equation 8.9).

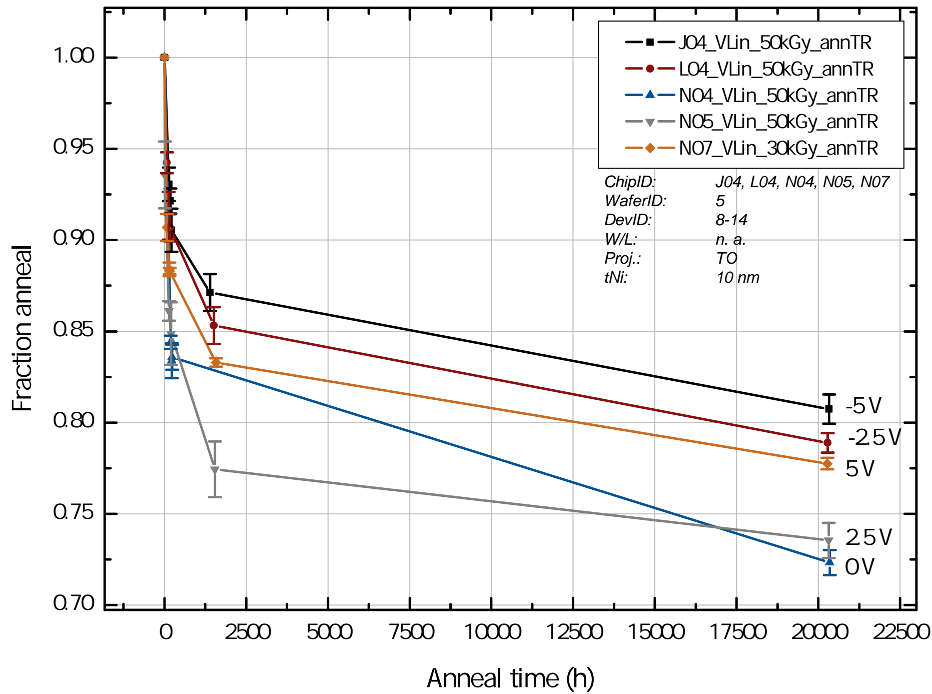


Figure 8.6.: Fraction anneal of MOSFETs which exhibit a Si_3N_4 thickness of 10 nm.

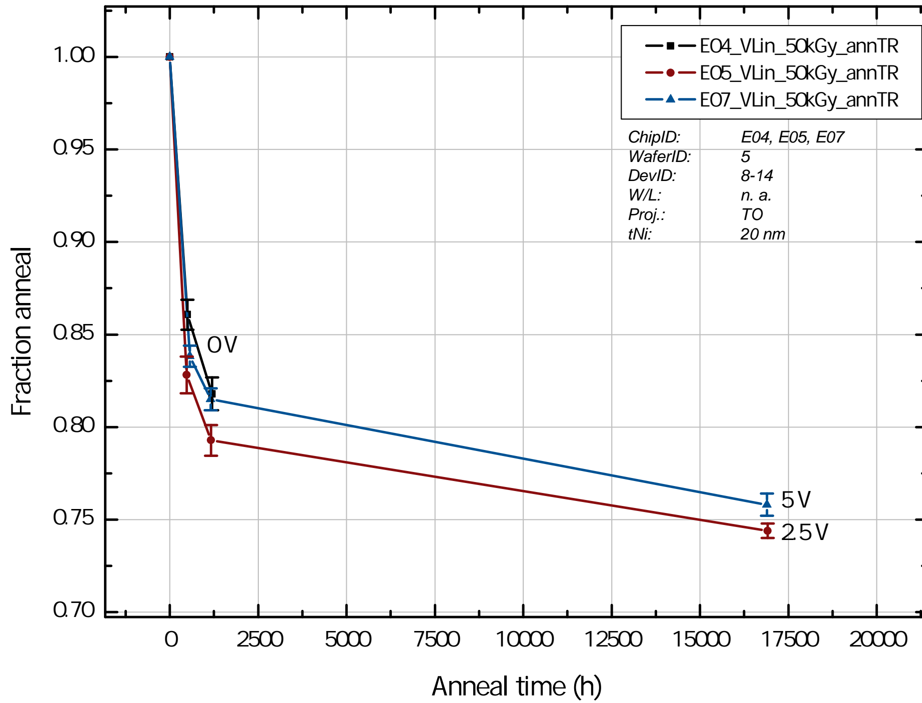


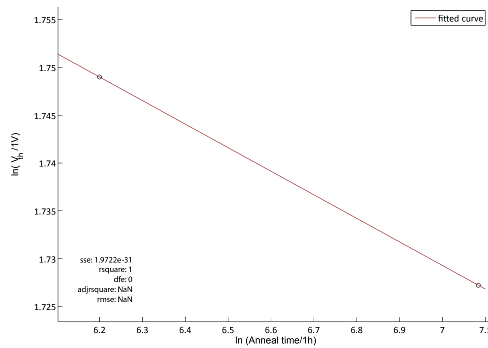
Figure 8.7.: Fraction anneal of MOSFETs which exhibit a Si_3N_4 thickness of 20 nm.

Besides the fraction anneal, it is clear that devices which exhibited a positive voltage on V_G during irradiation have a higher oxide trapped charge concentration. The fraction anneal shows what percentage of the threshold voltage shift has been removed by this charge.
The shown figures reveal a nearly universal trend in this issue. The considerably faster anneal of devices with a 20 nm nitride thickness (cf. figure 8.5) from MOSCAP measurements is found with the studied MOSFETs, too.

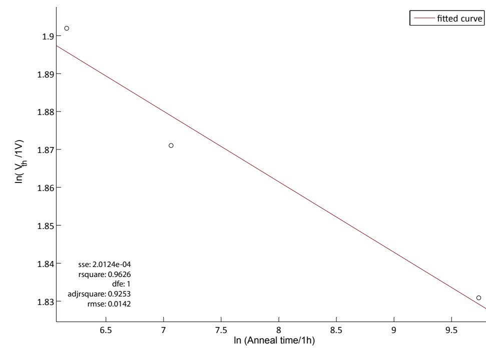
The already mentioned exponential behavior of the threshold voltage vs. the annealing time in equation 8.8 can be found with the studied MOSFETs as well. Figures 8.8 and 8.9 summarize the data of the different DUTs. The data was subjected to a ln operation and a linear fit was applied. The data point directly after irradiation, $t = 0$, is therefore lost. However even with this reduced data a good agreement between data and fitted behavior can be observed.

Summary

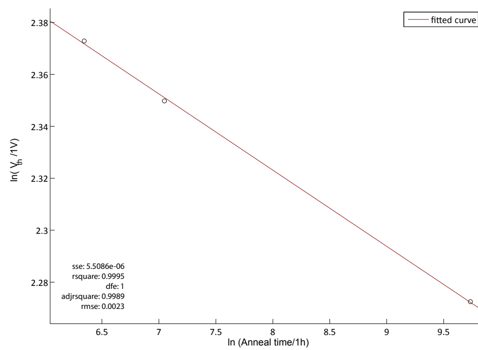
From the data shown in this study no clear distinction between a simple exponential model and the logarithmic model can be made. Whereas the studied MOSCAPs can be fitted reasonably well with the model proposed by McLean et al. [119] a better accordance can be observed with the simple exponential model. The shown MOSFETs depend also very well on an exponential behavior of time.
The typical time constant of MOSFETs is shown in figure 8.10 and is similar to the ones which can be observed from MOSCAP studies ($\sim$ 50 h and $\sim$ 80 h). The devices which exhibit a longer anneal time are J04 and L04 (both with a 10 nm nitride thickness) in



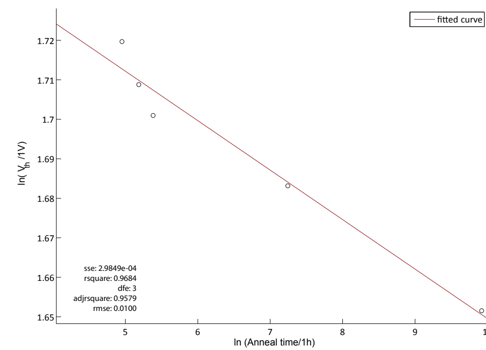
(a) E04.



(b) E05.

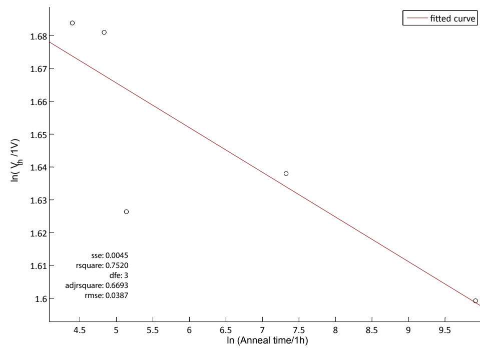


(c) E07.

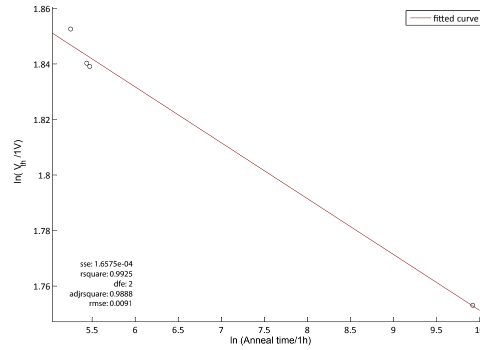


(d) J04.

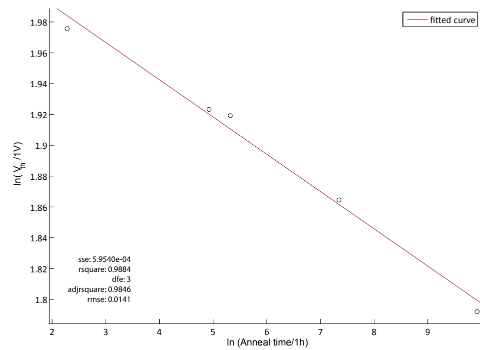
Figure 8.8.: Annealing behavior of MOSFETs. The data is the weighted average from 7 MOSFETs from the right-hand side of the DUT. The standard deviation to this average was used as a weighting parameter for the linear fit.



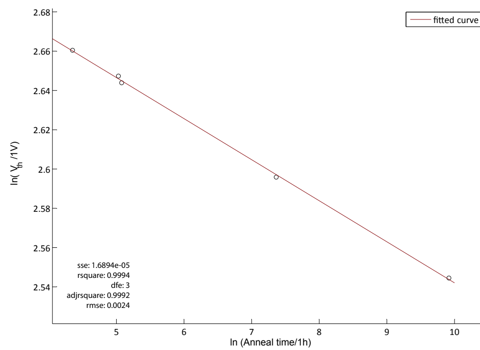
(a) L04.



(b) N04.



(c) N05.



(d) N07.

Figure 8.9.: Annealing behavior of MOSFETs. The data is the weighted average from 7 MOSFETs from the right-hand side of the DUT. The standard deviation to this average was used as a weighting parameter for the linear fit.

contrast to the devices B07 and B12 (20 and 60 nm). Thus a dependency on nitride thickness alone is hardly valid. To obtain a clearer picture on this issue, detailed trap investigations would be needed. However, for the final experiment the relevant information is the threshold voltage after a long-time anneal period.
From the shown fraction anneal figures a conclusion for the Belle II experiment can be drawn. The dose rate in the experiment will be much smaller than during the irradiation experiments for the studied devices and of course there will be idle times of the detector in which no beam will be present. Thus a continuous annealing will take place and despite the various amounts of radiation damage in the oxide due to the applied gate bias during irradiation, the final amount of threshold voltage shift will be reduced by $\sim 20\% - 25\%$.

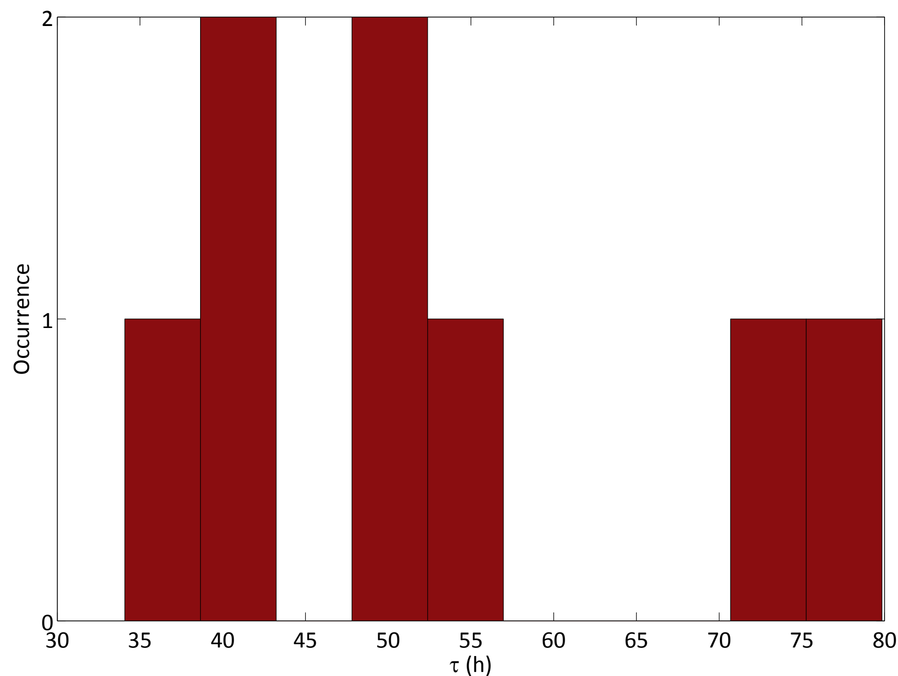
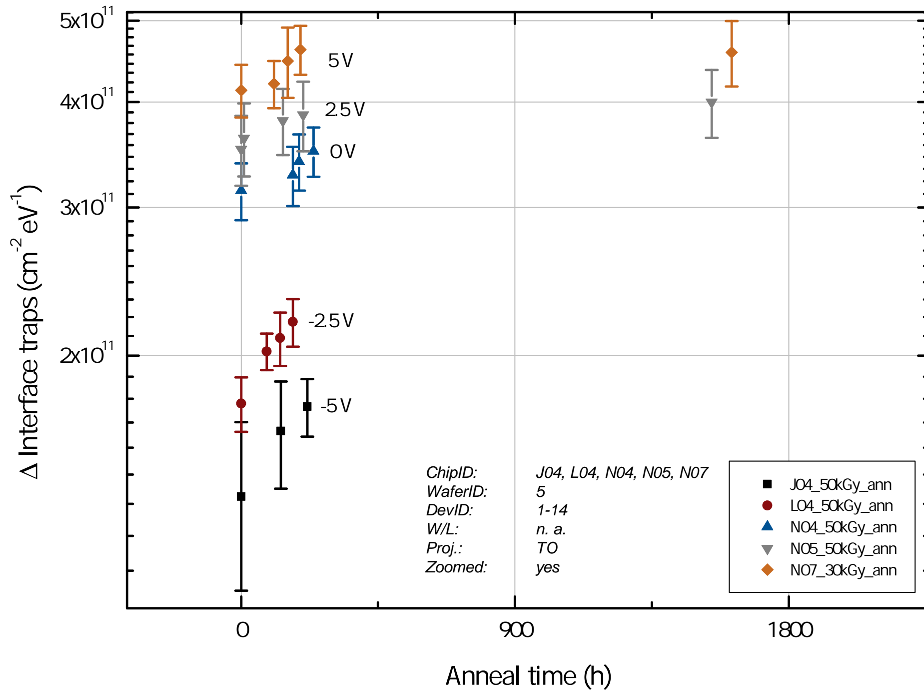


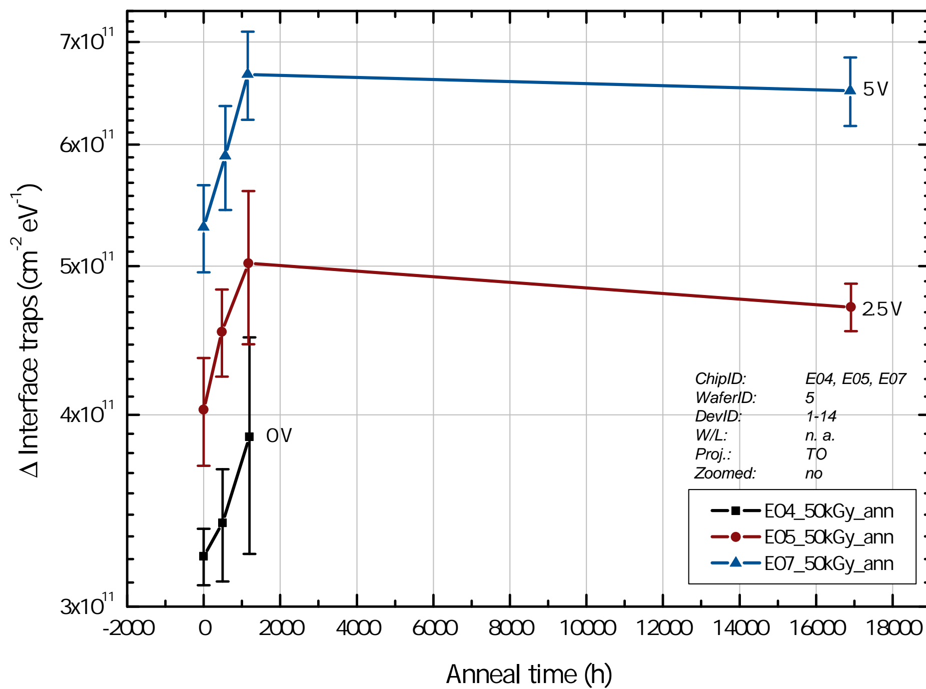
Figure 8.10.: Occurrence of the anneal time constant τ in MOSFET annealing.

8.2.2. Interface Trap Annealing - Latent Build-Up

For a real annealing of interface traps hydrogen would be needed. However, according to literature the build-up of interface traps is a multi-type process, see e.g [124, 65]. This results in a retarded increase of interface traps. Figure 8.11 shows a summary of this issue. The data is the weighted average of the 14 MOSFETs according to the single measurement errors, the error bars represent the standard deviation to the weighted average.
Figure 8.11a shows a detailed view of the latent interface trap build-up on a short time scale, while figure 8.11b focuses on the long term aspect in which a small decrease in trap concentration can be observed.



(a) Latent interface trap build-up of 10 nm nitride thickness devices.



(b) Long term aspect of 20 nm nitride thickness DUTs.

Figure 8.11.: Evolution of interface trap increase of MOSFETs with respect to the anneal time. A latent build-up is visible. The mean of the data is the weighted average with the standard deviation as error bars.

8.3. Elevated Temperature Annealing

8.3.1. Description of Experiment

In this experiment an irradiated DUT was exposed to three temperature cycles with characterizations before and after the heat treatment.
The DUT is a gate equivalent structure from the TO project, i.e Chip G16. It exhibits a 60 nm nitride layer and was subjected to an X-ray irradiation of 100 kGy prior to the heat treatment. The temperature treatment was done with an ATV SRO 703 Reflow oven. Nitrogen was used as an atmosphere during the heat treatment, to ensure that no hydrogen contamination took place during heating. After heating, the characterization was performed at room temperature roughly one day later. Temperature during heating was supervised with a temperature sensor. Each heat treatment lasted for 1 h, selected temperatures for the first and second hour were 200°C and for the third hour 250°C. The stability of the selected temperature on DUT level can be seen in figure 8.12.

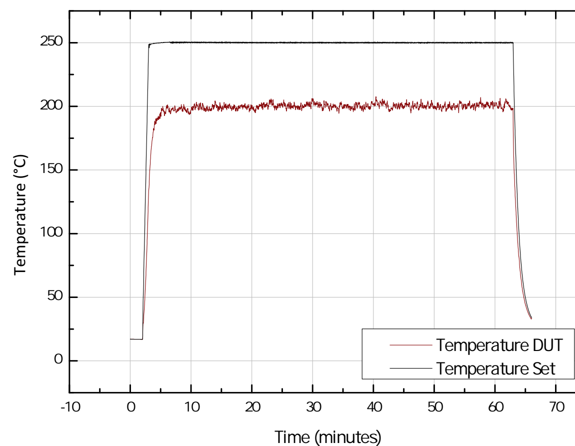


Figure 8.12.: Temperature stability of the heat treatment. To achieve 200°C at DUT level, the oven had to be set at roughly 250°C.

8.3.2. Results of Transistor Annealing

First, an improvement in threshold voltage can be seen from the shape of the curves in the input characteristics, see figure 8.13a. The evolution of the threshold voltage with each temperature step is shown in figure 8.14. It can be seen that already after 1 h with 200°C a huge portion of the threshold shift can be annealed away, a second hour with this temperature is less effective, but still a minor improvement is possible. In order to anneal more of the trapped charge higher temperatures are required, as can be seen from the last step with 250°C.
Figure 8.13b shows the transconductance of a selected MOSFET from the chip G16. While room temperature annealing has a slightly negative influence, already 1 h with 200°C is sufficient to restore the g_m to its original value, as can also be seen from figure 8.15b.
In addition, the subthreshold swing (see figure 8.15a) shows nearly the same behavior as the transconductance from figure 8.15b. While a fast degradation takes place with irradiation, an additional degradation with room temperature annealing is visible. This deterioration of

performance might also happen considerably fast (in comparison to the 250 days of room temperature annealing) after irradiation. In [124] a typical increase in this latent interface trap build-up started after $\gtrsim 10^5\ s(\approx 27\ h)$. Dose rate effects for interface traps (e.g. dose rates in [94]) can in most cases be attributed to this latent build-up [66].
In addition, the combined behavior of g_m and swing is in good agreement with the formation of interface traps, since they are visible as mobility degradation in the transconductance (leading to a lower g_m) and in an increase in swing. Already one hour at $200°C$ is sufficient to achieve nearly the same value as prior to irradiation.

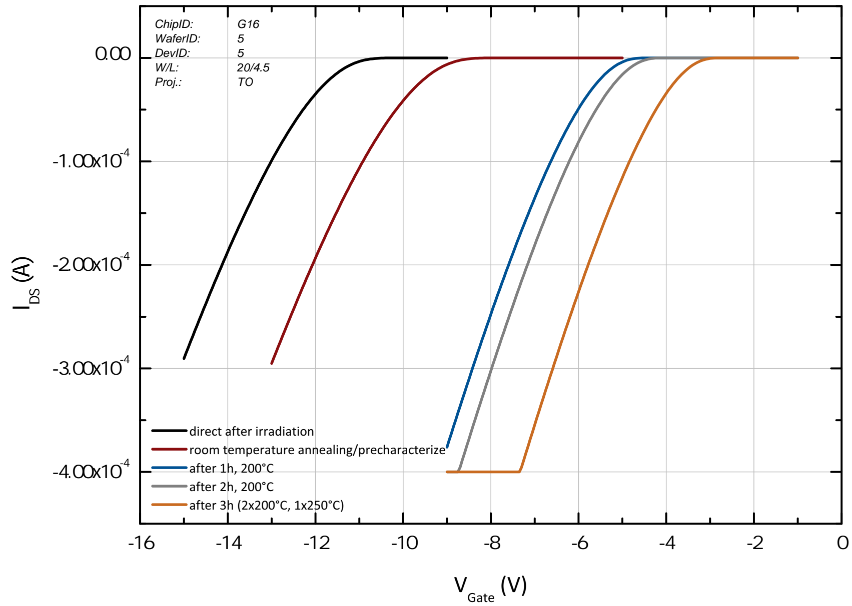
8.3.3. Results of GCD Annealing

An interesting question in the whole subject of thermal annealing is how to reduce surface generated current. As aforesaid, the GCD is designed to investigate surface currents. With its large gate area this effect becomes visible. The gate controlled diode therefore is a good measuring device. Figure 8.16a shows a summary of the diode reverse current vs. gate voltage from initial characterization up to the last temperature step. Clearly, X-ray radiation caused a strong increase in current and a shift for the onset of depletion.
Comparing the shift in depletion voltage from the GCD, figure 8.16b, with the evolution of the threshold voltage shift in figure 8.14, there is a recognizably larger shift in the GCD and also a better room temperature annealing than with MOSFETs. However, biasing conditions and structure of the transistors are different in comparison to the GCD. When looking at the effect of enhanced thermal annealing, the reductions are comparable and the trends in both plots are similar.
Figure 8.17a shows the increase of the surface recombination velocity s_g. Directly related (via equation 3.55) to this quantity is the density of interface traps, shown in figure 8.17b. Exemplary a cross-section of $\sigma = 2 \cdot 10^{-15}\ cm^2$ is chosen, however the remarks in section 6.3.1 regarding the issue of the various capture cross-sections have to be kept in mind. This value originates from Wei [75], who also used HLL devices. It is obvious that the surface generation is reduced drastically when exposed to the temperature treatment.

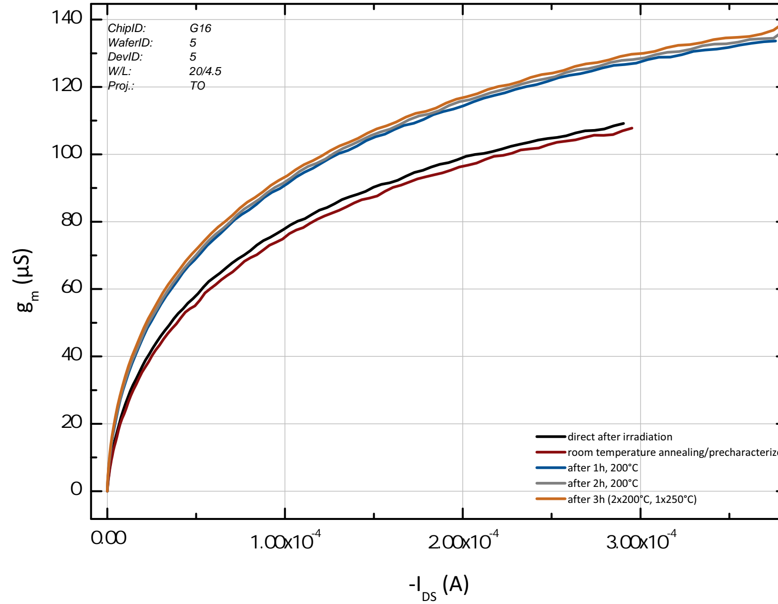
8.4. Impact on PXD/Belle II

The aforementioned elevated temperature annealing studies are not in total relevant for Belle II. It has to be said that the PXD itself will be operated at room temperature or a temperature lying close by[1]. Therefore the enhanced temperature treatments can only be relevant for experiments which exhibit an easy access to the detector and a robust mechanical design which can resist the elevated temperatures.
However, the presented temperature study shows the characteristics of the DEPFET to deal with radiation damage. Especially the reduction of surface generated current is only possible (in the studied scenario) with elevated temperature, as shown in figures 8.15a and 8.17.
The annealing of threshold voltage shifts at room temperature is a relevant condition which has to be taken into account. In the experiments in this study, radiation facilities were used which exhibited higher dose rates than in the final experiment. Therefore, together with the shut-down times of Belle II, a continuous annealing takes place over time. For the threshold

[1]The cooling system is designed to keep the PXD in the range of $[0°\ C, 30°C]$ [125].



(a) Input characteristics of a selected MOSFET of the G16 DUT. The first temperature treatment shits the input characteristic of the MOSFET considerably.



(b) Transconductance with respect to drain current. Room temperature annealing has only a minor effect on the change of g_m, while already 1 h at $200^{\circ}C$ is enough.

Figure 8.13.: Measurement data and derived transconductance of a selected transistor of G16.

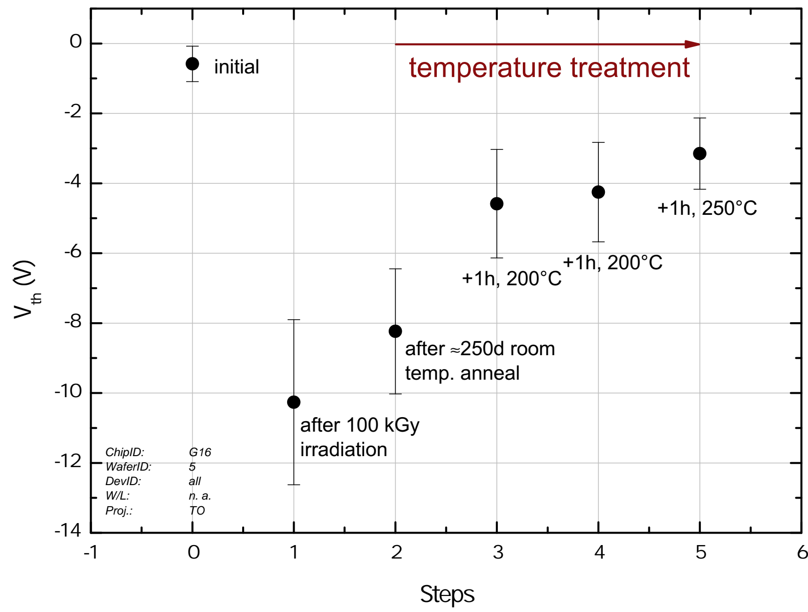
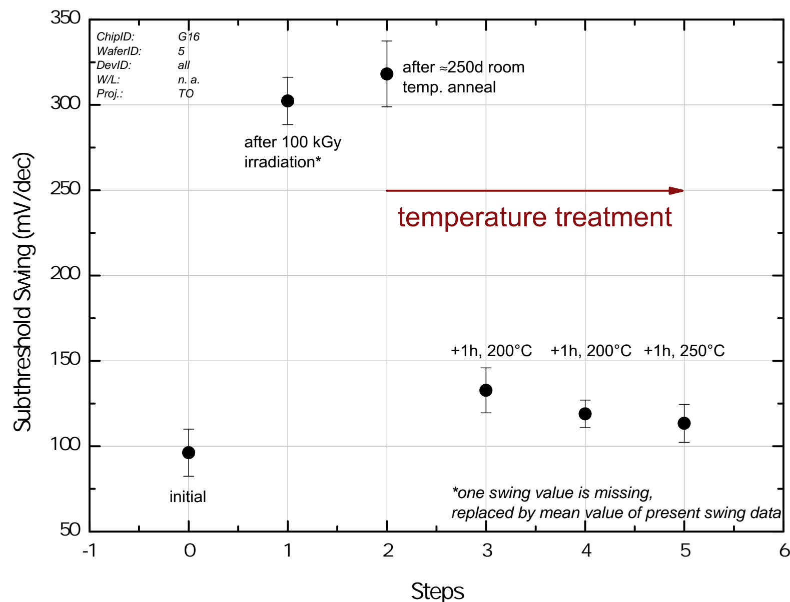
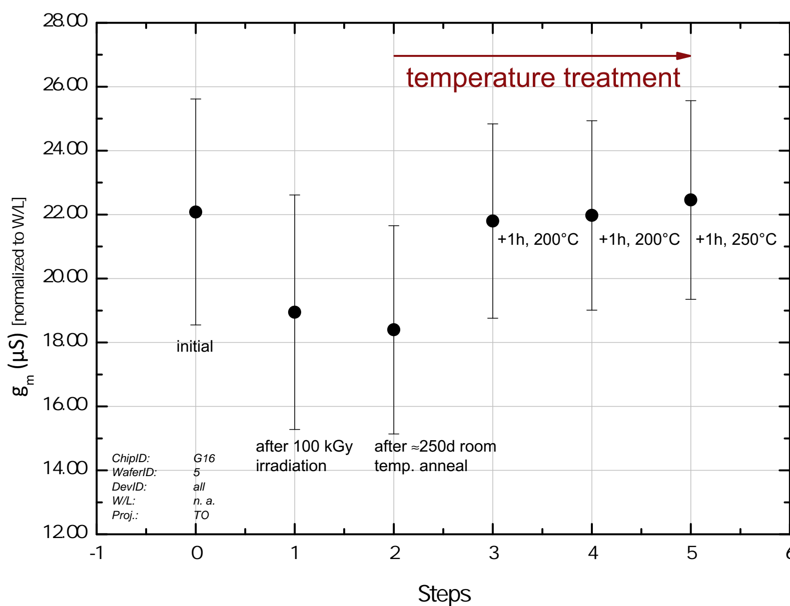


Figure 8.14.: Threshold voltage evolving with irradiation, room temperature annealing and heat treatment. Error bars represent the standard deviation of all 14 MOSFETs of the DUT.

voltage shifts a value at roughly 75 % – 80 % of the shifts encountered in chapter 7 should be used.

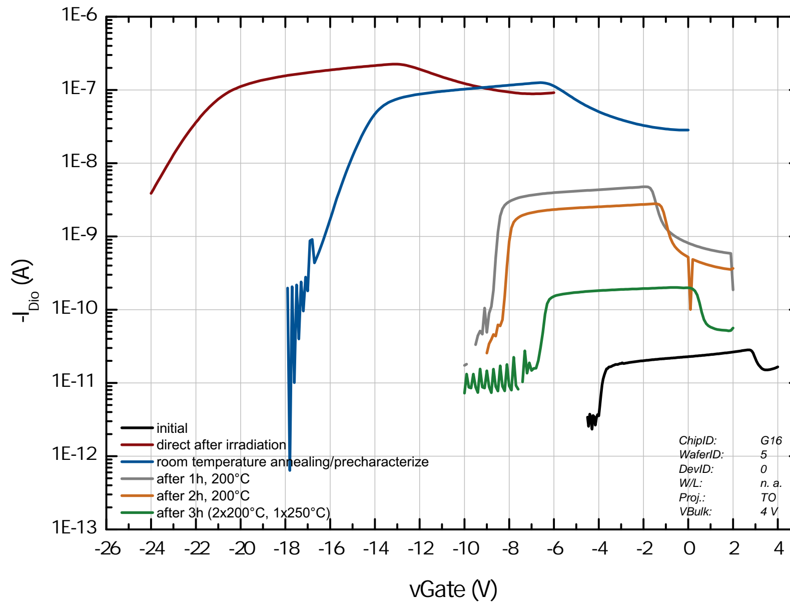


(a) Subthreshold swing of all 14 MOSFETs of the chip G16. A fast recovery after one hour of heat treatment is visible.

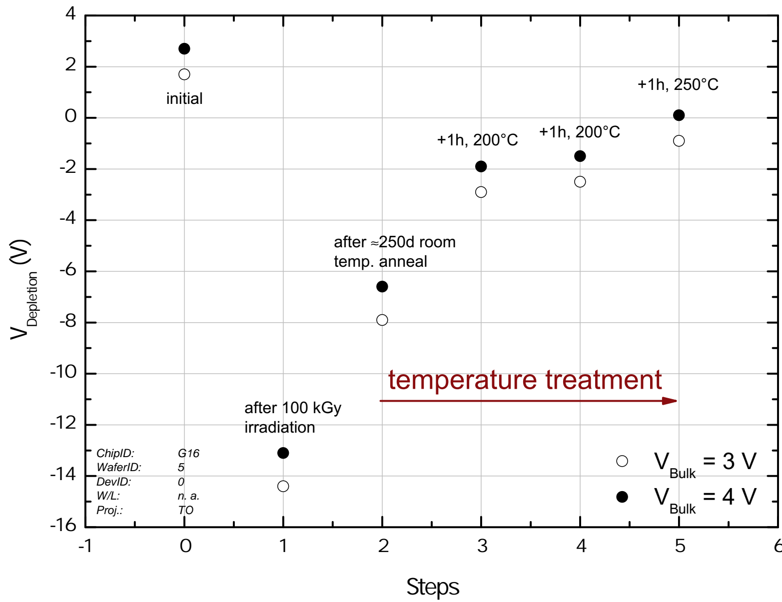


(b) Normalized transconductance of G16. Error bars represent the standard deviation of all 14 MOSFETs of the DUT. The g_m was extracted at 100 μA and then normalized to W/L.

Figure 8.15.: Overview of derived characteristics of all 14 transistors of G16.

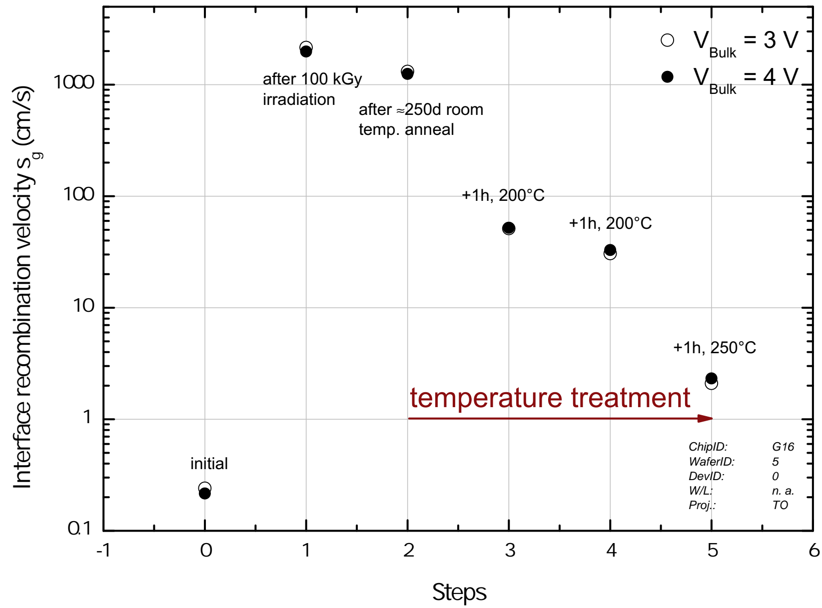


(a) Reverse current vs. gate voltage of the GCD. The data shown was measured with a reversed biasing of $4\ V$. Room temperature annealing is beneficial for threshold voltage, whereas the surface generation current is only slightly affected.

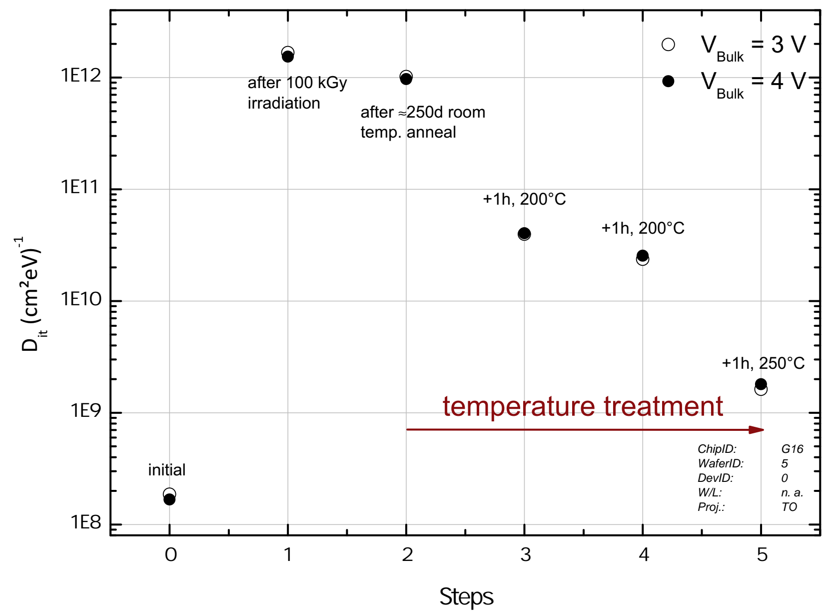


(b) Evolution of the onset of depletion.

Figure 8.16.: Change in reverse current and depletion voltage of the gate controlled diode.



(a) Interface recombination velocity of G16. Temperature treatment reduces generation of charge carriers dramatically.



(b) Interface trap density changes with radiation and temperature. No hydrogen was added during the temperature treatment. For the evaluation a cross-section of $\sigma = 2 \cdot 10^{-15}\ cm^2$ was assumed.

Figure 8.17.: Overview of derived characteristics. Interface recombination velocity and interface trap density are proportional to each other.

Chapter 9.

Proposed Model for Radiation Damage in MNOS Devices

This chapter is dedicated to a proposed model of the radiation induced threshold voltage shift in MNOS devices. The key aspect of the model is the charge yield of the generated ehps in the insulator. Other models rely on the trap precursor density for E' center. However, measurements in this thesis on similar devices with different biasing showed that a saturation of precursors cannot be the origin of the saturation in $\Delta V_{th}(D)$.
The MNOS composition of the insulator is common in all the devices in this thesis. The model was evaluated with devices from the TO project only, due to the fact that the production influence in ΔV_{th} can be neglected as it is the same in all devices.
A test of the model to single datasets is made followed up by predictions of the threshold voltage shift for different devices.

9.1. Motivation for a Model of Radiation Damage in MNOS Devices

The origin of the shift of the threshold voltage of MNOS devices due to ionizing radiation is the trapping of electric charge in both insulator materials. A model to describe this effect should therefore include these two materials. Previous models, e.g. in [115, 74, 75], are based on a finite trap precursor density of the form

$$N_t = N_0(1 - e^{-\sigma\eta}). \tag{9.1}$$

Here N_t is the density of trapped charge, N_0 is the density of precursors, and σ is the capture cross-section for the hole fluence η that cross the trap sites.
The various biasing studies for the clear gate (cf. section 7.4) revealed a saturation at higher doses. However this saturation was always at different levels of ΔV_{th}. It is thus fair to state that the finite density of precursors is not the leading cause of saturation.
The following model is based on the idea of Raparla et al. [126] but was extended and modified[1].
The proposed model could serve as a tool in further productions of MNOS devices. The behavior to ionizing radiation damage could be predicted to a certain degree, making design considerations for the radiation hardness easier.

[1] Commercial MNOS structures are used as memory devices. However, the devices studied for this model exhibit a relatively thick oxide of $t_{ox} = 85\ nm$ in comparison to the thickness of commercial devices with $t_{ox} \approx 2\ nm$ ([127]). Due to the thin oxide layer electrons are able to tunnel the oxide barrier very effectively. Therefore this model does not apply for such thin insulating layers of SiO_2.

9.2. Charge Yield and Trapping

The basic idea of the model is that the amount of charge (initially created by ionizing radiation) which can be trapped in the insulators is based on a charge yield depending on the electric field over the insulator. The stronger the electric field is, the more charge separation takes place and recombination is suppressed. In the range of the electric fields in this work ($\approx [-25\,\frac{MV}{m}, 15\,\frac{MV}{m}]$) the yield can be assumed as a linear function (see e.g. [128] and [60]). In the next step, a mechanism is introduced to describe the saturation of ΔV_{th} at higher doses. This is done via reducing the electric field in the insulator by the trapped charge.
Trapping can occur at defect sites in the bulk and at the boundaries of both insulators. However, detailed microscopic information on the location of defect sites cannot be determined with the data at hand. Thus only the projection of the charge to the insulator boundaries is taken into account.
Since SiO_2 is known to preferably trap holes the boundary Si/SiO_2 is assumed to be only positively charged. The interface SiO_2/Si_3N_4 is assumed to be either positively or negatively charged. An illustration of the model concepts is shown in figure 9.1.

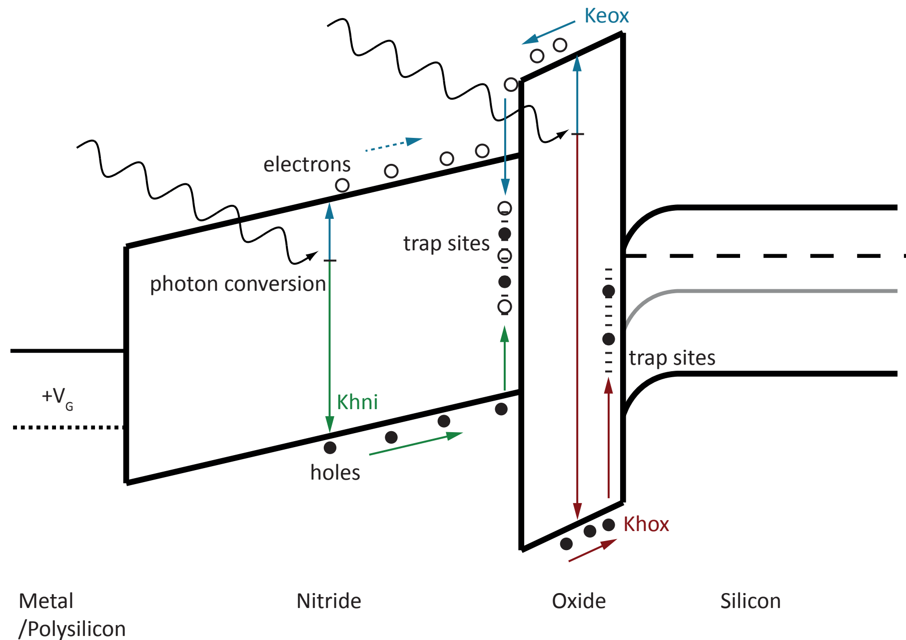


Figure 9.1.: Illustration of the MNOS interface. Incoming ionizing radiation (e.g. via photons) is converted in the insulators and dependent on the generation parameters K (explained in the text) a different amount of electrons and holes is trapped at defect sites in the insulators.

The charging of trap sites is realized with different parameters. $Khox$ describes the generation and trapping of holes in the oxide. The amount of charge increases the more insulator material is present as an absorber for incoming irradiation. This is described with the two thicknesses of the insulators, t_{ox} and t_{ni}.
The generation of holes in the nitride and subsequent trapping at the Si_3N_4/SiO_2 bound-

ary is described with the parameter $Khni$. For simplification the common generation and trapping of electrons from both insulators is represented by the parameter $Keox$[2].

External electric fields in the insulators are taken into account via the parameters $E_{ext_{ox}}$ and $E_{ext_{ni}}$. At the beginning, i.e. dose $D = 0$, they determine the initial charge yield. However, even if the electric field is zero, a small amount of charge may escape the recombination process, e.g. via diffusion. To take this effect into account a parameter G_{const} is introduced into the yield.
For the Si/SiO_2 interface the charge q_{ox} with respect to the dose D is then given by

$$\frac{dq_{ox}}{dD} = Khox \cdot t_{ox} \cdot \left(\frac{1}{2\epsilon_{ox}} (q_{ni} - q_{ox}) + E_{ext_{ox}} + G_{const} \right). \tag{9.2}$$

For the SiO_2/Si_3N_4 interface the equation is slightly different because both insulator layers contribute, thus

$$\begin{aligned} \frac{dq_{ni}}{dD} = & Khni \cdot t_{ni} \cdot \left(\frac{1}{2\epsilon_{ni}} (q_{ni} + q_{ox}) + E_{ext_{ni}} + G_{const} \right) \\ & - Keox \cdot t_{ox} \cdot \left(\frac{1}{2\epsilon_{ox}} (q_{ni} - q_{ox}) + E_{ext_{ox}} + G_{const} \right). \end{aligned} \tag{9.3}$$

This set of linear coupled differential equations was solved using *Mathematica 6.0* with

$$q_{ox}(0) = 0 \tag{9.4}$$

$$q_{ni}(0) = 0 \tag{9.5}$$

as boundary conditions. The shift in threshold voltage was calculated using a capacitor plate model of the MNOS interface. The series circuit of the nitride and oxide capacitor constitutes the total insulator capacitance.

9.3. Applied Voltage and Resulting Electric Field

9.3.1. Potential for the Clear Gate

For the electric field over the insulator two cases can be separated:

1. $V_{Gate} < V_{th}$
2. $V_{Gate} > V_{th}$

In the first case (see e.g. figure 9.2a) a conducting channel is established, with a potential of $2\Phi_B$. The difference of V_{Gate} to V_{th} drops over the insulator.
In the second case of a higher gate voltage, the channel is suppressed and the potential difference of V_{Bulk} and V_{Gate} is relevant. The bulk potential reaches up to $\approx 0.4\ \mu m$ to the interface. The potential difference drops over the insulator and partially over the silicon (see figure 9.2b).

[2] This assumes equal generation and trapping processes in both insulators. The higher mobility of electrons in comparison to holes justifies this assumption to a certain degree. However, a more detailed view on the processes would require a different treatment of electrons in their appropriate insulators.

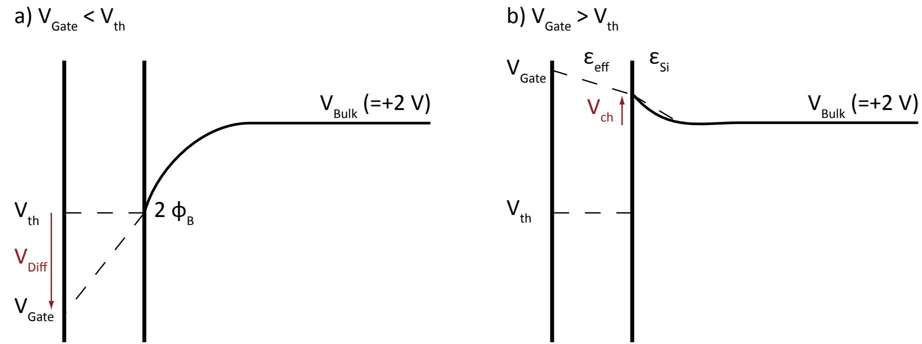


Figure 9.2.: Illustration of potential and electric field for the clear gate equivalent test structures from the TO project. In a) the potential drops over the insulator, in b) a small amount of silicon is included.

9.3.2. Potential for Gate

The potential at the gate is determined by the properties of the internal gate. If a voltage is applied which is higher than V_{th}, the internal gate will follow this voltage, since it is a floating potential. Irradiations with gate equivalent test structures were conducted with a fixed $V_G = 2\ V$ and they exhibit a threshold voltage $V_{th} \approx 0\ V$. This results in a zero potential over the insulator and therefore zero electric field in all devices studied for the model.

The situation becomes different when considering scenarios where the gate voltage is adapted or inhomogeneous irradiation already leads to a conducting channel, whereas other DEPFETs are still off. In such a case the conducting channel is the corresponding electrode and the electric field must be calculated to this potential.

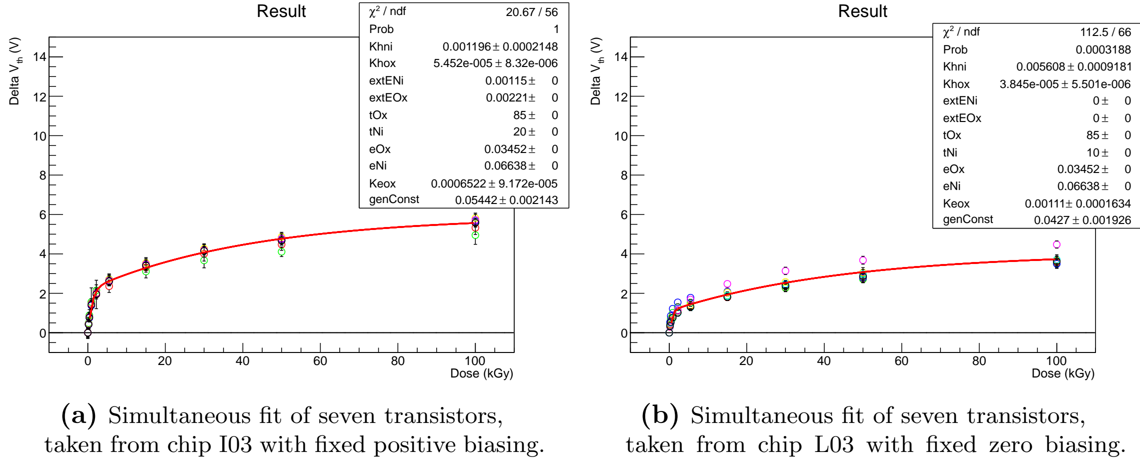
9.4. Fitting of Data

The solution of the differential equation was implemented in a ROOT[3] program and used for fitting the data from the TO project. Hereby a fitting tool, which could simultaneously fit different datasets with only the model parameters ($Khox$, $Khni$, $Keox$ and G_{const}) available as degrees of freedom, was developed.

In order to gain an oversight of the parameters similar datasets were fitted together. For this purpose only devices which exhibited a fix biasing during irradiation experiments were used. Adaptive biasing would implicate a dose dependency of the external electric fields and thus require a change in the model equations 9.2 and 9.3. In addition, only data from measurements which were conducted in the linear regime of the MOSFETs was used to prevent alterations of the measured V_{th}, e.g. due to DIBL (cf. section 3.3.5).

In addition side effects, which can occur at the interface of the insulator close to source and drain (i.e. lateral electric fields) were neglected. Typical results are shown in figure 9.3.

[3] http://root.cern.ch



(a) Simultaneous fit of seven transistors, taken from chip I03 with fixed positive biasing.

(b) Simultaneous fit of seven transistors, taken from chip L03 with fixed zero biasing.

Figure 9.3.: Fit of model equations to the measured threshold voltage shifts. Model parameters were extracted from such fits. Quantities like the external electric field are set as fixed values in the model.

9.5. Model Parameters

A dependency on the appropriate electric field could be found for the quantities which are inherent in the model, i.e. $Khox$, $Khni$, $Keox$, and G_{const}. The quantities were extracted from isolated fits to each dataset and arranged to their appropriate electric fields. This is shown in figures 9.4 to 9.8. This dependency on the electric fields is hardly surprising since the transport equations for the generated charge are missing in the model. For simplicity these were omitted and the motion and trapping of charge carriers is included in the model parameters. Table 9.1 summarizes these parameters and the values returned from the fits are stated in table E.1 (appendix E).

Quantity	Appr. el. field	Description
$Khni_{10}$	$E_{ext_{ni}}$	Generation/trapping of holes for a 10 nm nitride thickness
$Khni_{20}$	$E_{ext_{ni}}$	Generation/trapping of holes for a 20 nm nitride thickness
$Keox$	$E_{ext_{ox}}$	Generation/trapping of electrons for both oxide and nitride
$Khox$	$E_{ext_{ox}}$	Generation/trapping of holes in the oxide
G_{const}	$E_{ext_{ox}}$	Finite generation of charge

Table 9.1.: Overview of model parameters and their dependency on the external electric field.

In order to make proper predictions a simple look-up of the parameters had to be found. This was done by using appropriate equations to describe the behavior of the parameters due to the electric field. Additional dependencies for the parameters are:

- $Khni$. In addition to a function of the electric field, a dependency on the nitride thickness could be found for the parameter $Khni$, as shown in figures 9.4 and 9.5.
- $Keox$ and $Khox$. These two depend on the electric field, as shown in figures 9.6 and 9.7. Possibly the parameters additionally depend on the oxide thickness, yet this could

not be investigated. All devices exhibited the same oxide thickness in this study.

- G_{const}. This parameter was used in the yield for both oxide and nitride, because the introduction of more parameters would have lead to an overfitting of the observed data.

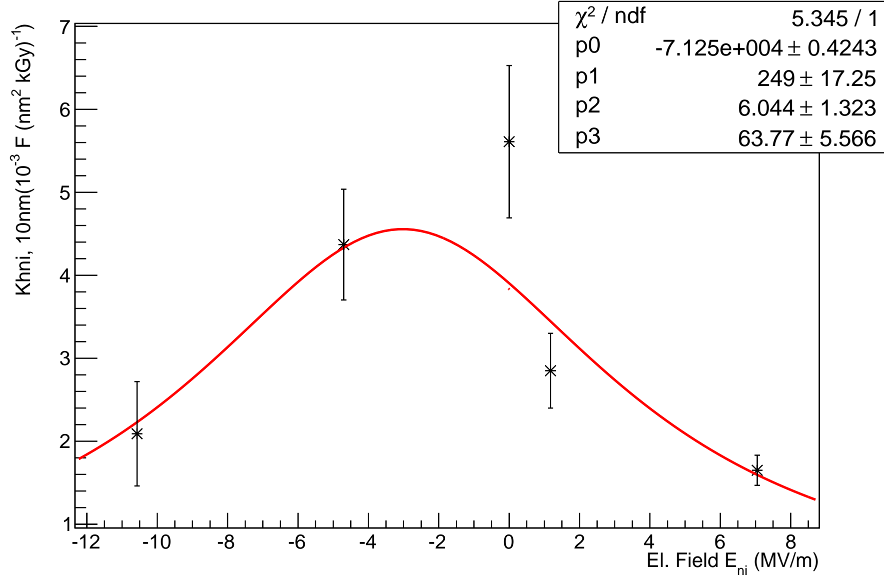


Figure 9.4.: Dependency of $Khni$ on the electric field present in Si_3N_4 for 10 nm nitride devices. The used function is $Khni_{10} = (p_1 \cdot E_{ni} + p_2)/(E_{ni}^2 + q_1 \cdot E_{ni} + q_2)$ (equation 9.6). Scaling of values was introduced to aid the fitting algorithm.

The look-up table for the parameters is used via fitting these equations to the extracted fit parameters (parameters like p_i and q_i are independent for each equation/quantity):

$$Khni_{10} = (p_1 \cdot E_{ni} + p_2)/(E_{ni}^2 + q_1 \cdot E_{ni} + q_2) \tag{9.6}$$

$$Khni_{20} = (p_1 \cdot E_{ni} + p_2)/(E_{ni}^2 + q_1 \cdot E_{ni} + q_2) \tag{9.7}$$

$$Keox = p_1/(E_{ox}^2 + q_1 \cdot E_{ox} + q_2) \tag{9.8}$$

$$Khox = p_1 \cdot E_{ox}^2 + p_2 \cdot E_{ox} + p_3 \tag{9.9}$$

$$G_{const} = p_1 \cdot E_{ox}^2 + p_2 \cdot E_{ox} + p_3 \tag{9.10}$$

9.6. Comparison of Prediction and Data

With the aforementioned parameter description it is possible to predict the radiation damage for a limited set of devices. Since only one oxide thickness was available, a prediction to other oxide thicknesses has to be considered with caution. If the parameters do not depend very

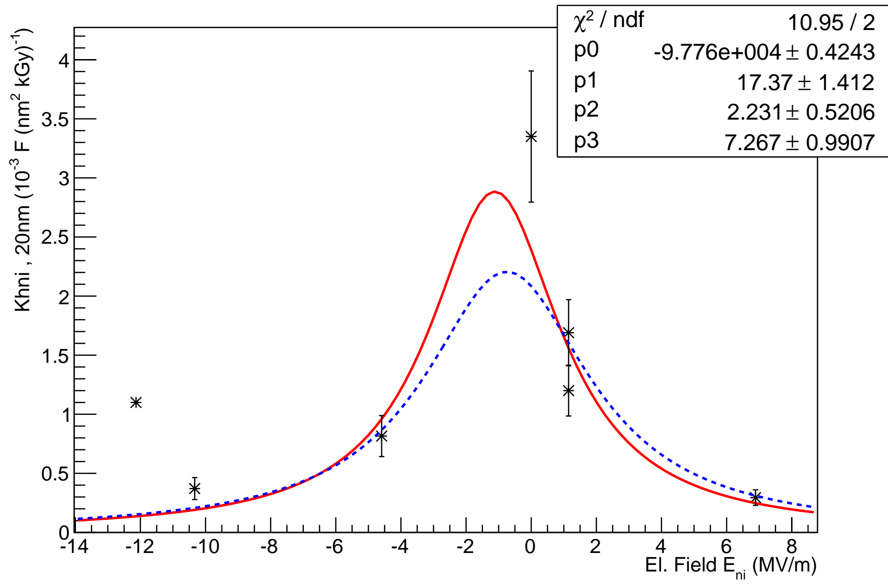


Figure 9.5.: Dependency of $Khni$ on the electric field present in Si_3N_4 for 20 nm nitride devices. The used function is $Khni_{20} = (p_1 \cdot E_{ni} + p_2)/(E_{ni}^2 + q_1 \cdot E_{ni} + q_2)$ (equation 9.7). The values of 20 nm devices are smaller for corresponding fields than in 10 nm devices. Scaling of values was introduced to aid the fitting algorithm. The blue dashed line indicates the starting values of the fitting algorithm.

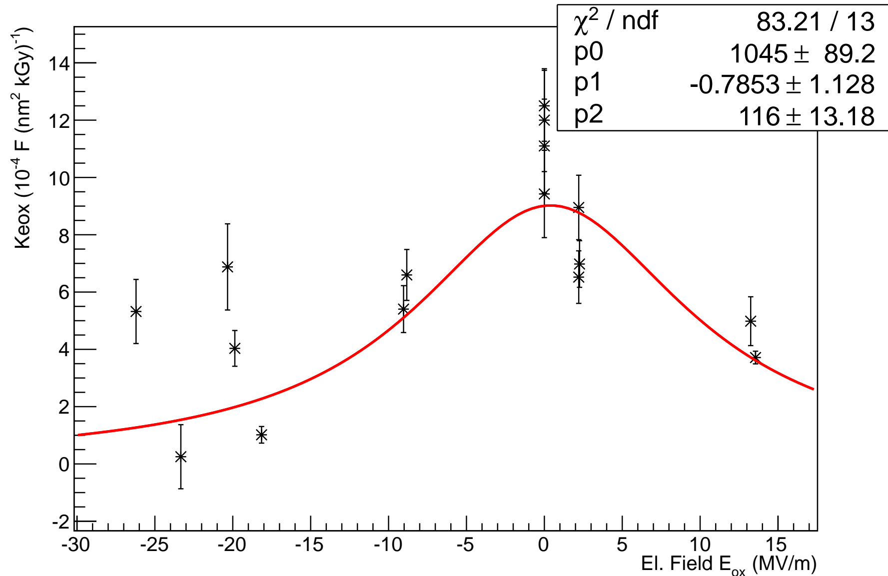


Figure 9.6.: Dependency of the parameter $Keox$ on the electric field in SiO_2. $Keox = p_1/(E_{ox}^2 + q_1 \cdot E_{ox} + q_2)$ (equation 9.8) was used as a fitting function.

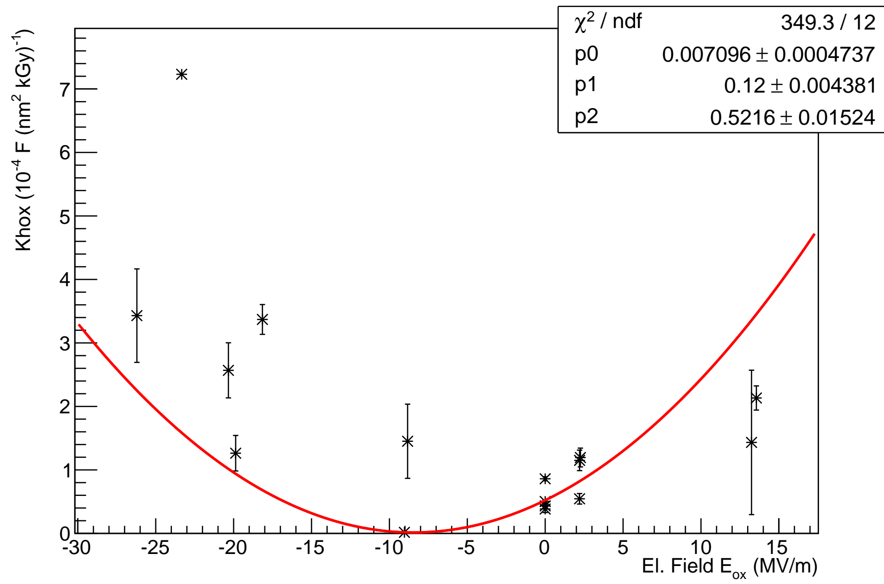


Figure 9.7.: Generation of holes in SiO_2 depending on the electric field. Equation 9.9, $Khox = p_1 \cdot E_{ox}^2 + p_2 \cdot E_{ox} + p_3$, was used for fitting the initial fit results.

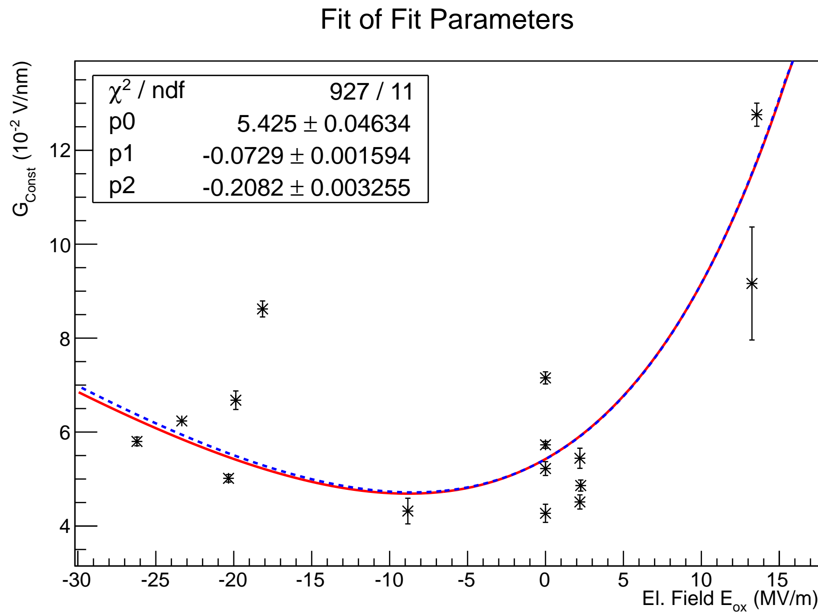


Figure 9.8.: Yield parameter G_{const} dependency of the electric field in SiO_2. G_{const} was only determined with respect to E_{ox}, the value is then the same for both insulators. As a fitting function equation 9.10 with $G_{const} = p_1 \cdot E_{ox}^2 + p_2 \cdot E_{ox} + p_3$ was used. The blue dashed line indicates the starting values of the fitting algorithm.

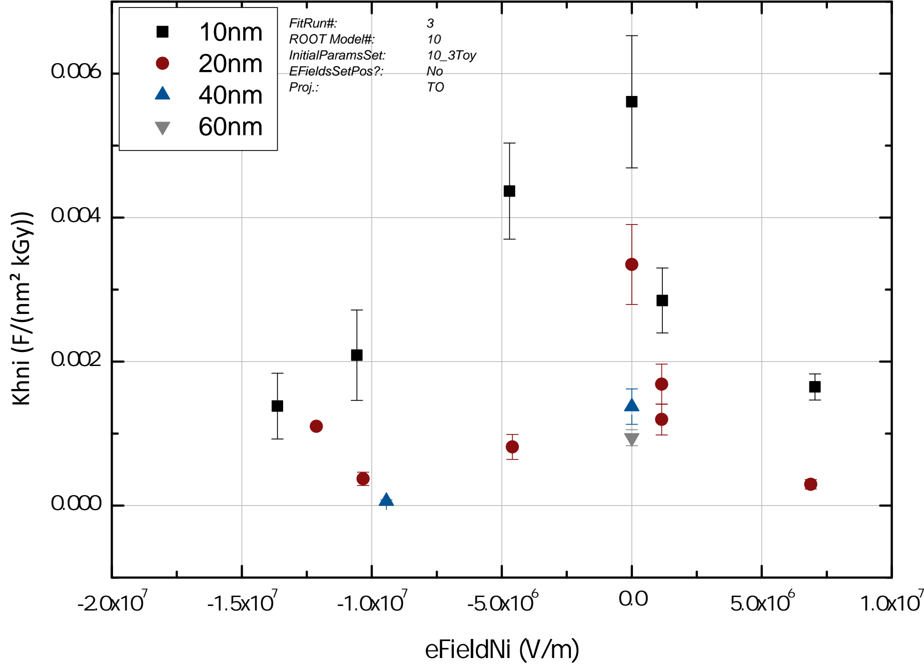


Figure 9.9.: Comparison of $Khni$ for available nitride thicknesses. Thicker nitrides could be treated similar to the 20 nm device.

much, or in the best case not at all, on the SiO_2 thickness, such an estimation is possible. In addition, choosing another nitride thickness than 10 nm or 20 nm can lead to false results, however as figure 9.9 indicates, thicker nitrides tend to behave similar to the 20 nm layer. Yet, since only little data is available for thicker nitrides, no conclusion can be drawn on this matter.

In figures 9.10 to 9.22 predictions by the model are shown together with corresponding data. The error areas were calculated using the values and errors given by the fits of the initial fit parameters. To these data points the fit functions (e.g. equation 9.6) were applied. The resulting errors on the parameters (p_i and q_i) were propagated to the appropriate equation and, together with the required electric field, values and errors for quantities of the model (i.e. $K's$ and G_{const}) were calculated.
The resulting range of these quantities was then given to a MC generator which randomly used this specific variable and its error (e.g. $Khni_{10} \pm \sigma_{Khni_{10}}$) to create variables in a Gaussian distribution. These values were then put into the solutions $q_{ox}(D)$ and $q_{ni}(D)$ of the differential equations 9.2 and 9.3.
The model parameters used for the predictions are listed in in table E.1 (appendix E).

In table 9.2 the observation of the studied DUTs is summarized. Some predictions deviate too much from the comparable data. In these cases, the likely cause for the discrepancy is listed along with the used parameters and the prediction.

A distinct reason for the partially bad behavior of the prediction is not trivially found. As can be seen from table 9.2 the worst prediction is found with the two devices E04 and N04. These two were irradiated with a zero gate bias, which resulted in a relatively low electric field in the oxide of $E_{ox_{E04}} = -8.8\ MV/m$ and $E_{ox_{N04}} = -9\ MV/m$, due to the

ChipID	Observation	Cause (Params in P)	V_G (V)	t_{ni} (nm)
A07	Curve shape reproduced well, M is higher than P (5V vs. 3V)	G_{const} is too low in P	-2.5	20
E04	P is bad (stays at 1V)	Khox too low (2 orders of magn.)	0	20
E05	Curve shape reproduced well, P is higher than M	G_{const} is too high	2.5	20
E07	At low doses OK, P lower than M at higher doses	Khox too low	5	20
G03	Good prediction (Gate)	-	2	20
I03	Good prediction	-	2.5	20
I04	Prediction is bad, M is higher than P (5V vs. 3V)	All K parameter too low	-5	20
J04	Prediction OK	Keox too low	-5	10
L03	Good prediction (Gate), P is higher than M	G_{const} too high	2	10
L04	P at low doses bad, fine at medium doses	Khox too low	-2.5	10
N04	Worst prediction	G_{const} much too low	0	10
N05	Good prediction	-	2.5	10
N07	Good prediction	-	5	10

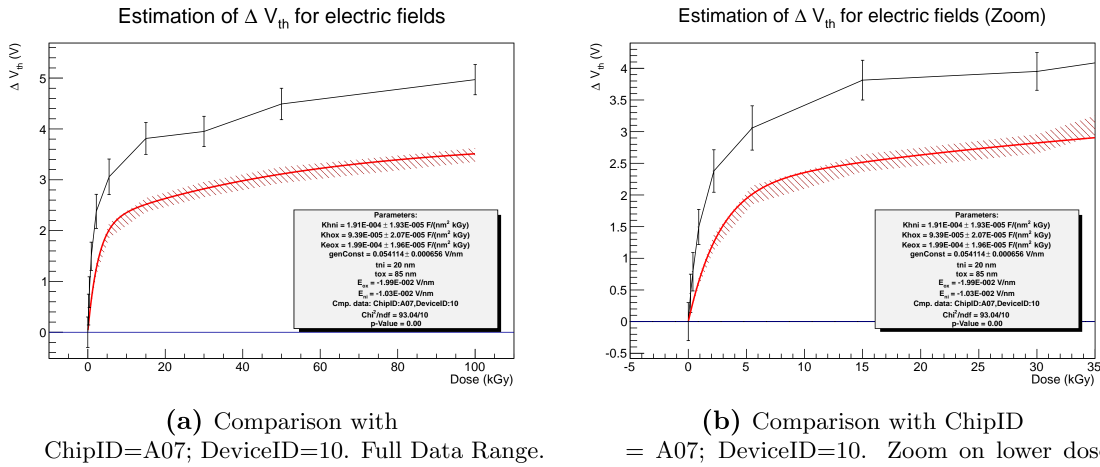
Table 9.2.: Overview between the Prediction P of the model and the measured data M for comparison.

aforementioned biasing scheme. At this field, the prediction of either $Khox$ or G_{const} is amiss for one of the devices.
Devices for which the predictions are also misaligned to the measured data are A07, E07, I04, and J04. With theses devices the origin of the misbehavior cannot be clearly identified. However, the likely candidates are the parameters $Khox$ and G_{const} from which most of the misalignment results.

This model excellently matches single datasets, i.e. MOSFETs with similar electric fields. Predictions, depending on nitride thickness and electric field in the insulators, are possible. Although the results are not entirely good, a model which is able to do so with sufficient precision has not yet been published.
A better fit/estimation to the model related parameters ($K's$ and G_{const}) with respect to the electric field would of course result in a better prediction. However, a reduction of the parameter space was necessary in order to prevent a simple reproduction of the data. Nevertheless, for a wide range of devices the estimation works well.

9.7. Summary and Conclusion

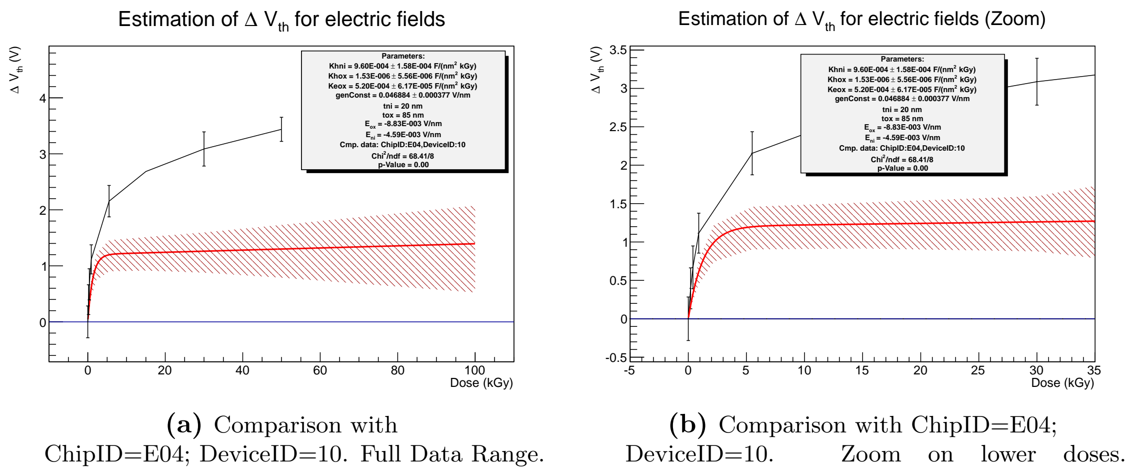
A model which is based on the idea of Raparla et al. [126] is presented. The basic mechanism is that the charge yield in the insulators depends on the electric field. By trapping of charge a counter electric field builds up, which reduces the charge yield at higher doses. In difference to the model by Raparla et al. [126] an additional charge yield parameter was introduced to take e.g. effects of diffusion of charge carriers into account.
Another difference is the dependence on the nitride thickness t_{ni} in the set of differential equations. This parameter was found to be negligible in the aforementioned publication ([126]).
Fitting of the model to a single dataset extracted from irradiations of the TO project worked quite well, however the fit is, due to the set of degrees of freedom, too good. By fitting si-



(a) Comparison with ChipID=A07; DeviceID=10. Full Data Range.

(b) Comparison with ChipID = A07; DeviceID=10. Zoom on lower doses.

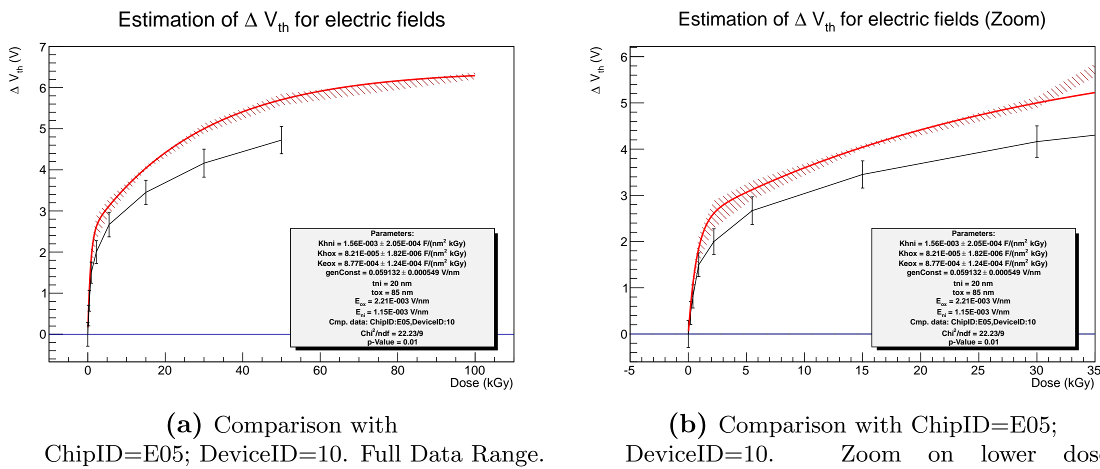
Figure 9.10.: Comparison of prediction (red) and measured data.



(a) Comparison with ChipID=E04; DeviceID=10. Full Data Range.

(b) Comparison with ChipID=E04; DeviceID=10. Zoom on lower doses.

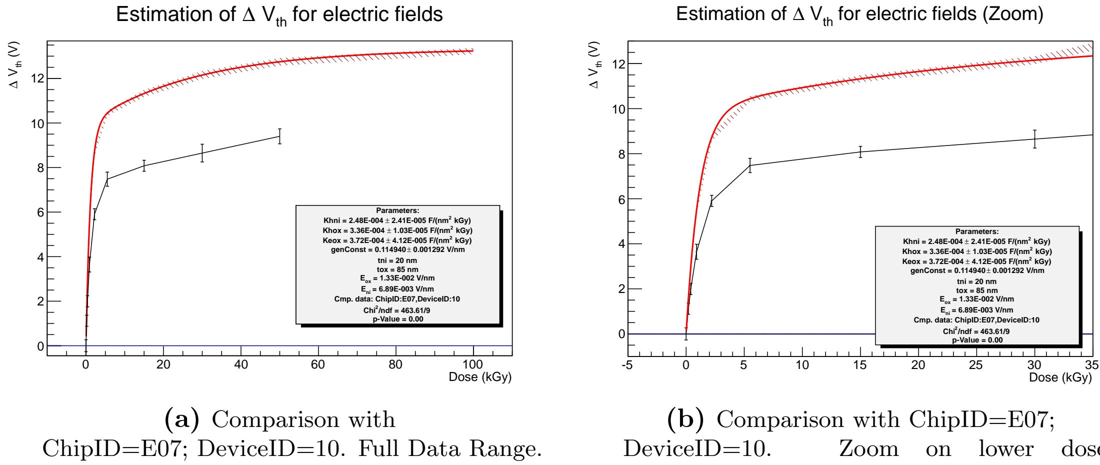
Figure 9.11.: Comparison of prediction (red) and measured data.



(a) Comparison with ChipID=E05; DeviceID=10. Full Data Range.

(b) Comparison with ChipID=E05; DeviceID=10. Zoom on lower doses.

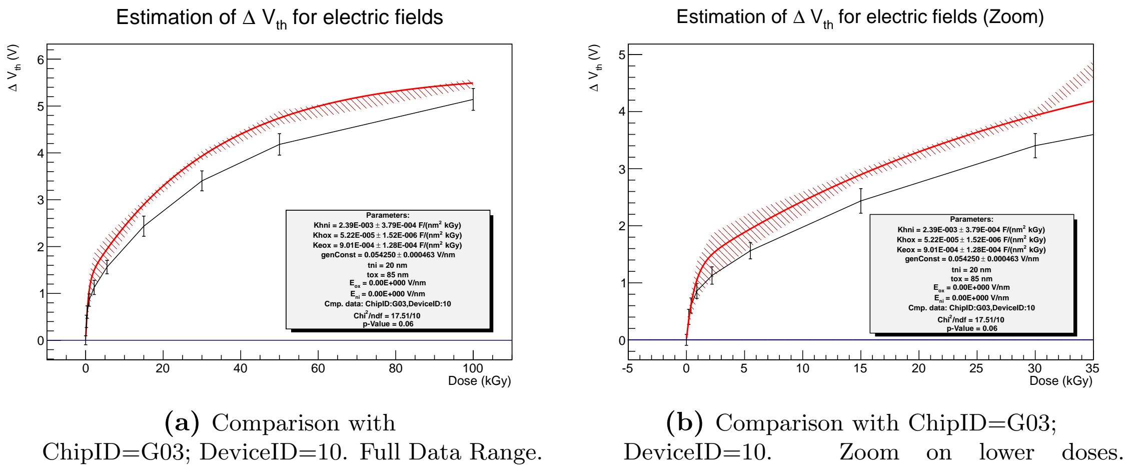
Figure 9.12.: Comparison of prediction (red) and measured data.



(a) Comparison with ChipID=E07; DeviceID=10. Full Data Range.

(b) Comparison with ChipID=E07; DeviceID=10. Zoom on lower doses.

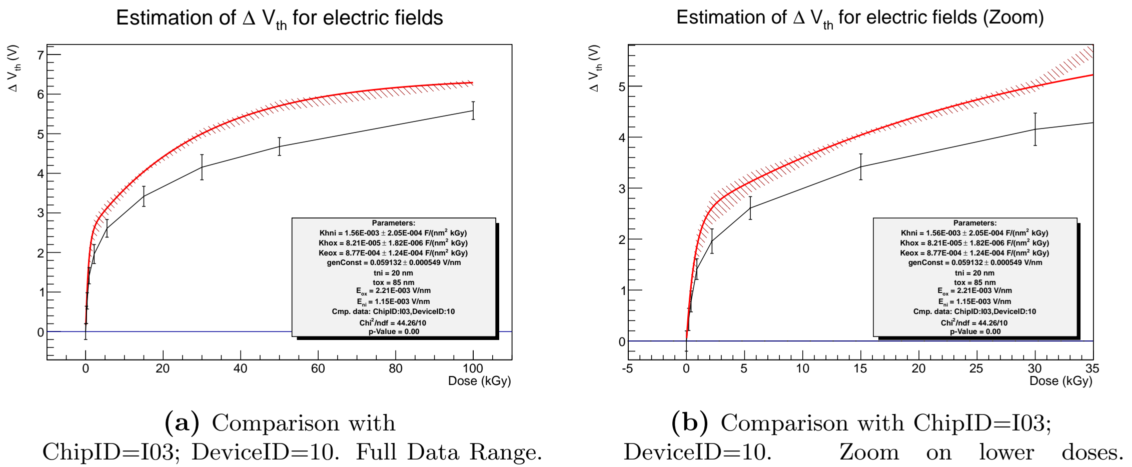
Figure 9.13.: Comparison of prediction (red) and measured data.



(a) Comparison with ChipID=G03; DeviceID=10. Full Data Range.

(b) Comparison with ChipID=G03; DeviceID=10. Zoom on lower doses.

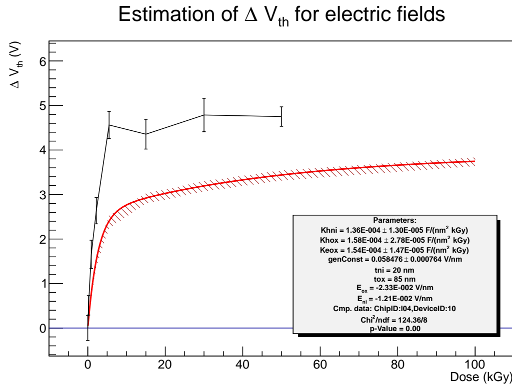
Figure 9.14.: Comparison of prediction (red) and measured data.



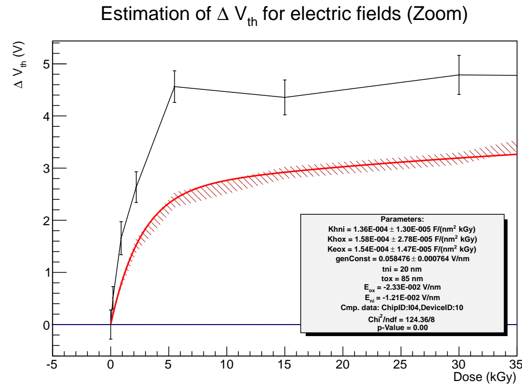
(a) Comparison with ChipID=I03; DeviceID=10. Full Data Range.

(b) Comparison with ChipID=I03; DeviceID=10. Zoom on lower doses.

Figure 9.15.: Comparison of prediction (red) and measured data.

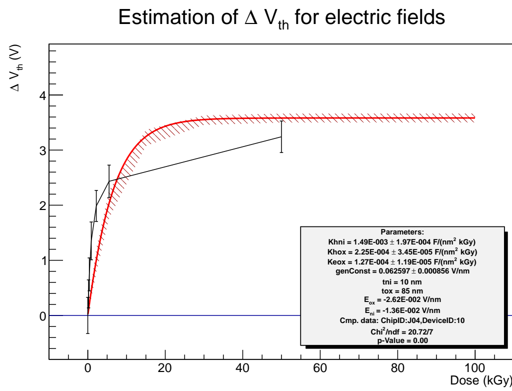


(a) Comparison with ChipID=I04; DeviceID=10. Full Data Range.

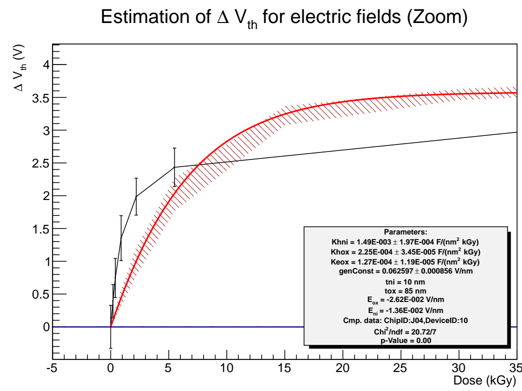


(b) Comparison with ChipID=I04; DeviceID=10. Zoom on lower doses.

Figure 9.16.: Comparison of prediction (red) and measured data.

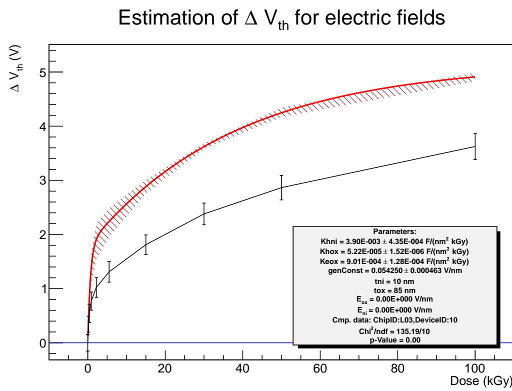


(a) Comparison with ChipID=J04; DeviceID=10. Full Data Range.

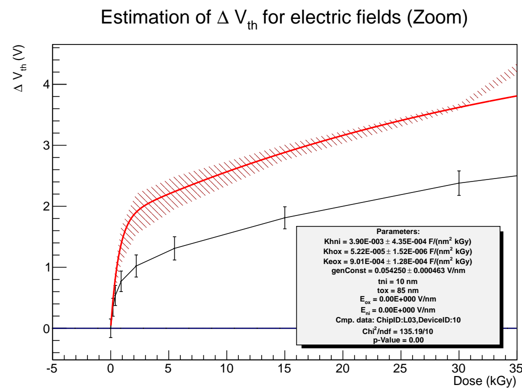


(b) Comparison with ChipID=J04; DeviceID=10. Zoom on lower doses.

Figure 9.17.: Comparison of prediction (red) and measured data.

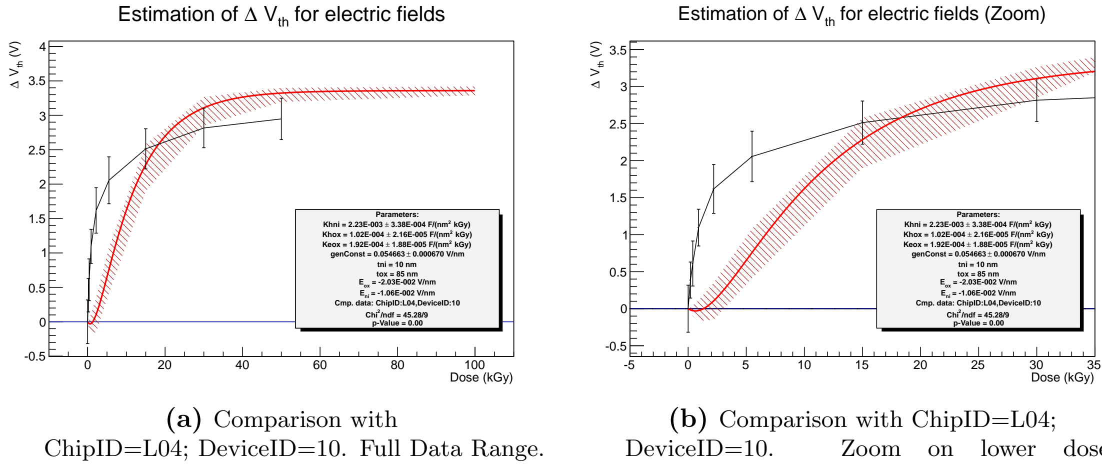


(a) Comparison with ChipID=L03; DeviceID=10. Full Data Range.



(b) Comparison with ChipID=L03; DeviceID=10. Zoom on lower doses.

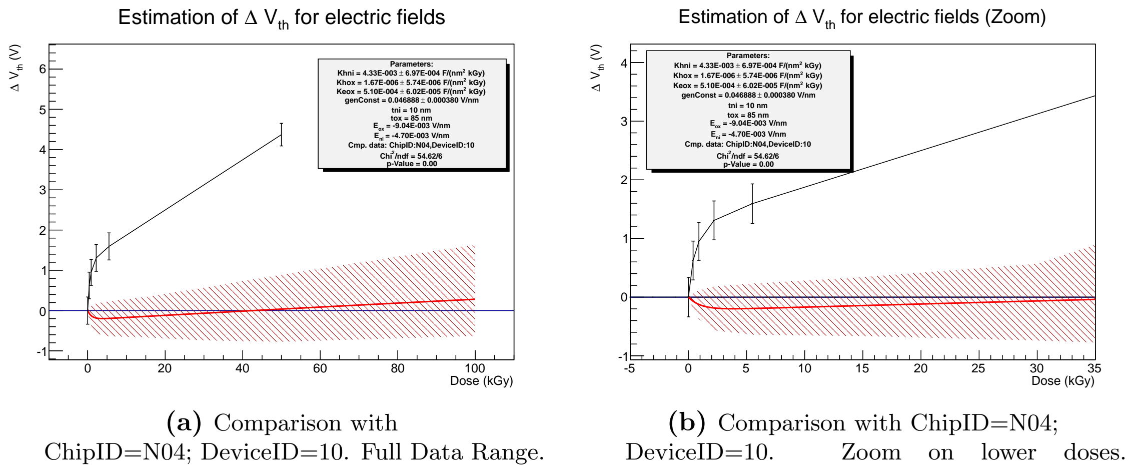
Figure 9.18.: Comparison of prediction (red) and measured data.



(a) Comparison with ChipID=L04; DeviceID=10. Full Data Range.

(b) Comparison with ChipID=L04; DeviceID=10. Zoom on lower doses.

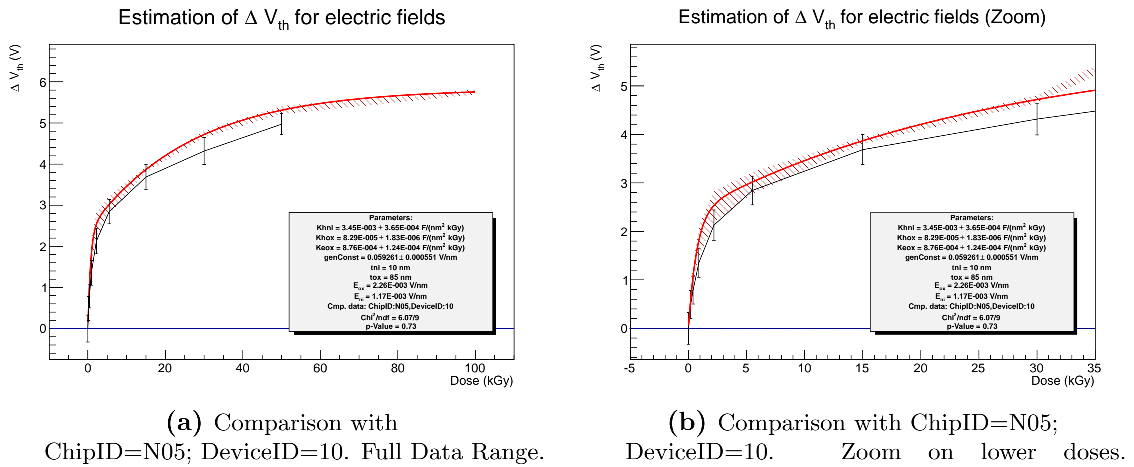
Figure 9.19.: Comparison of prediction (red) and measured data.



(a) Comparison with ChipID=N04; DeviceID=10. Full Data Range.

(b) Comparison with ChipID=N04; DeviceID=10. Zoom on lower doses.

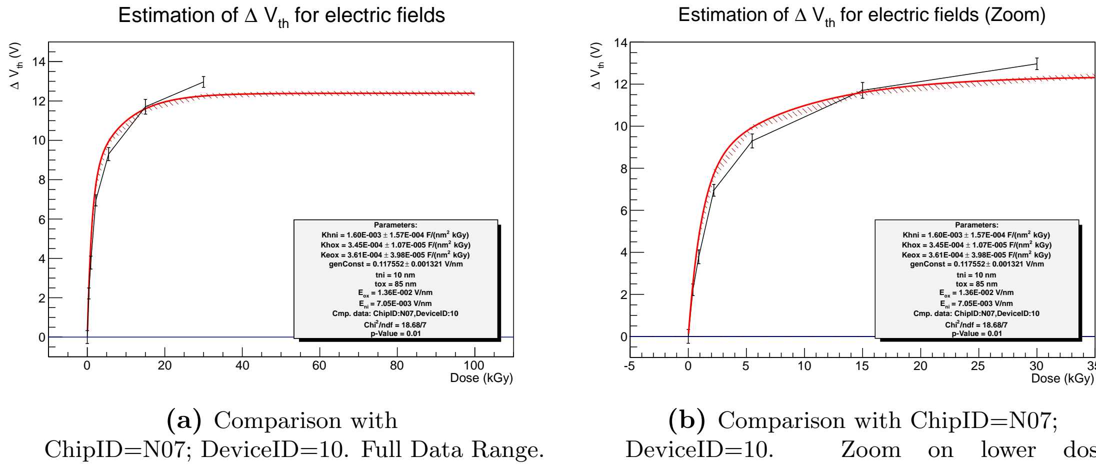
Figure 9.20.: Comparison of prediction (red) and measured data.



(a) Comparison with ChipID=N05; DeviceID=10. Full Data Range.

(b) Comparison with ChipID=N05; DeviceID=10. Zoom on lower doses.

Figure 9.21.: Comparison of prediction (red) and measured data.



(a) Comparison with ChipID=N07; DeviceID=10. Full Data Range.

(b) Comparison with ChipID=N07; DeviceID=10. Zoom on lower doses.

Figure 9.22.: Comparison of prediction (red) and measured data.

multaneous datasets it turned out that only similar datasets in the electric field could be described by one set of parameters. Since transport equations of charge carriers in the insulators are not included in the model, the effects of drift motion and charge capturing had to be hidden in the free parameters.
By creating a look-up function for each parameter depending on the electric field (and in one case on nitride thickness), a good agreement of prediction and measured data could be found. However, the error bars only include the errors from the look-up function. In order to make a proper prediction, these errors should be treated carefully and are certainly bigger than depicted. Neglected effects are e.g. uncertainties in dose, temperature, and annealing. In addition, this model describes the devices from the TO project quite well, however as literature indicates (e.g. in [60]), differences in the production process can cause considerable differences in the radiation hardness of a device.

The model on the radiation damage of MNOS devices could of course be extended and refined. An extension could incorporate the motion of charge carriers in the insulator and treat electrons from the oxide and nitride differently. After an appropriate drift/diffusion process in the insulators the created charge carriers could then either get trapped at defect sites or escape. This would depend on a capture cross-section for the charge carrier type. Additionally the presented model reveals no information on the spatial location of traps. A further improvement would include the trap precursor density of the oxide trapped charge E'. This quantity could then depend on the production process and thus could lead to better results, e.g. if a prediction for a wet oxidation process was desired.
Yet, the aforementioned extensions would introduce many new parameters, thus a dedicated measurement/irradiation program would have to accompany such extensions in order to test the new hypotheses.

Chapter 10.

Estimations of the DEPFET Performance in Belle II

The data and conclusions extracted in this thesis so far can help to predict the behavior of the DEPFET and the PXD in the radiation environment of Belle II.
The first part is dedicated to the noise and signal of the DEPFET. The accumulated dose during the operation of Belle II changes the DEPFET characteristics and the question arises in which way this will affect the signal of the PXD.
The second part focuses on an inhomogeneous irradiation along the z-axis of the detector (i.e along the modules of the PXD). This irradiation in the PXD would lead to a spread in drain currents of differently irradiated parts of the detector matrix. Different scenarios for different dose rates in the PXD are presented.

10.1. Expected DEPFET Signal Performance

10.1.1. Introduction

As in all detectors noise plays a crucial role in the PXD. In order to have a sufficient signal, the amplification of the system has to be high enough. Since the DEPFET is the device first in line, its characteristics can dominate the read-out chain. A good internal amplification g_q can reduce the influence of noise generated by devices later in the read-out chain.
The view on the signal strength alone is not sufficient, therefore in section 10.1.3 a closer look is taken at the various noise sources and how they influence the behavior of the PXD. One source of noise depends on the temperature. This shot-noise of the bulk is evaluated in section 10.1.4 and a tolerable temperature is presented.
Noise and signal eventually lead to an assessment of the detector efficiency, shown at the end of this section.

10.1.2. Required Internal Amplification

One design parameter of the DEPFET is the internal amplification g_q. As already mentioned in section 3.4.3 the reduction of the oxide thickness requires a decrease in the gate length L in order to satisfy reasonable amplification.
The sections on noise from various sources of the DEPFET (cf. section 5.2.2 and 6.3.3) have shown that the noise which is produced in the detector still is small. Instead the digitization in the read-out ASICs adds considerable noise. The DCD exhibits at the moment a typical noise in the order of $\sim 100\ nA$, although it is specified to 40 nA. For digital algorithms used in reconstruction and analysis the figure of merit is the Signal-to-Noise Ratio (SNR).

Typically a value of ~ 20 is considered sufficient. This leads to a required signal current produced by the DEPFET of $I_{DS_{Sig}} = 2\ \mu A$. With reference to a typical charge deposition (cf. section 5.2.2) of $Q_{MIP} \sim 4800\ e^-$, the required amplification is given by

$$g_{q_{req}} = \frac{I_{DS_{Sig}}}{Q_{MIP}} = 416 \frac{pA}{e^-}. \tag{10.1}$$

10.1.3. Noise Overview

In the aforementioned chapters on bulk and surface damage several noise sources are presented. In the PXD the noise sources contribute to a total noise according to the equation

$$N(T) = N_{leak}(T) \oplus N_{surf} \oplus N_{DCD} \oplus N_{PT}, \tag{10.2}$$

in which $N_{leak}(T)$ is the strongly temperature dependent noise of the bulk generated leakage current and N_{surf} the noise originating from surface generated currents. N_{DCD} and N_{PT} represent the noise of the DCD and the noise arising due to the punch-through mode of the DEPFET. The different sources have to be added quadratically, designated by the $\oplus$ operator. In equation 10.2 not all noise sources are listed, e.g. the 1/f noise of the MOSFET channel was neglected. Other sources, such as the analog-to-digital noise of the DCD are included in the the total noise of the DCD.
In section 5.2.2 it is shown that the noise which originates from the punch-through mode can be neglected as well as the temperature dependence of the surface generated current (cf. section 6.3.3).

With a signal charge of $\sim 4800\ e^-$ and a tolerable SNR of ~ 20 a maximum noise level of $240\ e^-$ can be tolerated. This noise is composed of:

1. The DCD contributes $100\ nA$, which results with an estimated $g_q = 500\ pA/e^-$ into $N_{DCD} = 200\ e^-$.
2. Surface generated current and its noise can be estimated to $N_{surf} \approx 45\ e^-$ after $100\ kGy$. The data from figure 6.25 indicates that at higher doses the increase saturates. Thus, a $N_{surf} \approx 50\ e^-$ is assumed after $40\ ab^{-1}$
3. The bulk generated leakage current. After $40\ ab^{-1}$ the leakage current has reached $I_{leak_{40}} = 1.5 \cdot 10^{-11}\ A/pixel$ with its corresponding noise (e.g. $43\ e^-$ at $T = 293\ K$).

Although the noise of the DCD dominates the total noise, an assessment of the temperature dependence of the shot-noise from the bulk is presented in the next section 10.1.4.

10.1.4. Tolerable Temperature

The temperature dependence of the leakage current follows equation 5.1. With the data given above the noise from the leakage current $I_{leak_{40}}$ after an integrated luminosity of $40\ ab^{-1}$ can be calculated and is shown in figure 10.1 (together with the behavior after $80\ ab^{-1}$).

The presented data shows that after an acquired integrated luminosity of $40\ ab^{-1}$ roughly $43\ e^-$ contribute to the already quite high noise. However, the contribution from the DEPFET itself is still smaller than the contribution of the DCD. In light of this argument, DCDs of the next generation are likely to have better noise performance.
Two scenarios are discussed:

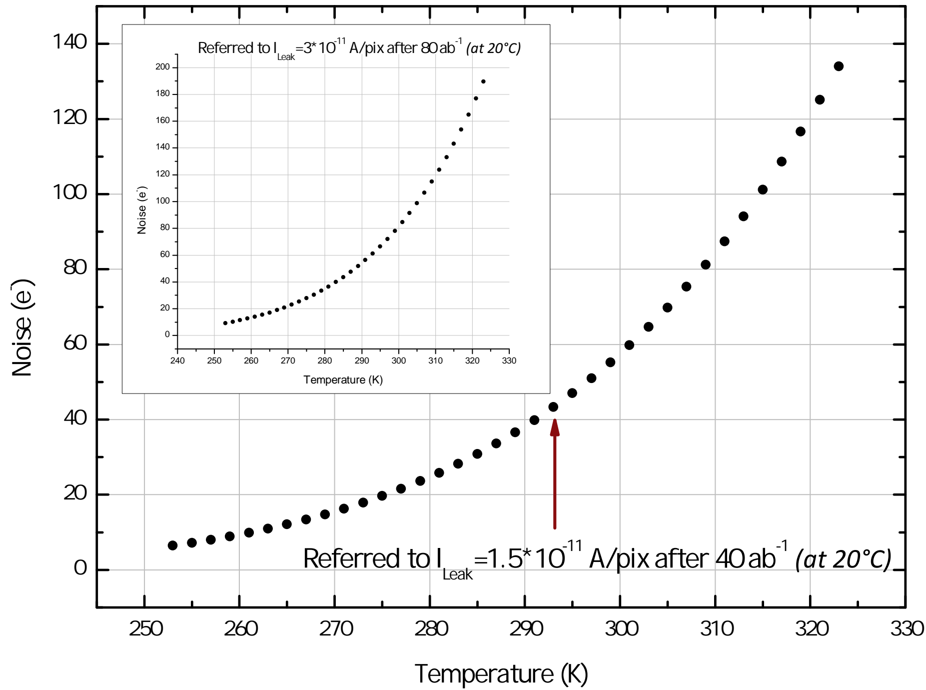


Figure 10.1.: Noise contribution from the bulk generated leakage current after an integrated luminosity of 40 ab^{-1}. At room temperature $\sim$ 43 e^{-} contribute to the noise in the internal gate. The embedded data shows the situation after an integrated luminosity of 80 ab^{-1}.

1. Assuming the nominal noise performance of 40 nA results in a considerably smaller noise charge of 80 e^{-}. Thus the tolerable temperature in which $N_{leak}(T) = 231\ e^{-}$ would be $> 330\ K$. Even after a doubled acquired luminosity of 80 ab^{-1} the DEPFET would perform fine.

2. Assuming the present DCD version, with 200 e^{-} noise. This scenario would result in a tolerable temperature due to $N_{leak}(T) = 122\ e^{-}$ of 320 K (= 47 °C) after an integrated luminosity of 40 ab^{-1}. Even after 80 ab^{-1} a temperature of 312 K (= 39 °C) could be tolerated.

These results imply a more relaxed temperature scenario (and cooling scenario) for the PXD, however the best performance depends on a better noise behavior of the DCD. Further reading on the cooling of the PXD can be found e.g. in [129, 130].
In addition, if a better SNR was required, the limits on tolerable noise would be tightened. E.g. a SNR of $\sim$ 30 could not be achieved with the present version of the DCD.

10.1.5. Detector Efficiency

The drain current from the DEPFETs in the PXD is read-out by the DCD. The amount of drain current necessary to sustain a sufficient internal amplification is given by equation 3.49.
A conservative estimation for the various drain currents includes:

1. A $SNR = 20$, leading to a noise level of $N = 240\ e^{-}$ in the DEPFET.

2. A sufficiently low occupancy in the PXD of 0.1%. This requires a noise-cut N_{cut} of 6.6 σ ([131]). Such threshold levels can be set by the DHP.

3. A minimum required internal amplification according to equation 10.1.

4. The input range of the ADC of the DCD.

With the stated numbers the cut on the drain current can be calculated to be

$$I_{cut} = N_{cut} \cdot g_{q_{req}} = 6.6 \cdot 240\ e^{-} \cdot g_{q_{req}} = 1584\ e^{-} \cdot 416 \frac{pA}{e^{-}} \approx 659\ nA. \tag{10.3}$$

The resolution of the DCD is given by the input range over the amount of available sampling bits, thus

$$res = \frac{8\ \mu A}{128\ ADU} = 62.5\ \frac{nA}{ADU}. \tag{10.4}$$

With these values, the cut on the current corresponds to 10.5 ADU. The efficiency of the PXD can be estimated via figure 10.2 to be at least better than 91%, since the figure corresponds to a test beam module from the production PXD 6 which exhibited a bulk thickness of $d_{Si} = 50\ \mu m$. DEPFETs for Belle II are being produced on a bulk with $d_{Si} = 75\ \mu m$, which will lead to a higher signal.
Figure 10.2 may correspond to a final DEPFET module if the seed signal axis is scaled with the relative thickness $\frac{50\ \mu m}{75\ \mu m} = 0.66$. Thus the cut of 10.5 ADU corresponds to $\sim 6.9\ ADU$, leading to an efficiency of $\sim 97\%$.
As a comparison, the same calculation for a $d_{Si} = 50\ \mu m$ device from PXD 6 results in a cut on 6.3 ADU. Here, the signal charge from equation 5.11 is $S_{50} = 3194\ e^{-}$. Thus a lower noise of $N_{50} = 133e^{-}$ results from the $SNR = 24$, which is achieved with PXD 6 devices (assuming a conservative $g_q = 450\ \frac{pA}{e^{-}}$[1]). This leads to a good efficiency of $> 98\%$.
Similar or even better results than the abovementioned $\sim 97\%$ can be expected for the PXD due to the thicker silicon bulk and an optimized internal gate.

10.2. Influence of Inhomogeneous Irradiation

10.2.1. Motivation

The main radiation background in the PXD originates from the 4-fermion final state radiation (cf. section 2.4.2). Although the dose delivered by this type of radiation is considerable, an additional problem could arise if the dose distribution of all sources combined was inhomogeneous along the z-axis of the detector. From Belle (I) such a scenario does not seem so unlikely. Figure 10.3 shows a hit distribution for the first layer of the former SVD.

The shift in the threshold voltage is one of the main manifestations of surface damage. Due to the issue of a z-axis dependency of ΔV_{th} a three-fold segmentation is introduced for each half ladder. Thus, regions of the modules can be independently biased with gate and clear gate voltages due to this segmentation.
At the moment the simulations of the background distribution indicate similar dose variations along the z-axis of the detector. Figures 10.4 and 10.5 show a present simulation of the background along z.

[1] In beam tests a $g_q \sim 500\ \frac{pA}{e^{-}}$ was achieved ([132]). In [125] a corresponding $g_q \sim 480\ \frac{pA}{e^{-}}$ is stated.

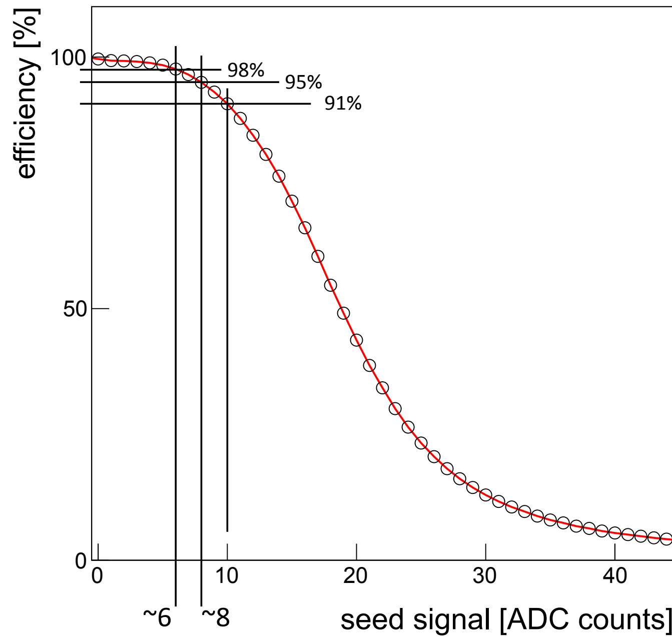


Figure 10.2.: Efficiency for a PXD 6 module in the test beam of 2012 with MIPs of perpendicular incidence. It exhibited a silicon bulk thickness of $d_{Si} = 50$ μm, *taken from [125].*

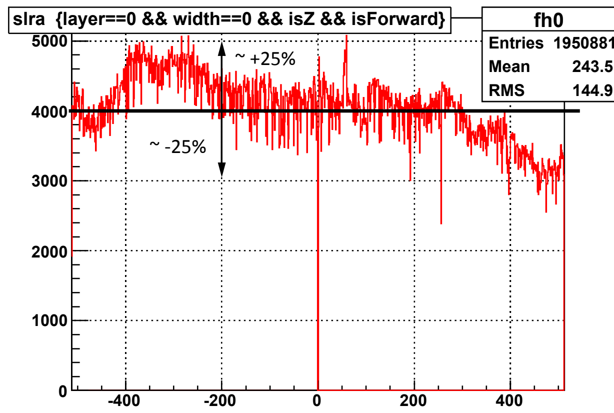


Figure 10.3.: Hit distribution from Belle in layer 1 of the former SVD along the detector z-axis [133]. A peak to peak difference of roughly ±25 % is visible.

From this data small variations in the order of $\approx \pm 10\%$ should be taken into account. However, the issue of a highly irradiated region should not be neglected. This issue is represented by a $+30\%$ variation in the later discussed scenarios (see section 10.2.3).

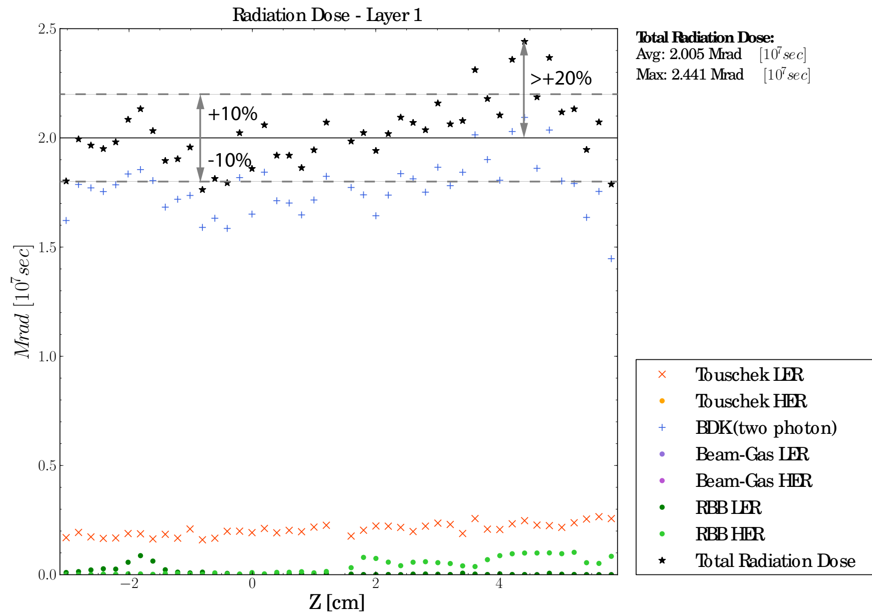


Figure 10.4.: Dose distribution from all relevant background sources for the first layer of the PXD. Six segments are available in total along the z-axis. The highest variations take place in the edge segments. *Courtesy of Moll [24], current status of simulation.*

10.2.2. Impact on the PXD

The problem of inhomogeneous irradiation will manifest in two ways in a DEPFET. First, as a shift in the threshold voltage and second, as a degradation of g_m. Additionally, the differences from higher to lower irradiated regions in the PXD will increase with the ongoing operation of Belle II.
The regions with a higher dose rate will decrease their threshold voltage further. In order to turn those DEPFETs on, the DEPFETs from parts with smaller dose rates will exhibit a higher drain current. This difference has to be compensated by the read-out ASICs.

Depending on the scenario, a degradation of g_m can lead to either worse or better situations. This depends strongly on the adaption of the gate voltage for the reference region. At higher doses the degradation in g_m leads to a lesser sensitivity of the current to a change in gate voltage. Thus, if a more irradiated region is chosen as a reference, the gate voltage, with respect to the accumulated dose ($\sim \int \mathcal{L} dt$), can be adapted to a lesser degree. With the reduced adaption, the lesser irradiated regions exhibit a smaller current increase or, due to the degradation of g_m, may even have a current reduction.

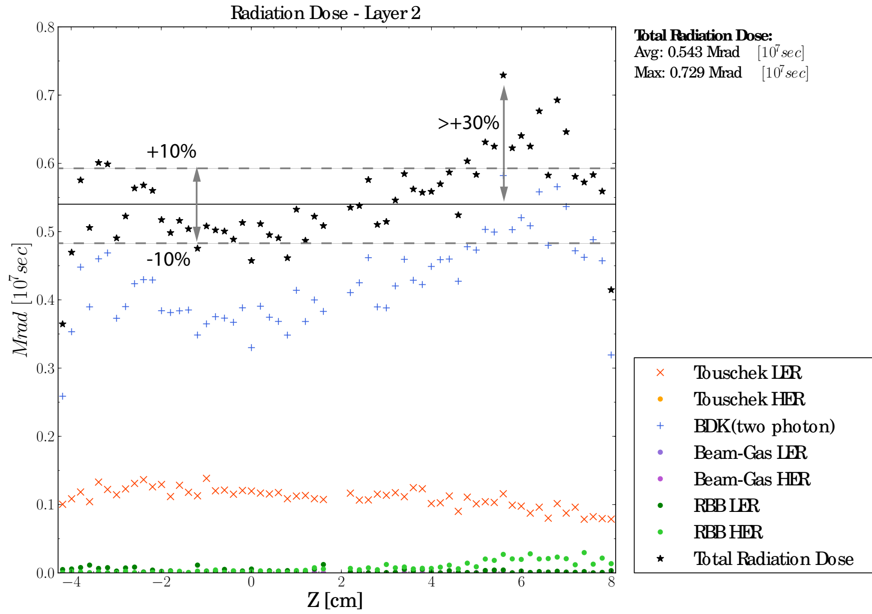


Figure 10.5.: Dose distribution from all relevant background sources for the second layer of the PXD. In the outer layer of the PXD the variations are higher (especially in the edge segments) yet the dose rate is small. *Courtesy of Moll [24], current status of simulation.*

Tolerable Difference in the Threshold Voltage

In order to estimate the tolerable difference in the threshold voltage of the highest and least irradiated regions, due to inhomogeneous irradiation, within one segment, several considerations are necessary.
The internal amplification depends on the drain current (equation 3.49). Thus in order to fulfill the required internal amplification of 416 $\frac{pA}{e^-}$, a corresponding minimal drain current $I_{D_{min}}$ is needed. Investigations in [134] show that for a DEPFET with a gate length of $L = 5\ \mu m$ a minimal current of

$$I_{D_{min}} = 35\ \mu A \tag{10.5}$$

is needed.

The maximum drain current $I_{D_{max}}$ which can be tolerated by the DCD is given by the features of the DCD. These are:

1. A current source, which can subtract a maximum of $I_{cs} = 24\ \mu A$ in four steps (two bits resolution) from the drain current.

2. A common mode correction of 200 μA. This correction is introduced to cancel noise effects, which are common in one row of the module. The manifestation of inhomogeneous irradiation is similar to this effect, since one row differs in their pedestal current from another.

3. The aforementioned ADC resolution of $res = 62.5\ \frac{nA}{ADU}$ and a range of $2 \cdot 8\ \mu A$.

In case of an applied common mode correction the maximum drain current is given by

$$I_{D_{max}} = 200\ \mu A - 8\ \mu A(ADC) = 192\ \mu A, \tag{10.6}$$

or, if this correction is not in effect, it is given by

$$I_{D_{max}} = I_{D_{min}} + I_{cs} + 8\ \mu A(ADC) = 67\ \mu A. \tag{10.7}$$

The gate voltage V_G in this estimation is determined by the least irradiated region. In this region, the highest current $I_{DS,LowDose}(V_G)$ flows. In order to max out the dynamic range of the DCD this value is limited by $I_{D_{max}}$. The corresponding $V_G = V_0$ for the highest irradiated region is the same in one segment due to the design of the module. In this region, a smaller current $I_{DS,HighDose}(V_G)$ flows. However, to max out the available range, this current still has to deliver the minimal amount of $I_{D_{min}}$. The question is by which amount of ΔV the input characteristic of the DEPFET can be shifted.
For this issue, the two equations

$$I_{DS,LowDose}(V_0) = I_{D_{max}} \tag{10.8}$$

and

$$I_{DS,HighDose}(V_0 + \Delta V) = I_{D_{min}} \tag{10.9}$$

have to be fulfilled.
For the two aforementioned possibilities of the DCD, i.e. with and without common mode (CM, $\overline{CM}$), two solutions can be calculated. They are given by

$$\Delta V_{CM} = 2.47\ V, \tag{10.10}$$

$$\Delta V_{\overline{CM}} = 0.7\ V. \tag{10.11}$$

The procedure is illustrated in figure 10.6a when the common mode correction is in effect and in figure 10.6b when it is not. Clearly, the common mode correction tremendously enhances the ability of the PXD to handle inhomogeneous irradiation.

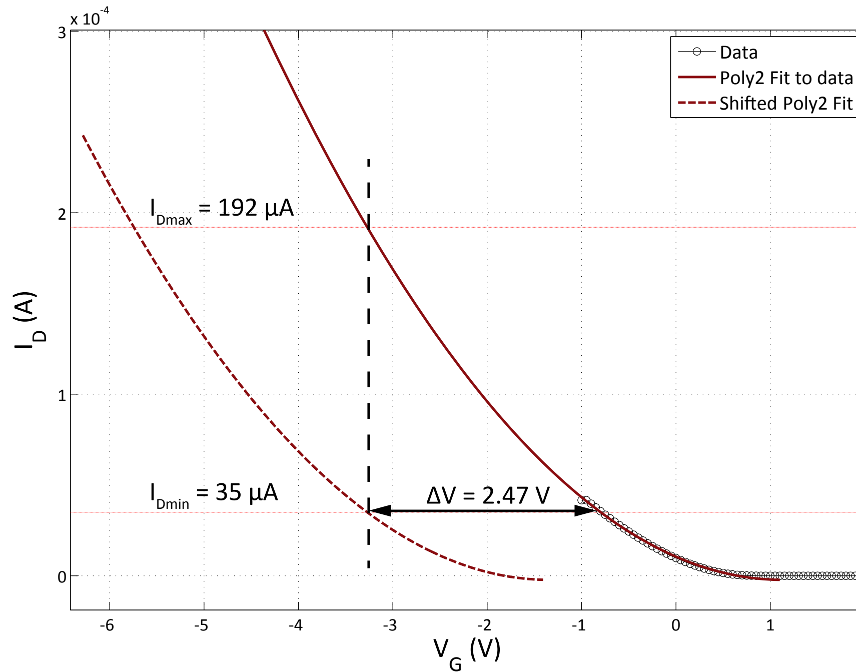
However, to max out the available range of the DCD may lead to complications. The highest possible drain current of $I_{D_{max}} = 192\ \mu A$ results in a higher internal amplification. Studies in [134] show that for such I_{DS} a $g_{q,max} = 600\ \frac{pA}{e^-}$ is achieved. This will increase the typical MIP signal of $S = 4792\ e^-$ to a signal current of

$$I_{sig,MIP} = 2.88\ \mu A. \tag{10.12}$$

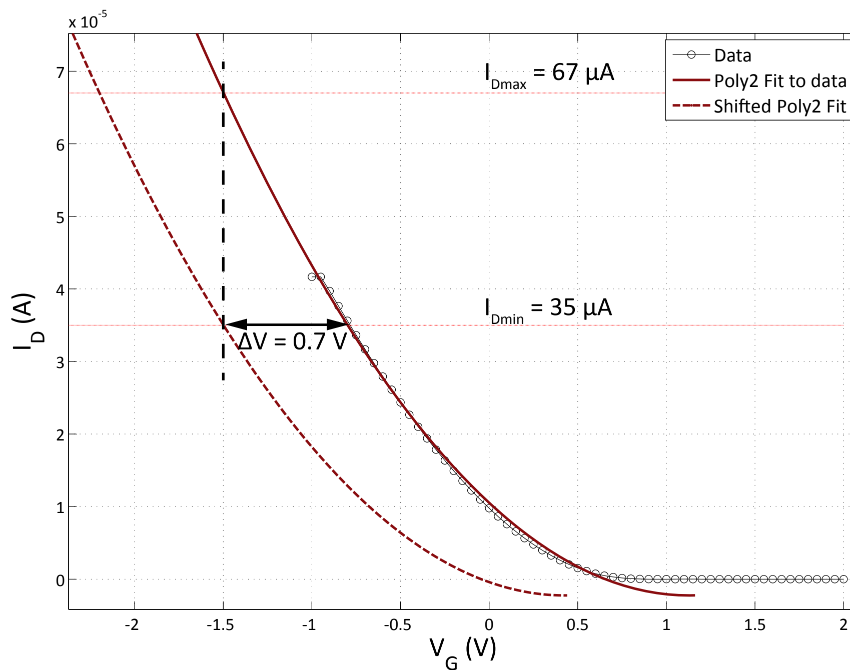
Thus, only two MIP particles of perpendicular incidence can be resolved, while in the nominal amplification case four MIPs could have been detected.
The detection of pions with a low momentum may become even harder. A considerable fraction of those pions deposits $S_{pion} \sim 30000\ e^-$ in one pixel [135]. When taking the above conditions into account, this deposition results in a signal current of

$$I_{sig,pion} = 18\ \mu A. \tag{10.13}$$

This value exceeds the range of the ADC and could thus not be resolved. A saturated pixel would be the consequence. In order to tag this particle, the value of $I_{D_{max}}$ would have to be lowered, leading to a reduced range for ΔV.
In order to incorporate the inhomogeneous irradiated regions, a safer operating of the detector requires the common mode correction ability of the DCD. In the worst case, for a pixel with the highest drain current and therefore the highest g_q a signal range of $S_{poss} = 13300\ e^-$ still remains.



(a) Scenario with common mode correction applied.



(b) Scenario without the common mode correction.

Figure 10.6.: Maximum tolerable voltage shift for two scenarios. The weakest irradiated pixel (shown with data points and a corresponding fit) delivers the maximum drain current $I_{D_{max}}$ and sets V_G. Thus, the highest irradiated pixel (red dashed line) exhibits a smaller current.

10.2.3. Drain Current Scenarios

Introduction

The impact of inhomogeneous irradiation is estimated by evaluating five scenarios, summarized in table 10.1. Scenario 1 is aimed at a harsh condition. Upon a 10% variation of the dose rate a 30% is included and set as a reference for the drain current of $I_{DS_{ref}} = 80\ \mu A$. This means that the highest irradiated region is to deliver $I_{DS_{ref}}$, which means the same gate voltage results in a lesser irradiated region in a higher drain current.
Scenario 2 is in principle the same as scenario 1, but this time the reference is on a +10% variation. In the other two following scenarios the drain current is lowered in order to investigate if the spread in drain currents can be reduced.
Scenario 5 differs from all the former ones, since a degradation of g_m is excluded. During the production of PXD 6 devices a small p implantation is placed beneath the external gate in order to adjust the initial threshold voltage to $V_{th}(0\ kGy) \approx 0\ V$. However, the ion implanter has to penetrate the gate insulator. As only parts of the PXD 6 wafer exhibit a thin oxide, the implanting parameters were set for a penetration through thick insulators resulting in a deeper implantation in the devices studied in this work.
In the final DEPFETs the implanting parameters will be set to the appropriate insulator thickness. From this parameter a lesser reduction in the transconductance g_m is envisaged.

Scenario	Avg. dose rate	Ref. dose rate var.	$I_{DS_{ref}}$
Scen. 1, Max	2.5 kGy ab	+0.75 kGy ab	80 μA
Scen. 2, Medium	2.5 kGy ab	+0.25 kGy ab	80 μA
Scen. 3, Max + low I_{DS}	2.5 kGy ab	+0.75 kGy ab	35 μA
Scen. 4, Medium+low I_{DS}	2.5 kGy ab	+0.25 kGy ab	35 μA
Scen. 5, g_m	2.5 kGy ab	+0.25 kGy ab	80 μA

Table 10.1.: Different dose scenarios for inhomogeneous irradiation

Estimation Method

The measurement data consists of $I_{DS}(V_G)$ data for certain dose values. In this estimation, a dose rate for the different scenarios defines each simulation step. Therefore missing data for a dose D_{sim} defined by the simulation has to be generated.
A polynomial fit of the form $I_{DS} = p_1 V^2 + p_2 V + p_3$ is applied to the data. The parameters p_i of the fits can then be interpolated at the desired dose value. This procedure is illustrated in figure 10.7.

An interpolation is always a source of error and thus disputable. However, as figure 10.7 shows, the algorithm performs well. Regions where no data is available (i.e. $D < 0\ kGy$ and $D > 100\ kGy$) remain uncertain to a higher degree, since the interpolation algorithm lacks a sufficient derivative at this points.

After a certain integrated luminosity parts of the modules are differently irradiated. Depending on the scenarios the appropriate dose is calculated and the fit parameters are interpolated. The interpolated parameters p_i yield a data function of the drain current I_{DS}.

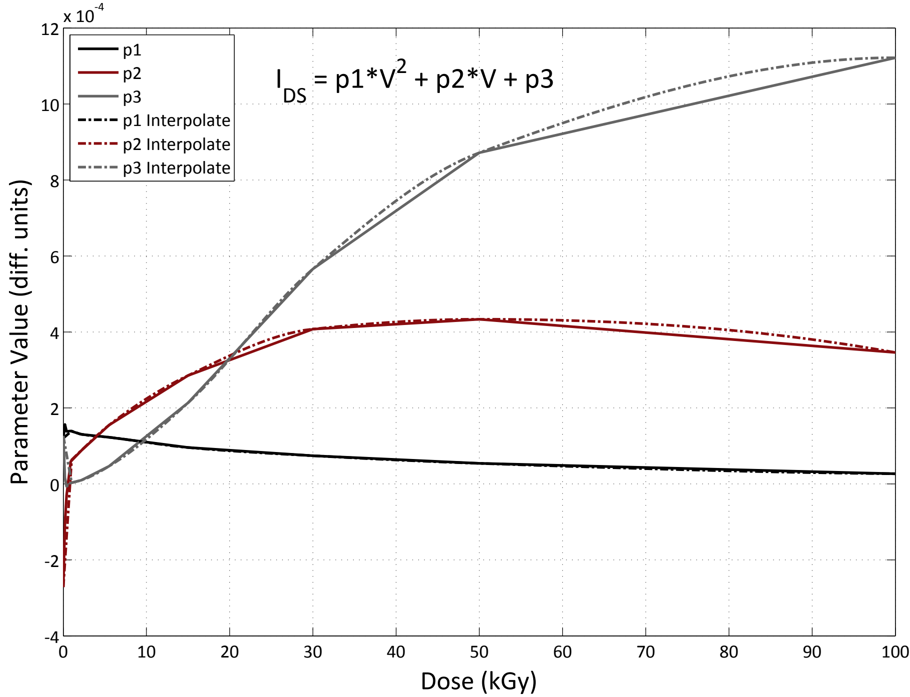


Figure 10.7.: Dependency of the second order polynomial fit parameters with respect to dose. The dashed lines show the applied interpolation algorithm.

The reference region has to deliver the current required by the scenario (cf. table 10.1). The required gate voltage for this current V_{ref} is now the same for all other regions within one segment of the module. The current for the different regions, e.g. $I_{DS,max} = p_{1,max} \cdot V_{ref}^2 + p_{2,max} \cdot V_{ref} + p_{3,max}$, can then be calculated.
The data from the input characteristics is taken from the measurements of the gate equivalent DUT 06U with gate length $L = 5\ \mu m$ (cf. figure 7.9a).
The data for the fifth scenario is generated by the data from the input characteristic $I_{DS}(V_G)$ of the unirradiated measurement. This data is then shifted by the threshold voltage shift ΔV_{th} to $I_{DS}(V_G + \Delta V_{th})$ of this DUT for higher doses. In this way, the degradation of g_m is omitted.

Results

The different dose rates in the scenarios lead to spread in the threshold voltage. This spread is in first-order independent of the scenario in place (corrections to a different biasing during the operation have been neglected) and increases with the ongoing operation of the PXD. This issue is depicted in figure 10.8.

The evolution of the drain currents in scenario 1 is shown in figure 10.9. In this figure, the hard limit by the common mode correction of the DCD (equation 10.6) is shown together with the currents. The highest irradiated region exhibits an $I_{DS} = 80\ \mu A$ and thus the lesser irradiated regions have an increased current flowing. The estimation is stopped at $\sim 31\ ab^{-1}$ since at this point the highest dose rate of $3.25\ kGy\ ab$ exceeds the available data of $D = 100\ kGy$.

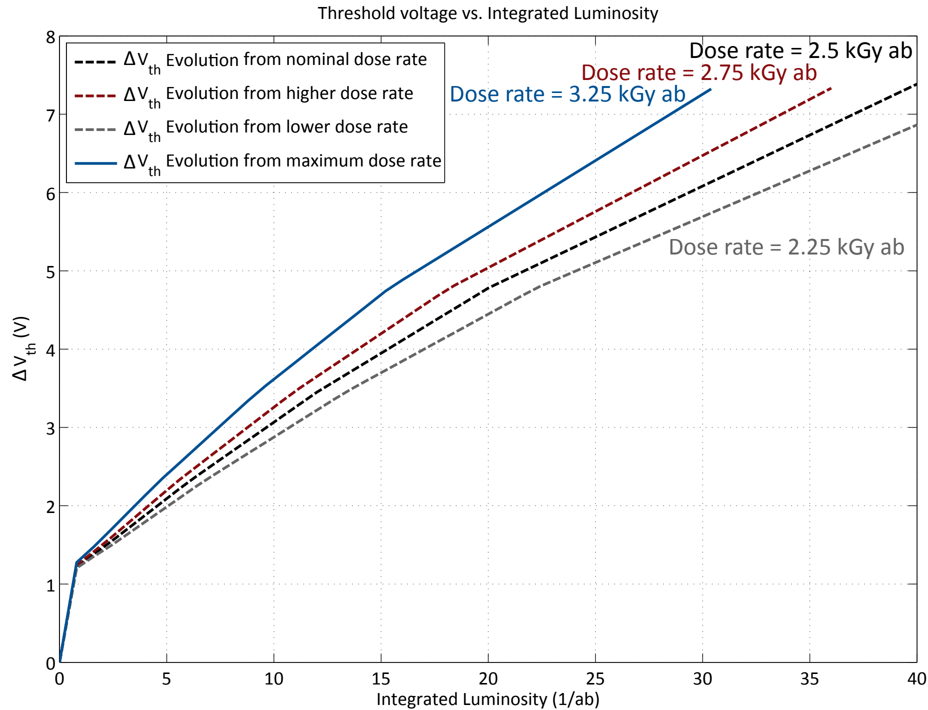


Figure 10.8.: Different dose rates lead to a spread of the threshold voltage with respect to the integrated luminosity.

The spread in the currents is reduced after $\sim 26\ ab^{-1}$. This effect has two sources: the adaption of the gate voltage and the reduction in g_m. At this point, the adaption of the gate voltage deviates from the pattern which can be observed at a lower integrated luminosity (cf. figure 10.10). Since the threshold voltage increases almost linearly at higher doses with the DUT, the adaption of the gate voltage follows this pattern. However, with higher doses the g_m reduces, thus the gate voltage has to be increased to a lesser degree. This reduces then the current of lesser irradiated regions, since there an ongoing linear adaption of the gate voltage would have been required and a degradation of g_m takes place.
In addition, the parameter interpolation of p_3 saturates at higher doses which is most likely not the case (cf. figure 10.7 for comparison).

Similar observations can also be seen in the other scenarios. If a lesser irradiated region is chosen as a reference region the effect is reduced.
The results from scenario 2 are shown in figure 10.11. A lesser irradiated region as a reference leads to a reduced spread of $\Delta I_{DS,2} \approx 100\ \mu A$, which is less than in the harsh scenario 1. There a maximum difference of $\Delta I_{DS,1} \approx 139\ \mu A$ can be observed.

A more relaxed situation can be found in the scenario 3 (figure 10.12). The spread in the drain current is reduced to $\Delta I_{DS,3} \approx 94\ \mu A$. In this plot, the “soft” limit of the DCD, i.e. no common mode correction is applied (equations 10.5 and 10.7), is shown together with the estimation of the drain currents.

The possibly best situation can be found in the fourth scenario, shown in figure 10.13. A total spread of $\Delta I_{DS,4} \approx 65\ \mu A$ can be observed. Yet, the drain current of the highest

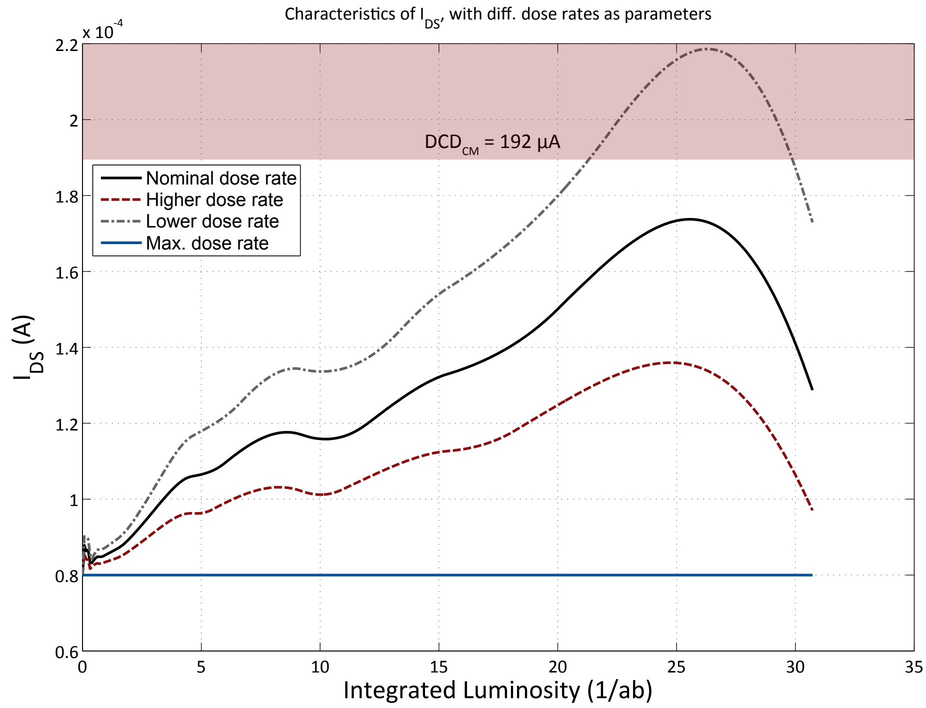


Figure 10.9.: Spread of various drain currents according to scenario 1. The hard limit by the common mode correction of the DCD is illustrated by the red patch. The reduction of I_{DS} at $\sim 26\ ab^{-1}$ is explained in the text.

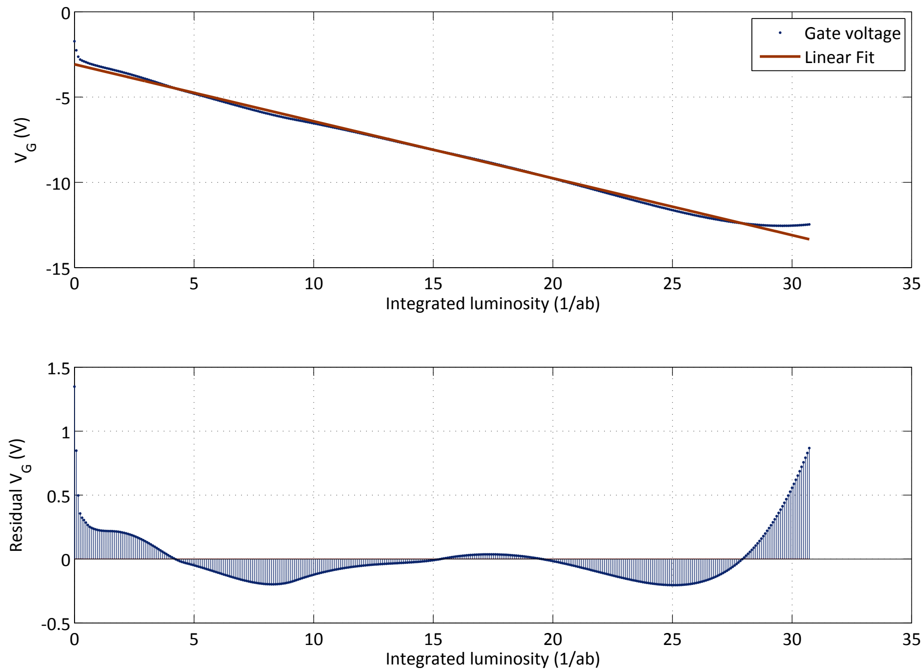


Figure 10.10.: Adaption of the gate voltage during the operation of Belle II (top) in the first scenario. The adaption is almost linear except at large integrated luminosities, visible in the residuals to the linear fit (bottom). This deviation can lead to a reduction in drain currents.

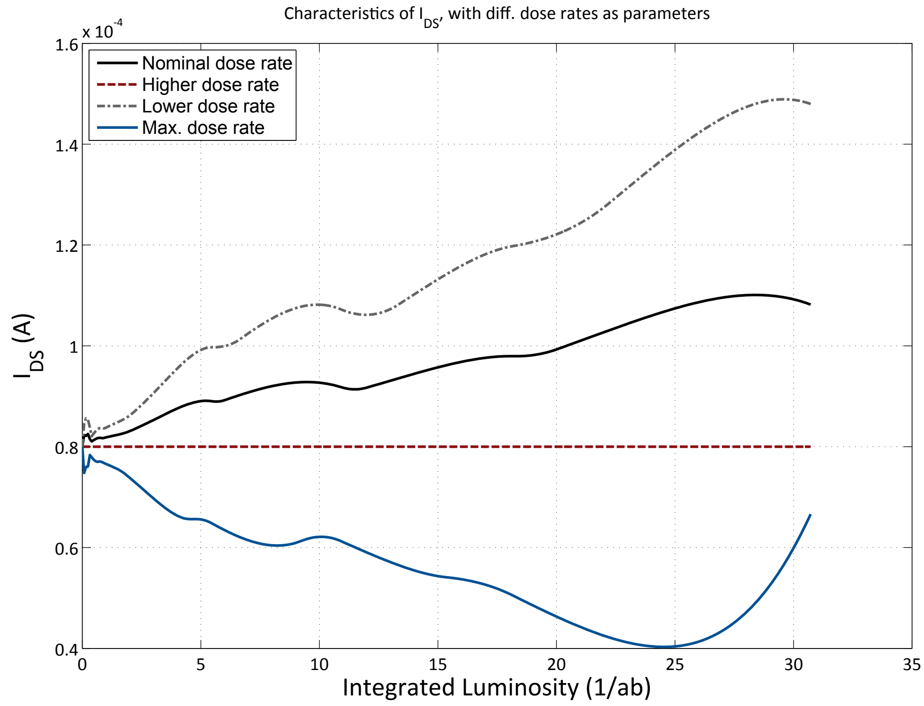


Figure 10.11.: Spread of various drain currents according to scenario 2.

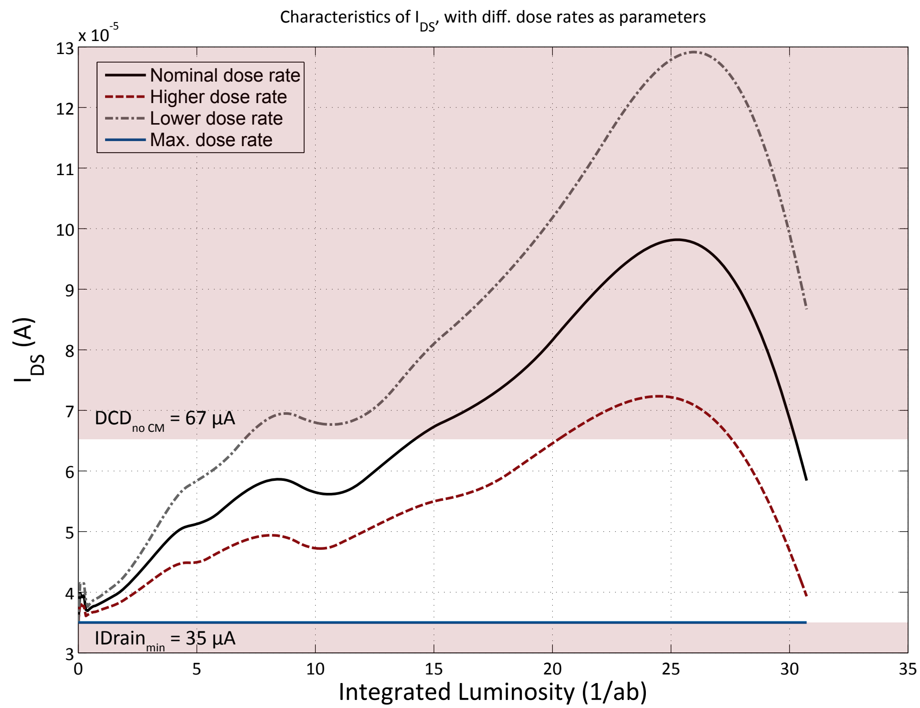


Figure 10.12.: Spread of various drain currents according to scenario 3. The smaller input range of the DCD (without common mode correction) is illustrated by the red patch.

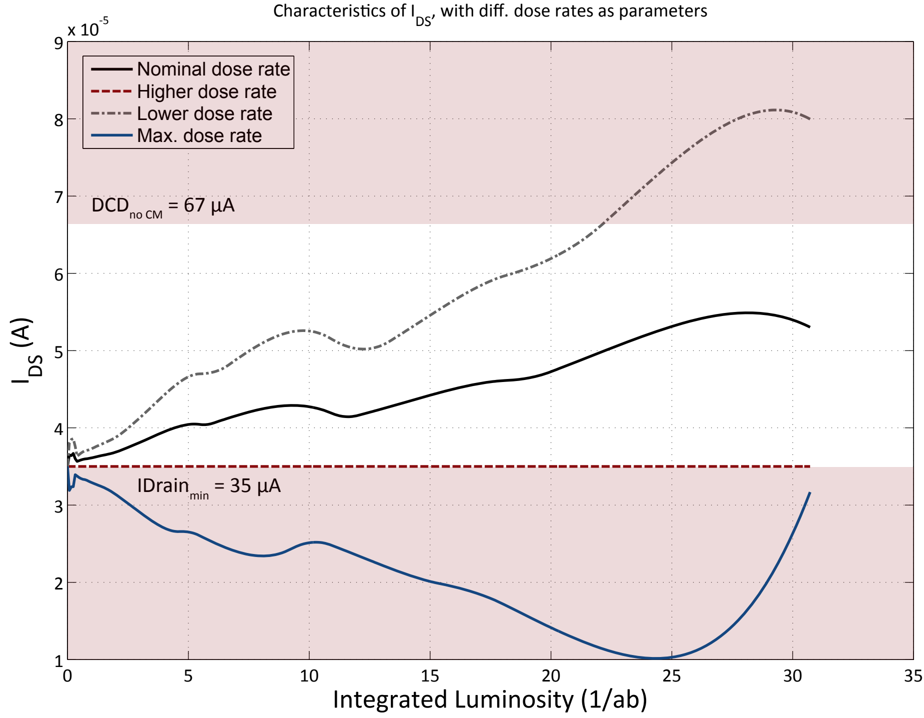


Figure 10.13.: Spread of various drain currents according to scenario 4. The smaller input range of the DCD (without common mode correction) is illustrated by the red patch.

irradiated region falls below the limit of equation 10.5. This makes this scenario less valuable when taking these regions into account.

In the fifth scenario the degradation of g_m is neglected. The reduction of the currents at higher integrated luminosities is thus omitted. A small reduction remains due to the interpolation method and a spread $\Delta I_{DS,5} \approx 91\ \mu A$ can be observed.

In table 10.2 the results from the scenarios are summarized.

Sceanrio	ΔI_{DS} (all) (μA)	ΔI_{DS} (w/o high irrad.) (μA)
Scen. 1, Max.	139	-
Scen. 2, Medium	100	70
Scen. 3, Max + low I_{DS}	94	-
Scen. 4, Medium+low I_{DS}	65	46
Scen. 5, const. g_m	91	55

Table 10.2.: Overview of drain current differences due to inhomogeneous irradiation scenarios. The last column states the spread if the highest irradiated region is omitted.

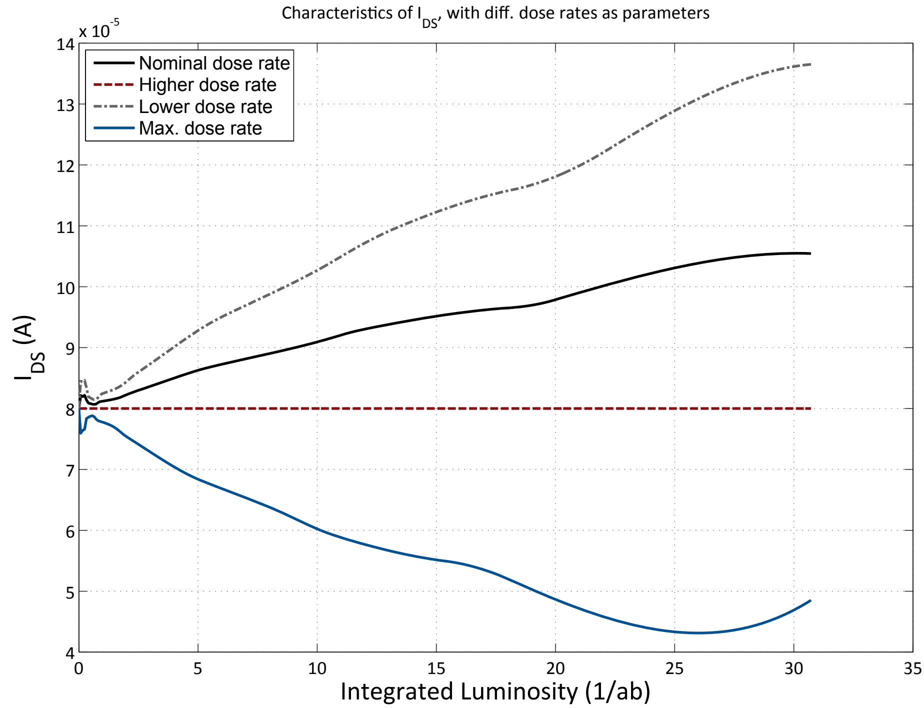


Figure 10.14.: Spread of various drain currents according to scenario 5.

Conclusions

From the summarized data in table 10.2 the scenario 4 is favored when considering a small spread. However, at this scenario the signal of the highest irradiated region cannot be sufficiently resolved, since the SNR is below 20. Thus either this region has to be "omitted" or the previous scenario 3 has to be taken into account.
Scenarios 1 and 2 exhibit a higher drain current as a reference. This will lead to better transconductance and thus g_q, however the spread in current is large and in the first scenario the maximum input range of the DCD is exceeded.
The fifth scenario shows promising results. Although the spread $\Delta I_{DS,5} \approx 91\ \mu A$ is considerable high, the continuously good transconductance g_m will result in a steady g_q during the lifetime of Belle II. The spread is still in the input range of the DCD, thus the highest irradiated region can be resolved by the ADC.

The various drain current scenarios depend on the interpolation method and the adaption of the gate voltage in the scenarios. Interpolation, especially at boundaries, is always a source of error and thus the results shown in this section have to be taken with a grain of salt at higher integrated luminosities. For the prediction at these values an irradiation to higher doses of suitable test devices would therefore be needed.
The DUT in question shows a considerable reduction in the transconductance due to the misalignment of the shallow p implantation. To what extent a reduction in g_m can be omitted in the final production is not quite clear. However, from measurements of devices of the TO project (cf. section 6.2.4) a smaller reduction of g_m is observed. At this production an already thin gate insulator was used. Therefore the scenario 5 appears to be a reasonable

prediction of the drain current spread in Belle II.

10.3. Summary

The estimation of the DEPFET signal performance showed that the noise in the PXD is dominated by the noise of the DCD. A reduction of the current noise level to its nominal value in the newer versions of the DCD allows the PXD to be operated at higher temperatures.
Conservative estimations of the SNR lead to a detector efficiency of better than 91%. Taking into account similar or even better conditions as in the production of PXD 6 for the final production of DEPFETs lead to an estimated efficiency of $> 98\%$.
Inhomogeneous irradiation along the z axis of the detector is investigated. The maximum spread in drain current by the input range of the DCD leads to an allowable difference in the gate voltage between higher and lesser irradiated regions. The common mode correction ability of the DCD is a considerable relief in this matter.
This feature is also necessary in the ability to handle the different drain currents. The best situation results in a scenario in which no (or only marginal) degradation of g_m with respect to dose is present. Although the spread in drain current is quite high in this scenario, it does not exceed the input range of the DCD and ensures a good signal performance of the PXD.

Chapter 11.

Summary and Outlook

This thesis deals with the radiation damage which is to be expected in the DEPFET in the Belle II experiment. Electrons and positrons of low energies are the main source of background. These particles cause damage in the silicon dioxide via ionization and also damage the crystal lattice of the silicon bulk.

In order to scale the damage done by these particles, the hardness factor of electrons of similar energies is investigated. It turns out that the actual hardness of electrons of an energy of 10 MeV is $\kappa_{Exp_{10\ MeV}} = (1.05 \pm 0.03) \cdot 10^{-2}$, which is considerably lower than the anticipated value from literature. With the hardness factor extracted, neutron damage studies of DEPFETs and of DEPFET related silicon material, performed by Petrovics [39], are then scaled to the main background in Belle II. The studies show that a type inversion of the silicon bulk can be excluded with the resistivity of the silicon material and the fluence to be expected at Belle II. In addition, no evidence is found of an increase in punch-through noise, however, an increase in the bulk generated shot-noise is observed.

Besides the noise from the bulk also surface generated noise contributes to the total noise of the DEPFET. This surface part has its origin in the creation of additional interface traps through ionizing radiation. The MOS interface on a depleted volume of silicon is generation active. This is the case for the clear gate of the DEPFET and the generated charge thus contributes to the noise. In a conservative estimation a noise contribution of $N_{surf} \approx 50\ e^-$should be taken into account after a delivered luminosity of 40 ab^{-1}.
Details about the source of interface traps are extracted from measurements of four monitor devices, i.e MOS capacitors. The interface trap distribution is obtained for the upper part of the forbidden bandgap. A low increase could be found in the two devices with a silicon nitride thickness of 10 nm and 20 nm, while thicker nitride layers (40 nm and 60 nm) resulted in a higher interface trap density.
The irradiation and analysis of the MOS capacitor identified the P_b defect as one source of the interface trap density increase. An additional defect could be observed, yet a distinct classification is missing up to now.
Interface traps lead also to a reduction in the mobility of holes in the channel of the DEPFET and thus to a reduction of the transconductance of the device. This is studied and as a result a decrease of $\sim 15\%$ should be taken into account during the lifetime of Belle II.

Furthermore, ionizing radiation leads to a shift in the threshold voltage of the DEPFET. This shift has to compensated by an adaption of the voltage supply for the modules in the PXD during the operation of Belle II. However, the shift itself should be as low as possible to avoid complications with the Switcher control chip and break-downs between the two

polysilicon layers of the DEPFET. The situation gets more complicated for the clear gate since a compensation via external power supplies cannot compensate the intra-pixel voltage shift of this contact. Therefore production parameters are investigated to keep the threshold voltage shift within its allowed range.
With the various devices studied in this thesis a recommendation can be made for the production of gate and clear gate:

1. A wet oxidation procedure reduces temperature during the production of DEPFETs. Thus a low trap precursor density for the E' center defect is likely to be achieved. A smaller shift of the threshold voltage in gate equivalent devices which exhibited a wet oxidation can be observed, supporting this assumption.

2. A silicon nitride thickness of 30 nm is advantageous for the gate oxide. Even though a slightly better behavior is found by a nitride layer of 10 nm on a dry oxidation process, yet the conformal deposition of silicon nitride during the production enables the creation of a smooth surface which favors moderately thick nitride layers. Thus the 30 nm thickness is recommended.

3. For the clear gate the intra-pixel variations should be small. This can be achieved with a thickness of 20 nm, which is also favorable in the smoothing of rough surfaces.

In case of radiation hardness a thickness of 20 nm for the clear gate is advantageous. However, the deposition of silicon nitride of 30 nm thickness for the gate is the same as for the clear gate. For technological reasons the nitride layer of the clear gate is not thinned down to the recommended value. The recommended parameters for the silicon nitride thickness of the gate and the type of oxidation are now incorporated for the production of the DEPFETs for Belle II.

The overall shift in threshold voltage will be smaller in the Belle II experiment than in the results presented in chapter 7. This is due to the fact that the dose rate in the Belle II experiment will be considerably lower than in the irradiation experiments performed in this thesis. The investigations on the annealing of surface damage show that roughly $75\% - 80\%$ of the threshold voltage shift should be taken into account.

A model is proposed for the ionizing radiation damage in MNOS devices. Most models rely on the finite trap precursor density of the E' centers for the saturation of the threshold voltage shifts. However, this thesis shows that irradiation experiments on similar devices resulted, due to a different gate biasing, in different levels of the threshold voltage - yet nearly all of them showed a saturation behavior. Therefore a model is proposed which relies on the electric field in the insulators of the devices. The model is based on the model by Raparla et al. [126], yet it was modified and extended.
The proposed model describes the behavior of the threshold voltage shift due to ionizing radiation by a charge yield in the insulators and depends in contrast to [126] on the nitride thickness and on a finite generation parameter to take e.g. diffusion into account.
The model shows good results in describing single or similar device types/operation conditions, however different datasets could not be fitted by one common set of parameters. Since the transport equations of the charge carriers are missing in the model, their influence is hidden in the model parameters. In order to take these effects into account a dependence

on the electric field in the insulators of the parameters is introduced.
This step enables the model to predict results for various electric fields. Although the predictions should be taken with a grain of salt, a reasonable assessment of the device behavior to ionizing radiation is possible.

Estimations of the DEPFET behavior in the Belle II experiment are presented at the end of this work. They reveal a good signal and noise performance of the device, thus allowing higher temperatures of the DEPFET in the experiment.
Inhomogeneous irradiation of the DEPFET within one module still poses a threat to the PXD. However, as the investigation of several scenarios showed, this issue is handled well. The common mode correction of the DCD allows large spreads in the input currents and is mandatory to manage inhomogeneous dose profiles. The segmentation of the modules into three parts reduces the threat of inhomogeneous irradiation additionally. With an anticipated marginal reduction in the transconductance g_m a safe operation in Belle II is envisaged.

An improvement of the model for the radiation hardness of MNOS devices is possible. A good prediction of the radiation hardness of MNOS devices would be a useful tool in the development process. However, a model which includes different parameters like the type of oxidation, electric field, and insulator thickness would require a vast amount of test devices. The fabrication of suitable devices for this parameter scan would result in a production time of $> 1\ a$ and several irradiation experiments would have to be conducted to scan this parameter space and test the new hypotheses.

The annealing experiments with higher temperatures showed that a large fraction of the threshold voltage shift could be recovered. Thus an application of the DEPFET in a system with relatively easy access to the detector system allows a prolonged use of the device. It would have to be heated up for only $\mathcal{O}(h)$ with reasonably low temperatures in order to recover the initial system properties. Of course, such a system would not be trivial. E.g. it would have to deal with different thermal expansion coefficients of the detector system materials, and the reduction of Electrostatic Discharge (ESD) threats.

The reduction in the threshold voltage shift by utilizing thinner oxides showed the potential of this detector. A further reduction of the oxide layer thickness results in intrinsically radiation hard DEPFETs. The gate length L would have to be reduced in order to achieve a reasonable internal amplification g_q. The further miniaturization of the device leads also to a reduction in the operation voltages so that e.g. low power dissipating applications may become possible.

Appendix A.

Irradiation Facilities

A.1. X-Ray Irradiation at the Karlsruhe Irradiation Center

The X-ray tube used in this study is located at the Institute of Experimental Nuclear Physics (IEKP) of the Karlsruhe Institute of Technology (KIT). The tube parameters used in most cases in this study are listed in table A.1. For some irradiations, the tube current was higher and also the distance, but overall the dose power stated in table A.1 is a fair assessment. The precision of the tube with respect to dose may still be subjected to error. However, a calibration with RadFET devices states an accuracy of 10 %. Further reading on this issue is provided in [136].

Parameter	Setting
Acceleration voltage (kV)	60
Tube current (mA)	30
Distance Tube-Target (mm)	115
Applied Filter	Iron
Dose power (kGy/h)	5.78

Table A.1.: Typical X-ray tube parameters

A typical setup is shown in figure A.1.

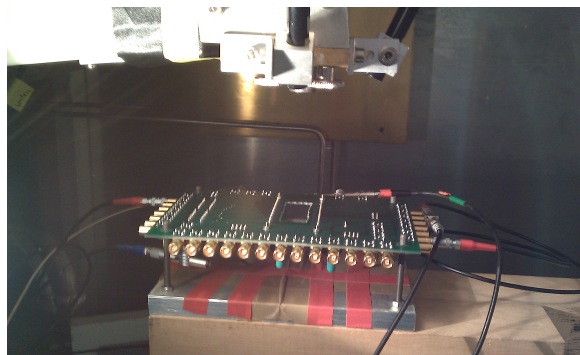


Figure A.1.: Typical setup of the irradiation procedure. The DUT, which is glued onto a ceramic carrier is socketed into the PCB. Lemo 00 cables supply voltages to the DUT while from the tube (top side) X-rays are emitted.

A.2. Electron Irradiation - Synergy Health

Electron irradiations were carried out at the Synergy Health facility in Radeberg [84]. This facility uses electrons with an energy of 10 MeV and is designed for the sterilization of medical devices. Therefore the proportions of the facility are outlined to accommodate large quantities of goods.
The irradiation procedure of the DUT is illustrated in figure A.2. The applied dose is controlled by adjusting the accelerator and the speed of the band conveyor. The highest accumulated dose in this thesis was achieved via four turns on the conveyor. In order to measure the dose an alanine dosimeter can be placed on the carriage.

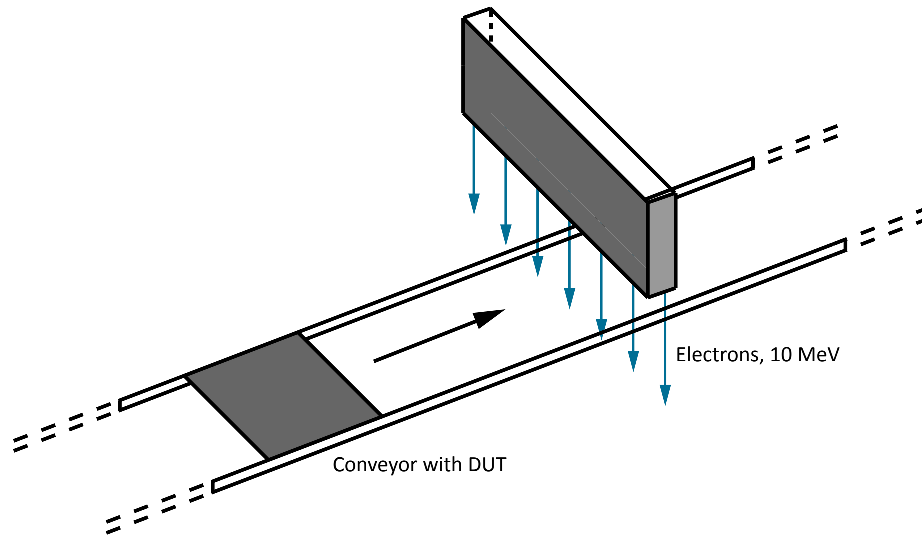


Figure A.2.: Illustration of the irradiation procedure with electrons at the facility of Synergy Health.

Appendix B.

Measurement of MOSFETs

B.1. DUT Overview MOSFETs

ChipID	Nitride thickness (nm)	Dose (krad)	Dose (kGy)	Type	Voltage (V)	Biasing	V_{DS} (V)
N04	10	5000	50	ClearGate	0	fix	-5
L04	10	5000	50	ClearGate	-2.5	fix	-5
J04	10	5000	50	ClearGate	-5	fix	-5
N05	10	5000	50	ClearGate	2.5	fix	-5
N07	10	3000	30	ClearGate	5	fix	-5
I04	20	5000	50	ClearGate	-5	fix	-5
E04	20	5000	50	ClearGate	0	fix	-5
E05	20	5000	50	ClearGate	2.5	fix	-5
E07	20	5000	50	ClearGate	5	fix	-5
A07	20	10000	100	ClearGate	-2.5	fix/adaptive	-5
I03	20	10000	100	ClearGate	2.5	fix/adaptive	-5
J15	20	10000	100	ClearGate	-5	fix/adaptive	-5
N14	20	10000	100	ClearGate	0	fix/adaptive	-5
Q07	10	3000	30	Gate	2	fix	off
B07	20	3000	30	Gate	2	fix	off
B12	60	3000	30	Gate	2	fix	off
Q12	40	11500	115	Gate	2	fix	off
G03	20	10000	100	Gate	2	fix/gate adaptive	-5
G16	60	10000	100	Gate	2	fix/gate adaptive	-5
L03	10	10000	100	Gate	2	fix/gate adaptive	-5
L16	40	10000	100	Gate	2	fix/gate adaptive	-5
06U	30	10000	100	Gate	5	fix/gate adaptive	-5
12U	30	10000	100	Gate	2	fix	-5
S1U	30	10000	100	Gate	2	fix	-5

Table B.1.: Overview of irradiated MOSFETs. Nitride thickness is the nominal thickness, all doses were applied via the X-ray facility in Karlsruhe. Type designates the DEPFET equivalent structure, voltage is the applied potential during irradiation, as well as V_{DS}. Fix/adaptive means that one side of the Chip (usually 7 MOSFETs) were fixed biased at the gate and the other half was adaptively biased.

B.2. Threshold Voltage

B.2.1. Threshold Voltage from Input Characteristics in Saturation Mode

From the input characteristic curve $I_{DS}(V_G)$ in saturation mode ($V_S = 0\ V$, $V_D = -5\ V$) an appropriate range is chosen. Typically this is given by $100nA \leq |I_{DS}| < 200\mu A$. The square root from the I_{DS} data is taken and a linear fit

$$\sqrt{I_{DS}} = a \cdot V_G + b \tag{B.1}$$

is applied. The fit results are checked on integrity to ensure a "good" fit. If the fit turns out to be bad, the algorithm cancels step by step low current values to be outside of the subthreshold-threshold region.
The resulting threshold voltage is calculated via

$$V_{th_{sat}} = -\frac{b}{a}. \tag{B.2}$$

Error on V_{th} in Saturation Mode

The statistical error on this value is given by

$$\sigma_{V_{th_{sat}}} = \sqrt{(\frac{b}{a^2})^2 \cdot \sigma_a^2 + (\frac{1}{a})^2 \cdot \sigma_b^2 + 2 \cdot (-\frac{1}{a})(\frac{b}{a^2}) \cdot cov(a,b)}. \tag{B.3}$$

B.2.2. Threshold Voltage from Input Characteristics in Linear Mode

Following the extrapolation in the ELR method from [36], the threshold voltage in this region is established via searching the maximum of the transconductance curve $\frac{\partial I_{DS}}{\partial V_G}(V_G)$ (point denoted by g_{max}) and fitting at this point with the maximum slope a straight line

$$I_{fit} = g_{max} \cdot V_G + I_{const} \tag{B.4}$$

to the voltage axis (see e. g. figure B.1). The intersection V'_{th} is equal to $V_{th} + 1/2V_D$, thus the resulting threshold voltage is given by

$$V_{th} = V'_{th} - 1/2 \cdot V_D. \tag{B.5}$$

Error on V_{th} in Linear Mode

The error on V_{th} is influenced by different sources. First there is the accuracy of the measurement device (whose specifications are listed in [137]) and second the accuracy of the extraction algorithm. This depends not only in finding the maximum point of the derivative but also in the accuracy of it.
The maximum point can be easily mistaken with a simple use of the maximum value. Unfortunately a change in the measurement range occurred in most devices close to the true maximum in the derivative. This results due to the deviation process, amplifying those small changes in the I_{DS} data.
Once this problem is solved, the accuracy depends mostly on the step size of the gate voltage

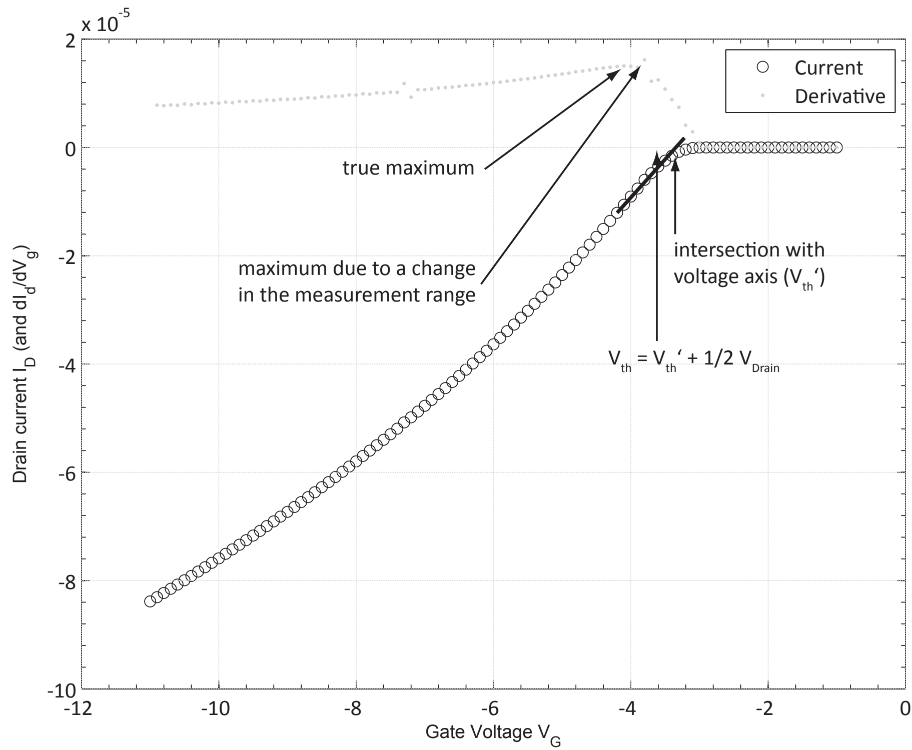


Figure B.1.: Input characteristics of a MOSFET. Besides the current values, also the derivative is shown. Due to a change in the measurement range of the ammeter, peaks in the deviation can arise which would fake the true maximum. The usually negative drain voltage adaption to the true threshold voltage is marked.

V_{step}. As one can see by the resolution (digit) and accuracy of the Keithley 4200 [137] it is fair to neglect the errors of this device.
The threshold voltage in the linear case is given by

$$V_{th} = V'_{th} - 1/2 \cdot V_D. \tag{B.6}$$

Whereas V_D depends only on the measuring device, V'_{th} depends additionally on the algorithm. V'_{th} is computed in the following way

$$V'_{th} = -\frac{I_{const}}{g_{max}}. \tag{B.7}$$

Both components in this equation are defective. The error on g_{max} originates from the step size in the gate voltage V_{step} and is estimated by using the average of the left and right data point of g_{max} in the derivative via

$$\sigma g_{max} = g_{max} - 1/2(g_{max}(left) + g_{max}(right)). \tag{B.8}$$

The error on I_{const} depends on the linear fit I_{fit} (equation B.4) and is given by

$$\sigma I_{const} = \sqrt{\sigma I^2 + V_G(g_{max})^2 \cdot \sigma g_{max}^2} \tag{B.9}$$

with

$$\sigma I = I_{fit}(V_{g_{max}}) - 1/2 \cdot (I_{fit}(Index(V_{g_{max}}) + 1) + I_{fit}(Index(V_{g_{max}}) - 1)) \tag{B.10}$$

with index designating the appropriate data point.

B.3. Subthreshold Swing

B.3.1. Extracting the Subthreshold Swing from Saturation Measurements

The swing is defined as that amount of voltage needed to increase the current I_{DS} by one decade. In an appropriate subthreshold region a transformation from “normal” current values to logarithmic values is performed, allowing a liner fit to the $\ln(I_{DS})(V_G)$ data. The slope of this linear fit a is used to calculate the swing S via

$$\begin{aligned} S &= \frac{V_{max} - V_{min}}{\#dec.} \\ &= \frac{1}{a \cdot \#dec.} \cdot \ln(\frac{I_{max}}{I_{min}}). \end{aligned} \tag{B.11}$$

Error on Subthreshold Swing

The uncertainty on the abovementioned extraction of the subthreshold swing is given by

$$\sigma S = \sqrt{\frac{1}{a^2 \cdot \#dec.} \cdot \ln(\frac{I_{max}}{I_{min}})^2 (\sigma a)^2}. \tag{B.12}$$

B.4. Transconductance

B.4.1. Extraction of Transconductance from Input Characteristics

The transconductance is extracted in the following way:

1. A quadratic fit $y_{qfit} = aV_{GS}^2 + bV_{GS} + c$ is applied to the $I_{DS}(V_{GS})$ curve. The fit range R is hereby restricted to $R = \{I_{DS}| \, |I_{DS}| > 1\mu A\}$ to ensure the quadratic behavior. In addition, the fit routine cancels noise at the beginning of the curve.

2. At a drain current of $|I_{DS}| = 100\mu A$ the corresponding voltage V_{g_m} is extracted.

3. The routine extracts then the final $g_{m_{fixCurrent}}$ value by inserting V_{g_m} into the analytical deviation $g_m = \frac{\partial y_{qfit}}{\partial V_{GS}}$ of the quadratic fit.

B.4.2. Errors on Transconductance

The formula for $g_{m_{fixCurrent}}$ is given by:

$$g_{m_{fixCurrent}} = 2aV_{g_m} + b, \tag{B.13}$$

propagating the error leads to:

$$\sigma g_{m_{fixCurrent}} = \sqrt{(2V_{g_m})^2 \cdot cov(a,a) + cov(b,b) + (2a)^2 \cdot (\sigma_{V_{g_m}})^2}. \tag{B.14}$$

The error for V_{g_m} has been neglected.

For some DUTs (e.g. J04) the mean of two similar transistor was calculated, therefore the error is then given by:

$$\sigma g_{m_{fixCurrentMean}} = \frac{1}{2}\sqrt{(\sigma g_{m_{fixCurrent1}})^2 + (\sigma g_{m_{fixCurrent2}})^2}. \tag{B.15}$$

Appendix C.

CV Measurements of MOSCAPs

C.1. DUT Description

In this work different MOSCAPs were studied and irradiated. Tables C.1, C.2, C.3, and C.4 summarize their properties.

DUT	Production	Wafer ID	Chip ID	Area	Oxide thickness	Nitride thickness
				(mm^2)	(nm)	(nm)
B07	TO	5	B07	10	85	20
B12	TO	5	B12	10	85	60
Q07	TO	5	Q07	10	85	10
Q12	TO	5	Q12	10	85	40
DUT 2-1	DIO 318B	W02		10	86	10

Table C.1.: Overview of MOSCAPs.

Device	Oxide thickness (nm)	Nitride thickness (nm)
B07	83	20
B12	83	55
Q07	83	11
Q12	83	41

Table C.2.: Insulator thickness of MOSCAP devices, measured with ellipsometry in the HLL.

C.2. Measurement Corrections

Corrections of the LCR Meter

In order to minimize the error of the LCR Meter (see e.g. [138]), several corrections were applied:

1. Short correction
   The two measurement cables are short-circuited to reduce parasitic residual impedances of the DUT. This is done very close to the DUT, in order to minimize the error of the connection cables.

ChipID	Nominal t_{Ni} (nm)	Double nitride	Calculated C (nF)	Measured C (nF)	Dev. in %
B07	20	yes	3.62	3.905	8%
B12	60	yes	2.97	3.207	8%
Q07	10	no	3.83	4.291	12%
Q12	40	yes	3.26	3.322	2%

Table C.3.: Overview of capacitors in this work. The devices deviate from the calculated maximum capacitance, which already was corrected for deviations from the intended nitride and oxide thickness. For extractions of D_{it} the measured maximum capacitance was used.

Dose (kGy)	Q07 LF (Hz)	B07 LF (Hz)	Q12 LF (Hz)	B12 LF (Hz)	Q07 HF (kHz)	B07 HF (kHz)	Q12 HF (kHz)	B12 HF(kHz)
0	20	20	20	20	10	10	10	500
10	20	20	20	20	100	100	100	100
15	20	20	20	20	100	100	100	100
30	20	20	20	20	100	100	100	100
90	-	-	20	-	-	-	100	-
110	-	-	20	-	-	-	100	-
115	-	-	20	-	-	-	100	-

Table C.4.: Measurement frequencies of TO devices.

2. Open correction
   Measurement cables are opened close to the DUT. This eliminates errors due to parasitic stray impedances.

3. Measurement mode
   Measurements have been taken in the $|Z| - \Theta$ - mode. This ensures original data without device model corrections of the LCR meter. The LCR meter does have the capability of corrections for parallel and series resistances (C_P or C_s -modes, figure C.1). However, the applied (internal) correction of the measurement device is unclear. For this reason, the original impedance Z was measured and a correction with assumed parasitic R_s and R_p was studied. However, if for the parallel resistance $R_p > 100\ k\Omega$, then the $C - V$ curves do not deviate much from each other and even for the 100 $k\Omega$ case the difference is only in inversion visible.
   For this reason, a simplified correction of taking only a series resistance R_s into account is sufficient.

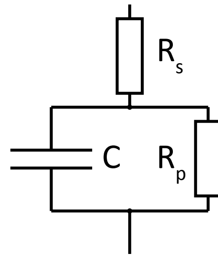


Figure C.1.: Measurement model for the LCR meter, including all parasitic resistances.

Appendix D.

Measurements of GCDs

D.1. Overview of GCDs

DUT	Pitch	Contact	Dopings	Area ($10^{-2}cm^2$)	Gate (V)	Biasing	t_{ni} (nm)
N04	Fine	Poly	nd1n	4.055	0	fix	10
N05	Coarse	Poly	nd1n	8.055	0	fix	10
N07	Fine	Poly	nd1n	4.055	0	adaptive	10
L04	Coarse	Poly	-	8.055	0	adaptive	10
J04	Coarse	Poly	-	8.055	0	fix	10
I04	Coarse	Poly	-	8.055	2	fix	20
E04	Fine	Poly	nd1n	4.055	0	fix	20
E05	Coarse	Poly	nd1n	8.055	0	fix	20
E07	Fine	Poly	nd1n	4.055	0	adaptive	20
J15	Coarse	Poly	-	8.055	0	fix	20
N14	Coarse	Poly	nd1n	8.055	0	fix	20
A07	Fine	Poly	nd1n, pshn	4.055	-8	fix	20
I03	Coarse	Poly	nd1n, pshn	8.055	-8	adaptive	20
L16	Fine	Poly	nd1n, pshn	4.055	0	fix	40
L03	Fine	Poly	nd1n, pshn	4.055	0	adaptive	10
G16	Fine	Poly	nd1n, pshn	4.055	0	fix	60

Table D.1.: Overview of GCDs.

Appendix E.

Model Parameters

ID	Fit/Pred. Param.	$Khni$	σ_{Khni}	$Khox$	σ_{Khox}	$Keox$	σ_{Keox}	G_{const}	$\sigma_{G_{const}}$
E05	Pred.	1.56E-03	2.05E-04	8.21E-05	1.82E-06	8.77E-04	1.24E-04	5.91E-02	5.49E-04
E07	Pred.	2.48E-04	2.41E-05	3.36E-04	1.03E-05	3.72E-04	4.12E-05	1.15E-01	1.29E-03
I03	Pred.	1.56E-03	2.05E-04	8.21E-05	1.82E-06	8.77E-04	1.24E-04	5.91E-02	5.49E-04
G03	Pred.	2.39E-03	3.79E-04	5.22E-05	1.52E-06	9.01E-04	1.28E-04	5.43E-02	4.63E-04
E04	Pred.	9.60E-04	1.58E-04	1.53E-06	5.56E-06	5.20E-04	6.17E-05	4.69E-02	3.77E-04
I04	Pred.	1.36E-04	1.30E-05	1.58E-04	2.78E-05	1.54E-04	1.47E-05	5.85E-02	7.64E-04
A07	Pred.	1.91E-04	1.93E-05	9.39E-05	2.07E-05	1.99E-04	1.96E-05	5.41E-02	6.56E-04
N05	Pred.	3.45E-03	3.65E-04	8.29E-05	1.83E-06	8.76E-04	1.24E-04	5.93E-02	5.51E-04
N07	Pred.	1.60E-03	1.57E-04	3.45E-04	1.07E-05	3.61E-04	3.98E-05	1.18E-01	1.32E-03
L03	Pred.	3.90E-03	4.35E-04	5.22E-05	1.52E-06	9.01E-04	1.28E-04	5.43E-02	4.63E-04
N04	Pred.	4.33E-03	6.97E-04	1.67E-06	5.74E-06	5.10E-04	6.02E-05	4.69E-02	3.80E-04
L04	Pred.	2.23E-03	3.38E-04	1.02E-04	2.16E-05	1.92E-04	1.88E-05	5.47E-02	6.70E-04
J04	Pred.	1.49E-03	1.97E-04	2.25E-04	3.45E-05	1.27E-04	1.19E-05	6.26E-02	8.56E-04
E05	Fit	1.69E-03	2.80E-04	1.15E-04	1.61E-05	8.95E-04	1.12E-04	4.51E-02	1.50E-03
E07	Fit	2.95E-04	6.57E-05	1.43E-04	1.14E-04	4.98E-04	8.53E-05	9.16E-02	1.20E-02
I03	Fit	1.20E-03	2.15E-04	5.45E-05	8.32E-06	6.52E-04	9.17E-05	5.44E-02	2.10E-03
G03	Fit	3.35E-03	5.55E-04	4.34E-05	3.53E-06	1.20E-03	1.80E-04	5.22E-02	1.50E-03
E04	Fit	8.15E-04	1.73E-04	1.45E-04	5.84E-05	6.60E-04	8.89E-05	4.32E-02	2.70E-03
I04	Fit	1.10E-03	–	7.23E-04	–	2.52E-05	–	6.24E-02	–
A07	Fit	3.71E-04	9.30E-05	1.26E-04	2.80E-05	4.03E-04	6.24E-05	6.68E-02	2.00E-03
N05	Fit	2.85E-03	4.50E-04	1.20E-04	1.48E-05	6.98E-04	8.13E-05	4.86E-02	1.18E-03
N07	Fit	1.65E-03	1.82E-04	2.13E-04	1.90E-05	3.71E-04	2.21E-05	1.28E-01	2.46E-03
L03	Fit	5.61E-03	9.18E-04	3.85E-05	5.50E-06	1.11E-03	1.63E-04	4.27E-02	1.93E-03
N04	Fit	4.37E-03	6.67E-04	1.67E-06	5.35E-08	5.40E-04	8.18E-05	5.00E-01	4.24E-01
L04	Fit	2.09E-03	6.29E-04	2.57E-04	4.34E-05	6.88E-04	1.50E-04	5.02E-02	7.98E-04
J04	Fit	1.38E-03	4.57E-04	3.43E-04	7.36E-05	5.32E-04	1.12E-04	5.80E-02	9.21E-04

Table E.1.: Overview of model parameters from the initial fitting and the used parameters for predictions. K parameters and their uncertainties are given in $F(nm^2kGy)^{-1}$ and G_{const} and its uncertainty is given in V/nm.

Appendix F.

Acronyms

AC	Alternating Current	32
ADC	Analog-to-Digital Converter	18
APD	Avalanche Photo Diode	15
ARICH	Aerogel Ring Image Cherenkov Detector	15
ASIC	Application-Specific Integrated Circuit	16
ATLAS	A Toroidal LHC Apparatus	78
BDK	Berends, Daverveldt, Kleiss	21
BNC	Bayonet Neill Concelman	115
CAD	Computer-Aided Design	16
CDC	Central Drift Chamber	14
CDF	Collider Detector at Fermilab	78
CDS	Correlated Double Sampling	43
CLG	Clear Gate	94
CMOS	Complementary Metal-Oxide-Semiconductor	64
CV	Capacitance-Voltage	58
DC	Direct Current	32
DB	Dangling Bond	51
DCD	Drain Current Digitizer	17
DEPFET	Depleted p-channel Field Effect Transistor	2
DHP	Data Handling Processor	17
DIBL	Drain-Induced Barrier Lowering	37
DUT	Device Under Test	44
ECL	Electromagnetic Calorimeter	15
ehp	electron-hole pair	25
ELR	Extrapolation in the Linear Region	116
EM	Electromagnetic	6
ENC	Equivalent Noise Charge	77
EPR	Electron Paramagnetic Resonance	56

ESD Electrostatic Discharge ... 189
ESR Electron Spin Resonance ... 60
FFT Fast Fourier Transformation ... 78
FZ Float-Zone ... 82
GCD Gate Controlled Diode ... 25
HAPD Hybrid Avalanche Photo Detector ... 15
HER High Energy Ring ... 11
HLL Halbleiterlabor der Max-Planck-Gesellschaft ... 44
IR Interaction Region ... 23
IV Current-Voltage ... 70
KLM Kaon and Muon Detector (more precisely: K_L^0, μ-Detector) ... 15
LER Low Energy Ring ... 11
LHC Large Hadron Collider ... 56
LPCVD Low-Pressure Chemical Vapor Deposition ... 51
MC Monte Carlo ... 20
MCP Micro Channel Plate ... 15
MiMa Mini-Matrix System ... 78
MIP Minimum Ionizing Particle ... 76
MIS Metal-Insulator-Semiconductor ... 26
MNOS Metal-Nitride-Oxide-Semiconductor ... 113
MOS Metal-Oxide-Semiconductor ... 2
MOSCAP Metal-Oxide-Semiconductor Capacitor ... 25
MOSFET Metal-Oxide-Semiconductor Field Effect Transistor ... 25
NIEL Non Ionizing Energy Loss ... 54
PCB Printed Circuit Board ... 115
PID Particle Identification ... 14
PKA Primary Knock on Atom ... 53
PMT Photomultiplier Tube ... 15
PSD Power Spectral Density ... 78
PXD Pixel Detector ... 2
QED Quantum electrodynamic ... 20
RBB Radiative Bhabha ... 21
ROI Regions of Interest ... 14
RPC Resistive Plate Chambers ... 15
scr space charge region ... 41
SM Standard model of elementary particle physics ... 1

smy	Snowmass year	21
SNOS	Silicon-Nitride-Oxide-Semiconductor	64
SNR	Signal-to-Noise Ratio	76
SR	Synchrotron Radiation	23
SUSY	supersymmetry	13
SVD	Silicon Vertex Detector	14
TO	Thin-Oxide	44
TOP	Time-of-Propagation	15
VXD	Vertex Detector	14
ZIF	Zero Force Injection	115

Bibliography

[1] Andrei D. Sakharov. Violation of CP invariance, C asymmetry, and baryon asymmetry of the universe. *Soviet Physics Uspekhi*, 34(5):392–393, 1991. doi: 10.1070/PU1991v034n05ABEH002497.

[2] James M. Cline. Baryogenesis. 2006. `http://arxiv.org/abs/hep-ph/0609145`. arXiv:hep-ph/0609145.

[3] J. Brodzicka, T. Browder, P. Chang, et al. Physics achievements from the Belle experiment. *Progress of Theoretical and Experimental Physics*, 2012(1):4D001–0, 2012. doi: 10.1093/ptep/pts072.

[4] Christoph Berger. *Elementarteilchenphysik. Von den Grundlagen zu den modernen Experimenten*. Springer, Berlin, 2. reviewed edition, 2006. ISBN 3540231439.

[5] B. Povh. *Teilchen und Kerne. Eine Einführung in die physikalischen Konzepte*. Springer-Lehrbuch. Springer, Berlin, 8. edition, 2009. ISBN 9783540680758.

[6] Martin Ritter. Track-based Alignment for the Belle Vertex Detector Using the Millepede Approach. Diploma thesis, 2009. Ludwig-Maximilians-Universität München, München.

[7] Emmy Noether. Invariante Variationsprobleme. *Nachrichten von der Gesellschaft der Wissenschaften zu Göttingen, Mathematisch-Physikalische Klasse*, 1918:235–257, 1918. `http://eudml.org/doc/59024`.

[8] S. Weinberg. The making of the Standard Model. *The European Physical Journal C - Particles and Fields*, 34(1):5–13, 2004. doi: 10.1140/epjc/s2004-01761-1.

[9] J. H. Christenson, J. W. Cronin, V. L. Fitch, and R. Turlay. Evidence for the 2 Pion Decay of the K_2 Meson. *Physical Review Letters*, 13(4):138–140, 1964. doi: 10.1103/PhysRevLett.13.138.

[10] Wikipedia.org. Standard Model of Elementary Particles, 2013. Wikipedia. `https://en.wikipedia.org/wiki/Standard_Model`.

[11] Nicola Cabibbo. Unitary Symmetry and Leptonic Decays. *Physical Review Letters*, 10(12):531–533, 1963. doi: 10.1103/PhysRevLett.10.531.

[12] Makoto Kobayashi and Toshihide Maskawa. CP -Violation in the Renormalizable Theory of Weak Interaction. *Progress of Theoretical Physics*, 49(2):652–657, 1973. doi: 10.1143/PTP.49.652.

[13] J. Charles, A. Höcker, H. Lacker, et al. CP violation and the CKM matrix: assessing the impact of the asymmetric B factories. *The European Physical Journal C*, 41(1):1–131, 2005. doi: 10.1140/epjc/s2005-02169-1.

[14] H. Schröder. B anti-B mixing. *DESY*, (91-139):1–21, 1991. http://ccdb5fs.kek.jp/cgi-bin/img/allpdf?199201335.

[15] Z. Dolezal and S. Uno. Belle II Technical Design Report, 2010. KEK - High Energy Accelerator Research Organization. arXiv:1011.0352. http://arxiv.org/abs/1011.0352.

[16] S. Hashimoto and M. Hazumi. Letter of Intent for KEK Super B Factory, 2004. KEK - High Energy Accelerator Research Organization.

[17] I. Adachi. sBelle Design Study Report. 2008. http://arxiv.org/abs/0810.4084. arXiv:0810.4084.

[18] T. Aushev, W. Bartel, A. Bondar, J. Brodzicka, and T.E. Browder. Physics at Super B Factory. arXiv:1002.5012. 2010. http://arxiv.org/abs/1002.5012.

[19] The Physics of the SuperKEKB/Belle II Super Flavor Factory. Fundamental Physics at the Intensity Frontier, 2011. Rockville. http://www.ph.utexas.edu/~heavyquark/.

[20] K. Nishimura. The time-of-propagation counter for Belle II. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 639(1):177–180, 2011. doi: 10.1016/j.nima.2010.09.164.

[21] Thomas Weis. Einführung in die Beschleunigerphysik WS 2007/2008. Universität Dortmund, Dortmund. Lecture, 2008.

[22] Carlo J. Bocchetta. The Touschek Effect. Large Angle intra-Beam Scattering, 2003. CERN Accelerator School, Brunnen. http://cas.web.cern.ch/cas/BRUNNEN/Presentations/PDF/Bocchetta/Touschek.pdf.

[23] Hiroshi Nakano. Simulation studies of the Touschek effect. 7th International Workshop on DEPFET Detectors and Applications, 2011. Tohoku University, Ringberg Castle. https://indico.mpp.mpg.de/contributionDisplay.py?sessionId=8&contribId=53&confId=1249.

[24] Andreas Moll. *Optimization of a pixel vertex detector, to be published.* PhD thesis, Ludwig-Maximilians-Universität München, Munich, 2013.

[25] S. Jadach, W. Płaczek, M. Skrzypek, B.F.L Ward, and Z. Waşs. Monte Carlo program KoralW 1.42 for all four-fermion final states in e+e− collisions. *Computer Physics Communications*, 119(2-3):272–311, 1999. doi: 10.1016/S0010-4655(99)00219-2.

[26] F.A Berends, P.H Daverveldt, and R. Kleiss. Monte Carlo simulation of two-photon processes. *Computer Physics Communications*, 40(2-3):285–307, 1986. doi: 10.1016/0010-4655(86)90115-3.

[27] Christian Kiesling. Status of Charged Particle Backgroung in the PXD. (Reminder). Joint PXD-SVD Meeting, 2013. Wetzlar. https://indico.mpp.mpg.de/getFile.py/access?contribId=30&sessionId=3&resId=0&materialId=slides&confId=2114.

[28] Hiroyuki Nakayama. Beam Background in the Interaction Region. 7th International Workshop on DEPFET Detectors and Applications, 2011. Ringberg Castle. `https://indico.mpp.mpg.de/getFile.py/access?contribId=54&sessionId=8&resId=0&materialId=slides&confId=1249`.

[29] Andreas Moll. PXD Background. 13th Open Meeting of the Belle II Collaboration, 2012. Tsukuba. `http://kds.kek.jp/getFile.py/access?contribId=128&sessionId=29&resId=0&materialId=slides&confId=10927`.

[30] Yuri Soloviev. Synchrotron Radiation Background. Status. 13th Intenational Workshop on DEPFET Detectors and Applications, 2013. Deutsches Elektron Synchrotron (DESY), Ringberg Castle. `https://indico.mpp.mpg.de/getFile.py/access?contribId=37&sessionId=1&resId=0&materialId=slides&confId=2172`.

[31] J. Kemmer and G. Lutz. New detector concepts. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 253(3):365–377, 1987. doi: 10.1016/0168-9002(87)90518-3.

[32] J. Kemmer, G. Lutz, U. Prechtel, et al. Experimental confirmation of a new semiconductor detector principle. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 288(1):92–98, 1990. doi: 10.1016/0168-9002(90)90470-Q.

[33] E. H. Nicollian and J. R. Brews. *MOS (metal oxide semiconductor) physics and technology*. Wiley, New York, 1982. ISBN 9780471085003.

[34] S. M. Sze and Kwok Kwok Ng. *Physics of semiconductor devices*. Wiley-Interscience, Hoboken and N.J, 3. edition, 2007. ISBN 9780471143239.

[35] Gerhard Lutz. *Semiconductor radiation detectors. Device physics*. Springer, Berlin [u.a.], 2007. ISBN 9783540648598.

[36] A. Ortiz-Conde, F. J. Garcia Sánchez, J. J. Liou, et al. A review of recent MOSFET threshold voltage extraction methods. *Microelectronics Reliability*, 42(4-5):583–596, 2002.

[37] Xiangli Li, Huadian Pan, and B.M. Wilamowski. Gate-controlled punch through transistor. In *15th Biennial University/Government/Industry Microelectronics Symposium*, pages 226–229, 30 June-2 July 2003. doi: 10.1109/UGIM.2003.1225731.

[38] Emilio Gatti and Pavel Rehak. Semiconductor drift chamber — An application of a novel charge transport scheme. *Nuclear Instruments and Methods in Physics Research*, 225(3):608–614, 1984. doi: 10.1016/0167-5087(84)90113-3.

[39] Stefan Petrovics. Neutron Irradiations and Punch-Through Biasing Studies with DEPFETs for BELLE II. Master thesis, 2012. Ludwig-Maximilians-Universität München, München.

[40] A. S. Grove and D. J. Fitzgerald. Surface effects on p-n junctions: Characteristics of surface space-charge regions under non-equilibrium conditions. *Solid-State Electronics*, 9(8):783–806, 1966. doi: 10.1016/0038-1101(66)90118-3.

[41] Dieter K. Schroder. *Semiconductor material and device characterization.* IEEE Press and Wiley, [Piscataway and NJ] and Hoboken and N.J, 3. edition, 2006. ISBN 978-0-471-73906-7.

[42] Marc J. Madou. *Fundamentals of microfabrication. The science of miniaturization.* CRC Press, Boca Raton, 2. edition, 2002. ISBN 9780849308260.

[43] Frank L. Riley. Silicon Nitride and Related Materials. *Journal of the American Ceramic Society*, 83(2):245–265, 2000. doi: 10.1111/j.1151-2916.2000.tb01182.x.

[44] J.R. Srour, C.J. Marshall, and P.W. Marshall. Review of displacement damage effects in silicon devices. *IEEE Transactions on Nuclear Science*, 50(3):653–670, 2003. doi: 10.1109/TNS.2003.813197.

[45] Michael Moll. *Radiation Damage in Silicon Particle Detectors.* PhD thesis, Universität Hamburg, 1999.

[46] F. Bridges, G. Davies, J. Robertson, and A. M. Stoneham. The spectroscopy of crystal defects: a compendium of defect nomenclature. *Journal of Physics: Condensed Matter*, 2(13):2875–2928, 1990. doi: 10.1088/0953-8984/2/13/001.

[47] Gunnar Lindström. Radiation damage in silicon detectors. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 512(1-2):30–43, 2003. doi: 10.1016/S0168-9002(03)01874-6.

[48] G.P. Summers, E.A. Burke, P.. Shapiro, S.R. Messenger, and R.J. Walters. Damage correlations in semiconductors exposed to gamma, electron and proton radiations. *IEEE Transactions on Nuclear Science*, 40(6):1372–1379, 1993. doi: 10.1109/23.273529.

[49] A. Vasilescu and G. Lindström. Displacement damage in silicon, on-line compilation. All particles, 2012. Hamburg. `http://sesam.desy.de/members/gunnar/Si-dfuncs.html`.

[50] G. Lindström, M. Ahmed, S. Albergo, et al. Radiation hard silicon detectors—developments by the RD48 (ROSE) collaboration. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 466(2):308–326, 2001. doi: 10.1016/S0168-9002(01)00560-5.

[51] S. Dittongo, L. Bosisio, M. Ciacchi, et al. High-energy electron irradiation of different silicon materials. *IEEE Transactions on Nuclear Science*, 51(5):2794–2798, 2004. doi: 10.1109/TNS.2004.835117.

[52] Angela Vasilescu and Gunnar Lindström. Notes on the fluence normalisation based on the NIEL scaling hypothesis. *Technical Note, ROSE Collaboration*, 2000. `http://www.researchgate.net/publication/234719468_rtn2000-02_Notes_on_the_fluence_normalisation_based_on_the_NIEL_scaling_hypothesis/file/32bfe50ffbab81f576.pdf`.

[53] H. Feick, E. Fretwurst, G. Lindström, and M. Moll. Long term damage studies using silicon detectors fabricated from different starting materials and irradiated with

neutrons, protons, and pions. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 377(2-3): 217–223, 1996. doi: 10.1016/0168-9002(95)01404-7.

[54] L. Dobaczewski, S. Bernardini, P. Kruszewski, et al. Energy state distributions of the Pb centers at the (100), (110), and (111) Si-SiO2 interfaces investigated by Laplace deep level transient spectroscopy. *Applied Physics Letters*, 92(24):242104, 2008. doi: 10.1063/1.2939001.

[55] Nicolas Schoeni and Gervais Chapuis. CrystalOgraph. An interactive applet for drawing crystal structures, 2004. École Polytechnique Fédérale de Lausanne, Switzerland. `http://escher.epfl.ch/crystalOgraph/`.

[56] Gary J. Gerardi, Edward H. Poindexter, Philip J. Caplan, and Noble M. Johnson. Interface traps and Pb centers in oxidized (100) silicon wafers. *Applied Physics Letters*, 49(6):348, 1986. doi: 10.1063/1.97611.

[57] Yoshio Nishi. Electron Spin Resonance in SiO2 Grown on Silicon. *Japanese Journal of Applied Physics*, 5(4):333, 1966. doi: 10.1143/JJAP.5.333.

[58] Edward H. Poindexter. Interface states and electron spin resonance centers in thermally oxidized (111) and (100) silicon wafers. *Journal of Applied Physics*, 52(2):879, 1981. doi: 10.1063/1.328771.

[59] P. M. Lenahan and Conley J. F. What can electron paramagnetic resonance tell us about the Si/SiO2 system? *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 16(4):2134, 1998. doi: 10.1116/1.590301.

[60] J.R. Schwank, M.R. Shaneyfelt, D.M. Fleetwood, et al. Radiation Effects in MOS Oxides. *Nuclear Science, IEEE Transactions on*, 55(4):1833–1853, 2008. doi: 10.1109/TNS.2008.2001040.

[61] Iskander G. Batyrev, Daniel M. Fleetwood, Ronald. D. Schrimpf, and Sokrates T. Pantelides. The Role of Water in the Radiation Response of Wet and Dry Oxides. *IEEE Transactions on Nuclear Science*, 55(4):2085–2089, 2008. doi: 10.1109/TNS.2008.2000841.

[62] S. Rashkeev, D. Fleetwood, R. Schrimpf, and S. Pantelides. Defect Generation by Hydrogen at the Si- SiO2 Interface. *Physical Review Letters*, 87(16), 2001. doi: 10.1103/PhysRevLett.87.165506.

[63] S.N. Rashkeev, C.R. Cirba, D.M. Fleetwood, et al. Physical model for enhanced interface-trap formation at low dose rates. *IEEE Transactions on Nuclear Science*, 49 (6):2650–2655, 2002. doi: 10.1109/TNS.2002.805387.

[64] J. R. Schwank, D. M. Fleetwood, P. S. Winokur, et al. The Role of Hydrogen in Radiation-Induced Defect Formation in Polysilicon Gate MOS Devices. *IEEE Transactions on Nuclear Science*, 34(6):1152–1158, 1987. doi: 10.1109/TNS.1987.4337445.

[65] D.M Fleetwood, M.J Johnson, T.L Meisenheimer, et al. 1/f noise, hydrogen transport, and latent interface-trap buildup in irradiated MOS devices. *IEEE Transactions on Nuclear Science*, 44(6):1810–1817, 1997. doi: 10.1109/23.658947.

[66] Timothy R. Oldham. *Ionizing radiation effects in MOS oxides.* International series on advances in solid state electronics and technology. World Scientific, Singapore and River Edge and NJ, 1999. ISBN 9810233264.

[67] I. Capan, V. Janicki, R. Jacimovic, and B. Pivac. C–V and DLTS studies of radiation induced Si–SiO2 interface defects. *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, 2011. doi: 10.1016/j.nimb.2011.08.065.

[68] N. H. Thoan, K. Keunen, V. V. Afanas'ev, and A. Stesmans. Interface state energy distribution and Pb defects at Si(110)/SiO2 interfaces: Comparison to (111) and (100) silicon orientations. *Journal of Applied Physics*, 109(1):013710, 2011. doi: 10.1063/1.3527909.

[69] R. C. Hughes. Hole mobility and transport in thin SiO2 films. *Applied Physics Letters*, 26(8):436, 1975. doi: 10.1063/1.88200.

[70] Siegfried Hunklinger. Festkörperphysik. Skript zur Vorlesung. Universität Heidelberg, Heidelberg. Lecture, 2002.

[71] H. J. Barnaby. Total-Ionizing-Dose Effects in Modern CMOS Technologies. *IEEE Transactions on Nuclear Science*, 53(6):3103–3121, 2006. doi: 10.1109/TNS.2006.885952.

[72] P. M. Lenahan and P. V. Dressendorfer. Hole traps and trivalent silicon centers in metal/oxide/silicon devices. *Journal of Applied Physics*, 55(10):3495, 1984. doi: 10.1063/1.332937.

[73] W.L. Warren, M.R. Shaneyfelt, D.M. Fleetwood, et al. Microscopic nature of border traps in MOS oxides. *IEEE Transactions on Nuclear Science*, 41(6):1817–1827, 1994. doi: 10.1109/23.340513.

[74] T. P. Ma and Paul V. Dressendorfer. *Ionizing radiation effects in MOS devices and circuits.* Wiley, New York, 1989. ISBN 9780471848936.

[75] Qingyu Wei. *Studies of Radiation Hardness of MOS Devices for Applocation in a Linear Collider Vertex Detector.* PhD thesis, Technische Universität München, 2008.

[76] M. Walters and A. Reisman. The distribution of radiation-induced charged defects and neutral electron traps in SiO2, and the threshold voltage shift dependence on oxide thickness. *Journal of Applied Physics*, 67(6):2992, 1990. doi: 10.1063/1.345421.

[77] Peter Fischer, Ivan Peric, Christian Kreidl, and Jochen Kinzel. Switcher-B Reference Manual, 2005. Lehrstuhl für Schaltungstechnik und Simulation, Heidelberg. `http://twiki.hll.mpg.de/twiki/pub/DepfetInternal/DesignResourcesSwitcher-B/SwitcherB-ReferenceManual-v1.1-05112010.pdf`.

[78] Ivan Peric, Peter Fischer, Jochen Knopf, and Thi Hong Hanh Nguyen. DCDB and SWITCHERB, the readout ASICS for belle II DEPFET pixel detector. In *2011 IEEE Nuclear Science Symposium and Medical Imaging Conference (2011 NSS/MIC)*, pages 1536–1539, 2011. doi: 10.1109/NSSMIC.2011.6154365.

[79] Kenneth G. Aubuchon. Radiation Hardening of P-MOS Devices by Optimization of the Thermal Si02 Gate Insulator. *IEEE Transactions on Nuclear Science*, 18(6):117–125, 1971. doi: 10.1109/TNS.1971.4326422.

[80] J. R. Schwank and D. M. Fleetwood. Effect of post-oxidation anneal temperature on radiation-induced charge trapping in metal-oxide-semiconductor devices. *Applied Physics Letters*, 53(9):770, 1988. doi: 10.1063/1.99828.

[81] M.R. Shaneyfelt, D.M. Fleetwood, P.S. Winokur, J.R. Schwank, and T.L. Meisenheimer. Effects of device scaling and geometry on MOS radiation hardness assurance. *IEEE Transactions on Nuclear Science*, 40(6):1678–1685, 1993. doi: 10.1109/23.273493.

[82] J. Scarpulla, A.L Amram, V.W Gin, T.C Morse, and K.T Nakamura. Gate size dependence of the radiation-produced changes in threshold voltage, mobility, and interface state density in bulk CMOS. *IEEE Transactions on Nuclear Science*, 39(6):1990–1997, 1992. doi: 10.1109/23.211395.

[83] B. Djezzar, A. Smatti, A. Amouche, and M. Kechouane. Channel-Length Impact on Radiation-Induced Threshold-Voltage shift in N-MOSFET' s Devices at Low Gamma Rays Radiation Doses. *Nuclear Science, IEEE Transactions on*, 47(6):1872–1878, 2000.

[84] Synergy Health Radeberg GmbH. Homepage, 2012. `http://gamma-service.de/`.

[85] Luka Snoj, Gašper Žerovnik, and Andrej Trkov. Computational analysis of irradiation facilities at the JSI TRIGA reactor. *Applied Radiation and Isotopes*, 70(3):483–488, 2012. doi: 10.1016/j.apradiso.2011.11.042.

[86] J. Beringer, J.-F. Arguin, R. M. Barnett, et al. Review of Particle Physics. *Physical Review D*, 86(1), 2012. doi: 10.1103/PhysRevD.86.010001.

[87] P. Azzi, N. Bacchetta, G. Bolla, et al. Radiation damage experience at CDF with SVX′. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 383(1):155–158, 1996. doi: 10.1016/S0168-9002(96)00621-3.

[88] L. Andricek, T. Gebhart, D. Hauff, et al. Single-Sided p+ n and Double-Sided Silicon Strip Detectors Exposed to Fluences up to 2E14 1/cm2 24-GeV Protons. *Nucl.Instrum.Meth*, 409:184–193, 1998. doi: 10.1016/S0168-9002(97)01259-X.

[89] L. Andricek, P. Kodyš, C. Koffmane, et al. Advanced testing of the DEPFET minimatrix particle detector. *Journal of Instrumentation*, 7(01):C01101, 2012. doi: 10.1088/1748-0221/7/01/C01101.

[90] Andreas Pahlke. *Einfluss der Oxidqualität auf die Stabilität von Halbleiterdetektoren bei Röntgenbestrahlung*. PhD thesis, Technische Universität München, 2004.

[91] G. Groeseneken, H.E Maes, N. Beltran, and R.F de Keersmaecker. A reliable approach to charge-pumping measurements in MOS transistors. *IEEE Transactions on Electron Devices*, 31(1):42–53, 1984. doi: 10.1109/T-ED.1984.21472.

[92] G. Groeseneken and H.E. Maes. Basics and applications of charge pumping in submicron MOSFET's. In *1997 21st International Conference on Microelectronics. Proceedings*, pages 581–589, 14-17 Sept. 1997. doi: 10.1109/ICMEL.1997.632911.

[93] N. Stojadinovic, S. Golubovic, V. Davidovic, S. Djoric-Veljkovic, and S. Dimitrijev. Modeling of radiation-induced mobility degradation in MOSFETs. *Microelectronics, 1997. Proceedings., 1997 21st International Conference on*, pages 355–356, 1997. doi: 10.1109/ICMEL.1997.625271.

[94] M.R. Shaneyfelt, J.R. Schwank, D.M. Fleetwood, et al. Interface-trap building rates in wet and dry oxides. *IEEE Transactions on Nuclear Science*, 39(6):2244–2251, 1992. doi: 10.1109/23.211427.

[95] Koichi Awazu, Kikuo Watanabe, and Hiroshi Kawazoe. Generation mechanisms of paramagnetic centers by gamma-ray irradiation at and near the Si/SiO2 interface. *Journal of Applied Physics*, 73(12):8519, 1993. doi: 10.1063/1.353380.

[96] E. H. Nicollian and A. Goetzberger. The Si-SiO2 Interface - Electrical Properties as Determined by the Metal-Insulator-Silicon Conductance Technique. *The Bell System Technical Journal*, 46(6):1055–1133, 1967.

[97] C. Becker, C. Gößling, C. Lichau, et al. Gate-controlled diodes for characterization of the Si–SiO2 interface with respect to surface effects of silicon detectors. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 444(3):605–613, 2000. doi: 10.1016/S0168-9002(99)01177-8.

[98] M.A Jupina and P.M Lenahan. A spin dependent recombination study of radiation induced defects at and near the Si/SiO2 interface. *IEEE Transactions on Nuclear Science*, 36(6):1800–1807, 1989. doi: 10.1109/23.45372.

[99] N. S. Saks. Measurement of single interface trap capture cross sections with charge pumping. *Applied Physics Letters*, 70(25):3380, 1997. doi: 10.1063/1.119177.

[100] N.S Saks and M.G Ancona. Determination of interface trap capture cross sections using three-level charge pumping. *IEEE Electron Device Letters*, 11(8):339–341, 1990. doi: 10.1109/55.57927.

[101] P.M Lenahan, N.A Bohna, and J.P Campbell. Radiation-induced interface traps in MOS devices: capture cross section and density of states of p/ sub 1/ silicon dangling bond centers. *IEEE Transactions on Nuclear Science*, 49(6):2708–2712, 2002. doi: 10.1109/TNS.2002.805357.

[102] Stefan Wölfel. *Neuartige DEPFET-RNDR-Detektoren im experimentellen Betrieb*. PhD thesis, Universität Siegen, Siegen, 2007.

[103] Phillip A. Newman and H. A. R. Wegener. Effect of Electron Radiation on Silicon Nitride Insulated Gate Field Effect Transistors. *Nuclear Science, IEEE Transactions on*, 14(6):293–298, 1967. doi: 10.1109/TNS.1967.4324809.

[104] A.V. Vishnyakov, Yu.N. Novikov, V.A. Gritsenko, and K.A. Nasyrov. The charge transport mechanism in silicon nitride: Multi-phonon trap ionization. *Solid-State Electronics*, 53(3):251–255, 2009. doi: 10.1016/j.sse.2008.07.005.

[105] J. R. Cricchi and D. F. Barbe. Compensation of Radiation Effects by Charge Transport in Metal-Nitride-Oxide-Semiconductor Structures. *Applied Physics Letters*, 19(3):49–51, 1971. doi: 10.1063/1.1653817.

[106] D. T. Krick, P. M. Lenahan, and J. Kanicki. Electrically active point defects in amorphous silicon nitride: An illumination and charge injection study. *Journal of Applied Physics*, 64(7):3558, 1988. doi: 10.1063/1.341499.

[107] S.-D. Tzeng and S. Gwo. Charge trapping properties at silicon nitride/silicon oxide interface studied by variable-temperature electrostatic force microscopy. *Journal of Applied Physics*, 100(2):023711, 2006. doi: 10.1063/1.2218025.

[108] M. Aminzadeh, S. Nozaki, and R.V Giridhar. Conduction and charge trapping in polysilicon-silicon nitride-oxide-silicon structures under positive gate bias. *IEEE Transactions on Electron Devices*, 35(4):459–467, 1988. doi: 10.1109/16.2480.

[109] Y. C. Park, W. B. Jackson, N. M. Johnson, and S. B. Hagstrom. Spatial Profiling of Electron Traps in Silicon Nitride Thin Films. *Journal of Applied Physics*, 68(10): 5212–5221, 1990. doi: 10.1063/1.347064.

[110] Y. Takahashi, K. Ohnishi, T. Fujimaki, and M. Yoshikawa. Radiation-Induced Trapped Charge in Metal-Nitride-Oxide-Semiconductor Structure. *Nuclear Science, IEEE Transactions on*, 46(6):1578–1585, 1999. doi: 10.1109/23.819124.

[111] Hao Jin, K. J. Weber, and P. J. Smith. Defect generation at SiO2-Si interfaces by low pressure chemical vapor deposition of silicon nitride. *Applied Physics Letters*, 89(9): 092120, 2006. doi: 10.1063/1.2345247.

[112] L. Andricek, Z. Doležal, P. Kodyš, et al. Laser tests of the DEPFET gated operation. *Journal of Instrumentation*, 8(01):C01051, 2013. doi: 10.1088/1748-0221/8/01/C01051.

[113] Felix Müller. Operation of DEPFET in gated mode for Belle II. Master Thesis, 2012. Ludwig-Maximilians-Universität München, München.

[114] Hans-Günther Moser. PXD progress and prospect. 13th Open Meeting of the Belle II Collaboration, 2012. Tsukuba. `http://kds.kek.jp/materialDisplay.py?contribId=18&sessionId=14&materialId=slides&confId=10927`.

[115] P.M Lenahan and J.R Conley. A comprehensive physically based predictive model for radiation damage in MOS systems. *IEEE Transactions on Nuclear Science*, 45(6): 2413–2423, 1998. doi: 10.1109/23.736480.

[116] Timothy R. Oldham. Switching Oxide Traps. *International Journal of High Speed Electronics and Systems*, 14(02):581–603, 2004. doi: 10.1142/S0129156404002533.

[117] J. R. Schwank, P. S. Winokur, P. J. McWhorter, et al. Physical Mechanisms Contributing to Device Rebound. *IEEE Transactions on Nuclear Science*, 31(6):1434–1438, 1984. doi: 10.1109/TNS.1984.4333525.

[118] A.J Lelis, T.R Oldham, H.E Boesch, and F.B McLean. The nature of the trapped hole annealing process. *IEEE Transactions on Nuclear Science*, 36(6):1808–1815, 1989. doi: 10.1109/23.45373.

[119] F. B. McLean, H. E. Boesch, J. M. McGarrity, and R. B. Oswald. Rapid annealing and charge injection in Al2O3 MIS capacitors. *IEEE Transactions on Nuclear Science*, 21(6):47–55, 1974. doi: 10.1109/TNS.1974.6498905.

[120] T. R. Oldham, A. J. Lelis, and F. B. McLean. Spatial Dependence of Trapped Holes Determined from Tunneling Analysis and Measured Annealing. *IEEE Transactions on Nuclear Science*, 33(6):1203–1209, 1986. doi: 10.1109/TNS.1986.4334579.

[121] T.R Oldham and F.B McLean. Total ionizing dose effects in MOS oxides and devices. *IEEE Transactions on Nuclear Science*, 50(3):483–499, 2003. doi: 10.1109/TNS.2003.812927.

[122] A.J. Lelis and T.R. Oldham. Time dependence of switching oxide traps. *IEEE Transactions on Nuclear Science*, 41(6):1835–1843, 1994. doi: 10.1109/23.340515.

[123] A.J. Lelis, H.E. Boesch, T.R. Oldham, and F.B. McLean. Reversibility of trapped hole annealing. *IEEE Transactions on Nuclear Science*, 35(6):1186–1191, 1988. doi: 10.1109/23.25437.

[124] J.R. Schwank, D.M. Fleetwood, M.R. Shaneyfelt, et al. Latent interface-trap buildup and its implications for hardness assurance (MOS transistors). *IEEE Transactions on Nuclear Science*, 39(6):1953–1963, 1992. doi: 10.1109/23.211391.

[125] Zdenek Dolezal, Christian Kiesling, Carlos Lacasta, and Hans-Günther Moser. The PXD Whitebook, 2013.

[126] V.A.K. Raparla, S.C. Lee, R.D. Schrimpf, D.M. Fleetwood, and K.F. Galloway. A model of radiation effects in nitride–oxide films for power MOSFET applications. *Solid-State Electronics*, 47(5):775–783, 2003. doi: 10.1016/S0038-1101(02)00375-1.

[127] Dietrich Widmann, Hans Friedrich, and Hermann Mader. *Technologie hochintegrierter Schaltungen*. Halbleiter-Elektronik. Springer, Berlin [u.a.], 2. edition, 1996. ISBN 978-3540593577.

[128] M.R. Shaneyfelt, D.M. Fleetwood, J.R. Schwank, and K.L. Hughes. Charge yield for cobalt-60 and 10-keV X-ray irradiations of MOS devices. *IEEE Transactions on Nuclear Science*, 38(6):1187–1194, 1991. doi: 10.1109/23.124092.

[129] C. Marinas and M. Vos. The Belle-II DEPFET pixel detector: A step forward in vertexing in the superKEKB flavour factory. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 650(1):59–63, 2011. doi: 10.1016/j.nima.2010.12.116.

[130] S. Heindl. Thermische Studien zur Entwicklung eines DEPFET-Halbleiterdetektors für das Belle II-Experiment. Diploma thesis, 2010. Universität Karlsruhe, Karlsruhe.

[131] J. Beringer. Statistics, PDG, 2012. Particle Data Group, Phys. Rev. D86 and 010001. http://pdg.lbl.gov.

[132] Benjamin Schwenker. Gated Mode Test Beam. DESY 2012. 10th International Workshop on DEPFET Detectors and Applications, 2012. Seeon. Internal document. https://indico.mpp.mpg.de/getFile.py/access?contribId=27&sessionId=6&resId=0&materialId=slides&confId=1364.

[133] Martin Ritter. Belle Hit Distribution in SVD, Layer 0, 22.09.2010. Personal Communication.

[134] S. Rummel. *Investigation of DEPFET as vertex detector at ILC intrinsic properties, radiation hardness and alternative readout schemes*. PhD thesis, Technische Universität München, München, 2009.

[135] Martin Ritter. PXD Digitizer Studies: Clusters and Dynamic Range. 7th International Workshop on DEPFET Detectors and Applications, 2011. Ringberg Castle. https://indico.mpp.mpg.de/contributionDisplay.py?sessionId=8&contribId=52&confId=1249.

[136] M. Guthoff, O. Brovchenko, W. de Boer, et al. Geant4 simulation of a filtered X-ray source for radiation damage studies. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 675:118–122, 2012. doi: 10.1016/j.nima.2012.01.029.

[137] Keithley. 4200-SCS Semiconductor Characterization System - Technical Data, 2011. Keithley. www.keithley.com.

[138] Agilent Technologies. Agilent 4284A Precision LCR Meter. Operation Manual, 2001. Agilent Technologies, Japan. http://www.home.agilent.com/agilent/editorial.jspx?cc=DE&lc=ger&ckey=1000002196:epsg:man&nid=-536902441.0.00&id=1000002196:epsg:man.

Acknowledgments

I want to thank Prof. Caldwell for supervising this thesis.

Special thanks belong to Hans-Günther Moser for giving me the opportunity to work in the Semiconductor Laboratory of the Max Planck Society. His mentoring and advice made this thesis possible. Thank you also for proofreading this work.

I am also indebted to Rainer Richter who shared his incredible knowledge of the DEPFET and semiconductor physics with me. Thank you for fruitful discussions.

I do not want to forget my colleague Christian Koffmane. He was always open-minded and spent time with me for discussions on the PXD and the DEPFET.
Also I have to thank Martin Ritter for his support concerning particle physics.
Special thanks go to Stefan Petrovics, who freely offered me the access to his measurements of the bulk damage studies of the DEPFET. It was great working with him.
I am also indebted to Ladislav Andricek. His pragmatic view on measurement setups and the assessment of data taught me to focus on important aspects.
Thanks also belong to Paola Avella for proofreading of some of my chapters and discussions about them.

I also want to thank my other colleagues at the Semiconductor Laboratory. First of all to the people who actually produced my devices and the DEPFET in general. Thanks also to the working crews in the institute and in the laboratory who attached the bond wires to the chips and made my measurements possible. And thanks to all whom I cannot list here. It was great working with you in the office and in the laboratory.

Special thanks also go to the facilities where my devices could be irradiated. First to the people at IEKP in Karlsruhe. They always welcomed me and ensured a pragmatic and easy work environment. Thanks is also owed to the people of the collaboration in Bonn who helped me with the electron irradiation.

I also want to thank my parents for their support.
Last but not least I want to thank Regine for proofreading and enduring assistance.