Fakultät für Physik
Lehrstuhl für experimentelle Physik E18

The Neutron-Lifetime Experiment PENeLOPE and the Intelligent FPGA Data Acquisition Framework IF-DAQ

Dominic Maximilian Gaisbauer

Vollständiger Abdruck der von der Fakultät für Physik der Technischen Universität München zur Erlangung des akademischen Grades eines Doktors der Naturwissenschaften genehmigten Dissertation.

Vorsitzender: Prof. Dr. Andreas Weiler

Prüfer der Dissertation:
1. Prof. Dr. Stephan Paul
2. Prof. Dr. Lothar Oberauer

Die Dissertation wurde am 13. Mai 2019 bei der Technischen Universität München eingereicht und durch die Fakultät für Physik am 18. Juli 2019 angenommen.

Abstract

The neutron lifetime $\tau_n = 879.6 \pm 0.8$ s is an important parameter in the Standard Model of particle physics and in Big Bang cosmology. Several systematic corrections of previously published results reduced the PDG world average by several seconds in the last years together with a measurement difference of several seconds between the beam type experiments and the storage experiments call for a new experiment. At the Technische Universität München a new **P**recision **E**xperiment on **Ne**utron **L**ifetime **O**perating with **P**roton **E**xtraction is currently under construction. It aims to determine the neutron lifetime with a precision of 0.1 s. It will confine ultra-cold neutrons in a magneto-gravitational trap using superconducting magnets and will measure their lifetime by both neutron counting and online detection of decay protons. In this thesis I will present the progress I have made on the experiment during this time. Recently, a lot of advances have been made to create a framework which enables an simplified construction of data acquisition systems for new and existing experiments. This framework, **i**ntelligent **F**PGA **DAQ** framework, is developed at the Technische Universität München and includes several FPGA cards for measuring times, digitize analog signals or process detector data digitally. Additionally, the framework includes an event builder and a newly developed communication framework for the communication between different FPGA modules. The second part of the thesis will introduce the iFDAQ framework and the progress which has been achieved there by myself in this area.

Zusammenfassung

Die Neutronenlebensdauer $\tau_n = 879.6 \pm 0.8$ s ist ein wichtiger Parameter im Standardmodell der Teilchenphysik und in der Untersuchung des Urknalls. Nachdem in den letzten Jahren einige Experimente ihre alten Daten korrigiert haben, reduzierte sich die Lebensdauer des Neutrons, veröffentlicht von der PDG, um einige Sekunden. Dies, zusammen mit der Diskrepanz zwischen Strahl- und Speicherexperimenten, verlangt nach einem neuen Experiment mit besserer Systematik. An der Technischen Universität München befindet sich das "**P**recision **E**xperiment on **Ne**utron **L**ifetime **O**perating with **P**roton **E**xtraction Experiment" im Aufbau. Dieses benutzt eine Speicherflasche für ultrakalte Neutronen, bestehend aus supraleitenden Spulen. Das Besondere an diesem Experiment ist die Kombination der Neutronenzählung zusammen mit der Detektion der Zerfallsprotonen. Diese Kombination führt dazu, dass das Experiment eine Genauigkeit von 0.1 s erreichen will. Diese Dissertation erläutert die Arbeiten, die ich während meiner Promotion an diesem Experiment ausgeführt und den Fortschritt, den ich hierdurch bislang erreicht habe. In der letzten Zeit floß viel Arbeit in die Entwicklung einer Rahmenstruktur, die es ermöglichen soll neue und alte Datennahmesysteme zu errichten oder zu ersetzen. Diese Rahmenstruktur heißt **i**ntelligent **F**PGA **DAQ** und wird an der Technischen Universität München entwickelt. Dazu gehören FPGA Module um Zeiten zu messen, analoge Signale in digitale umzuwandeln oder digitale Daten weiter zu verarbeiten. Weiterhin wurde in diesem Zuge ein neues Datenübertragungsprotokoll entwickelt, welches die Kommunikation zwischen zwei FPGA Karten erleichtern soll. Der zweite Teil dieser Dissertation wird iFDAQ einführen und detailiert beschreiben, welche Entwicklungen ich während meiner Promotion dort erbracht habe.

Contents

Part I

Precision Experiment on Neutron Lifetime Operating with Proton Extraction

Chapter 1

Introduction

1.1 The Neutron

In the year 1930 Walter Bothe and Herbert Becker [5] shot alpha particles from the radioactive decay of polonium onto beryllium and observed an untypical neutral radiation. By mistake, they took it as gamma radiation despite the fact that it showed strange behavior like accelerating of light particles which would lead to gamma energies way to high. One year after, the Curies used the radiation in an ionization chamber without any significant current flow [8]. The experiments of the Curies motivated Chadwick in 1932 [7] to prove, in a series of experiments, that the radiation consists of particles with a mass very close to that of a proton. His discovery led to the Nobel prize in 1935.

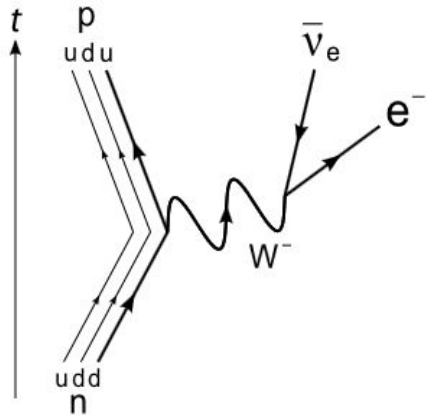


Figure 1.1: Feynman diagram of the neutron decay.

Nowadays, we know that a neutron is an electrically neutral baryon with a mass of 1.00866491588 u [52] where u is the atomic mass unit. The neutron consists of one up quark and two down quarks as shown in fig. 1.1. If it is bound within a

nucleus, the neutron is stable but when unbound, the neutron decays through weak interaction with a decay energy of 0.782343 MeV [52].

$$n^0 \rightarrow p^+ + W^- \rightarrow p^+ + e^- + \bar{v}_e \tag{1.1}$$

This involves the changing of one down into an up quark by emitting a short lived W^- boson, which by itself decays into an electron and electron anti-neutrino. Most of the decay energy is transferred to the electron which has a maximum kinetic energy of 0.782 ± 13 MeV [52].

1.2 Ultra-cold Neutrons

Free neutrons are typically produced in spallation sources or fission reactors. In spallation sources typically a tungsten or tantalum target is shot with an accelerated particle beam. The beam produces free neutrons by the spallation process within the target. Fission reactors commonly use uranium 235 which is bombarded by free neutrons and, by this, decays then into fission products with a mass around 95 and 135 u plus some additional neutrons which by themselves can induce more fission of uranium. This chain reaction leads to a continuous operation of nuclear fission reactors. Neutrons produced in both spallation source and fission reactor are typically in the energy range of several MeV. A classification of the neutron by velocity and energy range can be found in table 1.1.

Class	**Energy [eV]**	**Velocity [m/s]**
Fast	$10 \cdot 10^3$ to $20 \cdot 10^6$	$>$
Thermal	$\approx 10 \cdot 10^{-3}$	2200
Cold	10^{-3}	400
Very Cold	10^{-6}	100
Ultra-cold	$100 \cdot 10^{-9}$	5

Table 1.1: Classification of neutrons in energy and velocity regimes according to Golub [21].

Fast neutrons produced in neutron sources are moderated to the thermal energy regime by elastic scattering. Due to their long wavelength (several angstroms) thermal neutrons can be described as a material wave and are reflected by material walls under very small glancing angles. The total reflection of such a neutron beam can be enhanced by multilayer coating of the glass guides with nickel and titanium . In order to obtain even slower neutrons they first have to be moderated further by e.g. liquid deuterium at 25 K to reach the cold and very cold energy regime. To get to even lower energies of less than 300 neV several methods have been implemented in ultra-cold neutron (UCN) sources around the world. At the Institut Laue-Langevin (ILL) in Grenoble very cold neutrons with an average speed of 50 m/s are extracted by a curved vertical guide from the reactor core and guided towards a turbine rotating at 25 m/s. The neutrons are reflected on the turbine wheels

and are Doppler-shifted towards lower energies [50]. Another form of UCN source uses the super-thermal conversion process ([20]) where pre-moderated neutrons excite solid state excitations - mainly phonons - within the lattice of a solid state converter. If an incoming neutron scatters of the lattice and excites such a phonon, it can loose nearly all of its energy and reach the ultra-cold energy regime. This process is called down-scattering. Also the inverse process - up-scattering - is possible, where an excited phonon transfers its energy onto an ultra-cold neutron and by this accelerates it. In order to reduce such an up-scattering process the moderators are cooled to cryogenic temperatures. Examples for these sources are [16], [28] and [34] which either use super-fluid helium or frozen deuterium as a moderator. Ultra-cold neutrons interact with gravitation, magnetic fields, the weak force and the strong force. In interaction with gravitation UCN can gain or loose depending on the direction of movement $102.51945556(64)$ neV/m [21]. Magnetic fields interact with the magnetic moment of the neutron with $60.307740(15)$ neV/T [21]. Depending on the orientation of their magnetic moments in a magnetic field the neutrons are either attracted by large gradients - high-field-seekers (HFS) - or repelled by large gradients - low-field-seekers (LFS) - as can be seen in fig. 1.2.

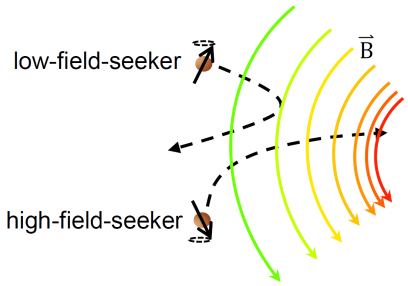


Figure 1.2: Flight path of high-field and low-field-seekers in a magnetic field [39].

The wavelength of UCN can be calculated with the De-Broglie equation $\lambda = \frac{h}{m_n v_n}$ where m_n is the mass of the neutron, v_n the velocity and h the Planck's constant. UCN thus have large wavelengths of more than 50 nm. If a UCN scatters on a material it will only see the combination of the nucleon interaction potentials since it has only a very short range in the order of 2 fm. Fermi [14] introduced an effective Fermi-Potential

$$V = \frac{2\pi\hbar^2}{m} N_A \tag{1.2}$$

describing the interaction of UCN with material. In the calculation of the effective wall potential in the equation above m is the mass of the neutron and N_A is the Avogrado's constant. UCN with energies less than this effective potential will be reflected under any angle of incidence. Table 1.2 lists the Fermi-Potential of some materials. Elements with a negative potential are very effective UCN absorbers. The critical velocity - below which the UCN are totally reflected from a material -

can be calculated from the Fermi-Potential via the equation $v_c = \sqrt{\frac{2V}{m_n}}$ where m_n is the mass of the neutron.

Material	Fermi-Potential [neV]
^{58}Ni	335
^{nat}Ni	252
Fe	210
Cu	168
Al	54
Ti	-48

Table 1.2: List of Fermi-Potential values of different materials from Golub [21].

1.3 Neutron Lifetime

Free unbound neutrons decay due to the weak interaction with a decay time of $879.6 \pm 0.8\ s$ [52]. Since they interact with all forces except for electric ones the neutrons are a perfect tool for manifesting the Standard Model of physics and for investigating the Big Bang nucleosynthesis.

1.3.1 Standard Model of Particle Physics

Within the Standard Model of particle physics the unitarity of the Cabibbo-Kobayashi-Maskawa (CKM) matrix is predicted. The CKM matrix describes the mixing of quarks of three flavor generations when interacting via the weak interaction. Thus the mixing of the mass eigenstates d, s and b into the weak eigenstates d', s' and b' can be described with the following equation.

$$\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \begin{pmatrix} d \\ s \\ b \end{pmatrix}. \tag{1.3}$$

The neutron lifetime τ_n is inversely dependent on the squared matrix element V_{ud} since it is dependent on the conversion of a down quark into a up quark.

$$|V_{ud}|^2 = \frac{(4908.7 \pm 1.9)s}{\tau_n(1+\lambda^2)} \tag{1.4}$$

In the equation above the numerator is a collection of radiative corrections and constants and $\lambda = \frac{g_A}{g_V}$ is the ratio of the axial vector and vector coupling. The latter can be calculated precisely with results of experiments like PERKEO I-III ([10], [42], [36]). Currently, the most precise value for V_{ud} is 0.97420 ± 0.00021 [52] but new experiments like PENeLOPE and PERC [33] will improve the error down by one order of magnitude if they meet their claimed precision.

1.3.2 Big Bang Nucleosynthesis

The Big Bang Nucleosynthesis (BBN) describes the formation and abundances of light elements at a very early stage of the universe with the help of Standard Model physics. When the energy of the universe was much higher than 1 MeV the reactions

$$n + \nu_e \rightarrow p + e^- \tag{1.5}$$

$$p + \bar{\nu}_e \rightarrow n + e^+ \tag{1.6}$$

were in a thermal equilibrium leading to a neutron to proton ratio of $\frac{n}{p} = e^{\frac{Q}{T}} = 1$. Here n and p are the amount of neutrons and protons, Q is the mass difference between the n and the p and T the temperature. At an energy of about 1 MeV the reactions above where no longer in an equilibrium and the ratio was dominated by the neutron decay (compare fig. 1.3). Starting from the freeze-out until nuclear reactions began the neutron to proton rate shifted from 1:6 to 1:7 by the decay. Approximately 100 seconds after the Big Bang or at an energy of below 0.1 MeV the threshold of photo-dissociation for the deuterium was undershot and deuterium started to form by the reaction

$$n + p \rightarrow d + \gamma. \tag{1.7}$$

From the deuteron heavier elements could form and mostly ended up in ^{4}He which is the most stable light element in the early universe at that time. The abundance of the ^{4}He can be described by the equation

$$Y_p = \frac{2n/p}{1 + n/p}. \tag{1.8}$$

The neutron lifetime in fact has an impact on the BBN in two ways. Firstly, it describes the time of the freeze out ($t \approx 1$ s) by changing the weak interaction rates and secondly, it defines the rate of neutron decays between the freeze out and the light element formation ($t \approx 100$ s) and by this has an impact on the equation above.

1.3.3 Lifetime Measurements

The measurement of the neutron lifetime can be divided into two kinds of experiments - beam experiments and storage experiments.

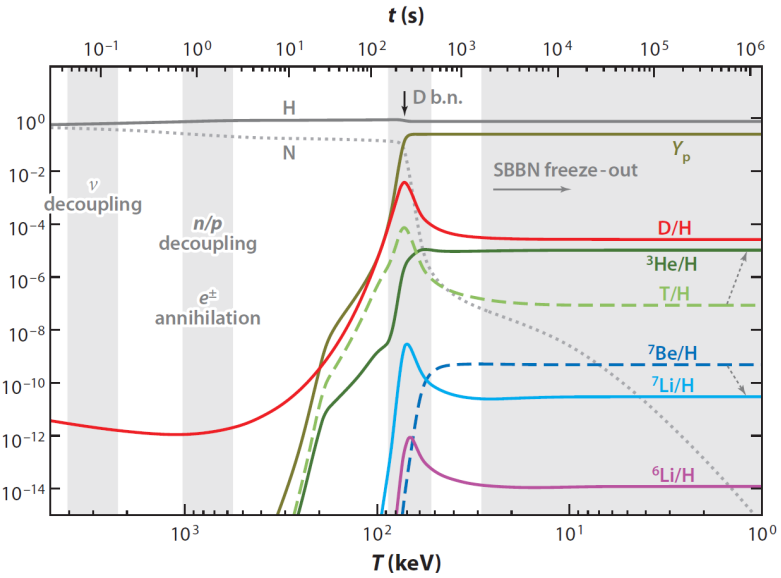


Figure 1.3: Time and temperature evolution of all standard big bang nucleosynthesis (SBBN)-relevant nuclear abundances [41]

Beam Experiments

In beam experiments the neutron lifetime is determined from the rate of the neutron decay products (protons and electrons) extracted from a neutron beam. A sketch of the experiment of Nico et al. ([37]) is shown as an example of this kind of experiment in fig. 1.4 a. Typically, the electrons and protons are guided via magnetic fields outside of the beam onto the detectors whereas the remaining neutrons can be stopped in a beam dump. For a precise measurement the decay volume, the neutron intensity and the proton and electron extraction and detection efficiency must be known precisely. Examples for this type of experiment are listed in table 1.3. Currently, the average of these most recent and precise experiments is $886.9 \pm 1.2 \pm 2.8\ s$.

Year	Group	Lifetime [s]
2013	Yue et al. [58]	$887.7 \pm 1.2 \pm 1.9\ s$
2005	Nico et al. [37]	$886.3 \pm 1.2 \pm 3.2\ s$
2003	Dewey et al. [9]	$886.8 \pm 1.2 \pm 3.2\ s$

Table 1.3: Neutron lifetime experiments using neutron beams. The lifetimes are given with systematic error in the first place and a statistical in the second.

Storage Experiments

Storage experiments fill e.g. ultra-cold neutrons into a gravitational, magnetic, material or combined trap and store them there for a specific time. After different storage times the remaining neutrons are extracted and counted. Together with the precise knowledge of the incoming neutron density or a constant neutron flux over the different storage times the lifetime can be determined precisely. Examples for this type of experiment are shown in table 1.4 and as an example sketch the experiment of Ezhov et al. ([13]) is shown in fig. 1.4 b. Currently, the average of these most recent and precise experiments is $879.9 \pm 0.87^{+0.83}_{-0.8}\ s$.

Year	Group	Lifetime [s]
2018	Ezhov et al. [12]	$878.3 \pm 1.6 \pm 1.0\ s$
2018	Pattie et al. [38]	$877.7 \pm 0.7^{+0.4}_{-0.2}\ s$
2018	Serebov et al. [48]	$881.5 \pm 0.7 \pm 0.6\ s$
2012	Steyerl et al. [51]	$882.5 \pm 1.4 \pm 1.5\ s$
2010	Pichlmaier et al. [40]	$880.7 \pm 1.3^{\pm}1.2\ s$
2005	Serebov et al. [47]	$878.5 \pm 0.7 \pm 0.3\ s$

Table 1.4: Neutron lifetime experiments using neutron beams. The lifetimes are given with systematic error in the first place and a statistical in the second.

Conclusion

As can be seen from fig. 1.5 there is a clear difference between the results of beam and storage experiments. Together with an error of nearly one second on the most recent PDG value of $\tau_n = 879.6 \pm 0.8\ s$ this is a reasonable motivation for a new precise neutron lifetime experiment. Currently, the PDG mean lifetime is mostly determined by storage experiments.

1.4 PENeLOPE

The **P**recision **E**xperiment on **Ne**utron **L**ifetime **O**perating with **P**roton **E**xtraction (PENeLOPE) combines the advantages of a storage experiment and that of a beam experiment (especially monitoring of the decay particles) into one measurement aiming for a precision of less than 0.1 s. Fig. 1.6 shows a CAD model of the experiment. The center of the experiment is a magneto-gravitational trap for UCN consisting of twenty-four superconducting coils with an overall height of one meter and an equal diameter. The principle of magnetic storage is more favorable than storing neutrons in a material bottle due to better storage times and easier error handling. Due to the large alternating current directions within the different coils and the gravitation, a storage potential for UCN of up to 115 neV is created which follows the equation $V = m_n g z + \mu_n B$ in a height z above the bottom of the trap. The UCN have to be polarized and spin flipped before entering the trap as low-field-seekers which can be stored nearly without losses. In some areas of the storage volume the

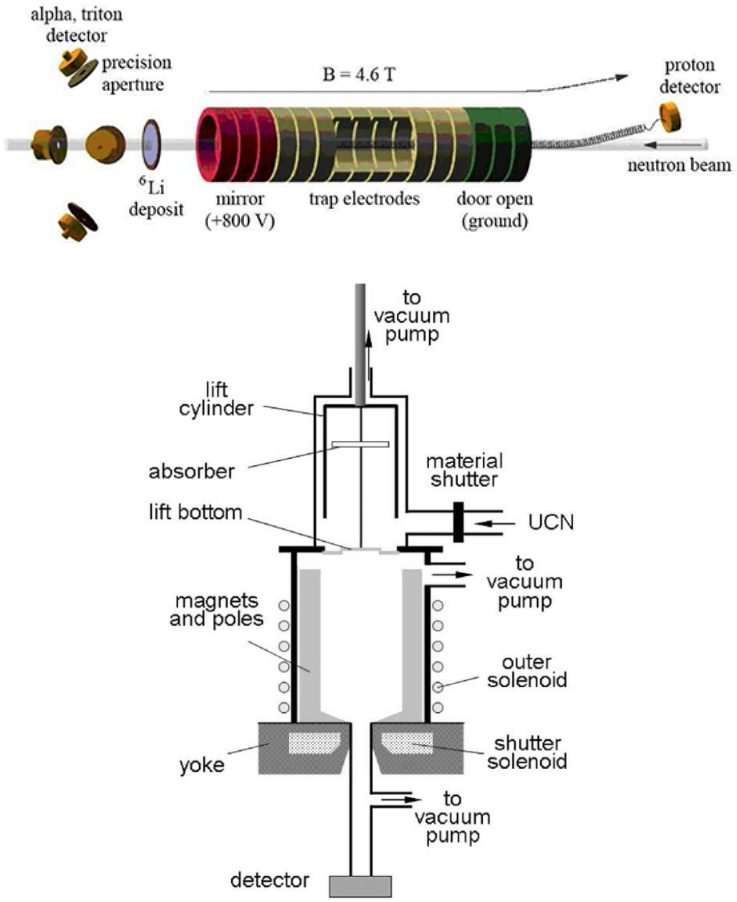


Figure 1.4: (a) Neutron lifetime beam experiment of Nico et al. ([37]). (b) Neutron lifetime storage experiment of Ezhov et al. ([13]).

topology of the coils can lead to zero field areas. These zero field areas can turn the LFS into HFS, which in turn can lead to losses of UCN and by this to a distortion of the measurement. To overcome this, a large central current is running vertically through the middle of PENeLOPE creating an azimuthal field overlaying the zero field areas. Due to the fact that the coils have a defined time for ramping to nominal current the LFS can turn into HFS by hitting the walls. These marginally trapped neutrons can shift the measurement to an effective lifetime which is lower than the real lifetime by hitting the wall during the measurement and leaving the trap. To clean up the high-field-seekers from the spectrum an absorber mechanism is also installed in the cryostat. The storage volume itself is covered by a proton detector counting the protons from the decay. It is placed on a high electrical potential in order to guarantee a sufficient extraction of protons out of the trap.

A typical experimental cycle of PENeLOPE can be found in table 1.5 and starts with the filling of the UCN from the source. When the UCN are filled, the magnets start to ramp up to generate the storage potential. This phase is then followed by the movement of the absorber removing the remaining HFS. Afterwards, the

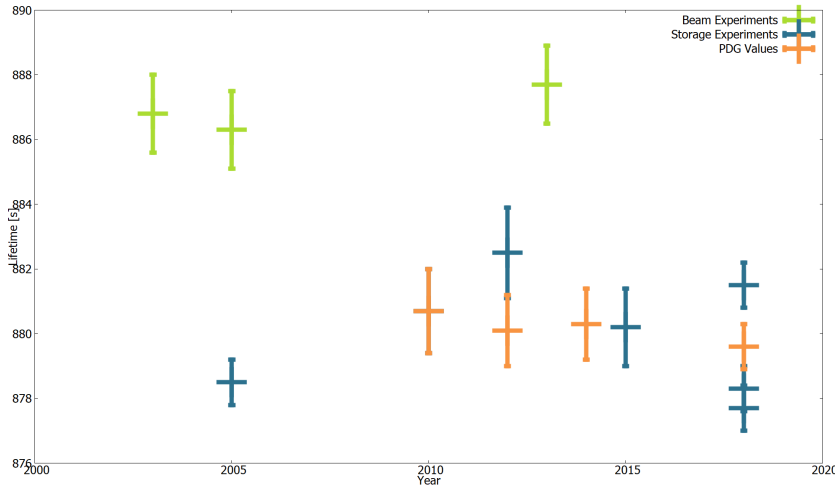


Figure 1.5: Most recent and precise neutron lifetime experiments with beam experiments marked in green and storage experiments in blue. All experiments plotted here are included in the PDG averages marked in orange.

UCN will be stored for different storage times. The ramping down of the magnets after the storage time is followed by the counting of the remaining neutrons. If this cycle is repeated several times and the count values are inserted into a graph plotting storage time versus the number of remaining neutrons, the decay curve of the neutron can be seen (compare fig. 1.7). For each point in this graph the proton count rate can be monitored over time and also here the decay curve is clearly visible following the equation $N(t) = N_o \cdot e^{-\frac{t}{\tau_n}}$. The following chapters will describe all parts of PENeLOPE in more detail. Starting with the UCN preparation in chapter 2, followed by the magneto-gravitational trap and all superconducting coil tests in chapter 3, the central coil in chapter 4, the absorber in chapter 5, the proton detector in chapter 6 and the experiment control in chapter 7. Error corrections for the lifetime measurement and impact assessments of different error sources have been done and can be found in [45]. They are not part of this thesis.

	Stage	**Duration [s]**
1	filling	~ 200
2	ramping up	100
3	cleaning	150
4	storage	variable up to 5000
5	ramping down	100
6	emptying	~ 200

Table 1.5: Experimental stages of PENeLOPE

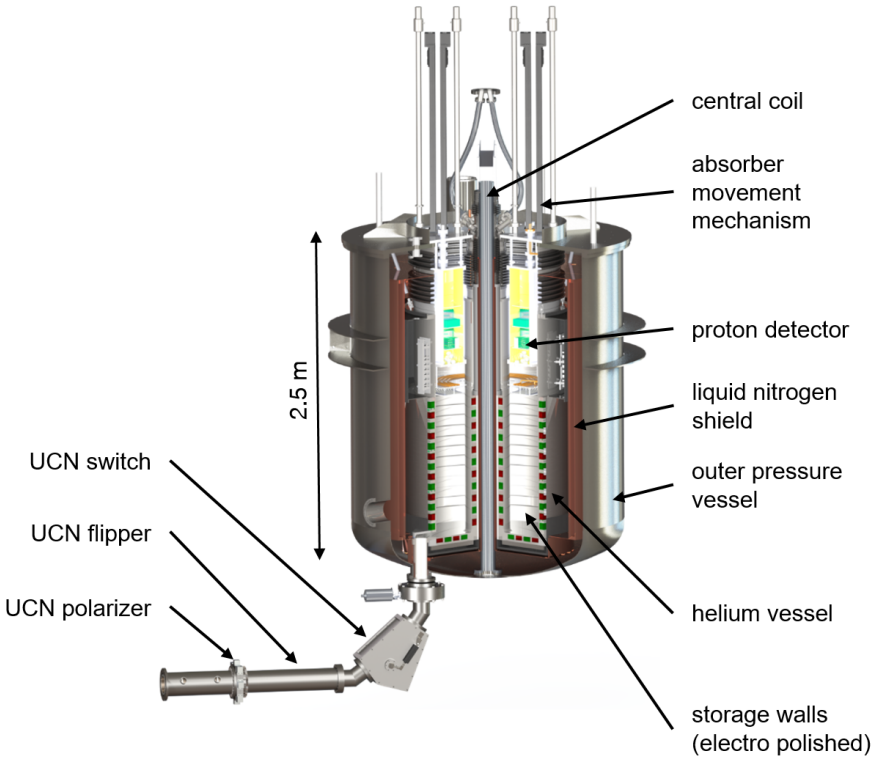
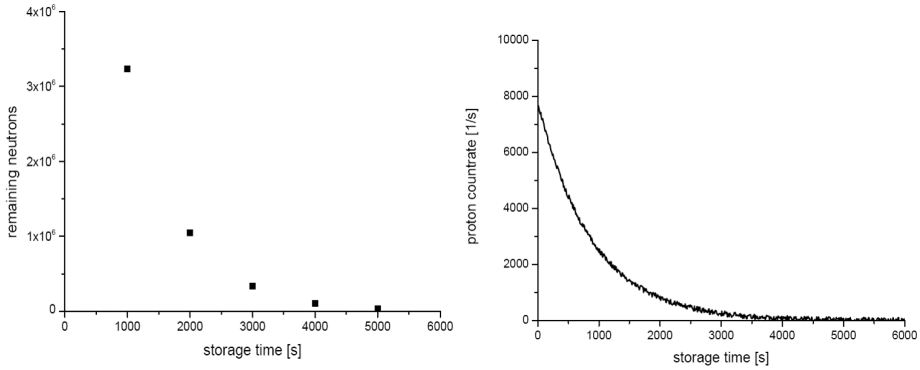


Figure 1.6: CAD model of the PENeLOPE cryostat. On the lower left all parts concerning the UCN guiding like the polarizer, flipper and switch are depicted. In the center of the picture is the LHe cryostat with the superconducting coils surrounded by the thermal radiation shield and the vacuum tank. In the upper part of the picture the absorber and additional instrumentation is shown.



(a) (b)

Figure 1.7: Decay curve of the neutron with storage measurements (a) and proton measurements (b). The error bars are hidden within the simulated points.

Chapter 2

UCN Preparation

Due to the design of the PENeLOPE experiment a precision of less than 0.1 s in the neutron lifetime measurement is only possible if the UCN from the source are polarized and turned into low-field-seekers by a spin flipper before being stored in the trap. According to [45] the polarization has to be approximately 90 %. If the polarization is less and too many high-field-seekers enter the trap they could introduce a large systematic effect (about 0.7 s [45]) on the measurement. The following sections will describe the theory and the hardware of the polarizer and the spin flipper and end with the results of the beam measurement in the TRIGA reactor in Mainz.

2.1 Polarization

2.1.1 Theory

Depending on the direction of the magnetic moment of the UCN mentioned in 1.2 they will observe a potential of

$$V = \pm\mu_n|B| \tag{2.1}$$

in a strong magnetic field. If UCN pass through a magnetically saturated iron foil they are exposed to a potential of

$$V = V_{Fermi} \pm \mu_n B \tag{2.2}$$

again depending on the orientation of the magnetic moment with respect to the field. It can be seen that the low-field-seeker will see a potential barrier of $V = V_{Fermi} + \mu_n B$ and high-field-seeker will observe a potential well of $V = V_{Fermi} -$

$\mu_n B$. In order to achieve a high transmission for the high-field-seeker and a low transmission for the low-field-seeker - which will then result in a large degree of polarization - the potential well should ideally vanish. Fig. 2.1 illustrates the potential barrier and well. [23] and [30] showed that a certain mixture of iron and cobalt ($Fe_{0.5}Co_{0.5}$) would have a polarization of more than 90 %. With the iron and cobalt mixture the potential well would be $V = 135 - 60.3 \cdot 2.4 = 9.72$ neV and the potential barrier would be $V = 135 + 60.3 \cdot 2.4 = 279.72$ neV.

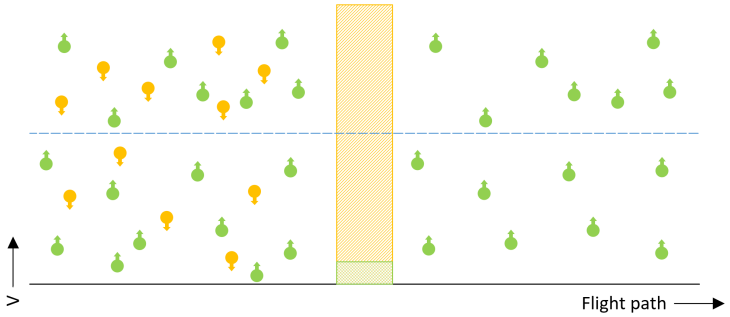


Figure 2.1: The potential barrier seen by LFS in orange and the potential well seen by HFS in green. The dashed blue line is the Fermi potential of the polarizer foil.

2.1.2 Hardware

The polarizer designed by [45] is shown in fig. 2.2 as a picture and a CAD model. On both sides it has the possibility to either connect a standard stainless steel UCN guide or a Replika UCN guide which is a rolled sheet of a nickel vanadium mixture ($Ni_0.93V_0.07$) within a stainless steel vacuum tube. The centerpiece of the polarizer are two stainless steel blocks (1.4401 /EN10088-2 - non magnetizing stainless steel) which press the polarizer foil within their center. The foil itself is made from aluminum and is coated with 150 nm of the iron mixture mentioned in section 2.1.1. Aside from being the backing material the aluminum foil separates the vacua before and after the polarizer which is crucial for PENeLOPE where the UCN guide system will have a vacuum of about 10^{-4} mbar whereas the experimental vacuum is in the region of 10^{-8} mbar. [45] calculated a minimum transverse magnetic field of 10 mT in order to saturate the iron foil. A minimum field of 13.4 mT is produced by a Halbach array of eight permanent NdFeB magnets oriented around the polarizer holder.

For holding the polarity and preventing undesired spin flips behind the polarizer a holding field must be generated surrounding the guide until the neutrons enter the storage volume. The holding field is generated by three pairs of Helmholtz coils shown in fig. 2.3. They generate a minimum field of 1 mT which is sufficient according to [45] to hold the polarity.

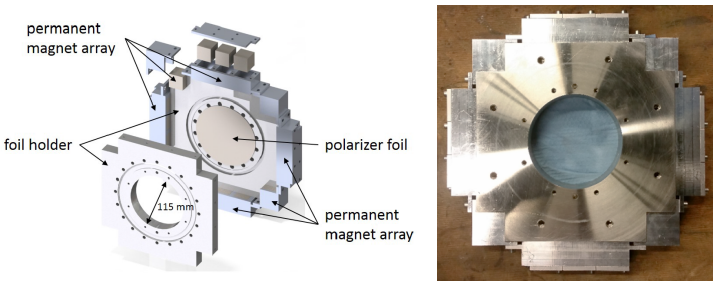


Figure 2.2: (a) CAD model of the polarizer. (b) Picture of the polarizer (size 40 cm x 40 cm).

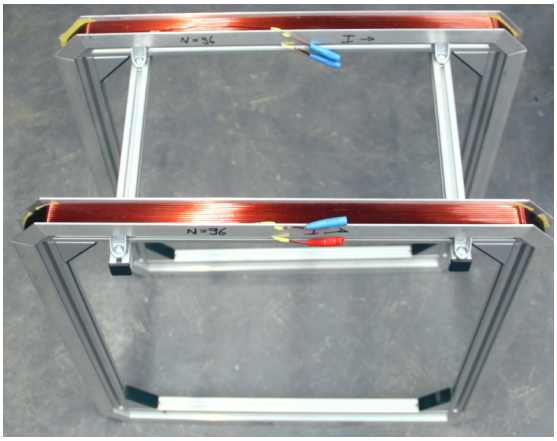


Figure 2.3: Picture of the Helmholtz coils designed by [45].

2.2 Spin Flipper

2.2.1 Theory

A combination of both - static and dynamic - magnetic fields for changing the spins is the fundamental principle of the nuclear magnetic resonance. A device from this technology is the adiabatic fast passage (AFP) spin flipper used for UCN spin changes. The AFP consists of a static field perpendicular to the direction of motion of the UCN and a rotating field oscillating around the direction of motion ([23],[19]). Another version of the AFP has a static field parallel to the direction of motion of the UCN and the oscillating field is perpendicular to it ([25]). For PENeLOPE the first version is preferable since it is easier to implement. The effective field seen by the neutron is described by

$$B_{\text{effective}} = \left(B_0 - \frac{\omega}{\gamma_n}\right) \cdot \mathbf{z} + B_1 \cdot \mathbf{x} \tag{2.3}$$

where $\gamma_n = 1.83247172 \frac{1}{sT}$ ([52]) is the gyro-magnetic ratio of the neutron. If the

oscillation frequency of the magnetic field B_1 is in the order of the Lamor frequency, the equation above will change to $B_0 = \frac{\omega}{\gamma_n}$ and the neutron is in a resonance point which will lead to a inversion of its spin with respect to the field B_0.

2.2.2 Hardware

The AFP spin flipper is enclosed by the Helmholtz coils described in section 2.1.2 which, according to [45], have a static field B_0 of 1 mT in their center. This field leads to a resonance frequency of

$$B_0 = \frac{\omega}{\gamma_n} \rightarrow f = \frac{\gamma_n B_0}{2\pi} = 29.165\ kHz. \tag{2.4}$$

The oscillating coil is a cylindrical solenoid wound onto a coated glass tube which is used as an UCN guide. It is coated with nickel and molybdenum ($\mathrm{Ni}_{0.85}\mathrm{Mo}_{0.15}$). According to [45] the flipper coil must produce a peak magnetic field of at least 0.05 mT. Following the equation

$$B = \mu_0 \frac{\mathrm{IN}}{\mathrm{L}} \tag{2.5}$$

for air filled cylinder coils the coil consists of 20 windings N on a length L of 160 mm. Together with a current I of 2.5 A this leads to a minimum field of 0.39 mT. The impedance of this coil which is wound with some distance between the windings is $38\ \mu\mathrm{H}$ leading to an impedance of $2\pi f L = 6.96\ \Omega$. This perfectly matches the impedance of the commercial Reloop Dominance 702 audio amplifier ([2]) used by [45] in the previous spin flipper design. Together with a standard sine frequency generator this completes the AFP spin flipper design.

2.3 Qualification Measurements

In order to test the polarizer and spin flipper system an experiment at the TRIGA reactor in Mainz was performed in 2018. The two setups used there are shown in fig. 2.4. The following section will give an overview of the different measurements and the spectrum of the UCN source.

2.3.1 UCN Source Spectrum

In order to get the spectrum of the UCN source in Mainz, the setup shown on the left side of fig. 2.4 was used. It consists of a chopper, a two meter UCN guide and a CASCADE-U ([1]) UCN detector. A chopper is a device containing two linear motors driving two titanium grids coated with gadolinium in opposite directions. By

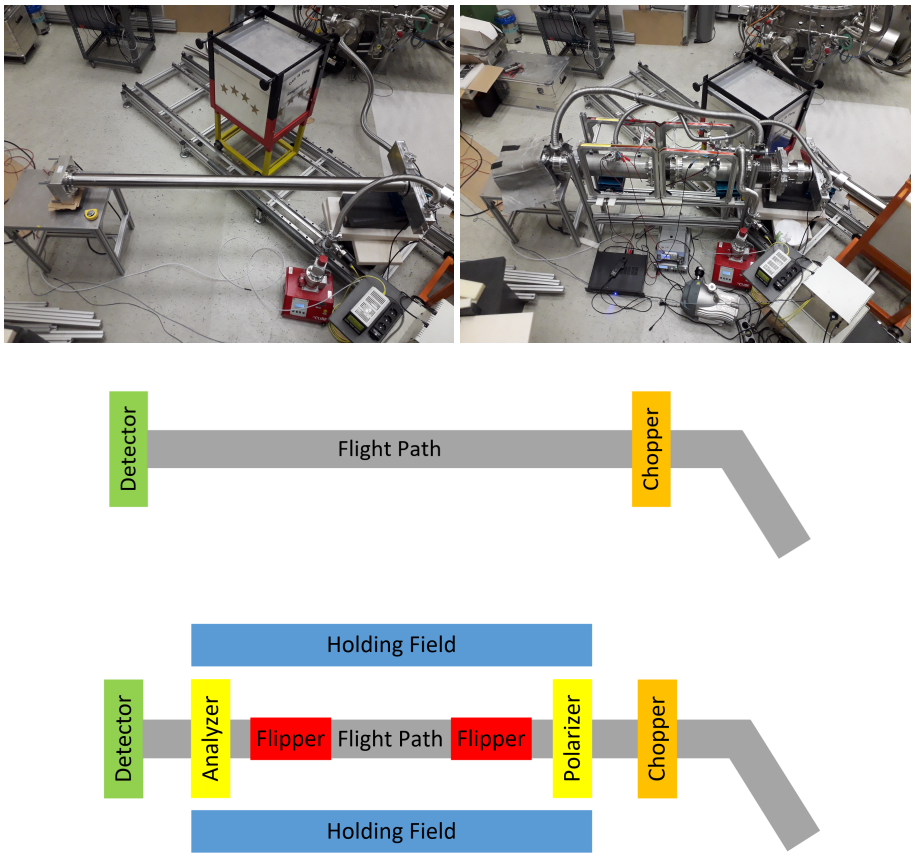


Figure 2.4: (a + c) Characterization setup for the UCN source spectrum. (b + d) Characterization setup for the spin flipper efficiency.

defining opening and closing times, the grids can either overlap in a way that they open half of the guide or they can overlap in a way that they completely close the guide and all UCN are absorbed in the titanium. For this setup the opening time was 100 ms followed by a closing time of 1000 ms. The CASCADE-U detector is made up of one $^{10}\mathrm{B}$ layer on an aluminum foil with GEM foils and the readout PCB in between. UCN are absorbed in the boron and charges which are then multiplied in the GEMs and readout via a pixel detector. The measurement principle used is the time-of-flight (TOF) measurement which will give a velocity dependent spectrum of the UCN. Fig. 2.5 and 2.6 show the raw and cleaned velocity spectrum collected during a two hour measurement time. One can identify the UCN peak at a velocity of 5.4 m/s. The right side of the graph is the VCN shoulder which is known to be quite significant in Mainz. In the second graph the UCN peak was fitted with a Gaussian and shows the actual UCN spectrum of the source.

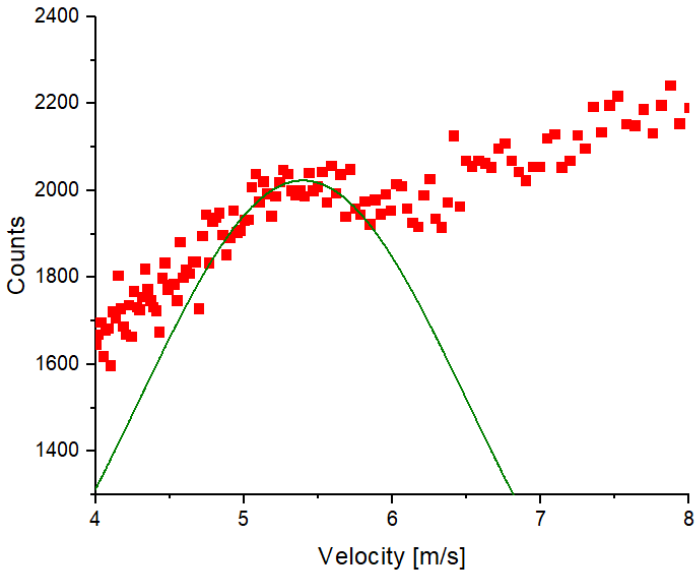


Figure 2.5: Velocity spectrum of the source in Mainz.

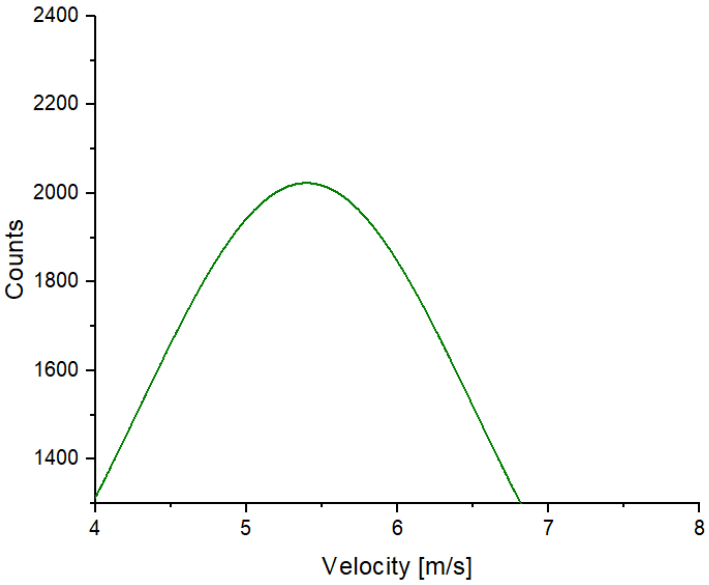


Figure 2.6: Cleaned UCN spectrum of the source in Mainz showing only the fit.

2.3.2 Background Measurement

For testing the background at the reactor in Mainz the shutter to the UCN source was kept close and all flipper devices in the setup shown in fig. 2.4 (b) where turned off. The setup consists of the chopper (same type as in the measurement before),

a polarizer as described in section 2.1.2, a 1.4 m flight path equipped with two spin flippers as described in section 2.2.2, an analyzer (same as the polarizer) and the CASCADE-U UCN detector. In fig. 2.7 the background collected in a two and a half hour period is shown. All following graphs in the other sections will be background subtracted with the mean background value of 421 counts.

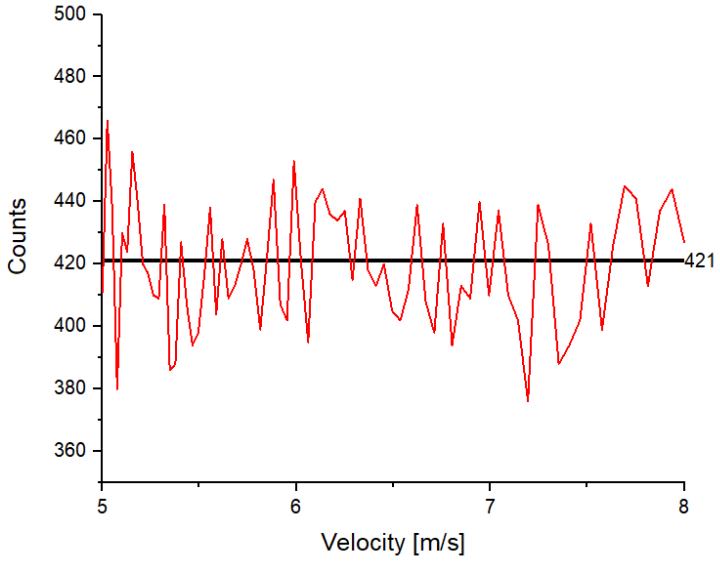


Figure 2.7: Background of the source in Mainz. The mean value was taken.

2.3.3 Reference Measurement

In order to determine the efficiency of the spin flipper there has to be a reference measurement on how the velocity spectrum looks like when both flippers are turned off and the UCN will only see the polarizer and analyzer in their flight path. Additionally, the holding field is turned on. This spectrum cleaned of the background is shown in fig. 2.8 and is the reference for 100 % transmission.

2.3.4 Flipper Measurements

In order to determine the efficiency of the spin flipper design, three more measurements were executed. All measurements are shown together with the reference in fig. 2.9. In the first measurement only one spin flipper was turned on which should result in almost no counts in the detector since the HFS from the polarizer are turned into LFS which cannot pass the analyzer. The second measurement repeated the same thing with the other flipper turned on. Finally both flippers were turned on and the transmission now should be close to 100 % again since now the HFS are turned into LFS by the first flipper and turn from LFS to HFS again in the second flipper.

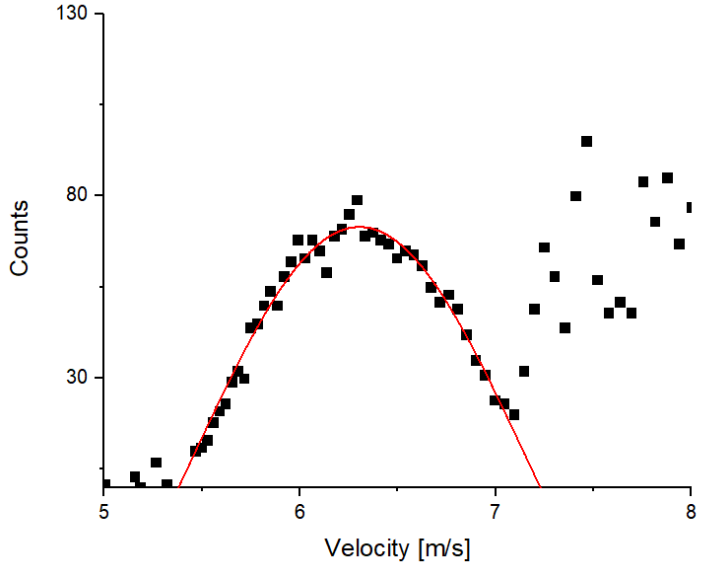


Figure 2.8: Reference measurement for the spin flipper efficiency.

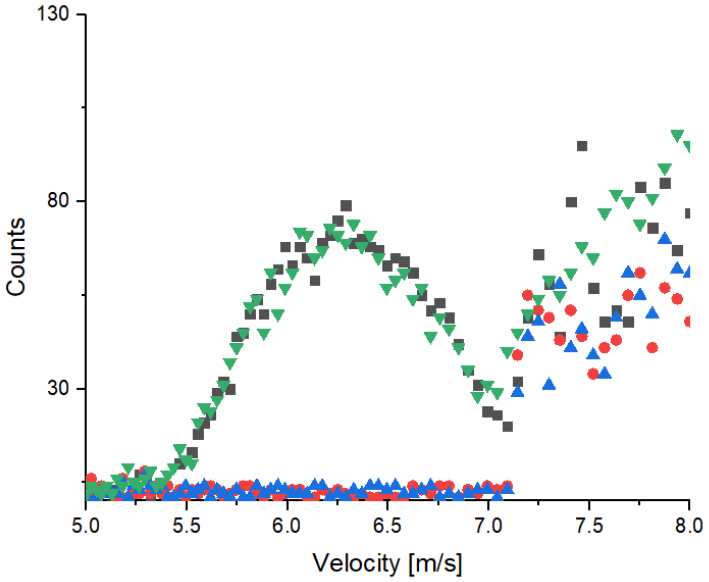


Figure 2.9: Neutron spectrum between 8 and 5 meter per second velocity. Grey is the reference, green the measurement with both flippers on, blue the one with flipper one on and red the one with flipper two on.

To determine the efficiency the UCN counted in the detector in the different bins was divided by the reference count in the respective bin. This is plotted in fig. 2.10 where additionally between the region of interest the mean value was calculated

for the measurements with one flipper and the one with two flippers. It can be seen that in the latter case only 2.5 % of the UCN still pass the setup and in the first case 97.5 % of the UCN reach the detector. Thus the overall efficiency of the spin flipper is 98.7 % which is according to [45] enough to reach the precision PENeLOPE is aiming for.

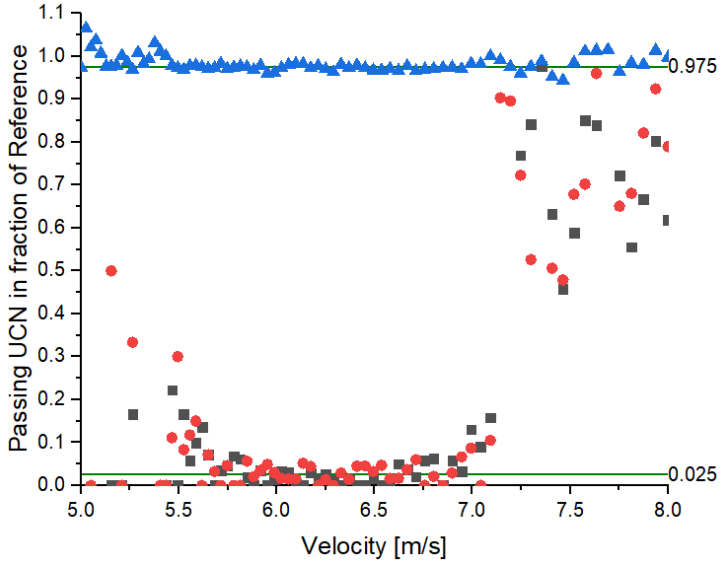


Figure 2.10: Efficiency of the measurements. Blue shows the two flipper measurement and red and grey the one flipper measurements. Additionally the mean is shown for the blue points and the red and grey together.

Chapter 3

Magneto-Gravitational Trap

The magneto-gravitational trap of the PENeLOPE experiment consists of twenty-four individual superconducting coils. All coils are wound onto a carrier made of stainless steel (1.4409 ; EN 1088-2), suitable for applications with high magnetic fields. The NbTi wire used for the coils is the Supercon VSF-SSCI. It is made of a copper core surrounded by 7400 superconducting filaments and has a bare diameter of 0.9 mm, a total diameter of 0.95 mm and a copper to superconductor volume ratio of $1.5:1$ [26]. Each of the coils has between 1520 and 1940 windings depending on the position and size in the coil stack. Due to the winding force of 105 N the superconducting wire even sticks to the coil former when there are thermal or magnetic forces. The ”air gaps” within the winding package are filled with an epoxy resin. A cut through the superconductor and a CAD model the coils can be found in figure 3.1.

3.1 Superconductor VSF-SSCI

The NbTi wire used for PENeLOPE becomes superconducting if the temperature falls below 9.2 K [26]. To guarantee a sufficient cooling of the magnet system it is embedded into a liquid helium tank cooling it to about 4.2 K. As every superconductor, the NbTi has a critical current density, a critical temperature and critical magnetic field above which it will become normal conducting again. According to [35] and [6] the critical current density and with it the critical current can be calculated via

$$J_c = \frac{C_0}{B} \cdot \left(\frac{B}{B_0}\right)^{\alpha} \cdot \left(1 - \frac{B}{B_0}\right)^{\beta} \cdot \left(1 - \left(\frac{T}{T_{c0}}\right)^{1.7}\right)^{\gamma} \tag{3.1}$$

$$I_c = J_c \cdot J_{Ref} \cdot A_{Eff} \tag{3.2}$$

(a) (b)

Figure 3.1: (a) A cut through the superconductor used with a diameter of 0.95 mm. (b) A CAD model of coil stack with a height of 1 m.

with

$$B_0 = B_{c0} \cdot \left(1 - \left(\frac{T}{T_{c0}}\right)^{1.7}\right) . \tag{3.3}$$

In these equations $T_{c0} = 9.2$ K is the critical temperature of NbTi at $B = 0$ T, $B_{c0} = 14.5$ T is the critical magnetic field of NbTi at $T = 0$ K, $J_{Ref} = 2122\ \mathrm{A/mm^2}$ is the reference current density of NbTi at $T = 4.2$ K and $B = 5$ T and $A_{Eff} = 0.254\ \mathrm{mm^2}$ the effective superconductor area within the diameter of the VSF-SSCI wire. The parameters for the equations were determined with the help of Supercon by testing to $C_0 = 28$ T, $\alpha = 0.6$, $\beta = 1$ and $\gamma = 2$. With these parameters the superconductor of PENeLOPE is underestimated meaning that the resulting calculated critical current is always below the effective real current density. The dependence of the current on the field, the temperature and the working point of PENeLOPE is shown in figure 3.2. It can be seen that at the operating point of PENeLOPE a nominal current of 283.5 A, necessary to create the storage potential of up to 115 neV, is 25 % below the critical line of the NbTi superconductor material. Nevertheless, superconducting coils need to be trained in order to reach the nominal current. During this training current is ramped through the coil and at some point the windings within the coil windings will move into a energetically more favorable position. These small movements introduce heat into the superconductor leading to a loss of superconductivity within the coil which is rapidly spreading over the whole coil. This process is called a quench. In the next ramping cycle the coil will sustain a bigger current until finally the nominal current is reached.

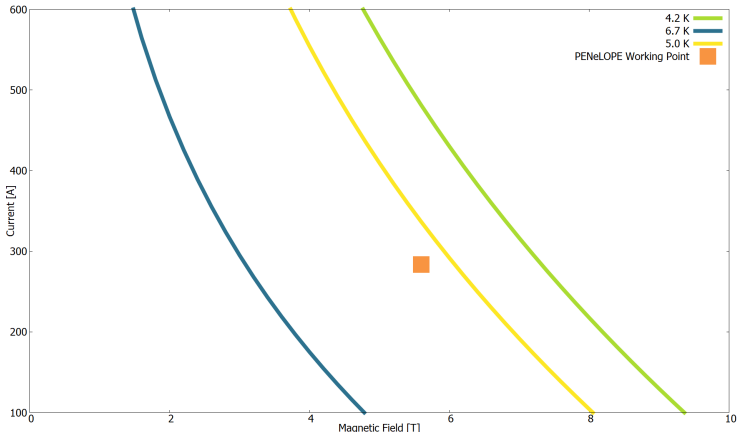


Figure 3.2: Critical current of the VSF-SSCI superconductor at different temperatures and the working point of PENeLOPE.

3.2 Magnet Training

As mentioned in the previous section superconducting coils have to be trained before they can reach their nominal current. This section will describe the quench training of individual coils and coil stacks of the PENeLOPE experiment, the coil testing facility and the quench protection needed.

3.2.1 Quench Protection

Figure 3.3 shows the electrical scheme of the magnet system. In the case of a quench the power supply tries to maintain the current flow and due to Ohm's law the voltage increases. The voltage over each coil pair and the power supply in general is monitored and if a sudden rise in any of these voltages is detected the interlock $IL1$ is released by the quench protection software. The energy still stored within the quenched coils has to be dissipated in the water-cooled dump resistor $R1$ within the power supply. According to Lenz's law high voltages are induced within the coils in order to maintain the current flow. These large voltages can damage the coil and have to be limited. Therefore, two coils are always bridged with DS502ST14 diodes from DYNEX. In the training set-ups described in the following sections only fractions of the quench protection system shown in figure 3.3 are used. Coils with alternating current directions are paired because according to [49] the overall forces within the whole system during a quench are the lowest with this set-up. The tensions reach up to a maximum of 62 MPa.

3.2.2 Coil Test Experiment

In order to test and train the coils for PENeLOPE the Coil Test Experiment (CoTEx) facility was used ([35], [46], [45] and [17]) and figure 3.4 shows a CAD cut through

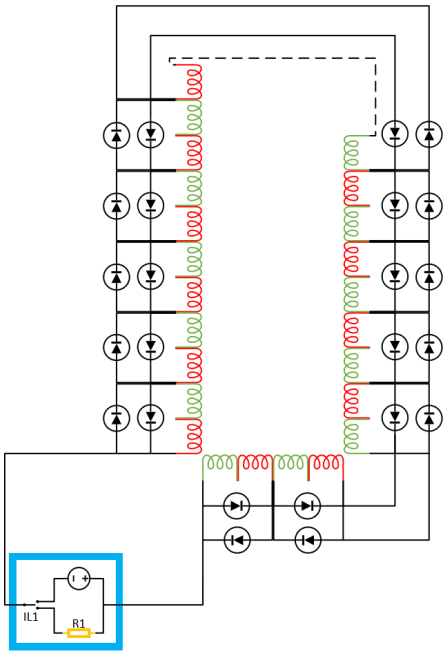


Figure 3.3: Electrical scheme of the PENeLOPE quench protection. The green and red symbolize the alternating directions of the current within the coils. The blue enclosed area is the power supply.

it. It consists of an inner liquid helium tank with a volume of roughly 1000 l and a diameter of 1.7 m. The 4 K inner tank is surrounded by a copper shield with pipes soldered onto it which are cooled with liquid nitrogen to 77 K. Both tanks are then surrounded with a vacuum tank of $3\ \mathrm{m}^3$ which is able to hold a vacuum of up to 10^{-6} mbar at 4 K. The lids of the different tanks are equipped with multiple feed-throughs which assure space for a proper experimental control and monitoring. To fill the cryostat, a helium liquefier with a liquefaction rate of up to 15 l/h was used. In order to control, monitor and protect the experiment a CompactRIO system from National Instruments ([27]) was embedded in an electrical cabinet. It is a modular system consisting of a central CPU with a real-time operating system and a FPGA in the backplane of the CompactRIO shelf holding all I/O modules.

Monitoring

The CoTEx experiment monitors and stores several different parameters which are useful for the quench analysis and the control of the experiment to a Citadel database. Pressure is measured via two WIKA A10 sensors capable of a pressure region of 0 to 250 bar connected to the $4...20$ mA modules of the CompactRIO. The vacuum is read out via a RS232 connection to the CenterThree from Leybold which is itself connected to two PTR90 ultra high vacuum sensors from Leybold. For temperature measures, there are PT100 sensors for the liquid nitrogen shield and the outside of the cryostat and CERNOX sensors for the inside of the cryostat and the

monitoring of the coil(s). PT100 sensors are directly connected to the CompactRIO whereas the CERNOX are connected to LakeShore LS218 temperature monitors having the calibration curve of each sensor stored inside. The latter are then read out via RS232. In order to have a measure of the liquid helium level within the cryostat, a helium level sensor from American Magnetics is used which is connected to an American Magnetics Model 135 helium level monitor which is then read out via RS232. The helium level sensor consists of a superconducting filament shielded in a metal pipe. Depending on the fill level the residual resistance of the filament is monitored. All data stored to the database are marked with a global time stamp for post analysis of quenches.

Control

For control purposes there are several relays and RS232 connections. Via RS232 connections the liquid nitrogen flow through the copper shield is controlled and via Ethernet the superconducting coil power supply is regulated. Several different digital I/Os are used for activating and deactivating the vacuum pumps and controlling their high and low speed modes. Furthermore, the vacuum shutter is controlled hereby.

Protection

Since CoTEx holds several hundred liters of cryo-liquids there are active and passive protection systems mounted onto the experiment. The nitrogen and helium systems are both protected with over pressure valves. If the pressure within the helium tank still gets too big or the over pressure valves fail, the gas is relieved via a burst disk opening at an overpressure of 1 bar. Additionally to the pressure protection system the experimental area of CoTEx also has an oxygen monitoring system in order to warn and protect the working personnel. As mentioned in section 3.1 the superconducting coils need a special quench protection and monitoring system. For this purpose, a floating differential voltages measurement module is connected to the CompactRIO. This measures the voltages across the bridged coils and triggers the interlock in the power supply if any differential voltage is above a set threshold. The NI9229 module is capable of voltages of ± 60 V and therefore too small for the PENeLOPE light system in section 3.2.6 which will generate differential voltages of more than 100 V. For this purpose, the system was adapted and an additional isolation amplifier module was connected in front of the existing one. The new module is the WAGO 2857 isolation amplifier capable of differential voltages of ± 200 V at the input. It transfers these voltages to a scale of ± 10 V at the output and is thus compatible with the existing system.

3.2.3 Prototype Coil

In order to verify and test the design and performance of the superconducting coils produced by Babcock Noell GmbH (BNG) the prototype coil was build. It equals in

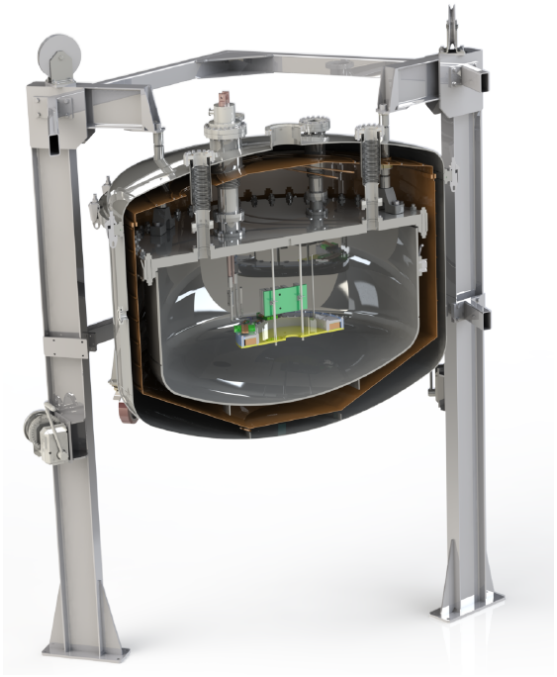
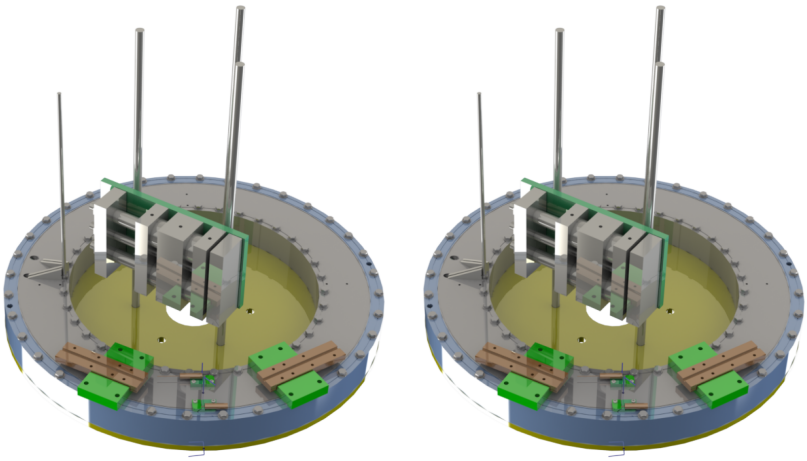


Figure 3.4: CAD cut trough CoTEx. The experiment has a height of 3 meters.

dimension the innermost bottom coil of the trap which was expected to be the most critical one due to its large winding package height-to-width ratio. Figure 3.5 shows a CAD and real image of the prototype coil. For the training procedure the coil was equipped with seven CERNOX sensors which should help to evaluate the position of the quench.

The prototype coil was the most extensively tested coil which, in addition to the training, went through mechanical and thermal stress introduced by welding and transportation. This was done to investigate the consequences of stress on the training achievements. Furthermore this coil was ramped with larger rate than actually required and it was mounted and dismounted several times. Figure 3.6 shows the quenching diagram of the coil with quench current versus quench number. It can be seen that eight different training cycles have been performed, indicated by different colors. In between the runs, the coil was either only warmed up for some time or the coil was mechanically or thermally treated. Overall the coil needs at least one quench after mechanical load (up to $7000\ \mathrm{m/s^2}$ [45]) or a temperature cycle of warming up and cooling down before being operated stably. The mechanical load might be transportation or disassembly and reassembly. A bigger thermal load on the coil like welding will result in a complete loss of the achieved training. In addition to the quench training the triple stack went through several ramping cycles with different ramp rates up to 3 A/s and the nominal current was held for several hours. In total this means that the complete coil system of PENeLOPE needs to be retrained no matter what achievements have been done already before welding. Nevertheless, the prototype coil fulfilled the design requirements and reached



(a) (b)

Figure 3.5: (a) Prototype coil (diameter of 40 cm) as a CAD image. (b) Prototype coil picture.

much more than the necessary current of 283.5 A.

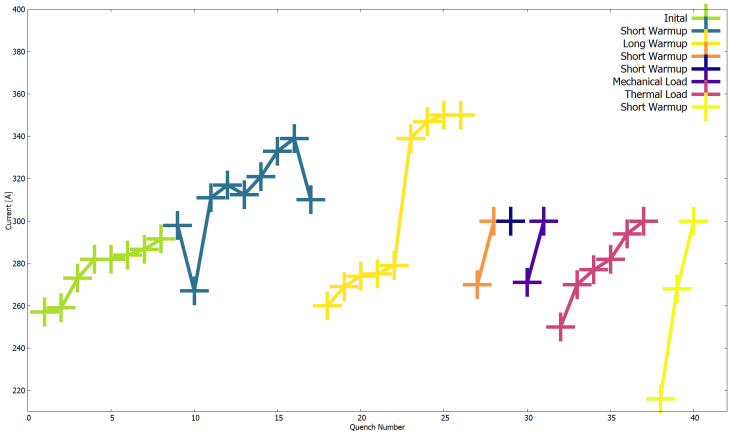
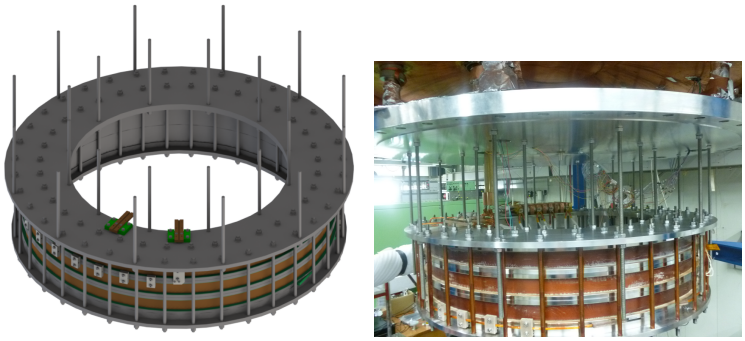


Figure 3.6: Quench history of the prototype coil

3.2.4 Triple Coil Stack

After the successful commissioning of the prototype coil, BNG started the production of the first outer coils in a stack of three coils (compare figure 3.7). Due to some qualification problems of the welding procedure of the coils they were delivered late and in a clamped state. As can be seen from figure 3.8 the unwelded stack reached at most 251 A and even went down in current again. After this behavior it was decided to test all coils individually in order to confirm that all coils

were manufactured properly. Figure 3.8 shows that all coils behaved as expected and reached the nominal current easily. The welding of the triple stack erased all training of the individual coils but, as can be seen, however, the nominal current was reached after nineteen quenches. Additionally to the quench training the triple stack went through several ramping cycles with different ramp rates up to 3 A/s and the nominal current was held for several hours.



(a) (b)

Figure 3.7: Triple coil stack with a diameter of 1 meter as a CAD image (a) and as a picture (b).

3.2.5 Inner Coil

The next coil in the training procedure was the first inner coil of the final coil production. A picture and CAD model of the coil can be found in figure 3.9. During the training procedure the inner coil showed a very fluctuating quench behavior and eventually did not reach the nominal current of 283.5 A. After sixteen quenches the inner coil reached the nominal current (compare figure 3.10). The last three quenches happened all on the same current while holding the current for some minutes. After calculating the forces on the coil, the definition of the nominal current on this coil was lowered to 270 A. This current represents the forces which are acting on the coil in the PENeLOPE trapping system. With the current of 270 A several ramping sessions were conducted successfully.

3.2.6 PENeLOPE Light

The next step in the buildup of PENeLOPE was to produce a first bottle shaped magnet assembly which can be seen in figure 3.11. It consists of the four bottom, two outer and two inner coils. This assembly also worked as a technology demonstrator of the complete magnet system since the most critical forces of the PENeLOPE system are impacting on the joints of bottom, outer and inner coils. Furthermore, a topology like this has never been built before with superconducting magnets operating under these conditions. Due to the large forces on the coils while being operated, the inner part of the trap would lift up several millimeters. This

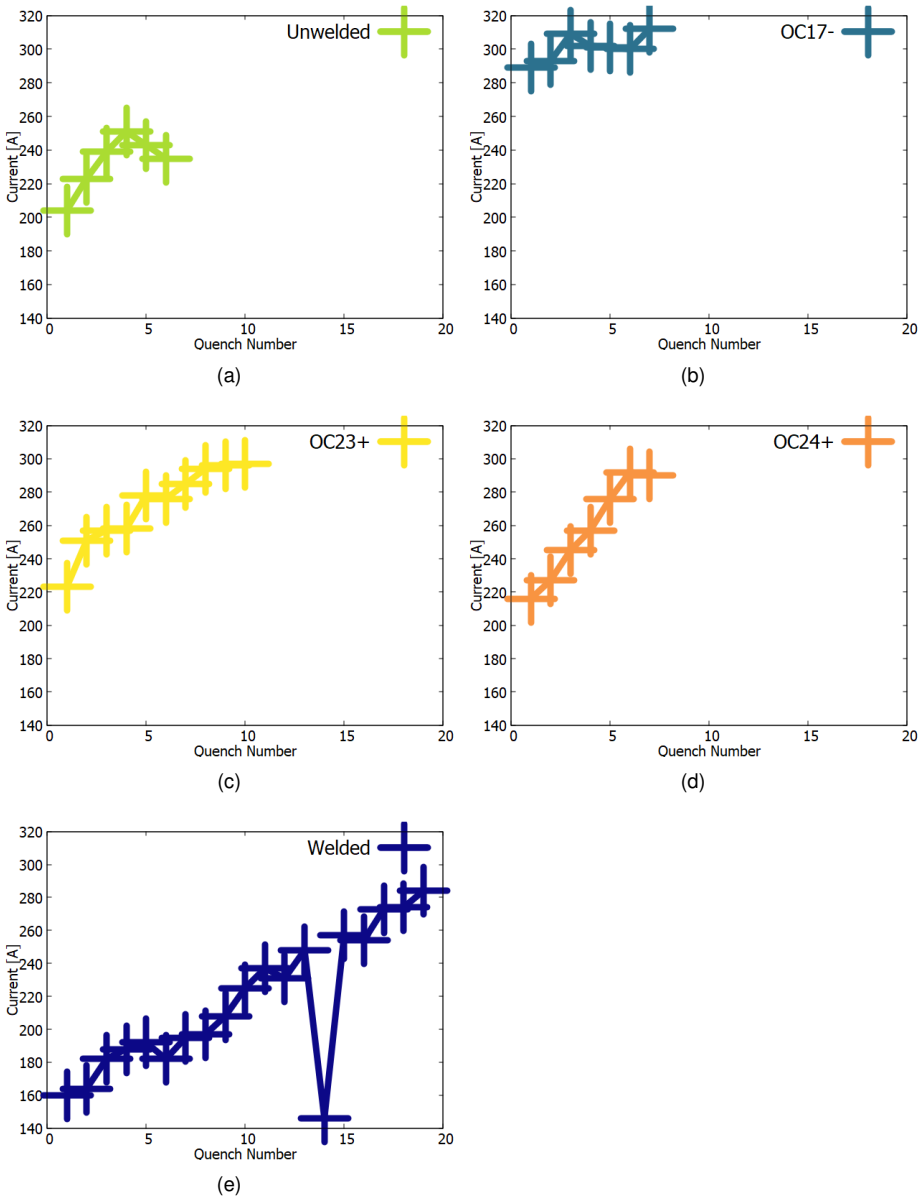


Figure 3.8: Quench history of the unwelded (a) and welded stack (e) and the three individual coils (b-d).

effect would distort the trapping potential and could potentially lead to quenches of the whole system. To overcome this, fins were welded to the bottom of the trap which can be seen in the CAD image in figure 3.11.

The training history of the PENeLOPE Light system consisting of eight coils (two inner, two outer and four bottom) can be found in figure 3.12 and shows, just like the inner coil, a very fluctuating quenching behavior. Several different approaches

(a) (b)

Figure 3.9: Inner coil with a diameter of 330 cm as a CAD image (a) and as a picture (b).

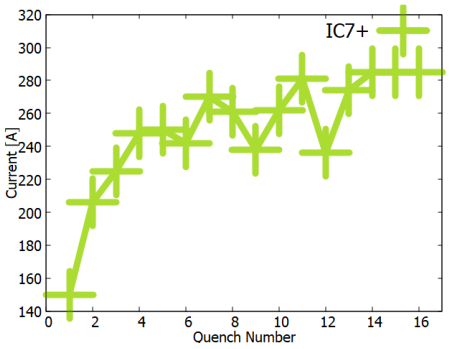
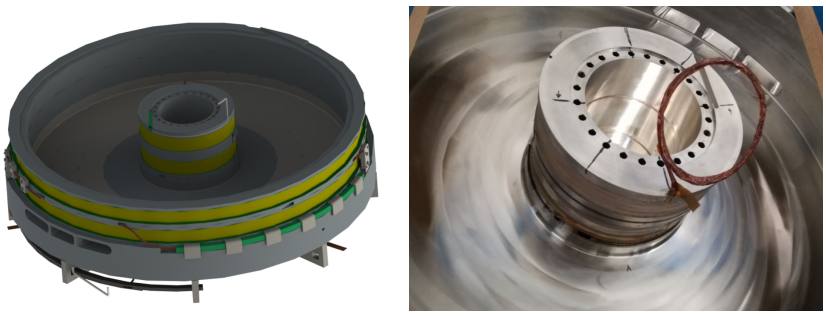


Figure 3.10: Quench history of the inner coil.



(a) (b)

Figure 3.11: PENeLOPE light with a diameter of 1 meter as a CAD image (a) and as a picture (b).

have been made to clarify this behavior of the system. At first, the magnetic field simulations done with the Opera tool have been checked by placing cryogenic Lake

Shore 3D hall sensors at different positions around the coils and comparing the measurements with the simulations. Table 3.1 shows the results and clearly both values agree very well.

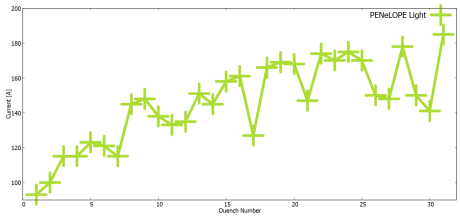


Figure 3.12: Quench history of PENeLOPE Light

Another suspicion was that one or more coil(s) in the system is/are somewhat damaged and degrade(s) the performance of the whole system. In order to check this, the voltage curves of each quench were analyzed and the quenching coil pair was determined. Table 3.2 lists the amount of quenches per responsible coil pair. It can be seen that the quenching source varies quite a lot and no pair can be properly identified as being damaged or primarily responsible for the quenches. Since after thirty one quenches only a current of $185\ A$ was reached, calculations have been made on which storage potential will still serve the precision goal of PENeLOPE within a feasible time and effort. The minimum current was determined by [44] to $180\ A$. Due to the fact that this current was already reached and the trend line of the quench training is still rising it was decided to continue the building of PENeLOPE and to stop the training session of PENeLOPE Light. Moreover all further training would just have been time and resource consuming and nevertheless been lost again after welding the whole system.

Current [A]	**Field Measured [mT]**	**Field Simulated [mT]**
0	0.01	0.00
50	56.50	55.00
75	82.50	83.00
100	115.00	110.00
0	0.012	0.00
50	−412.00	−411.00
75	−615.00	−617.00
100	−830.00	−822.50
0	0.01	0.00
50	−414.00	−411.00
75	−615.00	−617.00
100	−823.00	−822.50

Table 3.1: Measured and simulated magnetic field at three different sensor positions within the PENeLOPE Light system.

Responsible Coil Pair	**Amount of Quenches**
BC1/3	7
BC2/4	6
IC5/10	9
OC22/16	8

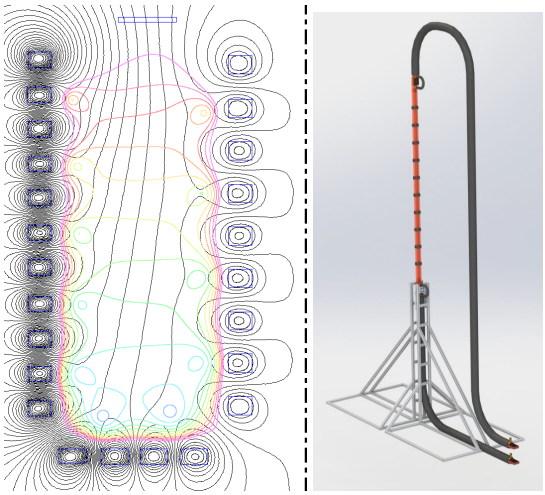
Table 3.2: Lits of coil pairs producing the different quenches in the PENeLOPE Light system (8 coils in total).

Chapter 4

Central Coil

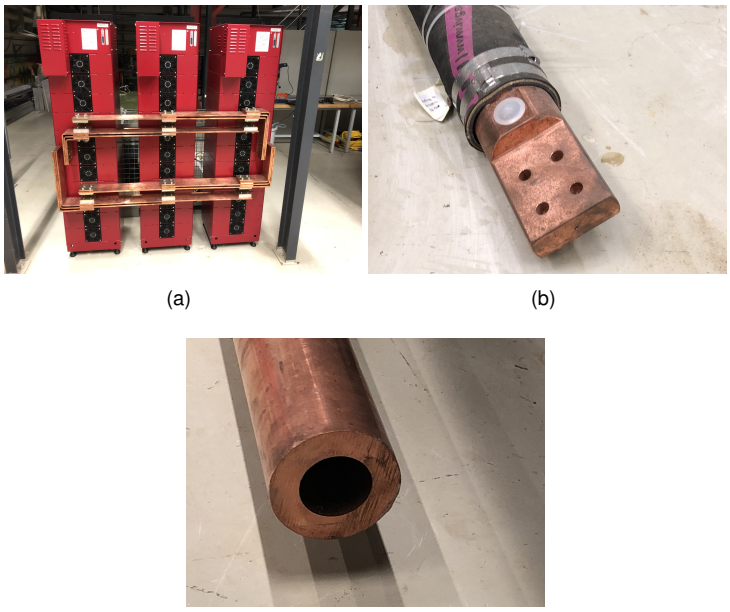
The magneto-gravitational trap mentioned in chapter 3 forms a storage volume with a potential barrier of 115 neV. One half of the trap with the equipotential lines of the storage potential is shown in fig. 4.1. The small closed circles within the volume point to areas where the magnetic field is vanishing. As mentioned in chapter 2 zero field areas can lead to undesired spin flips of the pre-polarized low-field-seeking neutrons into high-field-seeking ones. The latter will then disturb the lifetime measurement with systematic errors [45]. In order to overcome this problem, a central conductor is inserted into the warm bore in the center of PENeLOPE which will overlay the trapping potential with an azimuthal field around the central symmetry axis of the trap. According to [45] a field of at least 5 mT is necessary to maintain the spin orientation of the UCN - with a single central conductor this equals a current of at least 12500 A. In fig. 4.1 the central coil and symmetry axis is indicated by the dashed line. The central coil consists of a copper tube with a diameter of eight centimeters and a wall thickness of two centimeters, cooled with water flowing through the inside of the tube. A CAD image of the set up can be found in fig. 4.1 where water-cooled cables from Druseidt can be seen on the bottom and top side of the conductor. To separate the conductor from the PENeLOPE vacuum tank, small plastic spacers have to be mounted on the bare conductor tube. A stack of three 5000 A power supplies from RGB Heytekker with a total current of 15000 A at a maximal voltage of 10 V is used as a power supply. An image of the power supply, the conductor and the cable can be found in fig. 4.2.

In order to verify the design of the central coil, several simulations have been made for different currents and different water flows with the Solidworks Flow Simulation tool. Fig. 4.3 and 4.4 show the results of the simulations with a current of 15000 A and a water flow of 0.25 kg/s. The simulation goal was set to a saturating maximum temperature of the solid. It can be seen in the figures that the conductor itself and the mating for the cables at each end of the conductor will not increase beyond a temperature of 305 K. The starting temperature of the conductor and the cooling water was 293.5 K, so it merely increased by roughly 12 K.



(a) (b)

Figure 4.1: (a) Magnetic field lines in an axially symmetric cut of the storage volume of PENeLOPE. The 115 neV potential line is the most outer closed line (pink). (b) CAD image of the central conductor in its stand and connected to water-cooled cables.



(a) (b)

(c)

Figure 4.2: (a) Image of the power supply system of the central coil (Height of 1.8 meters). (b) Image of the mating of the Druseidt water-cooled cable. (c) Image of the central conductor before the assembly (diameter of 8 cm).

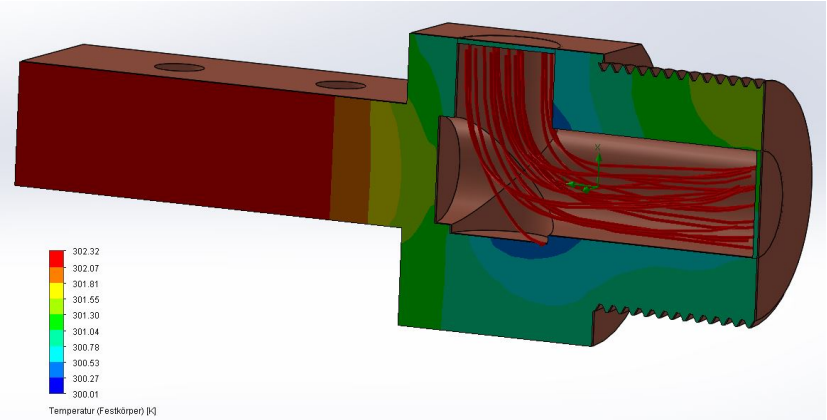


Figure 4.3: Maximum temperature in the mating adapter at 15000 A and a water flow of 0.25 kg/s.

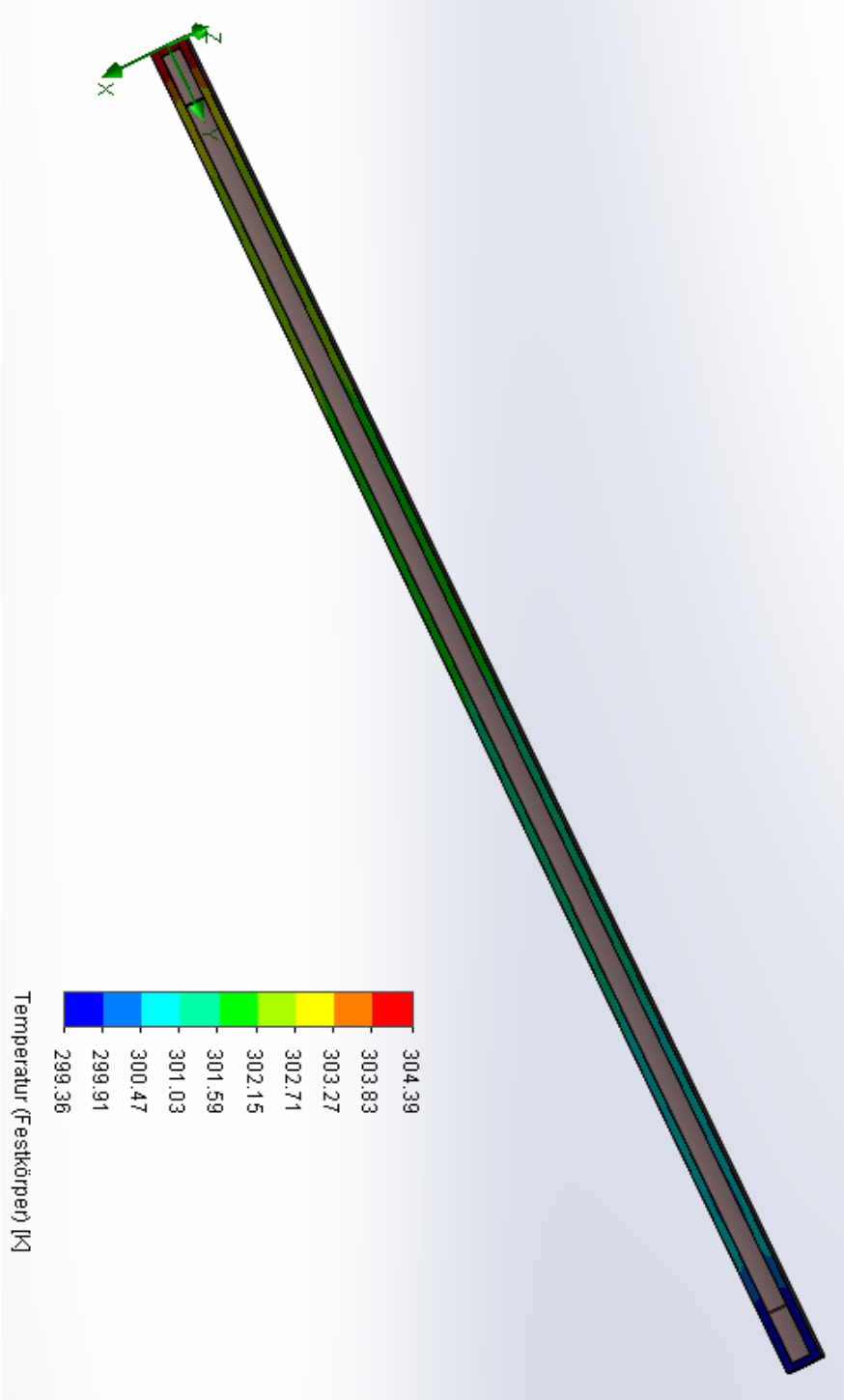


Figure 4.4: Maximum temperature in the conductor at 15000 A and a water flow of 0.25 kg/s.

Chapter 5

Absorber

When the superconducting coils of the experiment are ramped up to the nominal current, the low-field-seekers and the high-field-seekers are separated by their different properties in an outer magnetic field. The distribution of the LFS and HFS after ramping is shown in fig. 5.1. As already mentioned in previous chapters the HFS can introduce systematic errors to the neutron lifetime measurement and therefore have to be removed.

For PENeLOPE, it was decided to build an inner and outer neutron absorbing ring which can be lowered into the trap. Due to the design of the trap, there are several tight constraints on the design of such an absorber mechanism. First of all, the system is operating in a high magnetic field and an ultra-high vacuum area. Furthermore the system has to withstand a large temperature gradient from 4 K in the inside of the experiment to room temperature. Additionally, the space between the walls and the storage potential is only in the millimeter regime and only 5 mm in the most narrow spot.

A CAD image of the absorber and the necessary components can be found in fig. 5.2. The set-up consists of six linear servo drives from Bosch Rexroth with a very precise positioning in the micrometer range, six bellow feedthroughs which hold the rods for the absorber rings and the inner and outer absorber rings themselves [45]. The servo drives are all connected via the EtherCAT protocol to the experiment control described in chapter 7. Due to the very tight space constraints the rings of the absorber are made of a light weight plastic honeycomb structure where a neutron absorbing foil is wrapped around. In addition to the high-field-seeker cleaning, the absorber could also be used as a spectrum shaper when the absorber is lowered into the trap during the filling procedure and by this cuts off neutron energies above a certain level.

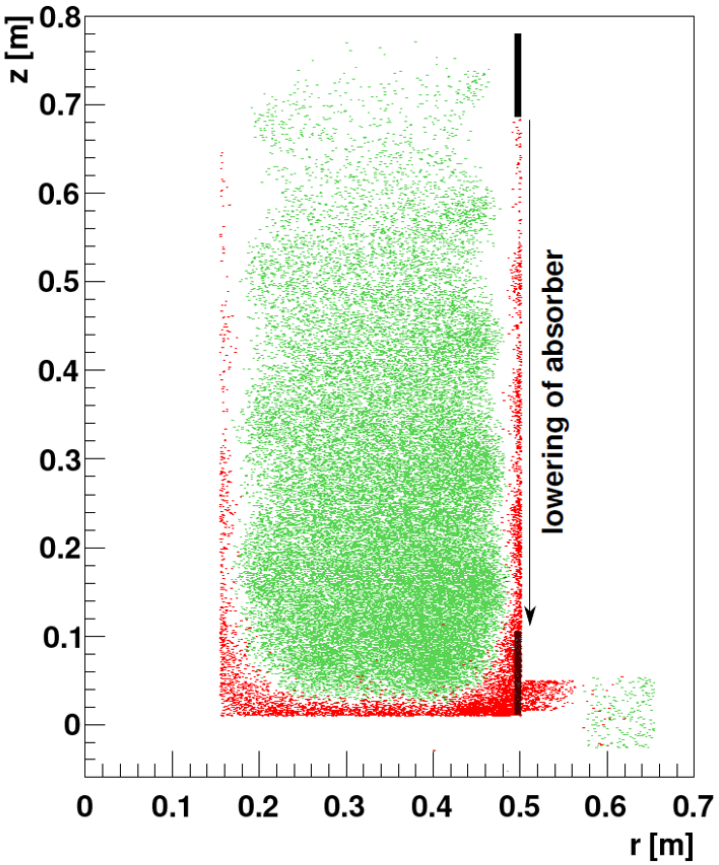


Figure 5.1: Distribution of LFS (green) and HFS (red) in the magneto-gravitational trap of PENeLOPE.

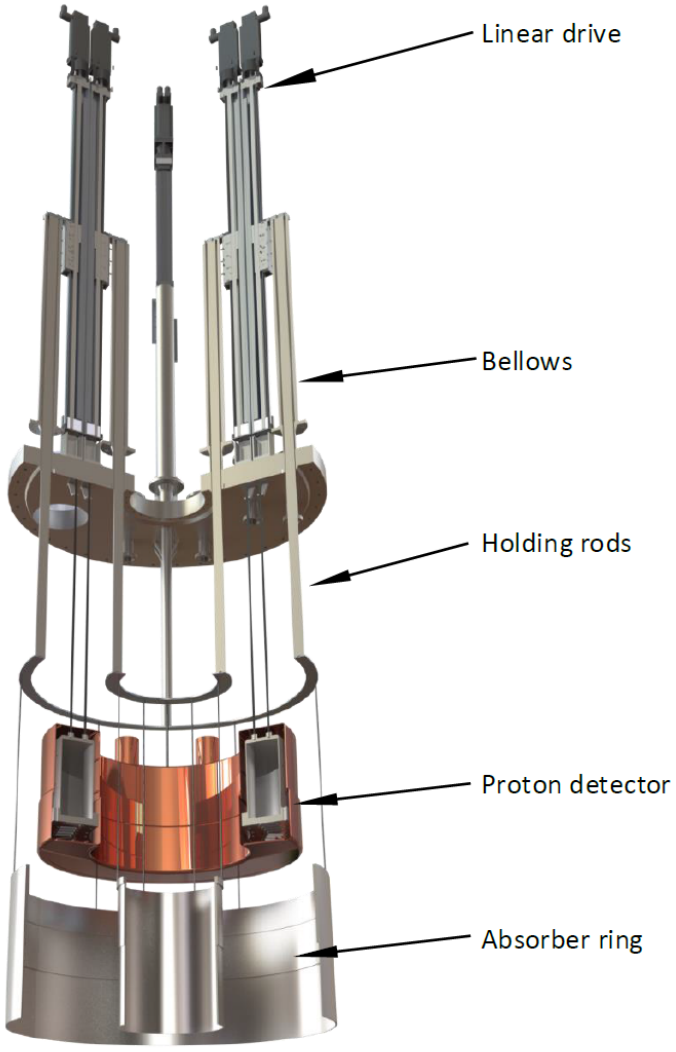


Figure 5.2: CAD image of the neutron absorber of PENeLOPE.

Chapter 6

Proton Detector

Within the PENeLOPE experiment the proton detector is another challenging part due to environmental conditions. The key facts of the proton detector are listed below.

- Electrostatic potential of -30 kV
- Detector temperature 77 K
- Electronics at room temperature within a tank in the cryostat
- Cryostat at 4 K
- Large magnetic field of 0.6 T
- Total of 700 events/s
- Sensitive area of $0.23\ \mathrm{m}^2$
- 1344 large area avalanche photodiodes (LAAPDs)

There have been several studies on the proton detector architecture and the detector which shall be used. [35] evaluated the use of caesium iodid crystals or plastic as scintillators, [35] evaluated micro-channel-plates and finally [54] tested LAAPDs for the proton detection. A crucial trade off led to the decision to use the LAAPDs for the PENeLOPE readout due to signal quality, easiness of the setup and cost. The following sections will describe the architecture and electronics of the final detector concept.

6.1 Detector Architecture

Figure 6.1 shows the data acquisition architecture of the proton detector. The upcoming section will, in detail, describe the data flow and each component from the left to the right. As mentioned in the previous section, the detector consists of 1344 APDs grouped in clusters of 24. Four of these clusters are connected to one bias

supply board where the bias voltage of the APDs and the signal path are separated. Signals will further proceed into the preamplifier and shaper boards where they are processed and digitized. Four of these chains are connected to one Signal Detection Unit (SDU) capable of handling 96 channels. 14 of these SDUs are placed within the cryostat on the high electrostatic potential and are connected via optical fibers to the multiplexer board called Network Access Controller (NAC). The NAC is placed outside of PENeLOPE and is galvanically isolated via optical links from the inside of the cryostat. Finally, the NAC is connected on the one side to the programmable logic controller (PLC) for slow control and monitoring and on the other side to the DAQ PC storing the events recorded.

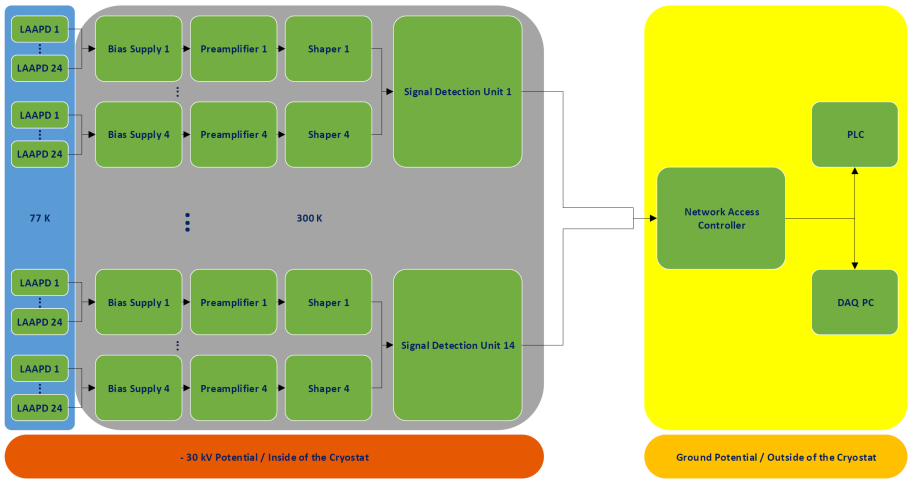
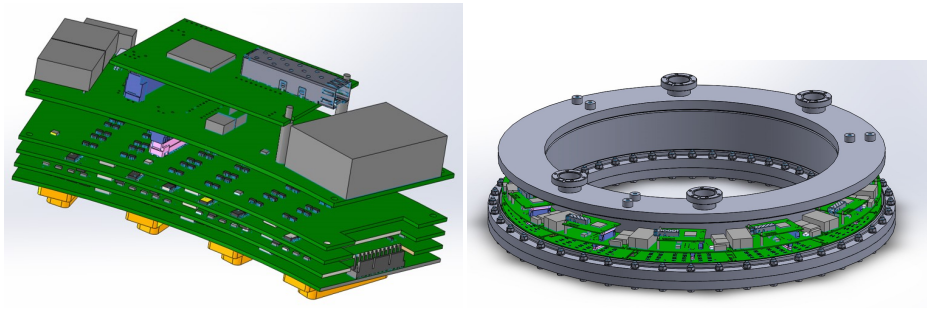


Figure 6.1: DAQ architecture of the proton detector of PENeLOPE

The different potential and temperature zones are symbolized with different colors in figure 6.1. Shaded with the blue color is the $77\ K$ zone of the APDs followed by the greyish zone of room temperature within the detector tank and the yellow zone of room temperature outside of the cryostat. In the bottom part of the figure the red bar shows all components on the $-30\ kV$ electrostatic potential and inside the cryostat and the orange bar shows the components on the ground potential and outside of the cryostat. Figure 6.2 shows a CAD model of one read-out stack for 96 channels and a CAD model of the 14 SDUs placed within the detector tank. On the top side of the tank six threads are placed which hold ceramic rods in order to mount the tank to the PENeLOPE cryostat. Furthermore, there are four CF40 feedthroughs to hold all optical fibers, the high voltage connection and the air flow inlet and outlet. Also, these feedthroughs will be ceramically isolated. A picture of the delivered tank can be found in 6.3.

6.2 Large Area Avalanche Photodiodes

For each of the detector channels one Hamamatsu S11048 LAAPD [22] will be used. Each of the LAAPDs consists of several doped layers of silicon. Figure 6.4



(a) (b)

Figure 6.2: (a) CAD model of a read-out stack of 96 channels. It is 15 x 8 x 8 cm in size. (b) CAD model of the detector tank with one meter in diameter and the read-out stacks inside.

Figure 6.3: Picture of the detector tank with a diameter of about one meter (Since it will be stored for some more time the air tight foil was not broken).

shows the structure of such an APD. It consists of a highly p-doped layer covered by a slightly p-doped intrinsic layer, a p-doped layer and a highly n-doped layer. A reverse-biased APD will internally create a field shown in the right part of figure 6.4. If a photon or low-energy proton is impinging the intrinsic zone of the diode an electron-hole pair is generated. The hole will drift towards the strongly p-doped zone, whereas the electron drifts towards the multiplication zone. When reaching this zone the electron is accelerated and generates more electron-hole pairs. This

avalanche of electron-hole pairs and the resulting jump in the photo current will stop when the last hole reached the highly p-doped area. Depending on the bias voltage of the APD, the signal on the photo current of the same photon/particle can be larger or smaller - this is called the gain of an APD. The gain M can be calculated via

$$M = \frac{1}{1 - \left(\frac{U_B - U_L}{U_D}\right)^m} \tag{6.1}$$

and depends on the bias voltage U_B, the breakdown voltage U_D, the loss voltage over the series resistance of the APD U_L and a characteristic factor m depending on the internal structure and material of the APD [22]. The current within the APD depends on the signal current, noise current and the gain. It can be written as

$$I_{APD} = (I_{Signal} + I_{Noise}) \cdot M \tag{6.2}$$

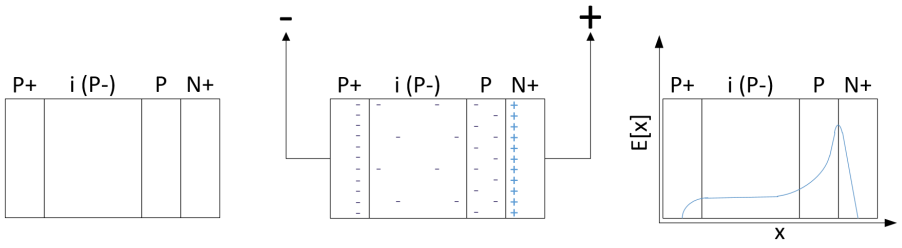


Figure 6.4: Structure of the APD in non biased (left), biased (right) mode and the resulting field strength inside of the APD when reverse-biased. Effective positive charges are marked with a blue plus and effective negative charges with a green minus.

Characteristic for all photodiodes is the temperature dependence of the noise on the photo current. The quadratic mean of the thermal noise can be formulated according to Nykvist as

$$\overline{I_{therm}^2} = \frac{4k_B T}{R} B \tag{6.3}$$

where T is the temperature, B the bandwidth and R the resistance of the APD. Additionally to the thermal noise there is the shot noise which depends on the background current I_B, the mean photo current $\overline{I}_{ph}$, the dark current I_D, the bandwidth B and the mean square of the gain $\overline{M^2} \approx M^2 M^x$ [24]. In the approximation of $\overline{M^2}$ x is a characteristic factor for the material used. For silicon it is 0.2 to 0.5. The shot noise can be formulated as

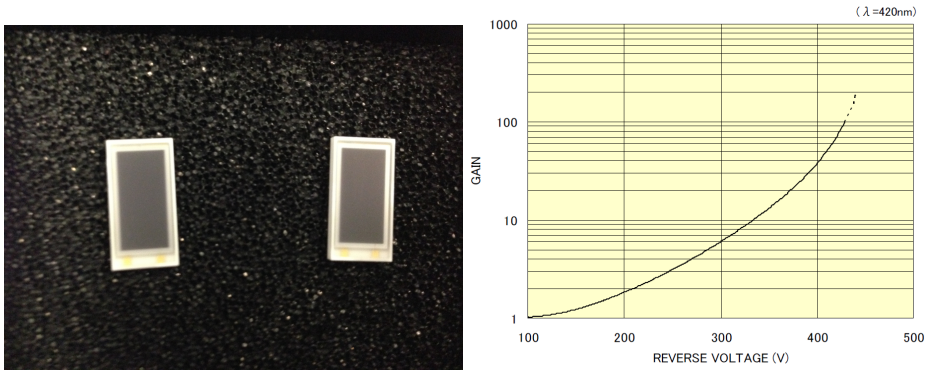
$$\overline{I_{shot}^2} = 2e\Big(|\overline{I}_{ph}| + |I_B| + |I_D|\Big) \cdot B \cdot \overline{M^2} \tag{6.4}$$

and together with the thermal noise it gives the total noise of an APD according to

$$\overline{I^2_{noise}} = \overline{I^2_{shot}} + \overline{I^2_{therm}}. \tag{6.5}$$

Parameter	Conditions	Value
Bandwidth		320 to 1000 nm
Peak Sensitivity	M = 100	580 nm
Breakdown Voltage		420 V
Terminal Capacitance	M = 100	250 pF
Dark Current	M = 100	30 nA

Table 6.1: Key parameters of the S11048 LAAPD according to [22]



(a) (b)

Figure 6.5: (a) Picture of two S11048 LAAPDs with a size of 14.5 mm x 7.2 mm. (b) A typical gain versus bias voltage curve of the S11048 [22].

An key parameter for a effective signal resolution of the detector is the signal-to-noise ratio which is defined as

$$\frac{S}{N} = \frac{\overline{I^2_{signal}}}{\overline{I^2_{noise}}} = \frac{\overline{I^2_{signal}}}{\overline{I^2_{shot}} + \overline{I^2_{therm}}}. \tag{6.6}$$

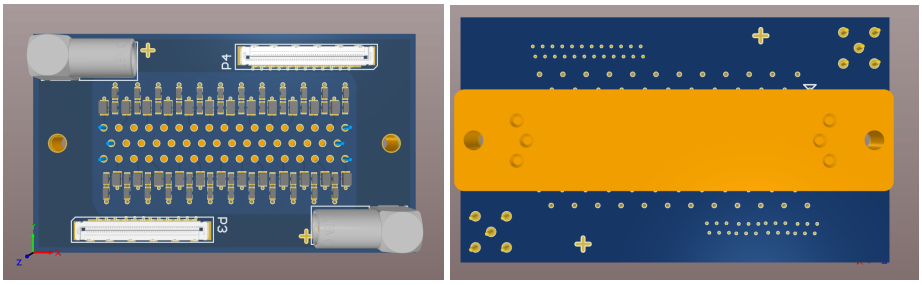
The key data of the Hamamatsu S11048 LAAPD used within PENeLOPE can be found in table 6.1, a picture of the APD and a typical gain versus voltage curve can be found in figure 6.5. In total, the S11048 has an active area of 14.0 mm x 6.8 mm. More details on measurements with the APD and the complete electronics can be found in 6.5.

6.3 Analog Electronics

In the analog electronics part, the signals from the APDs are decoupled from the high voltage, amplified, filtered and shaped. Finally, the signals are digitized. The following sections will describe the way of the signal throughout the electronics and all related printed circuit boards. Topology wise the design is based on the design of [11].

6.3.1 Bias Voltage Supply Board

The APDs in the detector are connected via twisted pair cables with the D-Sub connectors welded into the bottom of the detector tank (see figure 6.2). Figure 6.6 and 6.7 show pictures of the bias voltage supply board and the schematic. Via LEMO connectors the bias voltage is inserted and then coupled with the two 10 MOhm series resistors $R1$ and $R2$ to the APD. The capacitor $C1$ is discharged when a photon or low-energy proton hits the APD within a time constant of less than 91 ns, corresponding to a cut-off frequency of 11 MHz of the S11048 APD. Each of the D-Sub connectors can hold twenty-four APD connections and so can the bias voltage supply board. This, in turn, means that the bias voltage of the detector can be regulated in clusters of twenty-four channels.



(a) (b)

Figure 6.6: CAD model of top (a) and bottom (b) side of the bias voltage supply board. On the top side, the connectors to the following cards and the high voltage input via the LEMO connectors are visible. On the bottom side, the D-Sub connector can be seen which is plugged into the detector tank. The card is 3 x 8 cm in size.

6.3.2 Preamplifier Board

From the bias voltage supply board the signals are transferred via Molex 501083-5010 coaxial connectors and ribbon cable assemblies. The ground line of the pseudo-differential pair coming from the APD is connected via a zero Ohm resistor $R2$ to ground and the capacitor $C1$ in fig. 6.7 AC couples the output of the APD to the input stage of the preamplifier (see figure 6.8) consisting of a low-noise J-FET BF862 from NXP ($Q1$) and two over-voltage protection diodes CMLD4448

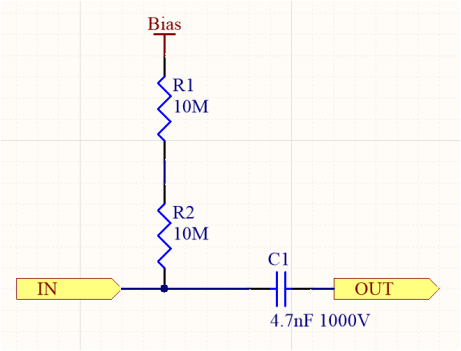


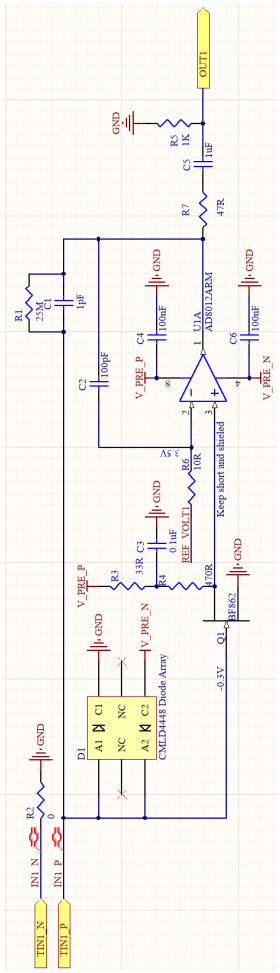
Figure 6.7: Schematic of the bias voltage supply board

from Central Semiconductor ($D1$). Together with an open drain resistor of 470 Ohm ($R4$) the circuit results in an AC gain of 14.

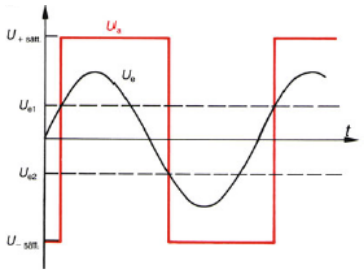
The amplified signal is then fed into the non-inverting input of an Analog Devices AD8012 current feedback amplifier ($U1$) which has an input bandwidth of 300 MHz and a gain of $G = +1$. Oscillations on the output stage of the amplifier are suppressed with the 100 pF ($C2$) feedback capacitor to the inverting input and the small 10 Ohm resistor ($R6$) at the input of the reference voltage setting, the trigger level of the amplifier output. With the design in figure 6.8 an inverting Schmitt-Trigger is implemented. The functional principle of such a trigger is shown in figure 6.8. It can be seen that the output of the amplifier is a rectangular pulse as long as the input signal is above or below the set threshold. The height of the output pulse equals the saturation voltage of the amplifier. Simply put, the voltage breakdown over the APD is transformed into a positive voltage pulse on the output of the preamplifier. For proper functionality, the output is DC coupled fed back to the input of the J-FET via the resistor $R1$ and the capacitor $C1$. Additionally, the output is AC coupled with a termination of 50 Ohm via the resistor $R7$ and the capacitor $C5$. The capacitor $C5$ and the resistor $R5$ form a high-pass filter which cuts of frequencies below the cut-off frequency determined by

$$f_{Cut-Off} = \frac{1}{2\pi R_5 C_5}. \tag{6.7}$$

In the schematic shown in figure 6.8 the threshold for the frequency is 159.15 Hz. One preamplifier PCB shown in figure 6.9 has a size of 123 mm times 196 mm and can handle four bias voltage supply boards and, as a consequence, 96 detector channels in total. Due to the small space and the ring shape of the detector and detector tank, respectively, the PCB is curved with a mean radius of 330 mm. The amplifiers need a negative and positive supply voltage of about 6 V. Fine tuning of the supply voltages can be achieved with the voltage distribution card shown in section 6.4.1. In addition to the output signals of the amplifiers and the supply voltages, the board-to-board connectors FX11A-60P/6-SV(71) from Hirose to the shaper PCB hold a 1-Wire communication line which is used to read out the four DS18B20U Maxim Integrated temperature sensors.

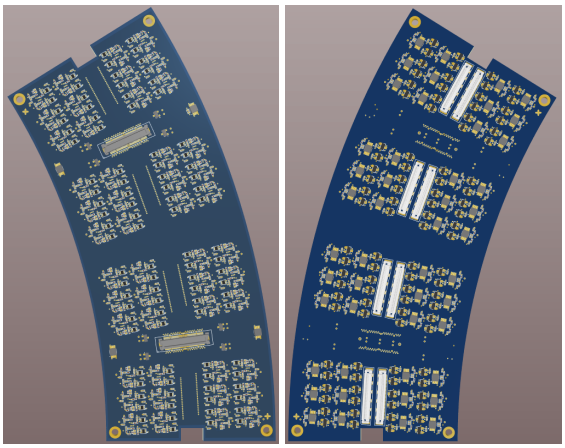


(a)



(b)

Figure 6.8: Schematic of the preamplifier board (a) and functionality of a Schmitt-Trigger (b)



(a) (b)

Figure 6.9: CAD model of top (a) and bottom (b) side of the preamplifier board. The size is 123 x 196 milimeter.

6.3.3 Shaper Board

The shaper board is divided into two parts. In the first part the analog signal from the preamplifier is shaped with a CR/RC shaper, described in this section and the latter part is the conversion of the analog waveform into a digitized form described in section 6.3.4. Signals from the preamplifier enter the PCB via two Hirose FX11A-60S/6-SV(71) board-to-board connectors and AC couple to the input of the shaper. As can be seen from figure 6.10, there is a high-pass filter at the input section with a cut-off frequency of $\approx 33\ kHz$ formed by $C6/C9 = 1$ nF and $R3/R13 = 4.7$ kOhm. Together with the high-pass filter the amplifier $U1A/D$ and the feedback resistors and capacitors surrounding it act as a differentiator circuit, transferring the negative pulse from the preamplifier into a positive rising edge on the output. This rising edge is DC coupled into the RC integrator part of the shaper. The capacitors $C5/C13 = 1$ nF and resistors $R9/R11 = 4.7$ kOhm act as a low-pass filter for frequencies below ≈ 68 kHz. With $U1B/C$ and the feedback resistors and capacitors an integrator circuit is formed which transfers the tail of the differentiator output into the characteristic output form of the CR/RC shaper shown in figure 6.11. As an amplifier, the AD8024 from Analog Devices is used. The output of each amplifier going to the ADC is terminated with a 50 Ohm resistor ($R10/R12$,) matching the input impedance of the ADC.

6.3.4 Analog-To-Digital Converter Board

In order to process the signals of low-energy protons further in the DAQ chain, the shapes have to be sampled and digitized. This is the task of an analog-to-digital converter (ADC). The ADC type used within PENeLOPE is the successive-approximation register ADC (SAR-ADC). A typical SAR-ADC consists of a clock

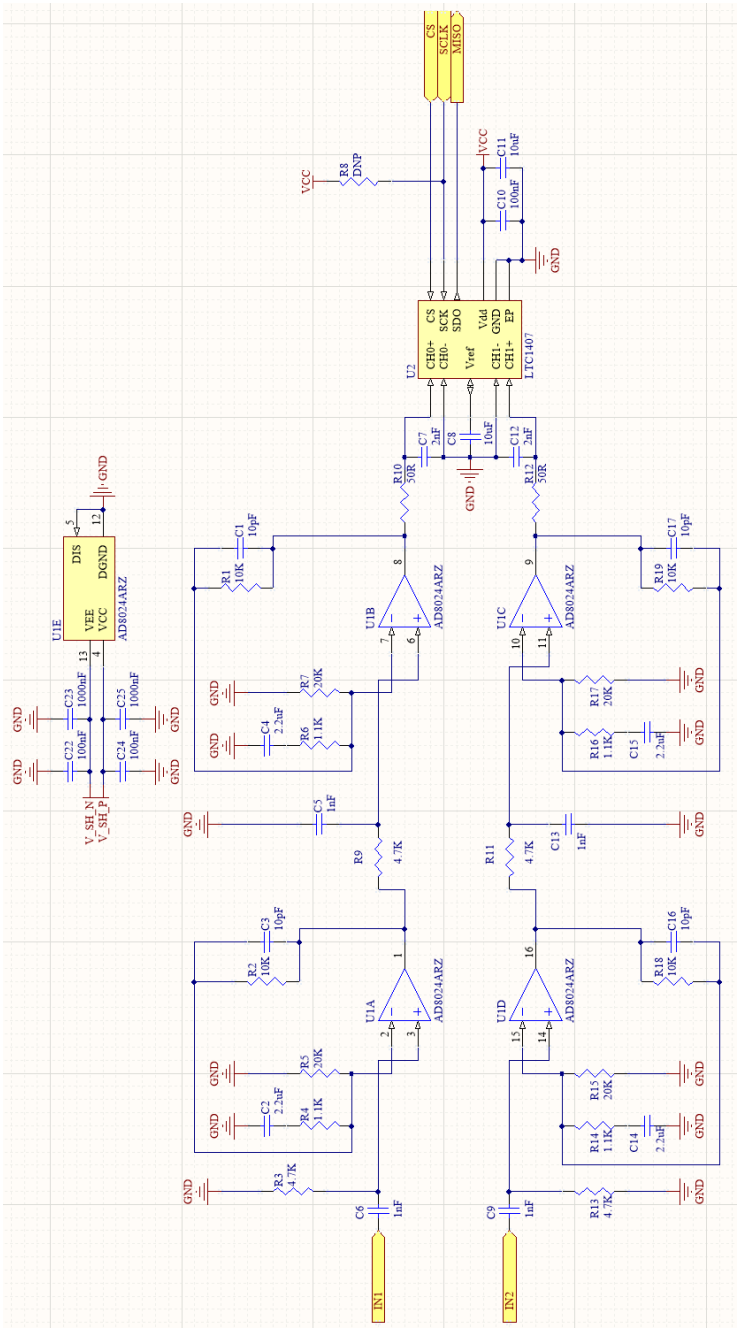


Figure 6.10: Schematic of the shaper and ADC board

and an enable signal which activates the conversion. In order to start a conversion the enable signal has to be pulled to logic zero. Additionally, the ADC contains a counter, a decoder, a successive approximation register (SAR), a digital to analogue converter and a comparator. The conversion in the ADC starts with the most

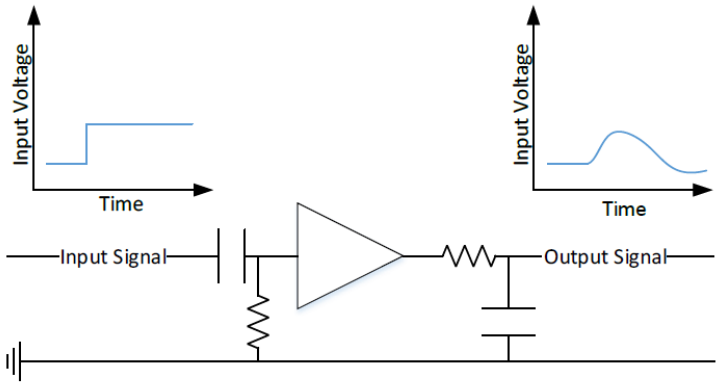


Figure 6.11: CR/RC shaper with a pulsed input

significant bit (MSB) and activates it in the SAR. Afterwards, the comparator will compare the input voltage with the numeric representation of the MSB (e.g. 128 for the 8th bit of an 8-bit ADC). If the input voltage is above this value the combinatorial logic will leave the logic one set in the SAR, if not it will be turned to logic zero again. The procedure described above will take one clock cycle and is repeated for each SAR bit until the least significant bit (LSB) is reached. The overall conversion time of the ADC is the number of bits times the clock period. For an 8-bit SAR-ADC the typical approximation evolution is shown in fig. 6.12.

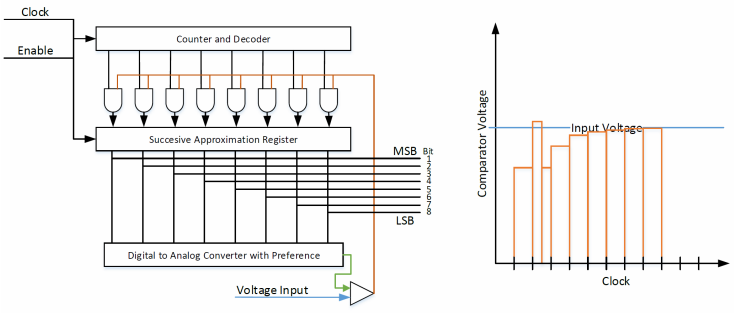


Figure 6.12: Scheme of a typical SAR-ADC (left) and an example of the iterative principle of the SAR-ADC (right)

The LTC 1407 form Analog Devices is a 3 MSPS dual input SAR-ADC with a resolution of 12 bit, perfectly suitable to sample the pulses from the analog electronics shown in figure 6.13. The length of the signal is in the region of $50\ \mu S$ (taking the signal itself and some time before and after the signal) equaling a frequency of roughly 20 kHz which easily fulfills the Nyquist-Shannon theorem, stating that the sampling frequency must be at least twice as big as the signal frequency. After digitization, the samples can be read out via a three wire serial interface shown in figure 6.14. A read out cycle is started with a running serial clock and a one clock cycle long pulse on the conversion signal. Afterwards, the LTC1407 will start

converting and stream out the twelve bit data word of the first channel followed by the second channel data word. The whole procedure takes at least thirty-four clock cycles.

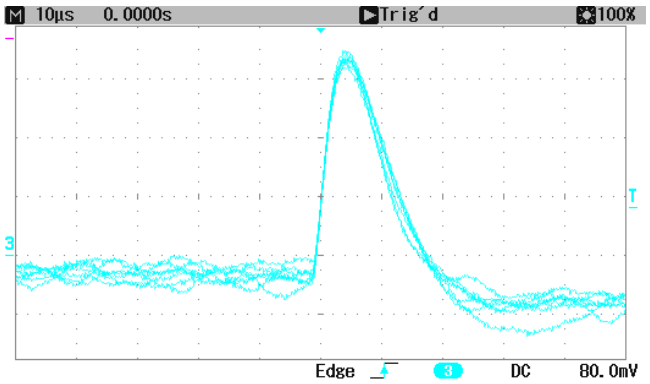


Figure 6.13: Signal shape after the analog electronics taken with a oscilloscope

Figure 6.15 shows the combined shaper and ADC card from the top and bottom side. Just like the preamplifier the PCB is curved with a mean radius of 330 mm and a size of 123 mm x 196 mm. The amplifiers of the shaper need a negative and positive supply voltage of about 7 V and the ADCs a positive supply voltage of 3.3 V. Fine tuning of the supply voltages for the amplifiers can be achieved with the voltage distribution card shown in section 6.4.1. Two fan-out chips for the conversion and the serial clock signal are also placed on the PCB. IDT8343-01 1:12 fan-outs from Integrated Device Technology are used. For temperature monitoring seven DS18B20U 1-Wire temperature sensors from Maxim Integrated are used. All interface signals from and towards the voltage distribution card use the FX23-120P-0.5SV20 board-to-board connector from Hirose.

6.4 Digital Electronics

In the digital section of the proton detector electronics all necessary voltages are created, the data from the detector is read out and the signals are processed, data is streamed out onto the DAQ PCB and the connection to the slow control is established. The following section will describe all necessary components for this in detail.

6.4.1 Voltage Distribution Board

The voltage distribution board generates all necessary voltages for the APDs, preamplifier, shaper, ADC and SDU from a single 15 V input supplied via a WAGO 734-136 connector. In a first step, three DCDC converters from Traco are used to generate 3.3 V (THN20-1210) for on-board logic and for the ADCs, 5.0 V (THN20-1211) for on-board logic and the SDU described in section 6.4.2 and ± 12.0 V

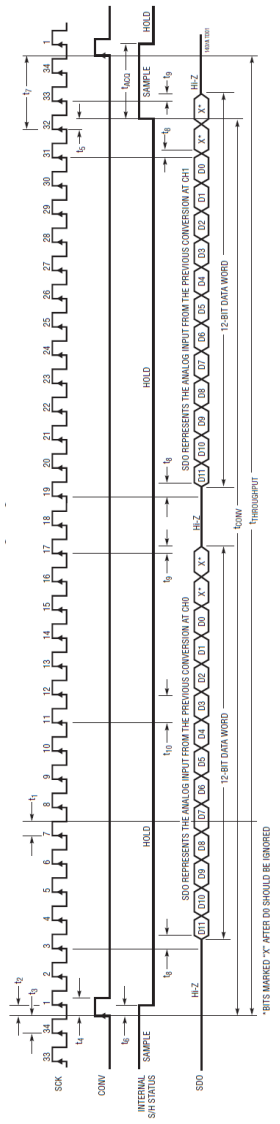
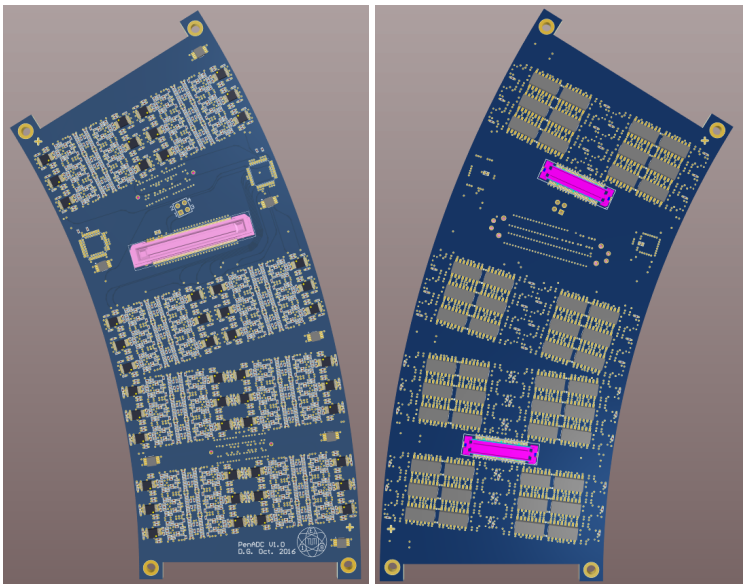


Figure 6.14: Timing diagram of the three wire interface of the LTC1407 [53]

(THL10-1222) for the generation of the amplifier voltages. The schematic circuit for the shaper and preamplifier voltages is similar and is, as an example, shown for the shaper in figure 6.16. From the ± 12.0 V the two converters LT3015 and LT3083 from Analog Devices generate the ± 6.0 V supply voltages for the shaper and preamplifier, respectively. With the help of the jumpers $P9$ and $P10$ the user can choose between manual potentiometers connected to $P11$ and $P12$ or the digital potentiometers $U16$ and $U17$ to be connected to the sense/set pins of the converters. These pins control the output level of the converters and, by this, the supply voltages for the shaper and preamplifier. The digital potentiometers can be controlled via an I2C connection from the SDU.



(a) (b)

Figure 6.15: Picture of top (a) and bottom (b) side of the shaper and ADC board. The size is 123 x 196 milimeter.

Figure 6.17 shows the bias voltage generation circuit. The Laser Components ABC550-04 series is used as a converter generating the necessary output voltages in the range of several hundred volts from a 15 V input. Via the two digital-to-analog converters (DAC) $U1$ and $U24$ the gain control and the output voltage control of the ABC550-04 can be regulated. The DACs are adjusted via an I2C line controlled by the SDU. Through the LEMO output connector $P3$, the bias voltage is transferred to the bias voltage supply card.

Just like the previous cards, the voltage distribution card has a curved shape with a mean radius of 330 mm and a size of 123 mm x 196 mm. All signals from the ADCs are just wired through to the board-to-board connector FX23-120P-0.5SV20 from Hirose, connecting the voltage distribution card with the signal detection unit described in section 6.4.2.

6.4.2 Signal Detection Unit

One signal detection unit (SDU) consists of a Xilinx Kintex 7 FPGA, a high-speed optical transceiver, several temperature monitoring DS18B20U 1-Wire temperature sensors from Maxim Integrated, general purpose I/Os (GPIOs), jumpers for the FPGA configuration and a serial NOR flash memory from Micron. The FPGA reads out the attached ADCs via a three wire serial communication link consisting of a 50 MHz serial clock (SCLK), a conversion signal (CS) from the FPGA to the ADCs and 48 Master-In-Slave-Out (MISO) links from the ADCs to the FPGA. Additionally, there are several more control lines going from the FPGA via the Hirose FX23-

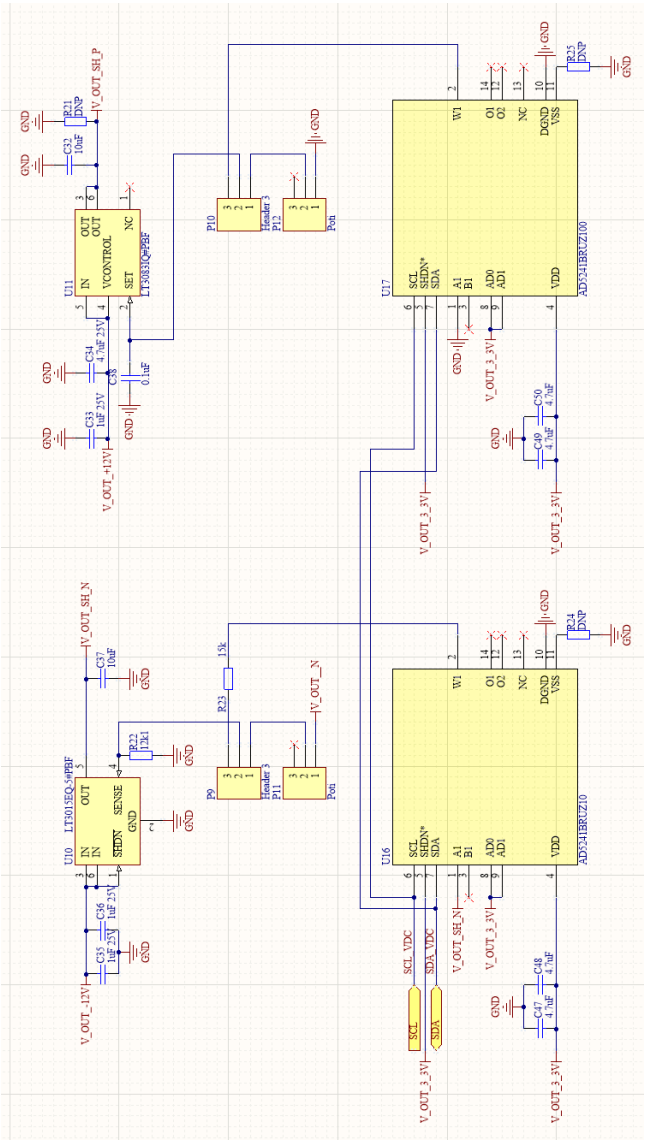


Figure 6.16: Schematic of the shaper voltage generation.

120S-0.5SV20 down to the voltage distribution card and from there further down in the read out chain. These links include one I2C line for the control of the adjustable voltages on the voltage distribution card and three 1-Wire links reading out the temperature sensors on the underlying cards. Furthermore, the SDU can either be powered via the Hirose connector from the voltage distribution card or it can be externally powered via a three pin pin-header connector on top of the card. A picture of the top and bottom side of the card can be found in 6.18. The dimensions of the PCB are 68 mm x 91 mm. Overall, there are 14 SDUs inside of the detector tank handling 96 channels each. All SDUs are connected via a point-to-point optical connection to the Network Access Controller described in section 6.4.3.

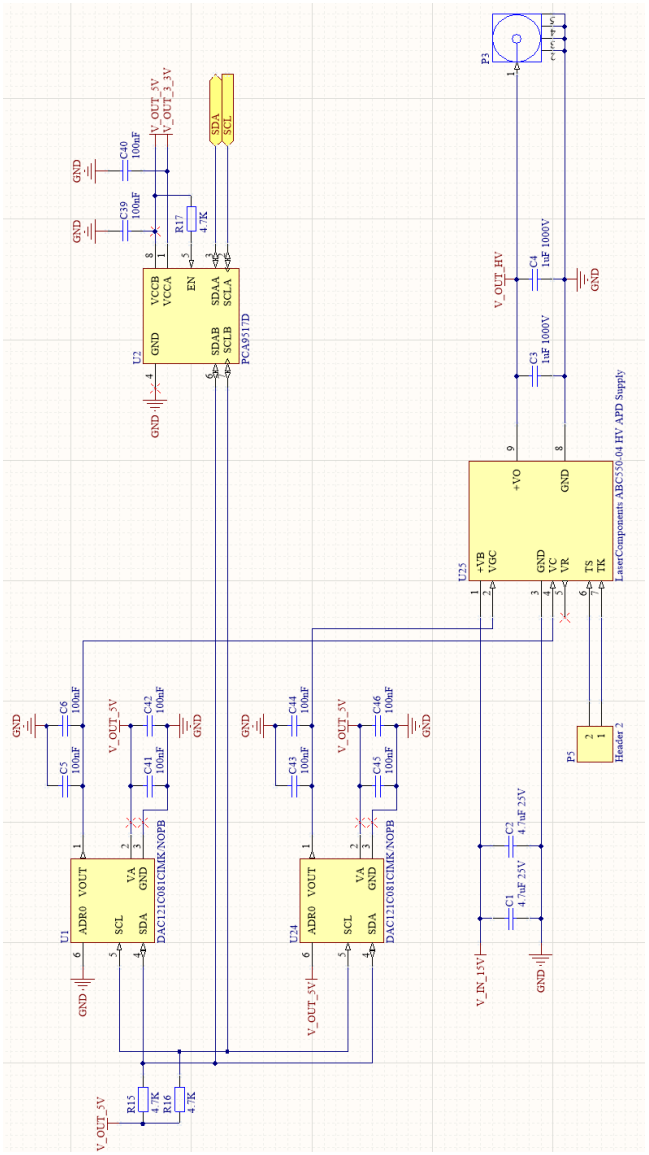
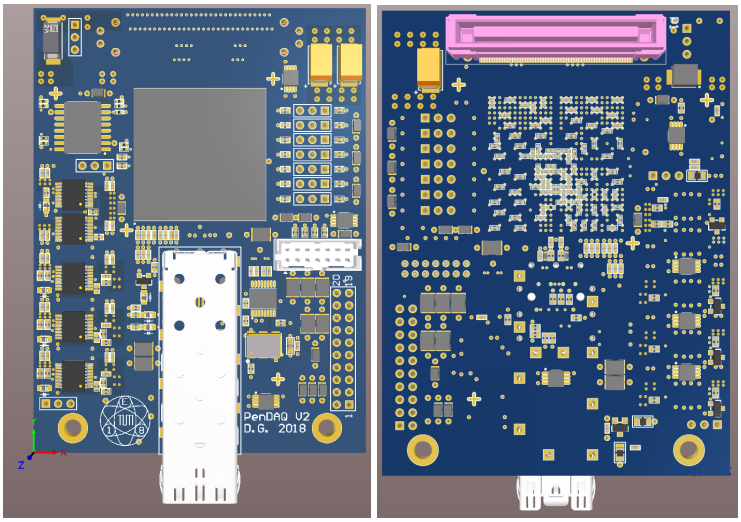


Figure 6.17: Schematic of the bias voltage generation.

Firmware Functionality

A functional diagram of the SDU firmware with the different clock domains used can be found in 6.19. In the lower part of the picture, in the 50 MHz clock domain, the module ”ADC SPI Master” generates the serial clock and the conversion signal that triggers the read out of the ADC. Via the MISO lines and the decouple FIFOs the data is transferred from the 50 MHz to the 100 MHz clock domain used for the signal processing. If no detector is attached, the ADC emulator can be used to simulate the presence of the ADC. Each channel can have its own emulator. The



(a) (b)

Figure 6.18: CAD model of top (a) and bottom (b) side of the signal detection unit. The size is 68 x 91 milimeter.

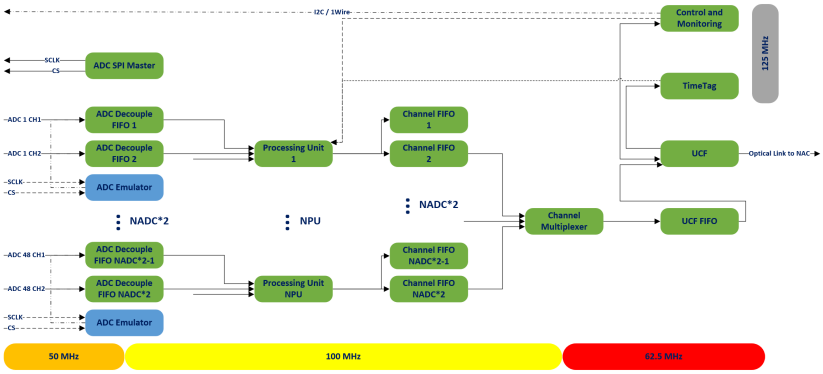


Figure 6.19: Functional diagram of the SDU

amount of ADCs attached to the SDU can be set by the constant NADC which is exactly half the amount of channels attached to the SDU. In PENeLOPEs standard case NADC equals 48. After the decouple FIFOs the data stream is split onto an adjustable amount (NPU) of processing units (PU). Every processing unit handles the channels attached to it in a multi-threading manner. This means that during every clock cycle one sample of another channel is handled by the processing unit described in the next section. Effectively, the channels share the processing logic and by this FPGA resources are saved. The amount of processing units is a trade off between FPGA logic resources on the one side and FIFO capacity and event rate on the other side. In the case of PENeLOPE there are 12 processing units, each handling eight channels. After being processed and packed into frames in the PUs the data frames are stored in channel FIFOs. The channel multiplexer

then scans these FIFOs in a round-robin manner and stores the frames serially in the UCF FIFO and by this makes the transition between the 100 MHz to the 62.5 MHz clock domain. The central communication hub within the SDU is the UCF described in detail in chapter 13. Next to the data channel the UCF also provides one communication channel for the time tag module which synchronizes all SDUs and the NAC. Moreover, the control and monitoring block within the firmware also has a dedicated communication channel. Via the latter module the temperature read out of all boards in one stack is controlled and the voltages of the preamplifier and shaper can be regulated. Furthermore, there are configuration registers for the PU that are described in the next section.

Processing Unit

The processing unit incorporates the actual signal detection and frame generation as can be seen in figure 6.20. It is based on the work of [18]. In a first step, after booting, the PU samples an adjustable amount of samples $N_{Samples}$ and calculates the pedestal. After this initial step the new pedestal value will further be calculated via

$$P_{New} = \frac{P_{Sum} - P_{Old} + S_{New}}{N_{Samples}} \tag{6.8}$$

with P_{Sum} being the old sum over $N_{Samples}$, P_{Old} the old pedestal value and S_{New} the new sample from the ADC. The pedestal is continuously calculated for each detector channel separately and, by this, automatically floats with the background which will be important for the actual signal detection later on. In addition to the pedestal, the module pedestal calculation will also determine the mean quadratic deviation σ^2 of the samples by the equation

$$\sigma^2 = \frac{\sigma_{Sum} - \sigma^2_{Old} + (S_{New} - P)^2}{N_{Samples}} \tag{6.9}$$

with σ_{Sum} being the sum over $N_{Samples}$ of σ^2, σ^2_{Old} being the old sample and P the current pedestal.

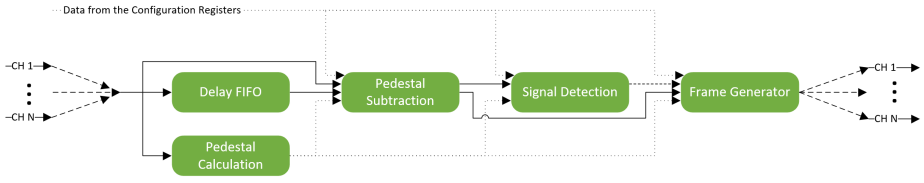


Figure 6.20: Functional diagram of the PU

Additionally to the pedestal calculation the data stream is further split into two parts. The first one is bypassing the delay module and directly enters the pedestal subtraction module in order to remove the baseline offset of the signal. This stream is

then used to perform the actual signal detection. The second one enters the delay module which produces an adjustable delay of N_{delay} samples on the signal. This stream is then entering the pedestal subtraction and further the frame generation. Figure 6.21 shows the principle of the signal detection of PENeLOPE. Marked with the red dotted line is the calculated pedestal of the signal and the orange dashed lines are marking the quadratic deviation of the pedestal. An event will be triggered if an adjustable number of consecutive samples is above the threshold shown in green which is determined by an integer multiple of the mean quadratic deviation plus the pedestal. Defining the signal detection in such a way can guarantee a deterministic and fixed signal-to-noise ratio. If the signal detection triggers an event the pedestal calculation is paused for the duration of the event since otherwise one would get a distortion and slow drift of the pedestal and mean quadratic deviation. Table 6.2 shows all parameters for the signal detection and what they are used for.

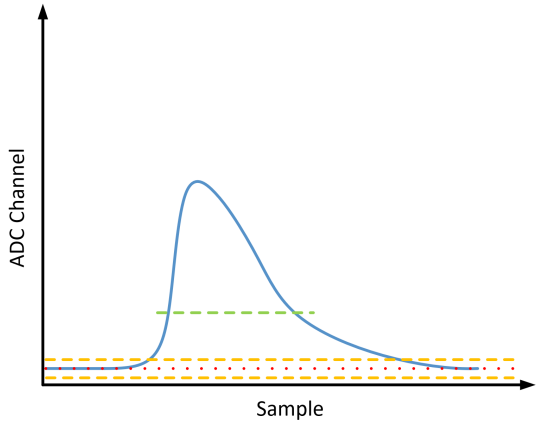


Figure 6.21: Signal detection of PENeLOPE

Parameter	Typical Value	Usage
iDelay	5	Defines the delay of the signal stream for the frame generation
iFactor	5	Defines the integer multiple of the σ^2 used for the signal detection
iNMBSamples	3	Defines the number of consecutive samples above the trigger threshold
iNMBSamplesFr	30	Defines the number of samples of the event used in the frame generator
iAveragePower	12	Defines the number of samples used for the pedestal and mean quadratic deviation calculation according to $N_{Samples} = 2^{iAveragePower}$

Table 6.2: User adjustable parameters of the signal detection

If the signal detection triggers an event the frame generator is started. Figure 6.22 shows the frame structure of the SDU. It starts with a 32-bit header full of zeros, followed by a 32-bit word consisting of the number of words in the frame -

this equals half the number of samples as can be seen from the figure 6.22 - the channel number and the pedestal value. This is followed by a word consisting of the mean quadratic deviation and the random/manual trigger flag. The last word in the header holds the time tag of the frame. In the main body of the frame always two samples are combined in one 32-bit word including four leading zeros in front of every sample. The frame is ended by a trailer full of ones. Purpose of the random or manual trigger is the test and calibration of the detector channels. With the help of the configuration registers each channel and ADC can be manually activated or deactivated. All parameters in table 6.2 can only be set globally for all channels of one SDU.

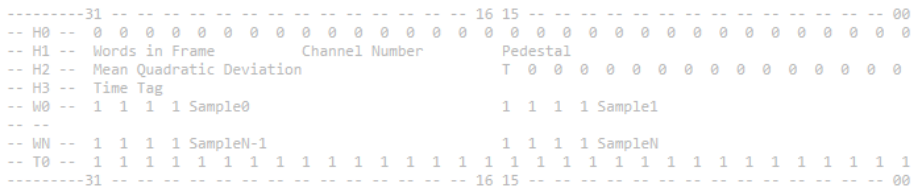


Figure 6.22: Frame structure of the signal detection

6.4.3 Network Access Controller

The network access controller (NAC) is the link between the front-end modules of the detector within the cryostat on the one side and the DAQ-PC and the PLC on the other side. Figure 6.23 shows the functional diagram of the NAC. It can be seen that there are 14 optical links coming from the different SDUs entering the UCF instantiations on the NAC. The three different communication channels used with every UCF master are the timing channel, the control channel and the data channel. Data coming from the detectors is streamed unidirectional out of the UCF into the data multiplexer with a frequency of 62.5 MHz. The purpose of this module is to serialize the data streams from all SDUs and forward them to the UDP preparation module that packs the data into UDP frames and stores them into a clock domain crossing FIFO. Finally, the UDP core reads the data from this FIFO with a 125 MHz clock and streams out the data on a normal gigabit Ethernet link to the DAQ-PC. Furthermore, the NAC incorporates the time tag module which generates the global clock to which all SDUs will synchronize. This module is also unidirectional connected to the UCF on the timing channel. The last communication channel on the UCF is the control one which is bidirectional connected to the control multiplexer which deserializes and serializes the control data received from the Beckhoff FB1111-0142 EtherCAT communication module. All slow control monitoring and control of the whole detector is done via the Beckhoff PLC described in chapter 7.

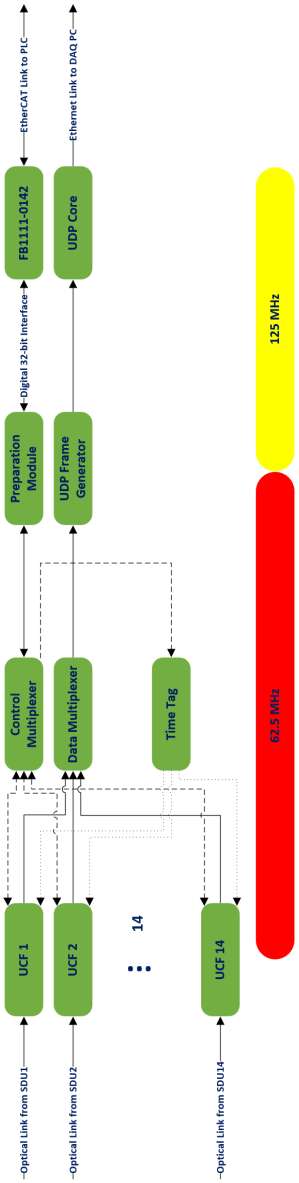


Figure 6.23: Functional diagram of the NAC

6.5 Qualification Measurements

In order to verify the functionality of the read out chain and all control components of the detector, a test board with a size of 300 mm x 160 mm for eight channels was created which can be seen in figure 6.24. This board represents the exact layout of the analog section with the identical components and traces. Moreover, it also represents the exact layout of the control section for the voltages. Overall, all tests of functionality and performance can be achieved with this set-up before the actual

production of the final electronics.

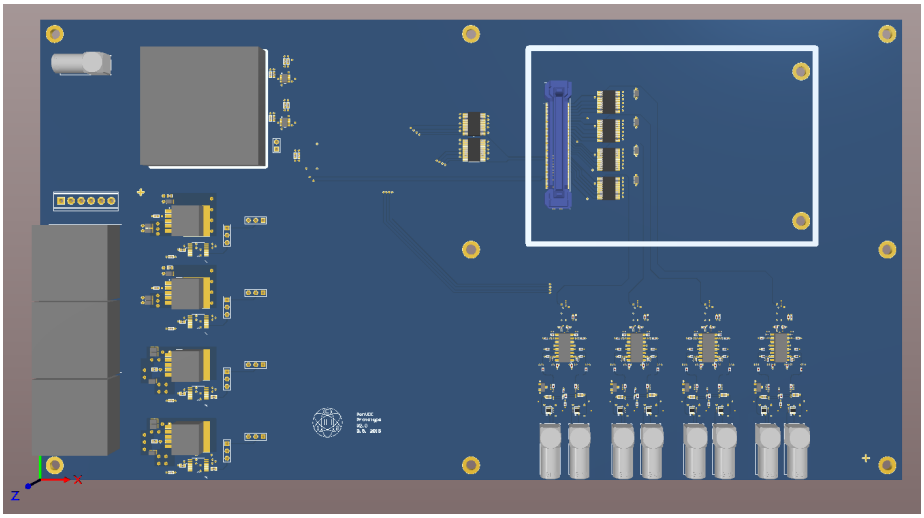


Figure 6.24: CAD model of the qualification set-up of the proton detector

6.5.1 Simulation

In a first step the design functionality was tested in the hardware with simulated ADC signals. Therefore an ADC emulator was designed which generates pseudo random signal values with linear feedback shift registers (LFSR) and overlays it in random distances with a proton signal. The frequency of signal events and all adjustable values for the signal detection can be set via the NAC. Fig. 6.25 shows a simulated signal event read out by the signal detection. As can be seen some samples before and after the actual event are also collected within the trigger window. The size of this windows is adjustable. Fig. 6.25 shows a vetoed event. The veto can be set on single channels or the whole card.

In order to test the performance of the SDU the simulated event frequency was increased from 1 Hz per channel (which is the expected event rate) up to 10 kHz per channel without any problems or a significant decrease of the performance.

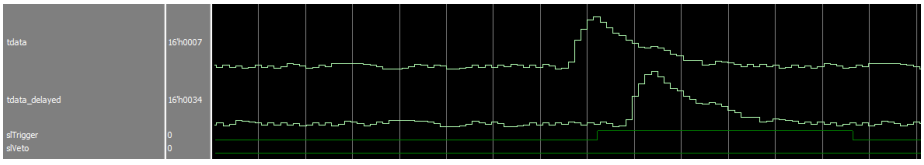


Figure 6.25: Picture of a simulated signal event.

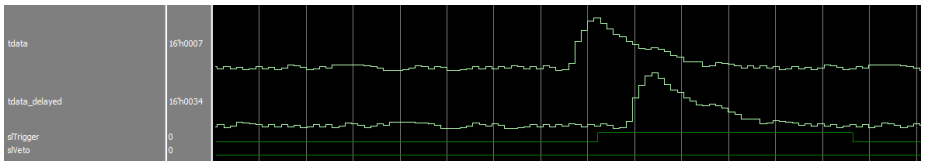


Figure 6.26: Picture of a simulated signal event which is vetoed.

6.5.2 Signal Generator

In a second step the design functionality was tested in the hardware together with the ADC read out and the analog electronics. A signal generator was used to generate signal events for all detector channels. Via DIP switches the different channels could be turned on and off for receiving the generated signal. The measurements were started with signal event frequencies of 1 Hz on six channels. The output read on the SDU was used to adjust the voltages of the preamplifier and the shaper to the optimal values. These are +/-4.5 V on the preamplifier and +/-5 V on the shaper.

Fig. 6.27 shows a signal event read out by the signal detection which was collected with the optimal preamplifier and shaper voltages. In order to test the performance of the SDU also here the event frequency was increased from 1 Hz per channel up to 10 kHz per channel without any problems or a significant decrease of the performance.

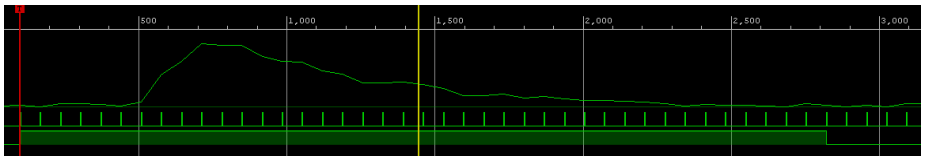


Figure 6.27: Picture of a signal event read out with the ADC and the analog electronics.

6.5.3 Conclusion

In total the tests with the ADC emulator and the signal generator showed that the complete electronics and read out chain is fully functional and can be used for the final production. It is even possible to read out the complete detector with event frequencies ten thousand times higher than the expected one.

Chapter 7

Experiment Control

In this chapter the control hardware of the PENeLOPE experiment will be described. It consists of several different electrical cabinets, power supplies and computation units. The following sections will first give an overview of the complete control topology and afterwards describe all parts of the experiment control in detail.

7.1 Overview

Fig. 7.1 gives an overview of the different components of the experiment control together with their interconnections and the designator. All designators mentioned here match the ones which can be found in the electrical layout plan of the experiment.

7.2 Power Cabinet - A2

The power cabinet A2 is the interface of PENeLOPE for power connections. PENeLOPE needs three three-phase connections. One is appropriated the superconducting power supply with 64 Ampere, one for the central coil power supply with 64 Ampere and the last one is a 32 Ampere connection suppling DAQ and slow control. The purpose of this cabinet is to have a defined power interface where the complete power to the experiment can be interrupted. All three lines are equipped with lockable rotary switches for this purpose.

7.3 PLC Cabinet - A3

The PLC cabinet A3 is located at the bottom of the PENeLOPE experiment and is the interface to the outer network and the experiment cabinet. Due to its physical

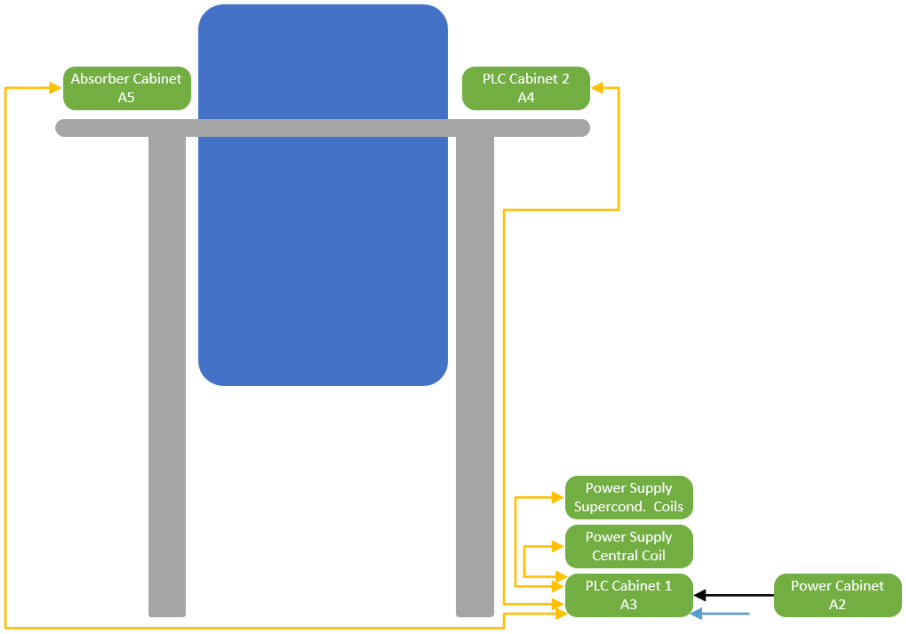


Figure 7.1: Scheme of the architecture of the experiment control, their connections and their positions throughout the experiment. The orange connections symbolize EtherCAT connections, the black one a power connection and the blue one an Ethernet connection.

position at the bottom of PENeLOPE all electronics needed for the UCN transport like the spin flipper and UCN switch are placed in this cabinet. Furthermore, it controls the power supplies for the central coil and the superconducting coils and monitors and controls the vacuum in the UCN guides. Additionally, the cabinet holds the industry PC which is used for implementing the human machine interface (HMI) and the interfaces to the detectors. The following subsection will describe the different components used in more detail.

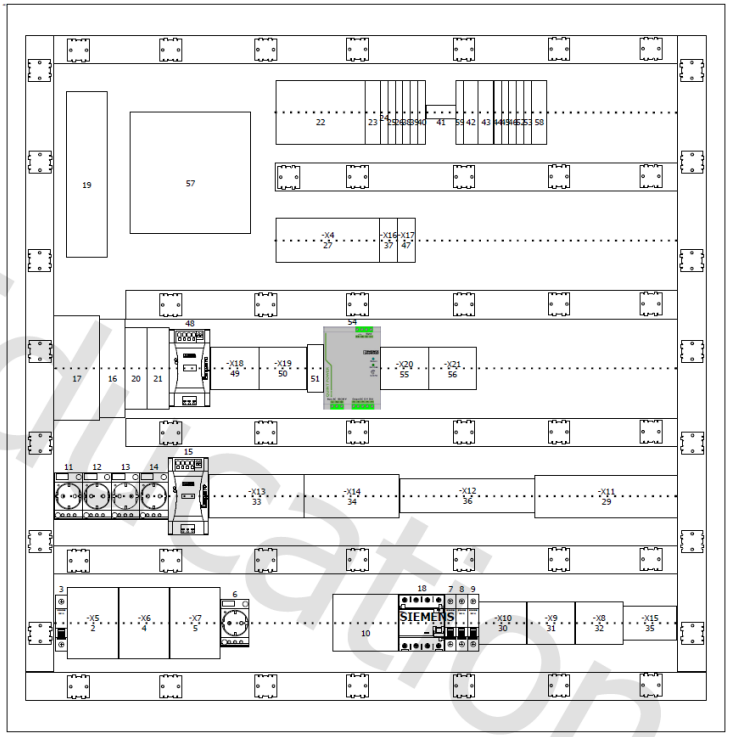


Figure 7.2: Schematic drawing of the PLC cabinet.

7.3.1 Power Supply

For the different components within the cabinet four different voltages - 230 V, 48 V, 24 V and 12 V - are needed. At the input the three phase connector is split into the individual phases each suppling a 230 V bus bar in the cabinet. The load of all components is distributed evenly on all three phases. All actual values like current, voltage and power of the three phases are monitored via a Beckhoff EL3413 PLC module.

In order to supply the 48 V an Emparro 5-100-240/48 power supply is installed. An Emparro 10-100-240/24 24 V power supply together with a Block 24 V under-voltage protection system are used to power the 24 V bus bar. For the 12 V line a Phoenix Contact QUINT-PS/1AC/12DC/20 is mounted.

7.3.2 Network Connections

Two Weidmueller IE-SW-BL05-5GT gigabit network switches are used for distributing the external and internal network connections. The external network is only connected to the industry PC within the cabinet whereas the internal network is connected to the industry PC, the PLC, the power supply for the superconducting coils and the other cabinet on top of PENeLOPE.

7.3.3 Industry PC

A Beckhoff C6920-0040 industry PC is used for implementing the different interfaces to the proton and neutron detector and to the HMI.

Proton Detector Interface

The interface to the proton detector is implemented with an UDP connection for the data which is received by the PC, processed and then stored onto a mirrored network attached storage. A live event display is included in the HMI. For the control line the EtherCAT protocol and the Beckhoff FB1111-0142 are used. The latter translates EtherCAT messages into a 32 bit wide digital interface which is then connected to the FPGA of the network access controller of the proton detector.

Neutron Detector Interface

The CASCADE-U neutron detector is equipped with an USB interface for both control and data logging. This interface together with the included software is used within the industry PC. A live event display is included into the HMI of the experiment control.

Human Machine Interface

The human machine interface of the experiment control is a server based web application which is provided by the industry PC and can be accessed via the external network connection. In order to protect the sensitive control access different user levels have been created that are controlled via a user access control. From the start up interface all important control parameters of the experiment can be steered manually. The PLC software in the background takes care of all supervision tasks and prevents undesired behavior of the experiment. The PLC and the related software will be described in more detail in the respective subsection.

7.3.4 UCN Infrastructure

In order to guide neutrons to the experiment, to prepare them for the storage and to count them several electrical and mechanical components are needed. To control

the flux of UCN there are two UCN valves produced by VAT. They are controlled via two digital I/Os each connected to a Beckhoff EL1859 digital I/O module. One is used for controlling the open and close functionality and the other one is used as a monitoring input of the current valve position. The first valve is used for the interface to the UCN source and the other one is used for closing the experiment storage volume.

For turning the high-field-seeking neutrons into low-field-seeking neutrons an adiabatic fast passage spin flipper is utilized as described in chapter 2 which consists of a high frequency flipper coil driven by an IED HMS 30 KHz sine function generator whose signal is amplified by a JVC KS-DR3002 amplifier. For guiding the neutron into the experiment or from the experiment to the detector a neutron switch is installed which is driven by a stepper motor VG-SFL010-KF40-STEP from BeamTec that is controlled by a Beckhoff EL7201-0010 stepper controller.

The CASCADE detector for the UCN is supplied with a gas mixture flow controlled by a red-y mass flow controller that is connected via two single ended connections to an analog input 4 to 20 mA EL3058 from Beckhoff. The connections are used for monitoring and setting the current flow.

7.3.5 Vacuum Infrastructure

Within the cabinet A3 the control of two different vacua - the guide vacuum and the cryostat isolation vacuum - is installed. This includes two 28691 ultra high vacuum shutters from Leybold which are both monitored and controlled by two digital I/Os connected to the Beckhoff EL1859. The vacuum is monitored by four ITR90 ultra high vacuum sensors from Leybold connected to two GraphixThree also from Leybold. Each of the GraphixThree is connected via a RS232 serial connection to the Beckhoff EL6002 RS232 module. As turbo-molecular pumps both vacua use the TURBOVAC 450 i/iX from Leybold. These pumps are controlled and monitored via several digital I/Os connected to a Beckhoff EL1859 and an analog output for pump speed monitoring connected to a Beckhoff EL4008. The fore-pump used together with the TURBOVAC is the Leybold Ecodry 65+. It is controlled via two digital I/Os connected to the Beckhoff EL1859 and one analog I/O connected to the Beckhoff EL4008.

7.3.6 PLC

The heart of the experiment control is the Beckhoff CX5130-0120 PLC where all modules are connected to via the EtherCAT protocol. It has a Windows 7 real-time operating system and offers to have tasks with different priorities and different cycle times. These can be independently programmed to cover all different requirements on the PLC software. This PLC is connected via a 10 m EtherCAT cable with distributed modules in the PLC cabinet A4 on top of PENeLOPE.

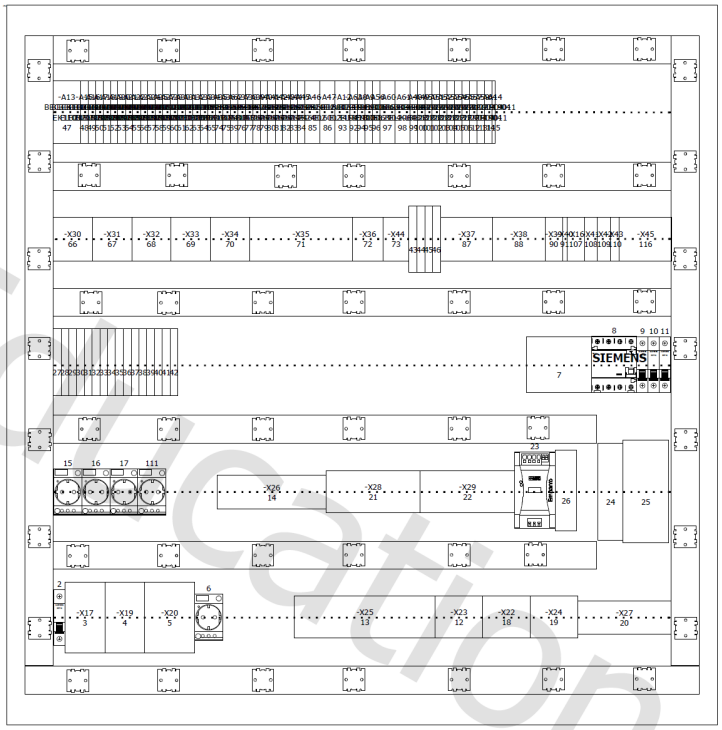


Figure 7.3: Schematic drawing of the PLC cabinet.

7.3.7 PLC Module List

Tables 7.1 and 7.2 list all modules of the PLC that are placed in the cabinet A3. They are listed from top to bottom as they are connected to the PLC. Additionally, a short description to every module is given - for more details the EPLAN can be used.

7.4 PLC Cabinet - A4

The PLC cabinet A4 is located on the platform of the PENeLOPE experiment and is the interface to the inside of the cryostat. Within the cabinet the electronics for controlling and monitoring the cryostat and the safety modules are placed. Via an EtherCAT and Ethernet connection the cabinet is interconnected with the cabinet A3. The following subsection will describe the different components used in more detail.

Module	Designator	Module Description	Connection Description
CX5130-0120	A03+A3-A4	24 V PLC main module	Internal network connection
EL3413	A03+A3-A5	Three phase power monitor	Monitors the three supply phases
EL1859	A03+A3-A5	Digital 8 Ch. In/8 Ch. Out	Monitors the network switches, the industry PC, the 12 and 48 V power supplies, the NAC and controls the NAC, the UPS and the industry PC
EL1859	A03+A3-A6	Digital 8 Ch. In/8 Ch. Out	Monitors and controls the turbo molecular pumps
EL1819	A03+A3-A7	Digital 16 Ch. In	Monitors the main rotary switch, the UPS, the UCN and vacuum shutter and the 12 V power supply
EL3068	A03+A3-A8	Analog 8 Ch. In 0-10 V	Monitors the superconducting coil power supply and the speed of the vacuum pumps
EL4008	A03+A3-A9	Analog 8 Ch. Out 0-10 V	Spare module
EL7201-0010	A03+A3-A10	Servo motor module with OCT	Controls the UCN switch
ZB8610	A03+A3-A11	Fan module	Cools the servo module
EL9100	A03+A3-A20	24 V power supply module	Provides power to the following modules
EL6002	A03+A3-A12	2 Ch. RS232 module	Controls and monitors the central coil and superconducting coil power supplies

Table 7.1: List of PLC modules and their connections.

Module	Designator	Module Description	Connection Description
EL6002	A03+A3-A13	2 Ch. RS232 module	Monitors the GraphixThree
EL3058	A03+A3-A14	Analog 8 Ch. In 4-20 mA	Controls the flow controller of the neutron detector
EL4124	A03+A3-A15	Analog 4 Ch. Out 4-20 mA	Controls the function generator of the spin flipper and the flow controller of the neutron detector
EL2624	A03+A3-A16	Relays 4 Ch.	Controls the UCN and vacuum shutter
EL1859	A03+A3-A17	Digital 8 Ch. In/8 Ch. Out	Monitors and controls the fore-pumps
EL2624	A03+A3-A18	Relays 4 Ch.	Controls the amplifier of the spin flipper
EK1122	A03+A3-A19	2 Ch. EtherCAT module	EtherCAT connection to cabinet A4
EL9011	–	Bus end cap	Shields the bus contacts

Table 7.2: List of PLC modules and their connections (continued).

7.4.1 Power Supply

The cabinet A4 needs 230 V and 24 V to supply all components with power. At the input the three phase connector is split into the individual phases each supplying a 230 V bus bar in the cabinet. The load of all components is distributed evenly on all three phases which are monitored via a Beckhoff EL3413 PLC module. An Emparro 10-100-240/24 24 V power supply together with a Block 24 V under-voltage protection system is used to power the 24 V bus bar.

7.4.2 Network Connections

One Weidmueller IE-SW-BL05-5GT gigabit network switch is used for the internal network connections. The connection is only a spare since it is not used within the cabinet.

7.4.3 Vacuum Infrastructure

The cabinet A4 controls the experiment vacuum of the storage volume. This includes a 28691 ultra high vacuum shutter from Leybold which is both monitored and controlled by two digital I/Os connected to the Beckhoff EL1859 and one relay connected to a Beckhoff EL2624. Three ITR90 sensors from Leybold together with a GraphixThree also from Leybold are used for monitoring. The latter is connected to a Beckhoff EL6002 for control and monitoring. The fore-pump - a Leybold Ecodry 65+ - and the turbo molecular pump - a Leybold TURBOVAC 450 i/iX - are controlled via digital and analog inputs and outputs connected to Beckhoff EL1859 and EL4008 modules.

7.4.4 Temperature Infrastructure

In order to monitor the temperatures of the different parts of the experiment 16 CERNOX low temperature sensors and 15 PT100 sensors are placed throughout the experiment. The CERNOX sensors are connected to two LakeShore LS218 temperature monitors which are read out via two RS232 connections and the Beckhoff EL6002 module. Beckhoff EL3202-0010 PT100 modules are used for reading out the PT100 sensors in a four wire mode.

7.4.5 Cryogenic Infrastructure

The cryogenic infrastructure controlled by the cabinet A4 includes the cryogenic valves, the flow controller, the helium level measurement and the pressure monitoring. In order to control and monitor the valves two digital I/Os on an EL1859 and one relay connection on an EL2624 are used. For steering the flow of the helium and nitrogen red-y series flow controllers from Voegtlin are used. They are connected via analog I/Os to the EL3058. The pressure of the system is monitored by

four Wika A-10 pressure sensors that are read out via a 4-20 mA analog signal on a Beckhoff EL3058. Six American Magnetics Model 1700 Liquid Level Controllers are used for reading the helium level. They are connected via analog signals to a Beckhoff EL3058 and via RS232 to Beckhoff EL6002 modules.

7.4.6 High-Voltage Infrastructure

In order to supply the high-voltage of 30 kV to the proton detector a FUG high voltage power supply is installed which together with a FUG 0-15 V power supply provides the voltages needed for the proton detector on the high electrostatic potential of 30 kV. For control purposes the high-voltage power supply is connected via RS232 to a Beckhoff EL6002 module.

7.4.7 Safety Infrastructure

The safety system of the experiment is connected to the EtherCAT bus and can be monitored by the regular PLC but it is a completely independent system which does not need neither the EtherCAT bus nor the regular PLC. The heart of the system called TwinSAFE is the EL6900 TwinSAFE PLC. This PLC is independently programmed and has a small UPS inside in order to guarantee the safe state also in the loss of electric power. The program within this PLC only consists of logic AND, OR and NOT operators and is TÜV certified for the use at nuclear reactors. All highly critical parameters of the experiment are directly monitored with TwinSAFE modules - this includes the voltages of the superconducting coils and the emergency stop buttons. Additionally, there are some spare inputs which could be used for more parameters. The voltages are monitored via ES3068, ES1904 and KS3122. Moreover, there are two signal lamps controlled via a TwinSafe EL2904. For converting the voltages on the coils to signals of 0-10 V and 4-20 mA the WAGO 2857-401 isolation amplifier is used.

7.4.8 PLC Module List

Tables 7.3, 7.4 and 7.5 list all modules of the PLC that are placed in the cabinet A4. They are listed from top to bottom as they are connected to the PLC. Additionally, a short description to every module is given - for more details the EPLAN can be used.

7.5 Absorber Cabinet - A5

The electronics of the absorber mechanism described in chapter 5 are installed in the electrical cabinet A5 which is placed next to the cabinet A4 on the platform of PENeLOPE. The main part of the cabinet are the six Bosch Rexroth IndraDrive CS frequency converters which are used to steer the linear actuators of the absorber.

Module	Designator	Module Description	Connection Description
EK1100	A04+A4-A13	24 V bus entry module	EtherCAT bus entry connection
EL3202-0010	A04+A4-A15	PT100 4-wire module	Monitors the PT100 sensors
EL3202-0010	A04+A4-A16	PT100 4-wire module	Monitors the PT100 sensors
EL3202-0010	A04+A4-A17	PT100 4-wire module	Monitors the PT100 sensors
EL3202-0010	A04+A4-A18	PT100 4-wire module	Monitors the PT100 sensors
EL3202-0010	A04+A4-A19	PT100 4-wire module	Monitors the PT100 sensors
EL3202-0010	A04+A4-A20	PT100 4-wire module	Monitors the PT100 sensors
EL3202-0010	A04+A4-A21	PT100 4-wire module	Monitors the PT100 sensors
EL3202-0010	A04+A4-A22	PT100 4-wire module	Monitors the PT100 sensors
EL3202-0010	A04+A4-A23	PT100 4-wire module	Monitors the PT100 sensors
EL3202-0010	A04+A4-A24	PT100 4-wire module	Monitors the PT100 sensors
EL9100	A04+A4-A62	24 V power supply module	Provides power to the following modules
EL3202-0010	A04+A4-A25	PT100 4-wire module	Monitors the PT100 sensors
EL3202-0010	A04+A4-A27	PT100 4-wire module	Monitors the PT100 sensors
EL3202-0010	A04+A4-A28	PT100 4-wire module	Monitors the PT100 sensors
EL3202-0010	A04+A4-A30	PT100 4-wire module	Monitors the PT100 sensors
EL3202-0010	A04+A4-A31	PT100 4-wire module	Monitors the PT100 sensors

Table 7.3: List of PLC modules and their connections.

Module	Designator	Module Description	Connection Description
EL1859	A04+A4-A32	Digital 8 Ch. In/8 Ch. Out	Monitors the network switch and the 24 V power supply and controls the UPS
EL1859	A04+A4-A33	Digital 8 Ch. In/8 Ch. Out	Monitors and controls the vacuum pumps
EL1819	A04+A4-A34	Digital 16 Ch. In	Monitors the UPS, the main rotary switch, the cryo valves and the vacuum shutter
EL3068	A04+A4-A35	Analog 8 Ch. In 0-10 V	Monitors the vacuum pump speeds
EL3068	A04+A4-A36	Analog 8 Ch. In 0-10 V	Monitors the system pressure
EL3068	A04+A4-A37	Analog 8 Ch. In 0-10 V	Monitors the flow controller
EL4004	A04+A4-A38	Analog 4 Ch. Out 0-10 V	Spare module
EL9100	A04+A4-A63	24 V power supply module	Provides power to the following modules
EL6002	A04+A4-A39	2 Ch. RS232 module	Controls the helium level
EL6002	A04+A4-A40	2 Ch. RS232 module	Controls the helium level
EL6002	A04+A4-A41	2 Ch. RS232 module	Controls the helium level
EL2624	A04+A4-A45	Relays 4 Ch.	Controls the valves and shutter
EL6002	A04+A4-A46	2 Ch. RS232 module	Controls the high voltage and CERNOX readout
EL6002	A04+A4-A47	2 Ch. RS232 module	Controls the vacuum and CERNOX readout

Table 7.4: List of PLC modules and their connections (continued).

Module	Designator	Module Description	Connection Description
EL6900	A04+A4-A8	TwinSAFE PLC	TwinSAFE PLC
ES3068	A04+A4-A9	Analog 8 Ch. In 0-10 V	Monitors the superconducting coil voltages
ES3068	A04+A4-A56	Analog 8 Ch. In 0-10 V	Monitors the superconducting coil voltages
EL2904	A04+A4-A60	Digital 4 Ch. Out	Controls the signal lamps
EL2904	A04+A4-A61	Digital 4 Ch. Out	Controls the signal lamps
KS3122	A04+A4-A48	Analog 2 Ch. In 4-20 mA	Monitors the superconducting coil voltages
KS3122	A04+A4-A49	Analog 2 Ch. In 4-20 mA	Monitors the superconducting coil voltages
KS3122	A04+A4-A50	Analog 2 Ch. In 4-20 mA	Monitors the superconducting coil voltages
KS3122	A04+A4-A51	Analog 2 Ch. In 4-20 mA	Monitors the superconducting coil voltages
KS3122	A04+A4-A52	Analog 2 Ch. In 4-20 mA	Monitors the superconducting coil voltages
KS3122	A04+A4-A53	Analog 2 Ch. In 4-20 mA	Monitors the superconducting coil voltages
KS3122	A04+A4-A54	Analog 2 Ch. In 4-20 mA	Monitors the superconducting coil voltages
KS3122	A04+A4-A55	Analog 2 Ch. In 4-20 mA	Monitors the superconducting coil voltages
EL1904	A04+A4-A57	Digital 8 Ch. In	Monitors the emergency buttons
EL1904	A04+A4-A59	Digital 8 Ch. In	Monitors the emergency buttons
EL1904	A04+A4-A64	Digital 8 Ch. In	Monitors the emergency buttons
EL9011	A04+A4-A14	Bus end cap	Shields the bus contacts

Table 7.5: List of PLC modules and their connections (continued).

Via an EtherCAT line from the cabinet A3 the converters are connected in-between themselves and the PLC. Control-wise one of the converters is used as the master and the other five follow the actuation curve of the master.

Part II

Intelligent FPGA Data Acquisition Framework

Chapter 8

On The Way Towards an Intelligent FPGA Data Acquisition Framework

Modern data acquisition systems for experiments in high-energy physics but also other fields face high demands on their data throughput, reliability, resolution and accuracy. This is successfully implemented in several CERN experiments like e.g. ATLAS, COMPASS and CMS or LHCb. All these experiments use different FPGA cards and high-speed serial links for communication, data compression and synchronization. As an example for the underlying topology and the system architecture the DAQ system of the COMPASS experiment is shown in fig. 8.1. Data links connect the front-ends to the first FPGA stage, which are then connected via multiple links to computer farms. The trigger and timing information and the slow control data are distributed in star-like networks to the front-ends and FPGA stages. It can be seen that a given similarity in the systems' architecture allows to generalize and re-use system components like the FPGA cards or the communication links or the read-out interfaces in different experiments. This idea led to the development of the Intelligent FPGA Data Acquisition Framework (IFDAQ) [3]. The architecture of the framework is shown in fig. 8.2. It consists of front-end, data concentrator and trigger generator modules connected all via a unified communication framework (see chapter 13). The front-end modules interface to the detector and digitize the incoming data either via a TDC (see chapter 9) or ADC (see chapter 10). After being digitized the data are processed further in multiple stages of concentrator modules which also build the final event(s) of the system (see chapter 10). The trigger generator is used in parallel to the data concentrators. It collects data from the front-ends and uses the information to generate trigger signals. Both, the concentrator and trigger module, are implemented with a FPGA card described in chapter 12. The front-ends can also be implemented with standard cards described in the concerning chapters but also can be freely adapted and implemented on any card housing a Xilinx FPGA.

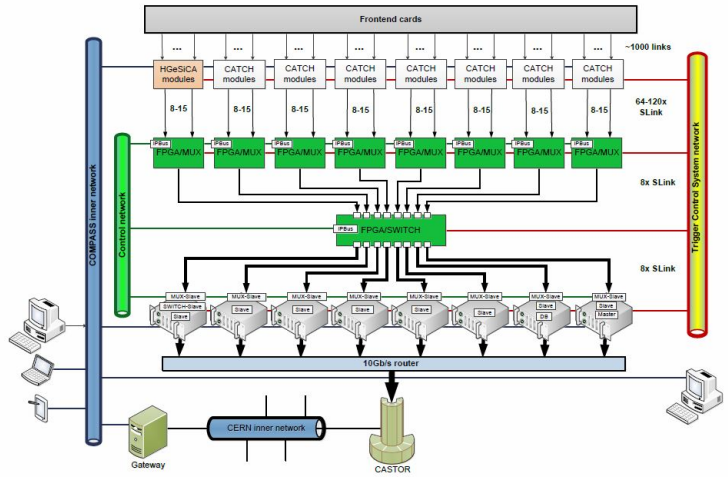


Figure 8.1: DAQ topology of the COMPASS experiment [4]

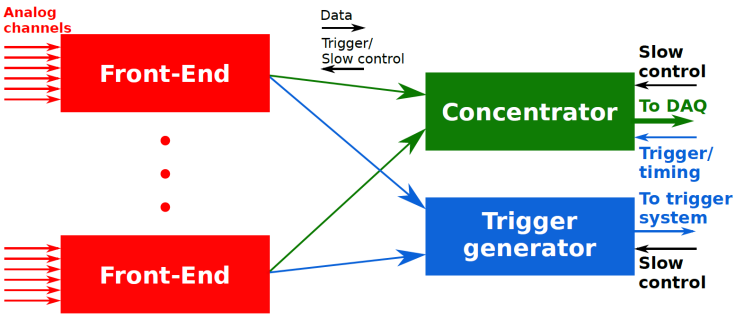


Figure 8.2: Architecture of the IFDAQ

Chapter 9

Time-to-Digital Converter

The time-to-digital converter utilizes hardware components present in each FPGA to perform a very accurate (picosecond region) and fast conversion (nanosecond region). Each input of a Xilinx FPGA has a built-in programmable temperature stabilized delay component called IODELAY and a serial-to-parallel converter called ISERDES. The actual measurement can either use two or four IODELAY/ISERDES pairs depending on the desired accuracy of the measurement. The incoming signal is distributed via the programmable IODELAYs to the ISERDES where the data is parallelized. For the Artix 7 FPGA which is also used as a hardware basis of the IFDAQ TDC card the registered output width of each ISERDES is 8 bit which in turn leads to a bin width of $f_{SampleClock}/16$ for two pairs and $f_{SampleClock}/32$ for four pairs. Together with the granularity of the IODELAY component (typically in the 50 ps region for Xilinx 7-Series FPGAs [56]) the differential non-linearity of the measurement can be calculated via

$$DNL = \frac{T_{delay}}{2 \cdot T_{bin}}. \tag{9.1}$$

9.1 Hardware

Within the IFDAQ framework a small low cost FPGA card based on an Artix 7 FPGA from Xilinx was developed. It is capable of handling 64 input channels and is connected via UCF to data concentrator and trigger cards or it can be used in a table top set-up with only an IPBus [15] connection for the slow control and a UDP connection for the data stream. A CAD image of the card is shown in fig. 9.1. Currently similar cards are used by the COMPASS and NA64 experiments at CERN.

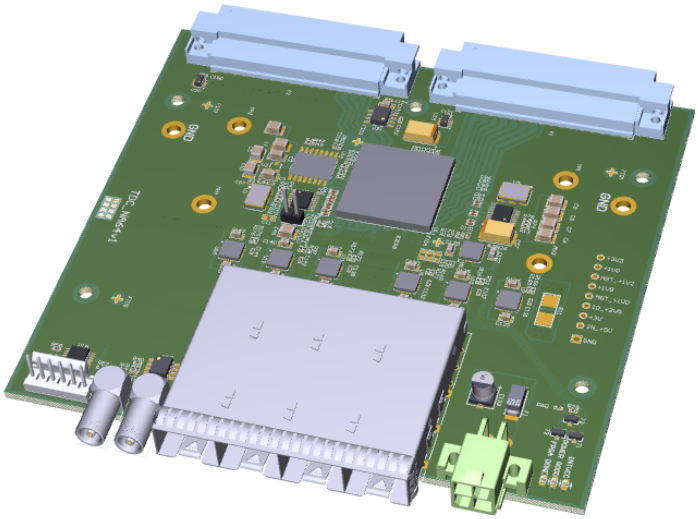


Figure 9.1: IFDAQ TDC card.

Chapter 10

Analog-to-Digital Converter

The ADC core of the IFDAQ consists of three different interfaces depending on the required sample rate and hardware used. The different cards developed are all pin compatible with the MSADC card developed for COMPASS experiment [32] and are described in the following sections.

10.1 MSADC 40/80 MSPS

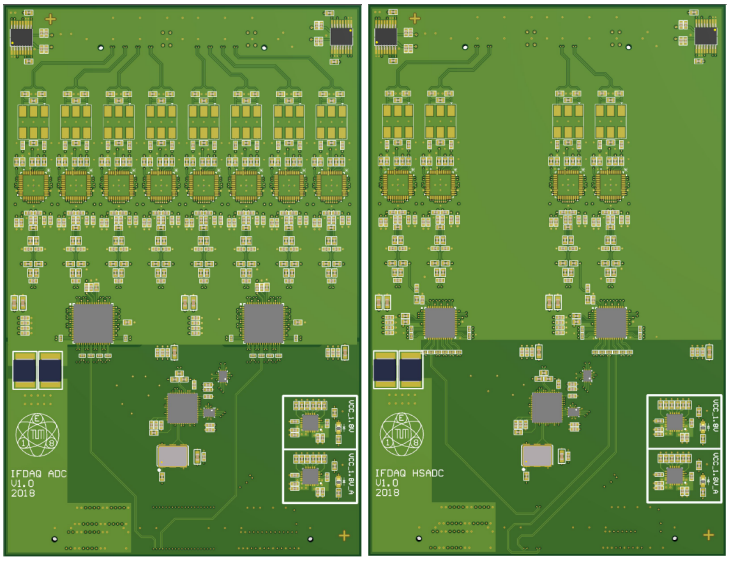
The MSADC card developed for the COMPASS experiment [32] is the basis of the ADC cards developed within the IFDAQ. All further cards are based on the same form factor and are pin compatible. Implemented on the MSADC card are four ADS5270 ADCs from Texas Instruments capable of eight channels each. Depending on the mode the card is used in the sampling rate is either 40 MSPS in the non-interleaving mode or 80 MSPS in the interleaving mode effectively cutting the number of channels by half. A parallel LVDS interface for data communication and a serial I2C interface for the slow control are used.

10.2 MSADC 80 MSPS

The planned upgraded version of the old MSADC card described in the previous section can be seen in fig. 10.1. It implements two AD9637 ADCs from Analog Devices each capable of eight channels at 80 MSPS and 12 bit resolution. From the interface point of view the data is now transmitted directly from the ADC via one serial LVDS line per channel and one I2C line for the slow control.

10.3 MSADC 105/640/1000 MSPS

The new planned top line card for very high data rates is capable of handling eight channels at 105 MSPS and 14 bit resolution, four channels at 640 MSPS and 12 bit resolution and two channels at 1000 MSPS and 8 bit resolution. This is achieved with two HMCAD1250 ADCs from Analog Devices. Interface wise the cards is read out via eight serial LVDS lines and can be configured via one I2C line. A image of the card can be found in fig. 10.1.



(a) (b)

Figure 10.1: (a) CAD model of the MSADC card implementing the AD9637. (b) CAD model of the MSADC card implementing the HMCAD1520.

Chapter 11

Event Builder

Until the COMPASS experiment at CERN introduced the first FPGA based event builder [4] all the event building was done on PCs and conventional network switches reducing the data throughput and reliability of the whole system. The new event builder algorithm is designed using 4 GB of external memory which is accessed from the FPGA via the MIG core from Xilinx. As a memory type currently DDR3 is used but this will be upgraded to DDR4 with the next generation FPGA card described in chapter 12. Depending on the number of outgoing links of the event builder the memory is divided in just as many banks which are then sub-divided into slots which have the size of the largest possible event in the system. Data from the incoming links is checked for consistency at first. If the data frame is corrupted it is replaced with a dummy frame in order to preserve the event structure. If in turn the data is not corrupted, it is passed to the data writer modules which will put what is part of an event into the different slots. As soon as all data writers have written their information belonging to an event into the memory the pointer to the event is handed over to the reader module which is able to extract the complete event from the memory. Fig. 11.1 and fig. 11.2 show the architecture of the event builder with a DDR3 memory and the event fragments before and after the memory/event builder. For the DDR3 memory the data throughput of 3 GB/s is sufficient to have multiple writers and readers sharing the memory access depending on the link speed.

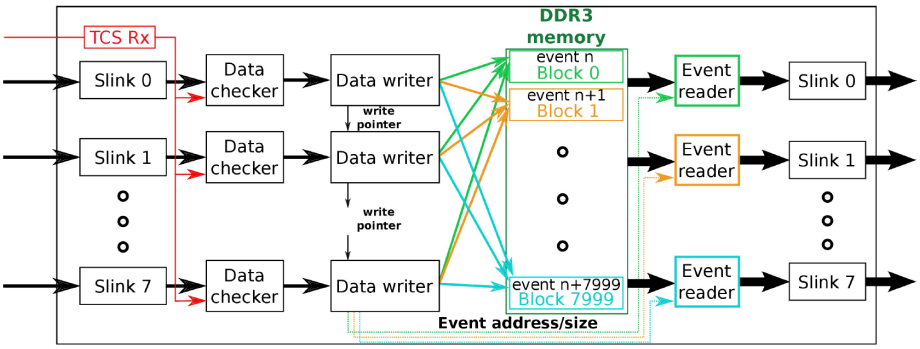


Figure 11.1: IFDAQ event builder architecture.

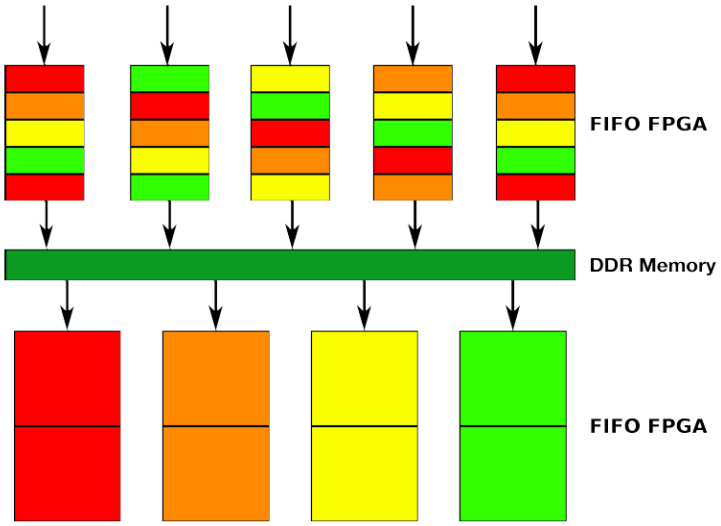


Figure 11.2: IFDAQ event builder event fragment propagation.

Chapter 12

Multi-purpose FPGA card

When the IFDAQ was originally developed [3] the multi-purpose card for the framework was the DHx card developed for the COMPASS [4] and BELLE2 [31] experiments . This card was designed in the AMC form factor and implemented one 2 GB DDR3 memory and a Virtex 6 Xilinx FPGA with a maximum link rate of 6 GB/s. For the BELLE 2 experiment five DHx cards were connected to the detector and then concentrated further into one DHx card. This was the starting point of the development of the new multi-purpose FPGA card since this single card should replace at least one of these clusters. Additionally, it was decided to upgrade the memory and the high-speed serial links to the nowadays state-of-the-art transmission rates of up to 30 GB/s.

12.1 Architecture

The new FPGA card of the IFDAQ can be seen in fig. 12.1. In comparison to the previous card the new one features a state-of-the-art FPGA, 64 high-speed-serial links with speeds of up to 30 GB/s and two DDR4 memories with a total memory of 16 GB. All important components and parts of the card are described in details in the following sections. From the size point of view the card only increased to double the width AMC form factor size despite it is able of replacing several AMC form factor cards.

12.1.1 FPGA

The FPGA type used is the Xilinx Kintex UltraScale XCKU095 in the B2104 package with a size of 47.5 x 47.5 mm. A unique feature of this FPGA type is that it is pin compatible with the higher performance Virtex UltraScale FPGAs. Thus, the exact same card developed could be also equipped with larger FPGAs if the demands on the card are growing. The XCKU095 overall has the capability of connecting up to four DDR4 memories and 64 high-speed serial links. In total it has a pin count

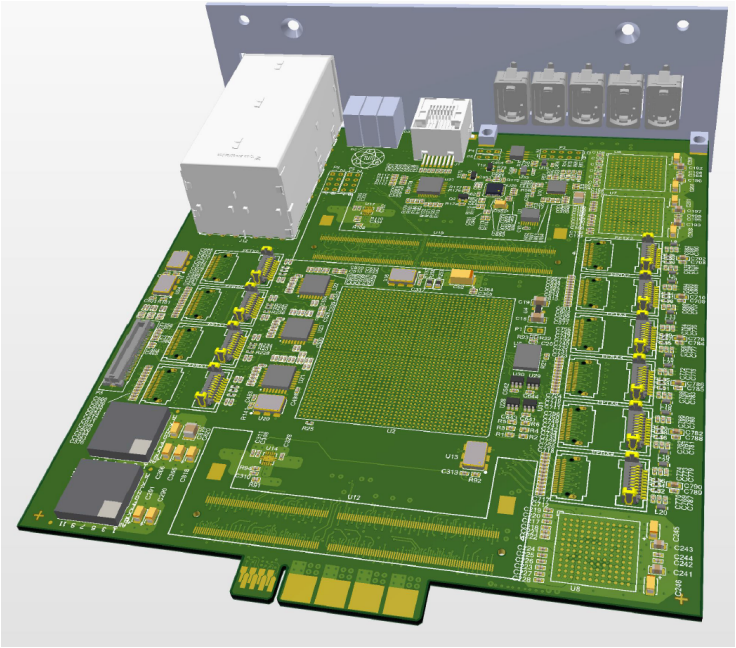


Figure 12.1: CAD model of the multi-purpose FPGA card.

of 2104 of which nearly all are used and connected. Compared to the old Virtex 6 FPGA the amount of logic cells available grew from 128,000 to 1,176,000, the amount of configurable logic blocks increased from 20,000 to 1,075,200 and the block memory available increased from 9,504 kB to 59,100 kB.

12.1.2 Power Supply

Due to the complex design of the FPGA and the internal different voltages, these should be switched in certain sequences during power-on and power-off which shall be followed in order to get a reliable performance of the chip. In order to guarantee a correct sequencing the UCD9081 power sequencer and monitor chip from Texas Instruments are used. During power-up the 3.3 V supply for this chip is immediately present and the further power-up sequence is only started when receiving an external signal from the carrier card (see section 12.2) or if the power on button on the card itself is pressed. This pre-active mode of the PCB can also be used to program the sequencer via an external I2C programmer or via the carrier card. Additionally, the sequencing function the UCD9081 can also be used to monitor all voltages present on the board. Since the voltages required for the FPGA and the high-speed links also require high currents the LTM4650 and the LTM4627 from Analog Devices are used in the design. These chips are small sized high performance DCDC converters with low losses developed specifically for FPGA designs. In total, the card can draw up to 30 A using an input voltage of 12 VDC which equals a maximum power of 360 W.

12.1.3 Clocking

Due to the large variety of demands on the link speed or timing synchronizations the clocking structure of the card is relatively complicated. In total, there are four different crystal oscillators on the PCB of which one 250 MHz oscillator is only used for the two DDR4 memory interfaces. By default a 125 MHz oscillator is installed via a fan out to all high-speed serial links and to several banks of the FPGA. Thus, this clock can be used as a system clock and as a reference clock to all high-speed links. In addition to these two there are two oscillators with frequencies of 127.76 MHz and 152.52 MHz (frequencies come from the demands of the experiments the card will be used in). Both of them are connected together with an external clock input from the front panel to a clock synthesizer chip which is on a piggyback PCB and connects up to three different synthesized clocks to FPGA input banks and two synthesized clocks to all FPGA high-speed links as reference clocks. All outputs of the synthesizer chip can be phase adapted to the inputs which could then be used as a clock recovery and synchronization circuit. The synthesizer chip also functions as a clock jitter cleaner for the external clock input. In total, the error of all oscillators and generated clocks shall be in the region of ± 15 ppm.

12.1.4 Flash

As a memory device which stores the FPGA firmware the Micron serial NOR flash memory MT25QL02GCBB with a total size of 2 GB is used. The device is interfaced via a quad width SPI line from the FPGA in the ”Master SPI Quad (x4)” configuration mode. In this mode the FPGA controls the communication with the flash and loads the firmware always after a rising edge signal on the ”PROGRAM-B” input of the FPGA. The FPGA indicates that it is fully programmed with a logic high signal on the ”DONE” pin. Via an external button connected to the ”PROGRAM-B” pin the FPGA can be manually reloaded.

12.1.5 Memory

There are two DDR4 2400 MT/s interfaces implemented in the XCKU095 which are connected via two 260 pin SODIMM connectors to external SDRAM modules with a size of 8 GB each. As a module the Micron DDR4 SDRAM SODIMM module MTA16ATF1G64HZ-8GB is used. The module enables very fast data rates according to the PC4-2400 standard. The latency of the module itself is in the order of 0.83 ns. The selected memory module is natively supported by the Xilinx memory interface generator. A step further could be made if the Xilinx memory interface is replaced by a custom GDDR6 memory interface which would enable memory speeds of 15 Gb/s and beyond.

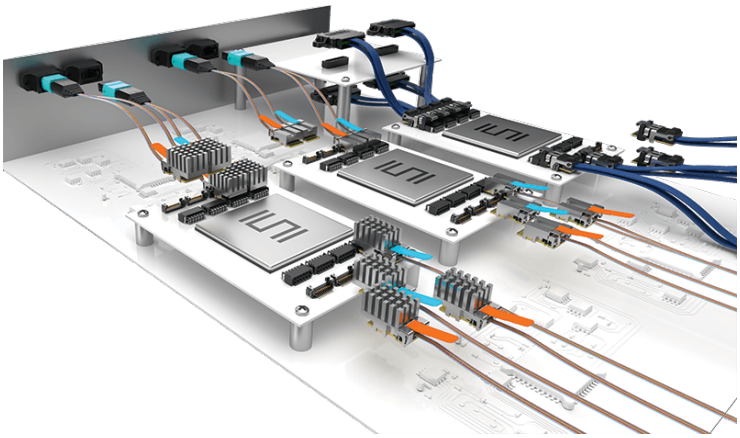


Figure 12.2: Image of the Samtec FireFly transceiver [43].

12.1.6 High-Speed Serial Links

There are two different types of high-speed transceivers used in the design of the card. Four of the 64 links use a two by two SFP+ cages with link speeds of up to 6 Gb/s. The other 60 links are equally distributed around the FPGA in order to have the same traces length for all the links. As a transceiver type a new high-speed transceiver module from Samtec is used which is called FireFly. A picture of such a transceiver can be found in fig. 12.2. The exact type used in the design is the ECUO-Y12-16-180-0-2-1-1-21 capable of handling 12 channels fully duplex with a speed of up to 16 Gb/s in a y configuration. This means that there is one transceiver dedicated for receiving and one for transmitting both combined into one MPO connector mounted on the front panel. All FireFly transceivers are connected via an I2C line to the FPGA in order to be monitored and configured via the FPGA.

12.2 Carrier Card

In order to mount two of the FPGA cards into a 1U high 19 inch rack box the carrier card shown in fig. 12.3 was developed. The carrier is powered via a Traco Power TPP150-112 providing a power of 150 Watt at 12 VDC. In addition to the TPP150 there is one TDK Lambda PFE500F-12 per FPGA card slot providing up to 500 W at 12 VDC. From fig. 12.3 it can be seen that additionally to the power supplies and the two slots for the FPGA cards there are additional switches to turn on and off the FPGA cards, a four slot SFP+ cage and a USB connection for the JTAG connection to the on board FPGA and the two FPGA cards in the slots. The SFP+ cage is connected to an Artix 7 FPGA from Xilinx which is used to interface the I2C lines to the two FPGA cards. Furthermore, the small FPGA controls the cooling fans within the 19 inch rack box. In total nine EBM Papst 422 J/2HP fans can be connected to the FPGA providing a total air flow of 234 m^3/h which is sufficient to provide enough cooling power even for the worst case power consumption of 1.15 kW.

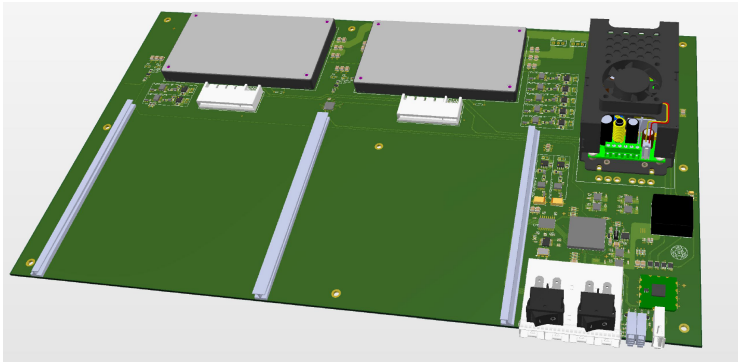


Figure 12.3: CAD image of the multi-purpose FPGA card carrier.

Chapter 13

Unified Communication Framework

13.1 Introduction

In state-of-the-art experiments in high energy physics the demands on the data acquisition systems are rising in the context of trigger-less readout, high data throughput, trigger accuracy and timing resolution. Currently these requirements are coped with by installing separate high-speed links for the different data, control, trigger and timing channels. As an example the DAQ topology of the COMPASS experiment [4] at CERN is shown in fig. 13.1. This topology is exemplary also for the other big CERN experiments like e.g. ATLAS, CMS or LHCb but also smaller experiments like the NA64 also at CERN.

The typical structure with different links for different purposes can clearly be seen. On the right side of the picture the Trigger Control System Network (TCS) represented by the red lines is used for synchronously distributing the triggers to the different modules throughout the experiment. Furthermore, the control links are represented by the green lines and are implemented with the IPBus protocol [15] via standard Ethernet links. Data is transported with separate links from the front-end modules to the multiplexers and from there via the FPGA switch to the read-out engines.

13.1.1 SODA

The first extension towards a unified communication framework was done with the Synchronization of Data Acquisition (SODA) time distribution system developed by Konorov et al.([29]). In contrast to the TCS system or Time Trigger Control (TTC) the SODA not only provides global trigger information but also synchronizes all modules connected in the system to the global time. Topology wise SODA uses a star-like 1 to n topology in a bidirectional manner - in contrast to the TCS and TTC.

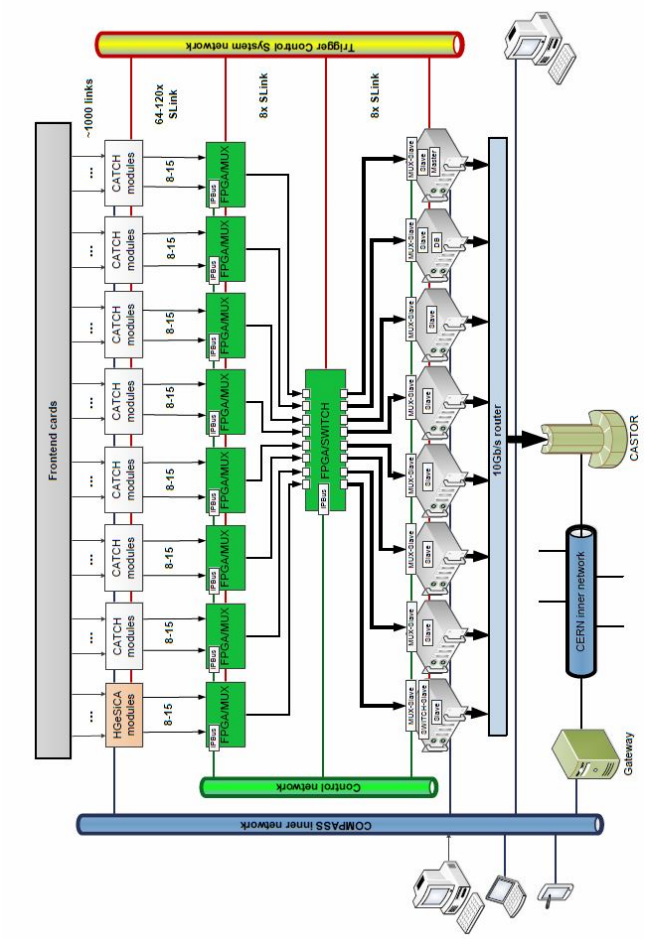


Figure 13.1: DAQ topology of the COMPASS experiment [4]

The underlying protocol uses the standard 8b/10b encoding scheme for inserting control and synchronization commands on the high-speed link which is also not dependent on the link speed itself. More detailed information on the SODA can be found here [29].

13.1.2 On the way to a unified framework

If the development started by the SODA group is consequently followed and extended the next step towards a unified framework is to combine all links for all different purposes in one single high-speed link only - and this without big losses in data throughput or timing resolution. This idea lead to the development of the UCF. The UCF combines overall up to 65 different bidirectional protocols via a single high-speed serial link. The 65 links can be divided into three classes. Different transmission priorities guarantee a deterministic and fixed latency for the first class and a transmission with a low delay for the second class. Timing and trigger messages belong to the first class (protocol number one) whereas the slow control messages belong to the second class (protocol number two) in order to avoid time-outs due to high traffic on data channels. The third class should be used for data transmission (all other protocols). To provide an easy integration of the UCF into the user code, the interface to all the different protocols is standardized and uses the ARM AMBA AXI Interface. The UCF can be used as a direct point to point connection between two or more FPGAs where one is the master and the other(s) the slave(s). The amount of masters and slaves per FPGA is just limited by FPGA resources. Fig. 13.2 shows the possible topology. The following sections will start with describing the underlying protocol and hardware that is used and will then describe in detail the initialization and communication procedure and the user interface. Finally, some tests and example projects will be presented.

13.2 Transport Layer Protocol

The basis of the UCF is a low level transport layer protocol that handles the whole communication and initialization. The key part of the protocol is the 8b/10b encoding scheme and the predefined 10b comma characters coming along with it. These are used to deal with the transmission control and also for the initialization. All high-speed serializer/deserializer related files used in the framework are compatible with Xilinx FPGAs (currently the Artix7, Virtex6, Kintex7 and Kintex7 UltraScale). In general the framework can also be implemented on e.g. Lattice FPGAs if the necessary SERDES files are adapted.

13.2.1 High-Speed Transceiver

The general structure and functionality of the high-speed transceivers is essential to understand the working principle of UCF and thus will be described in this

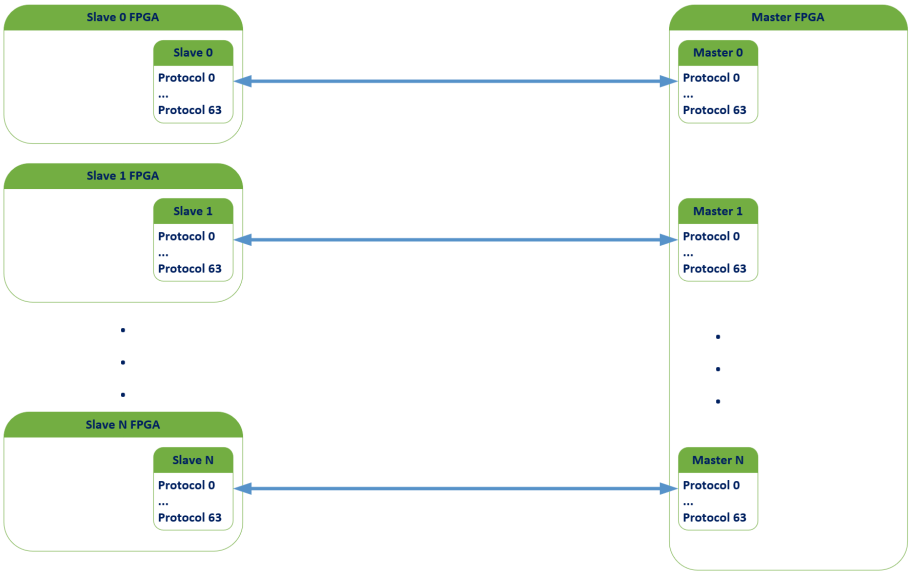


Figure 13.2: Topology of the UCF

subsection with the GTH transceiver of the Xilinx UltraScale FPGAs [57] as an example. Figure 13.3 shows the general structure of the GTH transceiver with the transmitting part on top and the receiving part on the bottom. The path taken by UCF is marked with a red line so it is clearly visible which features are used. The receiving part has two different paths since the master uses the elastic buffer and the slave bypasses it. The reason for this and the functionality of all components used will be described going from the left to the right in the transceiver schematics.

SerDes

The conversion from a serial data stream of the high-speed serial link to a parallel data stream within the FPGA is done with the Serializer/Deserializer (SerDes). A SerDes consists of two functional blocks - the PISO (Parallel Input Serial Output) and the SIPO (Serial Input Parallel Output). When going from a parallel to a serial data stream in the PISO typically a single shift register is used with the size determined by the number of bits in the parallel stream. This shift register is then filled by the parallel clock domain and read one by one by the serial clock domain. It is obvious that the serial clock rate must be higher than the parallel one. A typical problem occurring when crossing clock domains is the metastability which can lead to undesired bit changes within the data. To overcome this a SerDes features a double-buffered register. The general principle of a SerDes is visible in the left part of fig. 13.4.

In order to generate the necessary serial and parallel clocks the SerDes also features a phased locked loop (PLL) which is shown in the right side of figure 13.4. PLLs consist of a phase comparator, a loop filter and a voltage controlled oscillator.

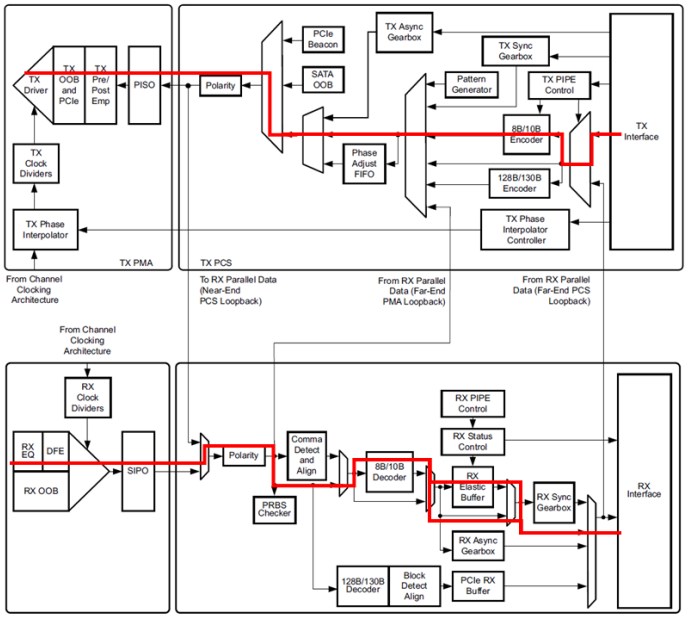


Figure 13.3: Schematic drawing of the GTH transceiver

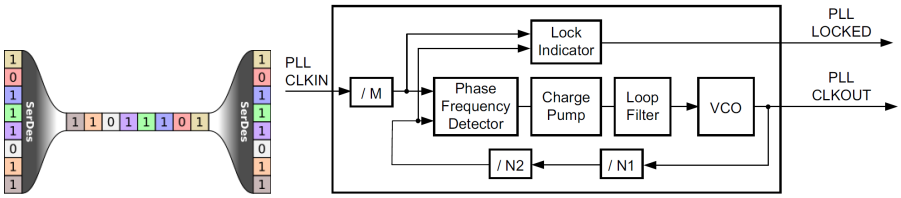


Figure 13.4: Schematic drawing of the SerDes (a) and PLL (b) functionality

Additionally, the PLL used in the transceiver features some dividers. These are used to match the PLL input frequency - typically in the 100 MHz range - with the PLL output frequency - typically some GHz - in the phase comparator. The input to the PLL is the reference clock of the transceiver and the output is then the serial clock of the link. Some additional dividers behind the PLL generate the clock(s) for the parallel data domain (also called physical coding sublayer (PCS)). Depending on the provided reference clock and the divider settings the serial clock frequency in GHz and the line rate in Gb/s can be calculated with the following equations:

$$f_{PLLClkOut} = f_{PLLClkIn} * \frac{N1 * N2}{M} \tag{13.1}$$

$$f_{LineRate} = \frac{f_{PLLClkOut} * 2}{D} \tag{13.2}$$

In the latter equation the factor two is due to the fact that both rising and falling edge

of the serial clock are used to transmit the parallel data. Typical settings for the UCF are e.g. $N1 = 5$, $N2 = 4$, $M = 1$, $D = 1$ and a reference clock of 125 MHz which leads to a serial clock frequency of 2.5 GHz, a parallel clock frequency of 62.5 MHz and a line rate of 5 Gb/s. The determination of the parallel clock frequency and a more detailed information on the meaning of the different letters will be described in 13.2.1. In addition to the SerDes the physical medium attachment (PMA) part of the transceiver visible in the left part of picture 13.3 consists of emphasizers on the sending part and equalizers on the receiving part. These are used to shape and control the signal shape and signal quality of the link which can be determined with the help of an eye diagram.

Polarity

High-speed serial links are typically connected to an FPGA with a differential pair connection in order to reduce the impact of electromagnetic noise to the signal line. A differential pair connection has a plus and a minus pin whereas the signal on the one pin is the negated signal of the other pin. If the connections of these pins are accidentally swapped on the PCB or within the transmission line the data received within the transceiver is negated. To overcome this problem the transceivers have a polarity control feature which is also actively used by UCF. During the initialization of the UCF the consistency of the data is checked and the polarity is swapped when necessary. A detailed description of the initialization and automatic polarity detection can be found in section 13.2.2.

8b/10b Encoder/Decoder

If transceivers send digital zeros and ones in an unbalanced manner this can lead to DC bias which can then introduce errors in the transmissions. Depending on the direction of the bias, charges can build up in the transmission media and either false zeros or ones are inserted. To overcome this problem and transmit an equal amount of zeros and ones on the serial link the 8b/10b encoding scheme was developed in 1983 by Albert X. Widmer and Peter A. Franaszek of the IBM Corporation. If this scheme is employed there are no more than five transmissions without a transition between one and zero or vice versa. By this not only the DC bias stays balanced but also a sophisticated and reliable clock recovery of the serial link is possible on the receiver/decoder side.

In the 8b/10b encoding the original eight bit data word is divided into five least significant bits (EDCBA) and three most significant bits (HGF). The first block is encoded to a six bit wide block (abcdei) and the second into a four bit wide block (fghj). The combination of both encoded blocks results in the encoded 10 bit value. By this combination overall a set of 256 data characters (Dx.y) and 12 control characters (Kx.y) is formed. The control characters are uniquely encoded 10 bit symbols that do not have an 8 bit data word representation. In the Xilinx transceivers the transmission and reception of these characters is shown by the CharIsK flag at the input and output of the transceiver block. A portion of this encoding set can be found in fig. 13.5. In principle, more combinations than the 268 visible are possible

Code Group	kin/ kout	8-bit data HGF EDCBA	10-bit data (RD-) abcdei fghj	10-bit data (RD+) abcdei fghj	Code Group	kin/ kout	8-bit data HGF EDCBA	10-bit data (RD-) abcdei fghj	10-bit data (RD+) abcdei fghj
D0.0	0	000 00000	100111 0100	011000 1011	D0.1	0	001 00000	100111 1001	011000 1001
D1.0	0	000 00001	011101 0100	100010 1011	D1.1	0	001 00001	011101 1001	100010 1001
D2.0	0	000 00010	101101 0100	010010 1011	D2.1	0	001 00010	101101 1001	010010 1001
D3.0	0	000 00011	110001 1011	110001 0100	D3.1	0	001 00011	110001 1001	110001 1001
:					:				
D31.0	0	000 11111	101011 0100	010100 1011	D31.1	0	001 11111	101011 1001	010100 1001
D0.2	0	010 00000	100111 0101	011000 0101	D0.3	0	011 00000	100111 0011	011000 1100
D1.2	0	010 00001	011101 0101	100010 0101	D1.3	0	011 00001	011101 0011	100010 1100
D2.2	0	010 00010	101101 0101	010010 0101	D2.3	0	011 00010	101101 0011	010010 1100
D3.2	0	010 00011	110001 0101	110001 0101	D3.3	0	011 00011	110001 1100	110001 0011
:					:				
D31.2	0	010 11111	101011 0101	010100 0101	D31.3	0	011 11111	101011 0011	010100 1100
D0.4	0	100 00000	100111 0010	011000 1101	D0.5	0	101 00000	100111 1010	011000 1010
D1.4	0	100 00001	011101 0010	100010 1101	D1.5	0	101 00001	011101 1010	100010 1010
D2.4	0	100 00010	101101 0010	010010 1101	D2.5	0	101 00010	101101 1010	010010 1010
D3.4	0	100 00011	110001 1101	110001 0010	D3.5	0	101 00011	110001 1010	110001 1010
:					:				
D31.4	0	100 11111	101011 0010	010100 1101	D31.5	0	101 11111	101011 1010	010100 1010
D0.6	0	110 00000	100111 0110	011000 0110	D0.7	0	111 00000	100111 0001	011000 1110
D1.6	0	110 00001	011101 0110	100010 0110	D1.7	0	111 00001	011101 0001	100010 1110
D2.6	0	110 00010	101101 0110	010010 0110	D2.7	0	111 00010	101101 0001	010010 1110
D3.6	0	110 00011	110001 0110	110001 0110	D3.7	0	111 00011	110001 1110	110001 0001
:					:				
D31.6	0	110 11111	101011 0110	010100 0110	D31.7	0	111 11111	101011 0001	010100 1110
K28.0	1	000 11100	001111 0100	110000 1011					
K28.1	1	001 11100	001111 1001	110000 0110					
K28.2	1	010 11100	001111 0101	110000 1010					
K28.3	1	011 11100	001111 0011	110000 1100					
K28.4	1	100 11100	001111 0010	110000 1101					
K28.5	1	101 11100	001111 1010	110000 0101					
K28.6	1	110 11100	001111 0110	110000 1001					
K28.7	1	111 11100	001111 1000	110000 0111					
K23.7	1	111 10111	111010 1000	000101 0111					
K27.7	1	111 11011	110110 1000	001001 0111					
K29.7	1	111 11101	101110 1000	010001 0111					
K30.7	1	111 11110	011110 1000	100001 0111					

Figure 13.5: Portion of the 8b/10b Encoding/Decoding table.

but they are not embedded since the disparity of each 10 bit value is limited to be either $+2$ ($RD+$), 0 ($RD+, RD-$) or -2 ($RD-$) . All data and control characters have a $RD+$ and $RD-$ representation. The running disparity state machine within the 8b/10b encoder will assume a negative disparity at startup so thus will use the $RD-$ representation of the eight bit value at the input. If the disparity of this value is zero the $RD-$ representation will still be used and if not the state machine will use the $RD+$ representation for the next incoming value. Depending on the disparity of this value the state machine will either remain in the $RD+$ representation or change back to the $RD-$ one.

Internal Data Width

Within the transceiver the data width is 40 bits which corresponds to a data width of 32 bits at the user interface. To calculate the parallel clock which is used at the user interface to the transceiver the serial clock frequency must be divided by the internal data path width. For the example in the last paragraph this would be 2.5 GHz/40 = 62.5 MHz.

Phase Alignment

On the receiving side of the transceiver the clock and data recovery (CDR) checks for data and clock transitions in the incoming data stream. By this the CDR recovers the serial link clock frequency which is then fed into the PLL of the transceiver in order to match the clock generated by the PLL to the recovered clock of the CDR. By doing so the transceiver guarantees a correct decoding of the data stream. If the elastic buffer of the receiver is bypassed not only the frequency of the PCS must be tuned correctly to the frequency of the incoming data but also the phase difference between PMA and PCS must be fine tuned to be exactly the same since otherwise the data might get corrupted.

All Xilinx transceivers feature an automatic phase alignment between the PMA and PCS parallel clock domain. This is also used on the slave part of the UCF in order to guarantee a deterministic latency when sending data from the master to the slave. Another possibility of crossing the clock domain between the parallel PMA and parallel PCS is the elastic buffer which is implemented on the receiving side of the UCF master. If the elastic buffer is used clocking resources can be saved and the RX and TX side can share a common interface clock.

An additional feature that must be implemented when using the elastic buffer is the clock correction. The clock correction can insert and remove certain predefined symbols into and from the data stream. UCF will ignore these symbols but they are needed in order to maintain a constant fill level of the elastic buffer and prevent an under- or overflow of the buffer which would lead to corrupted data or the loss of the link itself.

13.2.2 Initialization

After startup of the FPGA, after a reset signal, or after the loss of the link the UCF enters the initialization phase. During the initialization the UCF sends the alignment pattern x”BCDCBCDC” with the CharIsK of b”1111” for a time specified in the core package file (CorePkgUCF_ucf.vhd). During this sending of the alignment pattern the receiving side of the UCF continuously tries to lock on the pattern by resetting the CDR and PLL of the receiver. If finally the locking succeeded the polarity pattern x”4567BCDC” with a CharIsK of b”0011” will be send. The receiver will then check the consistency of the non comma characters in the pattern which would appear corrupted with wrong polarity settings. If this corruption is detected, the UCF changes the polarity on the receiver and resets the transceiver. When the polarity check succeeded both master and slave will enter the transmission of the constant pattern x”DCDCBCDC” with the CharIsK of b”1111” followed by a 32 bit wide constant after which the idle state is reached and the UCF is ready for transmitting protocols. The constant exemplary can be used to assign an IP address to a specific slave. During the idle mode the activation pattern x”01FCBCDC” with a CharIsK of b”0111” is send continuously. Fig. 13.6 shows the data transmitted during the initialization procedure - there is no difference between master and slave. The state machine diagrams can be found in fig. 13.7.

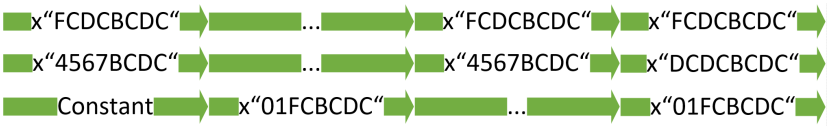


Figure 13.6: Data transmitted on the link during initialization

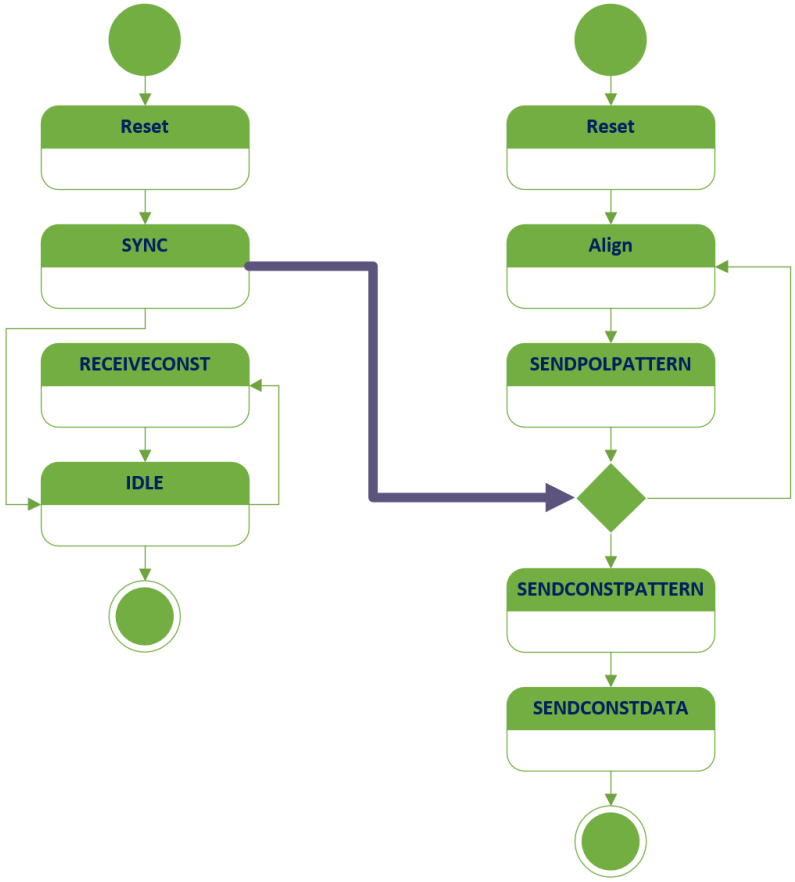


Figure 13.7: State diagram of the RX (left) and TX (right) side of the UCF during initialization

13.2.3 Frame Transmission and Priority Handling

After the initialization the UCF enters the normal operation, respectively the idle state, and is waiting for data to be sent. During the idle state the activation pattern x”01FCBCDC” with a CharIsK of b”0111” is continuously transmitted. All data transmitted via any of the 65 possible protocols is packed into frames whereas these frames do not have a constraint on their size. In the architecture of the frames only the channel with the highest priority and by this the channel with the determined latency differs from the other ones. This protocol - called TCS from

here on and in the state machine diagrams - has a dedicated identifier and can be sent at any time and can interrupt any ongoing transmission of data. It consists of a start of frame character x"A6DCA6DC", the data and the end of frame character x"A3DCBCDC". The structure of the frames for all other channels - USP from here on - is similar and only differs in the start of frame identifier. It consists of a 24 bit wide constant x"5CBCDC" concatenated with the 8 bit identifier of the protocol - which goes from decimal 0 to 63. Examples for a TCS frame, a USP frame and a TCS frame inserted into a USP frame can be found in fig. 13.8.

From the state diagram in fig. 13.9 it can be seen that the USP transmission at any time can be interrupted either by a TCS frame or by another USP frame and exactly this is the idea behind the priority handling. At the input of the UCF all protocols are packed into a big array and, depending on the index in this array, a frame can either be interrupted or not. The bigger the index the higher the priority. For example the protocol sent over index 63 can interrupt protocols 62 down to 0 but protocol 30 can only interrupt protocols 29 down to 0. By this it is also possible to have nested frames in nested frames etc.. For each transmission that is started on any channel the UCF marks this channel as actively transmitting and will only go back to the idle mode if all open transmissions are ended.

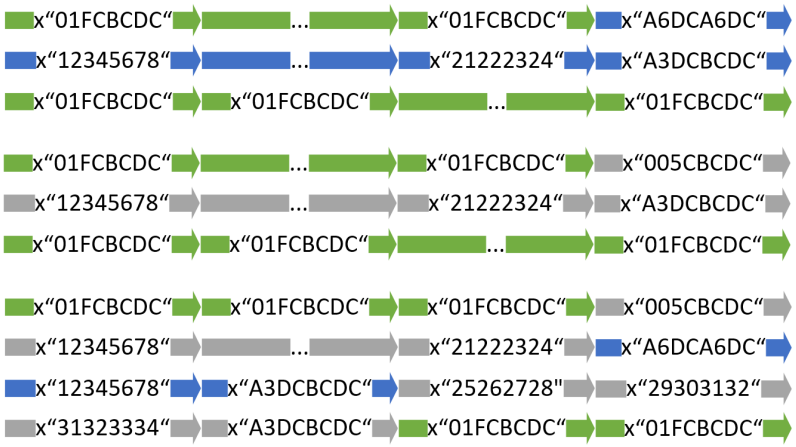


Figure 13.8: TCS frame (top), USP frame (middle) and TCS frame inside a USP frame (bottom)

13.2.4 Veto

The UCF also provides the possibility to veto certain protocol channels. This feature might be used to block communication over a single protocol or to implement the feature of back pressure in data acquisition systems. In order to implement the veto feature there are certain veto frames that are sent if the veto on any of the channels changed. All veto frame transmissions are allowed to interrupt ongoing USP frames in order to guarantee a minimum latency on the veto signal. The structure of a veto frame can be seen in figure 13.10. It splits the 64 channels in groups of 16 and

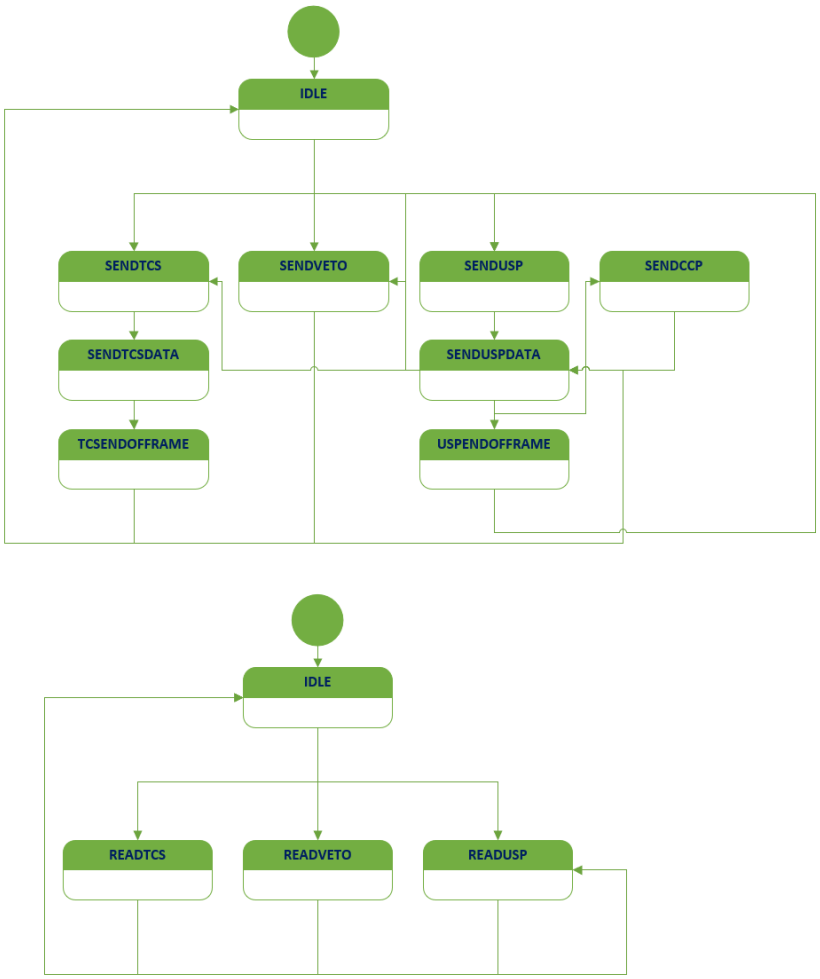


Figure 13.9: State diagram of the TX (top) and RX (bottom) side of the UCF during normal operation

concatenates each group with the veto character x”5CDC”. This means that at first the veto status of channels 63 to 48 is transmitted followed by the channels 47 to 32, 31 to 16 and 15 to 0. In the example frame the veto array for the channels is x”0000000000111100” which would result in the vetoed channels 8, 12, 16 and 20. How a channel is vetoed and how thew veto is released will be described in the section 13.5.

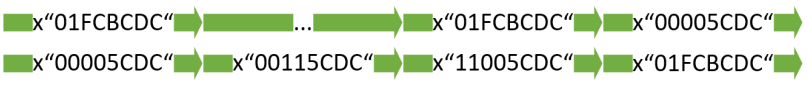


Figure 13.10: Veto frame

13.2.5 Clock Correction

As mentioned in the phase alignment paragraph the UCF will insert clock correction patterns from time into the data stream. The purpose of those correction patterns is a stable and reliable link also with huge data frames transmitted over the link. Clock correction only takes place when going from the slave to the master since the master uses the elastic buffer. Figure 13.11 shows a typical clock correction pattern x"FCFCBCDC" with a CharIsK of b"1111" inserted into a data frame.

Figure 13.11: Clock correction inserted into a normal data frame

The elastic buffer fill level can be monitored with a specific output "RXBUFSTATUS[2:0]" of the transceiver. If this output turns into b"101" or b"110" the buffer has an underflow or overflow which means that data is corrupted at the output. In the case of an error status like this the link and transceiver have to be reseted and the initialization has to start again. All data at the inputs will be lost. The error state of the buffer might also be reached if the provided clocks do not meet the frequency requirements.

13.3 Configuration

For the configuration a distinction between internal and external must be made. Internally the UCF makes use of two VHDL package files where all the necessary records and timeout constants et cetera are declared. Externally the user just needs to modify generic entries in the instantiation of the UCF wrapper and provide valid connections to the FPGA hardware. The example instantiation can be seen in figure 13.12.

13.3.1 Instantiation

The complete power of the UCF can be used by just including the wrapper file into the user VHDL. As can be seen from figure 13.12 the amount of UCF instantiation can easily be increased by just placing a generate statement around the necessary lines. All needed records for this are already defined in the package files coming with the UCF.

All features like the reference clocking or the link speed or the amount of protocols are defined in the generic assignment. With the entry "recg.intInterfaces" the user can define the amount of USP protocols next to the TCS. The distinction between master and slave is done by assigning "Master" or "Slave" to the "recg.cusCardPurpose" entry. By setting the "recg.cusDeviceType" to any of the values defined in the core package of UCF (Artix7, Virtex6, Kintex7UltraScale) all

```
Generate_Transceivers : for i in 0 to iNumberSDU-1 generate
    Inst_UCF_Wrapper : entity work.ucf_wrapper_ucf
    generic map(
        recg.intInterfaces                  => 2,
        recg.intCyclesMin                   => 10,
        recg.slP2PActivation                => '1',
        recg.cusCardPurpose                 => Master,
        recg.slActivateSim                  => slActivateSim,
        -- Transceiver Settings
        recg.cusDeviceType                  => Virtex6,
        recg.intRefClkPeriodRX              => 8.0,
        recg.intRefClkPeriodTX              => 8.0,
        recg.slSharedClkGen                 => '0',
        recg.intTraNumber                   => i,
        recg.intTransceivers                => iNumberSDU,
        recg.intMasterTransceiver           => 1,
        recg.intPllDivFDB                   => 5, -- N1
        recg.intPllDivOUT                   => 1, -- D
        recg.intPllDivREF                   => 2, -- M
        recg.intPllDivSEL                   => 4, -- N2
        recg.intPLLDivCLK                   => 5
    )port map(
        clk                                 => SYS_CLK_125,
        reco                                => reco(i),
        reci                                => reci(i)
    );

    Inst_UCF_REFCLK_SELECTION : entity work.ref_clock_change_ucf
    Port Map (
        slExtClk                            => SYS_CLK_125,
        iGenerateID                         => i,
        slUseGenClock                       => '0',
        slGenClockLock                      => '0',
        -- FROM/TO UCF
        slRstOut                            => UCF_RST(i),
        slvRefClkSel                        => reci(i).slvRefClkSel,
        slvMGTREFCLK                        => reci(i).slvMGTREFCLK,
        slvSOUTHREFCLK                      => reci(i).slvSOUTHREFCLK,
        slvNORTHREFCLK                      => reci(i).slvNORTHREFCLK,
        slREFCLK0_IN                        => REF_CLK,
        slREFCLK1_IN                        => REF_CLK,
        slREFCLKGEN0_IN                     => '0',
        slREFCLKGEN1_IN                     => '0'
    );

    -- From here it is for the Transceiver
    reci(i).slRXP                           <= RXP(i);
    reci(i).slRXN                           <= RXN(i);
    TXP(i)                                  <= reco(i).slTXP;
    TXN(i)                                  <= reco(i).slTXN;

    -- For Simulation only
    reci(i).slvRXDAT                        <= slvRXDAT(i);
    reci(i).slvRXCHK                        <= slvRXCHK(i);
    reci(i).slSyncDone                      <= slRXSYNC(i);
    slvTXDAT(i)                             <= reco(i).slvTXDAT;
    slvTXCHK(i)                             <= reco(i).slvTXCHK;
    slTXDIS(i)                              <= reco(i).slTXDIS;

    -- From here it is for control
    reci(i).slLinkReset                     <= RESET_STARTUP when slActivateSim = '0' else '0';
    reci(i).slLinkReinitialize              <= '0';
    reci(i).slRst                           <= (UCF_RST(i) or RESET_SHORT) when slActivateSim = '0' else '0';

    reci(i).slvConstant                     <= (Others=>'0');
    reci(i).slvID                           <= std_logic_vector(to_unsigned(i,4));

    reci(i).slvDIFFCTRL                     <= b"1101";
    reci(i).slvPRECTRL                      <= b"1100";
    reci(i).slvPOSTCTRL                     <= b"11001";

    -- From here it is for the UI
    UCF_RXCLK(i)                            <= reco(i).slRXCLK;
    UCF_TXCLK(i)                            <= reco(i).slTXCLK;
    UCF_ENABLED(i)                          <= reco(i).slLinkStatus;

    reci(i).tcsi                            <= UCF_TCS;

    reci(i).uspi(1)                         <= idle_reci_axi;

    reci(i).uspo_veto                       <= (Others=>'0');

    UCF_DAT (i)                             <= reco(i).uspo(1);

    UCF_CTRL_RECO(i)                        <= reco(i).uspo(0);
    UCF_CTRL_RECI_RDY(i)                    <= reco(i).slvUSPRdy(0);
    reci(i).uspi(0)                         <= UCF_CTRL_RECI(i);
end generate Generate_Transceivers;
```

Figure 13.12: Instantiation of the UCF wrapper and configuration

needed files for the specific transceiver are used in the design. With the help of the entries ”recg.intPllDivFDB”, ”recg.intPllDivOUT”, ”recg.intPllDivREF”, ”recg.intPllDivSEL”

and ”recg.intPLLDivCLK” the user can define the link speed according to the equations in 13.2.1. All clock related generics are explained in the reference clocking section in 13.3.2.

Next to the generics there are several ports that need to be accessed from the top module. Transceiver wise the RX and TX pins are accessed via the inputs ”reci(i).slRXP” and ”reci(i).slRXN” and outputs ”reco(i).slTXP” and ”reco(i).slTXN”. With the help of ”reci(i).slvDIFFCTRL”, ”reci(i).slvPRECTRL” and ”reci(i).slvPOSTCTRL” the transmission emphasis and amplifiers can be controlled. If no change is required on these they can also be skipped and remain to their default values according to the Xilinx manual [57]. In the section 13.2.2 the transmission of a constant was described in the end of the initialization. This constant can be written via ”reci(i).slvConstant” and read via ”reco(i).slvConstant”. The status of the UCF link can be checked via ”reco(i).slLinkStatus” - if this is logically high the link is established and if this is logically low the UCF is still initializing and the link is not up.

13.3.2 Reference Clocking

A very delicate part for all transceivers is the reference clocking. The period of the reference clocks for the receiving and transmitting part is set via ”recg.intRefClkPeriodRX” and ”recg.intRefClkPeriodTX”. In Xilinx FPGAs the high-speed transceivers are divided into quads whereas each quad can use the reference clock from the quad itself - ”reci(i).slvMGTREFCLK” - or the neighboring quads which are ”north” - ”reci(i).slvNORTHREFCL” - and ”south” - ”reci(i).slvSOUTHREFCLK” - of the original one. Detailed information about the quad structure and the possible values of the reference clock select vector - ”reci(i).slvRefClkSel” - can be found in the manual to the transceivers itself and depends strictly on the FPGA type used. As an example the value of b”000” on the reference clock select uses the first reference clock directly from the quad. For some applications it might be necessary to use a generated clock as the reference of the transceiver - for example a cleaned and recovered clock from another board. Together with the UCF a dedicated VHDL module is provided which can make reference clock changes automatically. For example the link itself is initialized with an on board reference clock and as soon as the generated clock is available the UCF will change to this one. If the clock is then lost afterwards the UCF automatically switches back to the local one. All changes of the reference clock will always lead to a loss of the link for some small time until the UCF re-initializes. Additionally, it is very important that all transceivers need a toggling reference clock already at the time of powering since otherwise a proper functionality cannot be guaranteed.

Figure 13.13 shows the configuration matrix of the reference clock changing module. At the input of the module there is the possibility to have two local and two generated clocks and currently up to 15 different transceivers connected to the module. They are distinguished by the index in the array and the port ”iGenerateID”. The usage can be seen in figure 13.12 where several UCF transceivers are instantiated with a generate.

In order to adapt the matrix to the needs of the user all columns have to be changed.

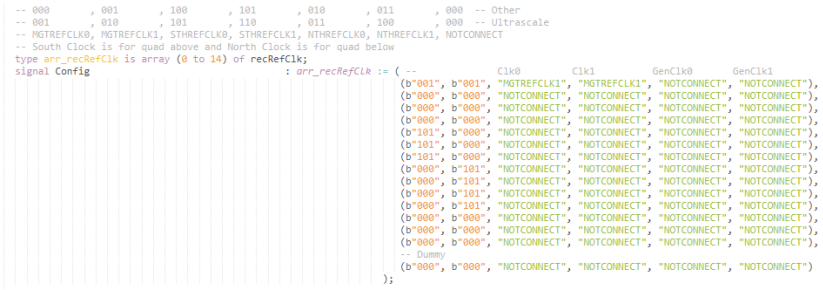


Figure 13.13: Configuration of the UCF reference clock module

The first two columns define the reference clock select vector of the transceiver. In the first column the default or fall back configuration is stored and in the second the configuration which is loaded as soon as the reference clock of this configuration is locked. All other columns define as which reference clock the inputs are used or if they are even connected.

In order to understand it properly two examples are made here. In the top line of the array, by default, the reference clock ”MGTREFCLK0” will be used which is connected to the ”slREFCLK0_IN” input of the module. If the clock provided on the input ”slREFCLKGEN0_IN” is locked - which shall be shown by a logic high on the input ”slGenClockLock” - the transceiver will use it in this case as the ”STHREFCLK0”. In contrast the second line only has the local reference clock input provided on port ”slREFCLKGEN0_IN” and uses it as the ”MGTREFCLK0” - here no reference clock change will take place. The automatic changeover of the reference clock can additionally be vetoed by the input ”slUseGenClock” forced to logically zero. This will prevent all changes and leave the local reference active no matter if the generated one is locked or not.

13.3.3 User Interface Clocking

In the default configuration the clocks for interfacing the UCF for reading and writing are created internally of each UCF instantiation and can be accessed via the ports ”reco(i).slRXCLK” and ”reco(i).slTXCLK”. An advanced feature is the possibility of sharing the clocks between several different instantiations of the UCF. For this feature the transceiver needs to get an unique ID via ”recg.intTraNumber”, the shared clock generation has to be active by forcing ”recg.slSharedClkGen” logically high and one of the transceivers needs to be marked as the master transceiver. This can be done by assigning ”recg.intMasterTransceiver” to a specific transceiver ID being used in one of the instantiations. Sharing of user clocks saves the amount of clocking resources used like clock generators and buffers. Notice that a sharing of the user clocks is only possible on the master side of the UCF since there the elastic buffer is implemented.

13.3.4 Reset Structure

From figure 13.12 it is visible that there are three different types of resets in the UCF. The ”reci(i).slLinkReset” will reset the transceiver itself whereas the whole state machines will stay untouched and remain working. Pulling the ”reci(i).slRst” logically high will result in a complete reset of the UCF including transceiver and state machines. If just the initialization of the link shall be repeated the port ”reci(i).slLinkReinitialize” shall be pulled high for at least one clock cycle of the system clock provided.

13.4 Simulation

With the flag ”recg.slActivateSim” pulled logically high the simulation mode of the UCF is activated which will reduce all waiting times in the state machines in order to shorten simulation time and will completely skip the transceiver implementation. The UCF is completely compatible with the UVVM simulation and verification framework [55]. The necessary scripts and files are included in the example project - see section 13.6 for more information.

13.5 User Interface

In order to interface the different protocols in the UCF the ARM AMBA AXI standard is used. It consists, in the UCF case, of the ready, keep, valid, last and data signal. If the user wants to write to the TCS channel this can be done as soon as the ready signal is logically high. Then the valid signal should be pulled high together with valid data. At the end of the frame the last signal shall be pulled high and the keep signal should be adapted according to the number of valid bytes in the last transmission. An exemplary TCS frames written to the UCF can be found in fig. 13.14. Additionally the output is shown.

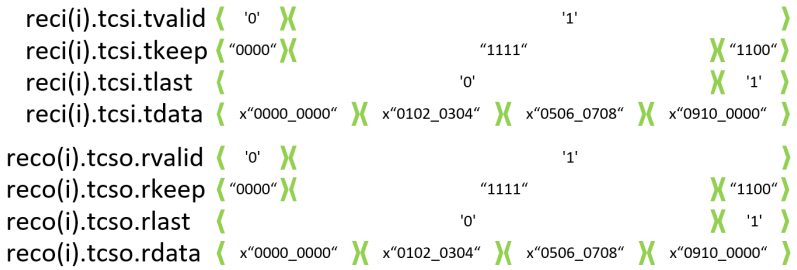


Figure 13.14: TCS interface to the UCF

Figure 13.15 shows the interface of the USP to the UCF. The different channels can be accessed via an array of records and only one USP at a time can write to the UCF and only data is taken to be transmitted if both the valid and ready signals are high at the same time. Ready signals on the output are ignored since there are

no buffers within the UCF and thus no data can be stored there. In this case UCF differs from the standard. For features like back pressure the veto signal shall be used which is valid only for the USP channels.

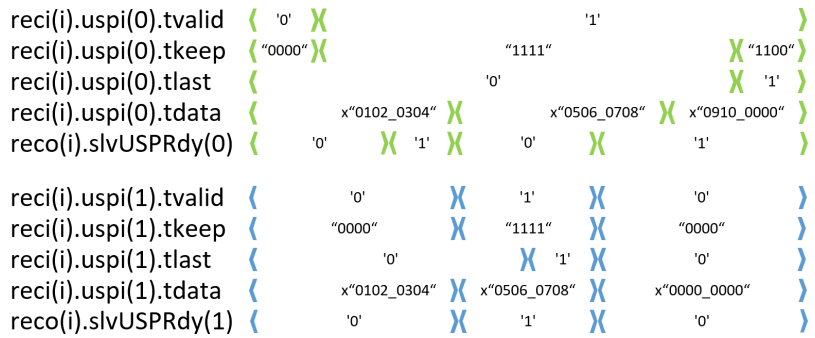


Figure 13.15: USP interface to the UCF

The veto signal can be accessed via the port ”reci(i).uspo_veto”. Each specific protocol has an entry in this veto array. If this signal turns from logic zero to logic one the UCF will send out the veto frame described in section 13.2.4. During the time it takes to transmit the veto to the counter part of the UCF the data stream will continue. Typically the latency for the veto frame is around 10 to 15 clock cycles of the user clock so this is the amount of data which would still need to be buffered on the output of UCF after the veto is set. Also, it will take this amount of clock cycles until the transmission of data will start again after resetting the veto. For data which is shown as valid by the valid flag but has no keep signal on logic high the UCF will introduce so called data fill bytes for each byte which has no keep signal along with the valid. On the user output these fill patterns will appear as zero bytes.

13.6 Example Projects

In the download of the UCF there are two example projects that can be used. One for the use with real hardware and the other one as a simulation verification.

13.6.1 Implementation

The implementation project for Vivado and the Xilinx Kintex7 UltraScale consists of a top module with integrated start up reset and the instantiation of the UCF and the reference clock changing module. Everything is packed into a generic so it can also be used for multiple instances of the UCF. Just by switching the ”cusCardPurpose” generic in the top module the user can switch between master and slave implementation.

13.6.2 Simulation

The simulation project for UVMM and the Questa simulator consists of a test bench instantiating a UCF master and a UCF slave and several AXI data stream generators provided with the UVVM tool. These stream generators are used to generate and verify data frames and their consistency after being transmitted via UCF. The default set up in the test bench generates one TCS channel and two USP channels going from the master to the slave.

13.7 References

The UCF is currently being used in several experiments already. The first experiment it was used in is the PENeLOPE experiment which is also part of this thesis.

The Belle II detector [31] at the KEK in Japan will be used for precision measurements of decay asymmetries in the heavy flavor sector. An important part of this experiment is the DEPFET pixel detector. It has 40 sensors consisting of 768x250 pixels each. Every sensor is then read out by one Data Handling Engine. Five of these are then connected via UCF to one Data Handling Concentrator. In the pixel detector read out the UCF is used for transmitting data, trigger and timing messages, and IPBus slow control messages.

The COMPASS experiment at CERN [3] is a high-energy physics experiment studying the hadron structure and making hadron spectroscopy with high intensity muon and hadron beams. Throughout the experiment several different types of detectors are used. For the read out of the TDC cards the UCF is used. Also, here it is used for transmitting data, trigger and timing messages, and IPBus slow control messages. The NA64 experiment at CERN also utilizes the same TDC cards and also the same UCF read out is used.

13.8 Installation

The UCF project is freely available on the LRZ Sync and Share (`https://syncandshare.lrz.de/dl/fiAwCPqFNqVZu1x7h6qn3CN2`) and is regularly updated. A change log is included with the download.

Chapter 14

Conclusions and Outlook

14.1 Conclusion of PENeLOPE

During the last years a lot of work on the way to a first neutron lifetime measurement with the PENeLOPE experiment has been achieved. Several of the superconducting coils for the trap have been extensively tested and also a first small bottle shaped coil assembly called PENeLOPE Light was successfully tested. For the UCN preparation and guiding system a new spin flipper was built and commissioned at the TRIGA reactor in Mainz. Additionally, a test setup for the central coil and the coil itself was constructed and tested. Furthermore, the complete electronics for the proton detector and the experiment control have been built and tested. In addition, all other necessary components for the actual construction of PENeLOPE have been ordered and, partly, have been built already.

14.2 Outlook

In the next months the Babcock Noell company who is manufacturing PENeLOPE will continue and finish the building process and deliver PENeLOPE as early as the end of 2019. The experiment will then be set up at the Maier Leibniz Laboratorium (MLL) in Garching for extensive tests. As a preparation for these test several changes of the gas system and cooling system at the MLL have to be made. The testing phase of PENeLOPE at the MLL shall last for about one year. After this period the experiment will be transported to the measurement facility. This will either be the Forschungsreaktor München 2 in Garching or the Institut Laue-Langevin in Grenoble.

14.3 Conclusion of iFDAQ

The intelligent FPGA data acquisition framework is a powerful tool for designing new or upgrading old data acquisition systems of experiments. During the last years several new software and hardware modules for the framework have been designed. These include new TDC cards with different resolutions, new ADC cards with different sampling speeds and a new multi purpose FPGA module with high computation power and high data throughput. Additionally, carrier cards have been designed for all the modules. On the software side a hardware event builder has been designed and a new inter FPGA communication protocol called UCF has been developed which combines several communication links into only one physical link.

14.4 Outlook of iFDAQ

In the next month the iFDAQ framework will be implemented in several different experiments and the developed cards shall be tested and qualified. Also, the UCF protocol will be made available for everyone. As a new development the FPGA cards shall be updated to the new GDDR6 memory standard in order to stay at the cutting edge of current technology.

14.5 Own Contributions

In this section I will list my own contributions to the PENeLOPE experiment and the iFDAQ framework. During my thesis I ...

- ... constructed a new spin flipper and qualified it during a beam test.
- ... extensively tested several outer, inner and stacks of the superconducting coils in CoTEx.
- ... designed and developed a test setup for the central coil.
- ... developed the electrical layout for PENeLOPE.
- ... built the electrical cabinets for PENeLOPE.
- ... developed the PLC firmware for PENeLOPE.
- ... developed the HMI for PENeLOPE.
- ... created the complete proton detector schematics.
- ... created the complete proton detector PCBs.
- ... developed the firmware for the proton detector (except the signal detection).
- ... qualified the proton detector read-out system.
- ... developed the new iFDAQ ADC modules.

- ... developed the new iFDAQ Kintex UltraScale Card.
- ... tested the new iFDAQ Kintex UltraScale Card.
- ... developed the Unified Communication Framework.
- ... implemented the Unified Communication Framework in several experiments (COMPASS, NA64, PENeLOPE, BELLE 2).

Acknowledgements

There are many people which deserve a special thanks and I apologize to all I might have forgotten in this list. Special thanks go to...

- ... Stephan Paul, for providing me the opportunity to work on these fantastic experiments.
- ... Rüdiger Picker, for hiring me in the very early days of my studies.
- ... Wolfgang Schreyer, for all the fun days together and pushing me to make everything ”smaller”.
- ... Andreas Frei, for supporting me on my experiments and physics related questions.
- ... Rainer Stöpler, for supporting me on the engineering side of PENeLOPE and much more.
- ... Igor Konorov and Stefan Huber, for supporting me on electronics related questions.
- ... Thomas Deuschle and the UCN hut, for supporting me in mechanical questions and the production of prototypes.
- ... Karin Frank, for supporting me on the whole bureaucracy.
- ... Christian Gorges, for his support during the beam time in Mainz.
- ... Thomas Pöschl, Dominik Steffen and Martin Losekamm, for keeping up my spirit and all the coffee breaks.

and especially to ...

- ... Veronika Schlosser, for keeping me up and supporting me during the hardest time of my PhD.
- ... Birgit and Hubert Gaisbauer, for supporting me in each and everything I did.

List of Figures

List of Tables

Bibliography

[1] *CASCADE-U*.

[2] *Reloop Dominance 702*.

[3] Y. Bai, M. Bodlak, V. Frolov, S. Huber, V. Jary, I. Konorov, D. Levit, J. Novy, D. Steffen, O. Subrt, and M. Virius. The daq debugger for ifdaq of the compass experiment. *International Journal of Mathematical, Computational, Physical, Electrical and Computer Engineering*, 11(12):498 – 506, 2017.

[4] Y Bai, M Bodlak, Vladimir Frolov, Vladimir Jary, Stefan Huber, I Konorov, D Levit, Josef Nový, Doug Steffen, and Miroslav Virius. Overview and future developments of the fpga-based daq of compass. *Journal of Instrumentation*, 11:C02025–C02025, 02 2016.

[5] W. Bothe and H. Becker. Künstliche erregung von kern-γ-strahlen. *Zeitschrift für Physik*, 66(5):289–306, May 1930.

[6] Luca Bottura. A practical fit for the critical surface of nbti. *IEEE transactions on applied superconductivity*, 10(1):1054–1057, 2000.

[7] J. Chadwick. Possible existence of a neutron. *Nature*, 129(3252):312–312, February 1932.

[8] Curie and Joliot. Emission de protons de grande vitesse par les substances hydrogenees sous l'influence des rayons gamma tres penetrants. *Comptes Rendus des Seances de l'Academie des Sciences*, 194(273), 1931.

[9] M. S. Dewey, D. M. Gilliam, J. S. Nico, F. E. Wietfeldt, X. Fei, W. M. Snow, G. L. Greene, J. Pauwels, R. Eykens, A. Lamberty, and J. Van Gestel. Measurement of the neutron lifetime using a proton trap. *Phys. Rev. Lett.*, 91:152302, Oct 2003.

[10] J. Döhner, H. Abele, I. Reichert, H. Borel, D. Dubbers, S.J. Freedman, and J. Last. Measurement of neutron-decay parameters with perkeo. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 284(1):123 – 126, 1989.

[11] Werner Erni. Manual/datasheet preamplier sp883d. Technical report, GSI, 2011.

[12] VF Ezhov, AZ Andreev, G Ban, BA Bazarov, P Geltenbort, AG Glushkov, VA Knyazkov, Nikolai Aleksandrovich Kovrizhnykh, GB Krygin, O Naviliat-

Cuncic, et al. Measurement of the neutron lifetime with ultracold neutrons stored in a magneto-gravitational trap. *JETP Letters*, 107(11):671–675, 2018.

[13] V.F. Ezhov, A.Z. Andreev, G. Ban, B.A. Bazarov, P. Geltenbort, F.J. Hartman, A.G. Glushkov, M.G. Groshev, V.A. Knyazkov, N.A. Kovrizhnykh, O. Naviliat-Cuncic, G.B. Krygin, A. Mueller, S. Paul, R. Picker, V.L. Ryabov, A. Serebrov, and O. Zimmer. Magnetic storage of ucn for a measurement of the neutron lifetime. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 611(2):167 – 170, 2009. Particle Physics with Slow Neutrons.

[14] Enrico Fermi et al. Motion of neutrons in hydrogenous substances. *Ricerca Scientifica*, 7(2):13–52, 1936.

[15] Robert Frazier, Greg Iles, Dave Newbold, and Andrew Rose. Software and firmware for controlling cms trigger and readout hardware via gigabit ethernet. *Physics Procedia*, 37:1892 – 1899, 2012. Proceedings of the 2nd International Conference on Technology and Instrumentation in Particle Physics (TIPP 2011).

[16] Andreas Frei. *Produktion von ultrakalten Neutronen mit einem festen Deuteriumkonverter*. Dissertation, Technische Universität München, München, 2008.

[17] Dominic Gaisbauer. Setup and tests of the rst coils of the neutron lifetime experiment penelope. Master's thesis, TUM, 2013.

[18] Dominic Gaisbauer. Development of the front-end electronics for the proton detection and design of the data acquisition for the penelope experiment. Master's thesis, TUM, 2015.

[19] P Geltenbort, L Göltl, R Henneck, K Kirch, A Knecht, M Kuźniak, B Lauss, T Lefort, A Mtchedlishvili, M Meier, et al. A compact, large-diameter adiabatic spinflipper for ultracold neutrons. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 608(1):132–138, 2009.

[20] R. Golub, P. Ageron, W. Mampe, and P. V. E. McLintock. *A 'Super-Thermal' Source for Ultra-Cold Neutrons*, pages 615–617. Springer US, Boston, MA, 1979.

[21] R. Golub, D. Richardson, and S.K. Lamoreaux. *Ultra-Cold Neutrons*. Taylor & Francis, 1991.

[22] Hamamatsu. Delivery specification sheet. Technical report, Hamamatsu, 2014.

[23] R Herdin, A Steyerl, AR Taylor, JM Pendlebury, and R Golub. Experiment on the efficient polarization of ultracold neutrons. *Nuclear Instruments and Methods*, 148(2):353–357, 1978.

[24] Ekbert Hering. *Elektronik für Ingenieure und Naturwissenschaftler*. Springer, 2014.

[25] Adam T Holley, LJ Broussard, JL Davis, K Hickerson, TM Ito, C-Y Liu, JTM Lyles, M Makela, RR Mammei, MP Mendenhall, et al. A high-field adiabatic fast passage ultracold neutron spin flipper for the ucna experiment. *Review of Scientific Instruments*, 83(7):073505, 2012.

[26] Supercon Inc. Certificate of compliance, wire lot no. 412-e11, sc-vsf-7400, 2016.

[27] National Instruments. Compactrio. Web.

[28] J. Karch, Yu. Sobolev, M. Beck, K. Eberhardt, G. Hampel, W. Heil, R. Kieser, T. Reich, N. Trautmann, and M. Ziegner. Performance of the solid deuterium ultra-cold neutron source at the pulsed reactor triga mainz. *The European Physical Journal A*, 50(4):78, Apr 2014.

[29] I. Konorov, H. Angerer, A. Mann, and S. Paul. Soda: Time distribution system for the panda experiment. In *2009 IEEE Nuclear Science Symposium Conference Record (NSS/MIC)*, pages 1863–1865, Oct 2009.

[30] Thorsten Lauer. private communication, 2013.

[31] K. Lautenbach, B. Deschamps, J. Dingfelder, D. Getzkow, T. Geßler, I. Konorov, W. Kühn, S. Lange, D. Levit, Z.-A. Liu, C. Marinas, D. Münchow, A. Rabusov, S. Reiter, B. Spruck, C. Wessel, and J. Zhao. The belle II pixel detector data acquisition and background suppression system. *Journal of Instrumentation*, 12(06):C06023–C06023, jun 2017.

[32] A. B. Mann, I. Konorov, H. Angerer, M. Krämer, S. Huber, B. Grube, J. Friedrich, B. Ketzer, S. Uhl, F. Haas, A. Dinkelbach, S. Grabmüller, and S. Paul. The universal sampling adc readout system of the compass experiment. In *2009 IEEE Nuclear Science Symposium Conference Record (NSS/MIC)*, pages 2225–2228, Oct 2009.

[33] Bastian Märkisch. Perc–a clean, bright and versatile source of neutron decay products. *Verhandlungen der Deutschen Physikalischen Gesellschaft*, 2010.

[34] Yasuhiro Masuda, Kichiji Hatanaka, Sun-Chan Jeong, Shinsuke Kawasaki, Ryohei Matsumiya, Kensaku Matsuta, Mototsugu Mihara, and Yutaka Watanabe. Spallation ultracold neutron source of superfluid helium below 1 k. *Phys. Rev. Lett.*, 108:134801, Mar 2012.

[35] Stefan Materne. *Tests of prototype magnets and study on a MCP based proton detector for the neutron lifetime experiment PENeLOPE*. Dissertation, Technische Universität München, München, 2013.

[36] B. Märkisch, H. Abele, D. Dubbers, F. Friedl, A. Kaplan, H. Mest, M. Schumann, T. Soldner, and D. Wilkin. The new neutron decay spectrometer perkeo iii. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 611(2):216 – 218, 2009. Particle Physics with Slow Neutrons.

[37] Jeffrey S. Nico and W. Michael Snow. Fundamental neutron physics. *Annual Review of Nuclear and Particle Science*, 55(1):27–69, 2005.

[38] RW Pattie, NB Callahan, C Cude-Woods, ER Adamek, Leah J Broussard, SM Clayton, SA Currie, EB Dees, Xinjian Ding, EM Engel, et al. Measurement of the neutron lifetime using a magneto-gravitational trap and in situ detection. *Science*, 360(6389):627–632, 2018.

[39] Stephan Paul. The Neutron and the Universe - History of a Relationship. *PoS*, BORMIO2012:025, 2012.

[40] A Pichlmaier, V Varlamov, K Schreckenbach, and P Geltenbort. Neutron lifetime measurement with the ucn trap-in-trap mambo ii. *Physics Letters B*, 693(3):221–226, 2010.

[41] Maxim Pospelov and Josef Pradler. Big bang nucleosynthesis as a probe of new physics. *Annual Review of Nuclear and Particle Science*, 60(1):539–568, 2010.

[42] J. Reich, H. Abele, M.Astruc Hoffmann, S. Baeßler, P.v. Bülow, D. Dubbers, V. Nesvizhevsky, U. Peschke, and O. Zimmer. A measurement of the beta asymmetry in neutron decay with perkeo ii. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 440(3):535 – 538, 2000.

[43] Samtec. Firefly aktiv-optische mikro flyover kabelkonfektion. Web.

[44] Wolfgang Schreyer. Personal communication, 2018.

[45] Wolfgang Sebastian Schreyer. *Magnets, polarizers, systematics, and optimizations of the neutron-lifetime experiment PENeLOPE*. Dissertation, Technische Universität München, München, 2017.

[46] Andreas Senft. Cotex 2.0 - a new coil test experiment. Master's thesis, TUM, 2011.

[47] A Serebrov, V Varlamov, A Kharitonov, A Fomin, Yu Pokotilovski, P Geltenbort, J Butterworth, I Krasnoschekova, M Lasakov, R Tal'daev, et al. Measurement of the neutron lifetime using a gravitational trap and a low-temperature fomblin coating. *Physics Letters B*, 605(1-2):72–78, 2005.

[48] AP Serebrov, EA Kolomensky, AK Fomin, IA Krasnoshchekova, AV Vassiljev, DM Prudnikov, IV Shoka, AV Chechkin, ME Chaikovskiy, VE Varlamov, et al. Neutron lifetime measurements with a large gravitational trap for ultracold neutrons. *Physical Review C*, 97(5):055503, 2018.

[49] Jochen Steinman. Progress report quench protection. techreport, BNG, 2011.

[50] A. Steyerl. A "neutron turbine" as an efficient source of ultracold neutrons. *Nuclear Instruments and Methods*, 125(3):461 – 469, 1975.

[51] Albert Steyerl, JM Pendlebury, Charles Kaufman, Surendra S Malik, and AM Desai. Quasielastic scattering in the interaction of ultracold neutrons with a liquid wall and application in a reanalysis of the mambo i neutron-lifetime experiment. *Physical Review C*, 85(6):065503, 2012.

[52] M. Tanabashi, K. Hagiwara, K. Hikasa, K. Nakamura, Y. Sumino, F. Takahashi, J. Tanaka, K. Agashe, G. Aielli, C. Amsler, M. Antonelli, D. M. Asner, H. Baer,

Sw. Banerjee, R. M. Barnett, T. Basaglia, C. W. Bauer, J. J. Beatty, V. I. Belousov, J. Beringer, S. Bethke, A. Bettini, H. Bichsel, O. Biebel, K. M. Black, E. Blucher, O. Buchmuller, V. Burkert, M. A. Bychkov, R. N. Cahn, M. Carena, A. Ceccucci, A. Cerri, D. Chakraborty, M.-C. Chen, R. S. Chivukula, G. Cowan, O. Dahl, G. D'Ambrosio, T. Damour, D. de Florian, A. de Gouvêa, T. DeGrand, P. de Jong, G. Dissertori, B. A. Dobrescu, M. D'Onofrio, M. Doser, M. Drees, H. K. Dreiner, D. A. Dwyer, P. Eerola, S. Eidelman, J. Ellis, J. Erler, V. V. Ezhela, W. Fetscher, B. D. Fields, R. Firestone, B. Foster, A. Freitas, H. Gallagher, L. Garren, H.-J. Gerber, G. Gerbier, T. Gershon, Y. Gershtein, T. Gherghetta, A. A. Godizov, M. Goodman, C. Grab, A. V. Gritsan, C. Grojean, D. E. Groom, M. Grünewald, A. Gurtu, T. Gutsche, H. E. Haber, C. Hanhart, S. Hashimoto, Y. Hayato, K. G. Hayes, A. Hebecker, S. Heinemeyer, B. Heltsley, J. J. Hernández-Rey, J. Hisano, A. Höcker, J. Holder, A. Holtkamp, T. Hyodo, K. D. Irwin, K. F. Johnson, M. Kado, M. Karliner, U. F. Katz, S. R. Klein, E. Klempt, R. V. Kowalewski, F. Krauss, M. Kreps, B. Krusche, Yu. V. Kuyanov, Y. Kwon, O. Lahav, J. Laiho, J. Lesgourgues, A. Liddle, Z. Ligeti, C.-J. Lin, C. Lippmann, T. M. Liss, L. Littenberg, K. S. Lugovsky, S. B. Lugovsky, A. Lusiani, Y. Makida, F. Maltoni, T. Mannel, A. V. Manohar, W. J. Marciano, A. D. Martin, A. Masoni, J. Matthews, U.-G. Meißner, D. Milstead, R. E. Mitchell, K. Mönig, P. Molaro, F. Moortgat, M. Moskovic, H. Murayama, M. Narain, P. Nason, S. Navas, M. Neubert, P. Nevski, Y. Nir, K. A. Olive, S. Pagan Griso, J. Parsons, C. Patrignani, J. A. Peacock, M. Pennington, S. T. Petcov, V. A. Petrov, E. Pianori, A. Piepke, A. Pomarol, A. Quadt, J. Rademacker, G. Raffelt, B. N. Ratcliff, P. Richardson, A. Ringwald, S. Roesler, S. Rolli, A. Romaniouk, L. J. Rosenberg, J. L. Rosner, G. Rybka, R. A. Ryutin, C. T. Sachrajda, Y. Sakai, G. P. Salam, S. Sarkar, F. Sauli, O. Schneider, K. Scholberg, A. J. Schwartz, D. Scott, V. Sharma, S. R. Sharpe, T. Shutt, M. Silari, T. Sjöstrand, P. Skands, T. Skwarnicki, J. G. Smith, G. F. Smoot, S. Spanier, H. Spieler, C. Spiering, A. Stahl, S. L. Stone, T. Sumiyoshi, M. J. Syphers, K. Terashi, J. Terning, U. Thoma, R. S. Thorne, L. Tiator, M. Titov, N. P. Tkachenko, N. A. Törnqvist, D. R. Tovey, G. Valencia, R. Van de Water, N. Varelas, G. Venanzoni, L. Verde, M. G. Vincter, P. Vogel, A. Vogt, S. P. Wakely, W. Walkowiak, C. W. Walter, D. Wands, D. R. Ward, M. O. Wascko, G. Weiglein, D. H. Weinberg, E. J. Weinberg, M. White, L. R. Wiencke, S. Willocq, C. G. Wohl, J. Womersley, C. L. Woody, R. L. Workman, W.-M. Yao, G. P. Zeller, O. V. Zenin, R.-Y. Zhu, S.-L. Zhu, F. Zimmermann, P. A. Zyla, J. Anderson, L. Fuller, V. S. Lugovsky, and P. Schaffner. Review of particle physics. *Phys. Rev. D*, 98:030001, Aug 2018.

[53] Linear Technology. *LTC1407/LTC1407A - Serial 12-Bit/14-Bit, 3Msps Simultaneous Sampling ADCs with Shutdown*. Linear Technology, 2019.

[54] Christian Tietze. Entwicklung eines detektors zum nachweis der protonen aus dem beta-zerfall des neutrons, 2009.

[55] UVVM. Uvvm. Github, 2019.

[56] Xilinx. *Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics*. Xilinx.

[57] Xilinx. *UltraScale Architecture GTH Transceivers*.

[58] A. T. Yue, M. S. Dewey, D. M. Gilliam, G. L. Greene, A. B. Laptev, J. S. Nico, W. M. Snow, and F. E. Wietfeldt. Improved determination of the neutron lifetime. *Phys. Rev. Lett.*, 111:222501, Nov 2013.