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To cite this article: Simon Pfaehler *et al* 2019 *Nanotechnology* **30** 395201

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Space charge-limited current transport in thin films of alkyl-functionalized silicon nanocrystals

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Received 8 March 2019, revised 26 May 2019

Accepted for publication 24 June 2019

Published 15 July 2019



CrossMark

Abstract


We describe the fabrication and electrical characterization of all-silicon electrode devices to study the electronic properties of thin films of silicon nanocrystals (SiNCs). Planar, highly doped Si electrodes with contact separation of 200 nm were fabricated from silicon-on-insulator substrates, by combination of electron beam lithography and reactive ion etching. The gaps between the electrodes of height 110 nm were filled with thin-films of hexyl functionalized SiNCs (diameter 3 nm) from colloidal dispersions, via a pressure-transducing PDMS (polydimethylsiloxane) membrane. This novel approach allowed the formation of homogeneous SiNC films with precise control of their thickness in the range of 15–90 nm, practically without any voids or cracks. The measured conductance of the highly resistive SiNC films at high bias voltages up to 60 V scaled approximately linearly with gap width (5–50 μm) and gap filling height, with little device-to-device variance. We attribute the observed, pronounced hysteretic current–voltage (I – V) characteristics to space-charge-limited current transport, which—after about twenty cycles—eventually blocks the current almost completely. We propose our all-silicon device scheme and gap filling methodology as a platform to investigate charge transport in novel hybrid materials at the nanoscale, in particular in the high resistivity regime.

Supplementary material for this article is available [online](#)

Keywords: space charge-limited current transport, silicon nanocrystals, alkyl-functionalized, silicon electrodes, thin film, gap filling, PDMS membrane

(Some figures may appear in colour only in the online journal)

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1. Introduction

Semiconductor nanoparticles and nanocrystals (NCs) have gained much significance in electronics and optoelectronics, ranging from fundamental studies on the intriguing transport phenomena in NC arrays to applications in thin-film transistor devices, photovoltaic devices, LEDs, [1, 2] and as fluorescent labels [3]. Among the variety of semiconductor materials under investigation silicon has adopted a particular role due to its dominating relevance in microelectronics, its abundance and low toxicity [4]. Silicon nanocrystals (SiNCs) show distinct optical properties such as size-tunable photoluminescence (PL) in the visible range with high quantum yields when their size is reduced below the Bohr radius of Si ($d < 5$ nm) [5–7]. For this reason, photoluminescent SiNCs have evolved as promising material for electronic and optoelectronic applications, including, e.g. (electroluminescent) synaptic devices [8, 9]. In order to prevent oxidation of the SiNCs surface as well as to control their (opto-) electronic properties, a well-tailored surface functionalization is essential [10, 11]. Methods to synthesize SiNCs and functionalize their surfaces with a variety of different molecules are well developed [12, 13], as predominantly demonstrated in optical studies [14–16].

For *electrical device* applications covering for example novel (ultra) thin-film transistors, sensors or non-volatile memories, based on hybrid inorganic-organic 2D or 3D networks of functionalized SiNCs, the characterization and understanding of their electronic transport properties is mandatory [17, 18]. The group of Kortshagen has reported electrical data, mostly focusing on alkyl-functionalized, doped SiNC networks [19]. The systematic investigation of *undoped* SiNCs which are functionalized with aliphatic (electrically insulating) molecules poses a particular challenge on the experimental realization: (1) due to the high resistance of the SiNC films, the spacing between the electrical contacts needs to be small (100 nm regime), (2) the space between the contacts (gap) needs to be filled with the SiNC material in a controlled, homogeneous and reproducible manner, and (3) the electrode contact material has to be inert, both chemically and physically with respect to the high electric fields that need to be applied. This way, artifacts arising from, e.g. electromigration of metal ions from the contacts into the SiNC film [20] shall be excluded.

Here, we report on the electrical characterization of films of hexyl functionalized SiNCs (Hex-SiNCs, $d \sim 3$ nm) [21], filled into 200 nm long and 110 nm high trench-like gaps, which separate pairs of degenerately doped Si contact electrodes (see figure 1(f), for the definition of the gap dimensions ‘width’ and ‘length’). Using a newly developed PDMS (polydimethylsiloxane) -based pressure technique related to solution micromolding fabrication processes [22], we achieved a high level of control over the film thickness within the trench, ranging from about 15–90 nm (almost complete filling). The obtained electrical transport data, carried out in the high voltage range up to 60 V, directly reveal the monotonic, practically linear dependence of current with respect to

gap width and filling level. A pronounced hysteretic current–voltage (I – V) characteristic points to a dominating space-charge-limited current transport mechanism in Hex-SiNC films. Our demonstrated Si electrode fabrication technique combined with the controlled gap filling method can serve as a platform for the electrical characterization of nm-thin films comprising different NCs passivated with various functional organic groups.

2. Experimental methods

The process of Si device fabrication and filling the active gap region between the contacts with a thin film of Hex-SiNCs is outlined in figure 1. Starting from a silicon-on-insulator (SOI) wafer with a highly doped top Si device layer (a), gap-separated electrodes were fabricated by using electron beam lithography (EBL) and reactive ion etching (RIE), after electrical contact metallization using conventional photolithography and physical vapor deposition (PVD) had been realized (b). At this stage, the device was ready to investigate the electrical properties of the material (here: Hex-SiNCs) to be filled into the gap—with the highly doped Si surfaces acting as electrical contacts in a two-terminal configuration [23–26]. We devoted much effort to the controlled and reproducible filling of the gap with SiNCs. Few procedures have been reported in literature, demonstrating the filling of (metallic) nanoscale trenches by different approaches [27, 28]. We tried several alternative methods, such as spin coating, drop casting or solvent evaporation to fill the gaps. However, none of these techniques led to satisfying filling with a homogeneous thin film of SiNCs. By far, the best results were obtained by mechanically pressing the SiNCs from solution into the gap, employing a pressure-transducing PDMS membrane (see figures 1(c)–(e)). This novel approach, particularly developed for this purpose, turned out to enable the formation of homogeneous Hex-SiNC thin films with precise control of thickness, practically without any voids or cracks in-between the Si electrodes. To achieve this, the native oxide on the Si electrode surface was first removed chemically by using hydrofluoric acid (HF). Immediately afterwards, a solution of Hex-SiNCs was drop-casted onto the chip surface (figure 1(c)) and mechanically pushed into the trench by application of a pressure-transducing PDMS membrane (d) which was subsequently removed (e). The final device structure featuring its gap filled with Hex-SiNCs was then ready for electrical characterization (f).

2.1. Preparative methods

2.1.1. Fabrication of silicon electrodes. Silicon electrodes were fabricated from SOI wafers (Soitec, France), composed of a (110 ± 7.5) nm thin silicon device layer (100) separated by a (200 ± 5) nm buried silicon dioxide (SiO_2) layer from the silicon handle wafer (100). The top silicon layer was heavily p-doped by ion implantation (p^+ , Boron, doping concentration ca $5 \times 10^{19} \text{ cm}^{-3}$). The SOI wafers were diced

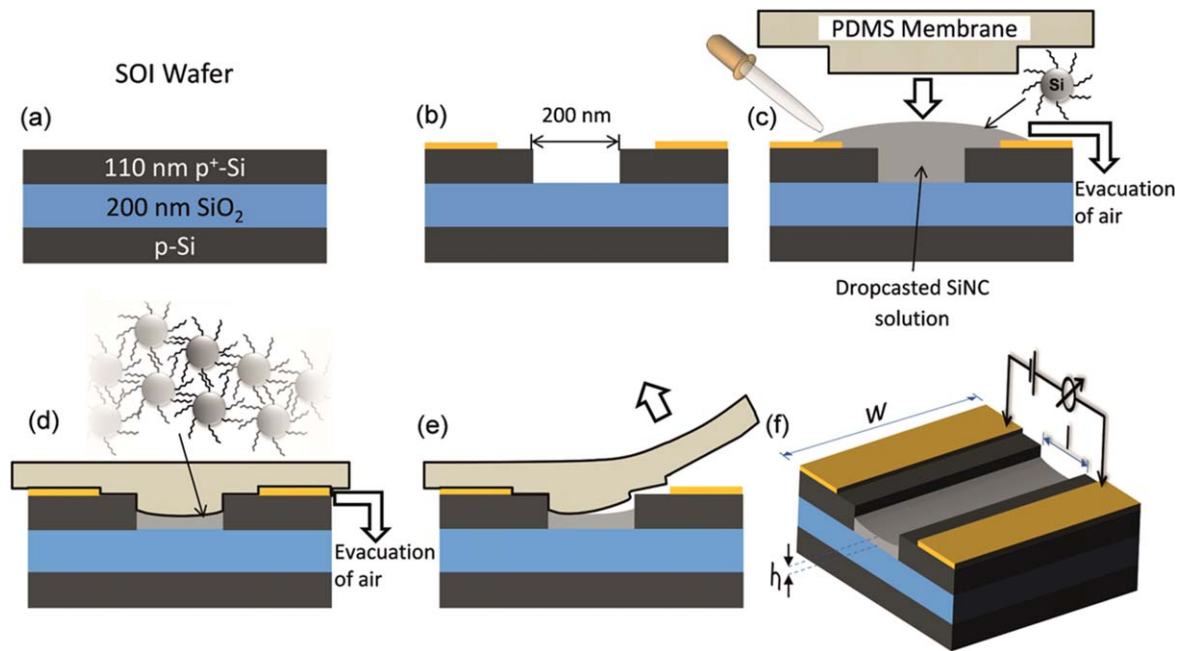


Figure 1. Schematic representation of device fabrication and trench filling with Hex-SiNCs. (a) SOI starting material. (b) Fabrication of Si electrodes by electron beam lithography and reactive ion etching, combined with optical lithography and metal deposition for probe contacts (yellow). The latter are located far away from the gap (μm distance, sketch not to scale). (c)–(e) Filling the gap between electrodes with a thin film of Hex-SiNCs by mechanically pressing the Hex-SiNCs from solution via a pressure-transducing PDMS membrane. (f) Final device structure for electrical characterization. Dimensions of the film are indicated as w (width), l (length) and h (height).

in $8 \times 8 \text{ mm}^2$ sample chips. For the fabrication of an array of electrode pairs (figure S11, available online at stacks.iop.org/NANO/30/395201/mmedia, supporting information), the SOI sample chips were first cleaned by sonicating them in acetone (VLSI Selectipur, BASF), subsequent sonicating them in isopropanol (VLSI Selectipur, BASF) and blowing them dry under a stream of N_2 , followed by an additional cleaning step in oxygen plasma (180 s, 400 W). We used conventional photo-lithography to pattern the etching mask for the mesa-structure of the electrodes array: At first, an adhesion promoter hexamethyldisilazane (HMDS, Aldrich Chemistry) and a positive-tone photo resist (AZ5214E, MicroChemicals) were deposited by spin-coating (film thickness: $1.6 \mu\text{m}$). Following resist development (AZ351B, 1:4 diluted with DI H_2O , MicroChemicals) and an additional oxygen plasma treatment to remove adhesion promoter and resist residues (180 s, 400 W), the mesa-structure was etched in the top silicon device layer down to the buried oxide by RIE ($\text{SF}_6/\text{C}_4\text{F}_8$ plasma, OXFORD Instruments, Plasma Lab 80 Plus). In that way, we produced an electrically conductive lead structure comprising an array of ten top silicon layer bars of widths w ranging from 5 to $200 \mu\text{m}$, which are electrically separated from each other and act as the basis for the later fabricated electrode arrays. After the RIE step, the remaining resist was removed in a subsequent ultrasonic bath of acetone, followed by rinsing in isopropanol and dry-blowing with N_2 .

To provide ohmic contact to the highly doped Si lead structures we fabricated a row of Ti/Au metallic contact pads on top of the Si layer. These pads of area $200 \times 200 \mu\text{m}^2$ were prepared by a combination of photo-lithography (positive photo resist AZ5214E, MicroChemicals), a short

dip in diluted HF (5%, 30 s) to remove the native oxide, and subsequent PVD of 10/100 nm Ti/Au (Leybold L560, max 0.2 nm s^{-1}), followed by lift-off in an acetone bath, rinsing in isopropanol and dry-blowing with N_2 .

EBL was used to prepare the etching mask for gap fabrication. After cleaning the samples by sonication in acetone (10 min), followed by sonicating them in isopropanol and dry-blowing with N_2 , and an additional cleaning step in oxygen plasma (60 s, 400 W) the sample chips were coated with positive-tone EBL resist (80 nm, AR-P 6200, Allresist) and exposed in an EBL system (30 kV acceleration voltage, e_LINE, Raith). After developing (60 s, AR 600–546, Allresist) the samples were baked on a hotplate at $130 \text{ }^\circ\text{C}$ for 60 s to improve the etching stability of the EBL resist. The resulting resist gap pattern was transferred into the top Si layer by RIE as previously described, eventually resulting in gaps in the silicon mesa (see figure 1(b) and figure S11, one between each pair of metal pads). In this way, each top silicon layer bar of the mesa was split in ten electrode pairs resulting in an array of 100 electrode pairs in total, on each sample. The remaining e-beam resist was removed by subsequent sonication in acetone and isopropanol plus the additional application of an oxygen plasma (5 min, 400 W).

2.1.2. Synthesis of hexyl functionalized SiNCs. Preparation of SiNCs embedded in SiO_2 like matrix started from the synthesis of polymeric hydrogen silsesquioxane (HSQ), based on a literature-known procedure [29]. To obtain free-standing hydride-terminated SiNCs, we applied a synthetic procedure which was recently described in detail [30].

Surface functionalization of the obtained SiNCs with hexyl groups was performed with organolithium reagents, as

we have reported before [21]. Freshly etched hydride-terminated SiNCs (from 300 mg Si/SiO₂ composite) were dispersed in 2 ml dry toluene and transferred to a Schlenk flask equipped with a stir bar. The dispersion was degassed via three freeze-thaw cycles. *n*-hexyllithium (0.2 mmol, from 2.3 M solution in hexane) was added. Upon addition of *n*-hexyllithium, the color of the reaction mixture turned dark brown. The reaction mixture was stirred at room temperature for 15 h under argon atmosphere. Functionalized SiNCs were precipitated in 5 ml 1:1 ethanol–methanol mixture, acidified with HCl conc. (0.2 ml) to terminate the reaction. SiNCs were centrifuged at 9000 rpm for 5 min and the sediment was redispersed in minimum amount of toluene. The precipitation-centrifugation-redispersion cycle was repeated two more times from toluene and ethanol-methanol. At the end of purification steps, functionalized SiNCs were dispersed in 2 ml toluene and filtered through a 0.45 μm PTFE syringe filter. This method assures a controlled, less dense monolayer coverage on the SiNC surface, unlike many other conventional surface functionalization techniques [31].

2.1.3. Filling the gap between Si electrodes with hex-SiNCs.

To fill the obtained Hex-SiNCs as thin films into the gaps separating the Si electrodes, solutions of different concentration of Hex-SiNCs in toluene were prepared and tested, ranging from ~5 mg ml⁻¹ to 20 mg ml⁻¹. The samples were first cleaned by sonication in acetone (10 min, VLSI Selectipur, BASF), subsequent sonication in isopropanol (VLSI Selectipur, BASF) and dry-blowing with N₂, followed by a short dip in diluted HF (2%, 30 s) to remove the native oxide from the silicon electrodes' surface, right before the coating with Hex-SiNCs solution. Next, about 70 μl Hex-SiNC solution was immediately drop-casted onto the sample covering the complete surface. We used a custom-made device originally designed for nano-imprint lithography to mechanically press the Hex-SiNC solution via a pressure-transducing PDMS membrane into the gaps. The membrane was fabricated by mixing base and curing agent (Sylgard 184 silicon elastomer kit, Dow Corning) in a weight ratio of 5:1, evacuating the mixture in a desiccator to remove air bubbles and curing it for 48 h at room temperature. In order to mechanically press the Hex-SiNC solution into the gaps, the volume between the PDMS membrane and the wetted sample surface was evacuated by a standard membrane vacuum pump, such that the PDMS membrane got into close contact with the sample surface. Thus, the solvent of the drop-casted Hex-SiNC solution on the sample was removed mainly by pumping but also to a little amount by being soaked by the PDMS membrane while mechanically pressing the Hex-SiNCs as a thin film into the gap separating the electrodes. No remaining solvent could be observed after 4 min of evacuation and having carefully released the PDMS membrane from the sample surface. For every sample we used a newly prepared, fresh piece of the same PDMS membrane. After release, the samples were heated on a hotplate to 100 °C for 60 s to evaporate remaining residues of the solvent. To investigate the quality and filling height of the

Hex-SiNC thin film in the gap between electrodes, we used reference samples based on the same SOI material and fabricated a set of six very wide ($w \approx 7$ nm, $l = 200$ nm) gaps per reference sample by e-beam lithography and RIE using the same fabrication and PDMS membrane coating protocol as for the gap electrodes array samples described before. All reference samples were coated with Hex-SiNC solutions from the same batch that was used for the coating of the gap electrode samples.

2.2. Characterization methods

2.2.1. Characterization of Hex-SiNCs. Upon surface functionalization, presence of hexyl groups on the SiNC surface was observed via FTIR (Fourier-Transform Infrared) spectroscopy (figure S12(a)). Presence of alkyl peaks between 2850 and 2955 cm⁻¹ (CH₂ and CH₃ v-stretching) and at ~1462 and ~1378 cm⁻¹ (CH δ-deformation) is a good indication for a successful reaction [21]. The spectrum also shows signals assigned for Si–H groups at ~2100, 906 and 660 cm⁻¹, together with minor oxidation evidenced by the Si–O band at 1050 cm⁻¹. The FTIR spectrum was collected with a Bruker Vertex 70 FTIR using a Platinum ATR from Bruker.

Transmission electron microscopy (TEM) revealed an average SiNC size (diameter) of 3.1 ± 0.2 nm (figure S12(b)). A histogram showing the size distribution is provided (figure S12(c)). The mean and standard deviation was calculated by measuring the size of 300 SiNCs. Bright field TEM images were obtained using a JEOL-2012 electron microscope equipped with LaB6 filament and operated at an acceleration voltage of 200 kV.

2.2.2. Atomic force microscopy. AFM images were taken with a Dimension V (Bruker/Veeco) AFM in tapping mode equipped with a silicon tip, coated with a diamond-like-carbon-coating (TAP190DLC, BudgetSensors). Scan rate was typically 1 Hz. Images were analyzed using the NanoScope Analysis 1.5 software (Bruker).

2.2.3. X-ray photoelectron spectroscopy. X-ray photoelectron spectroscopy (XPS) measurements were carried out in a home-built setup (parts from SPECS Surface Nano Analysis) under ultra-high vacuum (~6 × 10⁻⁹ mbar). The setup is equipped with an XR 50 x-ray source and a Phoibos 100 hemispherical electron analyzer. An aluminum anode was utilized, generating x-ray photons of the energy of the Al K_α edge ($E = 1486.6$ eV). The x-ray source was operated at a voltage of 12.50 kV and an emission current of 20.0 mA. Photoelectron spectra were acquired at an energy resolution of 0.1 eV and a dwell time of 1 s and averaged over two to four scan repetitions. A pass energy of 30 eV was used universally. XPS data were analyzed with CasaXPS software (www.casaxps.com; charge referencing, background subtraction and elemental analysis) and Origin (intensity normalization and plotting). The spectra were charge-referenced with respect to the C 1s hydrocarbon peak at 284.8 eV and corrected for analyzer transmission and photoelectron escape depth. For quantitative analysis and

normalization, relative sensitivity factors (Scofield cross-sections [32]) for each peak were retrieved from the CasaXPS library, accounting for the effective photoionization cross-section of the associated electronic transition. As reference samples for the XPS measurements, planar silicon substrates covered with ~ 100 nm titanium oxide (TiO_x) were used. They were coated with Hex-SiNC thin films, analog to the gap separated Si electrode samples.

2.2.4. Electrical characterization. For electrical characterization, the finished sample devices were mounted in a vacuum probe station (TTPX, LakeShore), without delay. All electrode pairs were electrically characterized in darkness at room temperature, at a base pressure of 10^{-5} – 10^{-6} mbar, by contacting the metal pads of each device with beryllium-copper probe needles. DC I – V curves were measured at a scan rate of about 150 mV s $^{-1}$ using a source meter (Keithley 2635B) controlled by a PC (Matlab software).

3. Results and discussion

In advance to electrical characterization, we have studied in detail to what extent the Hex-SiNCs film thickness between silicon electrodes can be controlled using our pressure-transducing PDMS membrane technique. In fact, the level of gap filling can be efficiently adjusted by the concentration of SiNCs in solution.

As shown in the scanning electron microscopy (SEM) cross-sectional images of figure 2, the thin-film thickness (h) in the gap increases monotonically with the solution concentration of the Hex-SiNCs, which was varied from $c = 5, 10, 15$ – 20 mg ml $^{-1}$ (figures 2(b)–(e), respectively). In general, the film shape adopted a concave form inside the gap. Here, we determined the (minimum) film thicknesses h from measuring in the middle of the cross section of the gap, as depicted in figure 1(f). Figure 2(f) summarizes the measured film thickness as function of Hex-SiNC solution concentration, starting from a thin film with $h \sim (15 \pm 3)$ nm up to an almost completely filled gap with $h = (92 \pm 8)$ nm. All resulting Hex-SiNC thin films filled the gap in a homogeneous manner, practically free from voids or cracks in the film or close to the interface to the electrodes: out of 80 examined cross-sections only one void was observed, and no cracks at all. This is an important requirement for stable and reproducible electrical measurements.

In order to obtain insight into the Hex-SiNC film composition, we measured the relative ratios of silicon to carbon in the Hex-SiNC thin films on planar surfaces, using XPS. For all films prepared from different solution concentrations, the measured Si-to-C ratios were in the range 87%–91%, hence showed very little variation (see, figure S13 and table S11). While a comparison of SiNC density for the different films cannot be derived from these results alone, still the composition of the organically functionalized SiNCs within each film neither did change as function of concentration nor was affected by the filling process, which is essential for comparing films of different thickness in electrical characterization.

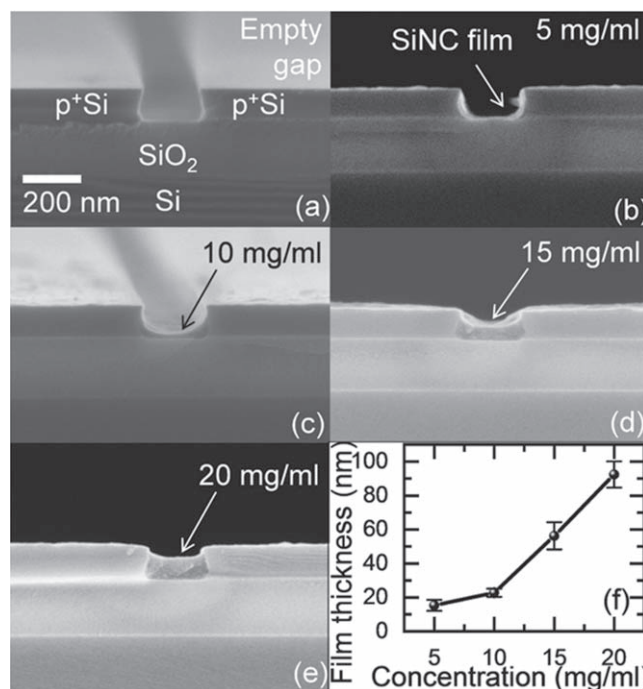


Figure 2. (a)–(e) SEM cross sections of Si gaps filled with thin films of Hex-SiNCs prepared from increasing solution concentrations, resulting in increasing thin film thicknesses. (f) Averaged thin film thicknesses as a function of Hex-SiNC concentration, measured in filled 200 nm gaps. All film thicknesses were obtained from averaging the measurement results of at least six test structures comprising wide (mm scale) trenches, for each Hex-SiNC solution concentration.

Small residuals of PDMS could be identified by XPS, which can be assigned to the membrane-based preparation process. These are most likely located at the surface of the thin films and would therefore not affect the charge transport properties of the Hex-SiNCs networks. No distinct presence of SiO_2 indicative of SiNC oxidation could be resolved by XPS (see supporting information).

We characterized the prepared Hex-SiNC films of different filling height h electrically, by measuring the DC I – V characteristics across the filled gaps. All gaps were of length (206 ± 11) nm, while their widths varied from 5 to 50 μm . Before measuring the coated samples, all devices were pre-characterized in their as-fabricated state, i.e. without any Hex-SiNC film filling. Only those fabricated devices with measured currents less than 1 pA at an applied voltage of 30 V (i.e. with insulating gap) were taken into further consideration for filling with Hex-SiNC films (see figure 3(a), gray curve, for such a reference measurement).

Figure 3(a) summarizes the I – V characteristics of the investigated devices ($w = 20$ μm) filled with SiNC films, prepared from Hex-SiNCs solution concentrations 5, 10 and 20 mg ml $^{-1}$ that resulted in thin film thicknesses of about $h = 15, 23$ and 92 nm, respectively. After filling the gaps with these thin films, all devices showed a pronounced non-linear increase in current with increasing voltage, when compared to the empty, insulating device directly after fabrication. With increasing thin film thickness, a larger current

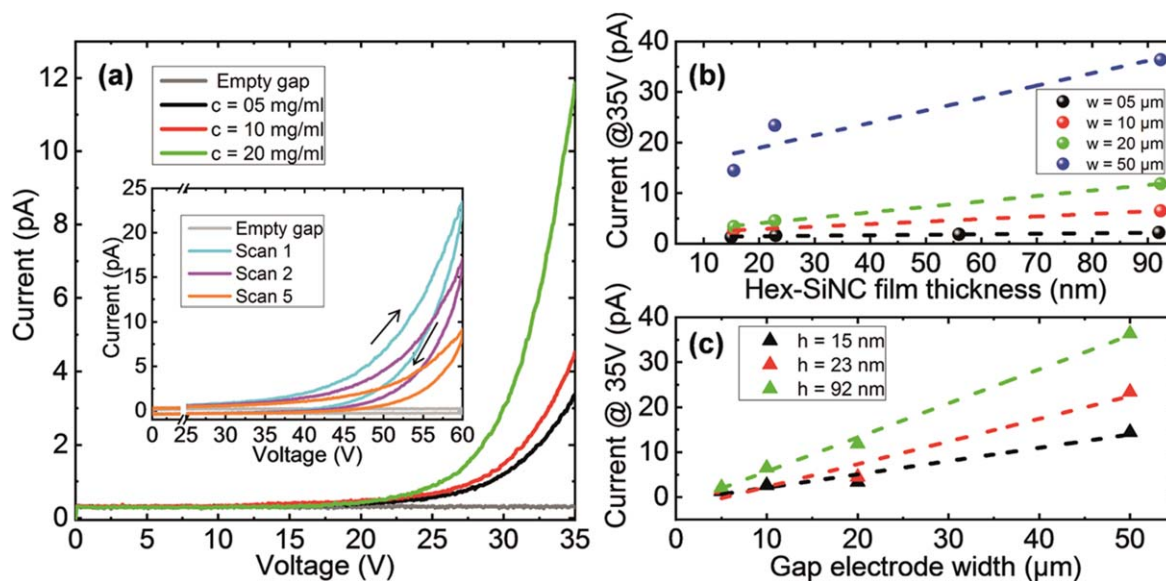


Figure 3. (a) Current–voltage characteristics for devices with $w = 20 \mu\text{m}$, filled with films of Hex-SiNCs that were prepared from different solution concentrations. Data shows the first bias scan from zero to 35 V, averaged over two individual devices. The inset shows three consecutive IV scans measured for the device prepared with a 4.6 mg ml^{-1} Hex-SiNC solution. The black arrows indicate the scan direction for the example of the first scan. (b) Current at $V = 35 \text{ V}$ as function of Hex-SiNC thin film thickness for devices with widths 5, 10, 20 and $50 \mu\text{m}$. The dashed lines are linear fits to the data points. (c) Current at $V = 35 \text{ V}$ as function of gap widths for different Hex-SiNC film thicknesses. The dashed lines are linear fits to the data points.

was measured over the entire voltage range. We note that the displayed curves are all averages from the *very first bias scans* from zero to 35 V. The reason for this choice of first curves was a pronounced hysteretic I – V behavior, which was observed for all investigated samples. By selecting the same (first) traces, all samples with different filling could be compared. The hysteretic behavior led to notable differences for consecutive forward and backward scans, carried out between the minimal ($V = 0 \text{ V}$) and maximal applied voltage. The inset of figure 3(a) shows the I – V traces of three subsequent scans as an example. As additionally apparent from the inset, for subsequent bias scanning cycles the overall reached maximum currents successively decreased, until typically after some twenty cycles the currents had already dropped by some 80%–90% (see, figure SI4). Yet, evaluating the first-scan data from 24 gap devices in total, we could determine the dependence of current as function of film thickness and channel width. As shown in figures 3(b) and (c), measured currents increased monotonically, roughly linearly as function of these two parameters, suggesting the well-defined, homogeneous filling of the gaps up to their edges. This is supported by an AFM image covering one full gap region, showing an overall homogeneous film with only minor surface undulation (see, figure SI5).

We note that all measured currents correspond to a very low conductance regime, with values in the range of 10 pA or below, at 35 V. Corresponding specific conductivities are estimated to be in the range 10^{-10} – $10^{-9} \Omega^{-1} \text{ cm}^{-1}$, hence can be roughly compared with conductivities of materials such as intrinsic wide-band-gap semiconductors or insulators. Previously reported specific conductivities for alkyl-functionalized SiNCs, which were about three orders of magnitude larger, could be assigned to slight doping of these SiNCs [19].

Yet, our study revealing the monotonic, approximately linear dependence of current as a function of film thickness and gap width indicates that charge transport presumably takes place homogeneously through the Hex-SiNC layer. This charge transport medium consists of a randomly ordered network of (undoped) SiNCs which are separated by surface bound hexyl molecules. The hexyl molecule thickness sets the SiNC-to-SiNC distance to a minimum of roughly 1.6 nm, assuming dense packing (see supporting information). This organic, insulating spacer represents a barrier for charge carriers to be transferred from SiNC to SiNC. For the traveling of charges over the total distance of 200 nm, percolation paths across the randomly connected network of SiNCs are likely [33–36]. The transport along these paths may involve a hopping-type of charge transport [37], Fowler–Nordheim tunneling [38], Pool–Frenkel conduction [19] or space-charge-limited-current (SCLC) transport [39]. If localized charges trapped within the semiconductor SiNCs may build up gradually with time under applied bias and continuous injection from the source, the overall resulting space-charge layer in the SiNC material will increasingly block subsequent charge injection. As a consequence, the resulting current at a fixed bias decreases with time. In fact, such a behavior has been observed for networks of oxidized or hydrogen-terminated SiNCs and explained within this framework [40]. The observed hysteretic behavior and particularly the successive degradation of current upon cyclic voltage ramping qualitatively agree with such SCLC mechanism, and first quantitative parameters may be extracted from the data. Figure 4 displays the I – V traces of figure 3(a) in a double-log plot. In this representation, two voltage ranges can be identified with disparate slopes, corresponding to a current–voltage dependence of the form $I = aV + bV^m$, with

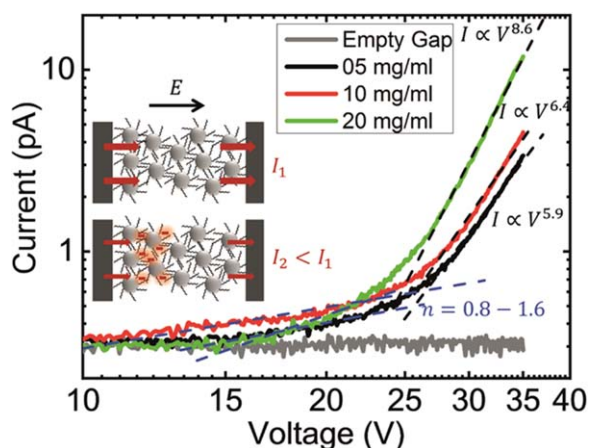


Figure 4. Current–voltage characteristics of figure 3(a) in a log–log plot. Dashed lines are linear fits to the curves, with extracted exponents n listed next to the data. Blue and black color refers to the medium and high-bias regime, respectively. Inset: schematic of trapped charges, limiting transport in a network of Hex-SiNCs.

a , b , m being fitting parameters adjusted to the experimental data. In the SCLC theory, the first (linear) term refers to the low-bias regime where mostly quasi-free charge carriers would contribute. In this regime, the parameter a corresponds to the Ohmic conductance whereas for higher voltages the second term with the power law coefficient m dominates [41, 42]. In fact, from fitting our data to a general $I \sim V^n$ dependence at medium bias, we obtain exponents in the range $n = 0.8\text{--}1.6$, which is in reasonable agreement with dominating Ohmic conductance. At low bias (below 5 V) no current could be resolved above our experimental resolution limit. At higher bias, our measured currents follow a distinct super-linear increase with voltage. According to previous reports, $m = 2$ would correspond to the absence of traps (Mott–Gurney law [43]), while $m > 2$ would indicate the presence of traps. Exponents of $m = 2\text{--}3$ have been reported for hydrogen-terminated SiNCs [33], while values of up to $m \sim 5$ were observed for oxidized SiNCs [40] and amorphous silicon [44]. The analysis of our data in the high-bias regime yields high values of $n = 5.9\text{--}8.6$. We assign this finding to a potentially high density of trap centers [41].

4. Conclusion

In summary, we have demonstrated that all-silicon electrode devices may serve as platform for the electrical characterization of thin films of functionalized, undoped SiNCs. A key factor to succeed in reliable measurements of these films in the high-resistance regime was a novel technique of filling the space between electrodes from solution, via a pressure-transducing PDMS membrane. This procedure led to homogeneous and dense thin films practically without any cracks or voids, and with precise control of the film thickness. The electrical functionality of our devices was demonstrated for thin films of hexyl functionalized SiNCs of various thicknesses, filled into the 200 nm trench separating the Si electrodes. Conductance was significantly enhanced compared to

untreated devices. The obtained current–voltage (I – V) characteristics showed the anticipated scaling with channel width, ranging from 5 to 50 μm , and with film thickness, ranging from 15 to 92 nm. A strongly hysteretic I – V dependence together with a successive decrease of current with time or with the number of I – V cycles can be assigned to SCLC-transport, with the functionalized SiNCs providing efficient charge trap centers. Future studies will focus on a microscopic understanding of this transport, including the influence of different SiNC surface-bound organic molecules, which can be varied over a wide range. Further, we plan to determine the actual contact resistance value (Si electrode to SiNC film) and its impact on charge injection.

We suggest our planar, all-silicon device architecture and functionalization methodology as platform for investigations of the transport properties of thin films of various hybrid nanomaterials, in particular in the high-resistivity range.

Acknowledgments

We are grateful to Rui Pereira for helpful discussions. This work has been supported by the Deutsche Forschungsgemeinschaft DFG (IRTG 2022 ATUMS). A Angi is thankful for the funding from the Studienstiftung des deutschen Volkes.

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