Fakultät für Elektrotechnik und Informationstechnik
Technische Universität München

# Design and Technology of Discrete Silicon-based Vertical SCR Devices for System-Level ESD Protection

**Vadim Valentinovic Vendt**

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Vorsitzender: Prof. Dr.-Ing. Klaus Diepold

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1. Prof. Dr. rer. nat. Franz Kreupl
2. Prof. Dr. rer. nat. Marc Tornow

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## Abstract

Discrete Electrostatic discharge (ESD) protection devices are the backbone of system-level ESD robust designs, fulfilling industry standards such as IEC61000-4-2. Modern ESD robust designs are facing two major challenges. First, advancing technology nodes and the continuous shrinking of device sizes result in a lower ESD robustness of modern integrated circuits (IC). On the one hand, thinner gate-oxides lead to lower breakdown voltages and, thus, increased susceptibility to ESD stress and IC damage and/or malfunctions. On the other hand, shrinking a device at a constant current density yields a lower absolute power level which this device can withstand. This illustrates the need for improved ESD protection, both in terms of clamping voltage and residual ESD current carried by the IC to be protected. Second, discrete ESD protection devices are added last to a new system design and are faced with a continuously decreasing design window in terms of allowed parasitic capacitance. Especially newer high data-rate applications such as USB3.2 require less than 300 fF parasitic capacitance per data-line in order to ensure signal integrity. As a consequence, more stringent device requirements have to be placed on the design of the discrete ESD protection device itself, both in terms of a lower clamping voltage and a reduced device capacitance.

State-of-the-art external protection devices are bipolar transistor structures (silicon-based NiPN or PiNP) or silicon-controlled-rectifiers (SCR). Both utilize series p-i-n diodes to decrease overall device capacitance but SCR devices offer a superior clamping performance due to their deep snapback behavior (holding voltage below 2 V). SCR devices can be realized as vertical or lateral structures with advantages and disadvantages on each side. The vertical device concept, namely a lateral triggered vertical thyristor (LTVT), has an inherently higher ESD robustness per silicon area than the lateral concept. This provides an advantage both from an design and economical point of view. Hence, this work is focused on the LTVT.

During device development a de-latching behavior of the thyristor was observed at high current densities ($>1 \cdot 10^6$ Acm$^{-2}$), leading to a increase in clamping voltage and loss of protection performance. For the first time, this work shows by means of TCAD simulations that the de-latching behavior and its subsequent impact on thyristor-based ESD protection devices is related to the $\beta$-roll off at high current densities. It has been shown by both experiments and device simulations that the

de-latching of a SCR can be avoided by increasing the internal gain-product thru technology optimization (e.g. base doping engineering). Moreover, the technology implementation of the novel LTVT device required the development of a unique pn-short concept to contact buried silicon layers. The purpose of the pn-short is to electrically short a blocking pn-junction and provide a low ohmic connection to a buried layer. This also includes the introduction of a sidewall doping process to prevent Schottky-Diode behavior.

The vertical device technology developed in this work supports a wide range of working voltages (3.3 V to 18 V) by means of a tuneable trigger device in a SCR-based protection structure. In combination with the novel LTVT device the resulting discrete ESD protection device can protect high-speed interfaces as well as RF applications. A first version of the developed LTVT achieved an ESD robustness of 20 kV and a device capacitance of 0.25 pF. The further optimized design achieved 23 kV at 0.3 pF and a trigger voltage of less than 10 V. Both the developed device concept and the associated technology are in mass production now.

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# 1 Introduction

Electrostatic Discharge (ESD) is a well known every day phenomenon. While the charge-up process is unnoticed the discharge event has a broad range from small surprising "shock" moments to severe lightning strikes with sound. A typical ESD experience is the well known zap when touching the car body after sliding out of the driver's seat [1].

The origin of ESD events is the charging of objects by triboelectricity. The voltage that is build up reaches several thousand volts and causes a short (1 ns to 200 ns) high current amplitude of several amperes during discharge [2], [3]. While humans notice a short zap or an acoustic sound, an electronic system, that consists of several integrated circuits (ICs), may be damaged by the discharge current and the resulting power dissipation.

Today, the semiconductor industry and electronic component manufacturers implement counter-measures to protect sensitive ICs against ESD damage because this is a major reliability issue. The continuous scaling of technology nodes increases the susceptibility of ICs to ESD. Therefore, further improvements of protection devices are required (see Section 1.3) [4], [5], [3].

The two following approaches are known as counter-measures against ESD:

1. **Prevention**

   Avoiding the charge-up of objects during assembly, testing and transportation. Prevention measures can be for example air ionizers, wrist straps, ESD shoes. This is described by the ESD protected area (EPA) in the DIN61340-5-1.

2. **Protection**

   Protection actively increases the intrinsic capability of the IC or system to withstand ESD events by itself without taking damage. ESD protection structures (e.g. silicon-based protection devices: pn-diodes, NMOS-transistors, silicon-controlled-rectifiers (SCRs)) are used to increase the robustness of the electronic system against ESD [4], [5], [6].

As prevention will not be covered in this work, the focus is on the active protection of electronic systems with ESD protection devices, more specifically on silicon-based ESD diodes.

The ESD robustness of ICs is rated by the Human-Body-Model (HBM)[1] voltage [7] and the required voltage levels are defined by the Industry Council on ESD Target Levels (ICoETL) [8]. A HBM level of 1000 V is commonly required and sufficient for ICs in a controlled manufacturing environment.

In contrast, electronic systems and -devices in daily application are exposed to severe ESD events because of the possibility of higher charging voltage in a non-EPA environment. System level ESD protection requires the understanding of the whole system to be protected because it consists of a multitude of ICs that mostly cannot withstand system level ESD events.

Therefore, discrete protection elements are commonly used to increase system level ESD robustness. They are known as transient voltage suppressors (TVS) or off-chip protection devices [9], [10].

In the following a brief introduction to System Level ESD, the testing method and the technology requirements for discrete silicon based protection devices is given.

## 1.1 System-Level Electro-Static Discharge

System level ESD considers pins on a system-board or -case/shell, which are exposed to the environment and have the possibility to experience ESD events. Those external pins need to be protected by ESD protection devices (see Figure 1.1). The internal pins are not considered, nevertheless they are susceptible to cross-talk during system level ESD events.

A system level ESD event has the potential to cause different failure modes depending on the individual ESD protection level of the electronic system. They start from clock signal glitches leading to corrupted bits (soft failure) [12] and end with hardware damage due to electrical over-stress of ICs (hard failure).

To give an example for a hard failure, a charged cable is plugged into a data-interface connector. The charged cable then discharges into a signal pin and causes

[1] charged human body is modeled by a 100 pF capacitor and a 1.5 kΩ discharging resistance

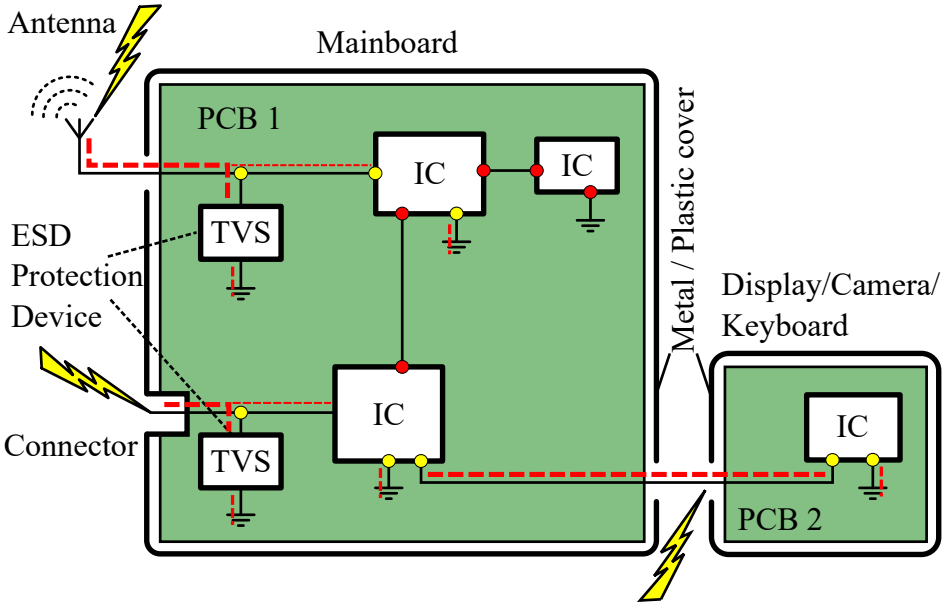



**Figure 1.1:** A wired system with its internal ICs and external ESD threats (indicated by thunderbolts) is shown. External pins and internal ports exposed to the ESD threat are indicated in yellow (bright). Internal ports in red (dark) are not protected by a TVS. Red lines (dashed) indicate the ESD current. TVS protection elements are placed at the antenna and connector lines to protect the ICs. The connection between printed circuit board (PCB) 1 and PCB 2 is not protected. The illustration is based on [11].

damage to the controller. This results in a hardware failure and permanent loss of functionality [13].

A similar event can also lead to a temporary freeze of the operating system and a full recovery of the software without permanent damage and is categorized as a soft failure.

It is important to mention that ESD events are radiating and can couple electromagnetic fields into signal lines and induce currents into adjacent lines on the system board (cross-talk), which is known as electromagnetic interference (EMI) [9].

Several textbooks describe different protection strategies and concepts for system level ESD and introduce methods to increase the robustness of an electrical system against ESD [3], [10]. Discrete ESD protection devices are the most efficient regard-

ing chip area consumption and protection performance [3]. Silicon-based external protection devices are currently state-of-the-art and investigated in this thesis.

## 1.2 System-Level ESD Immunity Test

A standardized test method like the IEC61000-4-2 is needed in order to evaluated the system-level ESD robustness [14]. The IEC61000-4-2 standard defines the typical waveform of the discharge current, test levels, setups, and the procedure. Tested systems are evaluated by pass or fail at defined stress levels. Insertion points for the ESD stress can be all places which are also accessible to the user. Two discharge modes are available, which are contact and air discharge. While air discharge is more realistic, the contact discharge is preferred because of better reproducibility [15].

To emulate the system level test method for components, the Human Metal Model (HMM) test method is used to apply the IEC61000-4-2 waveform into. Several publications address this method [16], [17] and [18].

The structures presented in this work will not be rated based on IEC61000-4-2 because it is not designed to test discrete devices. Instead, the Transmission-Line Pulse (TLP) characterization method is used to rate the protection performance of ESD structures because it is well acknowledged in the ESD community due to its reproducibility and good correlation to IEC61000-4-2 [19], [20], [21], [22], [23]. A brief description of the method is given in Section 3.4.5.

## 1.3 Requirements for ESD Protection Devices

The continuous demand for higher integration levels by following *Moore's Law* [24] and faster data-rates drive advances in IC technology, such as shrinking the feature size of transistors and gate oxides in combination with reduced operating voltages. This leads to lower gate oxide breakdown voltages (e.g. 3.1 V in 14 nm PFETSOI FinFETs) and a decrease in ESD failure current (e.g. 0.1 $\mathrm{mA\,\mu m^{-1}}$ TLP 1ns in 14 nm PFETSOI FinFETs) [25]. Corresponding to that, discrete ESD protection devices have to adapt and improve their ESD performance by improving key parameters like clamping voltage to protect gate oxides (see Section 2.2).

Discrete ESD protection devices are specialized to achieve highest system level ESD robustness levels of sensitive electrical systems by providing a high power dis-

sipation capability on smaller areas compared to integrated ESD structures. Silicon-based protection devices are leading the industry by sustaining highest ESD currents and thousands of ESD events without degradation in contrast to polymer-based ESD protection devices and varistors which typically only withstand 10-20 discharges before degradation [3], [10].

A major advantage of using discrete ESD protection devices is the flexibility to replace them without re-designing the printed circuit board. This offers flexibility to replace several discrete components to achieve the target performance. State-of-the-art discrete ESD protection devices are usually bipolar snapback devices (npn-structures) that are available in different voltage classes.

Two trends have clearly evolved in the past years:

- Continuous reduction of device capacitance in discrete ESD protection devices ($< 0.3$ pF) because of the capacitance budget in high data-rate communication interfaces (e.g. USB3.1).
- Continuous reduction of the ESD clamping voltage based on lower failure voltages of advanced technologies (e.g. gate oxide) breakdown $< 5$ V at 65 nm [26] and down to 3 V [25].

These two trends are linked because ESD clamping voltage depends on the device resistance, which is, reciprocal to device area but capacitance is proportional to junction area. Pnpn-structure are utilized to reduce the ESD clamping voltage without increasing device area. They are also known as Silicon-Controlled-Rectifier (SCR) and have a low forward voltage similar to a diode after triggering. SCR-based protection devices are known to have highest ESD performance per area [4]. *Park et al.* reported a capacitance optimized SCR with a failure current of 2.6 A at 355 $\mu m^2$ layout area, corresponding to 7.3 $mA/\mu m^2$ [27]. *Ma et al.* published a SCR in 65 nm CMOS with 4.2 $mA/\mu m^2$ against a gate-grounded NMOS with 2.5 $mA/\mu m^2$ [28].

SCRs are well known as on-chip ESD protection structures but are not frequently used as discrete ESD protection devices. The utilization of SCR structures are restricted to applications with limited current supply or no direct current (DC) signals due to possible latch-up [29], [30], [31].

## 1.4 Motivation and Objectives

The trends for discrete protection devices clearly focus on the continuous decrease of the ESD clamping voltage to increase system level ESD protection performance especially for advanced technologies with reduced ESD failure voltage. Decreasing ESD clamping voltage requires an optimized SCR-based ESD protection structure.

State-of-the-art communication interfaces like USB3.2, HDMI2.0 and Thunderbolt 3 are operating at high data-rates above 5 GBit/s and require low parasitic capacitance of the ESD protection device to ensure impedance matching and low signal insertion loss at their operation frequencies [3]. Additionally, the above mentioned applications have limited supply current and hence latch-up in SCRs can be avoided [32]. For example, USB3.1 and higher versions use AC coupling capacitors which block DC currents hence a latch-up will not be possible [33], [32]. It was shown in [34] that the trigger voltage of the external ESD device can be larger than the internal ESD device which makes this parameter less critical compared to clamping voltage and capacitance. In applications with RF signals, the trigger voltage can be lower than expected and needs a decent margin to the operation voltage to prevent false triggering [35].

Therefore, the motivation of this work is an upcoming demand for better external ESD protection with low clamping voltage based on SCR structures and low device capacitance while providing highest possible system level ESD robustness. A properly designed and optimized pnpn-structure, that is introduced in this work, fulfills the stated requirements.

SCR based ESD protection devices reported in literature are using lateral structures [3], [36]. It is known that lateral structures are scaling with its perimeter length and less with its area due to the lateral current flow which is less efficient compared to vertical ESD structures that are using all of their junction area. This work particularly focuses on vertical SCR structures to take advantage of the area efficiency that helps to minimize device area and, thus, the related device capacitance. One target is to achieve a device capacitance $< 300$ fF) in combination with a system level ESD robustness of $> 20$ kV) according to IEC61000-4-2. Today's external ESD protection devices achieve already low capacitance values but suffer from low system level ESD robustness [37], [36], [38].

The objectives of this thesis are the following:

- outline the fundamental physical background of vertical pnpn-structures to understand the impact on ESD performance parameters
- develop ESD protection device concepts based on vertical pnpn-structures to achieve better ESD performance compared to lateral SCR-based ESD protection devices
- identify design factors and optimize vertical pnpn-structure for system level ESD protection (e.g. switching speed, transient voltage overshoot)

## 1.5 Thesis Outline

Chapter 2 introduces the concept for system level ESD protection and important ESD protection parameters. State-of-the-art ESD protection structures like pn-diodes, pnp/npn-transistors and pnpn-structures are introduced. A concept for low capacitance structures comprising a series p-i-n diode with a zener diode is explained because this is a basic concept.

Chapter 3 discusses the design, simulation, technology and characterization of a novel vertical pnpn-structure for external ESD protection. First, a vertical SCR with ESD robustness of 30 kV and 0.28 pF device capacitance is presented. A trigger voltage ($< 10$ V) was not achieved while a reproducible increase in clamping voltage at high current densities ($1 \cdot 10^6$ Acm$^{-2}$) was observed. Second, a lateral trigger structure was embedded into the vertical pnpn-structure to lower the trigger voltage and prevent the SCR from de-latching. The trigger voltage of the SCR was successfully reduced to less than (10 V) without de-latching. Additionally, a faster response time was achieved by lowering the initial voltage overshoot in the SCR and reducing the transit time of the lateral trigger. A pn-junction short structure is presented which ensures a low ohmic connection for negative ESD polarities. Its implementation is unique and the purpose is to combine two vertical structures into one substrate while the first structure is a four-layer device and the second is a three layer p-i-n diode. Pseudo-3D device simulations of vertical SCR structures were carried out for technology development support and verification. Last but not least, characterization techniques and methods for ESD devices are introduced and explained. Static measurements like the DC breakdown voltage as well as device capacitance characterization in the femtofarad range are described. A high-current characterization method with Transmission-Line-Pulsing (TLP) is introduced.

Chapter 4 discusses the current gain roll-off effect which occurs in pnpn-structures and leads to an increase in clamping voltage during forward operation. A reason is the well known current gain roll-off that is known from bipolar transistors. It leads to a collapse of the internal gain product and a violation of the required feedback condition in SCRs to maintain the low operation voltage. This is discussed for the first time in detail and illustrated by measurements and device simulation results. An optimization of the proposed vertical structure by device simulations and experiments is shown and successfully implemented in the final structure to prevent de-latching.

Finally, a conclusion of this work is given together with suggestions of further topics which were not covered by this thesis.

# 2 System-Level ESD - Principles and Device Technologies

This chapter introduces system level ESD protection concepts. The utilization of discrete silicon devices is shown. Protection device parameters are defined by the ESD design window. State-of-the-art semiconductor-based structures for system level protection are described. Typical implementations and current versus voltage (IV) characteristics of discrete ESD protection devices are shown. A state-of-the-art concept for minimizing the device capacitance by a series connection of p-i-n structures and avalanche structures is introduced.

## 2.1 System-Level ESD Protection Concept

Several protection strategies are considered for successful system level ESD protection and one important measure is the application of external ESD devices. One major advantage is the possibility to combine multiple components on a PCB to meet the system level ESD targets [3]. External ESD protection devices are easily exchanged to match the required ESD robustness without expensive re-design of the PCB.

The function of external ESD protection devices is to shunt the ESD current, to absorb the injected energy of a ESD event and to protect internal circuits from damage due to over-voltage or -current [4].

An example of a system level ESD protection concept based on external ESD protection is shown in Figure 2.1. The integrated on-chip protection is sufficient for component level ESD protection but is not able to survive a system level ESD event. Therefore, an external ESD protection device (TVS) is placed at the external pin to shunt the ESD current and limit the voltage to a value lower than the failure voltage of the IC to be protected.

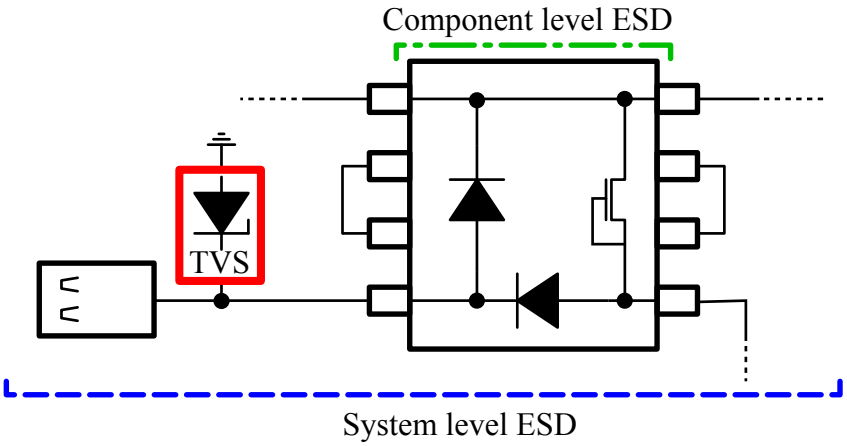



**Figure 2.1:** Concept of a system level protection design with an external ESD protection device (TVS) at the connector which is exposed to system level ESD events (adopted from [3]).

## 2.2 ESD Design Window and Protection Device Parameters

ESD protection devices are designed by specific requirements that are defined by the system to be protected. Figure 2.2 shows the ESD design window that defines the operation region of the ESD protection device. The region on the left side indicates the operation region of the IC and the region on the right side shows the critical area of the IC where an irrecoverable damage occurs. A safety margin is introduced between $V_S$ and $V_h$. Between the two regions, the ESD protection device operates and prevents the IC from reaching the critical region by limiting the voltage at the IC pin and shunting the ESD current to ground. This operation region is defined as ESD design window, which gets narrower for more ESD susceptible ICs (e.g. reduced gate oxide (GOX) breakdown voltage).

According to the ESD design window, a set of important ESD protection device parameters is summarized in Table 2.1. Parameters like $V_{t2}$ and $I_{t2}$ depend on the duration of the ESD pulse and decrease for longer period. $I_{t2}{}^*$ of the protection device limits the overall robustness and is desired to be higher than $I_{t2}$ of the IO. $V_h$ is a crucial protection device parameter that can either match $V_{t1}$ for pn-diodes or differ for bipolar devices with a current gain. $V_h$ has to be designed with a margin to

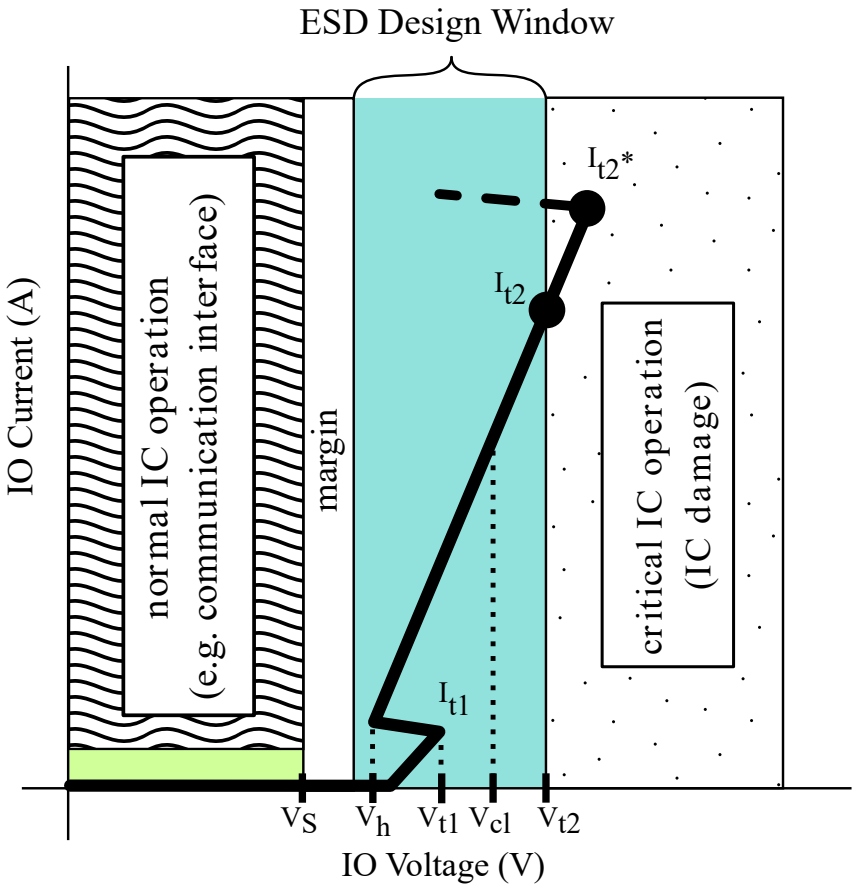



**Figure 2.2:** The ESD design window for protection is represented by a current over voltage graph for the IC IO pin. The operation area of the circuit is on the left while the critical operation regime is on the right. The area in between is the design window for ESD protection devices.

$V_S$. For example, SCR devices have the lowest $V_h$ compared to bipolar NPN or gate grounded MOS devices [5]. The clamping voltage ($V_{cl}$) is a function of time and current. For simplicity, $V_{cl}$ is specified in the steady state as shown in Figure 2.2. Due to the finite turn-on time of silicon pn-junctions and their forward recovery effect a voltage overshoot occurs in ESD devices [39], [40]. The duration can be several

**Table 2.1:** Definition of ESD protection device parameter.

| Parameter | Description | Comments |
|---|---|---|
| $V_S$ | supply voltage of the circuit to be protected | depends on application e.g. 1.8V, 2.2V, 2.8V, 3.3V, 5V |
| $V_{t1}$ | ESD protection device trigger voltage | voltage value which triggers the device into its on-state e.g. breakdown voltage of pn-diodes |
| $V_{t2}$ | ESD failure voltage | voltage at which damage occurs |
| $V_{cl}$ | ESD clamping voltage | clamping voltage of the ESD device during on-state |
| $V_h$ | ESD device holding voltage | lowest voltage value which is possible during the on-state of an ESD protection Device e.g. $V_{CE0}$ in transistor structures |
| $I_{t1}$ | ESD device trigger current | current value which is needed to trigger the device into its on-state |
| $I_{t2}$ | ESD failure current | current value at which damage occurs to the IC |
| $I_{t2}{}^*$ | ESD failure current (protection device) | current value at which damage occurs to the protection device |

picoseconds to nanoseconds and cause damage to gate oxides and pn-junctions of the IC to be protected [4], [5].

## 2.3 ESD Protection Structures

State-of-the-art silicon-based ESD protection structures are based on well known semiconductor devices like pn-diodes, bipolar transistors, metal-oxide-semiconductor (MOS) transistors and pnpn-structures (also called SCR). A complete overview of ESD devices is given in the literature [4], [5], [6], [3]. Here, the focus is on pn-diodes, pnp- and npn-transistors, and pnpn-structures because they are commonly used for external ESD protection. Operation mode, device physics, and high current characteristics of selected protection structures are introduced.

### 2.3.1 pn-Diode

The pn-diode is the basic silicon-based protection device structure which is used for ESD protection. Pn-diodes are standard elements in many technologies (e.g. BCD[1]) and utilized as integrated protection element as well as discrete device. Figure 2.3 shows some examples of pn-diode structures in different technologies. .

The pn-diode can be used in forward and reverse operation mode to conduct the ESD current and clamp the voltage at the terminal to be protected. In CMOS technologies the pn-diode is used only in forward conduction because the breakdown voltage in reverse operation is higher than the $V_{t2}$ of the nodes to be protected. A series connection of multiple pn-diodes is a method to fit the ESD design window (see Figure 2.2). The reverse operation is a standard application for ESD protection [4].

Figure 2.4 shows the high-current characteristics of selected pn-diode structures designed for external ESD protection. These structures consists of vertical pn-diodes comparable to Figure 2.3 (c) with the advantage of higher area efficiency[2] compared to lateral diodes because most of the conducting pn-junction area is used in contrast to perimeter length in lateral structures.

#### Forward Conduction

The forward operation is commonly used in CMOS ESD protection concepts to protect MOS structures with threshold voltages below 1 V [5], [45]. The ideal

[1] Bipolar, CMOS, DMOS

[2] area efficiency means a higher failure current per silicon area

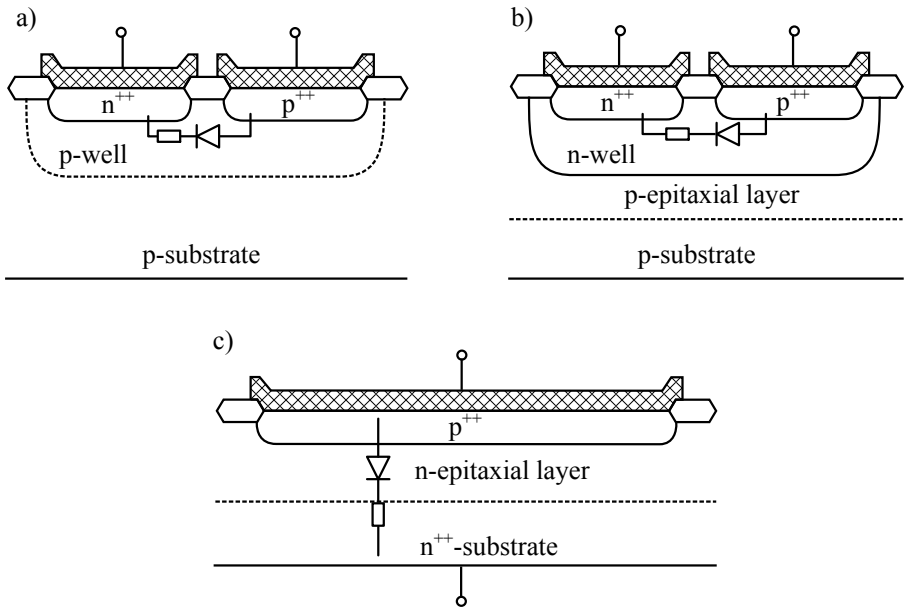



**Figure 2.3:** Cross-section of pn-diode structures in different technologies. (a) is showing a lateral pn-diode in CMOS, (b) a pn-diode implemented in BiCMOS and (c) an example of a discrete vertical pn-diode used for off-chip protection. The drawings were adapted from [5],[6], [41]

forward characteristics of a pn-diode is modeled by the *Shockley diode equation* in Equation 2.1 for low-injection ($n = 1$) and high-injection ($n = 2$). $J_D$ is the diode forward current density, $J_S$ the saturation current density which is different for recombination, diffusion and high-current conduction, $V_j$ the applied junction potential, $k_b$ the Boltzmann constant, $T$ the temperature, $N_D$ the doping concentration of the lower doped region of the diode and $n(x)$, $p(x)$ are the carrier concentrations during forward conduction.

$$J_D = J_S\left(e^{\frac{qV_j}{n \cdot k_b T}} - 1\right), \quad qV_j \geq 0, \quad n = \begin{cases} 2 & \text{if} \quad n(x) \simeq p(x) \geq N_D \\ 1 & \text{if} \quad n(x) \simeq p(x) < N_D \end{cases} \tag{2.1}$$

### Reverse Conduction

Reverse conducting pn-diodes are operated by applying a sufficiently large reverse voltage between anode and cathode. The applied reverse voltage forces the pn-junction into the junction breakdown operation. The breakdown voltage is determined by the doping concentration and shape of the pn-junction.

The breakdown process itself is not destructive but excessive Joule heating due to a high power density can lead to a thermal breakdown of the diode structure. In case of an ESD event a short but high current is conducted by the pn-diode. The dissipated energy in the silicon structure is limited due to the finite ESD event and damage due to Joule heating can be avoided if the diode is designed accordingly. A detailed description of the breakdown physics is found in [46], [47], [48], [49].

It is important to distinguish between two possible breakdown mechanisms which occur in a reverse biased pn-junction. The first mechanism is the *Zener-effect* that is related to quantum mechanical tunneling at very high electric fields. The second mechanism is the *Avalanche-breakdown* that describes the generation of electron-hole pairs (EHP) by collisions of free-carriers with the silicon lattice. The free-carriers were accelerated by the electric field in the reverse biased junction to reach the required kinetic energy for the impact ionization process [46], [47].

*Sze* assigned voltage domains to the two breakdown mechanisms based on the band-gap energy. This is summarizes as follows [47]:

$$\left.\begin{array}{ll} \textbf{tunneling (zener)} & V_{BD} < \frac{4E_g}{q} \approx 4.5\,\mathrm{V} \\ \\ \textbf{avalanche} & V_{BD} > \frac{6E_g}{q} \approx 6.7\,\mathrm{V} \end{array}\right\} \text{breakdown} - \text{mechanism} \qquad (2.2)$$

The energy range between $\frac{4E_g}{q}$ and $\frac{6E_g}{q}$ is described as a superposition of both breakdown mechanisms as both processes take place. Published results in [50] indicate that tunneling due to high local fields at crystal dislocations can occur in the silicon structure. This can lead to soft breakdown characteristics indicated by an increase of leakage current before the avalanche breakdown voltage is reached.

It is important to mention that the temperature coefficient of the *Zener-effect* is negative while the *Avalanche-breakdown* is positive [6], [51]. *K. Esmark* extracted an avalanche breakdown temperature dependency ($dV_{BD}/dT$) of $4.4\,\mathrm{mV\,K^{-1}}$ for a

0.35 µm technology with an avalanche breakdown voltage at 10 V, which confirms a positive temperature coefficient.

The breakdown voltage of the pn-junction is determined by the critical electrical field $E_{c,Si}$, which is about $2 \cdot 10^5\,\mathrm{V\,cm^{-1}}$ for silicon. Therefore, the breakdown voltage for an ideal single-sided pn-junction can be calculated from the solution of Poisson's equation:

$$V_{BD} = \frac{\varepsilon_0 \varepsilon_{Si} E_{c,Si}^2}{2q} \cdot \frac{1}{N_D}, \quad E_{c,Si} = f(N_D) \tag{2.3}$$

Figure 2.5 shows the plot of Equation 2.3, which is used by [47] compared to other empirical models from literature. *Sze* refers to the dependency of $E_{c,Si}$ with the background doping $N_D$. Therefore, $E_{c,Si}(1 \cdot 10^{17}\,\mathrm{cm^{-3}}) = 6 \cdot 10^5\,\mathrm{V\,cm^{-1}}$ is used on the comparison. This leads to a deviation from the empirical models for decreased and increased doping concentrations.

A general equation is not available because the junction profiles of real pn-diodes are not abrupt pn-junctions and depend on process technology. Hence, the breakdown voltage is estimated by the simplified Equation 2.3. Device simulation tools are capable of calculating breakdown voltages for arbitrary profiles which can be calibrated and evaluated by experiments.

### 2.3.2 Bipolar Junction Transistor

The bipolar junction transistor (BJT) is a common ESD protection structure included as parasitic structure in CMOS component level ESD protection (e.g. gate-grounded-MOS) or utilized as dedicated ESD protection device [4], [5], [26].

While a general transistor structure has three terminals, which are known as *emitter*, *collector* and *base*, an external ESD protection device is realized as a two terminal structure (compare Figure 2.6). The BJT structure can be realized as unidirectional or bidirectional device that conducts ESD current in both polarities. The base-emitter junction can be shorted for a unidirectional configuration while the bidirectional BJT comprises a floating base. Both devices are operated in avalanche breakdown of the collector-base junction in avalanche breakdown (compare Section 2.3.1). In both cases the floating base current is supplied by the avalanche process. A description of the physics in bipolar structures during ESD is found in [4], [5], [6], [3].

The BJT can operate at a reduced terminal voltage when a decent current gain is realized. A negative differential resistance which is known as *snapback* (see Figure 2.7(b)) can be observed in high current gain structures. A high current gain corresponds to a high emitter efficiency and base transport factor and increases the amount of free carriers available for avalanche multiplication and enhance the avalanche current [4]. A detailed description of the snapback effect and the modeling is given by *A. Amerasekera* and *C. Duvvury* [4] as well as in the dissertation of *C. Russ* [5].

The reduced terminal voltage due to the snapback is roughly estimated by the *Miller formulation* Equation 2.4 and shows good agreement for common BJT devices [5]. $V_{CE}$ is the collector emitter voltage, $V_{BD}$ the junction breakdown voltage of the reverse collector-base, $\beta$ is the common-emitter current gain and $n$ is a fitting parameter related to the junction doping profile.

$$V_{CE} = V_{BD} \cdot (1+\beta)^{\left(-\frac{1}{n}\right)}, \quad 1 < n < 6 \tag{2.4}$$

The snapback is a beneficial condition which is used in state-of-the-art ESD protection devices to reduce the ESD clamping voltage. It is obvious that $V_{CE}$ is similar to the holding voltage ($V_h$) of ESD protection devices and depends on the current gain of the BJT and its collector-base junction breakdown. The current gain is a function of the base, collect and emitter doping profile. $V_h$ lower than 3 V due to a snapback effect have not been reported so far.

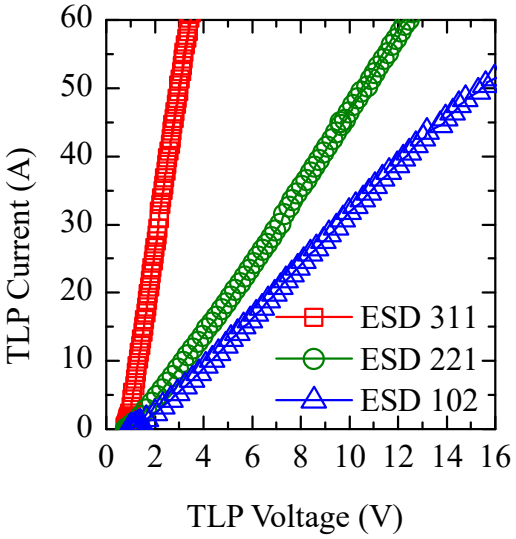
Figure 2.6 shows examples of common transistor structures which are utilized as ESD protection structures and Figure 2.7 illustrates typical high current characteristics of selected ESD protection devices based on transistors structures with and without snapback. The ESD200 is clearly a device with a low gain that has a lower $V_{t1}$ compared to ESD108 indicating higher collector-base doping. This is also confirmed by the device capacitance which is more than two times higher for the ESD200.

### 2.3.3 Silicon-Controlled-Rectifier

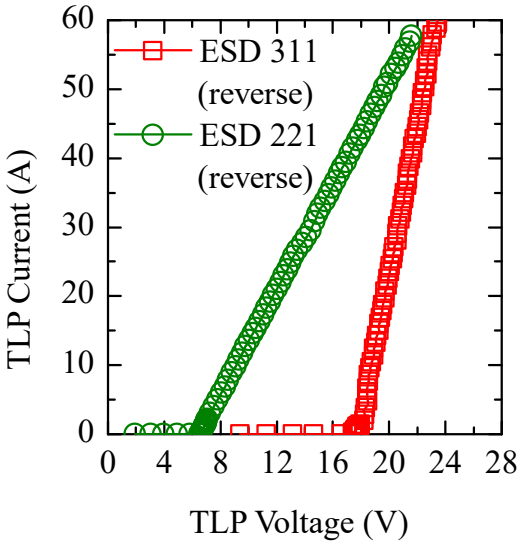
Silicon-Controlled-Rectifier (SCR) are well known as power devices consisting of four alternately doped semiconductor layer forming a pnpn-structure [46], [48], [49]. The device consists of three terminals that are named as anode, cathode and gate. The gate terminal is used to actively trigger the device into the on-state which

is called forward conduction. The three internal junctions ($J_1$, $J_2$, $J_3$) have to be forward-biased to enable current conduction from anode to cathode. A SCR can be divided into two BJT structures which are interleaved and sharing $J_2$ as a common collector-base junction [48]. The BJT terminology will be used to explain device function. The breakover voltage ($V_{BO}$) is a SCR specific parameter and specifies the internal junction breakdown voltage if the gate is not connected. Applying negative voltages to the anode forces the SCR into reverse blocking of $J_1$ and $J_3$. Reaching junction breakdown $J_1$ and $J_3$ leads to avalanche breakdown. A typical electrical characteristics of a SCR is shown in Figure 2.8.

Figure 2.9 shows a schematic of a pnpn-structure with its regions and terminals. The internal electron- and hole-current density composition in the forward conducting state are illustrated. Additionally, the idealized band structure at equilibrium (Figure 2.9(b)) and forward conduction (Figure 2.9(c)) are shown.




(a)




(b)

**Figure 2.4:** High-current (TLP) IV characteristics of selected external ESD protection pn-diodes [42], [43], [44]. Forward characteristics are shown in (a) and reverse breakdown operation in (b).

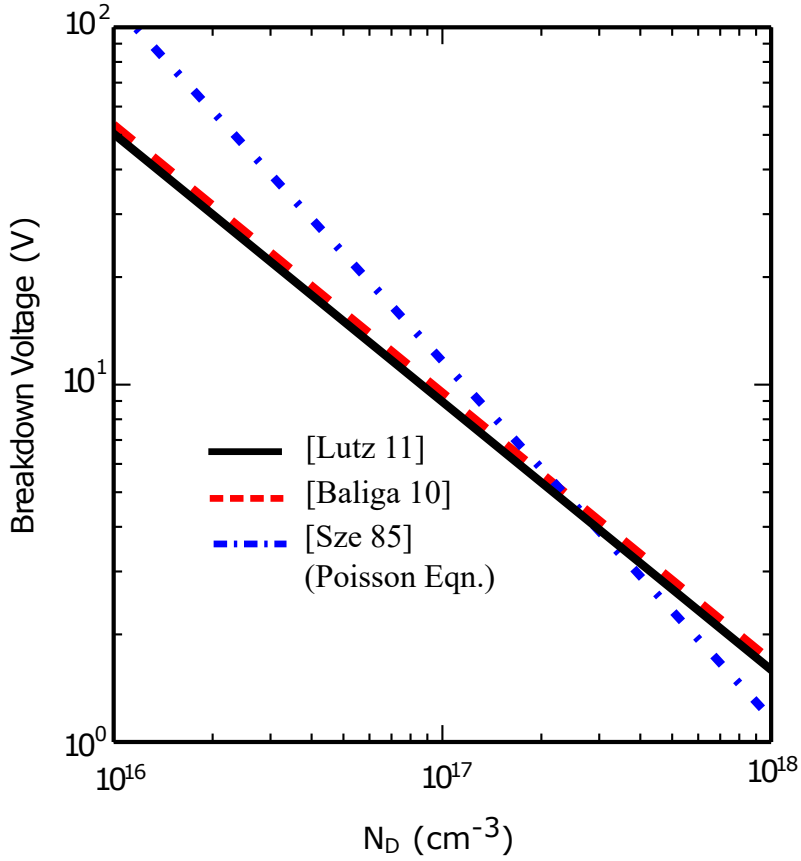



**Figure 2.5:** Breakdown voltages for single-sided pn-junctions. Analytical and empirical models from [47], [48] and [49] are compared.

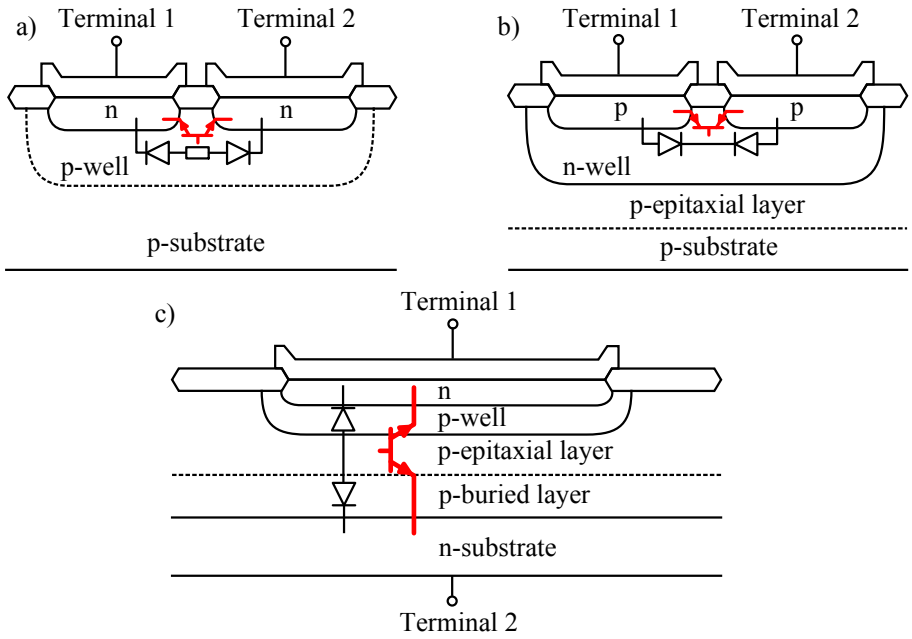
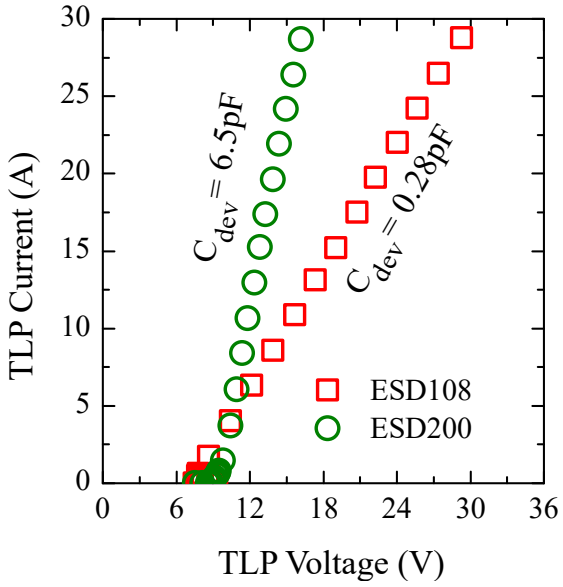
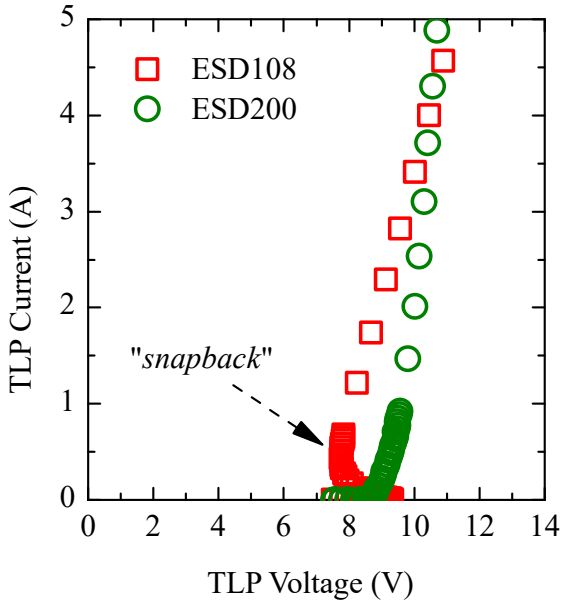



**Figure 2.6:** A schematic cross-section of typical transistor structures utilized for ESD protection. (a) shows a lateral floating base npn-transistor, (b) a lateral floating base pnp-transistor complementary to (a) and (c) a vertical floating base npn-transistor structure.




(a)




(b)

**Figure 2.7:** Measured high-current (TLP) characteristics of discrete ESD protection devices based on npn-/pnp-structures [52], [53]. The high current IV characteristics is shown in (a) and a detailed view of the lower current regime after triggering is shown in (b). The ESD108 shows a *snapback* behavior which reduces the device voltage below the trigger voltage $V_{t1}$.

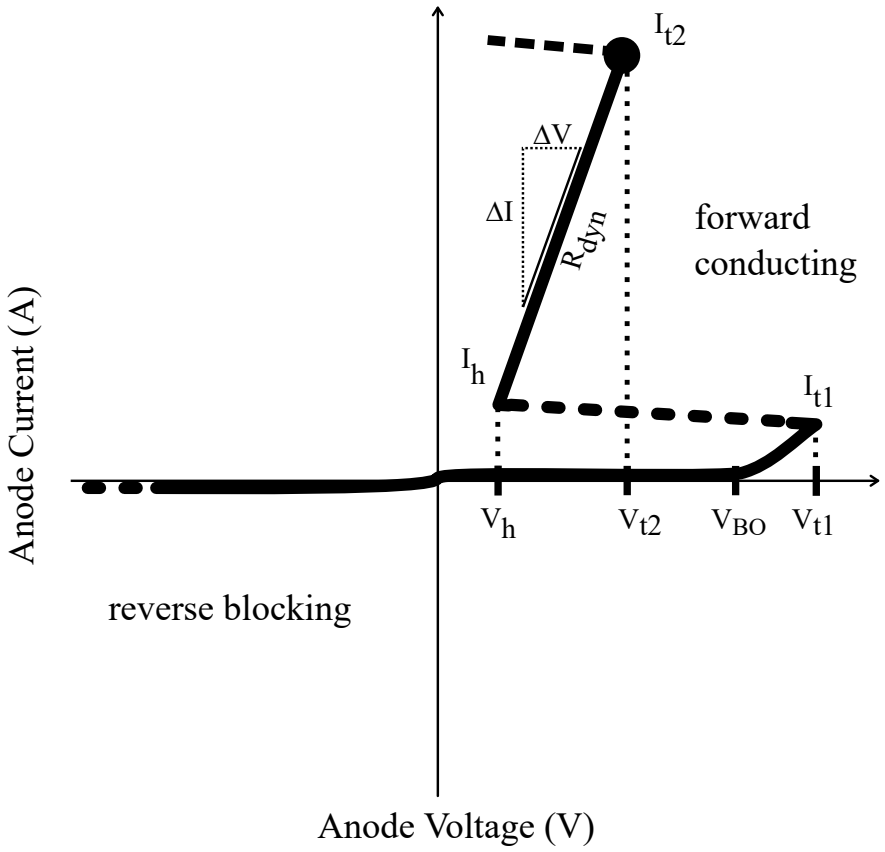
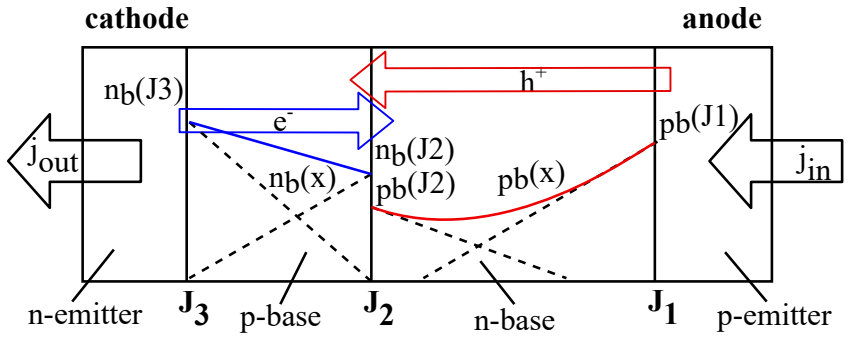
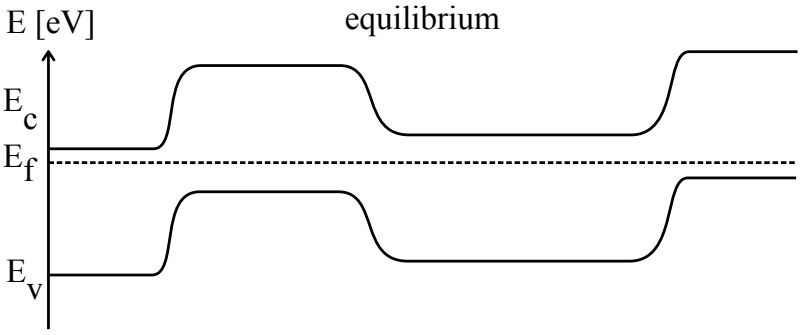



**Figure 2.8:** A schematic IV characteristics of a SCR device. The SCR is in forward operation for positive voltages at the anode terminal. Applying negative voltages to the anode forces the SCR into reverse blocking. When no gate signal is applied, the SCR is triggered by reaching $V_{BO}$ first followed by $V_{t1}$ and finally $V_h$.




(a)

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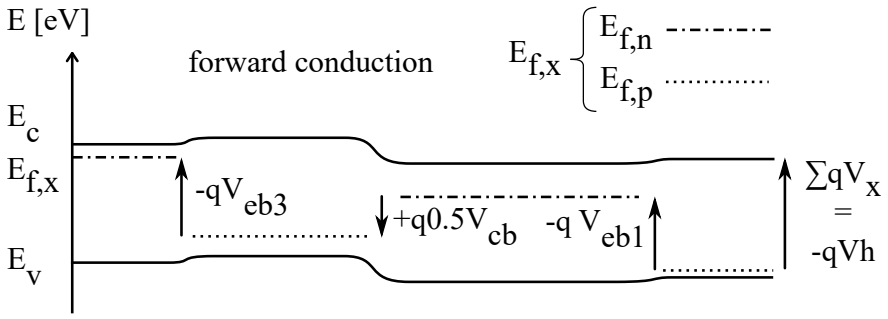



(c)

**Figure 2.9:** Schematic of a pnpn-structure with carrier transition in the base regions together with simplified band diagram at equilibrium and forward conduction. (a) shows the pnpn-structure with its four semiconductor regions and the internal carrier current through the base regions. (b) shows the band-diagram in equilibrium state. (c) shows the band-diagram in forward conduction with the internal junction voltages summed up to the externally measurable $V_h$.

### SCR Device Parameters

The specific pnpn-structure parameters are summarized in Table 2.2.

### Application for ESD protection

The forward conduction state qualifies the SCR as ESD protection structure because of the lower clamping voltage compared to a BJT. In the early 1980's *R. L. Avery* invented one of the first SCR based circuit protection structures [54] which are widely used as on-chip ESD protection structures as they are intrinsically included in CMOS technologies and offer highest ESD performance per silicon area [4], [26], [3].

The pnpn-structure has a low forward voltage in the on-state compared to other state-of-the-art ESD protection devices (e.g. avalanche-diode, npn-transistor) and is known to bare a latch-up risk for certain cases [55]. A possible Latch-up will disturb the IC operation and can lead to damage of IC and protection device. This prevents an effective application of SCR based ESD protection structures for external ESD protection as long as supply voltages ($V_S$) are higher than the $V_h$ or SCR specific latch-up requirements are fulfilled [32], [56].

Figure 2.10 shows examples of pnpn-structures in different technologies which are utilized as ESD protection structures. Lateral structures like in (a) are known in CMOS while (b) and (c) are commonly used in BCD technologies.

Figure 2.11 shows measured high current IV-characteristics of low capacitance TVS devices based on SCR. The expectation of a low forward voltage of about 1 V after triggering is confirmed. The DUT voltage is a function of the device resistance.

$$V_{clamp} = V_h + I_{ESD} \cdot R_{dyn} \tag{2.5}$$

### Switching into Forward Conduction

The switching or triggering of the pnpn-structure is initiated by forward biasing the two emitter-base junctions (compare Figure 2.9(c)) which are formed by $J_1$ and $J_3$. The order is not important and the second base-emitter junction will initiate the latching process. The emitter regions (anode and cathode) inject a high amount of

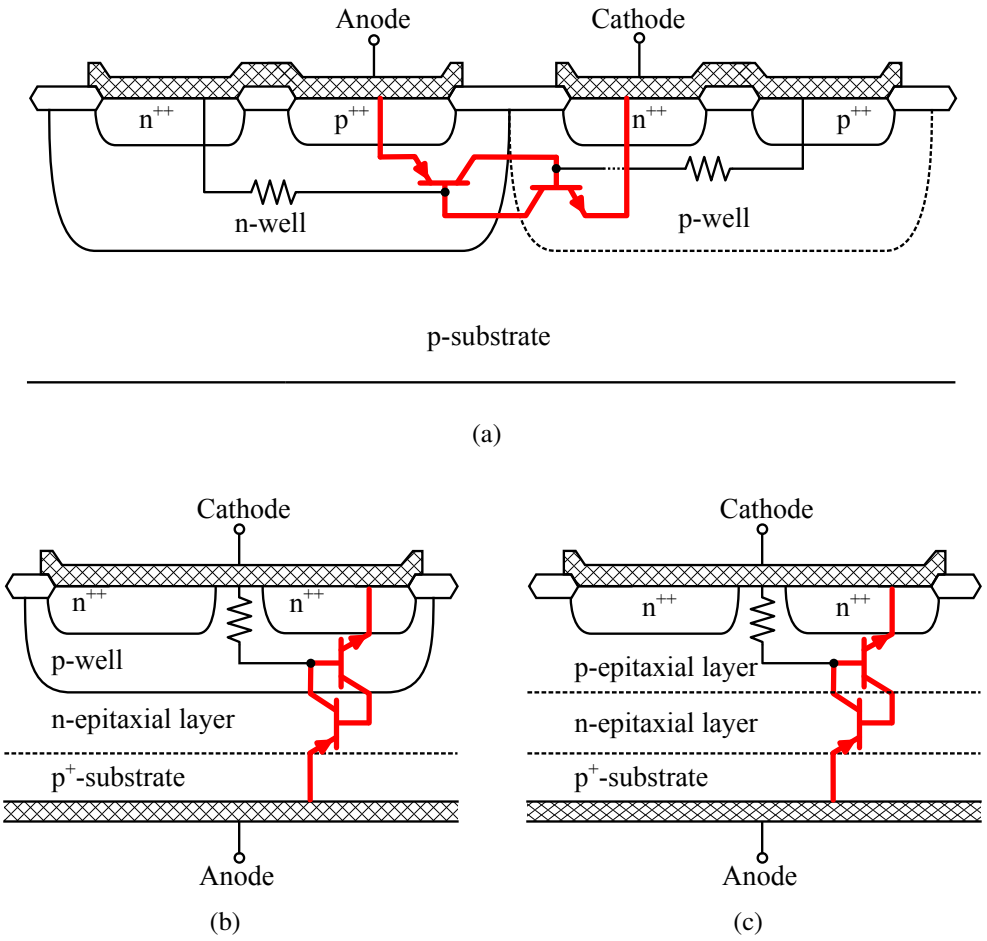



**Figure 2.10:** A schematic cross-section of SCRs in different technologies. (a) is showing a lateral low voltage triggered SCR. (b) shows a vertical SCR with a well diffusion and (c) a vertical thyristor with two epitaxial layers.

minority carriers into the base regions (n-base and p-base). The minority carriers transit the base regions by diffusion and arrive at the collector which is simultaneously the base region of the opposite transistor (compare Figure 2.9(a)). The arrived carriers are changing the electrostatic potential in the base region according to Poisson equation and lead to a forward biasing of $J_2$. All three internal junctions ($J_1$, $J_2$, $J_3$) are forward biased because the emitter-base potential is kept forward biased by the continuous carrier injection from both emitter regions (anode and cathode). The

forward biased $J_2$ is responsible for the injection of carriers from the base into the collector. This operation mode is known as saturation in BJTs and the voltage of $J_1$+$J_2$ or $J_2$ + $J_3$ similar to the collector-emitter voltage ($V_{ce}$) of the individual BJT structure in the SCR [47]. This is shown in Figure 2.9(c) and referring to definition of saturation in BJTs with Equation 2.6.

$$V_{sat} = V_{ce} = V_{be} + V_{cb} < V_{be} | V_{cb} < 0V \tag{2.6}$$

$$V_h = V_{be1} - V_{cb} + V_{be3} = V_{be1,2} + V_{ce} \tag{2.7}$$

The $V_h$ of the pnpn-structure is less than two forward biased pn-junctions[3] and independent of $V_{t1}$. The holding voltage ($V_h$) in a triggered pnpn-structure is the sum of the three junction voltages considering Equation 2.6 and concluded in Equation 2.7. For simplification, one can think of a saturated BJT with a series pn-diode. Figure 2.9(c) shows the band-diagram of a latched SCR and the voltages at $J_1$, $J_2$ and $J_3$ summarized to $V_h$. Resistive voltage drop was neglected for simplification.

The more detailed triggering process is determined by the internal BJT parameters. The internal current gain product of the incorporated pnp and npn specifies the ability of the pnpn-structure to operate at a low forward voltage. A common expression is the unity current gain product described by Equation 2.8. It specifies the stable forward operation of the pnpn-structure after the trigger event (ESD pulse) vanishes.

$$\beta_{pnp} \cdot \beta_{npn} = 1 \tag{2.8}$$

In the following a few mechanisms in the semiconductor which are capable to raise the base current and turn on the SCR by fulfilling Equation 2.8 will be mentioned. These mechanisms are able to generate a base current in the SCR by exposure to light, temperature or external signals to device terminals (e.g. anode). The known SCR trigger mechanisms are the following:

- avalanche carrier multiplication (ACM)
- punch-through (PT)
- thermal-carrier generation (TCG)
- photo-carrier generation (PCG)
- displacement current (DC)

A brief overview of the physical background is given in Table 2.3.

Additional trigger elements can be integrated as individual silicon devices together with the SCR to deliver a base current for triggering. These are well known RC trigger circuits, MOS trigger and pn-diode chains [26]. A commonly used trigger mechanism is the internal junction breakdown of $J_2$ (see Section 2.3.1) which is called *breakover* in a pnpn-structure [47], [48]. Therefore, a two terminal pnpn-structure is called *breakover diode* in literature [46].

### Transient Switching Behavior

As the latching condition and triggering process is established, the transient turn-on process of the SCR will be explained in detail. The carriers from the anode must reach the cathode, hence the anode to cathode distance defines the transit time and the switching time. Figure 2.12 shows the explanation of the turn-on theory in pnpn-structures. The neutral base regions are traversed by the slow diffusion process of the minority carriers described by Equation 2.9. $D_{n,p}$ are the diffusion constant for electrons and holes. $W_{neutr}$ is the width of the respective undepleted neutral base region.

$$\tau_{n,p} = \frac{W_{neutr}^2}{2D_{n,p}} \tag{2.9}$$

A faster transit time is achieved by the drift of carriers through the space charge region. In case of ESD events high current levels increase the majority carrier concentration above the background doping and built up an electric field which enhances the velocity of minority carriers in the neutral regions [4]. Therefore, the transit time decreases by a factor of two and summarized in Equation 2.10

$$\tau_{n,p} = \frac{W_{neutr}^2}{\mathbf{4}D_{n,p}} \tag{2.10}$$

In the following, two different SCR turn-on time models from literature are presented and discussed:

[3] Assuming a forward voltage for pn-junctions of $\approx 0.7$ V and a BJT saturation voltage of $V_{ce} \approx 0.2$ V, the anode to cathode voltage is $V_h \approx 0.9$ V (neglected resistive voltage drop).

- A study of design factors for lateral SCRs in 90nm and 60nm CMOS by *Di Sarro et al.* introduces several time constants which are responsible for the delay in a lateral pnpn-structure [59]. The complete turn-on time is defined by the sum of the internal base transit times and the charging of the base-emitter junction capacitance, described by Equation 2.11.

$$\tau_{delay} = \tau_{npn} + \tau_{pnp} + \tau_{on} \tag{2.11}$$

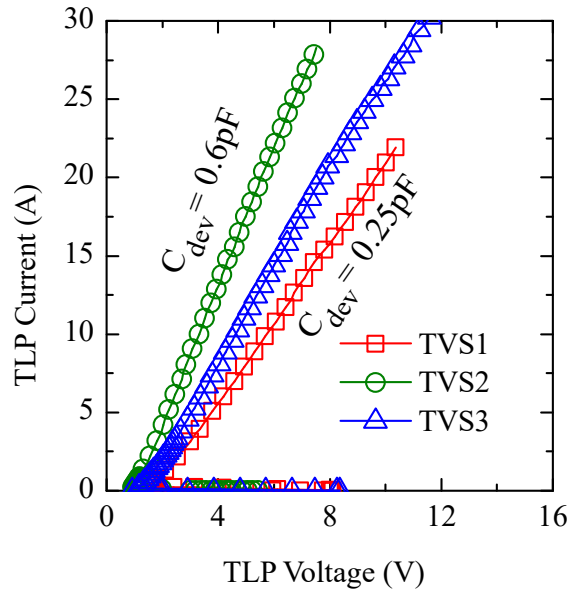
- *Baliga* introduced the turn-on of power thyristors in his textbook by a charge balance method [48] and *Vahler et al.* confirms the Sze-Blicher theory by 2D simulations and experimental data [60]. This is described by Equation 2.12.

$$\tau_{transit} = \sqrt{\tau_{npn} \cdot \tau_{pnp}} \tag{2.12}$$

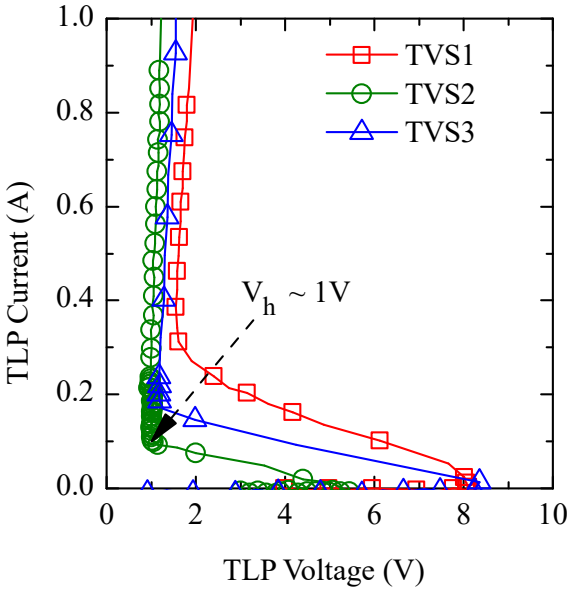
Both models are quite different because *Di Sarro et al.* sums up the transit time of the two internal BJTs with a charging delay while *Baliga* and *Vahler et al.* rely on the geometric mean of the BJT transit times. One major difference is the dimensions of the SCR structures that were investigated. Power devices have much bigger dimensions and high current effects are more dominant compared to CMOS SCRs in 90nm and less. When choosing a turn-on time model, Equation 2.11 should fit better for SCRs that are designed for ESD protection because their dimensions are definitely smaller than power SCRs.

**Table 2.2:** Definition of SCR based ESD protection device parameters.

| Parameter | Description | Comments |
|---|---|---|
| $V_{BO}$ | breakdown voltage of $J_2$ | determined by junction doping profile |
| $V_{t1}$ | ESD protection device trigger voltage | voltage value which triggers the device into its on-state. |
| $I_{t1}$ | ESD device trigger current | minimum current which is needed to start the trigger process of the SCR into on-state |
| $V_h$ | ESD device holding voltage | lowest voltage during on-state |
| $I_h$ | ESD device holding current | current value which is needed to keep the SCR device in the low voltage forward conduction |
| $V_{t2}$ | ESD failure voltage | voltage at which damage occurs to the ESD device |
| $I_{t2}$ | ESD failure current | current at which damage occurs to the ESD device |
| $V_{cl}$ | ESD clamping voltage | clamping voltage of the ESD device during on-state |
| $V_{OS}$ | ESD device voltage overshoot | highest transient voltage response in the time domain |
| $t_{on}$ | ESD device switching time | delay between start of pulse and fully switched on device |
| $R_{dyn}$ | ESD device dynamic resistance | dynamic resistance over a specific current range, high current region |




(a)




(b)

**Figure 2.11:** Measured high-current (TLP) characteristics of external ESD protection devices based on SCRs. Comparison of three external ESD protection devices with different device capacitance ($C_{dev}$) are shown in (a) and a detailed view of the device voltage of the snapback portion of the IV characteristics showing the low holding voltage ($V_h$) in (b).

**Table 2.3:** Overview of the important mechanisms that significantly increase internal currents.

| Mechanism | Specifics | Root Cause |
|---|---|---|
| ACM | super-exponential [57] | sufficient kinetic energy of free carriers to create electron-hole pair by collision with lattice |
| PT | exponential [58] | full depletion of majority carriers in base region |
| TCG | $\propto exp(\frac{-E_g}{mkT})$ [47] | thermal carrier generation and increase of $I_{SCG}{}^4$ with temperature |
| PCG | $\propto h \cdot v > E_g$ [46] | generation of $I_{opt}$ with photon generated electron-hole pairs |
| DC | $C \cdot \frac{dV}{dt}$ [48] | displacement current of majority carriers due to a fast changing potential in pn-junctions |

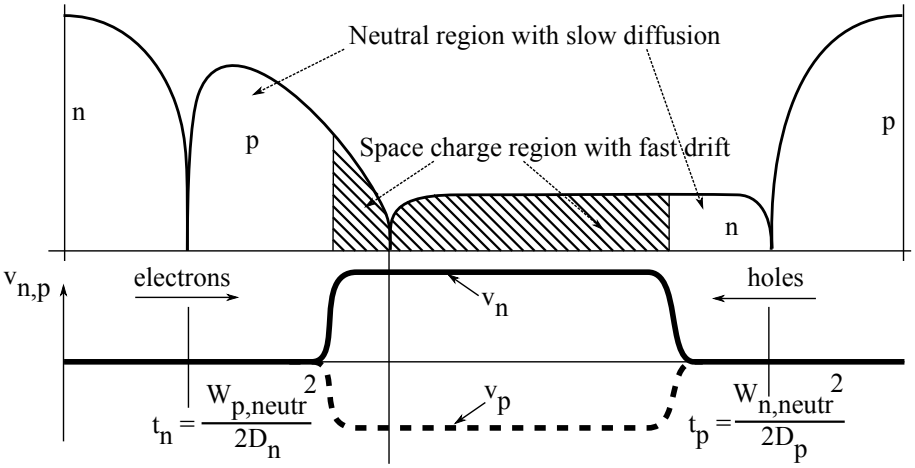



**Figure 2.12:** Illustration of the transit times in pnpn-structure. The non-depleted neutral regions are traversed by diffusion while the depletion region is traversed by drift velocity.

## 2.4 Ultra Low Capacitance Device Concept

### 2.4.1 Junction Capacitance

The capacitance of semiconductor structures are determined by their junction capacitance and additional components like inter-layer dielectric or gate oxides in field-effect structures.

The junction capacitance has a significant share in the overall device capacitance and is calculated by the plate capacitor approximation (Equation 2.13). With $\varepsilon_r$ as the dielectric material constant, $A_{plate}$ the area of the smaller plate and $d_{plate}$ which is the distance between the two plates or the thickness of the dielectric material.

$$C_{plate} = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{A_{plate}}{d_{plate}} \tag{2.13}$$

This approximation is valid because the depleted semiconductor region is free of mobile charges and is treated as dielectric material with $\varepsilon_{Si} = 11.7$ [47]. The depletion region of an abrupt pn-junction is calculated by *Poisson Equation* and the corresponding impurity concentrations of the semiconductor ($N_A$, $N_D$) with Equation 2.14. Here, $w_{depl}$ is equal to $d_{plate}$, while $V_{bi}$ is the built-in potential and $V$ is the applied voltage at the junction.

$$w_{depl} = \sqrt{\frac{2q}{\varepsilon_0 \varepsilon_{Si}} \cdot \left(\frac{1}{N_D} + \frac{1}{N_A}\right) \cdot (V_{bi} - V)} \tag{2.14}$$

Therefore, a large depletion region and a small junction area ($A_{plate}$) are required to minimize the device capacitance.

### 2.4.2 p-i-n Diode Structure

A common low capacitance semiconductor structure is the p-i-n diode which has an intrinsic- ($i$) or lightly doped semiconductor layer ($n^-$ or $p^-$) between the p-doped anode and the n-doped cathode. The $i$-layer is assumed to be fully depleted (Equation 2.14) and leads to a lower capacitance per area compared to a conventional pn-junction [48]. The structure is treated as an abrupt junction until the intrinsic layer is fully depleted. Figure 2.13 shows cross-sections of p-i-n diodes with their equivalent circuits in reverse biased condition. The intrinsic layer is typically lightly doped with acceptors (p) or donors (n) and in this illustration not fully depleted.

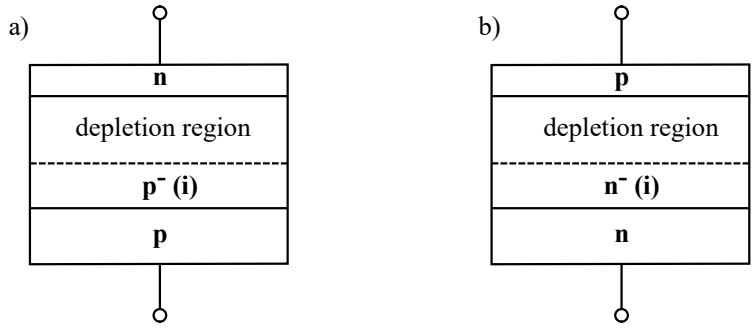



**Figure 2.13:** Cross sections of p-i-n diodes with equivalent reverse biased circuit are shown. (a) shows a diode with a not fully depleted lightly doped p-layer, (b) shows a not fully depleted diode with lightly doped n-layer.

### 2.4.3 Low Capacitance ESD Structures

Connecting a p-i-n diode structure in series to a high capacitance semiconductor device like an *avalanche*- or *Zener* diode (see Section 2.3.1) reduces the overall device capacitance to the value of the p-i-n structure. This approach is commonly used in low capacitance ESD protection devices [61], [62], [38]. The p-i-n structure is integrated as part of the ESD protection structure. Such configuration realizes a transistor structure with a low device capacitance combined with a low breakdown voltage. In detail, the base profile is engineered so that the collector-base junction has a high doping concentration while the base-emitter shows an intrinsic portion of the base with a high emitter doping. Such a concept enables the opportunity to tune the collector-base breakdown voltage independently of the device capacitance. The disadvantage of the described structure is a high breakdown voltage of the low doped base-emitter junction. Two solutions are known which are the following:

- An anti-parallel connection of two discrete devices into one package and forming a two terminal protection device. The capacitance will be the sum of both discrete devices.
- A series connection of two discrete devices that consist of a low capacitance transistor structure and a parallel p-i-n diode. The p-i-n diode has the purpose to offer a bypass path for polarities which would be blocked by the base-emitter of the first transistor. The two devices are connected as back to back

configuration. The capacitance will be half of the transistor plus p-i-n diode device capacitance due to series connection.

Such bidirectional low capacitance ESD protection device is reported in [37].

A typical implementation of a low capacitance ESD protection structure is shown in Figure 2.14.

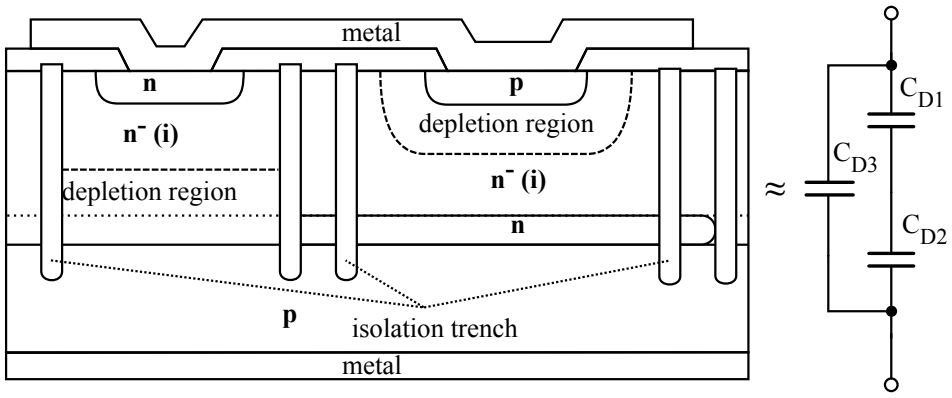



**Figure 2.14:** A typical unidirectional low capacitance ESD protection device structure is shown. A p-i-n diode structure connected in series reduces the overall device capacitance. $C_{D1}$ will dominate in the series configuration with $C_{D2}$. $C_{D3}$ is a n-i-p diode structure in parallel. The overall device capacitance is approximately $C_{D1} + C_{D3}$. The drawing was adapted from *US Patent No. 7538395 B2* [61].

The same principle is applied for SCR based ESD protection devices (see Section 2.3.3) which have three internal pn-junctions in series of which one junction is designed as a low cap junction to minimize the capacitance. *Park et al.* introduced a low-voltage and low-capacitance lateral SCR ESD clamp for radio frequency RF IC protection (component level ESD protection) with 0.213 fF/μm$^2$ and 2 kV HBM robustness [27]. *Notermans et al.* recently published an ultra-low capacitance SCR based ESD protection structure (system level ESD protection) with 0.25 pF which shows a scaling of 10 fF per kV system level ESD robustness [36]. This results in a 100 fF device capacitance for a typical required 10 kV system level robustness. Latest publication from *Qi et al.* [63] shows a non SCR based ILC-TVS low capacitance array with 720 fF and 11 kV which yields 65.5 fF per 1 kV system level

ESD robustness and confirms that SCRs dominate the low capacitance and high robustness field.

# 3 Novel Vertical SCR for System-Level ESD Protection

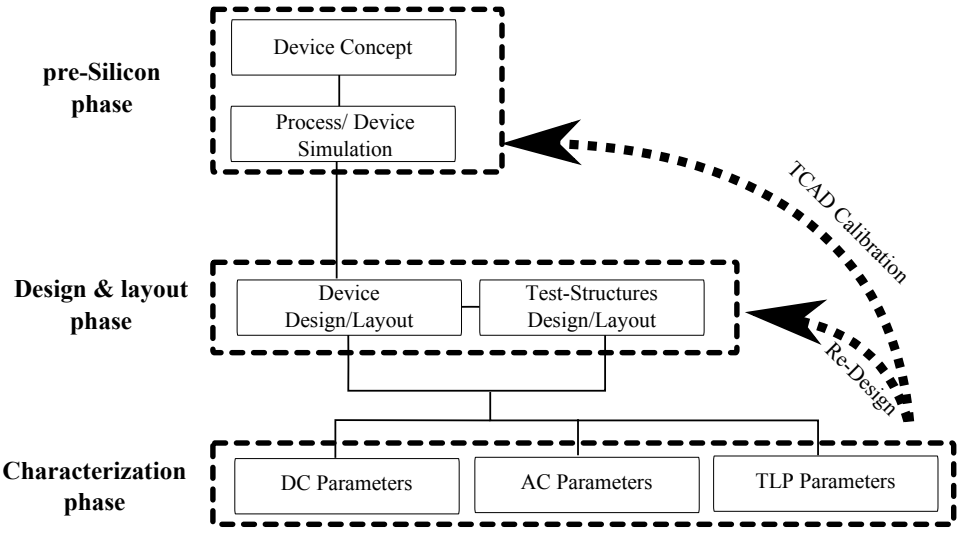



**Figure 3.1:** Development flow for a novel ESD protection device used during this work. The three phases are divided in pre-silicon, design and layout, and characterization. A positive feedback is included after characterization to improve re-design and optimization steps.

## 3.1 Design

This section presents the results of a novel discrete vertical SCR for ESD protection in a submicron bipolar technology. The novelty of the presented structure is the implementation of a vertical pnpn-structure together with a vertical diode in parallel while optimizing the system towards ESD protection performance.

First, a short overview on published results on vertical SCR structures is given.

Second, the dedicated vertical pnpn-structure integrated with a novel structure called the *pn-short* is introduced.

Third, the essential device parameters like capacitance per junction area, emitter-short resistance, internal junction breakdown, trigger-voltage and -current as well as their temperature behavior are explained and verified by experiments.

Finally, an optimization with an integrated lateral trigger structure that improves scalability of trigger-voltage, turn-on time and de-latching behavior is summarized by simulations and measurements for the proposed device structure.

### 3.1.1 Decision for a Vertical Device

Compared to state-of-the-art pnpn-semiconductor based protection structures [3] the complexity and the protection performance per junction area for vertical device technologies is higher and discussed in the following.

Only a few works in the field of vertical protection devices are published yet due to incompatibility to CMOS technology and the use in niche applications as discrete devices like *transient voltage suppressor* (TVS), e.g. in [64], [65], [66], [62].

This work proposes vertical SCRs for system level ESD protection with minimized device capacitance to improve protection performance per femtofarad, aimed at high-speed data line protection (see Section 1.3).

While [65] introduced a vertical DMOS device which forms a parasitic pnpn-structure as high voltage ESD protection most of nowadays published works on SCRs are lateral on-chip silicon-controlled rectifier (SCR) in CMOS technologies [4], [29], [67], [68] and [69], [70], [71], [30].

The ESD protection performance of such devices have continuously improved by reducing the clamping voltage [65], device capacitance [28], [27], [37] and turn-on time [72], [59]. Latest results from [36] and [73] show the lateral SCR structures as discrete protection devices for high speed data lines with a line capacitance below 300 fF and ESD robustness of 20 kV. The performance of the shown devices are benchmark for the structures proposed in this work.

The main advantage of vertical devices is the uniform current distribution and the corresponding increased current capability per junction area compared to lateral devices. This is known from semiconductor power device technologies [48], [46],

also true for the ESD domain[1] and is one hypothesis of this work to investigate vertical SCRs for ESD protection.

Another advantage is the low requirement for lithography resolution because the active device area is formed by epitaxial layers and large-area implantation. Nevertheless, epitaxial layers are more expensive and sensitive to process deviations, directly influencing device performance.

### 3.1.2 Vertical Reverse Conducting Breakover Diode

The basic structure is shown in Figure 3.2 and is called a breakover diode structure. It is similar to the well known *Shockley-Diode*[2]. The breakover structure is named by its trigger mechanism which is the internal junction breakdown of $J_2$ (called *breakover*) [47], [48]. Here, the device breakdown voltage $V_{br}$ is identical to the *breakover voltage* $V_{BO}$ and is an intrinsic device parameter controlled by design.

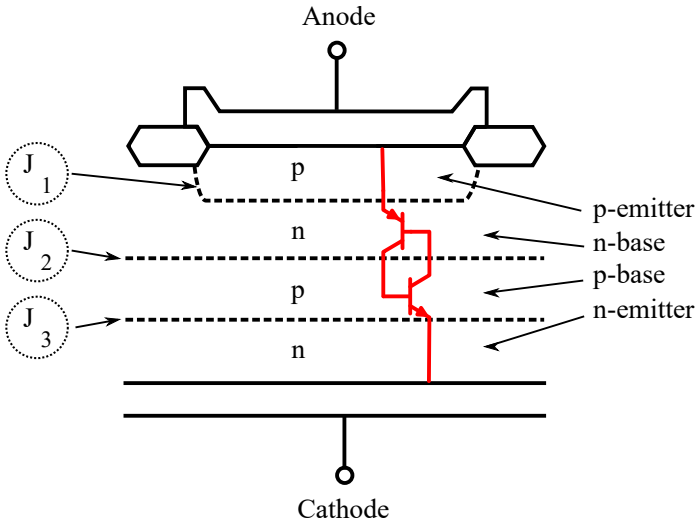



**Figure 3.2:** Schematic cross-section of a vertical breakover diode structure.

[1] ESD is a high power but low energy event [6]
[2] specifies a pnpn-structure with anode and cathode terminal only

Because ESD events occur with both polarities a stand-alone pnpn-structure is disadvantaged at protecting against negative ESD strikes at the anode terminal:

1. The device breakdown voltage ($V_{br}$) for negative voltages at the anode terminal is the sum of the individual breakdown voltage of $J_1$ and $J_3$.
2. There is no regenerative loop (or latch-up operation) in reverse direction because the pnpn-structure operates with two series diodes in reverse breakdown (avalanche).

Therefore, the robustness per area is similar to an avalanche diode and very low compared to the forward conduction of an pnpn-structure because:

1. Due to a higher power dissipation in reverse conduction operation compared to forward conducting operation ($P_{min} = A_{junction} \cdot J_{junction} \cdot V_{br}$)[3].
2. The power dissipation takes place in a small volume in the depletion region with the highest electrical field and leads to a thermal breakdown due to joule heating [51].

Due to the stated reasons an additional protection structure which is able to conduct the negative ESD current has to be placed in parallel to the pnpn-structure. The combination of a Shockley-diode with a parallel pn-diode is called a *reverse conducting breakover diode* and is illustrated in Figure 3.3. The integration of both structures in one silicon substrate is beneficial but requires differently doped substrates or a heavy backside implantation to switch from n-doping to p-doping and vice versa.

A new device concept is proposed in this chapter by embedding both structures in an n-type substrate and electrically short the undesired pn-junction [74], [75] by processing both structures on a common substrate. This is briefly described in the following subsections.

### Discrete ESD Structure Definition

The reverse conducting breakover diode is commonly used as vertical four-layer device for external ESD protection because it only requires two terminals and protects applications with unipolar signals.

[3] the smallest junction determines the robustness, assuming a homogeneous current density

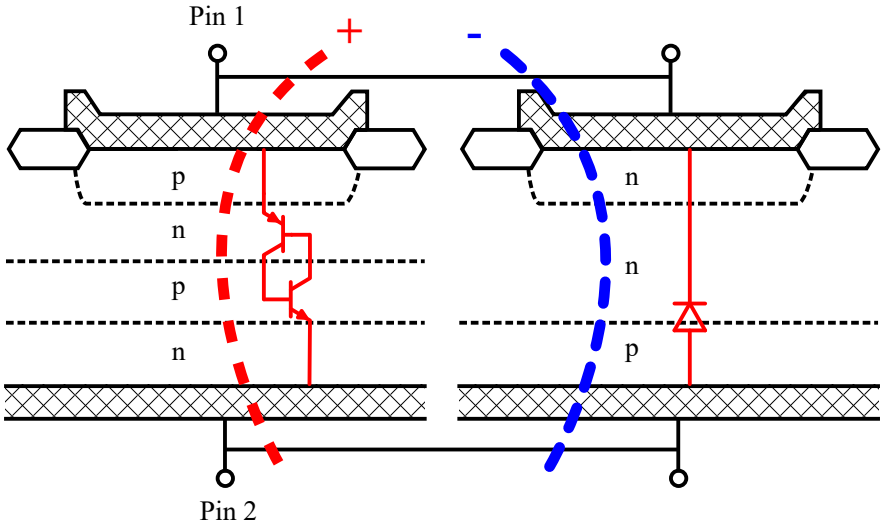



**Figure 3.3:** Schematic cross-section of a vertical reverse conducting breakover diode structure. A parallel pn-diode structure is conducting the negative ESD current. An isolation between the two structures is required.

A schematic of a device concept for a discrete reverse conducting vertical breakover diode is shown in Figure 3.4. The vertical pnpn-structure is isolated from the parallel reverse diode by junction isolation (p-sinker). The p-anode region forms the junction $J_1$ to the n-layer with a corresponding junction capacitance. $J_1$ determines the capacitance of the vertical pnpn-structure and depends on junction area $A_{J1}$ and doping level $N_{D4}$ of the n-layer (see Section 2.4). The n-layer is not connected to any terminal and has a floating potential which is coupled to the neighbor regions by the built-in potential in equilibrium.

The emitter short is required to define the device trigger current [48] and is realized by connecting the p-doped buried layer with the n-substrate by a pn-junction short structure (Section 3.3.3). The parallel pn-diode structure is formed by the buried p-layer and p-sinker surrounding the n-layer ($A_{JD}$). The capacitance of the formed junction increases the overall silicon device capacitance and has to be minimized in low capacitance devices.

A complete discrete ESD protection diode is shown in Figure 3.5. The introduced chip is integrated in a molded package and connected with a bond wire to Pin1 while

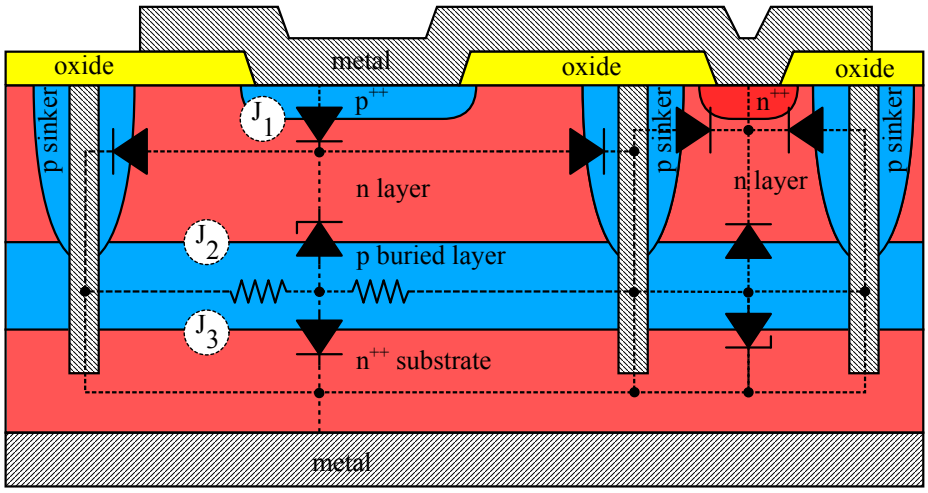



**Figure 3.4:** A schematic cross-section of a discrete reverse conducting vertical pnpn-structure for external ESD protection with integrated parallel diode structure. A junction isolation is used in combination with a unique pn-junction short [76] (indicated by the metal-filled trench structure).

sitting on Pin2. This discrete protection diode is placed on a PCB to protect ICs against system level ESD.

### 3.1.3 Device Capacitance Components

The device capacitance of discrete semiconductor device consists of several capacitance components like the junction capacitance, metal capacitance and parasitic stray capacitance. Here, the package is neglected as it is exchangeable and a constant addition. An overview of the existing capacitance shares in the introduced vertical structure is shown in Figure 3.6.

A detailed circuit representation of the protection device with its corresponding internal transistor, diode and capacitance components is shown in Figure 3.7. The schematic on the right side represents the unidirectional device modeled by transistors

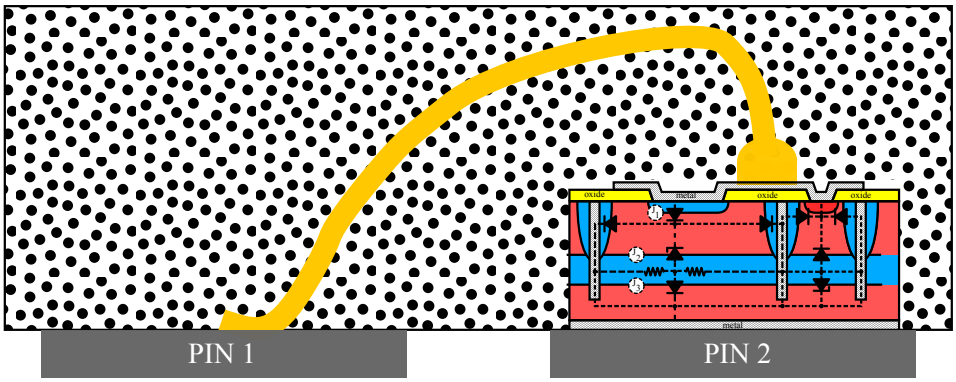



**Figure 3.5:** A schematic of a discrete ESD protection diode showing the ESD protection structure sitting in a package.

and on the left side the corresponding capacitance components are shown. $T_{V1}$ and $T_{V2}$ are formed by the vertical pnpn-structure, $T_{L1}$ is a lateral transistor that is formed by the p-sinker and the pn-short ($R_{cl}$). $R_1$ is the lateral resistor formed by the p-buried layer connected by the pn-short and $R_{sub}$ is the substrate resistance. Here, the overall device capacitance can be narrowed down to three main capacitance components. These are the series common shared emitter-base capacitance $C_{EB,L1}$ and $C_{EB,V1}$ of the positive ESD structure, the junction capacitance $C_{BD}$ of the negative ESD structure and the metal capacitance $C_{met}$. The simplified model was used for optimization toward lowest capacitance by measuring the device capacitance and extraction of the main components by solving the system of linear equations.

### Anode Junction Capacitance Extraction

The anode junction capacitance that corresponds to $C_{EB,L1} = C_{EB,V1}$ was extracted by on-wafer measurements of test structures. The metal capacitance is scaling with metal area because the back-end-of-line[4] (BEOL) is similar for all structures.

Different anode shapes were investigated and summarized in Table 3.1. Different geometries like circles and donut shapes were evaluated to extract the vertical

[4]all processes containing the inter-metal-dielectrics and metal interconnections in a technology

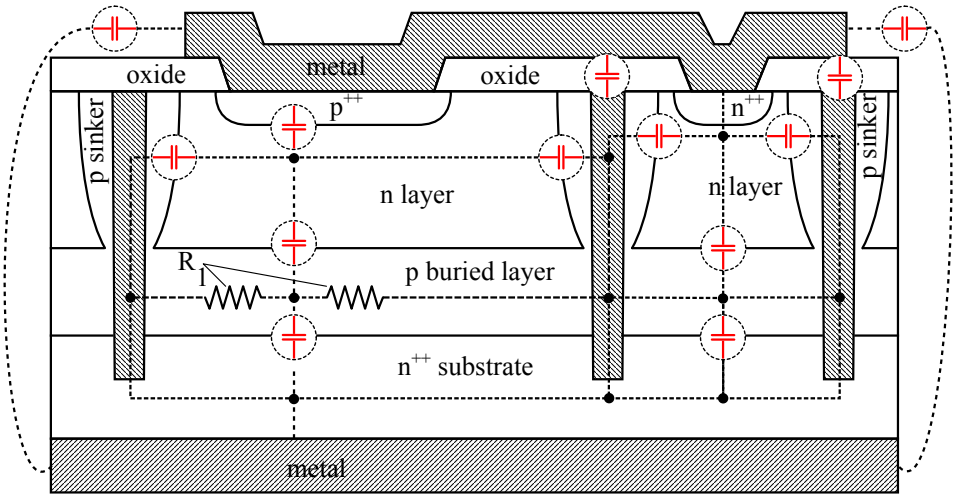



**Figure 3.6:** An overview of capacitance components in a unidirectional ESD protection device is shown. The junction capacitance has the major share and is divided in several regions. The front side metal layer has a parasitic capacitance to the pn-shorts and to the backside metal. The strain capacitance represented by the dashed lines is negligible due to the huge distance to the opposite terminal. The package capacitance is missing.

junction capacitance ($c_{vert}$) versus the border capacitance ($c_{lat}$). The corresponding set of linear equations are solved in Equation 3.1.

$$\vec{c}_{comp} = A^{-1} \cdot \vec{c}_{meas} \tag{3.1}$$

$$\vec{c}_{comp} = \begin{bmatrix} c_{vert} \\ c_{lat} \\ c_{met} \end{bmatrix} \tag{3.2}$$

Table 3.1 summarizes the results and shows the advantage of a circle anode design due to minimized border area. The extracted lateral capacitance per perimeter is significantly higher than the vertical junction capacitance for example in structure

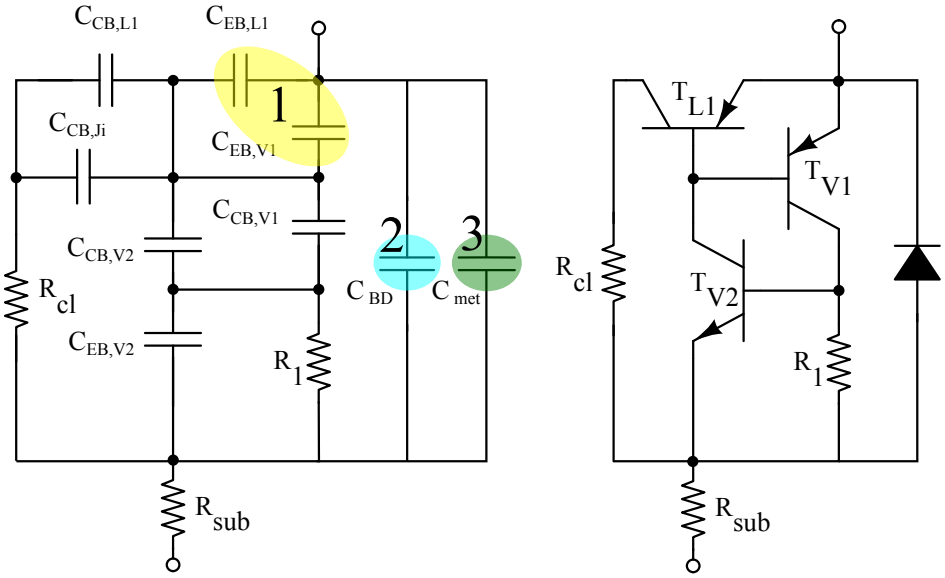



**Figure 3.7:** A detailed capacitance circuit model of the proposed unidirectional protection device is shown. On the right, the three transistors ($T_{V1}, T_{V2}, T_{L1}$) and two diodes represent the ESD structure. On the left, all device elements are substituted with their capacitance models. The overall device capacitance is reduced to three main components ($C_{EB,L1} + C_{EB,V1}, C_{BD}$ and $C_{met}$).

*A*8. One reason for the high border capacitance is the fact that the border region of the junction is adjacent to the $Si/SiO_2$ interface which has an influence on the depletion region and is explained in the following. First, a segregation effect takes place during formation of the field oxide (see Chapter 3.3.1), which accumulates dopands at the silicon interface and lead to an increase of doping concentration for n-type silicon (known as pile-up). The accumulated region decreases the depletion width and increases capacitance per area. Second, electrical charges in the $Si/SiO_2$ interface (due to *dangling-bonds*), which are also known as *charge traps*, represent a positive charge $Q_{ox}$ in the $SiO_2$ and lead to an accumulation of free electrons at the $Si/SiO_2$ interface, which again decrease the depletion region of the junction near the interface [77]. Oxide charges around $1 \cdot 10^{10}\,\mathrm{cm}^{-2}$ to $1 \cdot 10^{12}\,\mathrm{cm}^{-2}$ are reported in the literature [78], [79] and significantly impact the junction capacitance of layouts with large border area (e.g. wide finger structures). An illustration of the described effect is shown in Figure 3.8. A comparison of the extracted junction capacitance

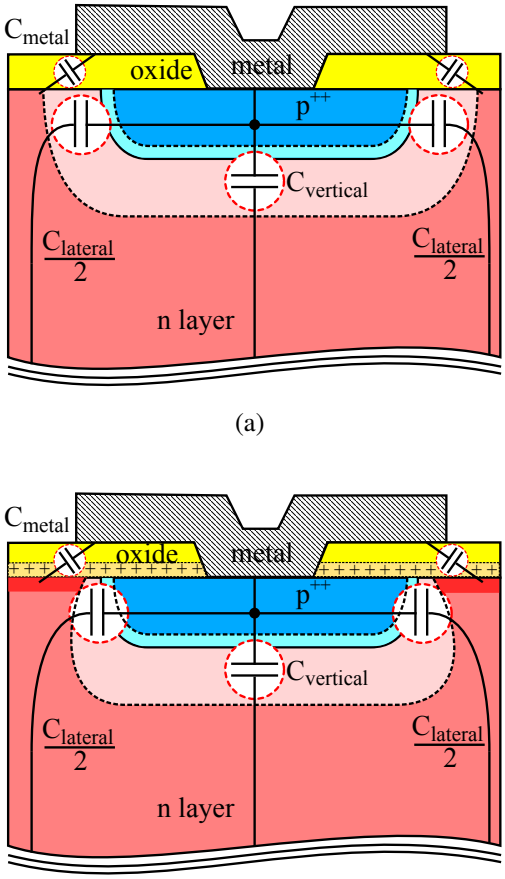



**Figure 3.8:** Two schematics of the anode junction with their capacitance components are shown. An ideal capacitance model is shown in (a), which assumes a homogeneous depletion region. A more realistic capacitance model is shown in (b), which includes several parasitic effects. The oxide charges $Q_{ox}$ and the *pile-up effect* are responsible for a non-ideal depletion region width and increased border capacitance.

per area with analytical calculations of abrupt pn-junctions versus 1D and 2D device simulations are illustrated in Figure 3.9. The extracted capacitance per area matches quite well with the device simulations. The analytical calculation underestimates the capacitance values by more than 30% due to the missing junction border.

**Table 3.1:** Measured device capacitance and calculated junction capacitance shares based on Equation 3.1.

| Geometry | Metal Area $[\mu m^2]$ | Vertical Junction Area $[\mu m^2]$ | Junction Border $[\mu m]$ | $C_{DUT}(0V)$ (measured) $[fF]$ |
|---|---|---|---|---|
| A1 | 3978 | 1964 | 157 | 170 |
| A2 | 6245 | 2116 | 604 | 330 |
| A3 | 3743 | 2196 | 460 | 270 |
| A4 | 6644 | 2011 | 619 | 340 |
| A5 | 8167 | 2036 | 679 | 350 |
| A6 | 7864 | 1185 | 498 | 290 |
| A7 | 6243 | 3906 | 591 | 400 |
| A8 | 8951 | 1975 | 830 | 415 |
| $C_{lateral}$ (calculated) | $\approx 0.2776$ | $\left[\frac{fF}{\mu m}\right]$ | | |
| $C_{vertical}$ (calculated) | $\approx 0.0422$ | $\left[\frac{fF}{\mu m^2}\right]$ | | |
| $C_{metal}$ (calculated) | $\approx 0.0115$ | $\left[\frac{fF}{\mu m^2}\right]$ | | |

### Buried Junction Capacitance Extraction

The parallel buried junction capacitance $C_{BD}$ is determined by the deep junction isolated with deep trench structures. In order to extract the capacitance per area two test structures in a ring shape with different areas were used and are shown in Figure 3.10. The two diodes differ in junction area by alternating the trench isolation. For example, D1 (Figure 3.10(a)) has no trench inside the diode while D2 (Figure 3.10(b)) has. The two structures are not ideal to extract all capacitance components because there is no information about the lateral border capacitance in the buried junction in D1 and D2. Additionally, parasitic effects similar to the

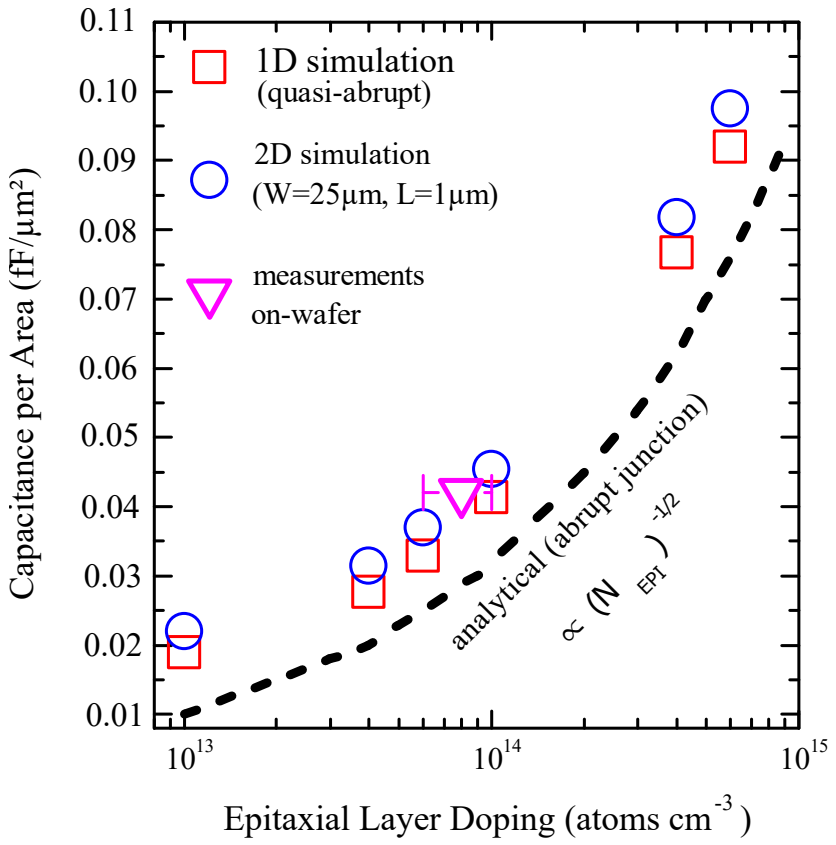
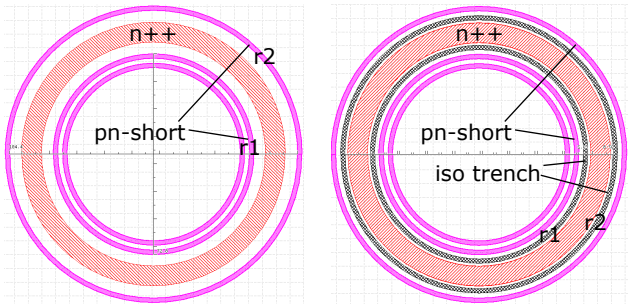



**Figure 3.9:** Normalized junction capacitance per area. On-wafer measurements are matching well with simulated values, especially the 2D simulations. Analytical calculations predicting lowest values. The junction border capacitance has a significant share which is underestimated by analytical calculations due to the abrupt pn-junction approximation.

pile-up effect at the anode junction are valid for the trench isolated structure D2 and cannot be separated. In Table 3.2 the junction areas and the measured capacitance values at 0V are shown with the calculated capacitance per area for both diodes. Both




(a) (b)

**Figure 3.10:** Two layout schematics of ring shaped diodes with different junction areas are shown. The junction area is determined by r1 and r2. a) shows a junction isolated diode formed by pn-shorts and b) a trench isolated diode.

calculated values include uncertainties which cannot be specified with the available structures.

**Table 3.2:** Measured device capacitance and calculated junction capacitance per area.

| Geometry | Vertical Junction Area $[\mu m^2]$ | $C_{DUT}(0V)$ (measured) $[fF]$ |
|---|---|---|
| D1 | 4400 | 290 |
| D2 | 2550 | 180 |
| $C_{D1}$ (calculated) | $\approx 0.065$ | $\left[\frac{fF}{\mu m^2}\right]$ |
| $C_{D2}$ (calculated) | $\approx 0.07$ | $\left[\frac{fF}{\mu m^2}\right]$ |

### 3.1.4 Determination of Emitter-Short Resistance

The design of the emitter short is crucial for the definition of the trigger current ($I_{t1}$) and trigger voltage ($V_{t1}$) of the pnpn-structure. For vertical structures, the lateral base resistance has to be determined.

The following results are based on cylindrical structures due to their homogeneity. Figure 3.11 summarizes the important parameters which determine the triggering for the vertical breakover diode structure.

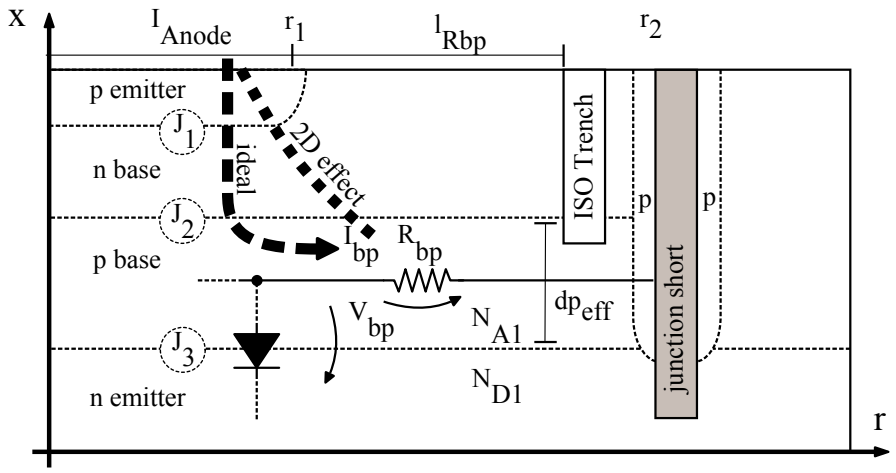



**Figure 3.11:** Illustration of a cylindrical pnpn-structure with a substrate emitter-short. The lateral p-base resistance $R_{bp}$ is determined by $N_{A1}, l_{Rbp}$ and $dp_{eff}$.

To design the trigger point of the pnpn-structure the well known cathode short concept which was introduced by *Baliga et al.* is used [48]. The structure in this work was modified by inverting the *Baliga's structure* which has the cathode on top. Here, the *pn-junction short* enables the connection of the p-base to the substrate (see Section 3.3.4).

The triggering of the pnpn-structure is achieved by forward biasing the substrate diode (n-emitter) which is formed by $J_3$. This happens approximately when the voltage $V_{bp}$ across $R_{bp}$ approaches the built-in potential[5] of $J_3$ [48]. Equation 3.6 is

[5] full forward biased diode

used to estimate the trigger current. A more detailed description of the exact trigger condition can be found in Section 4.1.2.

The built-in potential can be calculated by Equation 3.3 and is determined by the acceptor ($N_A$) and donor ($N_D$) doping concentration and the effective intrinsic carrier concentration ($n_i$).

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_{A1} \cdot N_{D1}}{n_i^2}\right) \tag{3.3}$$

The voltage drop is caused by the p-base current $I_{bp}$. To determine the required trigger current $I_{pb}$ the value of $R_{bp}$ is calculated by Equation 3.4 and Equation 3.5 for cylindrical devices.

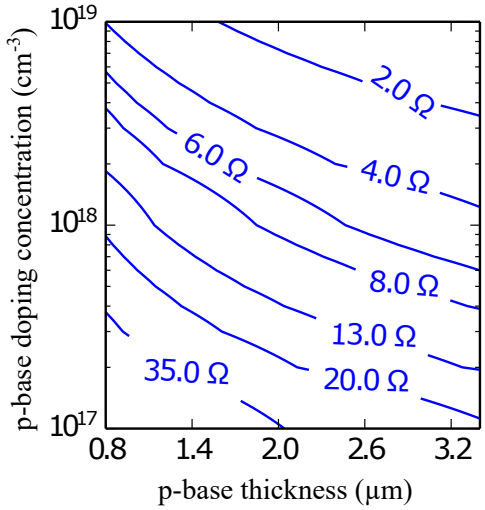
$$R_{bp} = \int_{r_1}^{r_2} \frac{1}{dp_{eff}} \frac{\rho_{pb}}{2\pi r} dr = \frac{\rho_{pb}}{2\pi} \cdot \ln\left(\frac{r_2}{r_1}\right), \quad l_{Rpb} = r_2 - r_1 \tag{3.4}$$

$$\rho_{bp} = \left(q\mu_p \int_{x_{j2}}^{x_{j3}} N_{A1}(x)dx\right)^{-1}, \quad dp_{eff} = x_{j2} - x_{j3} \tag{3.5}$$

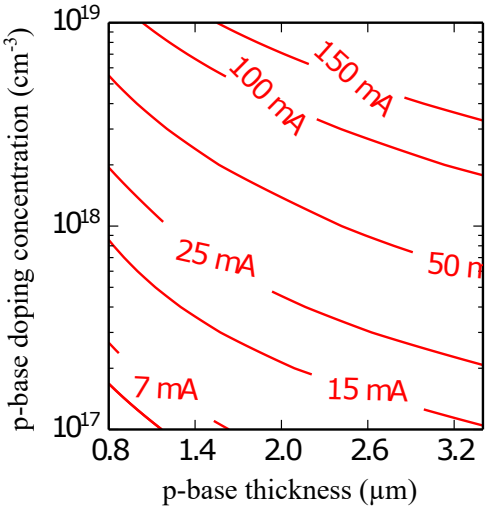
$$I_{pb} \approx \frac{V_{bi}}{R_{bp}} \tag{3.6}$$

Figure 3.12 shows the calculated values for various uniform p-base doping $N_A$ and p-base thickness $dp_{eff}$ with constant $l_{Rbp}$. For simplicity, $V_{bi} = 0.7V$ is assumed. However, $V_{bi}$ increases for high doped junctions and leads to higher trigger currents as well. High trigger current is required for some applications and is achieved by increasing the p-base doping concentration and increasing the effective p-base width.

Comparing DC measurement results of cylindrical devices (shown in Figure 3.13), the circle design has a larger $l_{Rpb}$ with $r_1 = 24\,\mu m$ while the ring design has a short $l_{Rpb}$ with $r_0 = 32\,\mu m$ and $r_1 = 38\,\mu m$ with $r_2 = 50\,\mu m$. The extracted $It_1$ is higher for shorter $l_{Rbp}$ as expected from Equation 3.5. However, the trigger current is inversely proportional to $R_{bp}$ and the circle design has two times higher $R_{bp}$ in the measured device.

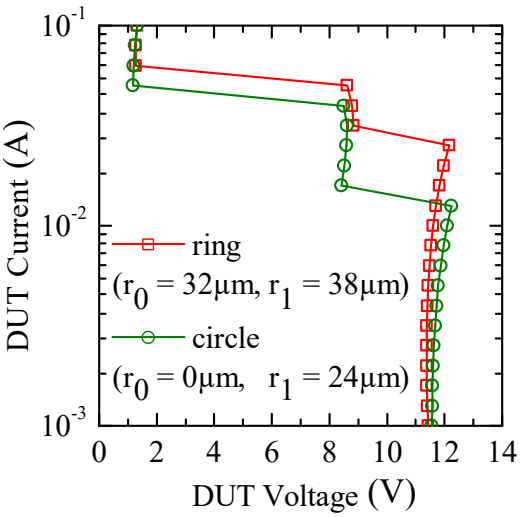



(a)

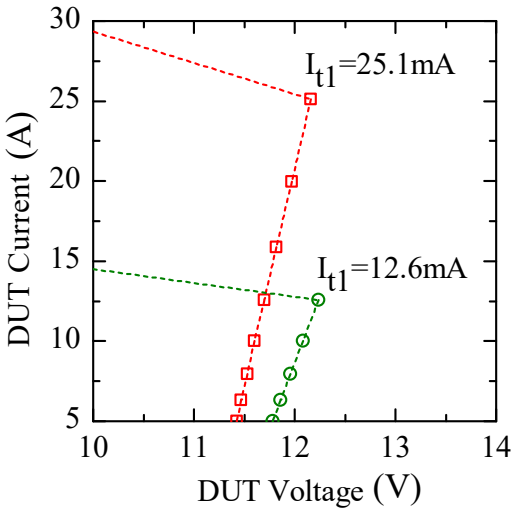



(b)

**Figure 3.12:** Calculated resistance values of the buried layer according to Equation 3.4 for a cylindrical design. Following design parameters were used: $r_2 = 50\,\mu m$, $r_1 = 30\,\mu m$.




(a)




(b)

**Figure 3.13:** Measured DC trigger currents $I_{t1}$ (Equation 3.6) for a cylindrical design with circle and ring anode. In (a) the triggering to the low holding voltage of the pnpn is illustrated, while (b) shows the extracted $I_{t1}$ values

### 3.1.5 Influence of the Isolation Trench Depth

The trench depth is a critical parameter which influences device functionality and across the wafer due to processing. Additionally, the layout of the trench has further impact due to the influence of aspect ratio and occupancy rate on etch depth.

The influence of the isolation trench depth ($d_T$) variation was evaluated by DC measurements and extraction of the trigger current which is directly related to $d_T$ and shown in Figure 3.14. The trench depth was varied by -3% and +9% in depth to investigate the influence on the effective buried layer thickness $d_2$ and the resulting trigger current of the pnpn-structure. As the exact depth of the trench is unknown because it requires in-situ analysis with cross-sections only a relative statement of the results is valid.

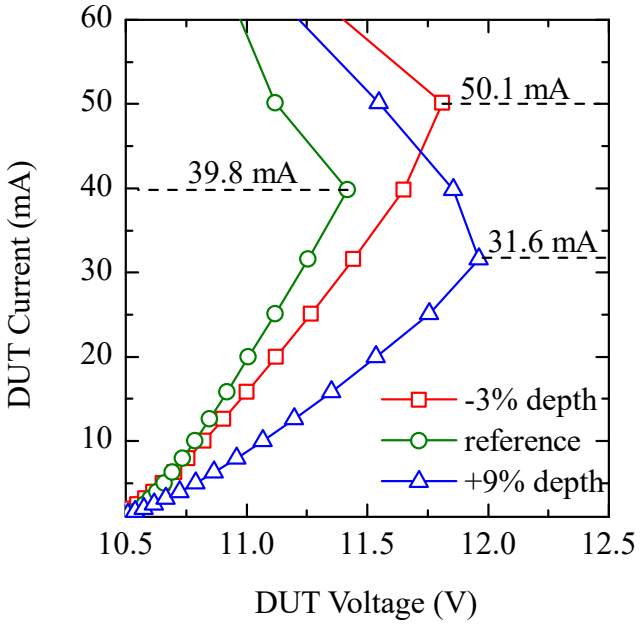



**Figure 3.14:** Influence of the isolation trench depth on device trigger current measured by DC conditions. The triggering is identified by reaching the voltage maximum. Variation of trench depth has strong impact on trigger current due to influence on the buried layer cross section (lateral resistance).

The trigger current increases with less deeper trench as expected because the cross section below the trench is bigger and less resistive. This is partially explained by the non-uniform doping of the buried layer which is schematically illustrated in Figure 3.15. The trigger current is roughly determined by Equation 3.6 and the buried layer resistance is calculated by Equation 3.4 and Equation 3.5. The bottom of the trench determines the effective doping at the cross section and $d_2$.

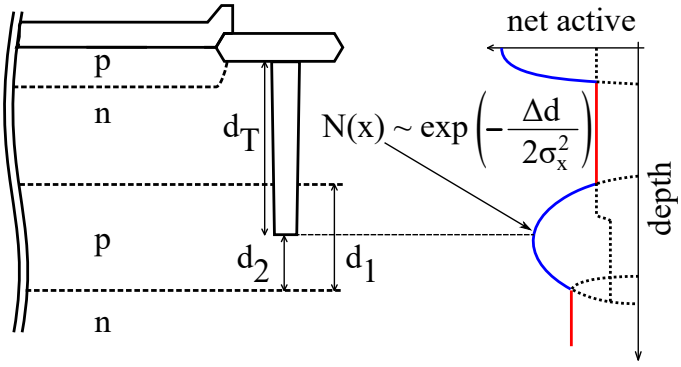



**Figure 3.15:** Schematic cross-section of a trench isolated vertical pnpn-structure. The trench depth $d_2$ determines the effective lateral cross section of the buried layer. $d_1$ is the buried layer thickness and $d_T$ is the trench isolation depth. The doping concentration $N(x)$ of the buried layer has a *Gaussian* distribution and determines the sheet resistance of the buried layer.

The presented results show the relative influence of the isolation trench depth $d_T$ on the trigger current which is depending on the buried layer thickness $d_2$ and the net active doping concentration $N(x)$. The deviation in the trigger current is significant and has to be considered in device concepts with trench isolation. As $d_1$ scales down the trench isolation concept is not recommended anymore because the probability of $d_2 > d_1$ or $d_2 \leq 0$ increases and leads to device failures.

### 3.1.6 Temperature Dependence of Device Parameter

The temperature dependence of device parameters is important because specific parameters significantly change their values for increased temperatures which is critical in applications. As SCRs consist of three pn-junctions several parameters

are responding to temperature variations and change their values, e.g. the built-in potential of pn-junctions [47].

The three most important parameters for the pnpn-structure are investigated and shown in, which are the following:

1. $V_{CE0}$ - snapback voltage after breakdown
2. $I_{t1}$ - trigger current
3. $V_h$ - holding voltage

Figure 3.16 shows a typical voltage-current characteristic of a pnpn-structure with the specified parameters and their temperature trajectories.

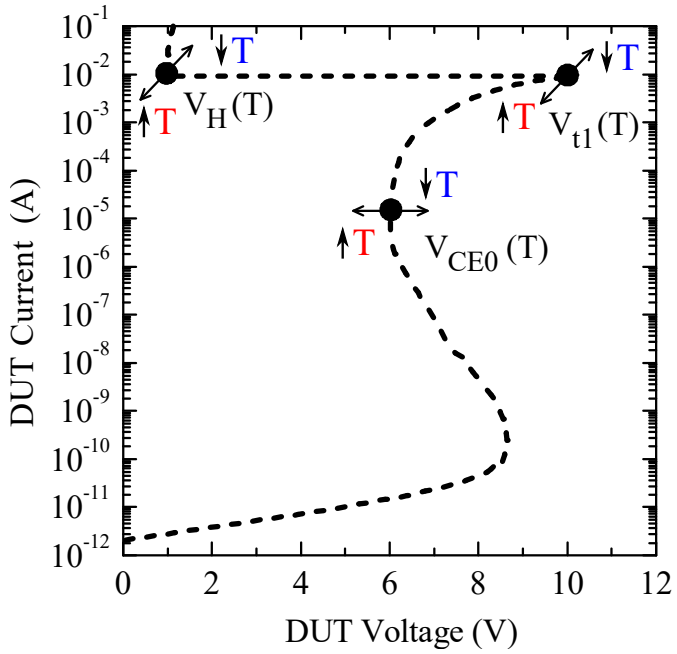



**Figure 3.16:** Schematic voltage-current characteristic of a pnpn-structure. Three of the important device parameters are indicated with the corresponding temperature-dependent transition.

The device voltage in the breakdown regime ($V_{CE0}$) is lower than the junction breakdown voltage which is known as *snapback* and is an intrinsic parameter of the internal transistor structure [5]. It was previously explained that the pnp-transistor structure is in open base configuration and its internal gain is depending on temperature. Due to the decrease of the built-in potential at the base-emitter junction the emitter efficiency is increasing. As a result more carriers from the emitter are involved in the avalanche process and lower the required terminal voltage which is needed to conduct the forced device current.

Figure 3.17 shows the measured current-voltage characteristic of a pnpn-structure for different temperatures. The reverse current increases due to thermal carriers. Additionally, the snapback at lower currents increases compared to currents above 1 µA at $T = 85\,^{\circ}C$.

The current gain at room temperature in the low current region is dominated by generation-recombination. This confirms the increase in gain due to thermal generation.

Also, the junction breakdown voltage is expected to increase because of the positive temperature dependence of the avalanche process. While the measurement results show a decrease in $V_{CE0}$ $V_{SB} = 6.85\,V$ at $T = 35\,^{\circ}C$ to $V_{SB} = 6.5\,V$ at $T = 85\,^{\circ}C$, the current gain is the dominating mechanism in SCRs.

The trigger current $I_{t1}$ indicates the switching of the pnpn-structure into its low forward voltage state and depends on the internal gain product ($\beta_{npn} \cdot \beta_{pnp}$) of the pnpn-structure which is explained briefly in Section 4.1. Again, the gain increases with temperature and lowers $I_{t1}$. Additionally, the base-emitter shunt resistance ($R_{be}$), which controls the base-emitter voltage, increases with temperature due to lower mobility in silicon for higher temperatures.

Figure 3.18 shows measured trigger currents at different temperatures and confirms the theoretical prediction. The trigger current decreases from $I_{t1} = 19.9\,mA$ at $T = 23\,^{\circ}C$ to $I_{t1} = 10.4\,mA$ at $T = 147\,^{\circ}C$. By fitting the $I_{t1}$ values over temperature a linear dependence is extracted with a slope of $\frac{I_{t1}}{K} = 74\,\mu A/K$ (Figure 3.18(b)).

Assuming a typical pn-diode forward voltage dependency of $-1.5\,mV\,K^{-1}$ at the base-emitter junction and a base-emitter shunt resistance of $R_{be} = 20\,\Omega$, the theoretical temperature of $74\,\mu A/K$ is calculated by Equation 3.7. This result matches

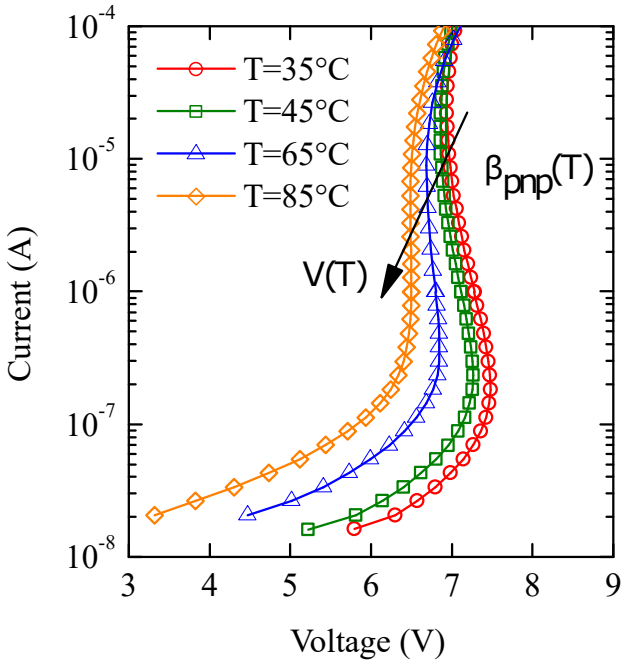



**Figure 3.17:** Measured current-voltage characteristic of a pnpn-structure at different temperatures. The internal open base pnp-transistor shows a snapback which is increasing for higher temperatures.

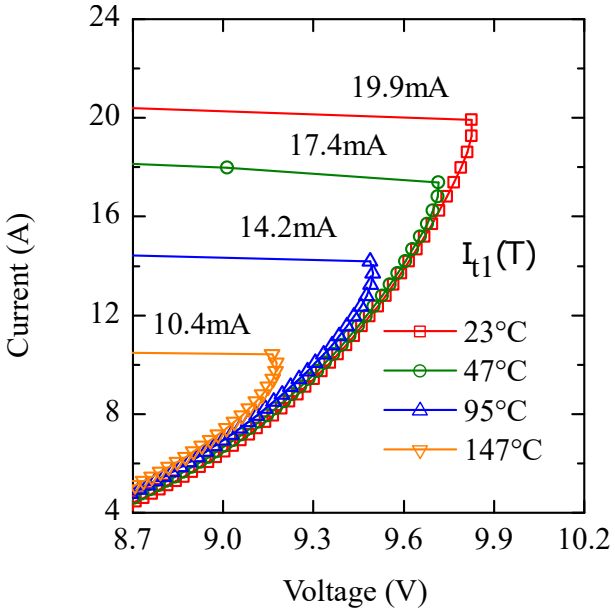
with the measurement data and identifies the built-in voltage of the base-emitter junction as dominant parameter.

$$I_{t1}(T) = \frac{V_{bi}(T)}{R_{be}} = \frac{V_{bi}(300K)}{R_{be}} - \underbrace{\frac{-1.5\,\mathrm{mV\,K^{-1}}}{R_{be}}}_{\frac{I_{t1}}{K}} \tag{3.7}$$

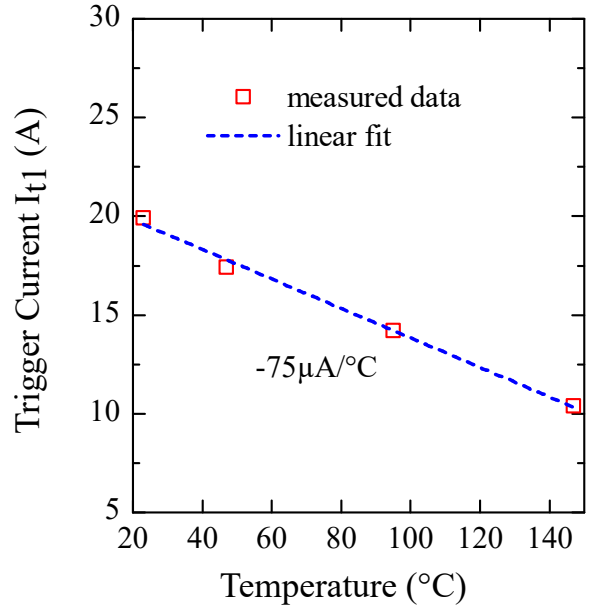
The holding voltage $V_h$ determines the lowest possible voltage between the anode and cathode terminal. $V_h$ is reached after the pnpn-structure is switched into its on-state. The temperature dependence is obvious because $V_h$ is the sum of the three internal junction voltages in a pnpn-structure.

Figure 3.19 shows measurement data of $V_h$ for elevated temperatures and confirms the decrease toward higher temperatures. Figure 3.19(b) shows a linear dependence on temperature. Again, this is explained by the temperature dependence of the internal junctions. The measured structure has an additional pn-diode in series which explains the higher $V_h$ of about 1 V compared to a stand alone pnpn-structure. Taking into account the two forward biased base-emitter junctions and the additional forward diode a negative temperature dependency of $-1.59\,\mathrm{mV\,K^{-1}}$ per pn-junction is calculated by assuming three identical pn-junctions. This result matches with the extracted temperature behavior of $I_{t1}$.

Finally, the results highlight the temperature dependence of silicon pn-junctions, which is typically $-1\,\mathrm{mV\,K^{-1}}$ to $-2\,\mathrm{mV\,K^{-1}}$, as the main key parameter in pnpn-devices.

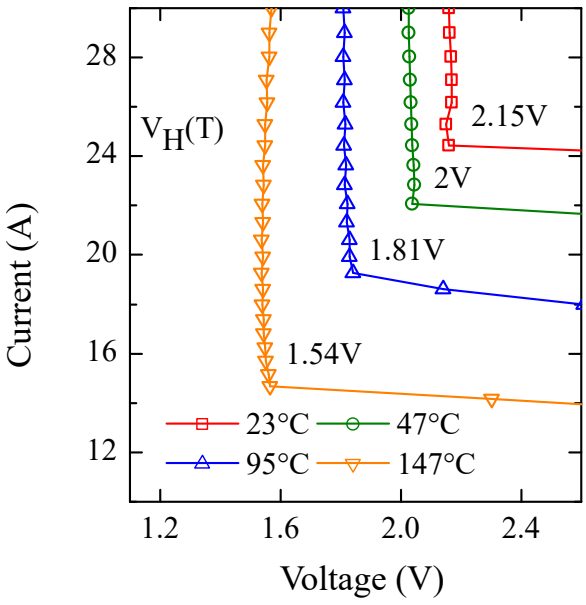



(a)

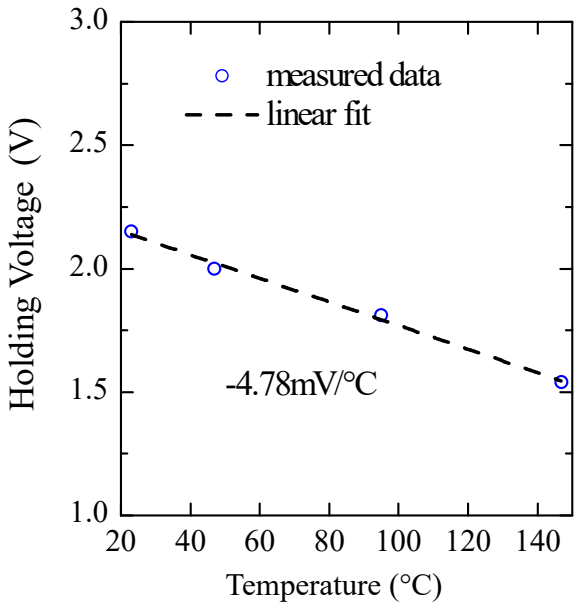



(b)

**Figure 3.18:** Measured temperature dependence of the DC trigger current in a pnpn-structure. The trigger current is decreasing for higher temperatures. The linear plot (a) is illustrating the decrease of the trigger current in the mA range while (b) is showing the extracted linear temperature dependency of the trigger current.




(a)




(b)

**Figure 3.19:** Measured temperature dependence of the DC holding voltage in a pnpn-structure. The holding voltage is decreasing for higher temperatures. The linear plot (a) is illustrating the decrease of the holding voltage while (b) is showing the extracted linear temperature dependency of $V_h$.

## 3.2 Device Simulation

During pre-silicon phase technology computer aided design (TCAD) software is used to set up a 1D, 2D or 3D device simulation of the newly developed ESD structure concepts based on physical and empirical models [80], [51].

The TCAD software is able to gives insights into the device physics at time resolutions and locations that are not possible to measure in real silicon devices with currently available measurement equipment, e.g. the spatial resolution of carrier concentrations in the picoseconds (ps) interval. Here, the commercial finite element method (FEM) simulator software of *Synopsys* is utilized to model and simulate semiconductor structures. Even complex ESD protection structures based on SCRs are successfully designed by applying TCAD methodologies.

There are a several works covering the application of TCAD for ESD device design available. Salacedo et. al proposes a methodology to design a lateral SCR device with TCAD [81] and Bourgeat et al. presents a TCAD study of a trigger element design for lateral SCR devices [82]. Esmark investigated the simulation of ESD protection elements in his PhD thesis and was one of the first who covered 3D simulations for ESD devices based on GGNMOS (gate-grounded-MOS) protection structures operating in avalanche breakdown [51]. Also *S. G. Beebe* and *K. Esmark* reported the lack of calibrated temperature models which leads to overestimation of the lattice temperature in silicon during ESD simulations [83], [51].

This work applies TCAD to vertical SCR devices with a two dimensional current flow due to a lateral trigger element and investigates switching behavior and technology impact on vertical device performance.

Primarily, DC simulations were carried out because the static results are similar to the quasi-static results achieved by transient ESD simulations. The temperature model was deactivated (isothermal) because the joule heating in the complete device volume has to be neglected in DC to match the short pulse condition during ESD.

Additionally, the real silicon device reaches current densities of $1{\cdot}10^6\ \mathrm{Acm}^{-2}$ during ESD (e.g. 100 ns) and the lattice temperature is overestimated by the temperature model of the simulator. This is seen in transient simulations where the local lattice temperature reaches very high values while measurements of silicon devices do not show any significant heating effects.

Because ESD protection devices are operating at above mentioned current densities isothermal simulation results are less accurate by neglecting local thermal effects.

Nevertheless, the results are still useful for understanding device behavior. Therefore, thermal models were deactivated in the device simulations.

### 3.2.1 Simulation Models and Setup

Based on the PhD thesis [51] results of *K. Esmark* about simulation of ESD protection elements, especially in the pre-silicon phase, several important models for ESD simulations are identified:

- The carrier lifetime ($\mu_{n,p}$) and its temperature dependence.
- The impact ionization process with its coefficients ($\alpha_{n,p}$) and corresponding temperature dependence which usually takes place during ESD. Impact ionization models are well calibrated by their ionization coefficient from literature [84], [85]. Currently, the university of bologna model is calibrated up to 600 K [86].
- The *Shockley-Read-Hall* recombination via deep level traps ($\tau_{SRH}$[6]) is important and described by the *Scharfetter relation*, which is an empirical model and links the carrier lifetime to the background doping [87].
- The Auger recombination ($\tau_{Aug}$) which plays a role at high carrier densities ($> 1 \cdot 10^{19}\,\mathrm{cm}^{-3}$) and has to be activated in ESD simulations.

The drift-diffusion (DD) model was used instead of the hydrodynamic model for all device simulations because the first simulation results showed no difference while computation effort was significantly higher for hydrodynamic simulations. The DD model is assumed to be accurate for simulated structures because the dimensions of the carrier transit regions are several microns so that the hydrodynamic effects are negligible and DD is sufficient.

The models which were used for device simulations are shown in Table 3.3.

### 3.2.2 1D Simulation

One dimensional device simulations are used to evaluate the feasibility of a novel device concept in short iterations. Compared to circuit simulations the 1D device simulation has a qualitative description of the device structure with real doping

[6] originated from impurities or implantation damage

**Table 3.3:** Activated TCAD models for static and transient device simulations.

| Model | Description |
|---|---|
| EffectiveIntrinsicDensity (OldSlotboom) | important model for bipolar gain in static simulations |
| Mobility (DopingDependence) | modeling of doping dependence of the carrier mobility |
| Mobility (HighFieldSaturation (GradQuasiFermi)) | important for the transient overshoot results and the turn-on of the device |
| Mobility (CarrierCarrierScattering (ConwellWeisskopf)) | Important for the correction of carrier mobilities at high fields which occur during fast ESD events |
| Recombination (Auger) | modeling of doping dependence of the carrier mobility |
| Recombination (SRH (DopingDependence TempDependence)) | modeling of doping dependence and the temperature dependence of the carrier mobility |
| Recombination (Avalanche (UniBo2)) | impact ionization model calibrated up to 600 K [86], suitable for low voltage breakdown ($< 20$ V) |
| Recombination (Band2Band) | band-to-band tunneling model for very high doped pn-junctions |

profiles which are calibrated by secondary ion mass spectrometry SIMS profiles or created by calibrated process simulation. The 1D results help to understand the device behavior and point out important technology parameters (e.g. doping concentration and junction shape).

Nevertheless, a 1D simulation cannot accurately predict the device behavior due to the presence of two dimensional effects. In case of vertical structures with lateral device dimensions (e.g. anode perimeter) which are several times larger then the active device depth ($d_{anode} >> w_{device}$), a 1D simulation delivers sufficiently accurate results. Junction breakdown voltages or conduction current densities during on-state are typical examples for 1D simulation results.

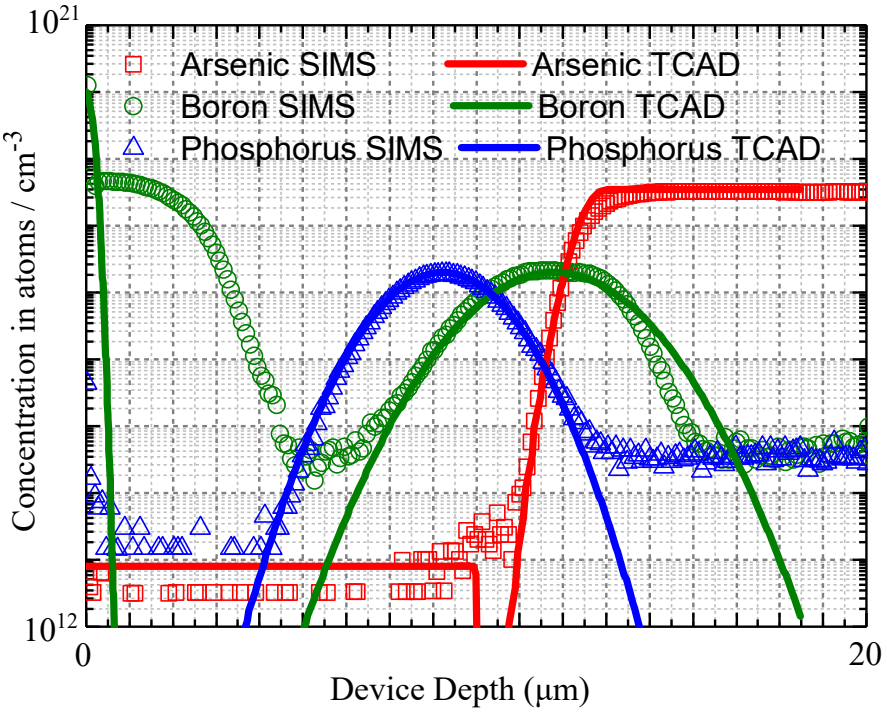



**Figure 3.20:** A comparison of the TCAD generated doping profile and the extracted SIMS profile from first silicon samples is shown. The TCAD generated profile shows sufficient matching with the SIMS data which increases the quality of the electrical simulation data.

### 3.2.3 2D Simulation

Two dimensional device simulations are required to capture advanced device behavior like spatial switching of the device during ESD or the formation of hot spots due to current crowding effects [51].

The investigated vertical structures in this work are conducting the main ESD current almost homogeneous, yet due to the lateral trigger element and a lateral shunt resistor a 2D current flow is still present. To investigate the full operation range of the device and accurately optimize the device switching 2D device simulations were

carried out. Due to significant increase in computation time the 2D simulations are only carried out for well chosen insertions.

### 3.2.4 Pseudo 3D Simulation

The three dimensional device simulations are able to achieve the most accurate results. Even the simulation of filamentation in ESD devices due to non-uniformal triggering is possible [51]. In [88] a guideline is given for 3D TCAD simulations which produce the most accurate results compared to pseudo 3D. Nevertheless, a full 3D simulation is time consuming and only applicable for single simulation points. Instead, a pseudo 3D simulation is a compromise to achieve more accurate results while saving simulation time. A 2D structure is simulated and the results are transformed into the corresponding 3D results for example by rotation of the 2D structure. This method is only applicable to cylindrical structures and used to simulate the vertical devices investigated in this work. The limitation of reducing the vertical breakdown can be resolved by the lateral breakdown of the trigger structure which is forming a lateral highly doped pn-junction. Because the junction is formed by a well implantation followed by a shallow contact implantation a steep junction profile is formed which can achieve junction breakdown voltages below 10 V or even in the zener region ($< 5$ V).

### 3.2.5 Turn-on Optimization

The decrease in turn-on time of the protection device helps to improve the protection performance and reduces the temporary over-voltage which is seen by the circuit to be protected.

The turn-on time of SCRs decreases for the following two measures:

- continuous decrease of the anode to cathode distance - $d_{AC}$
- increase of carrier velocity between anode and cathode - $v_c$

The decrease of $d_{AC}$ is one option to decrease turn-on time because carriers have to travel shorter distances. The limits of reducing $d_{AC}$ are set by the technology or by physical limits of silicon device parameters (e.g. breakdown voltage, leakage current or junction capacitance). To achieve very low junction capacitance or high reverse voltage a large depletion region is required which is contrary to short $d_{AC}$.

A second measure is to increase $v_c$ in a pnpn-structure which is composed of drift- and diffusion velocity (Section 2.3.3). As the diffusion process is slower compared to the drift of carriers $v_c$ is dominated by the diffusion velocity in the neutral regions [47]. The doping concentration in the neutral regions has influence on the carrier mobility in silicon and will modify the diffusion through this regions. To increase $v_c$ the doping has to be lowered and the width of the neutral regions have to be decreased with same restrictions like $d_{AC}$. The second effect of the lower doping in the neutral region is the increase of the depletion region which follows $\propto \sqrt{V/N_B}$ and substitutes the neutral region by a space-charge region with drift dominated carrier transport.

During system level ESD events, which have a typical risetime of less than 1ns, a large part of the neutral region is expected to be depleted and $v_c$ is dominated by drift velocity. With increasing ESD voltages $v_c$ is approximated by $v_{sat}$ and reduces the turn-on time to Equation 3.8. The widths of the neutral regions are $d_{n1}$ (n-doping) and $d_{n2}$ (p-doping). Saturation velocity values for electrons and holes in silicon are $v_{sat,n}$ and $v_{sat,p}$, respectively.

$$t_{on} = \sqrt{\frac{d_{n1}}{v_{sat,p}} + \frac{d_{n2}}{v_{sat,n}}} \tag{3.8}$$

A comparison of measured transient device voltages with transient device simulations at 2 A and 4 A TLP stress with a 600 ps risetime in Figure 3.21 confirms the increasing switching speed of the pnpn-structure. The depletion of the neutral n-base region increases for higher TLP stress and confirms the predicted improvement due to $v_c$ optimization. The deviation from the measured data is justified by two facts. First, the 2D structure is carefully modeled by analytical doping profiles and original layout geometry but a few details cannot be accurately modeled due to missing information like exact two dimensional doping profiles. Second, the stress pulse, which is seen by the device, is very important and can only be guessed in the simulations. The simulation results in Figure 3.21 are obtained by forcing a voltage pulse waveform into a 50 Ω resistor (lumped element). This voltage pulse waveform was captured by TLP measurements on a 50 Ω calibration resistor which might not represent the true condition of the voltage which is seen by the protection device at the moment due to a different impedance.

Another optimization for the turn-on of the protection device is the lowering of the first voltage peak which occurs during the transient switching. As the overall

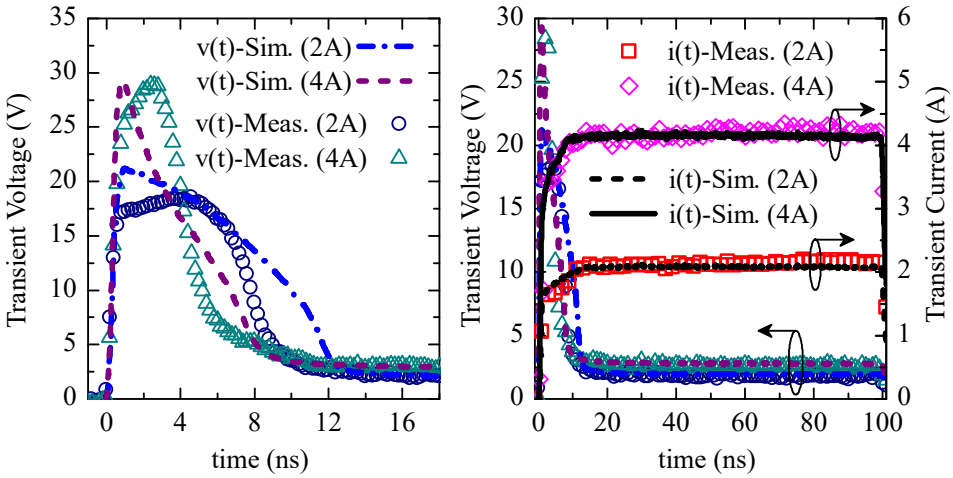



**Figure 3.21:** Comparison of simulated and measured transient voltages of a SCR protection device. The device is stressed with a 2 A and 4 A 100 ns-TLP pulse with a 600 ps risetime. Simulated transient voltage values completely matches after turn-on of the device whereas the switching phase (0 ns to 12 ns) differs.

switching is determined by the dimensions of the vertical pnpn-structure a lateral trigger element was included to control the breakdown independently of the buried layer properties. This lateral trigger is another integrated bipolar transistor with its own base length and transit time. By variation of the lateral distance of the trigger, the base width and transit time of diffusing carries were varied. In Figure 3.22 a decrease in the peak voltage of the protection device is shown for decreasing base width of the lateral trigger. The response of the lateral trigger was optimized to reduce the first voltage overshoot in the ESD protection device. With the widest base of 10 µm the lateral trigger is so slow, that the vertical structure can built up a significant reverse voltage during the voltage overshoot. This high voltage during the first nanoseconds is dangerous for devices that are protected by such ESD device but the turn-on time of the protection device itself is decrease due to a strong field effect in the depleted base regions of the vertical device. This effect can be used to improve turn-on speed in vertical devices with lateral trigger by allowing higher peak voltages. For lowest peak voltage a reduced base width for the lateral trigger element is desired. An optimized vertical protection structure with lateral trigger has

to target thin vertical base regions to reduce transit times and respective turn-on for the ESD protection device together with a lateral trigger with minimized base widths for lowest voltage overshoots.

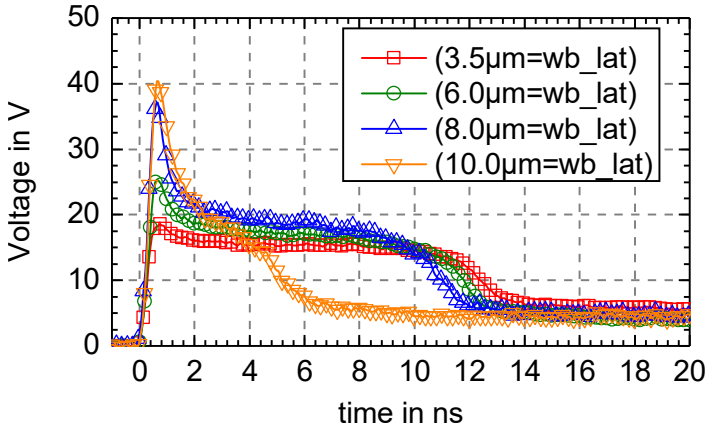



**Figure 3.22:** Measured voltage transients of vertical pnpn ESD protection structures at 4 A TLP current are shown. A lateral trigger structure (pnp) with different base widths shows the influence on turn-on behavior. For shorter pnp base widths a decrease in the peak voltage during device response is visible.

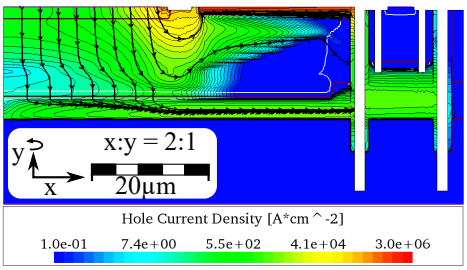
### 3.2.6 2D Device Simulations of the Triggering Process

The turn-on process in the lateral triggered vertical protection device is illustrated by the current density distribution at different times and shown in Figure 3.23. The triggering of the whole structure starts with the junction breakdown of the trigger element (lateral pnp-transistor) and a corresponding lateral current (see Figure 3.23(b)). Holes are injected by the forward biased p-emitter (anode) and diffuse omnidirectional. The vertical diffused holes, which arrive in the p-buried base (collector), are now majority carriers. They drift to the pn-junction short which is at ground potential (see Figure 3.23(a)) and increase the p-base potential continuously

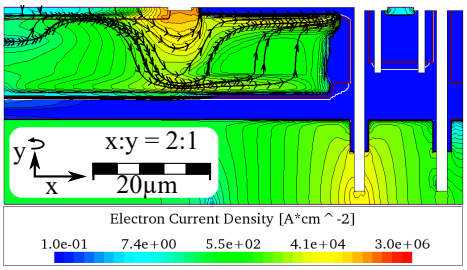
until the n-emitter starts to inject electrons (see Figure 3.23(d)). The electron- and hole current density relocates and shows a vertical dominated current flow during the switching process of the vertical structure. At 100 ns the device is already in the quasi-static regime and a homogeneous current flow is established for the electron current density, which is larger than the hole current density (see Figure 3.23(f)).

### 3.2.7 Current Density Distribution of the Vertical Protection Device with Lateral Trigger

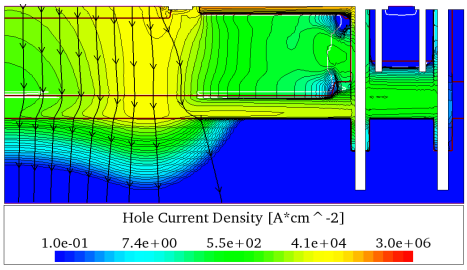
The current density distribution of a vertical pnpn-structure with lateral pnp-Trigger is shown in Figure 3.24 for different time steps. The first ESD current is conducted by the lateral trigger element and afterwards redistributed to the vertical ESD protection device. The captured current density at t = 10 ns shows a full conduction of the vertical ESD device. At t = 100 ns, the current density at the anode is lowered due to better distribution in the active region (x = 0 µm to 30 µm). A small hot-spot is located at the anode corner which has to conduct the lateral trigger current of the pnp as well .



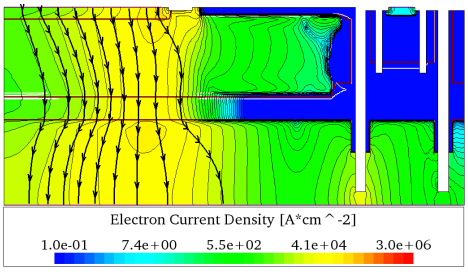

(a) hole current, t = 1 ns



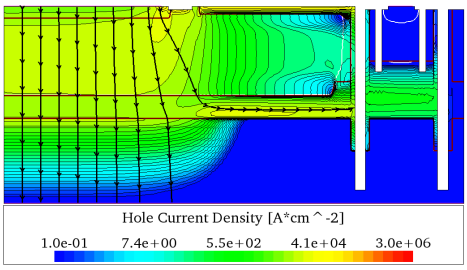

(b) electron current, t = 1 ns



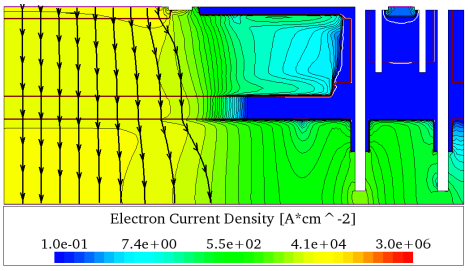

(c) hole current, t = 10 ns




(d) electron current, t = 10 ns




(e) hole current, t = 100 ns




(f) electron current, t = 100 ns

**Figure 3.23:** Simulated current densities for electron and holes in a protection device during turn-on phase. A 2 A rectangular pulse with a 600 ps risetime is applied to the anode terminal. In (a) the device at 1ns and is shown and (b) captures the switching process at 10ns. In (c) the current density is homogeneously distributed in the vertical pnpn-structure.

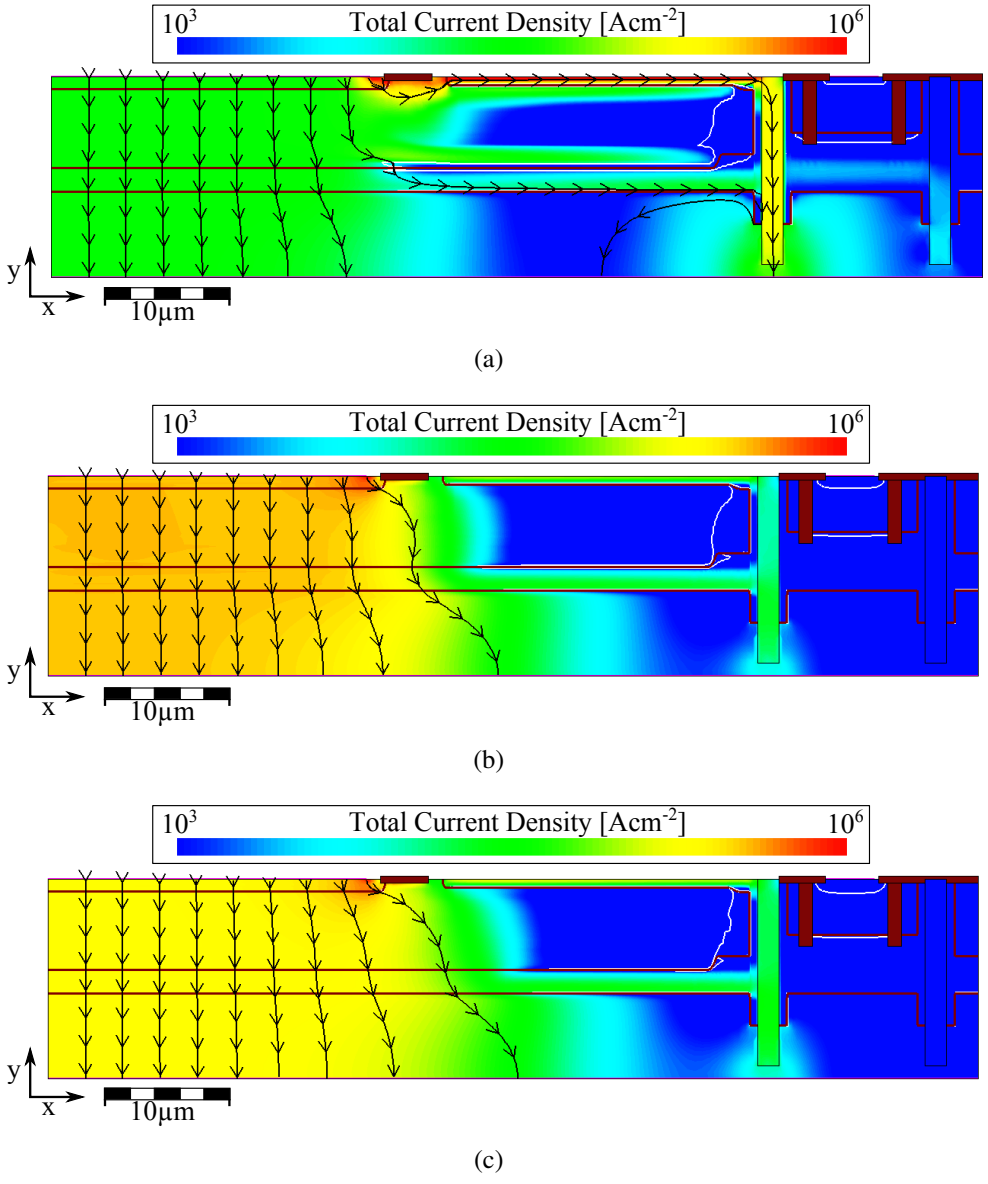



**Figure 3.24:** Simulated 2D current density map during turn-on phase. An 8 A rectangular current pulse with 600 ps risetime is forced into the anode contact. (a) shows the device at 300 ps and (b) captures the switched ESD structure at 10 ns. At 100 ns (c) the device is in the quasi-static regime with well distributed current density in the anode region.

## 3.3 Technology

### 3.3.1 Process Technology

The protection structures presented in this work are fabricated in a vertical submicron bipolar technology comparable to well known power device structures from [89] and [48].

In the following, a few specific features are introduced.

A low ohmic substrate (highly doped) is required because of two reasons:

1. to minimize the parasitic resistance of the vertical device
2. increase the emitter efficiency to support a high bipolar gain (see Chapter 4)

A simplified process flow is illustrated in Figure 3.25. The doping concentration of epitaxial grown layer and implantation doses are given by $N_{Ax,Dx}$, implantation masks are indicated by $M_x$. The dashed lines show the implantation peak of the dopands.

Excluding the pn-short, all single process steps are state-of-the-art silicon processing methods that are described in literature [41], [90], [47]. A more detailed formation of the device structure and additional embodiments are described in *US Patent App. 14/817,928* [74].

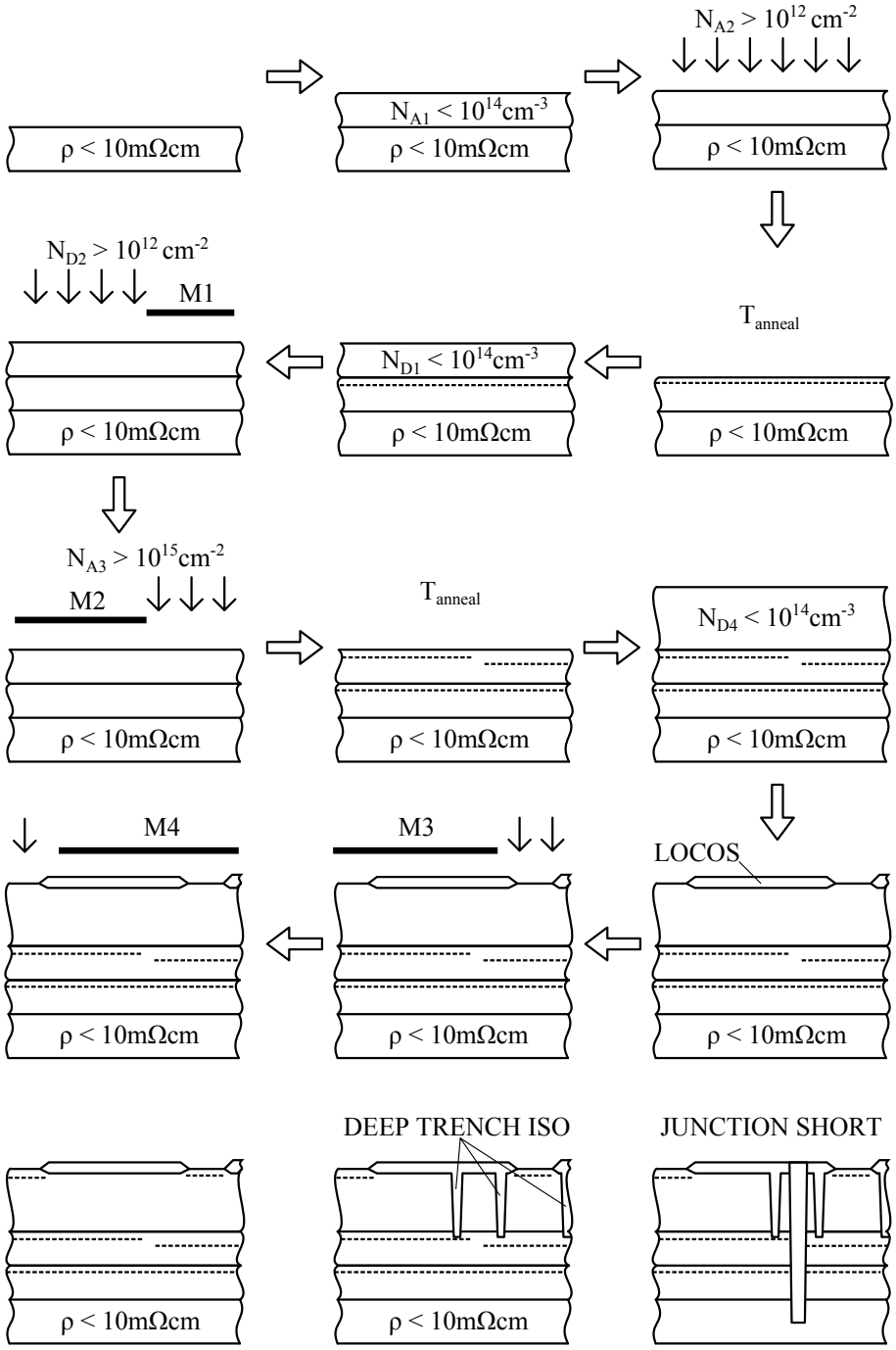



**Figure 3.25:** Simplified process flow of a vertical unidirectional reverse conducting breakover diode structure according to *US Patent App. 14/817,928* [74]. Doping concentrations are given by $N_{Ax,Dx}$ and implantation masks by $M_x$. The two parallel structures are electrically isolated by deep trenches.

### 3.3.2 Device Isolation Concepts

Two state-of-the-art isolation concepts are widely used to isolate active silicon structures according to [90] and [47]:

1. **junction isolation concept** - a pn-junction is created and connected in reverse direction to the active areas (a small leakage current is still present which corresponds to the generation current in the depletion region).
2. **trench isolation concept** - the active area of two devices is separated by an isolation material (e.g. $SiO_2$) which is deposited or formed at the sidewalls of a trench structure etched in the silicon material.

Examples of the described isolation concepts are shown in Figure 3.26 and Figure 3.27. The structure shown in Figure 3.27 uses a junction isolation which is cheaper and a less complex solution compared to the trench isolated in Figure 3.26, but requires shallow device because the diffusion range of the junction isolation is limited by the thermal budget of the used technology. Typical sinker depths are in the range of 5 µm to 10 µm [90] and require a high temperature diffusion process that has to be aligned with the junction profile of the active devices.

The advantage of a trench isolation concept is the effective isolation of the active area without significantly increasing the junction area and the corresponding junction capacitance. Additionally, the design rules (critical layout widths and distances) for a trench isolation are less strict and the lateral distance to junctions are less critical. For example, a punch-through occurs with a junction isolation in low doped silicon regions already at short lateral distances to other junctions which results in undesired leakage or low breakdown voltages [47].

The disadvantage of a trench isolation is the process variation of the trench depth which is related to process technology. The etch depth depends on several parameters like the aspect ration, open area and etch time functions which can result in hundreds of nanometers in depth deviation. This directly influences device parameters in submicron devices. An example for such a variation is the trigger current in a vertical pnpn-structure using trench isolation. It can vary in the double digit percent range and is discussed in Section 3.1.5.

A trench isolation is recommended for devices that are targeting lowest capacitance values and smallest chip areas. The protection structures in this work utilize a combination of trench isolation and junction isolation to have the advantage of both. In detail, the vertical low voltage pnpn-structure uses a junction isolation to avoid

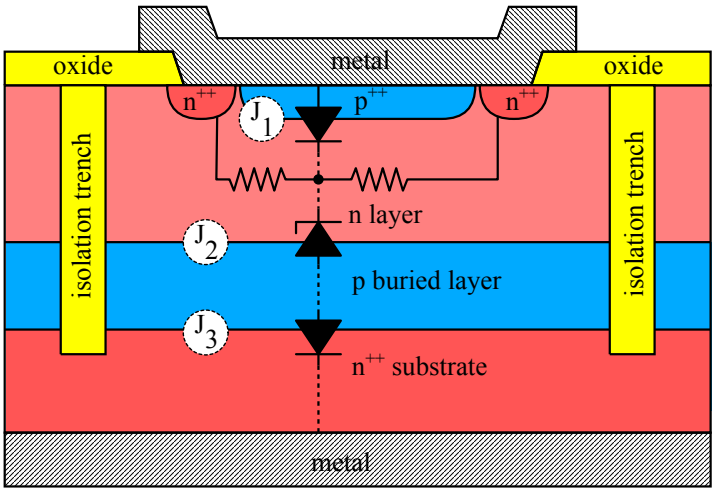



**Figure 3.26:** A schematic cross-section of a vertical pnpn-structure isolated by a deep trench. The three junctions $J_1$, $J_2$, $J_3$ are defining the vertical pnpn-structure. High doped n-regions at the surface are forming emitter shorts [48].

influence of the trench depth variation while the parallel bypass diode uses a trench isolation to reduce the junction area and capacitance.

### 3.3.3 pn-Junction-Short Concept

The key feature of the introduced ESD protection device structure is the unique pn-junction short concept realized by a vertical trench structure filled with metal. It was already illustrated in Figure 3.4 of Section 3.1.2. This trench structure is filled by a plurality of metal layers that act as barrier material to ensure a low ohmic connection to the silicon interface [90], [41]. A more detailed description of the formation is found in [74].

The pn-short structure is introduced for the first time in this work because it is required to electrically short a blocking pn-junction in the vertical device concept. Conventional concepts use sinker structures to route an electrical connection to the

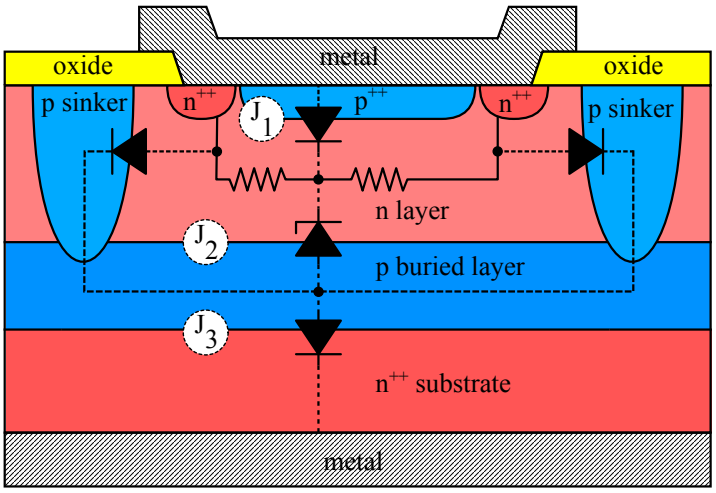



**Figure 3.27:** A schematic cross-section of a vertical pnpn-structure isolated by junction isolation. The three junctions $J_1$, $J_2$, $J_3$ are defining the vertical pnpn-structure.

surface which has to be connected to the backside via metal stacks or etching mesa structures like schematically shown in Figure 3.28.

The pn-junction short has two important functions in the proposed vertical pnpn-structure:

1. **Emitter short**: The cathode is connected to the buried p-base of the vertical pnpn-structure to shunt the base-current (holes) and prevent the pnpn-structure from triggering at low currents. The n-base is required to have a floating potential (see Section 3.1.3 and Chapter 2.4).
2. **Substrate junction ($J_3$) short**: The substrate junction $J_3$ must be electrically shorted to enable a reverse conducting diode in parallel which is embedded in the same substrate.

It is important that a low ohmic contact at the metal to silicon interface is formed across the trench sidewall to successfully implement the pn-junction short. Figure 3.29 shows the electrical results of diode structures with the integrated pn-

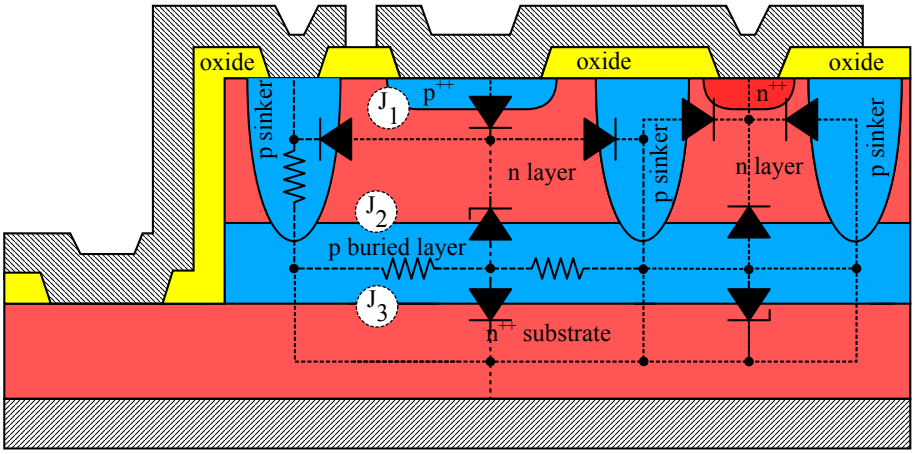



**Figure 3.28:** A schematic cross-section of a reverse conducting vertical pnpn-structure with a conventional metal mesa structure to connect the p-buried layer to substrate potential.

junction short. The two IV characteristics show a typical diode IV-characteristic and a diode with a significant series resistance. The higher series resistance is attributed to a non-ohmic contact and a formation of a Schottky barrier ($\phi_{Bp,n}$) in the pn-junction short structure. The Schottky barrier is formed at the semiconductor to metal interface and is determined by the difference in the electron affinity ($\chi$) in the semiconductor and the work function of the metal ($\phi_m$) by ignoring surface charges at the interface [41], [47]. The pn-short has contact to n-type and p-type semiconductor and uses a titanium-nitride liner as barrier material but without forming $TiSi_2$ as the annealing temperature is too low. According to [41], a barrier height of 0.60 eV to n-type is assumed for Titanium. With Equation 3.11 the p-type barrier is calculated to 0.51 eV.

$$e\phi_{Bp} = E_g - e(\phi_m - \chi), \tag{3.9}$$

$$e\phi_{Bn} = e(\phi_m - \chi), \tag{3.10}$$

$$e(\phi_{Bp} + \phi_{Bn}) = E_g \tag{3.11}$$

Several approaches to achieve ohmic contacts are found in literature and known from state-of-the-art silicon process technology [91], [47], [41]. One option is to choose a proper metal with $\Phi_m > \Phi_s$ to form a low ohmic contact to a p-semiconductor [92]. This introduces constrains to the interface which can be avoided by the common method of increasing the doping concentration at the silicon to metal interface. This decreases the depletion width ($x_d$) and the respective barrier thickness which increases the tunneling probability for carriers. The required doping concentration can be estimated by Equation 3.12 [93]. $\Phi_i$ is the built-in potential and $x_d$ is the depletion width.

$$N_A > \frac{2\varepsilon_0 \cdot \varepsilon_{si}\Phi_i}{qx_d^2} \tag{3.12}$$

The challenge of the novel structure is to form an ohmic contact deep in the semiconductor bulk region because the implanted buried layers diffuse during temperature process steps and cannot support the required doping concentration for low ohmic contacts. Figure 3.30 shows the schematic cross-sections of two different vertical diode concepts. The corresponding electrical results are shown in Figure 3.29. Comparing the latter two structures and the corresponding measurement data in Figure 3.30(a) one can conclude an ohmic contact is partially achieved at the top of the silicon surface with the additional $p^{++}$ implantation which is high enough to increase the tunneling current. An ohmic contact of the pn-junction short to the substrate (metal-bulk interface) is assumed due to the high doped silicon substrate material (2.5 m$\Omega$cm which corresponds to concentrations $>4 \cdot 10^{19}\,\mathrm{cm}^{-3}$). It has to be mentioned that the Schottky barrier is 0.09 eV higher compared to the p-type region.

In Figure 3.30(b) a diode structure with a trench isolation is shown as the most favorable diode concept to minimize junction capacitance. The electrical connection is only possible through the buried p-layer. The p-layer is doped by an ion implantation process with a boron dose of $5 \cdot 10^{15}\,\mathrm{cm}^{-2}$.

From the electrical results it is evident that the doping concentration of the buried p-layer is not sufficient to achieve a low ohmic contact. Secondary Ion Mass Spectroscopy (SIMS) analysis of the diode structure, which is illustrated in Figure 3.31, shows that the peak concentration of the buried layer is less than $1 \cdot 10^{19}\,\mathrm{cm}^{-3}$ while the peak concentration of the $p^{++}$ sinker implant is about $4 \cdot 10^{19}\,\mathrm{cm}^{-2}$.

The required boron concentration to form an ohmic contact with low contact resistance to the junction short has to be $> 1 \cdot 10^{19}\,\mathrm{cm}^{-3}$ according to the SIMS results. This matches the values found in literature [47] and the estimation of Equation 3.12. A further increase in the doping leads to an exponentially decrease of the contact resistance according to [47].

The characterization of such low contact resistances is described in [94] and is not the focus of this work because the following improved trench diode structure (compare Figure 3.34) shows a sufficiently low electrical resistivity of $\rho = 120\,\mu\Omega\,\mathrm{m}$ (calculated with $\mathrm{A} = 2000\,\mu\mathrm{m}^2, \mathrm{l} = 10\,\mu\mathrm{m}, \mathrm{R} = 0.59\,\Omega$) and confirms an ohmic contact.

### 3.3.4 Optimization of the pn-Junction-Short

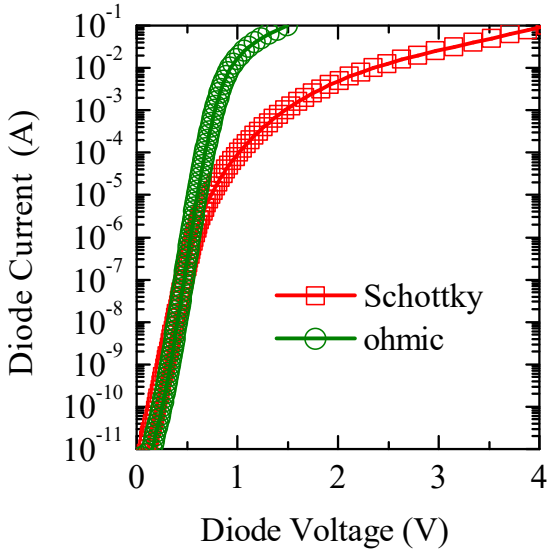
It was shown that the pn-junction short works only with a junction isolation concept because the buried layer peak doping concentration is insufficient for a low ohmic contact. The drawback of the sinker concept is a reduced area efficiency of the diode structure because the lateral current path is restricted to the surface. This is shown in Figure 3.32 and indicated by the dashed line. Additionally, the pn-junction area is increased compared to a trench isolated design (compare Figure 3.30(b)). Due to the lateral current the diode is declared as a lateral structure.

An improved concept of the pn-junction short is proposed in the following. A low ohmic contact to the buried p-layer was formed by a high doped boron layer at the pn-junction short sidewalls. It is realized by a shallow diffusion of boron atoms into the silicon region by a deposited dopand source on the sidewalls of the trench structure.

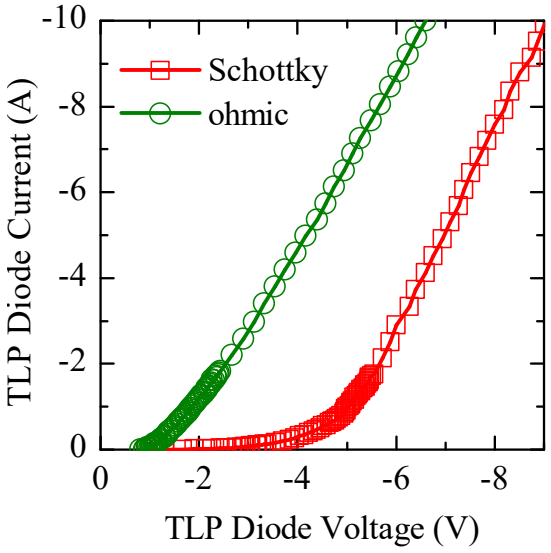
As previously verified a concentration greater than $1 \cdot 10^{19}\,\mathrm{cm}^{-3}$ is necessary to significantly reduce the contact resistance. The structure with a shallow and high doped boron layer at the sidewalls of the pn-junction shorts is shown in Figure 3.33(a). A uniform $\mathrm{p}^{++}$ doping along a defined depth is formed. The corresponding SIMS analysis of the boron concentration of the sidewall doping process is shown Figure 3.33(b).

Figure 3.34 shows high current IV curves of a trench isolation pn-diode structure with the original pn-junction short concept compared to the optimized new concept. The diode structure conducts the current through the buried layer due to the improved

pn-junction short. The combination with trench isolation can decrease the junction area of the diode which leads to lower device capacitance.

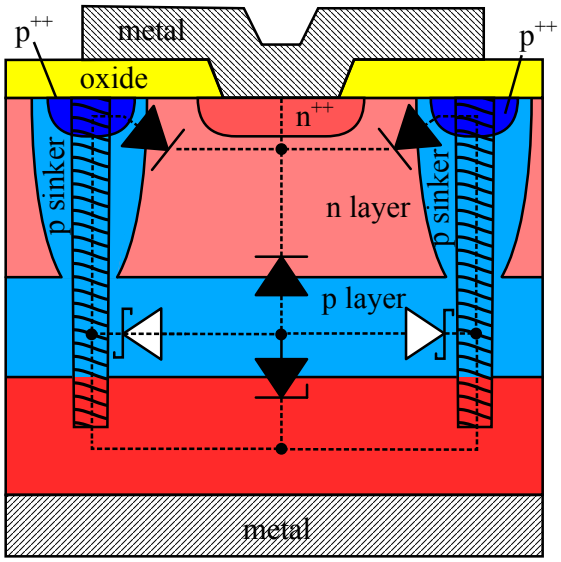



(a)

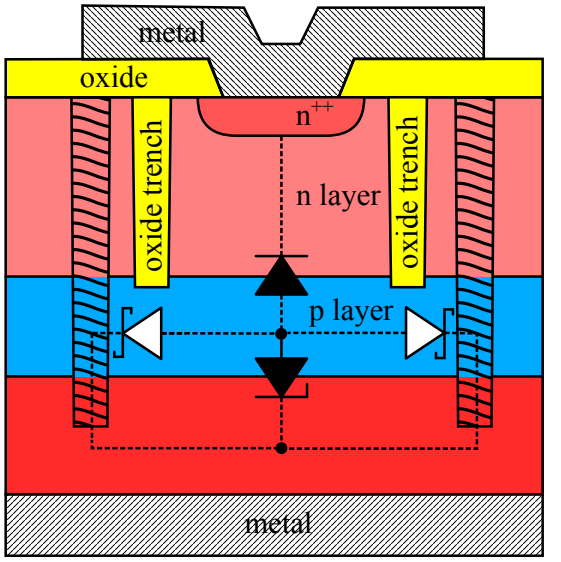



(b)

**Figure 3.29:** A measured DC characteristic (a) and high-current characteristic (b) of a diode structure with pn-junction short is shown. A Schottky contact in one diode structure is indicated by a high series resistance. In (b) a junction breakdown of the reverse biased substrate junction can be observed which confirms non-ohmic pn-junction short.




(a)




(b)

**Figure 3.30:** Two schematics of different vertical diode structures are shown. A diode structure with sinker and additional $p^{++}$ implants at the pn-junction short is shown in (a). A diode structure with only pn-junction shorts and deep trench isolation is shown in (b). The diode (a) has an ohmic contact at the surface $p^{++}$ implant while diode (b) does not (see Figure 3.29).

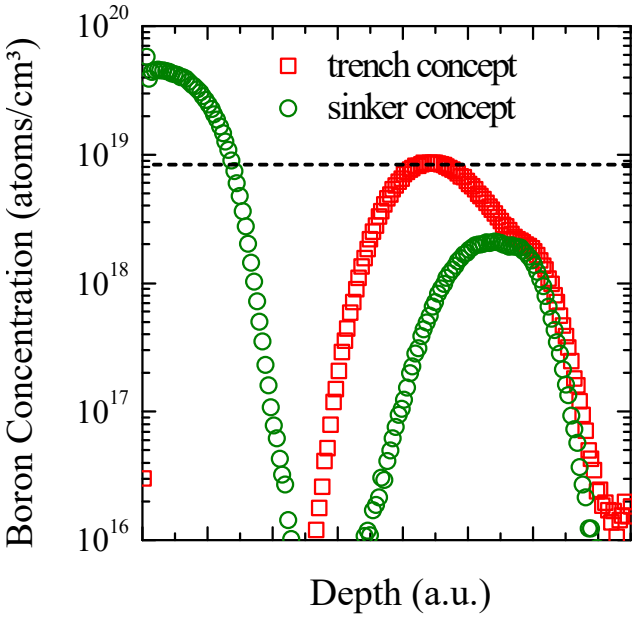



**Figure 3.31:** Boron doping profile of two vertical diode concepts are shown. Secondary Ion Mass Spectroscopy (SIMS) analysis of the ESD diode structure reveals the insufficient boron peak concentration of the buried p-layer. The surface concentration is much higher with the same dose implanted.

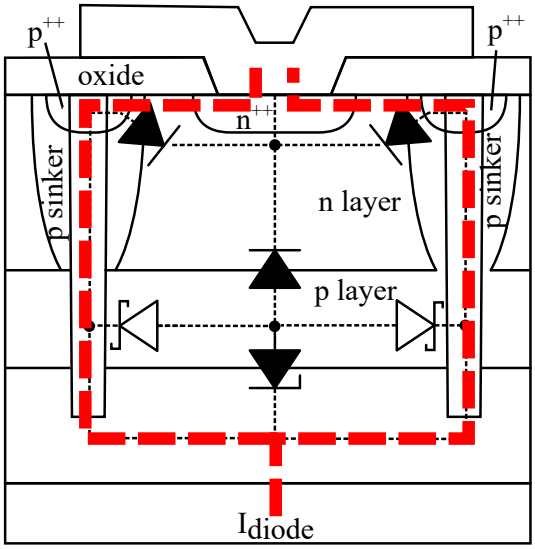
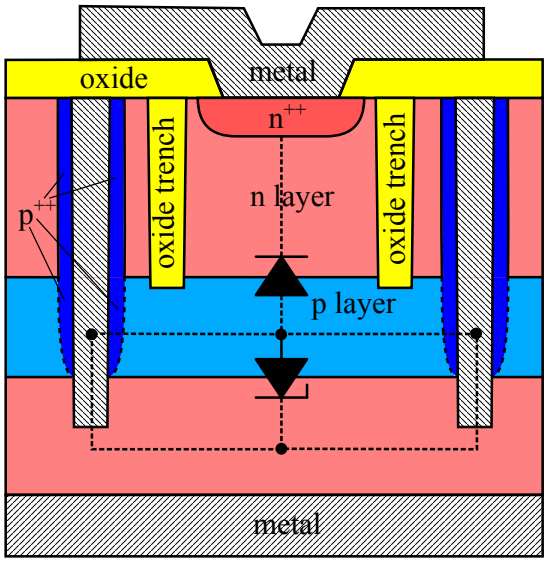
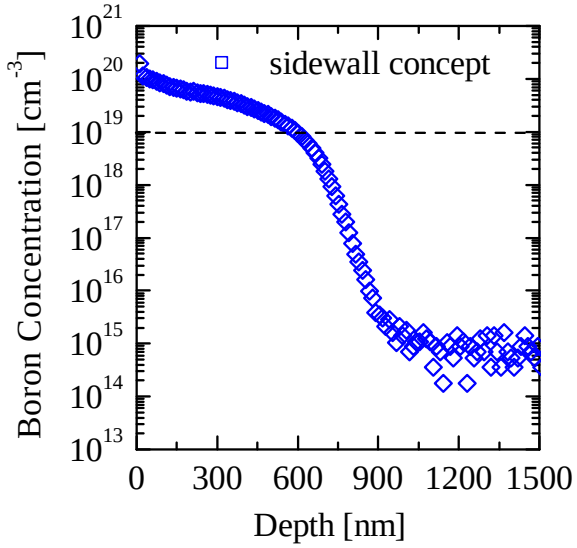



**Figure 3.32:** A schematic cross-section of a vertical diode with a sinker and pn-junction short structures. The main current path (dashed line) through the diode is shown. Due to the lateral current path this design has a low area efficiency because most of the diode area is unused.




(a)




(b)

**Figure 3.33:** A schematic cross-section of a vertical diode concept with trench isolation and sidewall doped pn-junction short is shown in (a) and the corresponding SIMS data of the boron concentration at the sidewall is shown in (b).

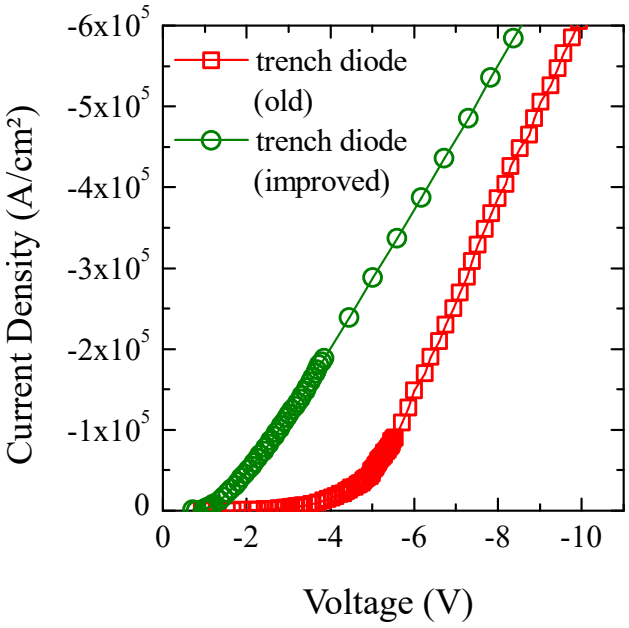



**Figure 3.34:** High current TLP IV characteristics of vertical trench diode structures with a pn-junction short are shown. The effective diode area is 1963 µm$^2$ and the applied pulse length was 100 ns. The 'old' trench diode shows a breakdown at 5 V while the improved diode conducts after the threshold voltage is reached. The improved 'new' diode has a better ESD performance due to the lower forward voltage throughout the shown current density.

### 3.3.5 Junction Breakdown Voltage

The internal breakover voltage of the vertical structure is adjusted by the doping profile of $J_2$. The junction profile is shaped by two Gaussian distributions of the buried layer implantations and has to be engineered to support the required breakdown voltage. Figure 3.35 shows the comparison of the simulation results with experimental data.

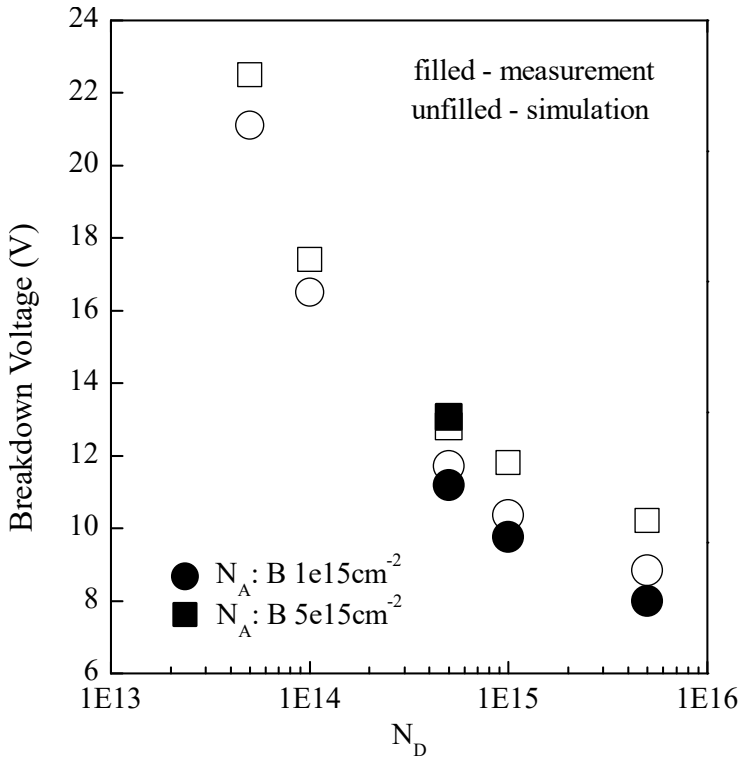



**Figure 3.35:** Comparison of measured and simulated breakdown voltages of junction $J_2$. Simulations were performed on 1D structures generated by process simulation. Filled symbols are representing experimental data, circle and square symbols are representing $N_A$ groups. The simulated breakdown voltages are matching well with the experimental results.

The breakdown voltage is a function of two implantation doses $N_A$ and $N_D$. The main function of $N_D$ is to adjust the breakdown voltage. In case of leaving out the n-buried layer the breakdown is determined by the doping of the top epitaxial layer. Contrary, $N_A$ has two function as it additionally controls the trigger current of the vertical device and is restricted in the doping range (see Section 3.1.4). Therefore, the range of the $N_A$ dose is set between $1\,cm^{-2}$ to $5\,cm^{-2}$ and the $N_D$ dose is varied to tune the breakover voltage of the device.

The target value for a low voltage breakdown is around 6 V which is an ideal avalanche breakdown. The measured breakdown voltage values cover the range of 8 V to 22 V which successful demonstrates the application for a low voltage ESD protection concept. A further decrease of the breakdown voltage is not possible due to the limit of the *Zener effect* (Section 2.3.1) and a corresponding increase of the device leakage current shown in Figure 3.36. Additionally, it was observed that the device operation of the SCRs with breakdown voltages less than 10 V start to change due to the very high base doping. This was found to be related to the device dimensions as well as to device physics of SCRs itself [95]. The ability to operate SCRs in a non-latched mode is briefly discussed in Chapter 4.

The maximum value for the breakdown voltage of the investigated structure is limited by the following four parameters:

1. $N_D$ **doping concentration**.
2. **n-layer thickness**: For low doped n-layer a vertical punch-through occur in the pnpn-structure.
3. **lateral distance between p-anode and junction isolation**: A lateral punch-through occur for small distances and lowly doped n-layer.
4. **n-layer doping** (silicon limit [48]): the silicon limit is reached for lowest possible n-layer doping if the maximum electrical field for silicon is reached (see Section 2.3.1).

In theory, the voltage class is only limited by the material limited electrical field and the current gain effect in SCRs (see Chapter 4).

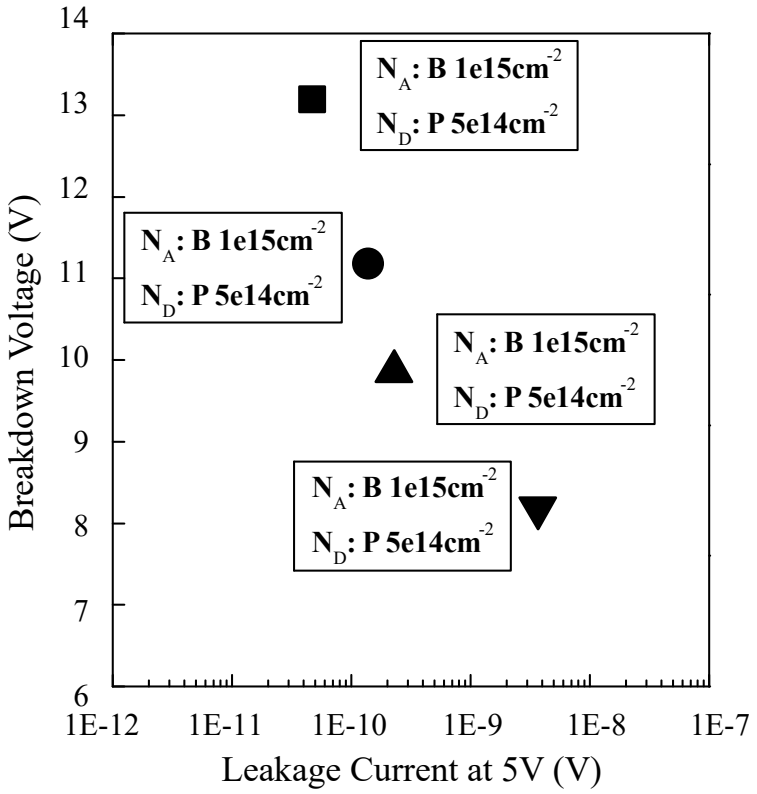



**Figure 3.36:** Measured breakdown voltage of junction $J_2$ versus typical junction leakage current at 5 V. The leakage current increases as the breakdown voltage approaches the working voltage. Avalanche multiplication starts before the breakdown voltage is reached.

## 3.4 Characterization

In this section give an overview of the electrical characterization techniques and methods for discrete ESD devices. The results shown in this work were generated by this techniques. An illustration of the development flow is shown in Figure 3.1.

ESD protection structures as well as special designed test structures are characterized by direct current (DC), alternating current (AC) and high-current measurements techniques. DC and AC measurements are state-of-the-art techniques, while the high current characterization is carried out by the transmission-line-pulse technique which is widely used for ESD device characterization [19], [21] and widely used within the industry [96].

A HP4156A semiconductor parameter analyzer was used to capture the IV-curves of the two terminal ESD protection devices. It supplies up to four source-measure-units (SMU) which are required to set up two- and 4-point measurements.

A two point measurement setup is used for low current ranges up to 10 µA because the parasitic voltage drop in the probes and cables can be neglected. Here, the two point setup is used to extract leakage currents in the off-state.

A 4-point measurement setup is recommended when exceeding the current range of 10 µA at which the ohmic voltage drop across the cables and probes has to be taken into account. The setup is realized by using two SMUs as force contacts and two other SMUs as sense contacts. The sensing SMUs are set to force a zero current while measuring the voltage (emulates a high ohmic input) of the device-under-test (DUT). This enables an accurate voltage measurement without a current in the sensing lines and therefore no parasitic voltage drop. Figure 3.37 shows the schematic of the 4-point measurement setup that was used to characterize ESD protection devices up to 500 mA. This technique also enables the measurement of DUTs with a negative differential resistance (NDR) characteristic which occurs in floating base transistor structures.

### 3.4.1 DC Characterization of ESD Protection Devices

The DC characterization of ESD protection devices has three purposes:

1. extract the leakage current of the ESD protection device in the operation region of the circuit to be protected

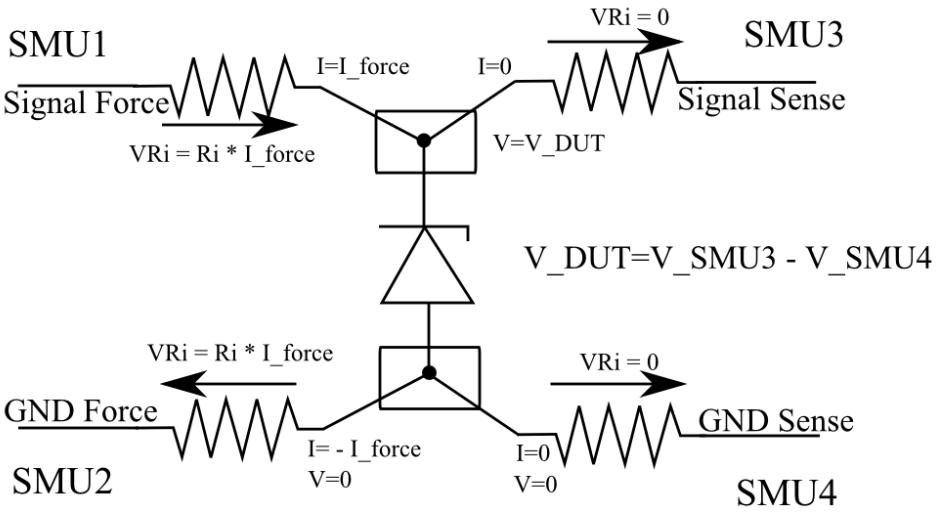



**Figure 3.37:** Schematic of a four-terminal measurement principle. The shown setup was used for characterization of ESD protection devices with a HP4156A semiconductor parameter analyzer. SMU1 is forcing current while SMU2 is the current sink. SMU3 and SMU4 forcing a current of 0 A and preventing any parasitic voltage drop across $V_{Ri}$. The device voltage ($V_{DUT}$) is measured as the difference between SMU3 and SMU4.

2. extract the breakdown voltage ($V_{BO}$) and trigger voltage ($V_{t1}$) of the ESD protection device
3. evaluate latch-up risk of snapback devices by extracting the holding voltage ($V_h$)

### 3.4.2 Negative Differential Resistance in Bipolar Structures

State-of-the-art ESD protection devices utilize the snapback of bipolar structures to reduce the ESD clamping voltage. A decreasing terminal voltage with increasing terminal current is defined as NDR region. To capture the snapback characteristic during DC measurements, a current forced setup (see Figure 3.37) is required because the negative $\delta V / \delta I$ cannot be captured by a forced voltage. This can be explained by Figure 3.38. The voltage forced measurement cannot resolve NDR region because the terminal voltage is continuously increased until the current jumps from $I_n$ to $I_{n+1}$. A current forced curve allows the DUT to reduce the terminal voltage and capture

data in the NDR region. The negative differential resistance is a well known behavior

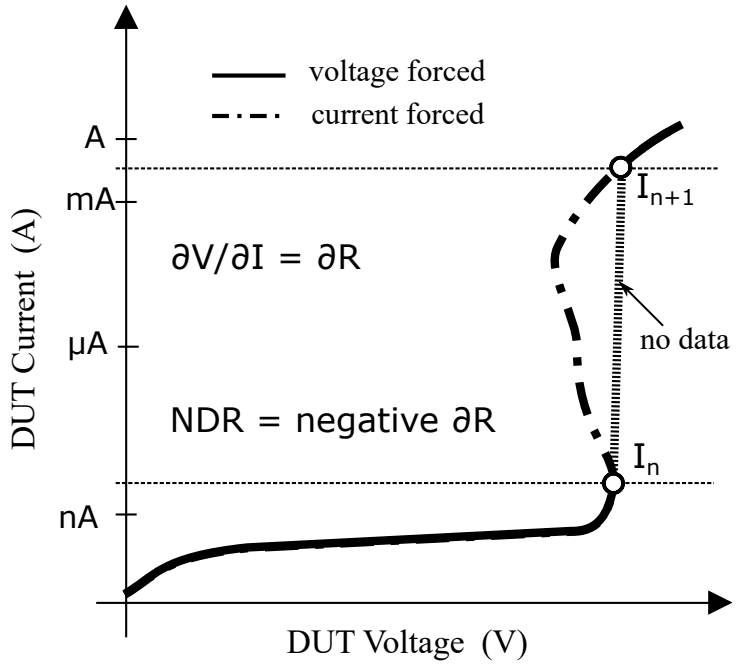



**Figure 3.38:** Schematic current-voltage characteristics of a snapback-device with negative differential resistance. The DUT current uses a logarithmic scale. The voltage forced curve does not show the negative differential resistance region (snapback). There is no data between $I_n$ to $I_{n+1}$. The current force curve can capture the negative differential resistance between $I_n$ to $I_{n+1}$.

in bipolar transistor structures due to their current gain. The current gain leads to a reduced collector-emitter voltage less than the collector-base breakdown voltage ($V_{CE0} < V_{CB0}$). In low capacitance ESD devices based on bipolar structures [62] a low doped base region leads to significant current gain values and a NDR region. It is important to characterize the S-shaped IV-characteristic to evaluate latch-up risks in snapback devices as the NDR region occurs at low currents ($1 \cdot 10^{-7}$ A to $1 \cdot 10^{-3}$ A). Low currents are here compared to the high current region of several ampere during ESD events. A typical NDR region of a low capacitance pnp-transistor structures with a low doped floating base region is shown in Figure 3.39. The snapback or NDR

region is more pronounced for increasing current gain ($\beta_0$). Additionally, the holding voltages ($V_h$) of the shown pnp-structures are located at different currents.

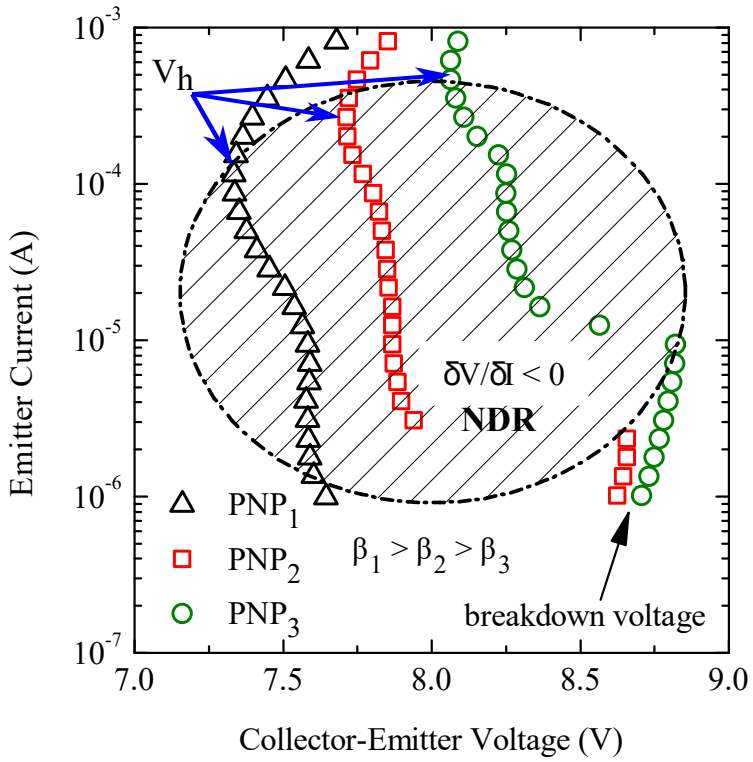



**Figure 3.39:** Typical S-shaped IV-characteristic of measured floating base pnp-transistors. The NDR region (shaded) is identified by a decreasing terminal voltage for increasing device current. The measured transistor structures $PNP_1$, $PNP_2$, $PNP_3$ have different current gain values $\beta_1$, $\beta_2$, $\beta_3$. With increasing current gain, the device $V_h$ is decreasing.

### 3.4.3 Voltage Collapse in a SCR

The SCR has a forward voltage of less than 2 V after reaching the trigger voltage ($V_{t1}$). As the trigger voltage ($V_{t1}$) is significantly higher compared to the forward voltage a strong voltage collapse at the device terminals occurs after switching into the forward conducting state. A SCR operates in a stable on-state after switching and

required a defined holding current ($I_h$) to sustain in the on-state. The anode to cathode terminal voltage is lower than $V_{t1}$ as long as the supplied current is higher than $I_h$. To measure the correct voltage at the device terminals a current forced measurement is recommended according to Figure 3.37. In Figure 3.40 typical IV data is shown for two SCRs. DUT1 and DUT2 have the same pnpn while DUT1 has an additional pn-diode in series. Both structures show the same strong collapse of the voltage after reaching the trigger voltage. The trigger current and trigger voltage of DUT1 and DUT2 is equal because it is only determined by the SCR. This collapse is an inherent device property.

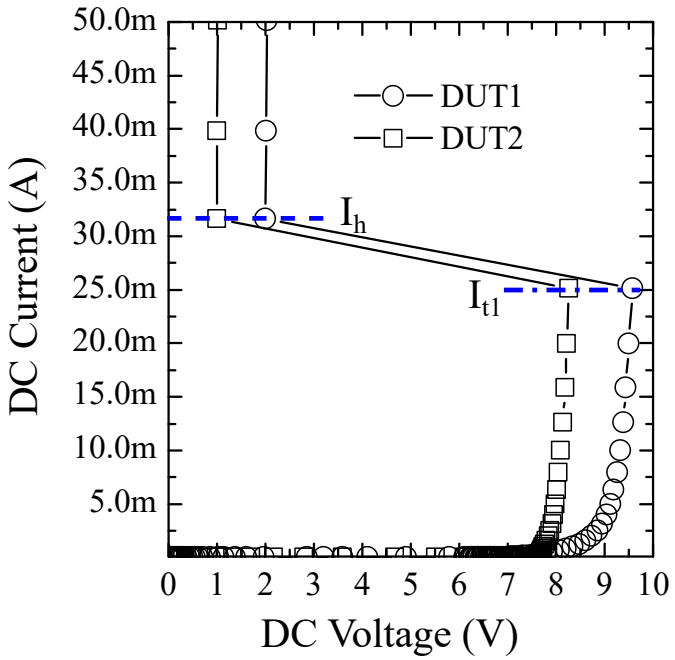



**Figure 3.40:** Measured IV-characteristic of SCRs. DUT1 shows a pnpn with a pn-diode in series while DUT2 shows only the pnpn. The pnpn structure switch into on-state with a forward voltage of about 1 V after reaching the trigger current of 25 mA. The series pn-diode does not change the trigger current and trigger voltage of the device.

### 3.4.4 AC Capacitance Measurements of Sub-Picofarad Structures

Device capacitance of ESD protection devices range from several hundred picofarads to femtofarads based on their application requirements. The extraction of sub-picofarad capacitance values require low parasitic elements of the measurement equipment. Such low capacitance values correspond to high impedance values and thus an impedance analyzer is preferred due to higher accuracy [97], [98]. S-parameter measurements are another option but require higher effort, especially when measuring vertical devices on-wafer because they need tailored contact areas and calibration structures for co-planar probes.

#### LCR-Impedance Analyzer

A HP4248 precision LCR meter with a maximum frequency of 1MHz and an absolute accuracy of $< 10\,\text{fF}$[7] was chosen for characterization as the primary measures capacitance values are below $< 1\,\text{pF}$ and mostly vertical structures.

The LCR meter uses the balance bridge method to determine the DUT impedance [97], [98]. As the device capacitance values are in the range of 0.1 pF to 10 pF which corresponds to impedance values of 16 kΩ to 1600 kΩ, a parallel equivalent circuit model is used (see Figure 3.41). The typical equations for the LCR meters are shown by Equation 3.13.

$$Z = R_s + jX = |Z|e^{j\theta} \quad , \quad \theta = \tan^{-1}\left(\frac{X}{R_s}\right) \tag{3.13}$$

The LCR meter terminals are configured in a four-terminal-pair method to minimize errors by preventing disturbances due to the induced magnetic field of the measurement current in the potential lines. The basic principle is shown in Figure 3.42.

Finally, the calibration is essential to prevent measurement errors due to residual components in the measurement circuit. Figure 3.43 shows the residual components which are introduced by the setup. For capacitance measurements, the open calibration is mandatory to exclude parasitic elements which otherwise introduce significant errors to sub-picofarad DUTs. Figure 3.44 shows an example of measured CV curves of low capacitance devices in the sub-picofarad range at 1 MHz and 25 mV signal amplitude.

[7] for 2pF measurement range at room temperature and 25 mV test signal level [97]

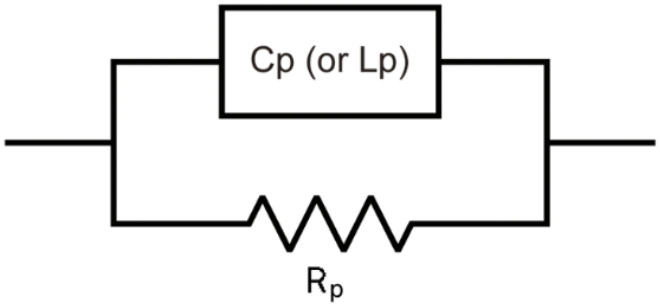



**Figure 3.41:** Parallel equivalent circuit model of the DUT. Low capacitive DUTs like reverse biased diodes or ESD protection structures are modeled by parallel equivalent circuit.

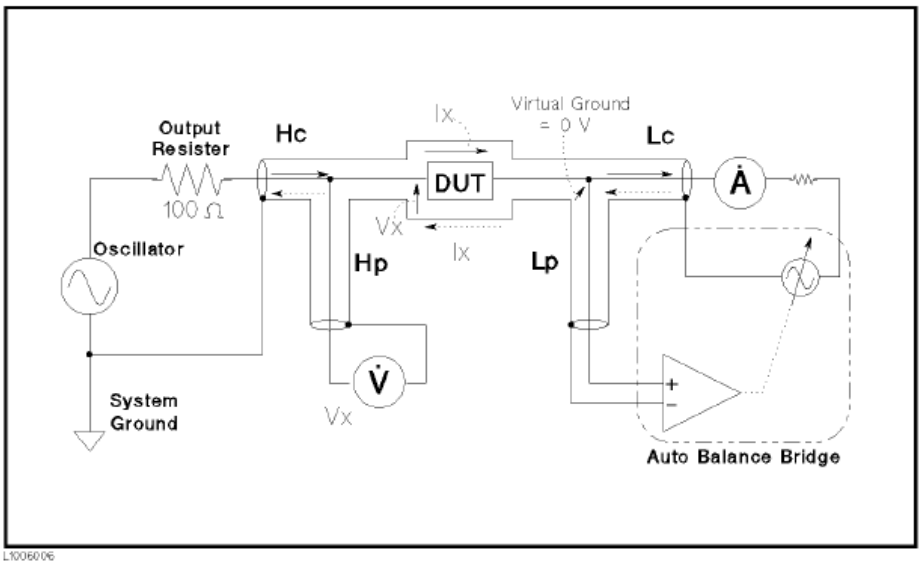



**Figure 3.42:** Four-Terminal Measurement Principle. Figure taken from the HP4284A manual [99].

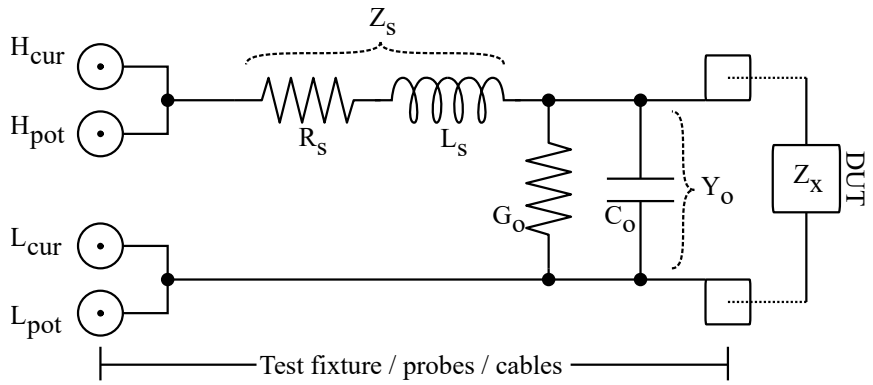



**Figure 3.43:** Schematic of equivalent circuit of the residual components of the measurement setup. Open and short calibration is required to remove offset due to residual components. For capacitance measurements an open calibration is sufficient. $Z_m$ is the measured value, $Z_s$ is the short residual impedance, $Y_o$ is the open residual admittance, $Z_x$ is the true DUT impedance

### On-wafer Characterization of Vertical Devices

During the silicon development phase the devices are characterized on wafer level. The structures are not separated but electrically isolated from each other. As the structures are vertical the substrate is a common terminal. The chuck has to be connected to the high potential of the LCR meter. This is important because the large substrate (compared to the active structures) introduces a high generation recombination currents which results in large noise current and an unbalanced bridge. The low potential has to be connected via needles to the top metal contact of the structure to be measured. Figure 3.45 shows the schematic of the on-wafer measurement setup for vertical devices.

Possible measurement errors are introduced by inaccurate calibration for example by executing the open calibration with large distance of the low potential needle to the wafer top side. Therefore, the probe needle has to be elevated only a few microns from the top metal contact. Additionally, if using an auto-probestation, the measurement error will increase for increasing distance from the calibration point. An interim open calibration has to be considered.

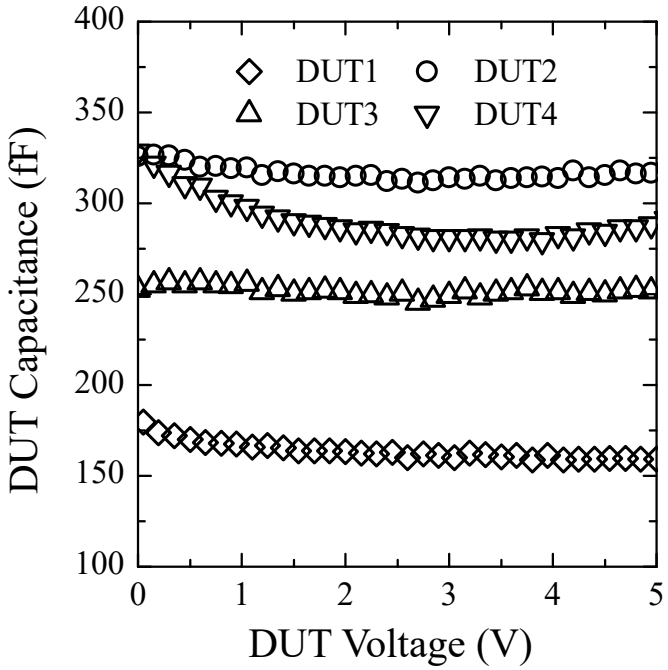



**Figure 3.44:** Measured C-V characteristics of low capacitance devices. Measured at 1 MHz and 25 mV signal amplitude. DUT1-4 have different active area size. Flat characteristic with reduced $\frac{\delta C}{\delta V}$ is better.

Last but not least, it has to be mentioned that lateral on-wafer measurements are not possible, at least for low capacitance structures, due to the fact that the large substrate will shunt the AC current so that the low potential terminal can not sense any signal. The only way to measure lateral structures on-wafer is to separate them physically e.g. by sawing.

### 3.4.5 Transmission-Line-Pulsing Characterization Method

Transmission-line-pulsing (TLP) is a state-of-the-art characterization method for ESD protection devices [96]. TLP offers defined and reproducible pulse shapes which are important for extraction of reliable device behavior. As described by RF theory, a 50 Ω cable with a defined length $L_{cable}$ is charged to a voltage $V_{TLP}$ by a

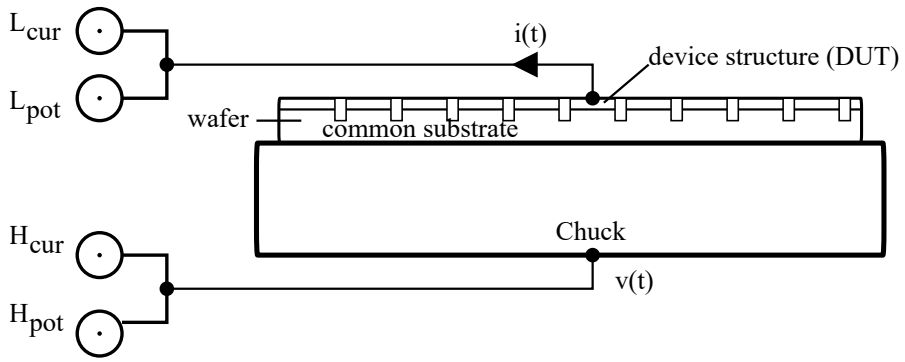



**Figure 3.45:** On-wafer measurement setup for vertical devices. The wafer is placed on a conductive chuck that is connected to the high potential. The single device is separated on the wafer and connected by a probe.

high voltage (HV) source and then discharged by switch operation into the DUT. The pulse duration can be calculated by Equation 3.14.

$$t_p = \frac{2L_{cable}}{v} \approx \sqrt{\varepsilon_r} \cdot \frac{2L_{cable}}{c} \tag{3.14}$$

where $c$ is the speed of light and $\varepsilon_r$ is the corresponding relative dielectric constant of the line. The voltage pulse propagates through the RF matched cable as a wave and arrives at the DUT which has an device impedance $Z_{DUT}$. Figure 3.46 shows the four point Kelvin TLP measurement setup which was used for high current characterization.

### Transient Voltage and Current Extraction

The transient voltage is directly measured at the DUT with a shunt resistor (typically 5 kΩ) integrated within the probe tips (see [100]) which supports on-wafer measurements up to 11 GHz [96]. A typical transient voltage waveform is shown in Figure 3.47 and current waveform in Figure 3.48.

The sampling rate and the bandwidth of the oscilloscope have to be high enough to capture fast transients. According to [101], a bandwidth of five times the signal is

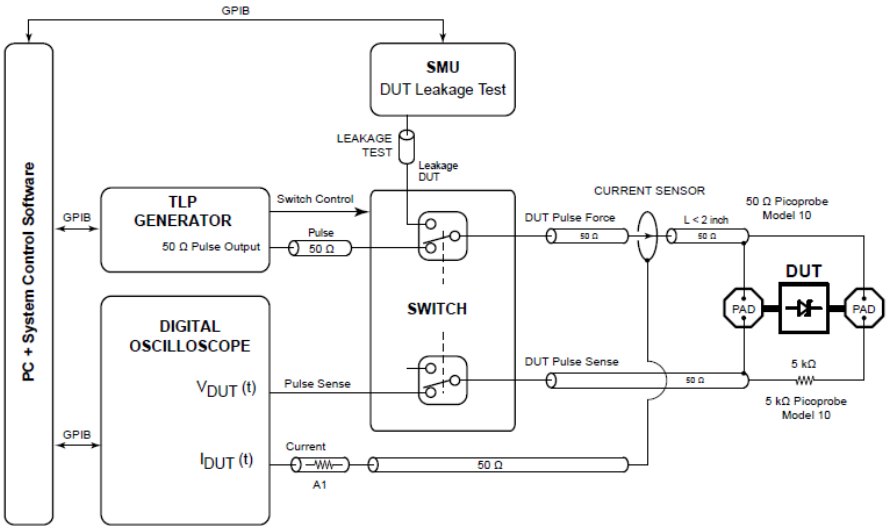



**Figure 3.46:** Schematic of the four point Kelvin TLP measurement setup including DC leakage measurement. Drawing adopted from [96].

sufficient. This corresponds to 4 GHz for 600 ps risetime according to Equation 3.15 and Equation 3.16.

$$BW_{osci} = 5 \cdot BW_{signal} [102], [101] \tag{3.15}$$

$$BW_{signal} = \frac{0.35}{t_{rise(10-90)}} [102] \tag{3.16}$$

All measurements are carried out using a high bandwidth oscilloscope with 12 GHz and $40 \cdot 10^9$ samples per second is used to capture the transient waveform and especially the voltage during the turn-on delay of protection device. The early voltage overshoot, which occurs in the picoseconds range, is of high interest for ESD protection structures as it leads to dielectric breakdown in susceptible gate oxides [39], [3].

The transient current is measured by a Tektronix (CT2) current sensor which has a sensitivity of $5\,\mathrm{V\,A^{-1}}$ and supports high current (50 A µs). The bandwidth is 200 MHz but sufficient for the transient current waveform.

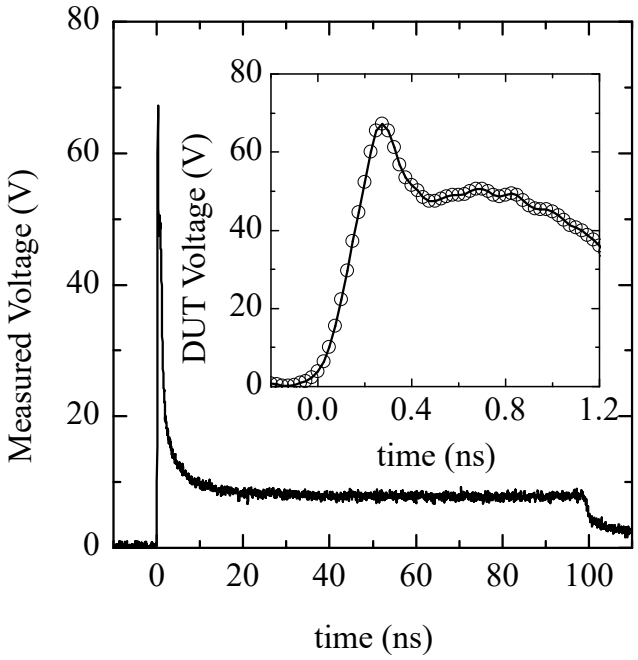



**Figure 3.47:** Transient voltage waveform measured with Picoprobes Model-10 on a 12 GHz oscilloscope with $40 \cdot 10^9$ samples per second. Datapoints are sampled every 25 ps to capture transient voltage overshoot.

Figure 3.49 shows transient voltage waveform of several ESD protection devices that are showing different peak voltages and switching times for a rectangular current pulse with 8 A amplitude.

### On-wafer Measurements of Vertical Structures

A calibration with a calibration substrate is mandatory to eliminate residual components which are introduced by probes and cables as well as attenuators which are needed to prevent the oscilloscope from damage (see 3.46).

Here, the non separated wafer with vertical structures is initially not suitable for on-wafer measurements because the substrate contact is on the bottom side of the wafer. Nevertheless, a device to device measurement concept is possible. Additionally,

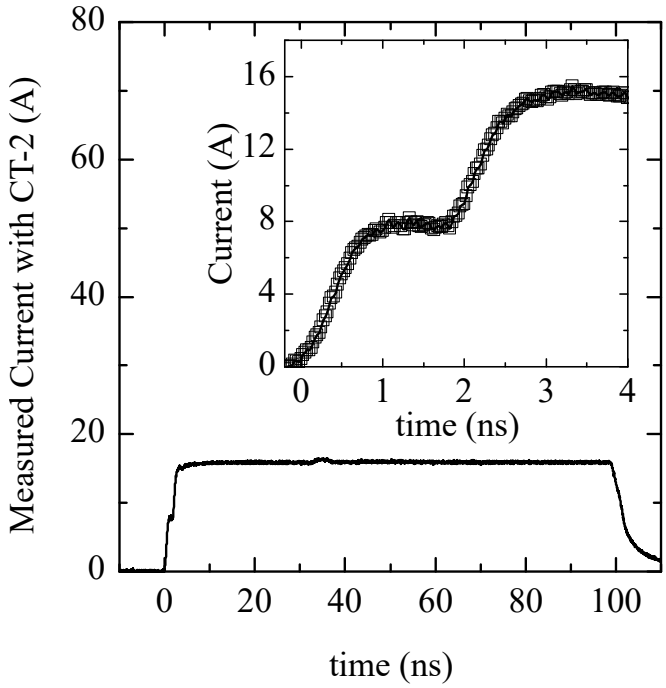



**Figure 3.48:** Transient current waveform measured with Picoprobes Model-10 on a 12 GHz oscilloscope with $40 \cdot 10^9$ samples per second. Current waveform shows a step at the beginning due to reflection and is lacking proper risetime information.

special structures are needed to support a substrate terminal on the topside of the wafer.

Another option, which was used here, is the thinning and a following backside metallization of the wafer. This enables to cut the thin wafer in pieces and solder them to a metallic substrate which can be measured by tilting the probes. Figure 3.50 shows the principle of measuring vertical structures with TLP.

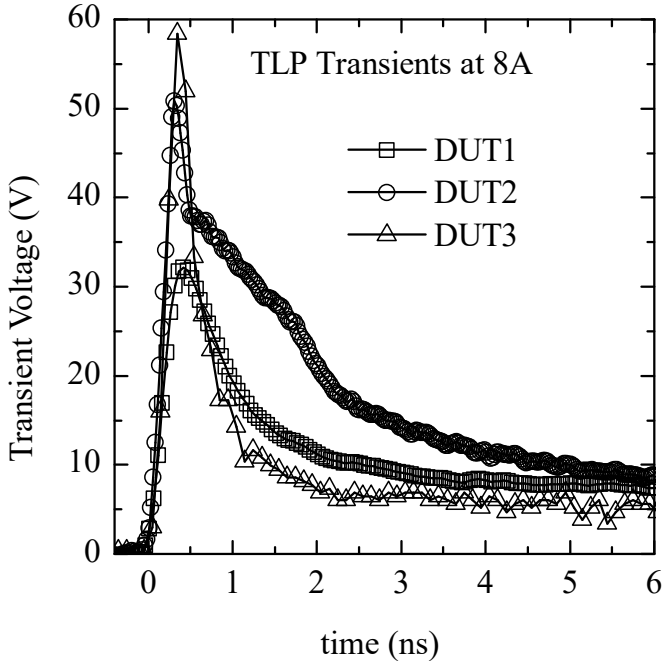



**Figure 3.49:** Transient voltage waveforms of different ESD protection devices. The voltage overshoot is device specific and requires high bandwidth and high sampling rates. DUT3 has a lower sampling rate compared to DUT1 and DUT2.

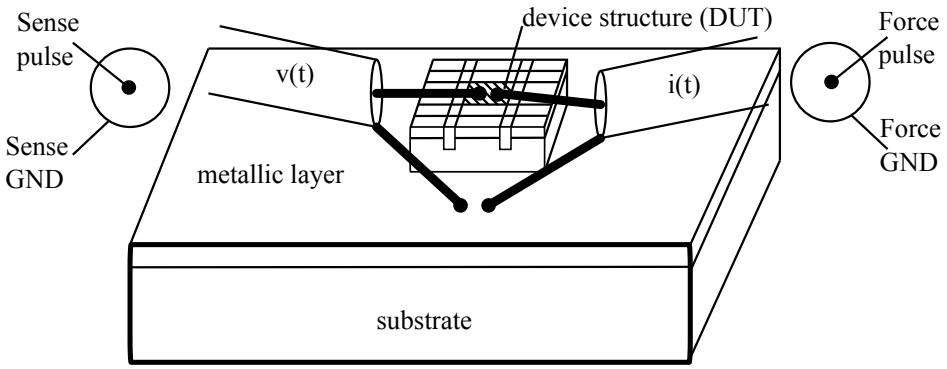



**Figure 3.50:** Setup for on-wafer TLP measurements of vertical structures. A thinned wafer with backside metallization is needed to mount the DUT to a conductive substrate to enable a quasi-planar measurement.

## 3.5 Results

This section summarizes the results of the final device including all improvements.

### 3.5.1 Chip

Figure 3.51 shows a scanning electron microscope (SEM) picture of the final SCR device. The chip consists of two vertical SCRs with an integrated lateral trigger embedded into one piece of silicon. Both devices are interconnected via the silicon substrate which has a low resistivity. Pads are connecting the centered structures via a lateral metal connection. The chip dimensions are 600 µm x 300 µm. The single SCR device has an effective area of 14 000 µm$^2$ with an anode area of 2100 µm$^2$.

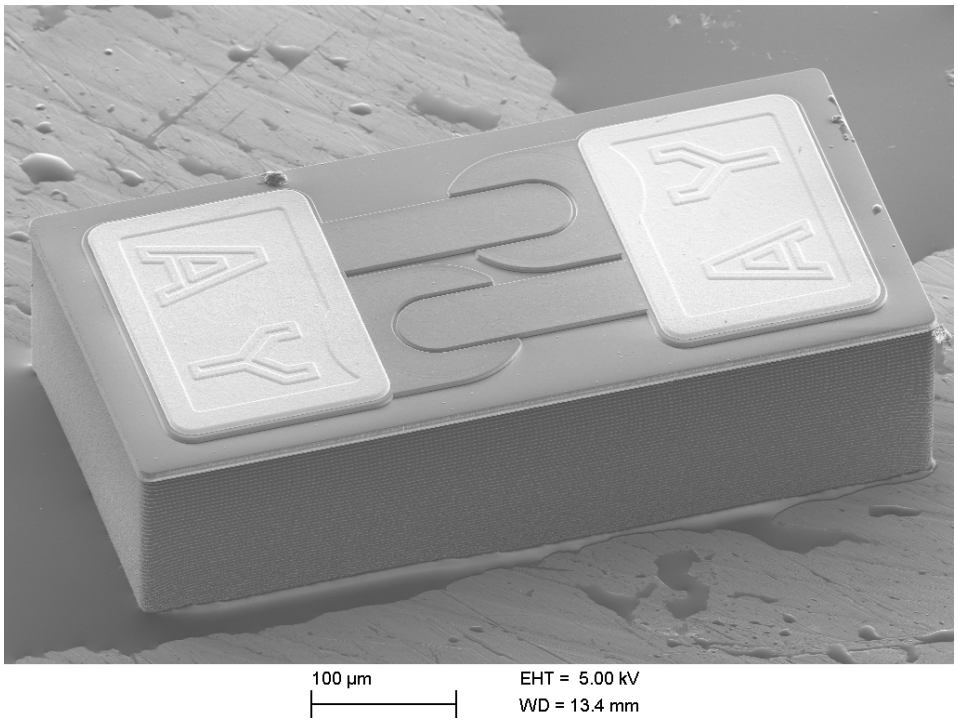



**Figure 3.51:** Chip photo of a vertical SCR with integrated lateral trigger device embedded in a silicon substrate.

### 3.5.2 TLP IV Characteristics

Figure 3.52 shows high current TLP IV characteristics of SCR devices developed in this work and reference SCR devices. The SCR of vendor A has a lower clamping voltage compared to the final LTVT device but a lower ESD robustness which is indicated by the 20 kV vs. 23 kV. The $I_{t2}$ of the final LTVT device is 66% higher and can be explained by the vertical device concept because more device area is available for current conduction in contrast to the perimeter in lateral device concepts like shown in [36], [38] or [63].

### 3.5.3 Device Capacitance Characteristics

Figure 3.53 shows the capacitance over voltage characteristics of SCR devices developed in this work and reference SCR devices. Both LTVT devices show flat capacitance values over voltage while vendor A SCR shows a decrease for higher voltages. This indicates a depletion of a pn-junction. Vendor B shows an increase in capacitance for higher device voltages and can be explained by increased leakage current in a reverse biased pn-junction. The final LTVT device was designed to have 300 fF with highest possible ESD robustness and lowest clamping voltage. Capacitance values equal or less than 300 fF are required for high data-rate applications like USB3.2.

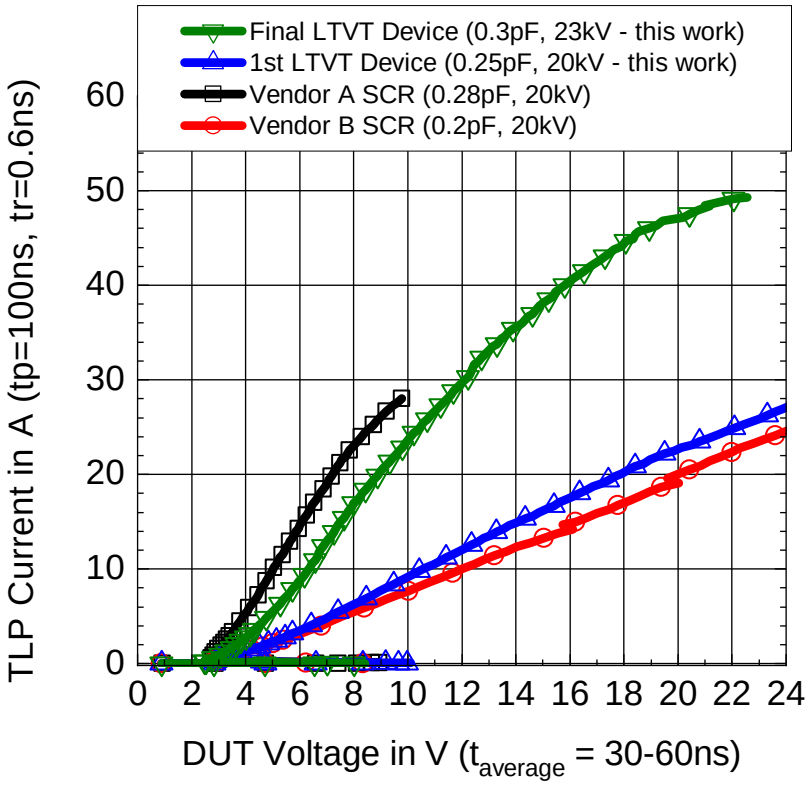



**Figure 3.52:** Comparison of TLP IV characteristics for low capacitance SCR devices. Discrete SCR protection devices from two different vendors (A, B) are compared to the SCRs of this work. Vendor A is a lateral device and vendor B is a vertical device. The final lateral triggered vertical thyristor (LTVT) has the highest TLP failure current ($I_{t2}$) and ESD robustness respectively. Device capacitance is comparable to vendor A while the clamping voltage is higher. The first LTVT device shows a lower clamping compared to vendor B but has higher capacitance and similar ESD robustness.

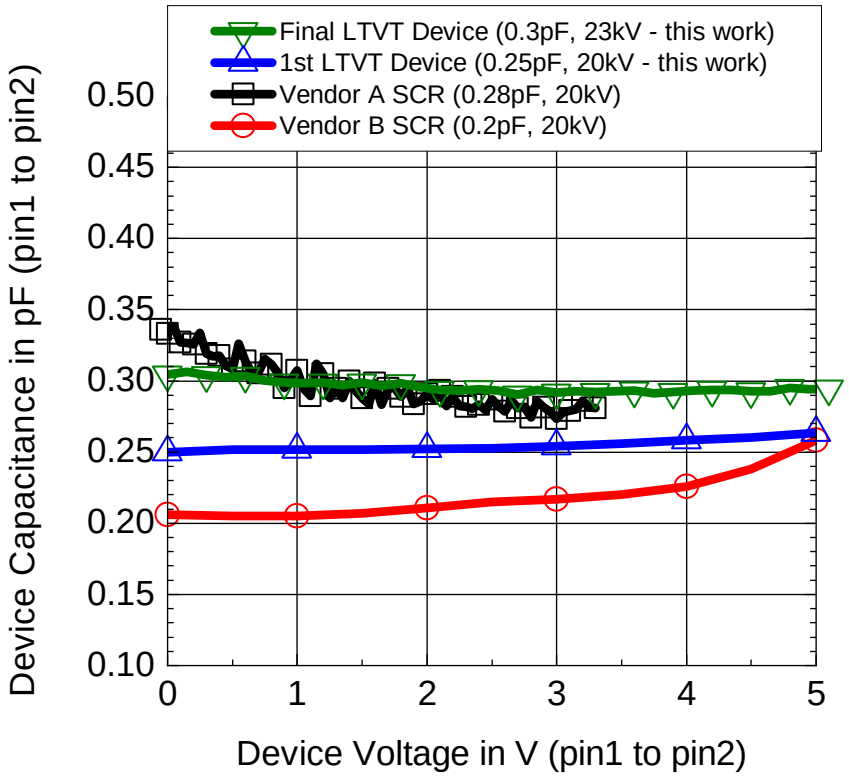



**Figure 3.53:** Comparison of capacitance over voltage characteristics at 1 MHz for low capacitance SCR devices. Discrete SCR protection devices from two different vendors (A, B) are compared to the SCRs of this work. Vendor A is a lateral device and vendor B is a vertical device. The final lateral triggered vertical thyristor (LTVT) has same capacitance value as vendor A device. Vendor B device has the lowest capacitance of the compared devices.

# 4 Avoidance of Current Gain Collapse in Vertical SCR

During the characterization of first silicon samples of the novel vertical protection device, which was described in Chapter 3, a significant increase in clamping voltage was observed which can be accounted to a current gain product collapse violating Equation 2.8. The effect of de-latching is non-destructive but leads to a loss of ESD protection performance by exposing the protected system to higher clamping voltages.

One explanation for the gain collapse was found in the bipolar device theory by the internal current gain in junction transistors. The gain product plays an important role in the forward operation in SCRs and is discussed in this chapter.

Isothermal device simulations based on the drift-diffusion model were used for understanding the device physics during operation.

The vertical four layer structure was optimized by adjusting the doping profile in the base regions to increase the current gain and to prevent gain collapse.

Measurement results of silicon samples of optimized vertical SCRs confirmed the prevention of current gain collapse in the ESD protection device.

## 4.1 Internal Current Gain in SCR

SCRs can be modeled by two interleaved bipolar junction transistors (BJT) [47], [103]. The internal BJTs are then described by their terminal current equations and the current gain $\beta$. It is known that SCRs have a latch-up condition described by the current gain product unity [90], [48], [49]. The current gain of bipolar transistors depends on device technology and operating condition. BJTs can show high current effects [47] which lead to a $\beta$ roll-off effect [103]. At high current densities the gain of the internal BJT structures can drop below a value which is needed to keep the gain product unity. The results is a de-latching of the pnpn-structure from a

low forward voltage. The pnpn has to keep up the current conduction by internal avalanche multiplication. The details are explained in the following subsections.

### 4.1.1 Ideal Shockley Diode

The *Shockley Diode* (pnpn) structure is used to analytically calculate the forward operation condition of a four layer structure due to its simplicity [46], [48], [49]. Figure 4.1 shows the idealized *Shockley Diode* structure with its terminals, internal junctions and currents. It is obvious that in the two terminal pnpn-structure all

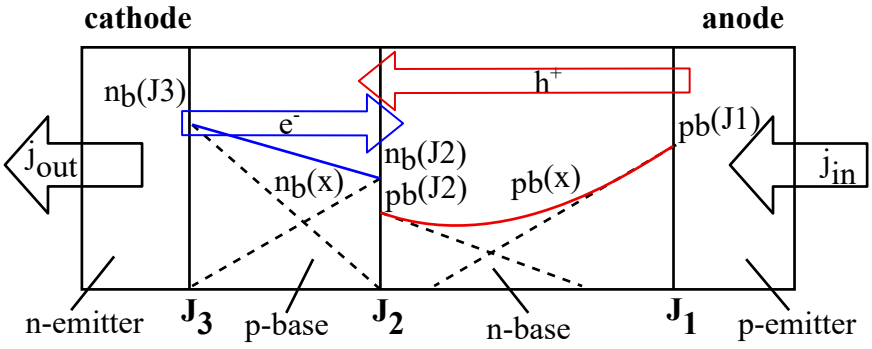



**Figure 4.1:** Idealized Shockley diode structure with internal carrier current compositions. The illustrated state is valid for a positive anode voltage/current during forward conduction of the pnpn-structure.

currents at the three internal junctions must be equal to the current at the external terminal. Applying *Kirchhoff's law* yields Equation 2.8, already introduced in Section 2.3.3.

$$\alpha_{pnp} + \alpha_{npn} = \beta_{pnp} \cdot \beta_{npn} = 1 \quad , \quad \alpha = \frac{\beta}{1+\beta} \tag{4.1}$$

Equation 4.1 describes the stable current conduction with the gain product unity of the pnpn-structure in forward operation, also known as the regenerative positive feedback condition [48]. As the gain is a function of current and it is evident that a transition region from the blocking state (Equation 4.1 not fulfilled) to the conduction state (Equation 4.1 fulfilled) exists.

In the following, a description of the internal processes that are necessary to keep the pnpn-structure in forward operation is given. The transition from the blocking state is initiated by injection of a first internal base current into n-base or p-base. This can be the avalanche breakdown at $J_2$. The initial base current drives both interleaved base-emitter junction ($J_1$ and $J_3$) into forward direction. As long as Equation 4.1 holds true, the pnpn-structure operates in a forward conducting state by supplying the p-base and n-base region with carriers from the n-emitter and p-emitter (anode and cathode). The pnpn structure has to balance the carrier concentration in the p-base and n-base region to keep the gain product unity. This is possible by reducing the collector current which are at the same time base currents. This is known as saturation in BTJs which can be applied here as well. The current gain in saturation compared to active mode is lowered because the collector-base junction is forward biased [46], [49]. The minority concentration gradient in the base region is reduced and the diffusion current lowered. The internal voltage can be described by $V_{be} + V_{cb}$ and by changing $V_{cb}$ the Equation 4.1 hold true and keeps the pnpn in forward conduction. The device voltage is therefore $V_{pnpn} = V_{be(J1)} + V_{cb(J2)} + V_{be(J2)}$ (e.g. $V_{pnpn} = 1\,V$ with $V_{be(J1)} = 0.7\,V, V_{cb(J2)} = -0.4\,V, V_{be(J2)} = 0.7\,V$ at forward conduction).

### 4.1.2 Vertical SCR with Single Base Shunt

In vertical SCRs, Equation 4.1 has to be extended to describe the forward switched-on operation condition of structures presented in Chapter 3.1. The difference between the ideal Shockley diode and pnpn-structures presented in this work is the base-emitter shunt resistor that is necessary for controlled switching into the latched state by a designed trigger current value (see Section 3.1.4). The triggering was introduced for the ideal Shockley diode and is extended to an embodiment of a vertical silicon structure with a controlled holding current ($I_h$) for system applications [29], [65], [30], [31], [36].

Considering the vertical pnpn-structures presented in this work, a shunt resistor between emitter and base of one internal transistors is used to control the switching while the other transistor has a floating base configuration. The base-emitter voltage (see Figure 4.2) is controlled by the shunt resistor $R_{be,p}$ for low currents and will be overtaken by the exponential characteristics shown in Figure 4.3 and described by the case Equation 4.2.

$$V_{be} = \begin{cases} k_B T \cdot \ln\left(\frac{I_e}{I_{s0}} + 1\right) & , I_d > I_{Rbe,p} \\ I_{Rbe,p} \cdot R_{be,p} & , I_e < I_{Rbe,p} \end{cases} \tag{4.2}$$

The transition region is determined by the npn-base current ($I_{b,npn}$) which is proportional to the exponential term shown in Equation 4.3 and is related to the emitter current ($I_e$) by Equation 4.4. The current through $R_{be,p}$ is not taking part to maintain the SCR function but has to be supplied by the structure. Thus, Equation 4.5 is used to calculate the gain product for a structure with one shunt resistor between base and emitter.

$$I_b \propto e^{\frac{-qV_{be}}{k_B T}} \tag{4.3}$$

$$I_d = I_{b,npn} \cdot (1 + \beta_{npn}) \tag{4.4}$$

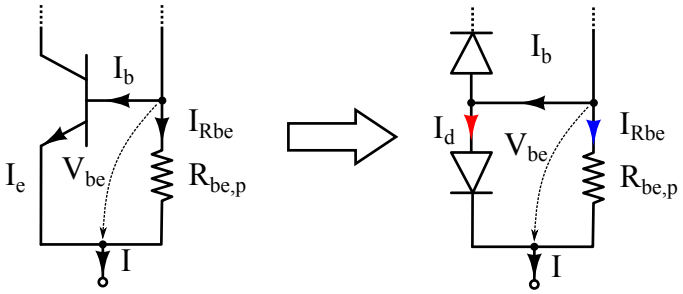
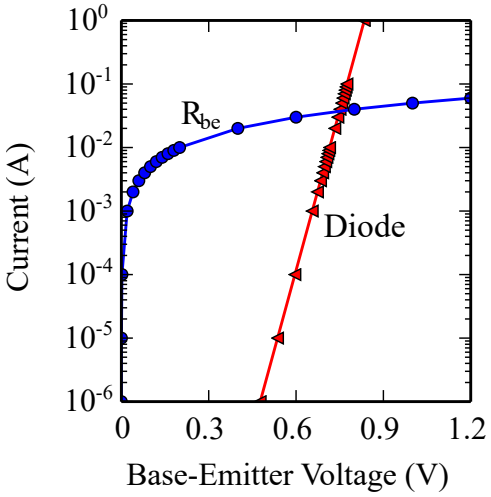
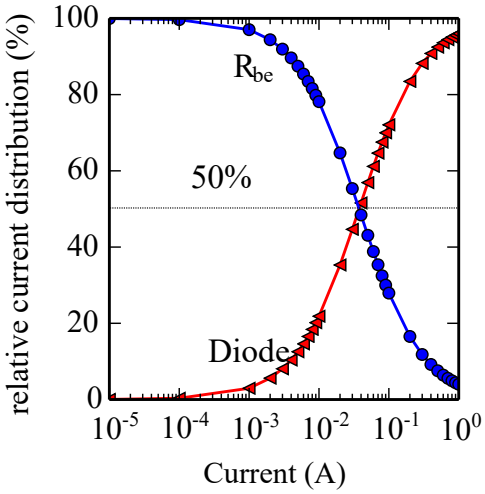



**Figure 4.2:** Shunted base-emitter circuit representation and a simplified two diode representation (Ebers-Moll). $I_{R,be}$ dominates at low currents while ($I_e$ takes over at high currents.

At high currents the base-emitter diode takes over and the second term of Equation 4.5 tends to zero for $I \to \infty$. In contrast, for low currents the second term is several orders of magnitude higher because it follows the behavior shown in Figure 4.3.




(a)




(b)

**Figure 4.3:** Calculated base-emitter forward voltage versus current of an ideal diode and a resistor (a) according to Figure 4.2 and the corresponding current distribution (b) between resistor and base-emitter diode.Following model parameters were used: $R_{be} = 20\,\Omega$, $I_s = 10\,\text{fA}$. Diode resistance neglected because it is less than $1\,\Omega$

Thus, Equation 4.5 is used to calculate the gain product for a structure with one shunt resistor between base and emitter.

$$\beta_{pnp} \cdot \beta_{npn} = 1 + \frac{V_{be}}{R_{be,p} \cdot I_{b,npn}} = 1 + \frac{I_{Rbe,p}}{I_{b,npn}} \tag{4.5}$$

### 4.1.3 Gain Product Collapse (De-latching)

The SCR in forward operation condition is operating its internal transistors in saturation to keep the required gain product condition (e.g. Equation 4.5). In saturation the gain is reduced and lower than the maximum gain $\beta_0$ in active mode. At high currents the internal BJT shows high level injection effects which reduce the gain inverse proportional to the collector current ($\beta_{HI} \propto \beta_0 \cdot J_c^{-1}$) [46]. *Romanescu et al.* points out the beta (current gain) degradation [104] at high injection levels due to the slow down of carriers in the base region and the high recombination in the collector base region [103]. The combination of saturation and high level injection yields a gain collapse model that is presented in this work by Figure 4.4. Here, $\beta_{HI}$ reduces $\beta_{0,npn}$ and decreases the theoretical $\prod\beta_0$. $\beta_{0,pnp}$ stays constant for simplification. The more important $\prod\beta_{SCR}$ which represents the SCR operation stays at unity. At a certain current density the crossing point between $\prod\beta_0$ and $\prod\beta_{SCR}$ is reached and the gain collapse happens.

The SCR is forced out of saturation and the collector-base switches to a reversed biased state to reach $\beta_0$ for pnp and npn. The collector-base reverse voltage increases until avalanche breakdown is initiated. The avalanche current in the collector-base junction keeps the SCR structure in forward conducting state by supplying additional current. Both internal transistors operate as avalanche transistors in a stable state [4].

A physics-based compact model for CMOS SCR devices based on modified Ebers-Moll transistor model describes the influence of $\beta_{pnp}$ and $\beta_{npn}$ on latching behavior by comparing a constant gain with a current dependent gain [105], [106]. It was shown that only a variable $\beta$ gives accurate trigger results and matches the measured data. By using a constant gain in the model, the SCR was not able to latch and showed a higher holding voltage than expected. This can be explained by Figure 4.4 and the de-latching model.

This operation mode is used in so called high holding voltage SCRs. Several publications describe the opportunity to increase the holding voltage and subsequently

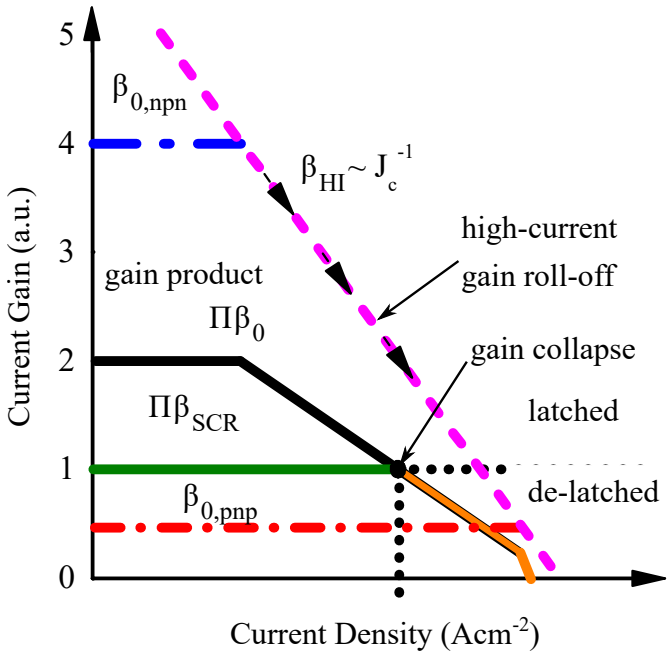



**Figure 4.4:** Schematic of idealized common-emitter amplifications during high current roll-off. $\prod\beta_0$ is the theoretical maximum gain product and $\prod\beta_{SCR}$ is the gain product of the pnpn-structure during latch-up operation. $\beta_{HI}$ is the high current gain roll-off. De-latching occurs after gain product is less than the latch-up condition due to gain roll-off.

the forward voltage by increasing the base widths [65], [68], [31]. In fact, this is a a method to influence the internal current gain which was not described by the authors. The gain of the internal transistors is reduced to a value so that the gain product cannot fulfill the latching condition for any current and the SCR is never working in saturation. By lowering the gain further, the holding voltage is increased as well. In this case, the gain product collapse is a desired results to prevent the deep snapback of SCRs.

## 4.2 Discussion on Current Gain Product

Several publications reporting model approaches of SCR for ESD protection with the target to achieve an accurate modeling of the switching behavior in the ESD domain (nanosecond events and high current densities) [103], [106], [107], [105].

Figure 4.5 shows a typical cross-section of a lateral SCR which is used in literature for compact modeling purposes [4], [103], [106]. The shown device has two base-emitter shunt resistors. Equation 4.6 is found in [6] and [90] for CMOS SCRs with two shunt resistors (n-/p-well resistance $R_{be,n}$, $R_{be,p}$). Here, the current gain product expression is given as an inequality.

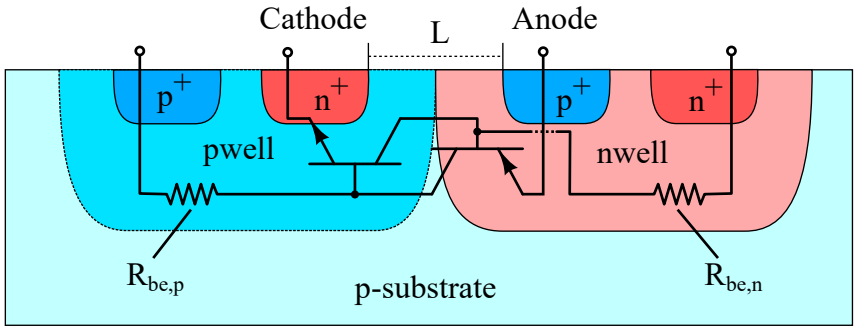



**Figure 4.5:** Cross-section with included circuit representation of a lateral pnpn-structure in a CMOS technology. PWELL and NWELL resistors are controlling the base-emitter voltage before switching. The anode to cathode spacing (L) is a main device parameter and scaled down in state-of-the-art CMOS nodes.

$$\beta_{pnp} \cdot \beta_{npn} > 1 + \frac{(\beta_{pnp}+1)(\frac{I_{R_{be,p}}}{\beta_{pnp}})}{I - I_{R_{be,p}} - I_{R_{be,n}}(1+\frac{1}{\beta_{pnp}})} \tag{4.6}$$

The findings in this work lead to the results that Equation 4.6 has to be an equality because the continuity equation is violated for a gain product that is higher than necessary. This is also explained by the case without shunt resistors (compare

Equation 2.8) and confirmed by device simulations in Section 4.3.3. The gain product is either matching the latching condition or less which results in de-latching.

By assuming that the forward current is significantly higher than the current through the well resistors ($I \gg I_{Rbe,n}, I_{Rbe,p}$), the second term of Equation 4.6 becomes negligible. It means that the small portion of the inserted current is shunted by the base-emitter resistors while most of the current is contributing to SCR function. The required gain product at high currents tend to unity for $I \rightarrow \infty$. Comparing the three different configurations with no, single and both base-emitter shunt resistors, the result at low current before and during latching plays the major role. At high currents the latch-up condition tends to gain product unity and the basic SCR function dominates.

## 4.3 Simulation based Current Gain Extraction in SCRs

Simulations are commonly used as efficient tools to analyze semiconductor structures [51] and to predict the performance of bipolar devices [108]. The necessity to extract the gain of the internal transistors in SCRs and predicting the gain collapse leads to the demand for a simulation based method. The advantages are less effort to design special test-chips and a shorter feedback loop for device optimization like demonstrated in Section 4.4. Therefore, two approaches are introduced and discussed in this thesis.

1. TCAD device simulations
2. Circuit simulations

Both simulation methods are capable of simulating the latching and de-latching process in SCRs. TCAD offers the advantage to simulate the device physics with more details (e.g. 2D effects) compared to the circuit simulation with a compact model. Another advantage is the option to model the device regions (e.g. transistor base) and the corresponding doping profile which yields better results for custom structures (e.g. P-i-N-P-N device).

### 4.3.1 TCAD based Gain Extraction

A new TCAD based extraction procedure was developed to extract the current gain during forward operation in a pnpn-structure. In the following, a method to extract

the internal current gain and the product of the interleaved transistor structures in a SCR using TCAD device simulator is presented.

The four layer structure and the internal currents are defined in Figure 4.6. The

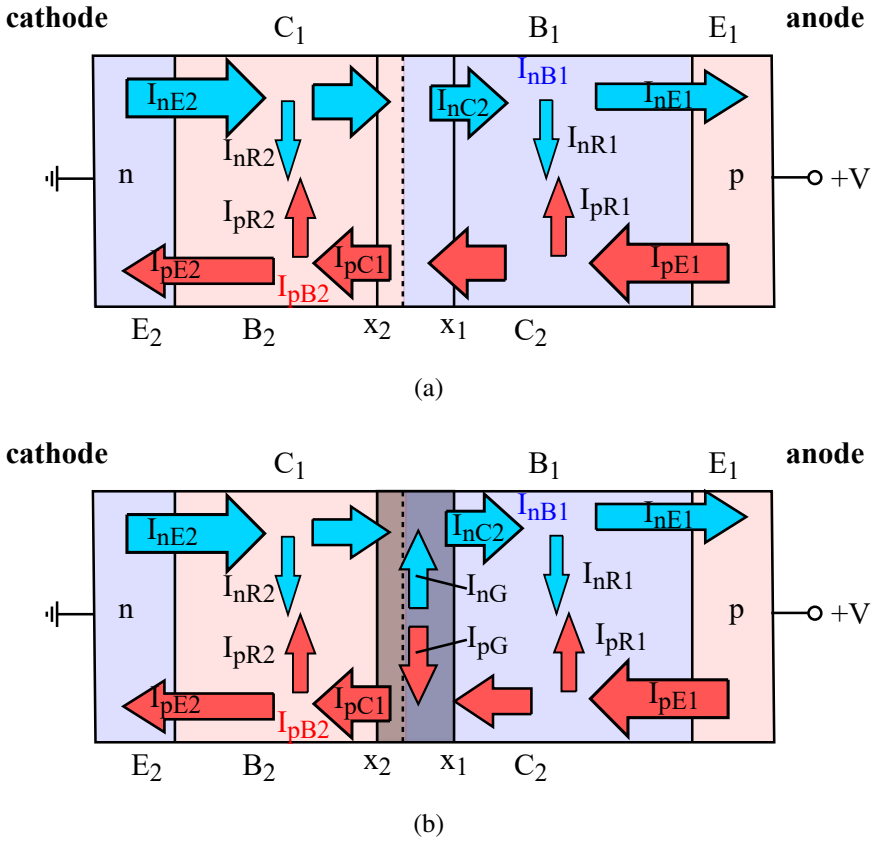



**Figure 4.6:** Schematic of a four layer structure in forward operation and the internal currents. $x_1$ and $x_2$ are the extraction points for the base currents which are necessary for gain extraction. The collector-base region between $x_1$ and $x_2$ is forward biased in (a) and reversed biased in (b). The generation current in (b) is the result of avalanche multiplication

emitter current at the anode ($I_{E1} = I_{pE1} + I_{nE1}$) side is equal to the emitter current at the cathode side ($I_{E2} = I_{nE2} + I_{pE2}$). $I_{E1} = I_{E2} = I_{device}$ which is the input current. For gain calculation, the collector current $I_{C1,2}$ and and the base current $I_{B1,2}$ have to be extracted for each transistor. The interleaved transistors share one collector-base

junction between $x_1$ and $x_2$ which means that $I_{C2} = I_{B1}$. To reduce the extraction effort only the majority carrier current is taken into account. Recombination current in the base region outside of $x_1$ or $x_2$ is neglected because the effect on gain is negligible at high current (e.g forward operation). Therefore, only the electron and hole currents at $x_1$ or $x_2$ are required to calculate the current gain. $x_1$ and $x_2$ is chosen with respect to the space charge region of the collector-base junction to prevent numeric artifacts because this region is dynamic during SCR operation. Equation 4.7 summarized the two equations for the gain of the interleaved pnp and pnp transistor. and Equation 4.8.

$$\beta_{pnp} = \frac{I_{pC1}}{I_{nB1}} = \frac{J_p|x_2 - J_{pG}}{J_n|x_1} \tag{4.7}$$

$$\beta_{npn} = \frac{I_{nC2}}{I_{pB2}} = \frac{J_n|x_1 - J_{nG}}{J_p|x_2} \tag{4.8}$$

As long as no avalanche multiplication occurs in the collector-base junction the generation current is set to zero ($J_{pG} = J_{nG} = 0$). When avalanche multiplication takes place the generation current has to be calculated at $x_1$ and $x_2$ by Equation 4.9.

$$J_{pG} = q \cdot \int_{x1}^{x2} G_p(x)dx, \qquad J_{nG} = -q \cdot \int_{x_1}^{x_2} G_n(x)dx, \tag{4.9}$$

The extraction routine requires $x_1$ or $x_2$ as input parameter for 1D simulations. Extending to 2D and 3D simulations requires several extraction locations in the device to be simulated and enables a multidimensional current gain mapping. This can be used for latch-up simulations because the device locations with the highest current gain are visualized.

### 4.3.2 Isothermal DC Device Simulation of a 1D Shockley Diode

One dimensional simulations of the ideal structure, defined in Section 4.1.1, were carried out by TCAD software to validate the theoretical considerations. The device characteristic, switching process and the internal gain in the pnpn-structure were extracted by post processing the internal current densities during simulation.

Figure 4.7 shows the pnpn-structure and doping profile which were used for device simulations. The junction at 9 µm has a breakdown at 15 V. The second portion of

the n-base region (1 µm to 5 µm) consists of a lowly doped region to provide a large depletion region in the reverse direction and a low junction capacitance as described in Section 2.4.

The two described design measures lower the common-emitter amplification of the pnp-structure because they increase the required n-base width by the length of the lowly doped region and increase the doping concentration in a part of the n-base. Both emitter regions (0 µm and 12 µm) are implanted with highest doses ($5 \cdot 10^{15}$ cm$^{-2}$) to minimize series resistance and maximize the emitter efficiency.

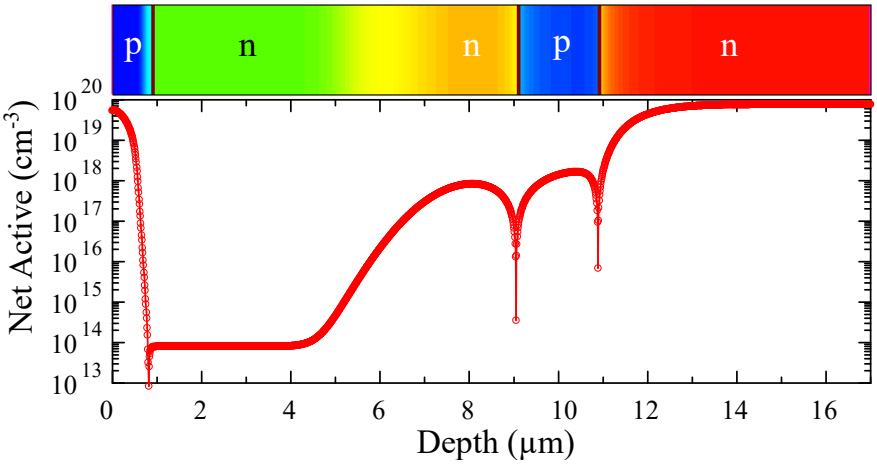



**Figure 4.7:** Simulated 1D Shockley diode structure with doping profile. The doping profile is designed to fulfill low voltage and low capacitance requirements (Section 2.4).

The DC simulation result of the 1D Shockley diode structure is shown in Figure 4.8. The current-voltage characteristics together with the extracted gain of each internal transistor structure and the corresponding gain product is shown over the forward current density up to $1 \cdot 10^6$ Acm$^{-2}$ (ESD regime). The different operation modes (blocking, switching, latched) of the pnpn-structure are visible for different current densities and the de-latching at $5 \cdot 10^4$ MAcm$^{-2}$ is predicted by violation of Equation 4.1.

After the internal junction breakdown voltage is reached the pnpn-structure goes from the blocking state into the switching state and the internal common-emitter amplifications ($\beta_{npn}$, $\beta_{pnp}$) increase in the range $1 \cdot 10^{-3}$ Acm$^{-2}$ to $1 \cdot 10^{-1}$ Acm$^{-2}$.

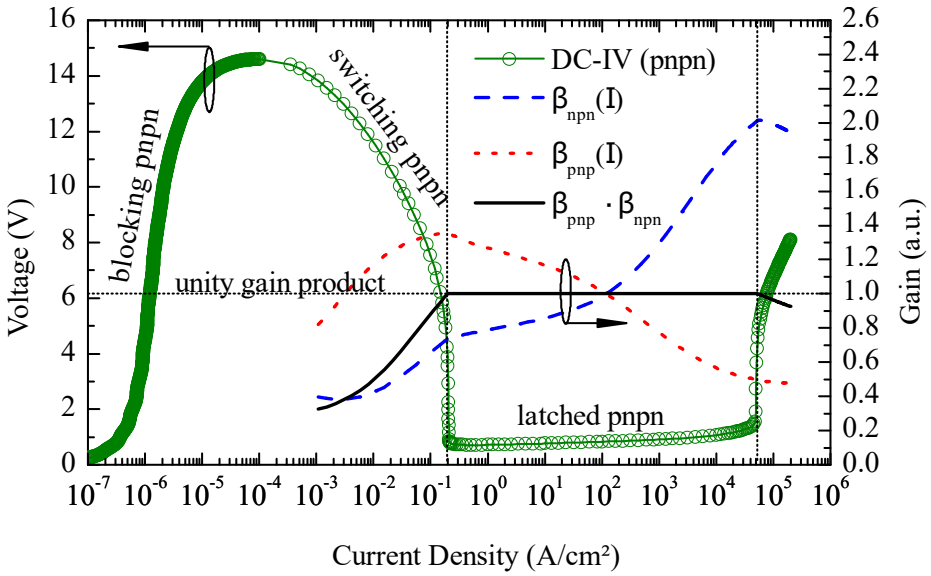



**Figure 4.8:** Simulated DC-IV characteristic of a 1D Shockley diode structure with the internal gain as function of current density. The gain product unity indicates the latched state of the pnpn-structure.

In the switching phase the internal transistors are going into saturation and leaving the avalanche breakdown regime [4], [5]. The unity gain product is fulfilled after the internal transistors can supply each other with a base-current that is sufficient to conduct the forward current without the avalanche breakdown ($2 \cdot 10^{-1}$ Acm$^{-2}$ to $3 \cdot 10^{4}$ Acm$^{-2}$).

The forward voltage is reduced to less than 1 V (compare Section 2.3.3). $\beta_{npn}(I)$ and $\beta_{pnp}(I)$ are balanced by the internal collector-base voltage. The simulation shows that $\beta_{npn}$ increases with current while $\beta_{pnp}$ decreases. $\beta_{npn}(I)$ and $\beta_{pnp}(I)$ values in the latched state (at $2 \cdot 10^{-1}$ Acm$^{-2}$) are lowered in saturation to maintain gain product unity.

Figure 4.9 shows the free carrier concentration between $4 \cdot 10^{4}$ Acm$^{-2}$ and $6 \cdot 10^{4}$ Acm$^{-2}$ and confirms HLI in the lowly doped n-base region. The npn-structure is able to compensate the decline of $\beta_{pnp}$. After the $\beta_{npn}$ enters HLI (at $6 \cdot 10^{4}$ Acm$^{-2}$)

the gain product unity can not be maintained anymore. The gain product collapses and the de-latching takes place.

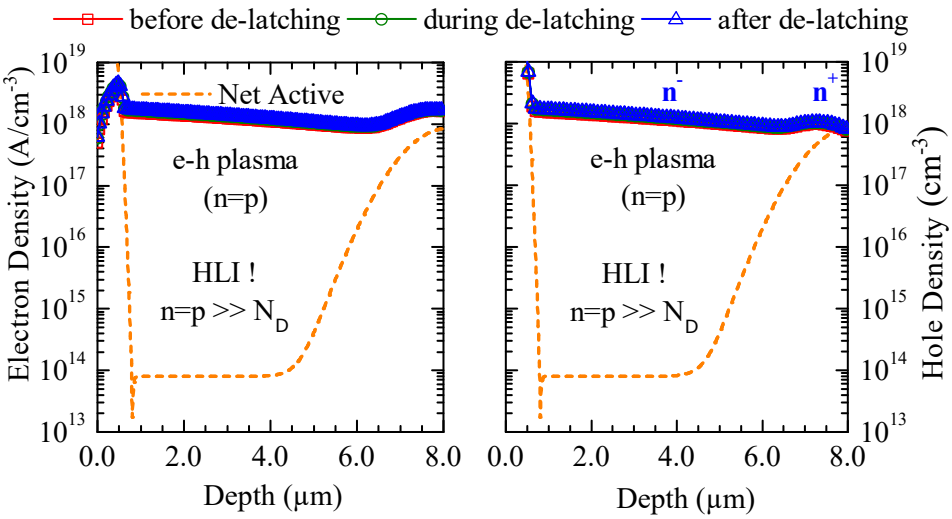



**Figure 4.9:** Simulated carrier densities in the lowly doped n-base region in a 1D Shockley diode at high current densities. High level injection is pronounced in the n-base region.

Figure 4.10 shows the simulated electron and hole densities. Figure 4.11 illustrates the simulated generation and recombination. Both show the collector-base junction region (8 µm to 10 µm) during the gain collapse which starts the transition into the de-latched state. The internal collector-base junction (9 µm) potential difference is smaller than the build-in voltage during saturation. Minority carriers are injected from the base region into the collector region and vice versa. Recombination takes place at the collector-base junction area [103] and impact ionization is not present. During the de-latching process a decrease in the free carrier concentration at the collector-base junction is observed. It indicates transition from saturation into forward active operation in the internal transistor. This is necessary to increase the collector current of the pnp which is the base current of the npn and vice versa. Hence, an increase of the pnp and npn gain to keep gain product unity. After the internal transistors reach forward active operation the gain saturates. Further increase in collector current is necessary and the reverse voltage in the collector-base increases until avalanche breakdown is initiated. The avalanche process generates free carriers that are required

to conduct the forward current and fulfill the unity gain product. This is confirmed in Figure 4.11 with a decrease of the recombination and an increase of the impact ionization. Recombination and generation have different signs which is not shown due to the logarithmic plotting in Figure 4.11.

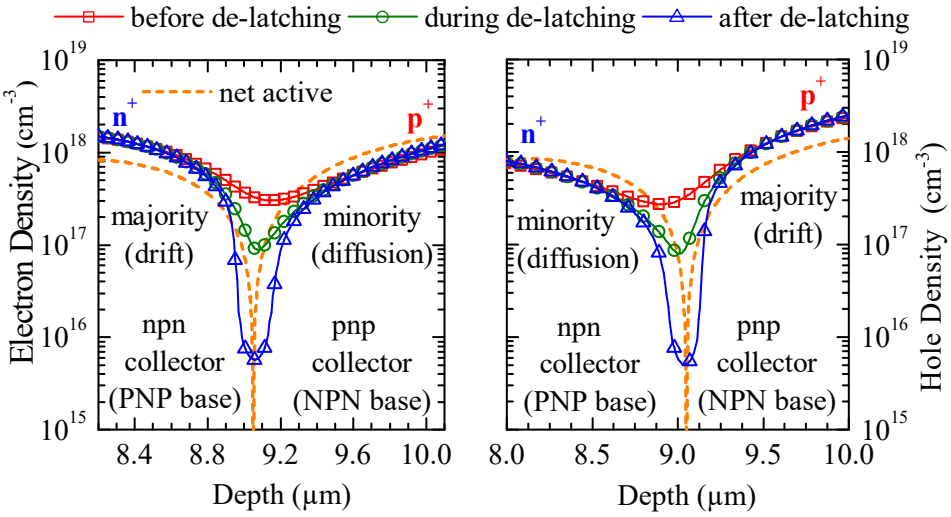



**Figure 4.10:** Simulated carrier density at the collector-base junction in a 1D Shockley diode during the gain collapse process. After the pnpn-structure de-latches the collector base junction is depleted and the internal transistors operate in forward active.

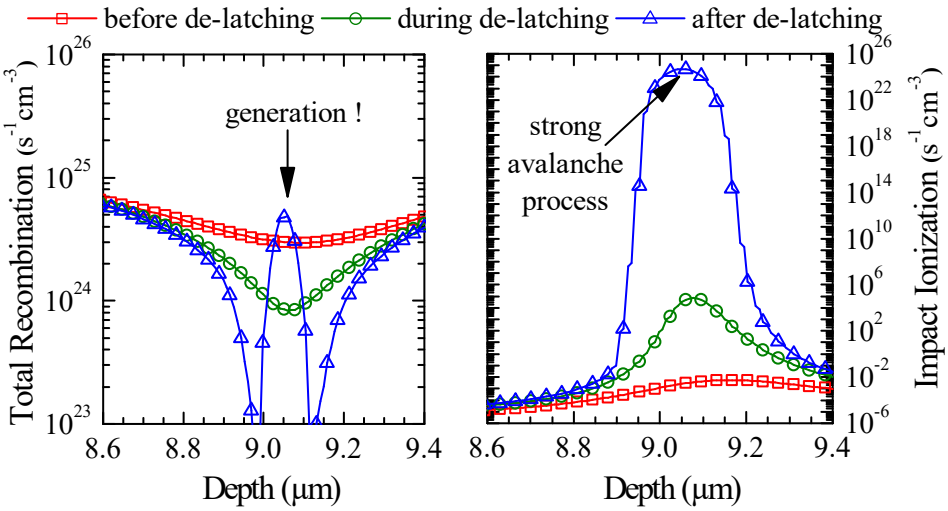



**Figure 4.11:** Simulated carrier recombination and impact ionization at the collector-base junction in a 1D Shockley diode during the gain collapse process. After the pnpn-structure is de-latched the avalanche generation current maintains the forward conduction.

### 4.3.3 Gain Product Simulation with an Equivalent Circuit

An equivalent circuit (EC) utilizing Spice-Gummel-Poon (SGP) was used to simulate the internal current gain and the gain product during latch-up operation in a SCR device. The scope of this EC is to demonstrate the theory of the gain product collapse which was introduced and observed in silicon devices. Additionally, the proposed EC is one approach to reduce the simulation effort compared to TCAD.

#### SCR Model Description

The EC circuit was simulated with *Advanced Design System* (ADS) software. A model for the avalanche breakdown was used from [109] to trigger the circuit because the SGP BJT models does not include avalanche breakdown. The complete circuit is found in the appendix. The SCR EC consists of two bipolar junction transistors. A standard BJT Model from the ADS library was used for the PNP and NPN transistor

(BJTM1 and BJTM2). A pnp and npn are interleaved so that the base terminal connects the collector terminal of the opposing one.

A Symbolically-Defined Device (SDD) is used to model the avalanche source with an equation from [109]. The chosen exponential expression for the avalanche has better convergence during simulations compared to the commonly used Miller formula with its singularity [57], [5]. The SDD takes the potential difference between the pnp-base and the npn-collector as input and multiplies the pnp-base current to simulate a avalanche multiplication effect. The avalanche current is then forced into the npn-base and the base-emitter shunt $R_{BE}$. The purpose of $R_{BE}$ can be recaptured in Section 4.1.2. The current gain of each transistor in its specific operation point is calculated by extracting the terminal currents.

### Parametrization

A set of parameters for the PNP and NPN transistor (BJTM1 and BJTM2) are documented in the appendix. For the following simulation results the gain ($\beta_0$= Bf) was increased to higher values for better graphical illustration. The conclusions are independent of the assigned values. For PNP the $\beta_0$ has been set to 0.2 and for NPN $\beta_0$ has been set to 45. The breakdown voltage Vbr is set to 9 V. $R_{BE}$ is set to 200 Ω if used. The knee current $I_{kf}$ determines the roll of and is set to 0.1 for both transistors. Other parameters are less significant and will not be discussed here.

### Results Floating SCR (Shockley diode)

Figure 4.12 illustrates the simulation results of a Shockley diode with its internal current gains (gray line and red line) and the gain product (black dashed line). The individual current gains are increasing with anode current because the avalanche source multiplies the leakage current of the PNP and feeds the base of the NPN until the trigger point (1) is reached. Afterwards the gain product unity is reached and the pnp switches into saturation. Here, only one transistor can go in saturation mode because the equivalent circuit is build of two separated devices which is not true in a real SCR (one shared collector-base for pnp and npn). The circuit is now operating in the latched state until the gain product collapses (3) due to the $\beta$ roll-off. It can be observed that the pnp gain increases again before de-latching (3) which is explained by the transition from saturation into forward active to increase the

gain. For both simulated gains a roll-off kicks in at $I_{kf} = 0.1$ A and lead to a gain collapse (3) at 1 A. The simulated current-voltage curves are shown in Figure 4.13.

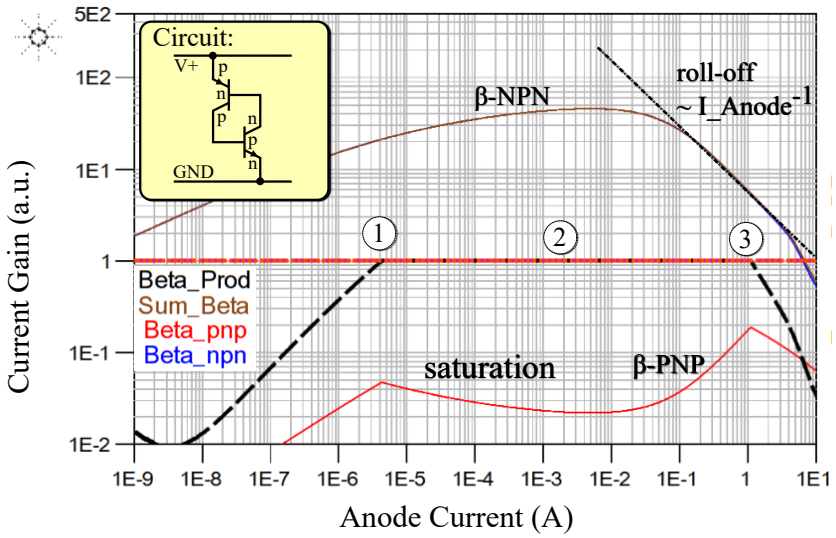



**Figure 4.12:** Simulated current gains and gain product of interleaved bipolar junction transistors. The internal gain product matches the latching condition (2) according to Equation 4.5 indicated by the dashed lines after triggering (1) and before de-latching (3).

The previously described operation regions for the current gain product are identified in the simulated IV characteristic and clarify the relation and importance of the current gain product with respect for the electrical characteristics.

### Results SCR with a Single Shunt

Figure 4.14 shows a SCR with a single base-emitter shunt resistor ($R_{BE}$) included and the corresponding simulated current-voltage characteristics. The value of $R_{BE}$ determines the current ($I_{t1}$) which is needed to open the NPN transistor and start the triggering into SCR forward operation (2). The influence of $R_{BE}$ on the gain product is described by Equation 4.5. The de-latching (3) happens at the same current (1 A) value because it depends on the gain characteristic and $I_{kf}$ respectively. The SGP model supports the current gain roll-off which is responsible for a gain product

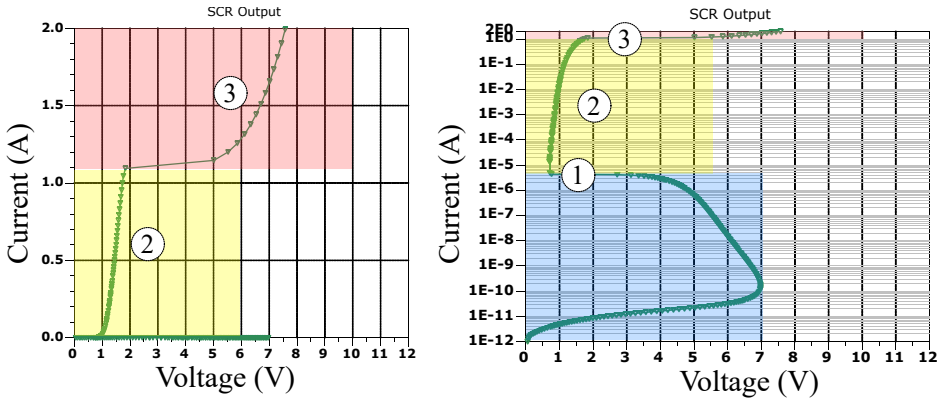



**Figure 4.13:** Simulated IV characteristics of a Shockley diode in a linear- (left) and logarithmic (right) scale. The blue region shows the device before latching (1). Yellow is the forward operation of the SCR (2). Red is the de-latching operation (3).

collapse and can be used to simulate de-latching. The roll-off is proportional to $I_c^{-1}$ [104] and leads to a current gain decrease in the BJTs. The value of $I_{kf}$ has not been extracted from silicon samples because the internal BJTs were not accessible due to missing test structures.

Figure 4.15 shows the individual gain of each transistor[1] and the gain product. The latching condition for a single shunted configuration according to Equation 4.5 is indicated by the red dashed line. It tends to unity for currents above 1 A. Comparing the PNP and NPN gain to the floating condition discussed before, the PNP gain is similar while the NPN gain is clearly different. This is explained by $R_{BE}$ and its shunting function which prevents any base-current into the NPN. The gain product approaches the latching condition after the NPN base-emitter starts to be forward biased due to voltage drop at $R_{BE}$. The gain product is matching the latching condition at about $1 \cdot 10^{-2}$ A. Again, the PNP transistors goes in saturation and reduces gain (valley between $1 \cdot 10^{-5}$ A and $1 \cdot 10^{-3}$ A). Finally, the SCR shows a gain collapse (3) at 1 A. This simulation results with the equivalent circuit of a SCR are able to illustrate the validity of the latching condition in floating and single shunted SCRs by calculating the gain product during forward operation. The saturation of the internal BJTs can be partially shown with the limitation of having to standalone BJTs and only one transistor in saturation. Nevertheless, the shown

[1] BJTM1=NPN, BJTM2=PNP

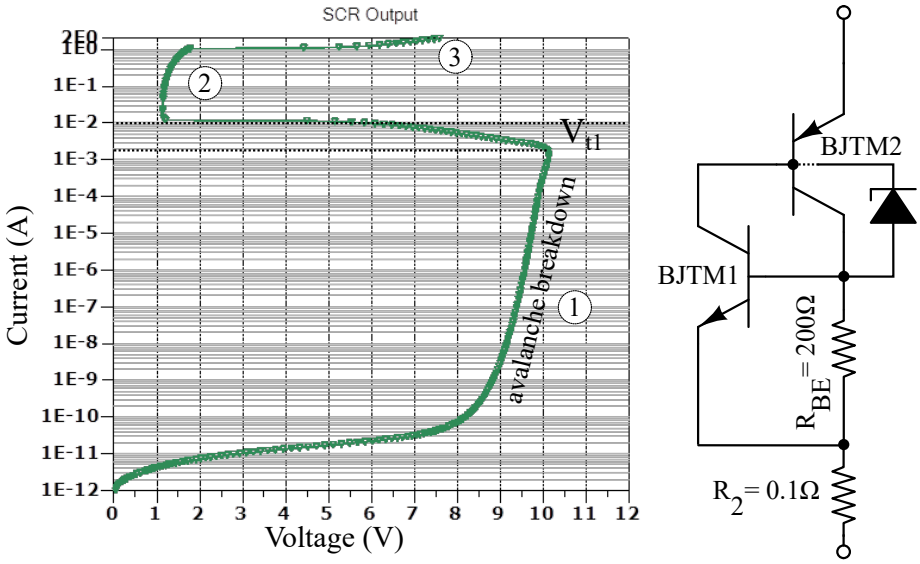



**Figure 4.14:** Simulated current-voltage characteristic of interleaved bipolar junction transistors forming an SCR. The internal avalanche current triggers the device (1) into latching condition (2) with a low forward voltage before de-latching (3) is observed. An avalanche current source (diode symbol) was used to model avalanche breakdown in the BJTs. $R_2$ is used to fit the device resistance at high currents.

results are suitable to explain the de-latching. A qualitative simulation of devices required proper parameter extraction with test structures and feedback into the SGP model. The presented equivalent circuit with base-emitter shunt explains the results of the measured silicon SCR devices in this work which showed a de-latching. It confirms the hypothesis of the gain product collapse that leads to de-latching.

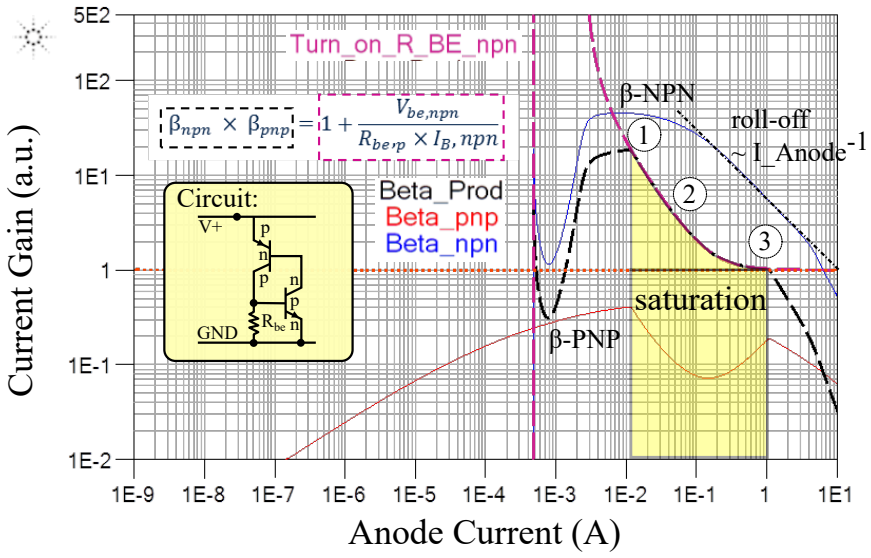



**Figure 4.15:** Simulated common-emitter amplifications of coupled bipolar junction transistors. The internal gain product (black line dashed) and the latching condition (red line dashed) according to Equation 4.5are shown. The SCR is operating in the latched state between (1) and (3). The NPN has a base-emitter shunt included to control the switching of the SCR.

## 4.4 Device Simulations of Vertical SCRs

The gain of the internal vertical transistor structures is determined by the base width and doping concentrations of base and emitter regions. Both parameters are defined by process technology (e.g. doping and thickness of epitaxial layers).

Here, device simulations are carried out to extract necessary changes in the process technology to prevent the SCR from de-latching by increasing the internal gain of the bipolar structures.

One-dimensional device simulations are sufficient to yield qualitative results by assuming that the vertical 2D structure has a homogeneous current density distribution. This assumption is justified because the lateral expansion is several times larger than the vertical dimension.

The lateral current density is negligible during device operation (compare Section 3.2.6). The simulation setup and models are described in Section 3.2.

The SCR has been created by a process simulation to increase accuracy of the simulation results. The comparison of the process simulation doping profile versus the SIMS profile of the real structure is shown in Figure 4.16.

### 4.4.1 npn-structure

First, the gain is optimized by adjusting the base and emitter doping concentration of the internal transistor structures. Here, the emitter doping of the npn-transistor is determined by the doping of the substrate material (24 µΩm to 26 µΩm) and the emitter doping of the pnp-transistor is determined by the p-contact implantation ($5 \cdot 10^{15}\,\mathrm{cm}^{-2}$). The lowly doped n-base concentration is minimized to achieve the lowest possible junction capacitance per junction area (e.g. $< 1 \cdot 10^{13}\,\mathrm{cm}^{-3}$).

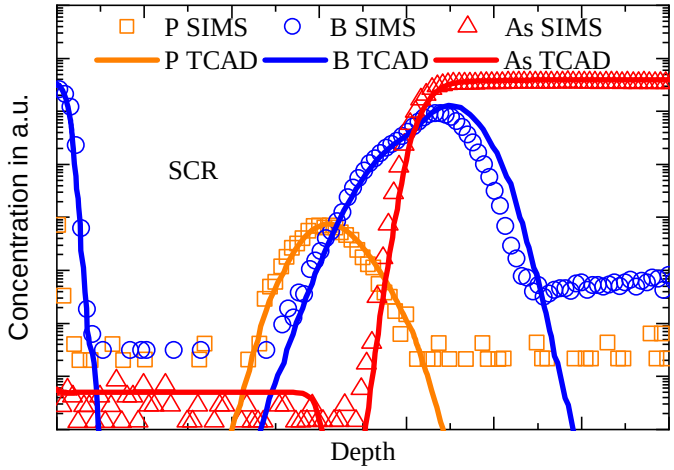
The implantation dose of the n-base buried layer and the p-base buried layer are the only available parameters for optimization and discussed in the following.

Figure 4.17 shows the DC simulation results for different p-base implantation doses in the range of $1 \cdot 10^{15}\,\mathrm{cm}^{-2}$ to $7 \cdot 10^{15}\,\mathrm{cm}^{-2}$ by $2 \cdot 10^{15}\,\mathrm{cm}^{-2}$. The n-base dose was constant at $2 \cdot 10^{14}\,\mathrm{cm}^{-2}$. The high boron doses are required to reduce the sheet resistance of the buried layer because of the trigger current (see Section 3.1.4). Figure 4.18 shows the internal current gain and the gain product for DC simulations. The npn has lower gain values compared to the pnp due to the high base doping. This cannot be compensated by the pnp and the gain product is dominated by the npn.

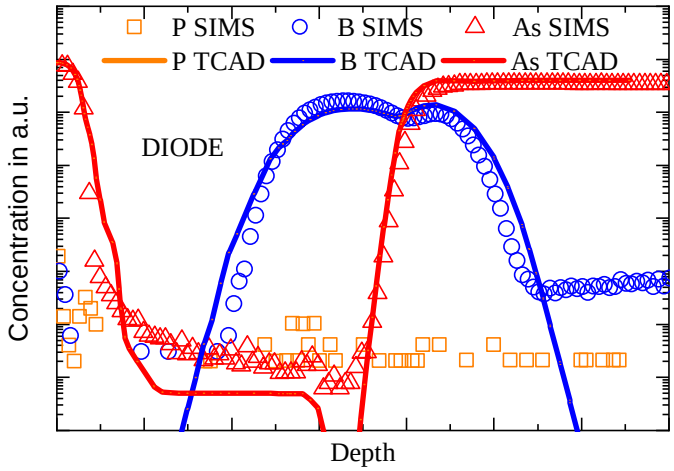
The gain of the internal npn-structure decreases for increased boron dose and leads to a lower gain until the latching condition cannot be fulfilled. For the boron dose of $1 \cdot 10^{15}\,\mathrm{cm}^{-2}$ the latched operation is limited to the current range of $1 \cdot 10^{-1}\,\mathrm{A\,cm}^{-2}$ to $1 \cdot 10^{5}\,\mathrm{A\,cm}^{-2}$ while higher doses operate in avalanche breakdown [5], [51].

This effect is known for pnpn-structures and called high-voltage SCR operation and commonly used for high-voltage applications where latch-up is critical [55], [3].

The results shown in Figure 4.17(a) confirm the data found in high holding voltage SCRs publications referring to pnpn-structures operating at increased holding voltages [67], [69], [31] and described by layout parameters that are influencing the internal gain.




(a)




(b)

**Figure 4.16:** Comparison of simulated doping profile versus SIMS analysis. The doping profile of the process simulation matches with the SIMS profile. a) shows the results for the vertical SCR and b) shows the parallel diode structure.

The logarithmic plot in Figure 4.19(b) and the extracted gain values in Figure 4.18 show the root cause for the increased holding voltage in the SCR. The four layer

structure cannot operate in the latched state because the gain product is too low. Instead, the device operates in avalanche breakdown which is known from pnp- and npn-ESD devices [5].

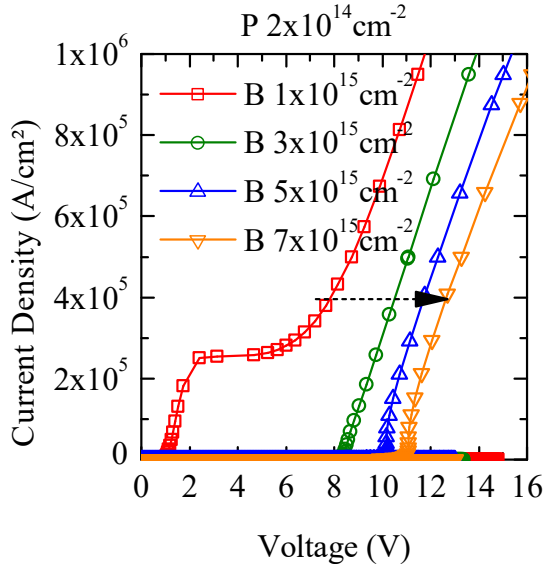
*Q. Cui et al.* and *C. Huang et al.* presented decreased ESD failure currents $I_{t2}$ in high holding voltage SCRs and confirmed the higher power dissipation in the reverse biased junction during avalanche breakdown in four layer structures.

### 4.4.2 pnp-structure

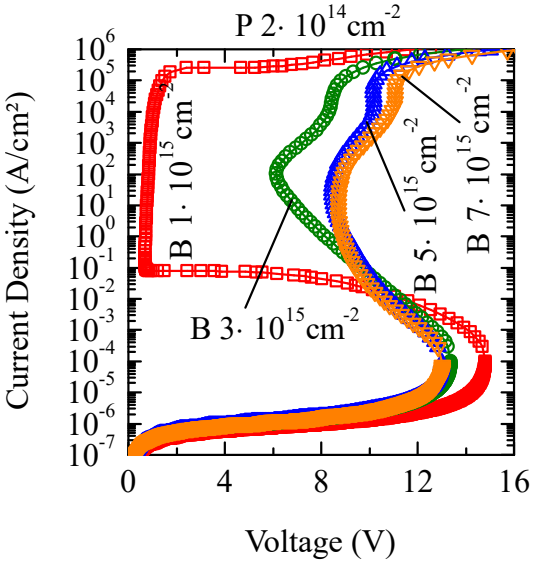
For the pnp-structure the phosphorus implantation dose of the n-base buried layer was varied and simulated. Again DC results and internal gain were extracted to analyze the impact of the pnp gain on the four layer gain product.

Figure 4.19 shows the DC simulation results for different n-base implantation doses in the range of $2 \cdot 10^{15}\,\mathrm{cm}^{-2}$ to $5 \cdot 10^{15}\,\mathrm{cm}^{-2}$ by $2 \cdot 10^{15}\,\mathrm{cm}^{-2}$. The p-base dose from the previous results was used with $1 \cdot 10^{15}\,\mathrm{cm}^{-2}$.

In Figure 4.20 the internal current gain and the gain product are shown. The npn gain is several times higher compared to the pnp. The gain product can fulfill the latching condition for all phosphorus doses. The breakdown voltage is decreasing for higher phosphorus doses and the resistance during forward conduction decreases due to lower sheet resistance (see Figure 4.19(a)). The n-base layer is less critical in the proposed vertical SCR and can be used to adjust the gain product of the four layer device.




(a)




(b)

**Figure 4.17:** Simulated DC-IV characteristics of SCRs for variation of p-buried layer boron implantation. The increased boron dose prevents the SCR from latching into its low forward voltage operation state.

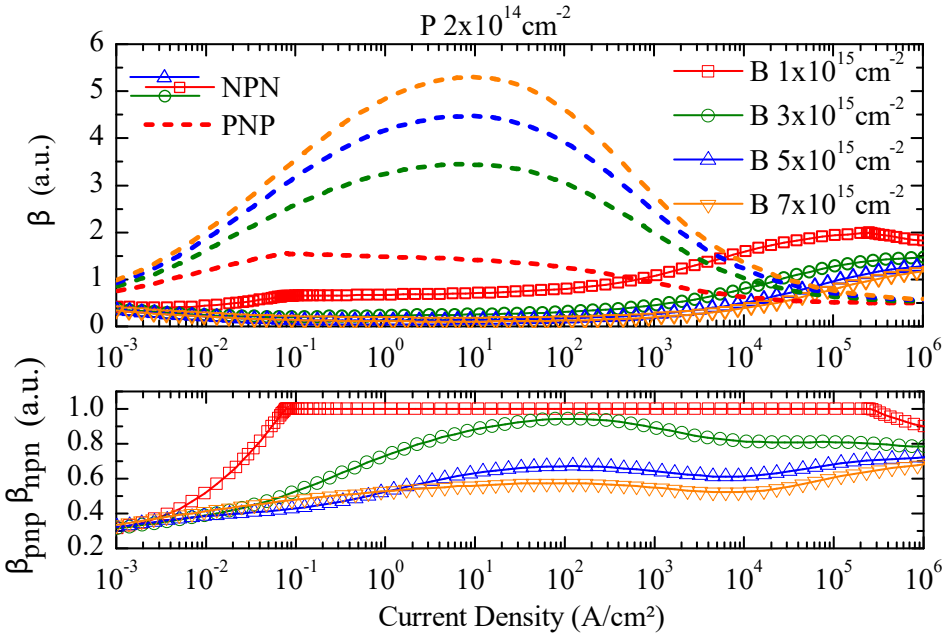
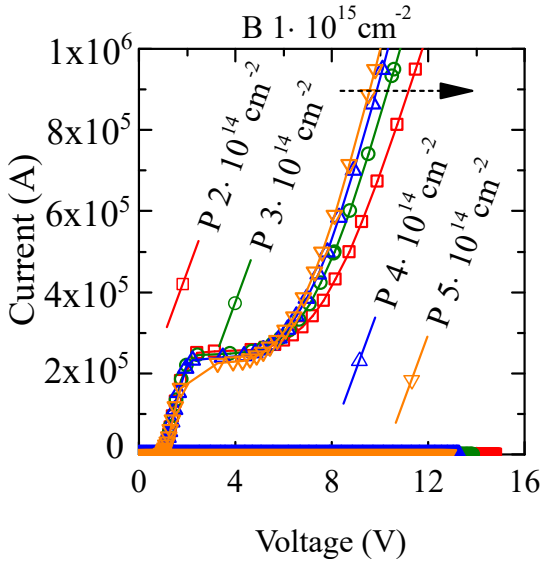
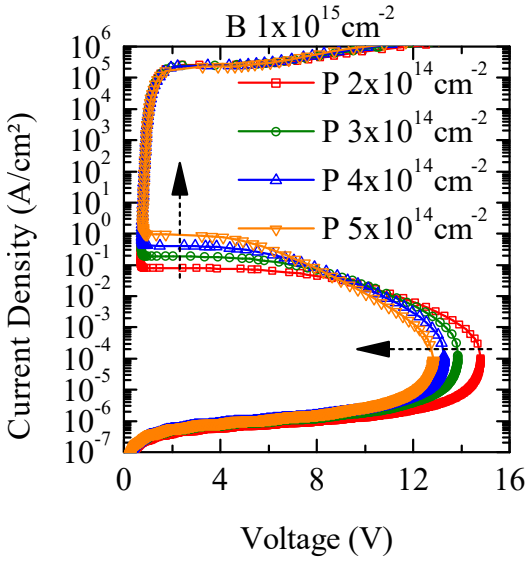



**Figure 4.18:** Extracted gain values and gain product of internal transistors in a SCR by device simulations. The dose for the n-base doping is fixed at $2 \cdot 10^{14}$ cm$^{-2}$ while the n-base dose is varied from $1 \cdot 10^{15}$ cm$^{-2}$ to $7 \cdot 10^{15}$ cm$^{-2}$.




(a)




(b)

**Figure 4.19:** Simulated DC-IV characteristics of SCRs for variation of n-buried layer phosphorus implantation. The increased phosphorus dose prevents the SCR from latching into its low forward voltage operation state.

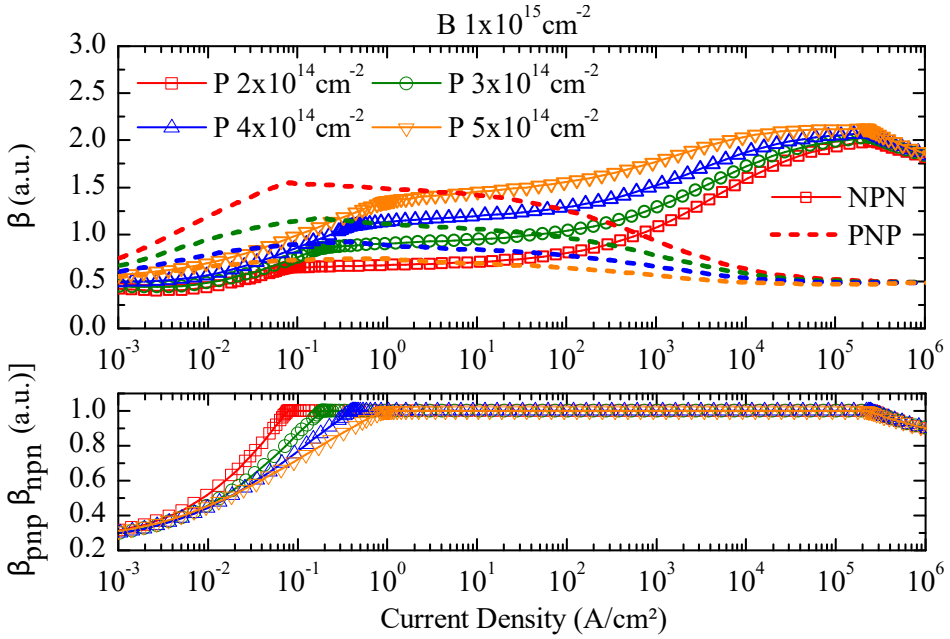



**Figure 4.20:** Extracted gain values and gain product of internal transistors in a SCR by device simulations. Dose for the p-base doping is fixed to $1 \cdot 10^{15}\,\mathrm{cm}^{-2}$ while the n-base dose is varied from $2 \cdot 10^{14}\,\mathrm{cm}^{-2}$ to $5 \cdot 10^{14}\,\mathrm{cm}^{-2}$.

## 4.5 Doping Profile Optimization of Vertical SCRs

The results from the simulated gain product in pnpn-structures were verified by silicon samples and characterized with high current TLP measurements. The p-base implantation dose of $3 \cdot 10^{15}\,\mathrm{cm}^{-2}$, $5 \cdot 10^{15}\,\mathrm{cm}^{-2}$ and $7 \cdot 10^{15}\,\mathrm{cm}^{-2}$ was used similar to the simulated structures because it has the highest impact on the gain product and clearly showed a strong change in operation voltage.

Figure 4.21 shows the pulsed high current IV characteristic with additional leakage current plots of the silicon pnpn-devices. A de-latching is observed for increased boron doses that is identified by increased forward voltage. The characteristic is similar to the DC simulations shown in Figure 4.17(a). The de-latching characteristic is smoother in the real structure compared to the simulated structure because the measured IV is based on an averaged voltage in a time range between 30 ns to 60 ns while the simulations results are static DC values.

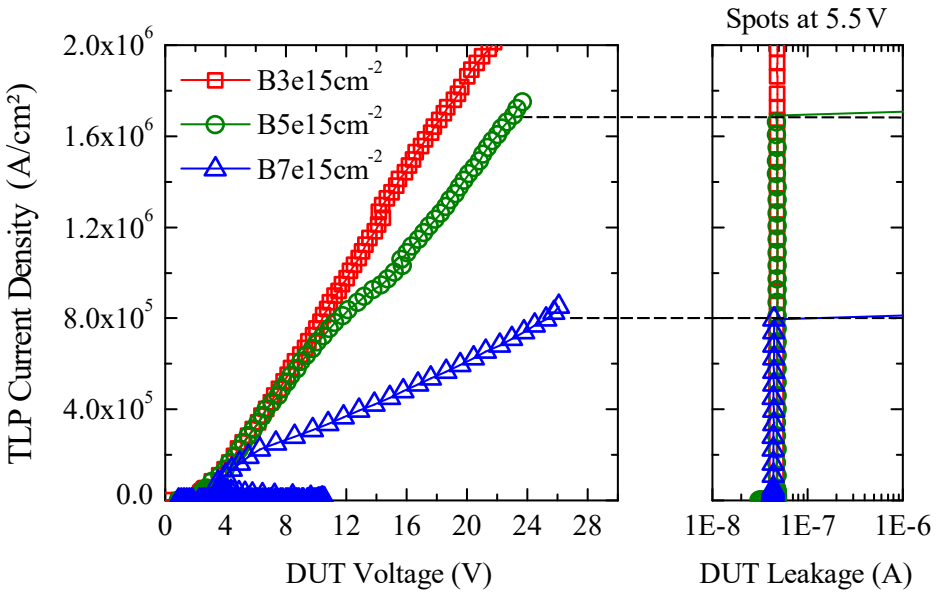



**Figure 4.21:** Measured TLP IV characteristics of bidirectional ESD pnpn-structures. The p-base dose was varied to influence the gain of the internal npn. De-latching occurs for higher boron doses.

Additionally, the robustness of the devices is reduced after de-latching which is indicated by the increase in leakage current. The highest p-base dose starts to de-latch at about $1 \cdot 10^5$ Acm$^{-2}$ and increases the forward voltage significantly until the device fails at $8 \cdot 10^5$ Acm$^{-2}$. The corresponding power dissipation is the highest for the three devices but it is only half of the device with $5 \cdot 10^{15}$ cm$^{-2}$ p-base dose (similar voltage but doubled current density). The device with a p-base dose of $5 \cdot 10^{15}$ cm$^{-2}$ shows no de-latching and no failure during the shown current range.

The n-base dose shows no difference as predicted by the device simulations because the p-base is dominating the current gain.

It has to be mentioned that the measured results differ from the simulations. The reason is the missing calibration of the simulator models for high currents. During simulations the de-latching occurred earlier and p-base doses higher than $1 \cdot 10^{15}$ cm$^{-2}$ already operated in avalanche breakdown.

The reduced p-base doping combined with reduced n-base doping show a vertical pnpn-structure with a breakdown voltage at 10 V without de-latching.

# 5 Summary and Outlook

Electrostatic discharge protection is an important topic for electronics manufacturers, be it in the area of consumer, industrial or automotive products. ESD protection is highly system dependent and insufficient ESD protection can lead to significant delays or even failures in product qualification. Due to the continuous shrinking of technology nodes and gate oxides ICs exhibit a lower ESD robustness. Often the integrated on-chip ESD protection is not capable of protecting efficiently against system level ESD events without excessive and expensive chip area [3]. Discrete ESD protection devices based on cost-effective silicon technologies can solve this issue and achieve up to 30 kV ESD robustness with a 0.3 x 0.6 $mm^2$ footprint [52]. Moreover, state-of-the-art discrete protection devices offer lowest capacitance per kV IEC61000-4-2 robustness [36], making them ideal for high data-rate applications (e.g. USB3.2) and their low parasitic capacitance requirements derived from signal integrity.

As detailed in this work, two bipolar-based device concepts are suitable for discrete ESD protection devices:

- NiPN or PiNP bipolar transistor structures in combination with p-i-n diodes. These devices utilize a snapback to reduce the clamping voltage. The holding voltage is controlled by design and hence latch-up can be avoided.
- Four layer pnpn-structures, e.g. a SCR in combination with p-i-n diodes. These devices utilize a deep snapback to less than 2V and offer lower clamping voltages compared to the before mentioned bipolar structures. This is of interest for applications which are very sensitive to ESD events like USB3.2 and Thunderbolt.

SCR devices are available as vertical [75] or lateral structures [36]. Both concepts reference the main direction of current flow in a surface pn-junction, either lateral over the junction sidewalls or vertical thru the junction bottom. Both concepts have advantages as well as disadvantages with respect to device parameters. Lateral concepts feature the shortest possible current path due to narrow, well controlled neighboring surface implantations. This reduces the device resistance and the clamping voltage.

Unfortunately, those devices are limited in their effective lateral device area and, thus, their ESD robustness (< 20 kV). Vertical device concepts, on the other hand, exhibit a higher ESD robustness for the same device area and capacitance (> 20 kV) due to the full bottom junction carrying the ESD current. Yet, connecting the vertical devices (e.g. substrate connection) introduces a non-negligible parasitic series resistance. The novel SCR devices presented in this thesis are based on a vertical concept because the target was to develop a passivated and packaged chip with smallest active area and high ESD robustness of at least 20 kV.

First, an understanding of the pnpn-structure has been accomplished by literature reviews as well as extensive device and technology process experiments, both by means of simulations and real silicon. Based on the experimental results the ESD protection performance of a newly designed SCR was optimized, leading to a robustness > 20 kV and a capacitance of < 0.3 pF. Yet, breakdown voltages lower than 10 V could not be realized due to limitations in the available temperature budget during device manufacturing. It was also shown, that high doping concentrations in the base regions of the pnpn lead to a de-latching of the device, forcing the device into avalanche operation with significantly worsened ESD protection performance.

Second, the de-latching of the SCR was investigated further. For the first time, this work showed that de-latching is related to the $\beta$-roll off at high current densities. Both experiments and device simulations confirmed the low current gain in the base regions of the pnpn as root cause. This can be avoided by increasing the internal gain-product by means of technology optimization (e.g. base doping engineering). Moreover, the impact of de-latching on pnpn-based ESD protection devices has been described in this work for the first time.

Third, both the device design (e.g. layout) and manufacturing processes (e.g. implantation) were further optimized. Experiments revealed a weakness in the vertical SCR's trigger mechanism by breakover of the buried junction. The inherently vertical manufacturing processes in combination with the device design could not fulfill the combined requirements for breakdown voltage, current gain, turn-on time and voltage overshoot as those cannot be adjusted independent of each other. In order to overcome this challenge a novel lateral trigger device, the lateral triggered vertical thyristor (LTVT), has been invented and patented. The LTVT was optimized by decreasing the internal transit time without changing the parameters of the vertical SCR device. This enabled the independent optimization of the breakdown voltage and the transient voltage overshoot without sacrificing the ESD protection performance. Experimental data confirmed that the LTVT concept reduces the breakdown

and trigger voltage to less than 10 V in combination with a lower overshoot voltage during turn-on compared to the concept without lateral trigger.

In addition, a unique pn-junction-short concept has been developed and patented. The latter serves as a low ohmic connection to buried silicon layers, including:

- the connection of a deep buried layer that is also a base region of the pnpn
- the connection of the lateral trigger device, located at the surface, to the substrate
- forming a junction isolation to the floating base region of the vertical pnpn structures which form the main ESD device
- bypassing a blocking pn-junction by means of an electrical short

From a technology point of view the unique pn-junction-short concept had to be combined with a sidewall doping process. This prevented Schottky diode behavior and realized an ohmic connection to a deep boron layer. The presented pn-junction short is a novelty and its resistivity is superior to a sinker by at least a factor of two.

In summary, within this work a novel SCR protection device utilizing the LTVT concept was developed and integrated into an existing production technology. The developed device is currently in mass production and patents have been granted to the author of this work. Furthermore, for the first time this work described the root cause of pnpn de-latching and how to solve it. The resulting device concept enables low-voltage (3.3 V and 5 V) applications by including a trigger device and mid-voltage (18 V) RF protection by omitting the trigger device.

## 5.1 Further research topics

Research topics in the field of ESD protection concepts and devices are mainly driven by new technologies (e.g. III-V semiconductors) and advancements in CMOS nodes. Thus, the demand for new protection concepts and better devices with respect to faster switching and lower clamping voltages is growing constantly. Based on the findings of this work a recommendation for two focus topics will be given.

### 5.1.1 Device Concepts

- New device concepts are needed for lower working voltages as well as for high voltages like antenna protection.
- Area efficient and cheap device technologies will be the focus for external protection devices. Focusing on decreasing production costs while maintaining or even improving ESD performance is a key for success.
- Complex structures like SCRs have superior ESD performance per area but require a complex multi-layer technology. Reducing the complexity in process technology is mandatory to reduce costs.
- SCR have to be triggered fast at different voltages. The presented LTVT device covers breakdown voltages down to 7 V which is sufficient for today's 3.3 V and 5 V working voltages but next generation applications require even lower trigger voltages. Different trigger mechanisms which are fast and deliver sufficient trigger current have to be investigated and implemented.
- The trend of reducing device capacitance values to 100 fF and less while maintaining ESD robustness of > 15 kV IEC61000-4-2 will soon have an end by reaching the physical limit for silicon. A solution to overcome this limit may be compound silicon devices.

### 5.1.2 Modeling

- Modeling of SCR structures is becoming more important due to the increasing number of SCR protection structures used in modern designs. Different equivalent circuits and behavioral models have been proposed but lack the speed and ease of use of dedicated compact models. Any development and standardization in this field would be of great help for the industry.
- Voltage overshoots due to diode forward-recovery and additional transient effects in the semiconductor are playing a major role in low capacitance devices. A dedicated model covering transient effects for use with ESD simulations would help significantly with ESD- and co-design.

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