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Complementary Tunneling-FETs (CTFET) in CMOS Technology

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to my wife Jing Zhao

Abstract

The short channel effects (SCE) are becoming serious problems as the metal oxide semiconductor field effect transistor (MOSFET) scales down to the deep sub-micron dimension. Recently, a silicon tunneling transistor called TFET was proposed as the candidate of MOSFET. This transistor realizes the gate-controlled tunneling at room temperature. As a novel device, there are still many unknowns and challenges in the physics, fabrication, and application of TFETs. In this work, the device and process simulations are carried out to investigate physical principle, optimized fabrication conditions, and future structure of TFETs. Starting from the simulation results, the necessary technologies are improved for the fabrication of high performance TFET.

Proved by both simulation and experimental measurement, the working principle of TFET is the gate-controlled band-to-band tunneling. Compared to MOSFET, TFET has several advantages: 1) Suitable for low power application because of the lower leakage current (due to the higher barrier of the reversed p-i-n junction in TFET). 2) The active region (band-to-band tunneling region) is about 10nm in TFET. Simulation shows that this transistor can be shrunk down to at least 20nm gate length. 3) The subthreshold swing of TFET is not limited by 60mV/dec because of its distinct working principle. 4) The tunneling effect and the ballistic electron transport in TFET can enhance the operating speed of TFET. 5) Since the threshold voltage of TFET depends on the band bending in the small tunnel region, but not in the whole channel region, V_t roll-off is much smaller than that of MOSFET while scaling. 6) The channel region can be intrinsic silicon which suppresses the V_t fluctuation caused by dopant atoms random distribution. 7) Because of the reverse biased p-i-n structure, there is no punch-through effect in TFET.

It is summarized from the simulation results that high performance TFET needs thin gate oxide (but relaxed compared to MOSFET), abrupt doping profile, and heavy source doping concentration. If both source and drain are heavily doped, one TFET has both n-channel TFET (NTFET) and p-channel TFET (PTFET) characteristics. By enhancing or suppressing the NTFET and PTFET characteristics inside of one TFET, the complementary TFET can be realized. From our investigation, it is found that the p^+ doping concentration of NTFET should be higher, but the n^+ doping level should be relatively lower. In order to fabricate PTFET, the n^+ doping concentration should be higher, but the p^+ doping level should be relatively lower.

According to simulation results, the technologies are developed for TFET fabrication. The Reactive Ion Etching (RIE) technology, the heavy boron doping diffusion and the Rapid Thermal Diffusion (RTD) technology are developed in this work. The heavy n-type diffusion and the gate dry oxidation process are also calibrated. The RIE technology is applied in the fabrication of the vertical TFET, the vertical mesa diode, the self-aligned gate, and the shallow trench isolation (STI) for device separation. The n and p type diffusion of spin-on-dopant (SOD) is also investigated. For the n^+ doping, the surface concentration of 2×10^{20} cm^{-3} can be achieved. For the p^+ doping, the active surface concentration of boron is about 2.8×10^{20} cm^{-3}. The patterning of SOD P507 is studied in order to form the distinctive doping profile. The patterning and thickness control of SOD P507 makes the self-aligned TFET fabrication process possible. In addition, SOD B150 is calibrated to form the p-well which enables the fabrication of the Complementary TFET (CTFET) on the single n^- doped wafer. Thin gate oxide fabricated in the normal thermal oxidation oven is studied. Stable 5nm and 6 nm oxide is fabricated at 950°C and 900°C by dry oxidation. Finally, the Rapid Thermal Processing (RTP) technology is developed and calibrated in this work. The RT-Diffusion can form the ultra-shallow junction. In the planar TFET fabrication, the RTD is applied to form the n^+ and the p^+ regions by the diffusion of SOD.

With these improved technologies, two types of TFETs - PTFET and NTFET- are realized on the same silicon substrate. The room temperature gate-controlled tunneling is realized in the silicon device. Very low leakage current in both NTFET and PTFET is found. The realization of NTFET and PTFET also make it possible to fabricate the CTFET circuits. According to the measurement results of TFET, many physical characteristics, such as drain current saturation, the punch-through, impact ionization and avalanche, ballistic electron transport, and gate-controlled tunneling will be discussed.

Finally, the applications of TFET are investigated. When the channel length is decreased below 20nm, TFET will be a hot electron device. That makes TFET suitable for microwave application because of the short electron transit time through the channel region. Due to the low leakage current, TFET can be used in the low power circuits. TFET can also configure the edge detector in the logic circuit using very simple TFET circuit, if the threshold voltage is well adjusted. Because of the similar characteristics to CMOS, CTFET is capable to configure many CMOS-like circuits. In this work, the CTFET inverter characteristics are derived from the CTFET characteristics. The switching of this CTFET inverter is faster and the noise margin is larger than the CMOS inverter. The reason is that TFET has a better saturation behaviour and also an earlier saturation than the conventional MOSFET. The CTFET inverter also has a smaller short circuit leakage current than the CMOS inverter. For this reason, the 6-transistor static RAM with the low stand-by power consumption can be configured using CTFET.

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Chapter 1

Introduction

The dimension of MOSFET keeps being scaled down to achieve the low power, high speed, and high density circuits. According to the ITRS roadmap 2002, the gate length of MOSFET will be scaled down to 25 nm by 2010. The channel doping level of 5×10^{18} cm^{-3} is needed to suppress the short channel effect. As a result, the gate dielectric with 1.2 nm electrical Equivalent Oxide Thickness (EOT) is needed to switch on the MOSFET with such a heavily doped channel [1-4]. However, the thin gate oxide results in the reliability problems for the tunneling through oxide [5, 6]. There is still no solution to fabricate the reliable thin gate dielectric of 1.2nm electrical EOT [7, 8]. Another problem is that the atomic doping fluctuation will be significant, when the gate length of MOSFET decreases to 50nm. Due to the atomic doping fluctuation, the threshold voltage will fluctuate accordingly. In addition, with the increasing channel doping concentration and electric field in MOSFET, the Zener tunneling current at the drain-channel junction will result in an increasing leakage current [9]. As mentioned in the roadmap, the nominal subthreshold leakage current of the 32nm Low Operating Power (LOP) NMOS at 25° C will be 3000pA/μm. Recently the double gate thin body MOSFET is proposed to solve these problems. In the proposed double gate MOSFET, the light channel doping is used to overcome the problem of threshold voltage fluctuation and the thin silicon body can shrink the leakage current. However, the leakage current through the thin gate dielectric and the gate induced drain leakage (GIDL) due to the band-to-band tunneling in such a transistor can not be avoided.

As the device dimension further scales, the semiconductor devices are entering into a tunneling epoch. For MOSFET, various tunneling leakage mechanisms, such as the band-to-band tunneling current at the drain-channel junction (GIDL), the gate tunneling leakage current through the ultra-thin gate dielectric and even the direct tunneling from source to drain are increasing with the shrinking dimension in this tunneling epoch [10]. It seems that quantum transistors may be a good solution because the quantum tunneling transistors have a smaller dimension, such as single electron transistor, and a higher operating speed [11, 12]. Up to now, most of the tunneling transistors were fabricated in the compound semiconductor materials. However, for mass production and the compatibility with the conventional digital circuits, the silicon-based tunneling transistors are preferred. Recently, a MOS-based tunneling transistor in silicon called Esaki tunneling FET (ETFET or TFET) was proposed [13-17]. TFET is a 3-terminal device built in silicon. The gate-controlled band-to-band tunneling is the working principle of this transistor.

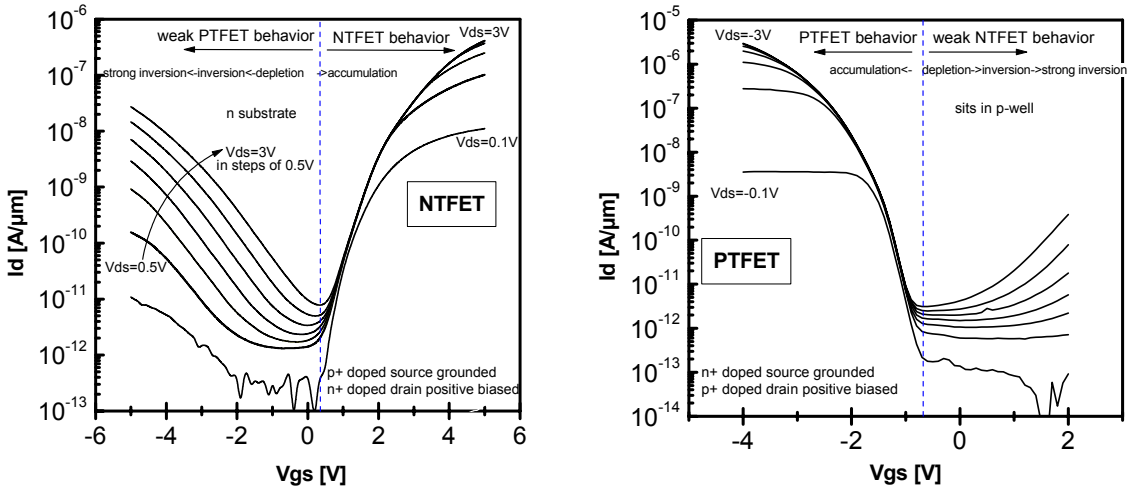
Compared to MOSFET, TFET should have several advantages: i) Suitable for the low power application because of the lower leakage current (due to the higher barrier of the reversed p-i-n junction in TFET). ii) The active region (band-to-band tunneling region) is about 10nm in TFET. Simulations show that this transistor can be shrunk down to at least 20nm gate length. iii) The good performance can be achieved with 3nm gate oxide, which relaxes the need of high-k dielectrics. iv) The tunneling effect and the velocity overshoot may enhance the device operating speed of the device. v) Much smaller V_t roll-off while scaling. The reason is that the threshold voltage of TFET depends on the band bending in the small tunnel region, but not in the whole channel region. vi) The channel region can be intrinsic silicon which suppress the V_t fluctuation caused by dopant atoms random distribution. The disadvantages of this transistor are: i) The drive current is relatively low because the tunneling region is quite small compared to the silicon body. ii) The sharp doping profile is needed for the high performance transistor. iii) The high n / p doping concentration is very important for the fabrication of high performance TFET.

In this work, the simulation and fabrication of TFET will be investigated.

1.1 TFET working principle and definition

As a novel semiconductor device, the working principle and the definition of TFET are important for future improvements and applications.

Fig. 1-1 shows the transfer characteristics of the NMOS-like TFET and the PMOS-like TFET fabricated in this work. In Fig. 1-1.a, the drain current increases with the increasing gate voltage at the right side of the blue line. TFET is switched on when $V_{gs} > V_t$. This type of TFET is named as NTFET. On the contrary, in Fig. 1-1.b, the drain current increases with the decreasing gate voltage at the left side of the blue line. TFET is switched on when $V_{gs} < V_t$. This type of TFET is named as PTFET.



a b

Fig. 1-1 Experimental transfer characteristics of NTFET (a) and PTFET (b)

The schematic models for NTFET and PTFET are shown in Fig. 1-2. The p-i-n diode is always reverse biased obtain the ultra low leakage current. For NTFET, the substrate is lightly n doped. The increasing gate voltage will result in the accumulated n channel. The surface tunnel junction is at the cross point of GOX/channel/p^+ doped region (Fig. 1-2, left). The corresponding energy band diagram is shown in Fig. 1-3. The electrons tunnel from the p^+ doped region into the channel region and flow to the n^+ doped region. In PMOS and NMOS, the source is defined as source of main carriers. In this work we use the similar definition for the electrodes of TFET. Therefore, in NTFET, the p^+ doped region is named as source (source of electrons) and the n^+ doped region is named as drain (drain of electrons). The NTFET is switched on when $V_{gs} > V_t$. If a negative gate voltage is applied, an inversion layer will be formed and the tunnel junction will move to the cross point of GOX/channel/n^+ doped region. The transistor behaves as a PTFET, which in this measurement setup is connected in a "source-follower" configuration. For PTFET, the substrate is lightly p doped. An accumulated hole channel can be formed with the negative gate voltage. The surface tunnel junction is at the cross point of GOX/channel/n^+ doped region (Fig. 1-2 right). The electrons tunnel from the p^+ channel region to the n^+ doped region and the generated holes in the channel flow to the p^+ doped region. Therefore, in this case the p^+ doped region is named as drain (drain of holes) and the n^+ doped region is called as source (the tunnel junction of channel/n^+ doped region is the source of holes in fact). The weak NTFET behavior can also be observed here when the positive gate voltage increases. The symbols of NTFET and PTFET for circuit design are also shown in Fig. 1-2.

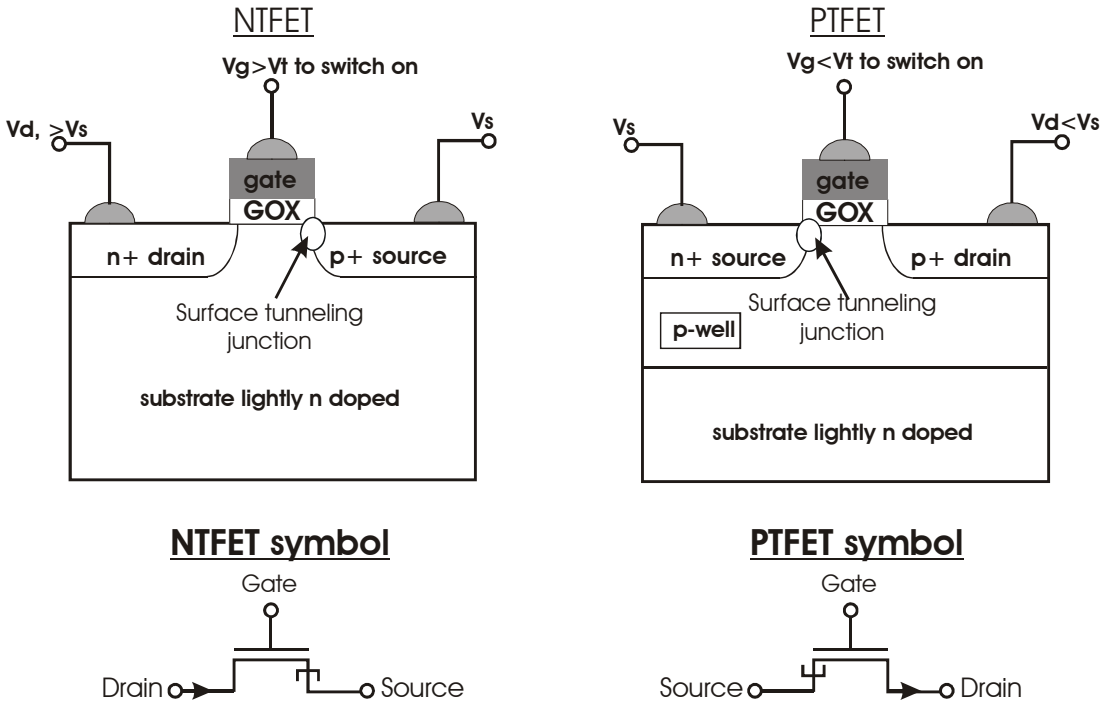


Fig. 1-2 Basic TFETs structural models and the electrodes definition of TFET

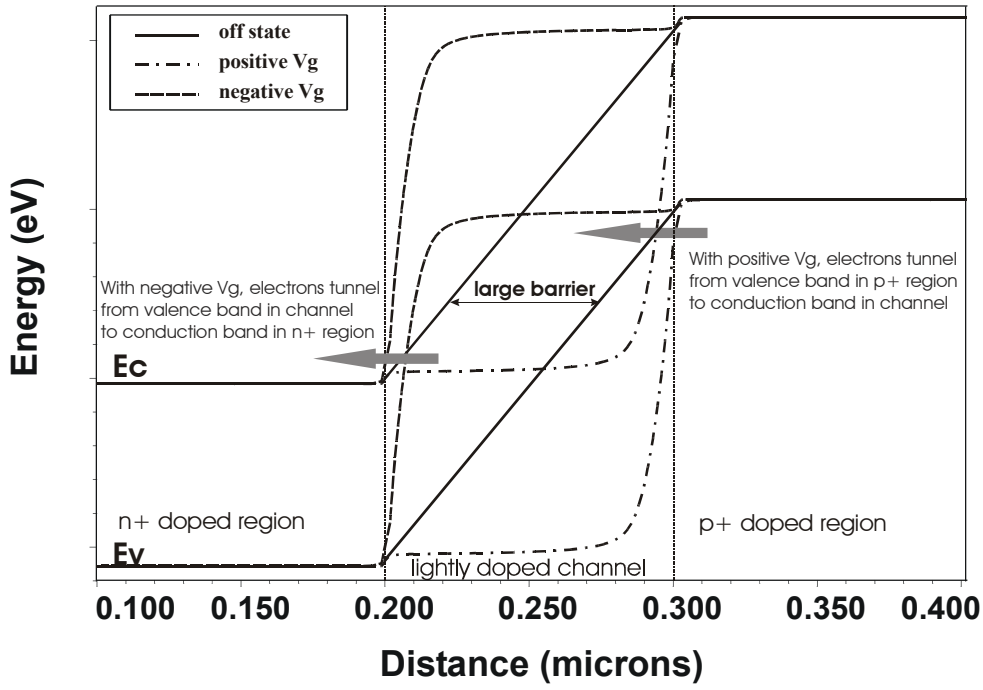


Fig. 1-3 MEDICI simulated band diagram of the on-state TFET (V_{ds}=1V, V_{gs}> V_t)

1.2 Simulation tools for TFET investigation

The numerical simulations are becoming more and more important in modern scientific research work. Using the simulation tools, the result can be approximately predicted in a relatively short time. It can provide useful information for the experiment. In this work, we use MEDICI and SUPREM for 2-dimensional TFET simulation. The TFET working principles and the structural optimization will be simulated. For 3-dimensional simulation, the Taurus device and process simulator are used.

The flow chart of the 2-Dimensional MEDICI and SUPREM simulation is shown in Fig. 1-4. In the SUPREM simulation, the mesh, material, region, and doping profile of the starting material (substrate) must be defined at the beginning. The processes can be simulated by executing the statements such as deposition, diffusion, implantation, and etching. The parameters which define the experimental conditions are included in these statements. For example, to deposit a 200nm SiO_2 layer at the temperature of 800°C, the statement for the simulation is:

```
DEPOSIT    MAT=OXIDE    THICKNESS=0.2    TEMP=800
```

During the deposition, the diffusion of dopant will be calculated and the mesh will be refined. After the whole simulation, the files, in which the structural and physical information is stored, can be created for the later use. The final structure resulted from the SUPREM simulation can be imported into the MEDICI simulator to calculate the device electrical performance. As illustrated in Fig. 1-4, the device can also be defined by MEDICI directly without any process simulation. In this case, the mesh, the region, the material, the electrode, and the doping profile should be defined. In order to get a fine mesh, the re-grid command can

be used to refine the grid on the doping concentration or other optional electrical parameters. The mathematical and physical models for the numerical calculation should be chosen to calculate the electrical properties. After the whole MEDICI simulation is finished, the physical information can be stored as the "tif" (technological information format) file. The syntax of MEDICI and SUPREM is similar. Three-dimensional simulation can also be done by the Taurus Process and Device simulator. Although more information is provided in 3-D simulation, 3-D simulation occupies much more computing resource than the 2-D simulation. For instance, a 2-D SUPREM simulation takes about 20 minutes, but the similar 3-D Taurus simulation may take 2 days. Therefore, most of the simulations in this work are done by 2-D simulation. The 3-D simulations are used for the final correction of experimental parameters. The Taurus visual tools can display the structures obtained from the MEDICI SUPREM and Taurus simulation. As an example, Fig. 1-5 shows a 3-D structure in the window of Taurus Visual. More information on the simulation can be found in appendix A.

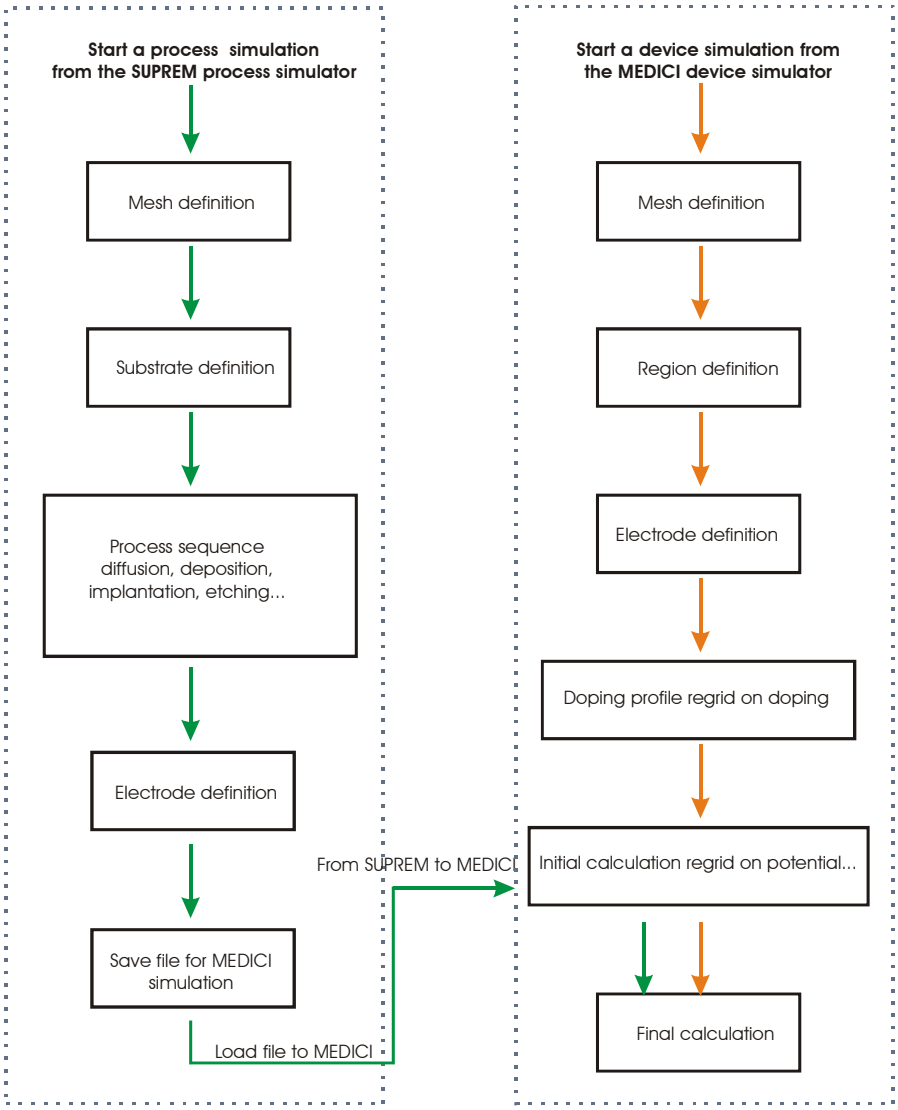


Fig. 1-4 Flow chart of the 2-Dimensional MEDICI and SUPREM simulation

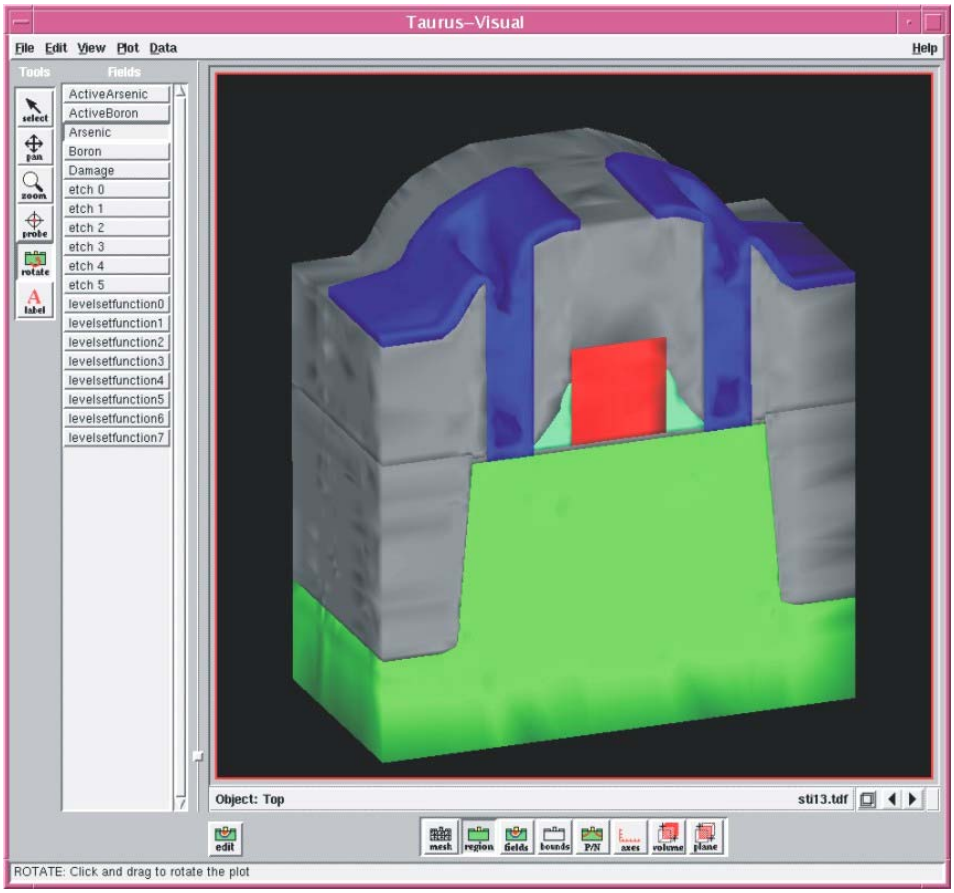


Fig. 1-5 A STI MOS obtained by 3-D simulation (displayed in the Taurus Visual window)

In this work, the optimized condition is derived from the simulation before the experiment. The experimental results are also used to calibrate the simulation.

1.3 Process development and mask design

Our clean room was built up for fabricating semiconductor sensors and laser diodes. Therefore, some facilities are not so compatible with the processes for tunnel transistor fabrication. The necessary processes must be developed, improved and calibrated to achieve the thin gate oxide, sharp doping profile, and heavy p / n doping. The processes developed in this work include: 1). The Rapid Thermal Chemical Vapor Deposition (RTCVD) system for the RT-Diffusion, oxidation and deposition. This JETLIGHT 200 RTCVD system was delivered from Siemens, but not in the working status. The program for the control unit is already vanished. Therefore, several panels were configured to enable the manual control of the power and the gas flow rates. The dopant diffusion and the thermal oxidation are investigated in this system. The rapid thermal process enables heavy, abrupt, shallow doping, and also the thinner gate oxide. 2). The Reactive Ion Etching (RIE) system for the shallow trench isolation (STI), the vertical silicon mesa, the self-aligned gate, the surface cleaning of SiB_x layer (which is formed by the p^+ diffusion), and the noble-metal patterning. The anisotropic etching of silicon, silicon oxide and metal using hard mask is investigated. 3). The

heavy and abrupt n^+ and p^+ diffusion in silicon. The Spin-on-Doping (SOD) is investigated to achieve the heavy, abrupt and shallow n^+ and p^+ doping.

Two types of mask-sets are used in our work depending on the precision requirement. For larger feature sizes, the emulsion masks are used and the software "CorelDraw" is used to design the mask. The minimum size of 10µm can be achieved using this kind of mask. Masks for the process calibration are of this kind. For high-precision requirements, the chromium masks are used. The chromium mask is designed using "IC Station" of Mentor Graphics in Institut für Physik, Universität der Bundeswehr München (Uni-Bw München). The smallest size is 0.5 µm in this kind of mask and these masks are used in the second version planar TFET fabrication in this work.

Several sets of masks are designed for fabricating MOS diode, pn diode, MOSFET and TFET. Before the TFET fabrication, the MOS diode, the p-n diode, and MOSFET are fabricated to calibrate the process. The mask-sets for the vertical and planar TFETs are also designed.

1.4 TFET fabrication

The first vertical TFET is proposed and fabricated in Universität der Bunderswehr München by Prof. W. Hansch and Prof. I. Eisele [13-17]. The definition of TFET electrodes in the first vertical TFET differs from the definition in this work. Fig. 1-6 is the schematic model of this experimental vertical Esaki-tunneling transistor. As mentioned in ref. [13], a 100nm intrinsic silicon layer acting as the channel region is grown by Molecular Beam Epitaxy (MBE) on the n^+ doped silicon substrate (source). The 300nm p 2×10^{19} doped silicon epitaxy layer is grown on the intrinsic layer and acts as drain. The gate oxide is formed on the sidewall and then the n^+ doped poly-silicon is deposited as the gate contact. The p^+ doped drain is negatively biased and the n^+ doped source is grounded. In this experimental TFET, the leakage current is one decade lower than the acceptable leakage given by the SIA-roadmap for 100nm MOSFET with supply voltage of 1.0 V.

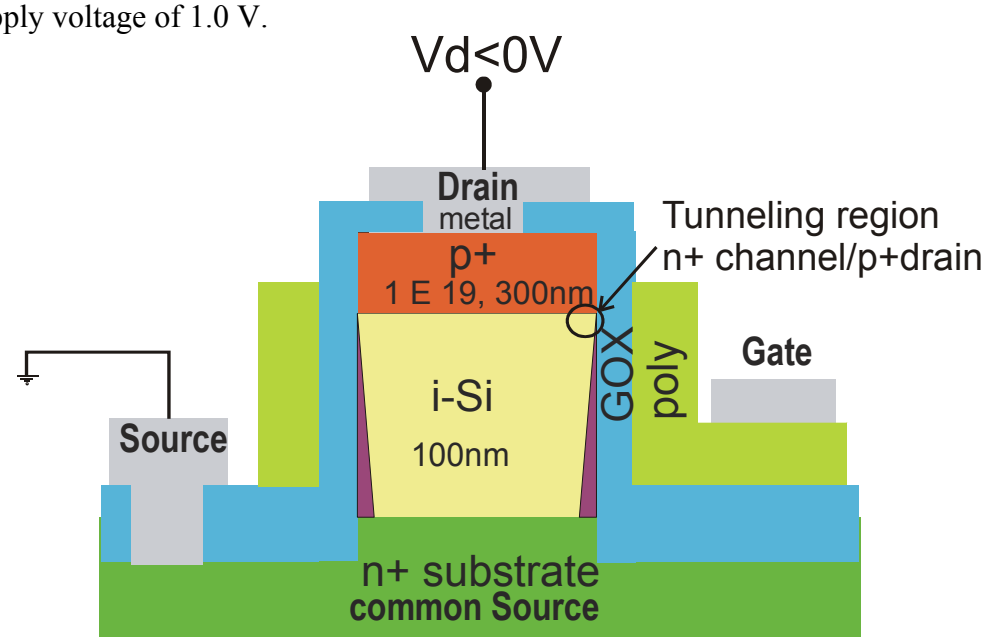


Fig. 1-6 Schematic structure of a vertical TFET fabricated using MBE

In this work, SOD is used as the diffusion source instead of the MBE doping method mentioned above and the planar TFETs are fabricated on the n^- doped <100> substrate. The schematic structure of the planar TFET is shown in Fig. 1-7. The heavily doped n and p regions shown in Fig.1-7 are formed by the diffusion of SOD in the RTP chamber. The high phosphorous / boron concentration at the silicon surface can be obtained (>2 $\times 10^{20} cm^{-3}$) and the ultra-shallow junction can be formed using the rapid thermal diffusion of SOD [18]. The gate oxide thickness of TFET is 6nm, formed by dry thermal oxidation at 900°C.

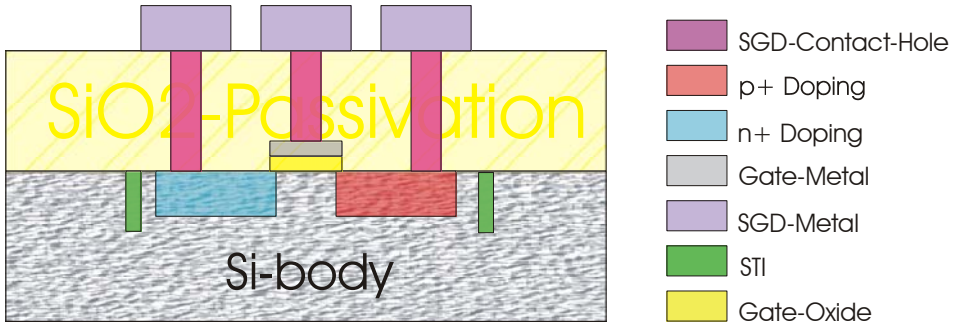


Fig. 1-7 Schematic structure of the planar TFET fabricated using the diffusion of SOD

For the first time, two types of TFETs which act like PMOS and NMOS respectively are fabricated on the single silicon substrate in this work. The NTFET with the current gain of 5 decades and the PTFET with the current gain of 6 decades are obtained. This enables the integration of complementary TFET (CTFET) circuits. Meanwhile, the experimental results fit the simulation results very well. As the simulation promised, very low leakage current in both NTFET and PTFET is found (e.g. 1.72×10^{-12} A/µm).

Compared to the vertical MBE-TFET, the drive current of the planar version TFET is improved. However, the leakage current of the planar TFET is also higher than that of the vertical TFET. That is because the vertical TFET has the smaller bulk leakage current due to the mesa structure. The silicon on insulator (SOI) together with the shallow trench isolation (STI) can further reduce the leakage current of planar TFET. In the MBE-TFET, the channel length is defined by the layer growth. The 100nm channel length TFET can be fabricated by this method. For the fabrication of the planar TFET, the challenge is to develop the self-aligned process. The minimum channel length of working planar TFET is 1µm because of the non-self-aligned process. Therefore, the self-aligned planar TFET fabrication process is proposed to shrink down the device dimension in this work.

1.5 Scope of this work

In this work, TFET is investigated in detail both in theory, fabrication and electrical characterization. In the simulation part, the physical principle, the optimized conditions, the future structure, and the comparison to MOSFET are investigated. In the fabrication part, the process development, the diode, MOSFET and the TFET fabrication are investigated.

The first chapter introduces the background and scope of this investigation. Chapter 2 introduces the semiconductor physical theories which are used in the simulation of TFET. Chapter 3 summarizes the process and device simulation results. In this chapter, some test structures are simulated in order to find out the better TFET structural design. In chapter 4, the process development for the tunnel transistor fabrication is discussed. In chapter 5, the diodes, MOSFET and TFET are fabricated and characterized. The experimental results are discussed. Chapter 6 is the summary of this work.

Chapter 2

Physical Theories

The structure of TFET is a gate-controlled p-i-n diode. According to its structural configuration, TFET is a combination of several devices: 1). The reversed p-i-n diode at the off-state. 2). The Esaki tunnel diode at the on-state. 3). The MOS diode, to form the inversion or accumulation layer when gate voltage is applied. To make the physics of TFET clear, the fundamental semiconductor theories will be reviewed first. The models for MEDICI device simulation such as carrier density and carrier transport are discussed in this chapter.

2.1 Fundamental semiconductor theories in TFET

2.1.1 Energy band diagram in TFET

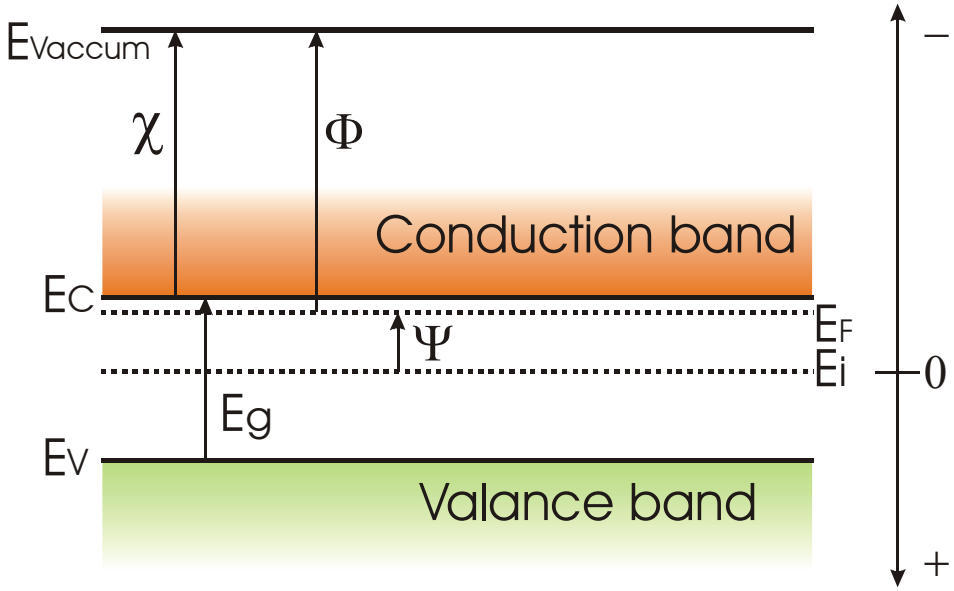


Fig. 2-1 Simplified energy band diagram of a n doped silicon

The energy band diagram of semiconductor is complex. It depends on the crystal direction. Along the main crystallographic directions in the crystal, there are multiple completely-filled and completely-empty bands. There are also multiple partially-filled bands. However, when analysing the semiconductor devices, the band diagram is simplified. The reason of this simplification is that the electronic properties of a semiconductor are dominated by the highest partially empty band and the lowest partially filled band. In the simplified energy band diagram for a n doped silicon, as shown in Fig. 2-1, the valance band and the conduction

band is defined by E_C and E_V, where E_C is the bottom of conduction band and E_V is the top of valance band. Between E_C and E_V is the band gap E_g. E_{Vacuum} is the vaccum level. The electron affinity χ is the energy difference from E_C to E_{Vaccum} in the band diagram. Ψ_{bulk} is the bulk potential of this doped silicon. Φ is the work function of silicon, which can be calculated using the following equation:

$$\Phi_{Si} = \left(\chi_{Si} + {E_g}/{2} + \psi_{bulk} \right) \tag{2-1}$$

The energy band gap E_g depends on the semiconductor material. At room temperature, the band gaps for Ge, Si, and GaAs are 0.66, 1.12, and 1.424 eV, respectively. E_g also depends on the temperature and doping concentration [19]. As the temperature increases, the band gap is narrowed. That can be explained by the increase in interatomic distance, as the volume expands due to heating. The average electron potential decreases, when the interatomic distance increases. That means that the band gap also decreases, if the interatomic distance increases. Therefore, stress can also enlarge or narrow the band gap [20]. The equation to describe the dependence of E_g on temperature is:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{2-2}$$

where $E_g(0)$, α, and β are the fitting parameters.

The increase of doping concentration will also narrow the energy band gap of a semiconductor. This effect is important for TFET because of the n^+ and p^+ heavily doped regions in TFET. The "BGN" model is used in MEDICI to describe the band gap narrowing effect in semiconductor.

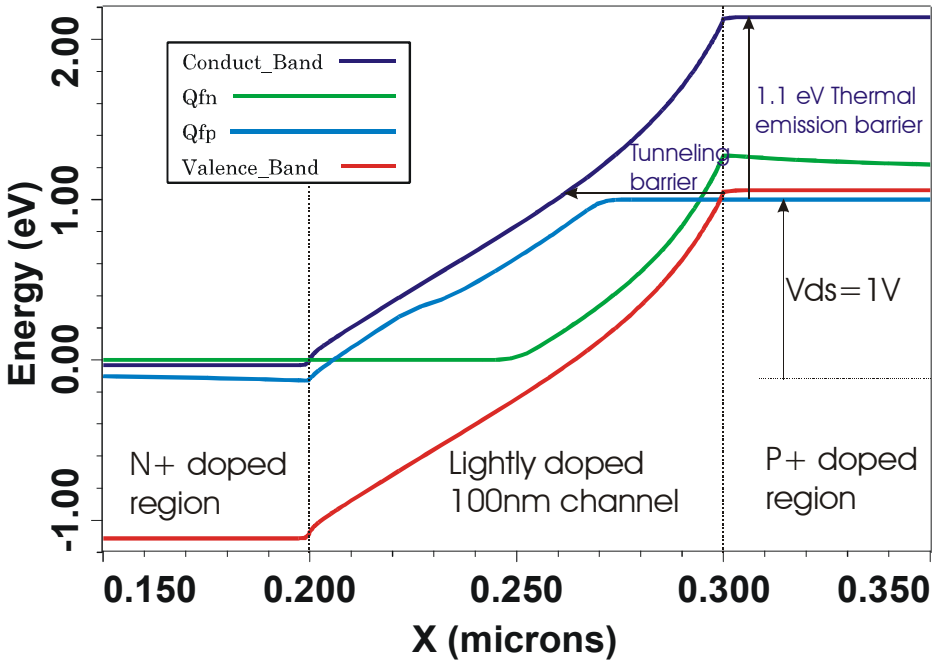


Fig. 2-2 Band diagram along the cutline beneath the gate oxide of the off-state TFET

Band diagrams are useful in the TFET working principle analysis. As an example, the band diagram along the cutline beneath the gate oxide of the off-state TFET is shown in Fig. 2-2. The quasi-Fermi levels of electrons and holes are shown in this figure. The n and p regions are heavily doped so that the Fermi level is in the band. At the off-state with V_{ds}=1V, the electric field points to the p^+ doped region. The electrons in the p^+ doped region can flow into the n^+ region by two means: thermal generation and Zener tunneling. The barriers for Zener tunneling and thermal generation are higher than that of the conventional MOSFET.

2.1.2 Carrier density in TFET

In the semiconductor, there are two types of carriers: electron and holes. The carrier density can be calculated using the density of available states and the probability that each of these states is occupied.

Using the Schördinger equation, the density of states in the conduction band and the valance band are obtained in equations 2-3 and 2-4 when the semiconductor is not degenerated:

$$N_C = 2\left[\frac{2\pi m_e^* kT}{h^2}\right]^{3/2} \tag{2-3}$$

$$N_V = 2\left[\frac{2\pi m_h^* kT}{h^2}\right]^{3/2} \tag{2-4}$$

where N_C and N_V represent the state density in the conduction band and the valance band; m_e^* and m_h^* represent the effective mass of electron and hole; T is temperature.

For the intrinsic semiconductor, the densities of electrons and holes are balanced so that the intrinsic carrier densities of electrons and holes are calculated as:

$$n_i = \sqrt{n_0 \cdot p_0} = \sqrt{N_C \cdot N_V \left(e^{(E_V - E_C)/kT}\right)} \tag{2-5}$$

The intrinsic Fermi energy is:

$$E_i = \frac{E_C - E_V}{2} + \frac{1}{2} \cdot kT \ln\left(\frac{N_V}{N_C}\right) \tag{2-6}$$

For the doped semiconductor, the total charge in the semiconductor body is zero. That means in the equilibrium status,

$$q(p_0 - n_0 + N_D - N_A) = 0 \tag{2-7}$$

Therefore, electron and hole density calculated assuming the dopants are ionized completely are:

$$n_0 = \frac{N_D - N_A}{2} + \sqrt{\left(\frac{N_D - N_A}{2}\right)^2 + n_i^2} \tag{2-8}$$

$$p_0 = \frac{N_A - N_D}{2} + \sqrt{\left(\frac{N_A - N_D}{2}\right)^2 + n_i^2} \tag{2-9}$$

The Fermi level is:

$$E_F = E_i + kT \ln\left(\frac{n_0}{n_i}\right) = E_i - kT \ln\left(\frac{p_0}{n_i}\right) \tag{2-10}$$

In the non-equilibrium status, the electron and hole density can be calculated using the Fermi-Dirac distribution. Then the total electron density is described as:

$$n = n_i \cdot \exp\left(\frac{F_n - E_i}{kT}\right) \tag{2-11}$$

the total hole density is:

$$p = n_i \cdot \exp\left(\frac{E_i - F_p}{kT}\right) \tag{2-12}$$

The TFET channel is a combination of MOS channel and tunneling channel. The MOS channel should be formed to apply potential drop on the tunneling junction. Therefore, the electron density is studied to find out the impact of this MOS channel on the performance of TFET. Fig. 2-3 shows the electrons density and the band-to-band tunneling generation rate. The electron density is low in the p^+ doped region and the p^- doped channel region. With 4V gate voltage, the electron channel is created in the middle layer so that the potential drop is concentrated on the tunneling junction as pointed in Fig. 2-3. The electron density in the n^+ doped region is also enhanced because of the accumulation of electrons.

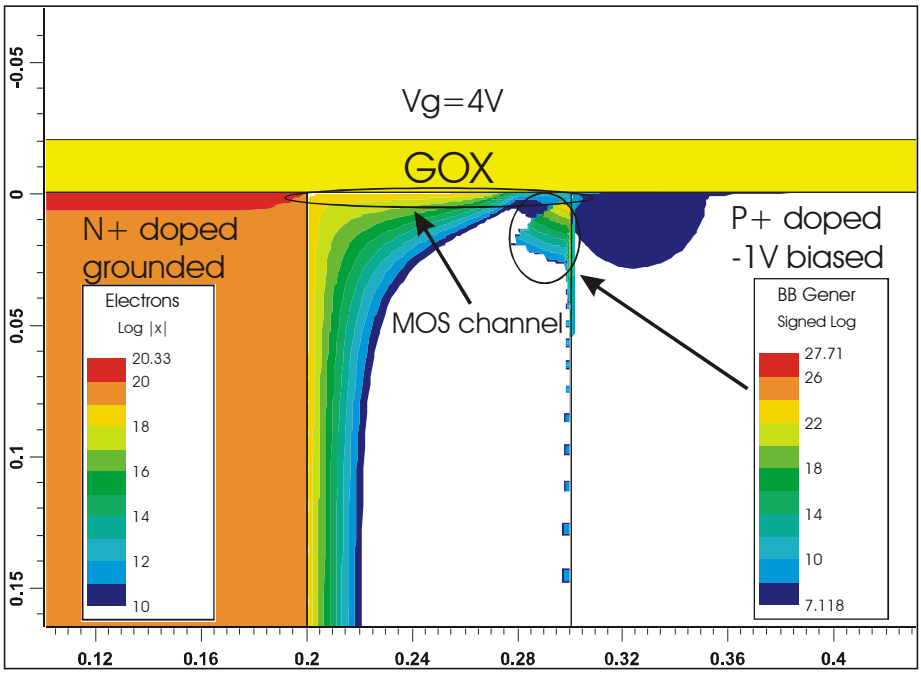


Fig. 2-3 Contour of electrons density and band-to-band generation rate in the on-state TFET (MEDICI simulation with 20nm t_{ox}, 100nm channel length)

2.1.3 Carrier transport in TFET

Several basic equations are used to describe the transport of carriers in the semiconductor.

The continuity equations are described as:

$$\frac{\partial n}{\partial t} = G_n - U_n + \frac{1}{q}\nabla \cdot J_n \tag{2-13}$$

$$\frac{\partial p}{\partial t} = G_p - U_p - \frac{1}{q}\nabla \cdot J_p \tag{2-14}$$

where G_n and G_p are the electron and hole generation rate, caused by the external influence such as the optical excitation with high-energy photon or impact ionization under larger electrical fields.

Equation to calculate the drift current is:

$$\vec{J} = qn\mu_n \vec{\varepsilon} \tag{2-15}$$

for the diffusion current:

$$0 = D_n \frac{d^2 n_p(x)}{dx^2} - \frac{n_p(x) - n_{p0}}{\tau_n} \tag{2-16}$$

$$0 = D_p \frac{d^2 p_n(x)}{dx^2} - \frac{p_n(x) - p_{n0}}{\tau_p} \tag{2-17}$$

Combine equation 2-15 and 2-16, the total electron current is

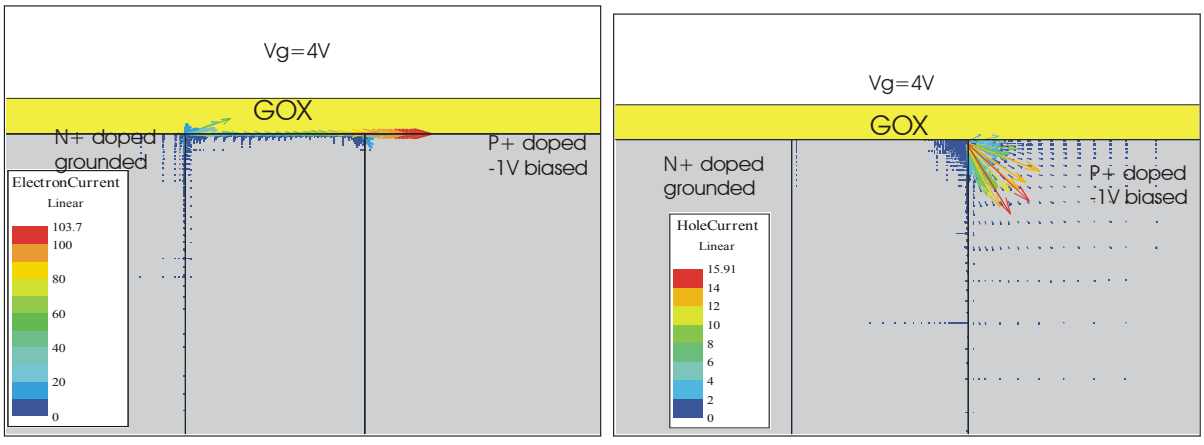
$$J_n = qn\mu_n \varepsilon + qD_n \frac{dn}{dx} \tag{2-18}$$

the total hole current is

$$J_n = qp\mu_p \varepsilon - qD_p \frac{dp}{dx} \tag{2-19}$$

the total current is described as:

$$I_{total} = A(J_n + J_p) \tag{2-20}$$



a b

Fig. 2-4 Contour of the electron (*a*) and the hole current (*b*) in the on-state TFET (MEDICI simulation with 20nm t_{ox}, 100nm channel length)

Using these equations, the current flow through TFET can be calculated. In Fig. 2-4, the electron and the hole current in the on-state TFET is shown. In the n^+ doped region and the MOS channel, the electrons are the majority carriers for the current flow. In the p^+ doped region, the holes are the majority carriers for the current transport.

Due to the injected hot electrons through the tunneling barrier, TFET is also a hot electron device. As the channel length scales down, the ballistic electron transport can be realized in TFET. The relative discussions on the ballistic electron transport can be found in chapter 5.

2.2 p-n diode, p-i-n diode and Esaki tunnel diode

2.2.1 p-n diode

The p-n junction is a basic structure for understanding other semiconductor devices. Its ideal case current-voltage characteristics are based on four approximations: 1) The boundary of depletion layer is abrupt. 2) Boltzmann approximation is used to calculate the distribution of carriers.3) The injected minority carrier densities are small compared to the majority carrier densities. 4) No generation current exists in the depletion layer[21]. The current-voltage characteristics for this ideal diode is described as:

$$J = J_p + J_n = J_0\left(e^{qv/kT} - 1\right) \tag{2-21}$$

where,

$$J_0 = \frac{qD_p p_{n0}}{L_p} + \frac{qD_n n_{p0}}{Ln} \tag{2-22}$$

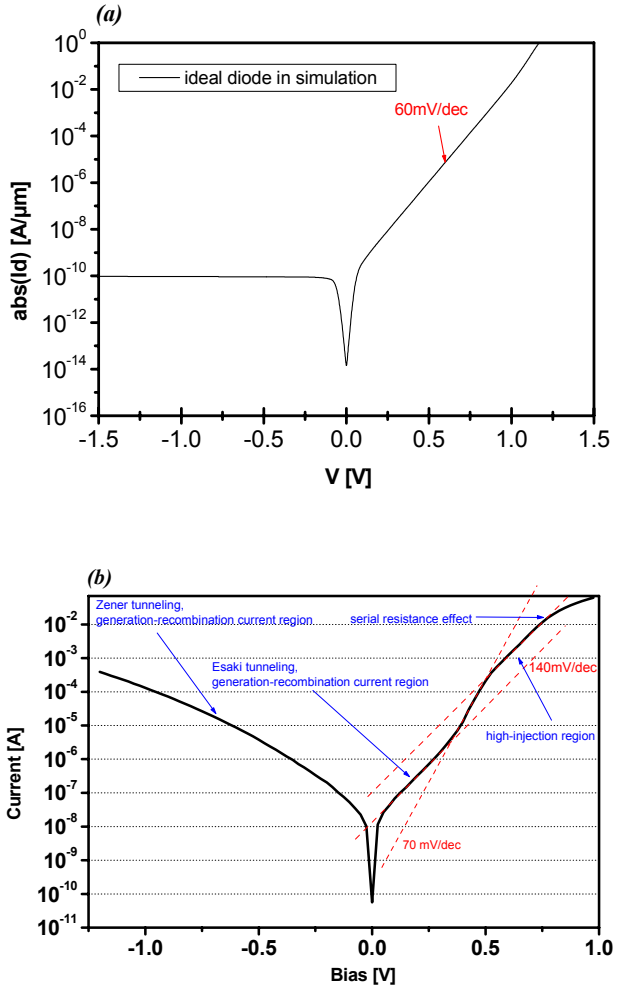


Fig. 2-5 Characteristics of a simulated ideal diode (a) and an experimental diode (b)

In the real diode, there are more effects which will cause the deviated characteristics from the ideal diode model. The comparison between the characteristics of the experimental diode and the ideal diode is shown in Fig. 2-5. Fig. 2-5 *a* shows the simulated ideal diode characteristics and *b* is the experimental characteristics of an experimental diode with high doping concentration at both sides of the p-n junction. In the experimental diode, the backward current is much higher than the ideal one. The backward leakage current consists of the generation-recombination and the tunneling current.

Generally, there are two types of recombine-generation mechanisms: the band-to-band recombination-generation and Shockley-Read-Hall (SRH) recombination-generation. In the MEDICI simulation, the "BTBT" model is used to calculate the band-to-band tunneling recombination-generation. The recombination–generation current due to the band-to-band recombination-generation can be obtained by integrating the net recombination rate. The current flow is calculated by equation 2-23. [22]

$$J_{b-b} = q\int_{-x_p}^{x_n} n_i^2\left(e^{V_a/V_t}-1\right)dx = qn_i^2 bw\left(e^{V_a/V_t}-1\right) \tag{2-23}$$

This current has the same dependence on voltage as the ideal diode current.
The SRH recombination-generation is caused by the trap assisted recombination-generation. The model "CONSRH" is used to calculate the SRH recombination-generation in MEDICI. The SRH recombination-generation current follows equation 2-24.

$$J_{SRH} = \frac{qn_i x}{2\tau}\left(e^{V_a/2V_t}-1\right) \tag{2-24}$$

The dependence of the diode current on the bias voltage is different to the ideal diode current. The $e^{V_a/2V_t}$ component results in a current slope of $\frac{2\cdot kT}{q}\left(\ln(10)\right)$ mV/dec (~120mV/dec) as shown in Fig. 2-5 *b*.

2.2.2 p-i-n diode

The pin diode is discussed here because it is the body structure of TFET. It is a diode with the sandwich structure of heavily p doped layer /high resistant "intrinsic" layer /heavily n doped layer. In practice, the "intrinsic" region is lightly n or p doped so that most of the potential drops across this region. This device is useful in the switching of the RF signals. The forward biased p-i-n diode has a large number of electron hole pairs in the intrinsic region and a significantly lower resistance at high frequency than the intrinsic material. The reaction time of the low doping material is also low, compared to the RF signals, allowing the p-i-n diode to be used as a low distortion variable resistor. Another application is that it can be used as a photo-detector. When the device is reverse-biased, an optical signal will excite the electron-hole pairs which provides a much higher reverse current or even avalanche breakdown. The p-i-n diode is sensitive to the intensity, wavelength, and modulation rate of the incident radiation. Therefore, the pin diode has the application in the optic fiber communications [23].

In TFET, the off-state transistor works like a pin diode. An experimental *I-V* curve of the off-state TFET is shown in Fig. 2-6. The leakage current of this diode is very low (TFET with V_{gs}=0V). The low leakage current results from the higher barrier in the reversed pin diode.

The band diagram of the off-state is shown in Fig. 2-2. The photo-detector function is tested by turning on the light during the measurement. The backward leakage current jumps up for 3 decades when the light is switched on.

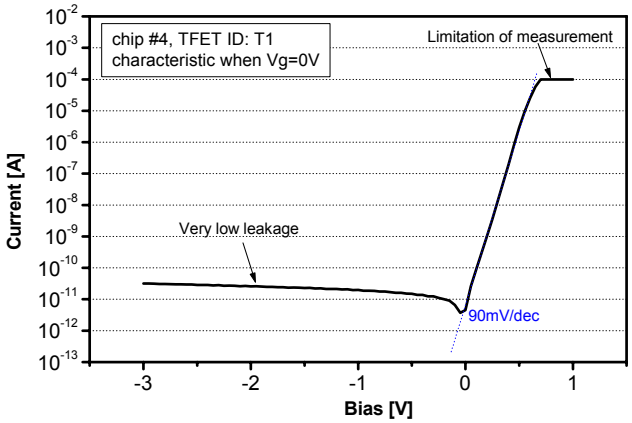


Fig. 2-6 Measured pin diode characteristic in the off-state TFET

2.2.3 Esaki Tunnel diode

The Esaki tunnel diode was first presented by Dr. Esaki in *Physical Review*, 1958. By forming the heavily doped p-n junction, the negative resistance was found in the forward *I-V* characteristics. This is the discovery of a new quantum mechanical tunneling phenomenon. This tunneling effect is called Esaki-Tunneling.

In the Esaki tunnel diode, the p-n junction is abruptly doped and also heavily doped so that the material is degenerated. Its energy band diagram at the thermal equilibrium is shown in Fig. 2-7. In this device, the Fermi level lies in the conduction band of the n-type material and in the valance band of p-type material. In Fig. 2-7, the large numbers of electrons prevail in the conduction band of the n-type material and many holes are available in the valance band of the p-type material. The width of the depletion layer is sufficiently small so that the electron transportation across this region by tunneling is rather probable [24].

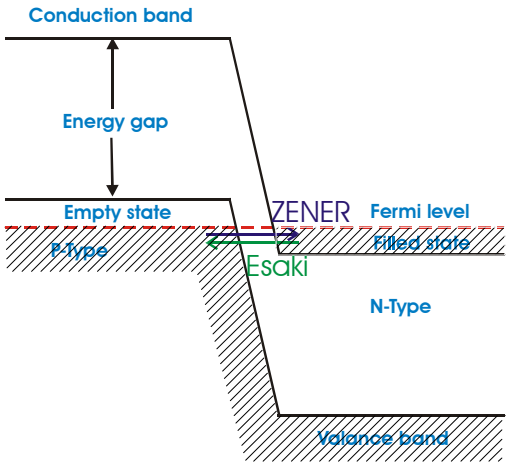


Fig. 2-7 Energy band diagram of the tunnel diode at the thermal equilibrium
(The Esaki tunneling current is of the same amount as the Band-to-Band current)

The theoretical tunnel diode current comprises three components: the tunneling current, the excess current, and the thermal current. [21] There are two types of tunneling currents in this diode: the Zener tunneling current I_Z and the Esaki tunneling current I_E. The Zener tunneling current results from the electrons tunnel from the valance band to the conduction band and the Esaki tunneling current results from the electrons tunnel from the conduction band to the valance band. Define $\rho_c(E)$ and $\rho_v(E)$ as the energy level densities in the conduction and the valance band respectively. $f_c(E)$ and $f_v(E)$ are also defined as the probabilities that a quantum state is occupied in the conduction and the valance band respectively. $f_c(E)$ and $f_v(E)$ can be calculated by the Fermi-Dirac distribution functions. The tunneling current from the conduction band to the valance band at the level E is equal to the number of electrons times the unoccupied states in the valance band times the probability for tunneling from the conduction band to the valance band without any energy change. As is shown as follows:

$$I_{c\to v}(E) = (f_c(E)\cdot\rho_c(E))\cdot((1-f_v(E)\cdot\rho_v(E))\cdot T_{c\to v} \tag{2-25}$$

where $T_{c\to v}$ is the probability for tunneling from the conduction band to the valance band.

Therefore, the total Esaki tunneling current I_E can be calculated by integrating over the range of overlapping energy states. I_Z can be obtained in the same manner [25]. Thus,

$$I_E = A\int_{E_c}^{E_v} f_c(E)\rho_c(E)\cdot[1-f_v(E)]\rho_v(E)T_{c\to v}dE \tag{2-26}$$

$$I_Z = A\int_{E_v}^{E_c} f_v(E)\rho_v(E)\cdot[1-f_c(E)]\rho_c(E)T_{v\to c}dE \tag{2-27}$$

where A is a constant.

By applying a mathematical technique called WKB approximation, the probability can be derived from the Schrödinger time-dependent wave equation.

$$T_t \approx \exp\left(-2\int_b^a p(x)\frac{dx}{\hbar}\right) \tag{2-28}$$

where T_t is the probability, $p(x)$ is the absolute value of the momentum of the particle in the barrier, $\hbar$ is the Planck's constant divided by 2π, *a* and *b* are the boundaries of the barriers.

In the case of the pn-junction diodes, the energy barrier for tunneling appears as a triangle shown in Fig. 2-8. The probability of tunneling can be calculated from equation 2-29:

$$T_t = \exp\left(-\frac{4}{3}\frac{\sqrt{2m^*}}{\hbar}\frac{E_B^{3/2}}{e\varepsilon}\right) \tag{2-29}$$

Introduce equation 2-29 into equation 2-26 and 2-27, the equations for the tunneling current are obtained. The relation between these two tunneling current in tunnel diode is shown in equations 2-26 and 2-27. These equations indicate that the Esaki tunneling current simulation needs the full band calculation which consumes lots of computing resource.

The total tunneling current I_t can be calculated as:

$$I_t = I_E - I_Z \tag{2-30}$$

where I_E and I_Z can be obtained from equations 2-26 and 2-27. As shown in Fig. 2-9, the Zener tunneling current equals the Esaki tunneling current when the bias is zero. The absolute total current increases rapidly when the bias moves in the negative direction. A closed form of equation 2-30 is given by:

$$I_t = I_P(V/V_P)\exp(1-V/V_P) \tag{2-31}$$

where I_P and V_P are the peak current and peak voltage shown in Fig. 2-9.

The excess current density J_x of tunnel diode can be calculated by:

$$J_x = J_V \exp[A_2(V-V_V)] \tag{2-32}$$

where J_V is the valley current density at the valley voltage V_V and A_2 is the prefactor in the exponent. [21]

The thermal current is the familiar equation to calculate the minority-carrier injection current of diode:

$$J_{th} = J_0\left(e^{qv/kT}-1\right) \tag{2-33}$$

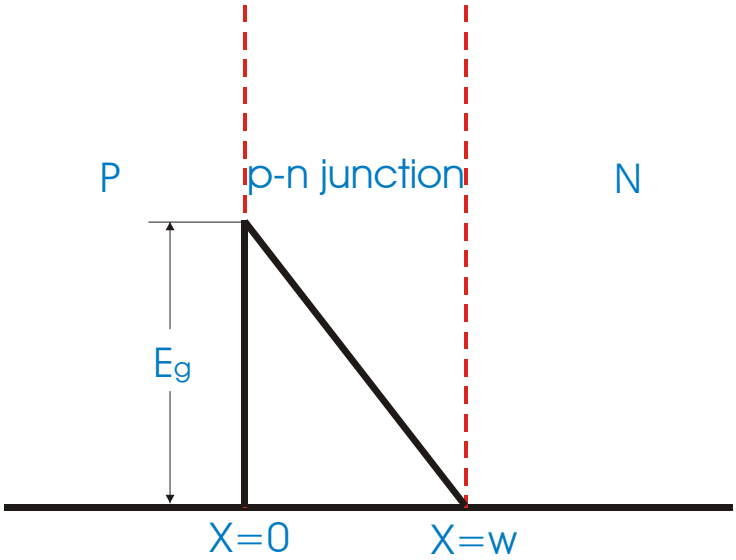


Fig. 2-8 Triangular energy barrier for tunneling calculation in the Esaki tunnel diode

The complete static *I-V* characteristic of the Esaki tunnel diode is the sum of three current components:

$$\begin{aligned} J &= J_t + J_x + J_{th} \\ &= J_P(V/V_P)\exp(1-V/V_P) + J_V \exp[A_2(V-V_V)] + J_0\left(e^{qv/kT}-1\right) \end{aligned} \tag{2-34}$$

In order to verify the gate-controlled Esaki tunneling in the experimental TFET, equations 2-31 to 2-34 will be applied in the calculation in section 5.5.5.

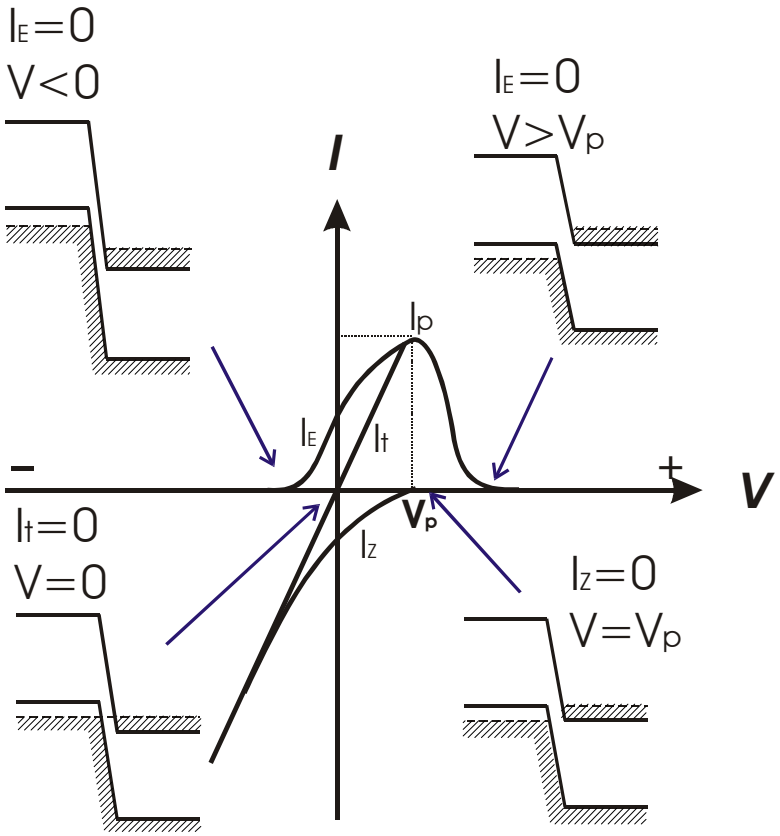


Fig. 2-9 Relation of Zener and Esaki tunneling current in the ideal Esaki tunnel diode ($I_t=I_E-I_Z$)

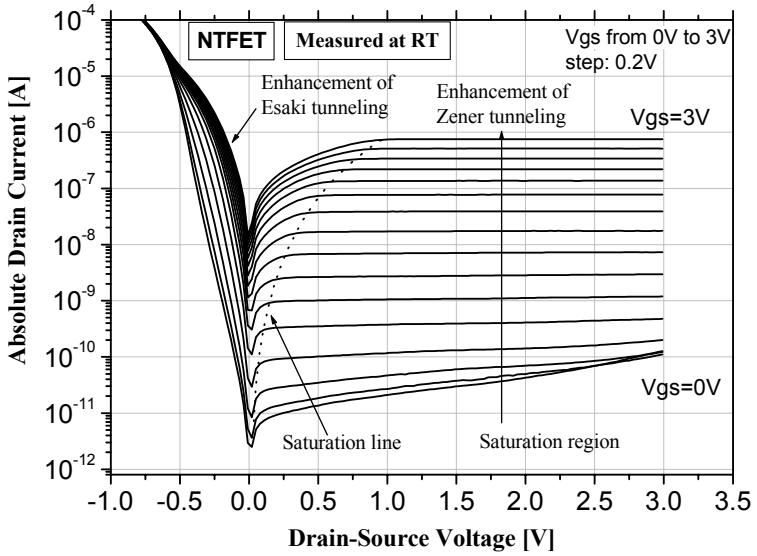


Fig. 2-10 Gate-controlled surface Esaki tunnel current and Zener tunnel current in the measured TFET output characteristics

In the gate-controlled TFET we investigate, this Zener tunneling is controlled by gate voltage when the pin diode structure is reverse biased. The gate-controlled surface Esaki tunneling current is also observed (Fig. 2-10). These tunneling effects in TFET will improve its operating speed.

2.3 Summary

In this chapter, the energy band diagram in TFET, the carriers density and the carrier transport are discussed. As mentioned in the introduction, the TFET we studied is a MOS gated pin diode. For the TFET simulation, the necessary models should be selected for the credible simulation. To simulate the current resulted from the tunneling effect and the impact ionization in TFET, the BTBT and the IMPACT models are chosen in the simulation. The dopant concentration dependant mobility model “CONMOB”, the parallel field mobility model “FLDMOB” , and the surface mobility model “SRFMOB2” are used to simulate the mobility in TFET. The principle and the improvements of this transistor will be discussed in detail in chapter 3 by the device and process simulation. The details of the corresponding models for the MEDICI device simulation can be found in the manual of MEDICI simulator. More discussion on the TFET measurement results can be found in chapter 5.

Chapter 3

Simulation of MOSFET and TFET

In this chapter the simulation results of TFET are presented. As introduced in chapter 1, the MEDICI and SUPREM simulators are used to do most of the device and process simulations. For the sake of investigating inherent physics in the devices, the MEDICI simulations of the Esaki tunnel diodes, the pin diodes and the tunneling transistor are performed. Meanwhile, the SUPREM simulation is used to extract optimized fabrication parameters and a better structural configuration.

3.1 Simulation of the Esaki tunnel diode

In order to check the models in the MEDICI simulator, the Esaki tunnel diode is simulated first. As mentioned in chapter 2, in the Esaki tunnel diode, there are two tunneling mechanisms, Esaki tunneling and Zener tunneling. Simulations are performed to certify these two models in the simulator. Fig. 3-1 is the structure of the p-n junction with the abrupt doping profile for the MEDICI simulation. Both anode and cathode doping concentration is 10^{21} cm^{-3}.

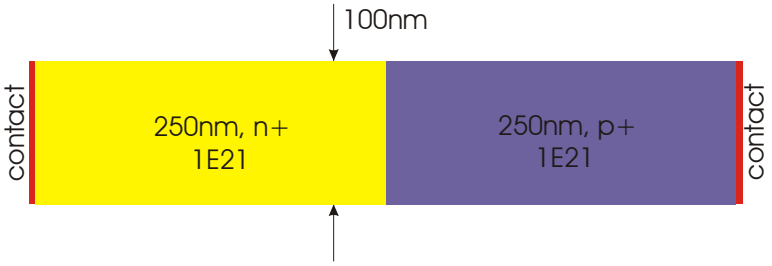


Fig. 3-1 Structure for the simulation of the Esaki tunnel diode

Considering the heavily doped material in the Esaki tunnel diode, the band gap narrowing model (BGN) is turned on or off to study the impacts of BGN model on the simulation results. In the same manner, the band-to-band tunneling model (BTBT) is tested. The concentration dependent mobility model (CONMOB), the parallel field mobility model (FLDMOB) and the enhanced surface mobility model (SRFMOB2) are chosen. At the same time, the CONSRH model is specified that the Shockley-Read-Hall recombination with the concentration dependent lifetimes is used. Furthermore, the IMPACT.I model is used considering that the carrier generation caused by the impact ionization is included in the solution self-consistently.

In Fig. 3-2, the *I-V* characteristics of Esaki tunnel diode simulated by MEDICI with the different models are displayed. The line with open circles corresponds to the *I-V* characteristic with both BTBT and BGN selected in the simulation. The voltage at the valley of the diode current is about 0.25V. Turning off the BGN model, the current is decreased a little bit. When the BTBT model is turned off, the strong backward current is disappeared and the valley voltage is at 0V.

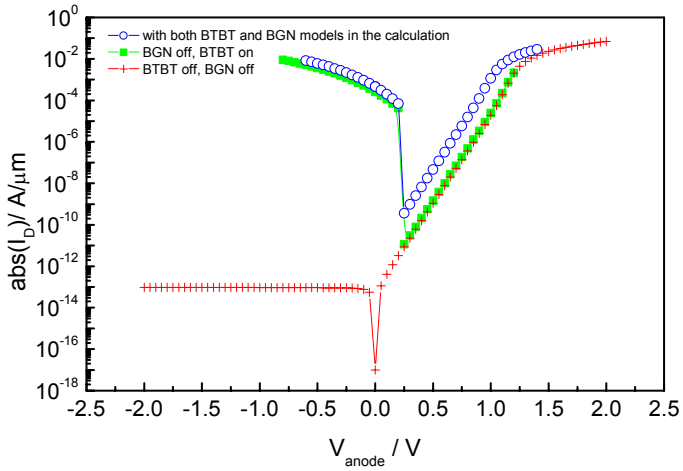


Fig. 3-2 Simulated *I-V* characteristics of the Esaki tunnel diode with the different physical models

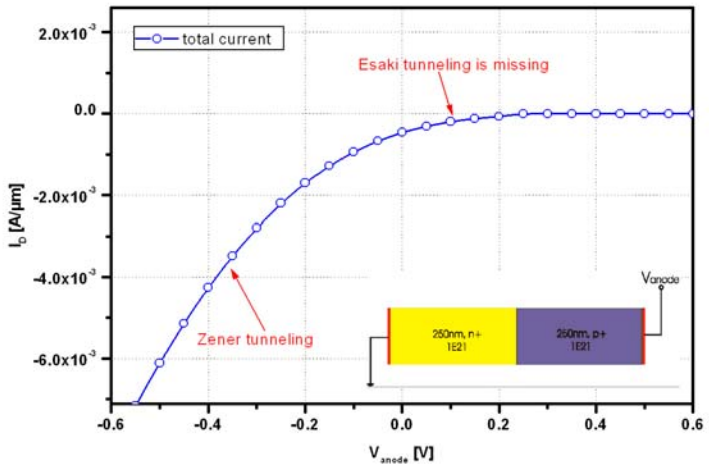


Fig. 3-3 *I-V* characteristics of the Medici simulated Esaki tunnel diode

The dependence of the total current on the bias voltage of the diode (Fig 3-3) is similar to the band-to-band tunneling current shown in Fig. 2-9 (in Chapter 2). In Fig. 3-3, the current is not zero when $V_{p\text{-}n} = 0V$. Comparing Fig. 2-9 with Fig. 3-3, it is obvious that the Esaki tunneling current is not calculated in the simulation because no negative resistance is observed in Fig. 3-3. That means that the Esaki tunnel model is not implanted in this simulator. The simulation of the Esaki tunneling current needs the full band Monte Carlo calculation and takes a very

long time. However, in this MOS gated tunneling transistor we proposed, the p-n junction is reverse biased. In this case the Esaki tunneling current is so small that it can be neglected. Therefore, the Esaki tunneling current will not be considered in our TFET simulation.

3.2 Simulation of MOSFET

3.2.1 Band-to-band tunneling in the 100nm vertical MOSFET

As the gate length of MOSFET scales down to sub-100nm, the electric field in the channel increases rapidly and the impacts of quantum mechanism on the devices rise. The electrons will tunnel directly through the gate oxide when the gate oxide thickness is close to the wavelength of electron in silicon. Moreover, the band-to-band tunneling will contribute a lot to the leakage current, when the channel doping is high in the sub-100nm MOSFET. These tunnel effects cannot be neglected in transistor fabrication and simulation. In this section, a 100nm NMOS is simulated to find out the increasing band-to-band tunneling leakage current in the short channel MOSFET.

In the vertical 50nm NMOS with the heavily doped channel fabricated by T. Shultz *et al.* [26], the high leakage current is found in the MOSFET with the high channel doping. This leakage current is assumed to be induced by the band-to-band tunneling of electrons from the drain to the channel. To verify this assumption, simulations of the similar structures are carried out.

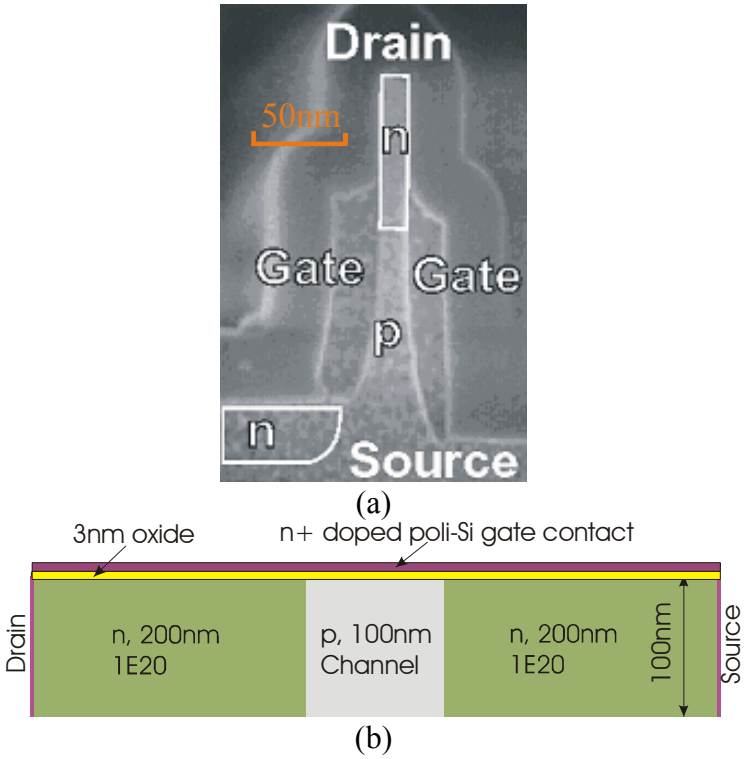
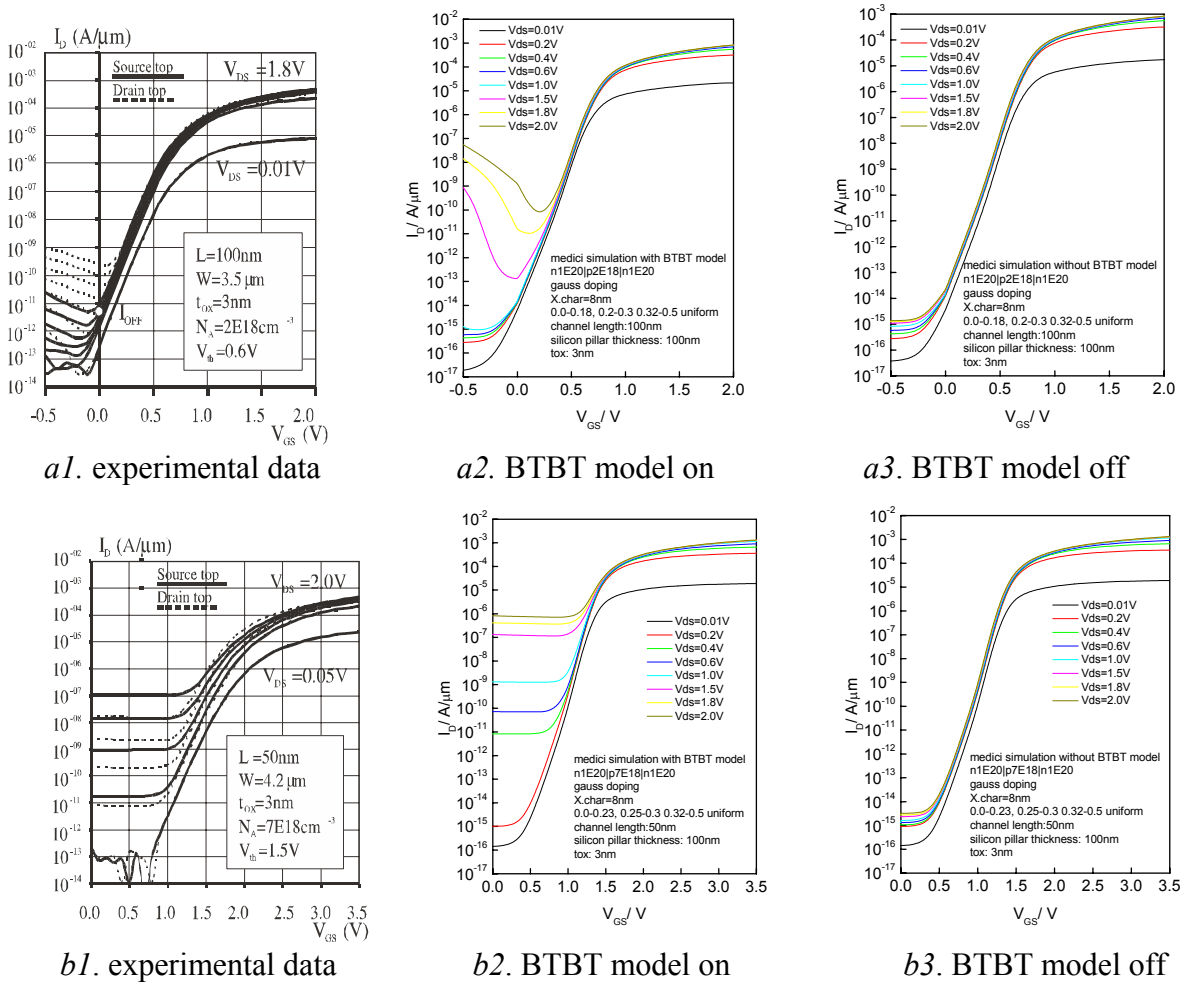


Fig. 3-4 Structure of the experimental in ref. [26] (a) and the simulated MOSFET structure (b)

Fig. 3-4 shows the structures of the experimental MOSFET and the simulated MOSFET. In both experimental and simulated structures, the oxide thickness is 3nm. The n^+ doped poly-Si is used as the gate contact. The thickness of the simulated structure is set as 100 nm. For the

difference between experimental and simulated structure, only qualitative simulation results can be obtained. Two NMOS with the 100nm p, 2E18 cm^{-3} doped channel and the 50nm p, 7E18 cm^{-3} doped channel are simulated respectively. The transfer *I-V* characteristics are simulated with the BTBT model switched on or off in order to test the source of the leakage current. The comparison of experimental and simulated transfer *I-V* characteristics is illustrated in Fig 3-5.



a1. experimental data *a2*. BTBT model on *a3*. BTBT model off

b1. experimental data *b2*. BTBT model on *b3*. BTBT model off

Fig. 3-5 Comparison of the experimental (a) and the simulated (b) transfer *I-V* characteristics a1, a2, a3 correspond to the experimental and the simulated data of the NMOS with 100nm p 2E18 cm^{-3} doped channel. b1, b2, b3 correspond to the experimental and the simulated data of NMOS with 50nm p 7E18 cm^{-3} doped channel

For the experimental data of the NMOS with 100nm p, 2E18 cm^{-3} doped channel, the leakage current increases exponentially with the drain voltage. Similar changes are found in the simulated *I-V* characteristics of this transistor. As shown in *a2* of Fig. 3-5, both ramping up the drain voltage and applying larger negative gate voltage will induce the larger leakage current. Turning off the BTBT model, the leakage current is scaled down by several orders of magnitude. This change on the leakage current distinctly confirms that the leakage is induced by the band-to-band tunneling. As regards the experimental and the simulated data of NMOS with 50nm p, $7\times10^{18}cm^{-3}$ doped channel, the leakage current is even larger due to the larger band-to-band tunneling generation rate when the channel doping level is higher. The contour

of the band-to-band tunneling generation rate in the condition of V_d= 2V, V_{gs} = -1.8V is shown in Fig. 3-6. The maximum band-to-band generation rate amounts to 5.13×10^{30} /cm^3·s. It is interesting that the tunneling is concentrated in the intersection of channel, drain, and gate. When the negative gate voltage is applied, the surface of p doped channel region is strongly accumulated and acts like a heavily p doped silicon. The formation of this surface junction results in the band-to-band tunneling of electron from the channel to the drain. When the gate voltage becomes more negative, the tunneling current increases. That means that part of the leakage current is controlled by gate voltage. This effect is called the gate induced drain leakage (GIDL).

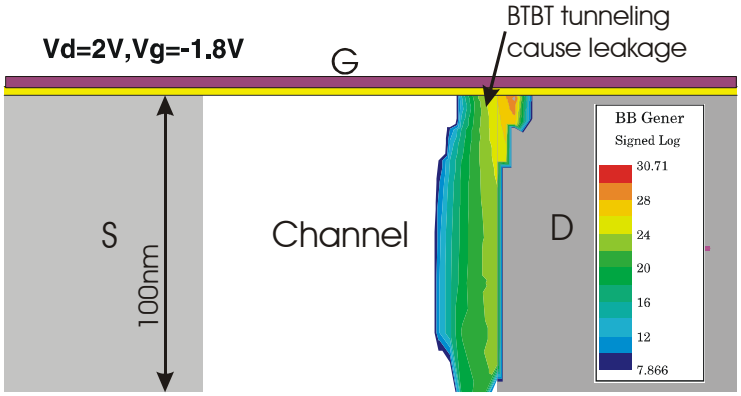


Fig. 3-6 Contour of the band-to-band tunneling generation rate of NMOS with the 100nm p 2×10^{18}cm^{-3} doped channel, V_{ds}=2V, V_{gs} =-1.8V

3.2.2 Double gate and fully depleted MOSFET

In order to avoid these problems caused by heavy channel doping, the double gate / fully depleted (FD) MOS was proposed recently. In the FDMOS, the channel region is intrinsic or lightly doped silicon so that the doping fluctuation problem can be avoided. The reduced leakage current is proved by simulation [27-30]. A FD-NMOS structure is simulated in this section. As shown in Fig. 3-7, a FD-NMOS structure with the silicon thickness of 20nm and the channel length of 100nm is defined. A 3nm gate oxide is used in this simulation. Both source and drain are n^+ doped with the concentration of 1×10^{20} cm^{-3}. The smear out of diffusion is considered in this simulation.

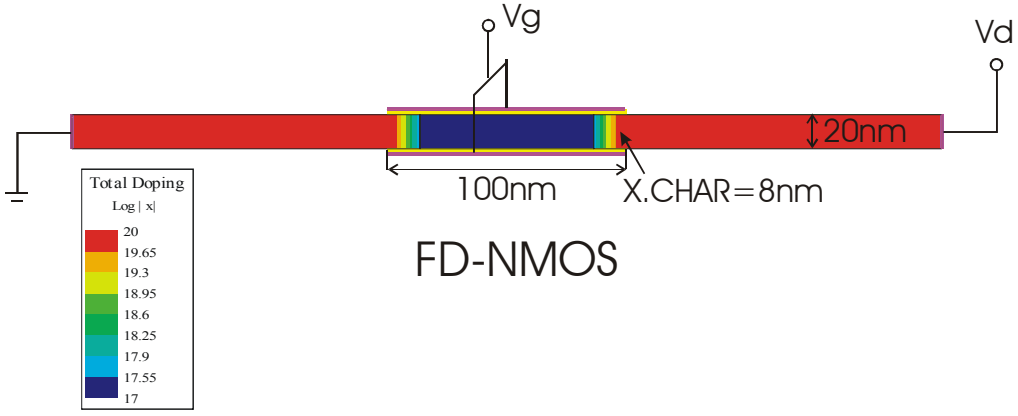


Fig. 3-7 FD-NMOS structure with silicon thickness of 20nm and channel length of 100nm

From Fig. 3-8 it can be seen that in the fully depleted NMOS, the gate material with the larger working function ϕ_m is needed to increase the V_t of this NMOS.

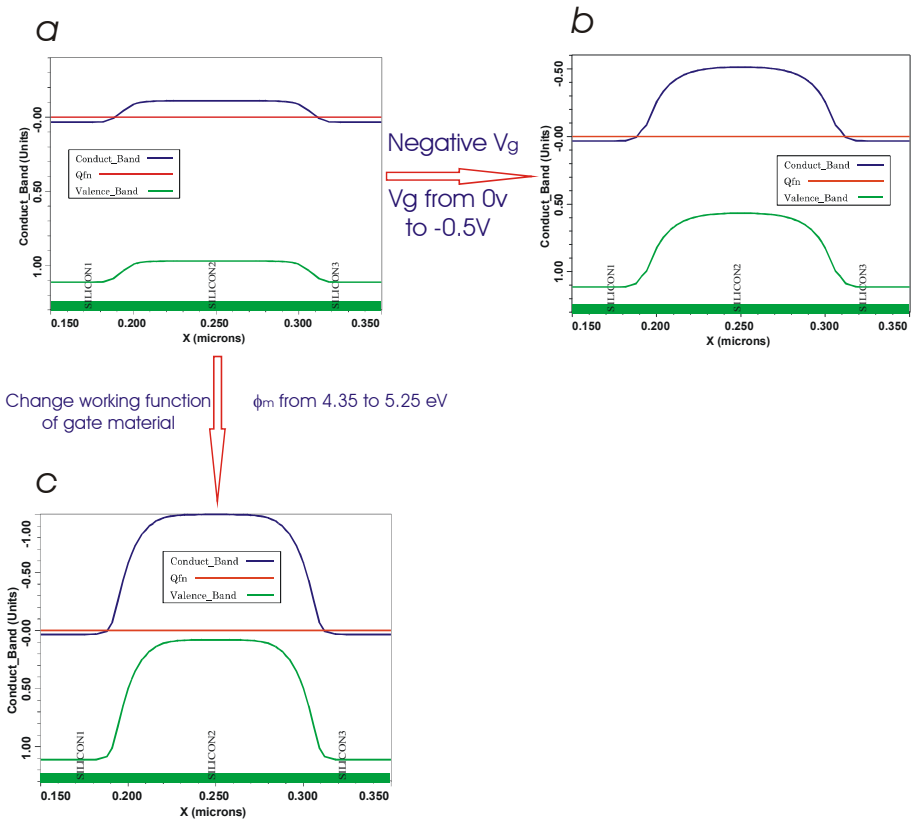


Fig. 3-8 Band diagrams of the FD-NMOS along the cutline 5nm away from the oxide interface. a). V_{gs} =0V, the gate is n^+ doped poly-Si (ϕ_m=4.35eV). b). Decrease V_{gs} from 0V to –0.5V, the electron barrier increases. c). Change the gate material to the p^+ doped poly-Si (ϕ_m=5.25eV), the barrier also increases. The simulations are performed at V_{ds}=0V and the channel doping is p $1\times10^{17}cm^{-3}$.

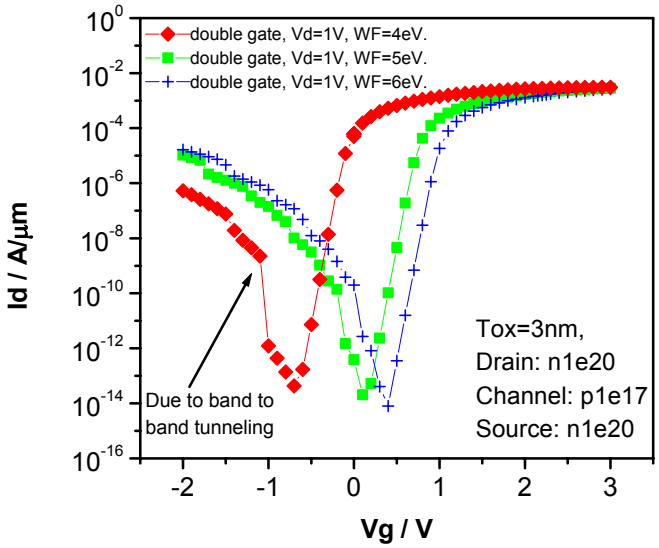


Fig. 3-9 Transfer characteristics of FD-NMOS with different gate materials, ϕ_m=4, 5, 6 eV

The transfer characteristics of the FD-NMOS with the different ϕ_m are shown in Fig. 3-9. It can be seen that the threshold voltage can be adjusted by changing the working function of the gate material. However, in this simulation of FD-NMOS, the band-to-band tunneling leakage still exists, when the transistor is turned off. As shown in Fig. 3-10, the band-to-band tunneling is still on, when the transistor is turned off (V_{gs} =0V). Fig. 3-11 shows the band diagram of this off-state FD-MOS. The bending of bands enables the band-to-band tunneling at the junction of channel-drain.

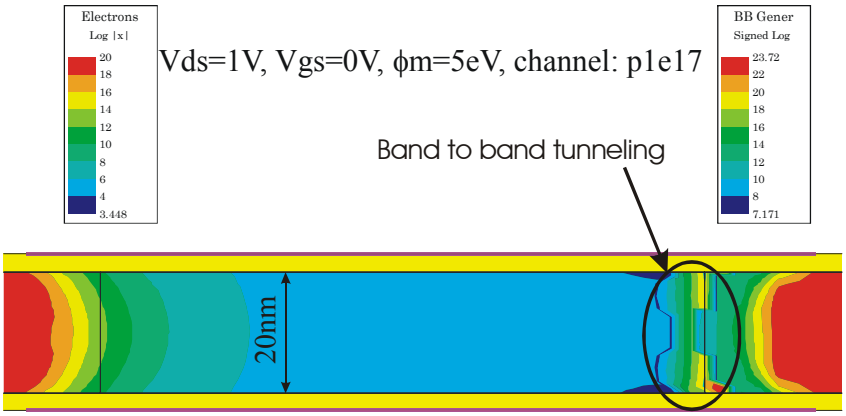


Fig. 3-10 Contour of the band-to-band tunneling generation rate and the electron density in an off-state FD-NMOS, V_{ds}=1V, V_{gs} =0V

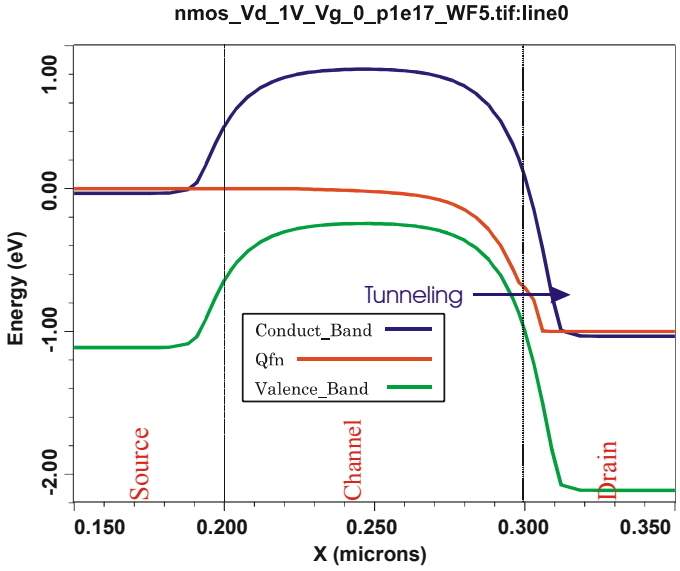


Fig. 3-11 Band diagram of a FD-NMOS with ϕ_m=5eV. (V_{ds}=1V and V_{gs} =0V)

The total current in the off-state FD-NMOS is investigated. Fig. 3-12 shows the total current of this FD-NMOS at V_{ds}=1V and V_{gs} =0V. The current density increases from the interface to inner silicon. With a thinner silicon body, the leakage current can be suppressed efficiently. At the channel-drain junction, where the highest current density can be found, the band-to-band tunneling generation rate is also very high.

From the discussion of this small dimension MOSFET, it seems that as the dimension of MOSFET scales down, the increasing leakage current is always a problem even in the FD-MOS.

For TFET, considering the high barrier of the reversed p-i-n junction, the leakage current of this tunneling transistor will be much smaller. Hence, the application of the tunneling mechanism in the TFET with MOS gated p-i-n diode structure enables TFET to be a hopeful candidate of future MOSFET. TFET will be simulated and compared to MOSFET in the next section. The comparison of MOSFET and TFET will also be discussed in detail.

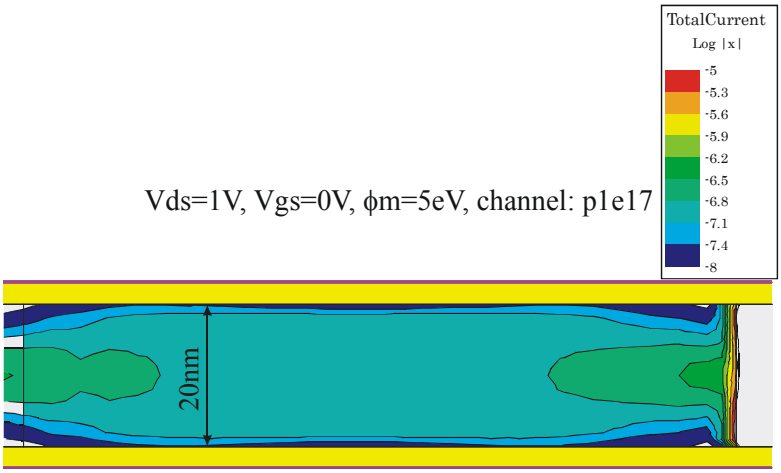


Fig. 3-12 Total current of FD-NMOS at V_{ds}=1V and V_{gs} =0V

3.3 Device simulation of TFET

In this section, various structures of TFET are simulated. The influences of the doping profile, the gate oxide thickness and the electric field on the characteristics of TFET are investigated in detail. In order to compare the impacts of these variations on the devices, the simulation is started from the basic tunneling transistor simulation.

3.3.1 Simulation of the basic TFET structure

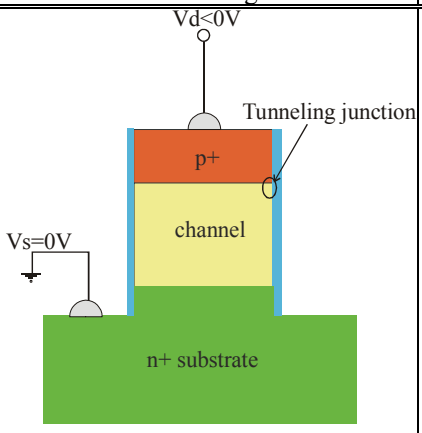
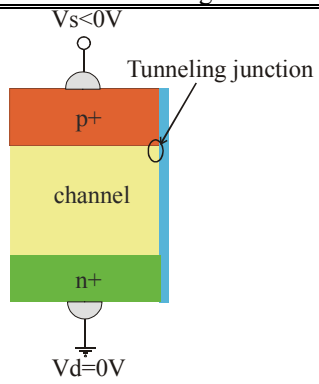
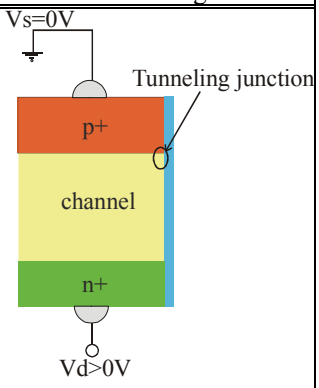
3.3.1.1 Definition of the simulated structure and electrodes

There are two types of TFETs which are called NTFET and PTFET (see chapter 1). The transfer characteristics of the NMOS-like and the PMOS-like TFET are shown in Fig. 1-1. As shown in Fig.1-1, the drain current of NTFET increases with the increasing gate voltage. The NTFET is switched on when $V_{gs} > V_t$. For PTFET, the drain current increases with the decreasing gate voltage. TFET is switched on when $V_{gs} < V_t$. In the NTFET, the p^+ doped region is named as source (source of electrons) and the n^+ doped region is named as drain (drain of electrons). In the PTFET, the p^+ doped region is named as drain (drain of holes) and the n^+ doped region is named as source. In table 3-1 three connection configurations of NTFET are listed. Our experimental NTFETs measurement is connected in the connection configuration *c*.

In the first publication of TFET, the first vertical NTFET is discovered and the definition of source / drain differed from the definition used in this work. As mentioned in Ref.[13], the first NTFET is fabricated using MBE on the n^+ doped silicon substrate. The heavily n doped

region was named as source and the heavily p doped region was drain. The p^+ doped drain was negatively biased with n^+ doped source grounded in the measurement shown in ref. [13-16]. This connection is defined as connection configuration *a* in table 3-1. Therefore, in order to be coincident with the experimental measurement results of this first NTFET, simulations of NTFET are performed at the beginning. At the same time, the simulated NTFET is with the negative biased p^+ doped source, the grounded n^+ doped drain and the positive biased gate, using the definition in this work. This connection configuration is *b* in table 3-1.

Table 3-1 Three connection configurations of NTFET

	Connection configuration ***a***	Connection configuration ***b***	Connection configuration ***c***
Connection and electrodes definition			
Comments	The first experimental vertical NTFET fabricated in Uni-Bw München by growing MBE layers on the n^+ substrate. The substrate is named as the source electrode. [13-16]	Simulated NTFET coincident to the first MBE-NTFET with the same bias but the different electrodes definition (source and drain are changed)	NTFET connected using the positive biased n^+ drain and grounded p^+ source. (In order to be compatible to the logic circuit design where both gate and drain voltages are positive)

The structure of this basic NTFET structure is shown in Fig. 3-13. The gate oxide thickness is set as 20nm and the thickness of the silicon is 500nm. The simulation setup of the 20nm gate oxide is the same oxide thickness of the first experimental TFET in Ref. [13]. The source, channel, and drain are set as 200nm p $1\times10^{20}cm^{-3}$, 100nm p $1\times10^{17}cm^{-3}$, 200nm n $1\times10^{20}cm^{-3}$ respectively. The doping profile at the n^+-p and p-p^+ junctions are assumed to be abrupt. The gate contact is defined as the n^+ doped poly-Si. Along the cutline beneath the gate oxide, the one dimension information such as the doping profile, the energy bands, etc. can be plotted. Details for the structure and calculation of the basis tunneling transistor model are given in table 3-2.

Table 3-2 Details of on TFET structure and the simulation model of the basis NTFET

Structure	Doping profile	Models used for calculation
T_{ox}: 20nm	Abrupt doping	CONMOB FLDMOB CONSRH SRFMOB2 BTBT IMPACT.I
Width: 500nm	Drain: 200nm n^+ 1e20cm^{-3}	
Depth: 500nm	Channel : 100nm p 1e17cm^{-3}	
	Source: 200nm p^+ 1e20cm^{-3}	

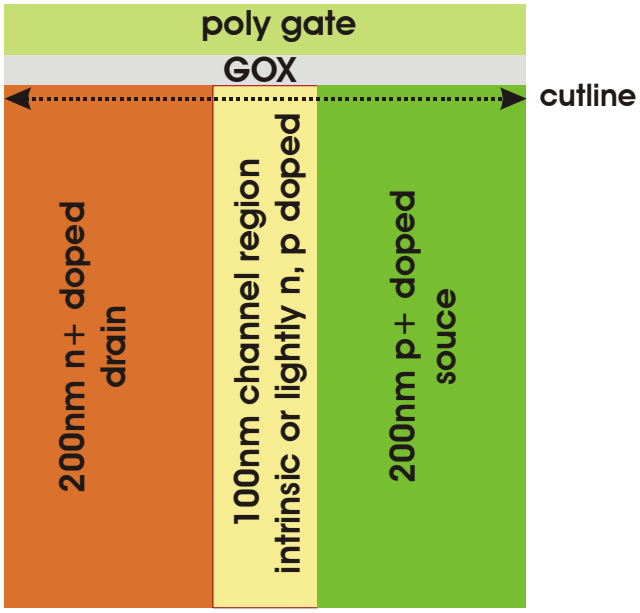


Fig. 3-13 Structural model for the NTFET simulation

3.3.1.2 Transfer and output characteristics of the simulated NTFET

Set the drain bias as zero and apply a negative bias on the source electrode. Then ramp up the gate voltage. The transfer and output *I-V* characteristics can be obtained by simulation (Fig. 3-14). With the absolute source voltage increasing, I_{off} and I_{on} increase, the "threshold voltage" decreases, the subthreshold swing remains almost the same. The leakage current is about 10^{-15} A/μm when the source voltage is -1.0V. That is much smaller than the leakage current of the traditional MOSFET. From the output transfer characteristics it is found that the current gain is about 9 orders of magnitude at the -0.8V supply voltage.
In this simulation, the band-to-band tunneling generation rate is calculated as [31]:

$$\text{G.BB}=\text{A.BTBT}\frac{E^2}{E_g^{1/2}}\cdot\exp\left(-\text{B.BTBT}\frac{E_g^{3/2}}{E}\right) \tag{3-1}$$

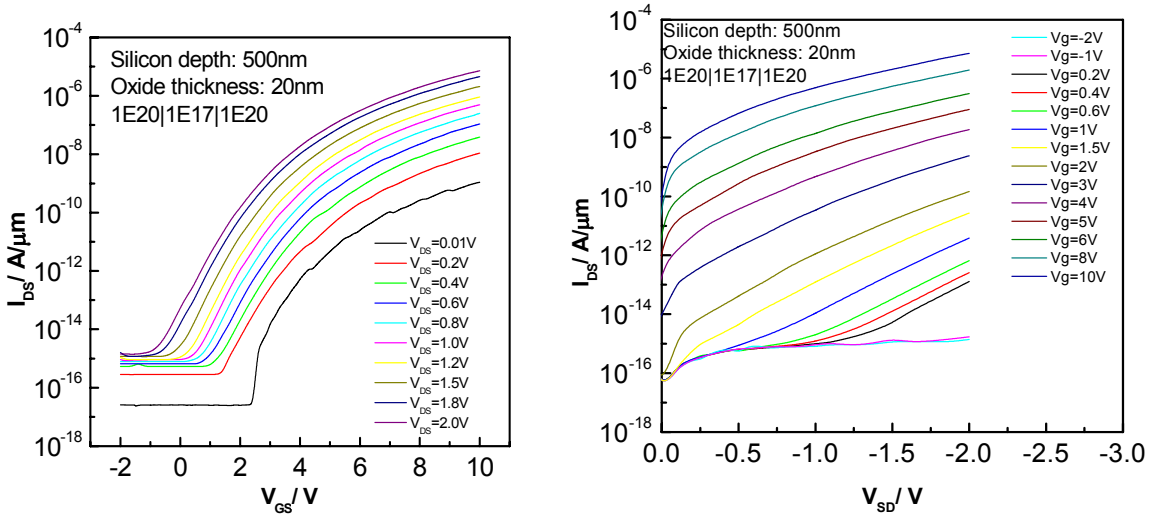
In this expression, *G.BB* is the band-to-band tunneling generation rate, *E* is the magnitude of the electric field and is E_g the energy bandgap. The parameters A.BTBT and B.BTBT can be used as constants in this model with the values A.BTBT=3.5×10^{21} $eV^{1/2}$ / $cm\cdot s\cdot V^2$, B.BTBT=22.5×10^6 V / $cm\cdot(eV)^{3/2}$. A search along the direction opposite to the electric field is performed to determine whether there is an electric potential increase at least for the band-to-band tunneling to occur. In the continuity equation:

$$\frac{\partial n}{\partial t}=\frac{1}{q}\vec{\nabla}\cdot\vec{J}-U_n \tag{3-2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\vec{\nabla}\cdot\vec{J} - U_p \tag{3-3}$$

U_n and U_p represent the electron and hole recombination respectively. As shown in Equation 3-1, *G.BB* increases monotonously with the electric field magnitude increasing. The more negative source voltage will provide the larger electric field at the channel-source junction. Thus, the absolute drain current increases with the source voltage decreasing (the more negative source voltage).

Although the behavior of TFET is similar to MOSFET, the threshold voltage of TFET using the connection configuration *b* in table 3-1 shows more dependency on the source voltage. Using the connection configuration *c* in table 3-1 the simulation with the source grounded and the drain positive biased is performed and the simulated transfer characteristics are shown in Fig. 3-15. The V_t shift is reduced a lot by grounding the source electrode. The similar effect as the DIBL of MOSFET is observed in TFET. However, this V_t shift should be named as the Drain Induced Tunneling-barrier Lowering (DITL) effect in TFET as will be discussed in the section 5.5.1.



a *b*

Fig. 3-14 Transfer (*a*) and output *I-V* characteristics (*b*) of the basic NTFET simulation model

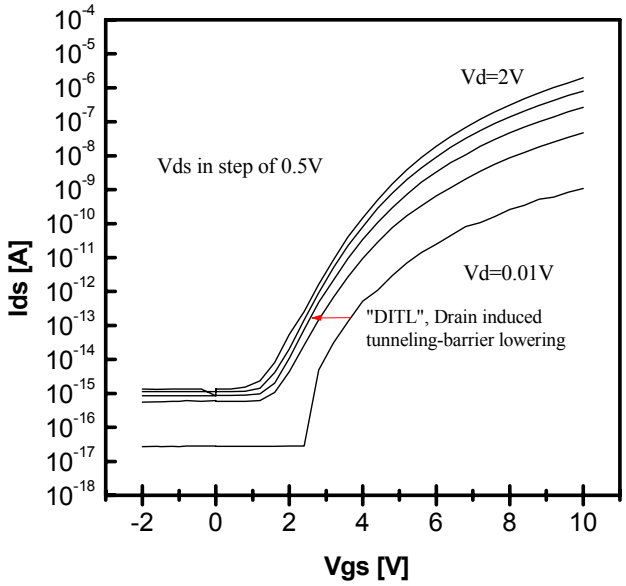


Fig. 3-15 Simulated transfer characteristics of the basic NTFET structure with the p^+ source grounded and the n^+ drain positive biased. The V_t shift is reduced.

3.3.1.3 Relation of Band Diagrams, II.GENER, BB.GENER and Electric Field

To investigate the mechanism of gate-controlled tunneling effects, the band diagrams are plotted in this section. Meanwhile, the dependence of II.GENER and BB.GENER on the electric field is investigated.

3.3.1.3.1 Energy band diagrams

The energy bands are used in the semiconductor simulators to calculate the carrier concentration. The electron and hole concentrations in semiconductors can be defined by Fermi-Dirac distributions and a parabolic density of states. When these are integrated, they yield:

$$n = N_C F_{1/2}(\eta_n) \tag{3-4}$$

$$p = N_V F_{1/2}(\eta_p) \tag{3-5}$$

where

$$\eta_n = \frac{E_{Fn} - E_C}{kT} \tag{3-6}$$

$$\eta_p = \frac{E_V - E_{Fp}}{kT} \tag{3-7}$$

In these equations, N_C and N_V are the effective density of states in the conduction and valance bands, E_C and E_V are the conduction and valance band energies, E_{Fn} and E_{Fp} are the electron and hole Fermi energies.

Fermi-Dirac integral is:

$$F_{1/2}(\eta_S) = \frac{2}{\sqrt{\pi}} \int_0^{\infty} \frac{\eta^{1/2}}{1 + \exp(\eta - \eta_S)} d\eta \tag{3-8}$$

Particularly, the Fermi–Dirac statistics should be used when the carrier concentration is high. For the operating range of most semiconductor devices, equation 3-4 and 3-5 can be simplified using the Boltzmann statistics which are used in our MEDICI simulations:

$$n = N_C \exp(\eta_n) = N_C \exp\left[\frac{q}{kT}(E_{Fn} - E_C)\right] \tag{3-9}$$

$$p = N_V \exp(\eta_p) = N_V \exp\left[\frac{q}{kT}(E_V - E_{Fp})\right] \tag{3-10}$$

In the MEDICI simulation, the energy levels are calculated in the semiconductor. The band diagram can be plotted along the cut line in the material. Fig. 3-16 shows the band diagram in the basic NTFET which is switched on with $V_d = 0V$, $V_s = -1V$, and $V_g = 10V$. The cut line is at the location of y=2nm, which is close to the Si-SiO_2 interface. In the drain and source regions, it is heavily doped so that the Fermi Energy level is out of the forbidden band. In the lightly p doped channel region, a strong inversion channel is formed with the positive gate voltage. As a result, the potential drop is focused on the channel-source junction. The energy levels have very steep slopes at the channel-source junction. The tunneling barrier is nearly transparent for the electrons to tunnel from the valance band in the source region to the conduction band in the channel region.

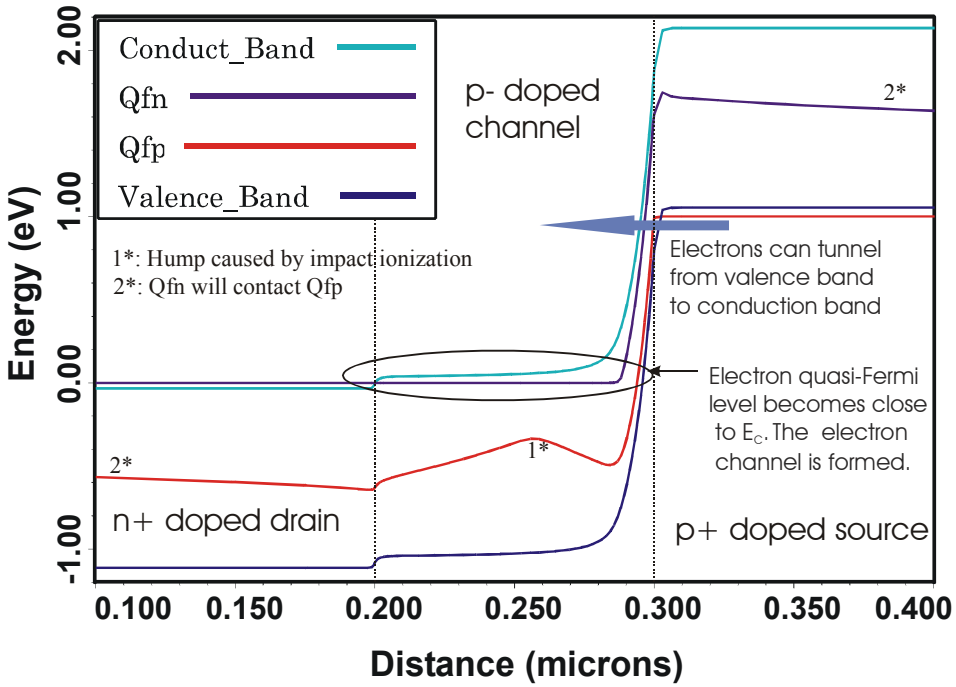
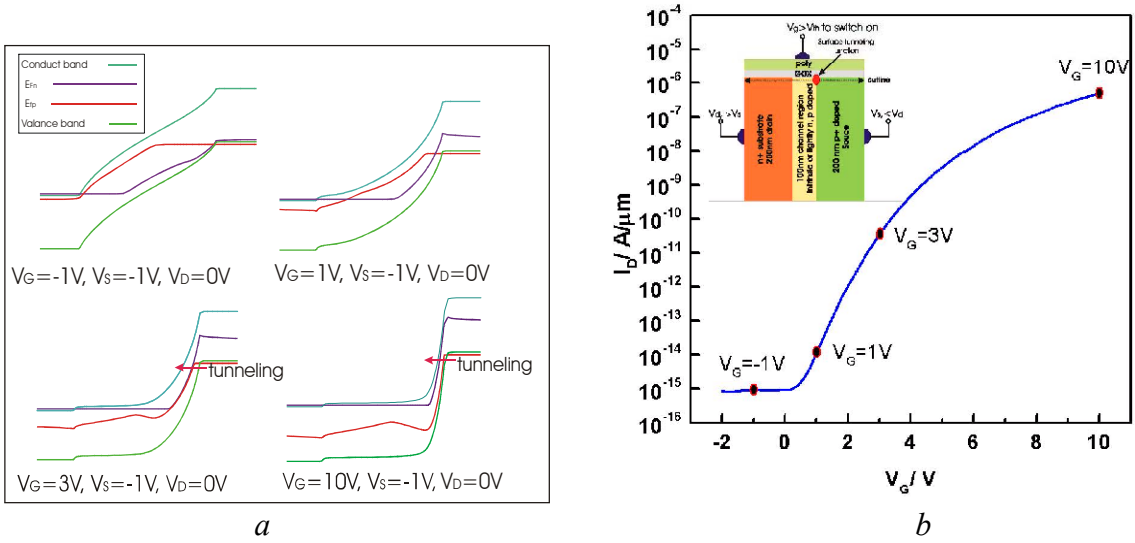


Fig. 3-16 Band diagram in the basic NTFET model with $V_s = -1V$, $V_g = 10V$, $V_d = 0V$ (the cut line is at the location of y=2nm, near the Si-Oxide interface in the silicon bulk)

Varying the gate voltage from –1V to 10 V when V_s is –1V, a series of band diagrams are obtained along the cut line of y=2nm. Fig. 3-17 shows these band diagrams and the corresponding *I-V* characteristic. It can be seen from Fig. 3-17 *a* that when the gate voltage is

–1V, the transistor is turned off. The corresponding band diagram with V_g=-1V is similar to the reverse biased p-i-n diode. The tunneling barrier and the thermal generation barrier are high. Thus the leakage current of this TFET is as low as 10^{-15} A/μm. As the gate voltage increases to 1V, 3V, and 10V, the slope of energy levels at the channel-source junction increases. This results in the increase of the band-to-band tunneling current.



a *b*

Fig. 3-17 Band diagram along the cut line at the location of y=2nm (a), and the *I-V* characteristic of the basic tunneling model (b). (V_d=0V, V_s =-1V). t_{ox} = 20nm

3.3.1.3.2 BB.GENER, II.GENER and Electric Field

The equation for calculating the impact ionization generation rate *II.GENER* (or *G.II*) in MEDICI is shown as:

$$G.II = \alpha_{n,ii} \cdot \frac{\left|\vec{J}_n\right|}{q} + \alpha_{p,ii} \cdot \frac{\left|\vec{J}_p\right|}{q} \tag{3-11}$$

where $\alpha_{n,\ ii}$ and $\alpha_{p,\ ii}$ are the electron and hole ionization coefficients, $\vec{J}_n$ and $\vec{J}_p$ are the electron and hole current densities. The ionization coefficients are decided by the local electric field:

$$\alpha_{n,ii} = \alpha_{n,ii}^{\infty}(T) \cdot \exp\left[-\left(\frac{E_{n,ii}^{crit}(T)}{E_{n,\|}}\right)^{EXN.II}\right] \tag{3-12}$$

$$\alpha_{p,ii} = \alpha_{p,ii}^{\infty}(T) \cdot \exp\left[-\left(\frac{E_{p,ii}^{crit}(T)}{E_{p,\|}}\right)^{EXP.II}\right] \tag{3-13}$$

where $E_{n,\|}$ and $E_{p,\|}$ are the electric field components in the direction of current flow.

The investigation of impact ionization is a sophisticated task in TFET. We simulated the distribution of impact ionization in this transistor. It is found that the impact ionization occurs

near the region of tunneling because of the injection of electrons from the drain to the channel due to the tunneling effect. The distribution of energy of the injected electrons is non-Maxwellian because the electrons are from the heavily p doped source (Electrons are confined in the valance band). According to the band diagram of the on-state TFET, the energy of the injected electrons depend on the magnitude of V_{sd}. As we know, the impact ionization in silicon starts, when the electron energy is above 1.1 eV. If the TFET works with the supply voltage of 0.5V, the impact ionization can be remarkably reduced. In addition, in the experimental measurement, the gate leakage is negligible and almost independent of the gate voltage when V_g / T_{ox} < 0.75 V / nm at V_{sd} = -1V. [13] Therefore, the impact ionization should be a problem of reliability, but can be handled by reducing the supply voltage.

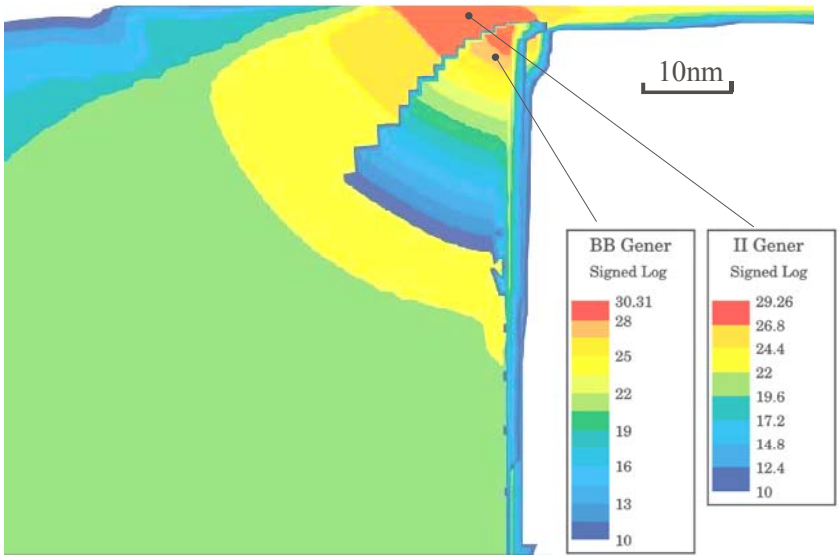
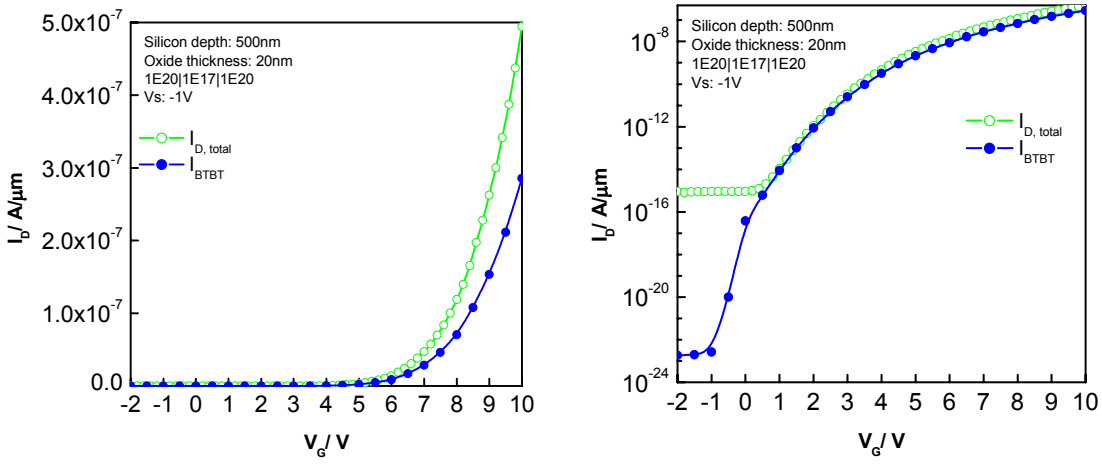


Fig. 3-18 Contour of *BB.GENR* and *II.GENER* @ V_g =10V, V_s =-1V, V_d=0V in NTFET



a *b*

Fig. 3-19 Relation of the total drain current and the band-to-band tunneling current with the linear Y axis (*a*), and the log Y axis (*b*), V_s = -1V, V_d = 0V in NTFET.

Fig. 3-18 plots the contour of *BB.GENR* and *II.GENER* @ V_g =10V, V_s =-1V, and V_d=0V. The maximum *BB.GENER* is $2.04\times10^{30}/cm^3\cdot s$ and the maximum *II.GENER* is $2.29\times10^{29}/cm^3\cdot s$. In the simulation, the total current of TFET consists of the band-to-band tunneling current and the impact ionization current. As shown in Fig. 3-19, the band-to-band tunneling current is nearly half the total drain current when the transistor is turned on. It is found that the impact ionization is induced by the band-to-band tunneling current. In Fig. 3-20, the transfer curves with BTBT model on and off are shown. When the BTBT model is turned off, the drain current remains the same level of 1×10^{-15} A/μm. The impact ionization current is also not induced. The gate cannot control the drain current any more. This proves that the gate-controlled band-to-band tunneling is the working principle of TFET.

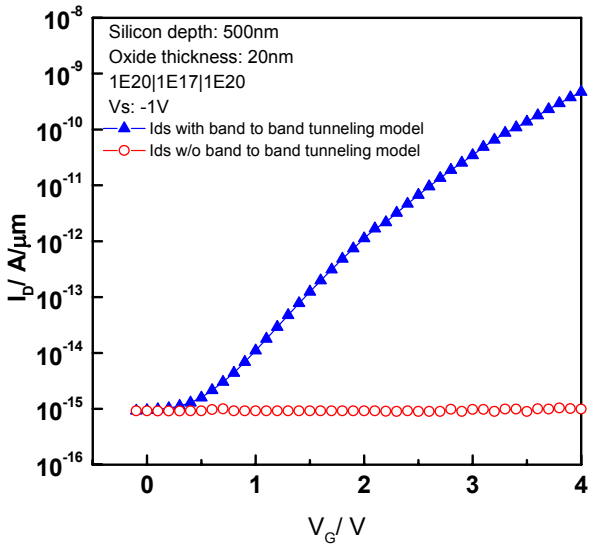


Fig. 3-20 Transfer curves with the BTBT model on and off when V_s =-1V, V_d=0V

3.3.2 Impacts of the gate oxide thickness on NTFET

In the MOSFET technology, the gate oxide thickness is scaled down to improve the gate capacitance. According to the equation 3-14, as the gate oxide thickness decreases, the control ability of gate is improved.

$$I_D = \frac{\mu_n C_{ox} W}{L}\left[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right] = \frac{\mu_n \varepsilon_{ox} W}{L t_{ox}}\left[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right] \quad (3\text{-}14)$$

To investigate the impacts of gate oxide thickness on the performances, NTFETs with gate oxide thickness varying from 3 nm to 30 nm are simulated. Figure 3-14 shows the transfer *I-V* characteristics of NTFETs with the supply voltage of –1V.

As shown in Fig. 3-21, both the threshold voltage (V_t) and the subthreshold swing (S) increase with the increasing t_{ox}. When the gate oxide thickness is 3 nm, the subthreshold swing is nearly 60mV/dec. For the ideal long channel MOSFET, the smallest subthreshold

swing is $\frac{kT}{q}\times\ln(10)\approx 60$ mV. Due to the short channel effects (SCE), the subthreshold swing of sub-100nm MOSFET will be much larger. Because of the different transistor structure and the different working mechanism, the subthreshold slope of TFET can be scaled below the limit of MOSFET. The subthreshold swing of TFET will be discussed in section 3.7.

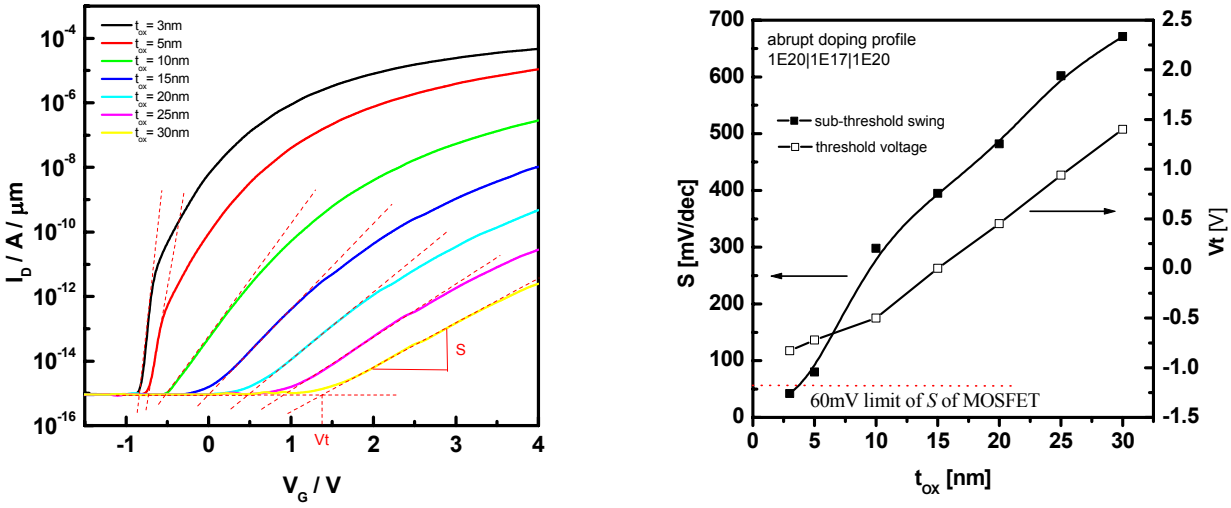


Fig. 3-21 Transfer *I-V* characteristics with the supply voltage of –1V (left); the dependence of subthreshold swing and threshold voltage on t_{ox} (right)

From this simulation, it is clear that decreasing the gate oxide thickness can improve the property of tunneling transistor remarkably.

3.3.3 Impacts of the doping profile on NTFET

Impacts of the doping profile on NTFET performance are investigated in this section. At the beginning of the simulations, the doping profile at the junctions are assumed to be abrupt. A series of NTFET structures with various doping level of source, channel and drain are simulated. Finally, the doping profile at the junctions are assumed to be Gaussian function and the effects of characteristic length in Gaussian function (X.CHAR) are simulated.

3.3.3.1 Characteristics of the NTFET with various source doping levels

In a NTFET, the tunneling junction is at the p^+ source-channel junction. In order to investigate the impacts of the p^+ source doping on the NTFET performance, the NTFET with various source doping levels are simulated. The channel doping concentration is defined as p $1\times10^{17}cm^{-3}$ and the drain doping concentration is n $1\times10^{20}cm^{-3}$ in the simulated transistors. The channel length is 100nm and the gate oxide thickness is 20nm. Varying the source doping concentration, the different transfer curves are simulated. Figure 3-22 shows the dependence of transfer *I-V* characteristics on the source doping of NTFET. When the source doping concentration decreases, the subthreshold swing increases. In the output transfer curves shown in Fig. 3-22, the drive current of NTFET is rather low, when the source doping concentration is below $1\times10^{19}cm^{-3}$. With the heavily p^+ doped source, the drive current can be improved. Therefore, the heavy p doping is necessary for the fabrication of high performance NTFET.

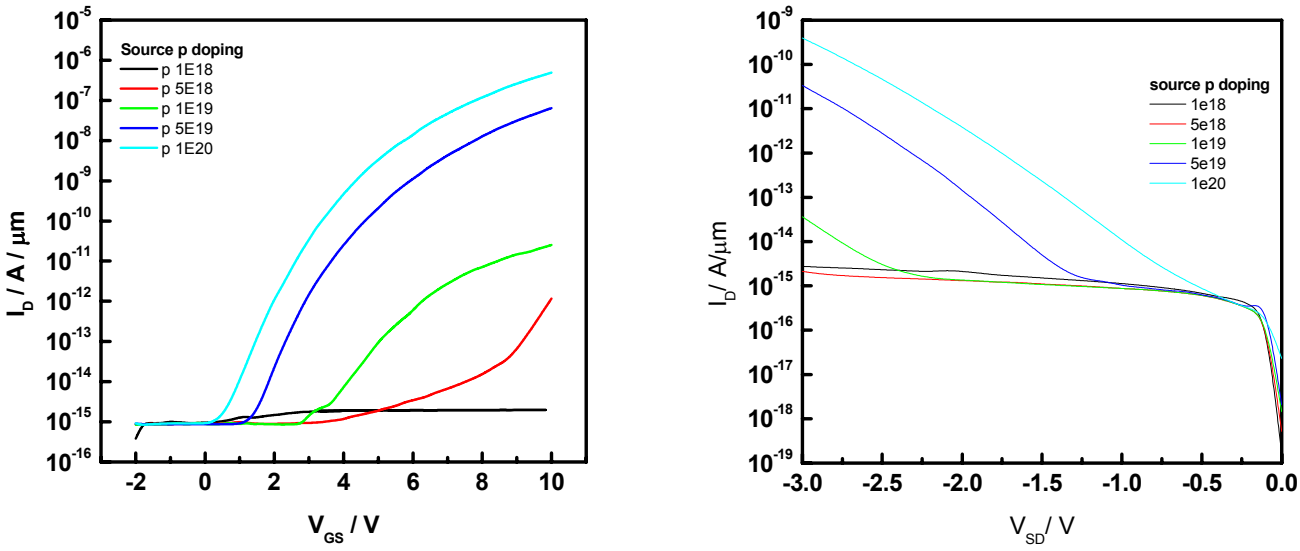
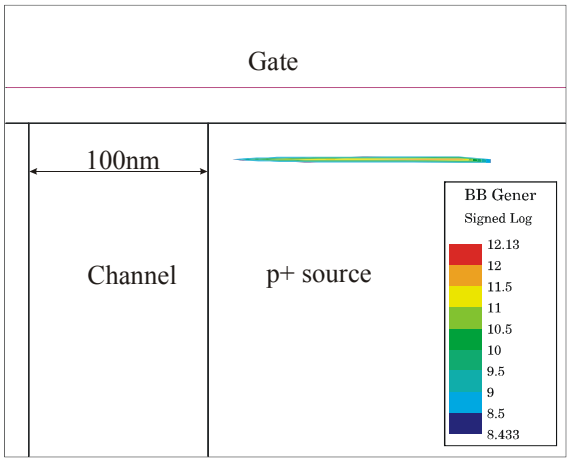
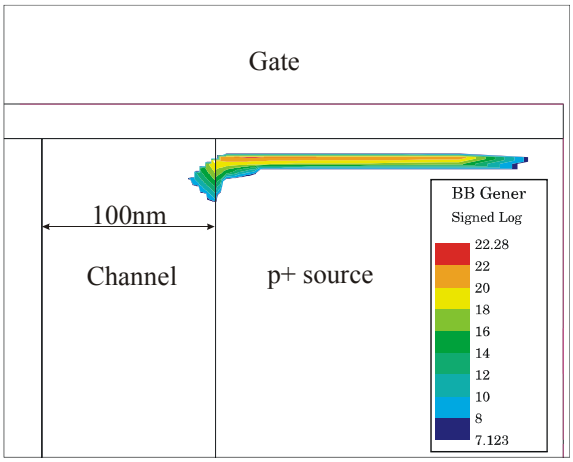


Fig. 3-22 Dependence of the transfer (left) and the output *I-V* characteristics (right) on the source doping of NTFET with V_s = –1V, V_d=0V

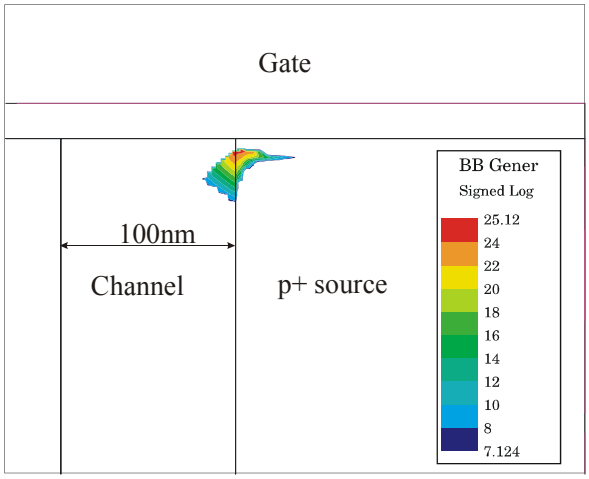
The distribution of the band-to-band tunneling generation rate and the electric field in the tunneling transistors with various source doping concentrations is investigated. Fig. 3-23 lists the contours of BB.GENER in the tunneling transistors with the source doping of p1e18 cm^{-3}, p5e18 cm^{-3}, p1e19 cm^{-3}, p1e20 cm^{-3} when V_s =-1V, V_g =4V. It is found that the tunneling region moves from the inner-source out to the source/channel junction when the source doping level increases. At the same time, the maximum BB.Gener increases from $1.35\times10^{12}cm^{-3}s^{-1}$ to $5.13\times10^{27}cm^{-3}s^{-1}$. The heavily p doped source can provide sharper doping profile at the source/channel junction and the larger tunneling probability. For the lightly doped source, the silicon in the source region can be reversed by the positive gate voltage due to the gate overlap. As a result, the band-to-band tunneling can occur inside the p^+ doped source region. For the heavily doped source, the voltage inside the source region is almost uniform because of the high hole concentration. The electric field is concentrated on the source/channel junction. Thus, the tunneling junction moves out to the source/channel junction.



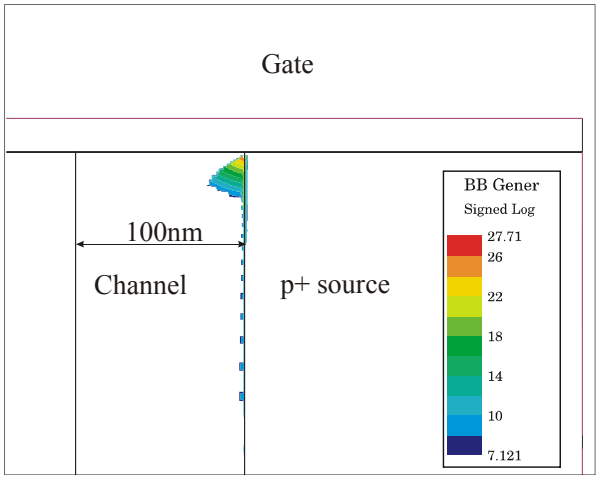
a. source doping level of p 1e18 cm^{-3}



b. source doping level of p 5e18 cm^{-3}

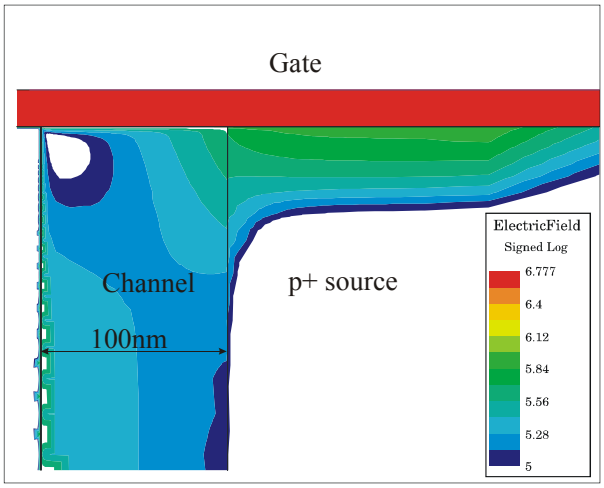


c. source doping level of p 1e19 cm^{-3}

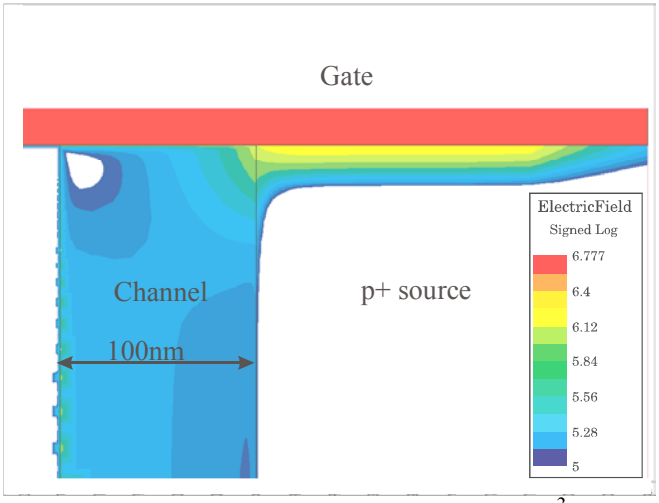


d. source doping level of p 1e20 cm^{-3}

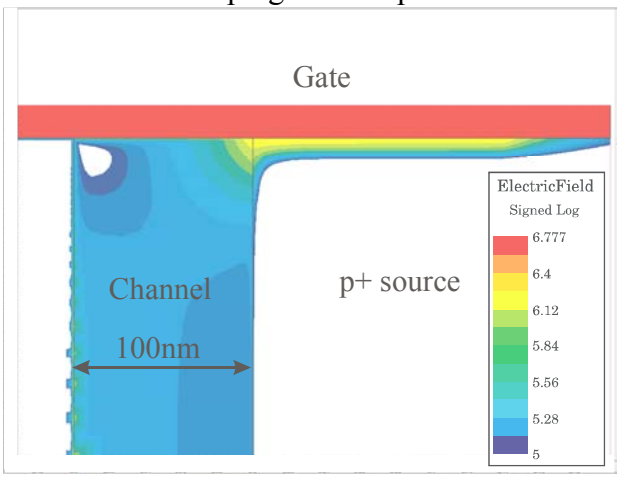
Fig. 3-23 Contour of BB.Gener in the tunneling transistors with the different source doping when V_s= -1V, V_d=0V and V_g =4V



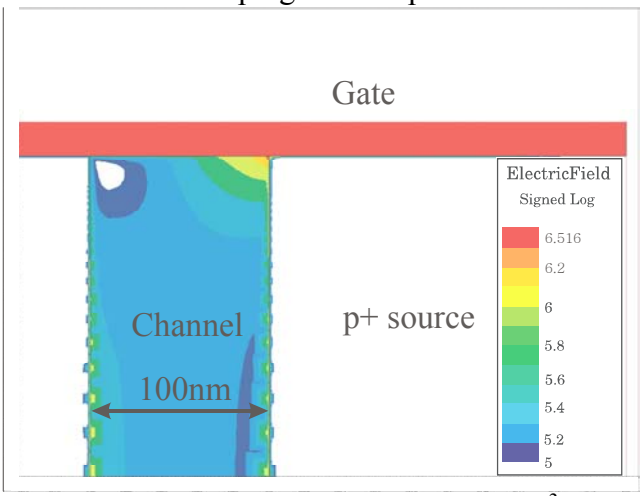
a. source doping level of p 1e18 cm^{-3}



b. source doping level of p 5e18 cm^{-3}



c. source doping level of p 1e19 cm^{-3}



d. source doping level of p 1e20 cm^{-3}

Fig. 3-24 Contour of the electric field in the tunneling transistors with the different source doping when V_s = -1V, V_d=0V and V_g =4V

Fig. 3-24 shows a series of contours of electric field in tunneling transistors with the various source doping levels when V_s = -1V, V_d=0V and V_g =4V. In these pictures, the electric field moves out of source, when the source doping level increases. For the transistor with source doping of $1\times10^{20}cm^{-3}$, the electric fields are concentrated on the oxide/source/channel cross point.

In conclusion, the heavy p doping is needed for high performance NTFET.

3.3.3.2 Impacts of the channel doping level and the channel length on NTFET

3.3.3.2.1 NTFET with various channel doping levels

In the same manner, the tunneling transistors with various channel doping levels are simulated. Figure 3-25 shows the transfer *I-V* characteristics of the tunneling transistors with various channel doping concentrations. With the increasing channel doping level, the leakage current I_{off} increases. In the contour of BB.Gener, the band-to-band tunneling occurs at the channel/drain junction when the gate voltage is zero (Fig. 3-25, right). Thus, this increase of leakage current is caused by the band-to-band tunneling at the source-channel junction. The threshold voltage is increasing when the channel is more p-doped. That means that the channel doping level should be optimized to obtain a preferred threshold voltage and a lower leakage current. Fig. 3-25 shows the simulated transport *I-V* curves for these transistors. The slopes of these curves remain almost the same.

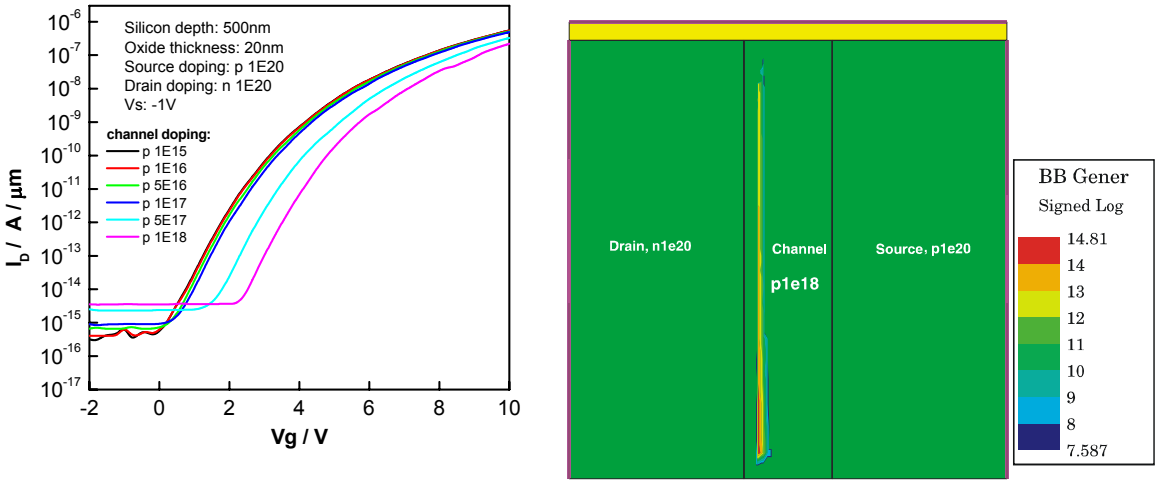


Fig. 3-25 Transfer *I-V* characteristics of the NTFET with different channel doping levels (left), and the contour of BB.Gener in the NTFET with the channel doping of $p1\times10^{18}$ cm^{-3} at V_s =-1V, V_d=0V, V_g =0V (right)

Summarized from the simulated results in this section, the channel doping level determines the drive ability, the subthreshold leakage and the threshold voltage of NTFET.

3.3.3.2.2 NTFET with various channel lengths

Impacts of the channel length on the device performance is of interest for the scaling of the tunneling transistor. When the channel of NTFET is shortened, the electric field in the channel will increase and the tunneling effect may occur without the gate bias. From the transfer characteristics shown in Fig. 3-26.*a*, the leakage current increases rapidly as the channel length decreases. For the NTFET with 30nm channel length, the leakage is only 1 decade lower than the drive current. This result is obtained from the simulation of NTFET with the silicon substrate thickness of 500nm. The leakage current can be remarkably reduced in the double gate thin body structure. As shown in Fig. 3-26.b, the double gate NTFETs with 3nm gate oxide and 20nm silicon thickness are simulated with various channel lengths (see section 3.3.5.1). These transfer characteristics show that the double gate NTFET with 20nm channel length still has much larger current gain than the projected 25nm high performance NMOS in the ITRS roadmap 2002.

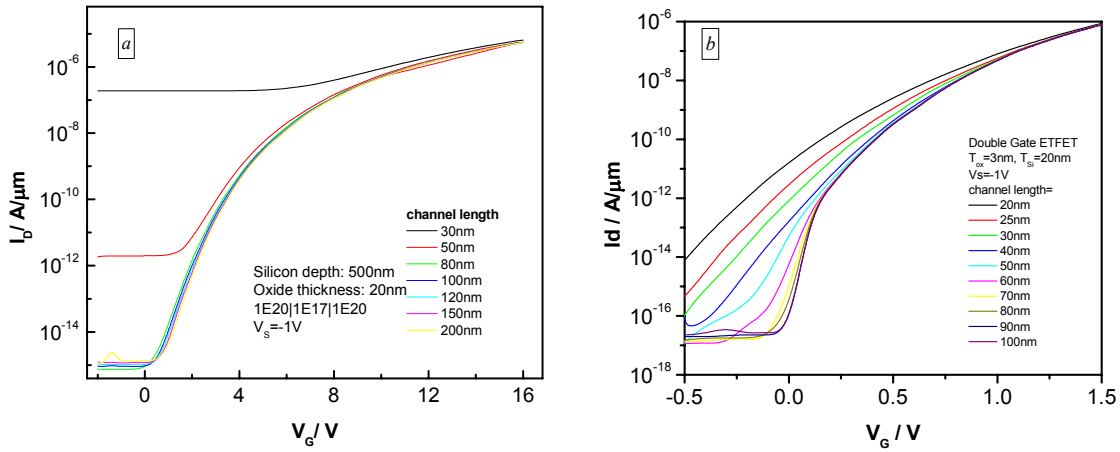


Fig. 3-26 Transfer characteristics of the basic NTFET structure with various channel lengths. (left), silicon body thickness is 500nm; and the transfer characteristics of the double gate NTFET with various channel lengths (right), t_{ox}=3nm and t_{Si}=20nm

3.3.4 Influence of the dopant smear-out on NTFET

As regards the previous simulations, the doping profile at junction is assumed to be abrupt. In this section, the influence of dopant smear-out on the NTFET performance is investigated by varying the smear-out parameters.

The Gaussian doping profile can be specified by X.CHAR or Y.CHAR in MEDICI simulator. The mathematical description of an analytic profile is given by

$$N(x,y) = N.PEAK \cdot a(x) \cdot b(y) \tag{3-15}$$

where *a(x)* describes the lateral doping profile and is given by

$$a(x)=\begin{cases}\exp\left[-\left(\dfrac{x-X.MIN}{X.CHAR}\right)^2\right] & x < X.MIN \\ 1 & X.MIN \le x \le X.MAX \\ \exp\left[-\left(\dfrac{x-X.MAX}{X.CHAR}\right)^2\right] & x > X.MAX\end{cases} \tag{3-16}$$

b(y) describes the vertical doping profile and is given by

$$b(y)=\begin{cases}\exp\left[-\left(\dfrac{y-Y.MIN}{Y.CHAR}\right)^2\right] & y < Y.MIN \\ 1 & Y.MIN \le y \le Y.MAX \\ \exp\left[-\left(\dfrac{y-Y.MAX}{Y.CHAR}\right)^2\right] & y > Y.MAX\end{cases} \tag{3-17}$$

As can be seen in equations 3-16, the lateral doping concentration at $x = X.CHAR + X.MIN$ is decreased to 1/e of the boundary doping concentration at $x = X.MIN$, so does the vertical doping profile. When X.CHAR or Y.CHAR increase, the smear-out effect becomes more significant. We simulated the tunneling transistor with the different X.CHAR values, and the corresponding transfer *I-V* curves are shown in Fig. 3-27.

In Fig 3-27, the device performance deteriorates for the larger subthreshold swing and threshold voltage when X.CHAR increases. The subthreshold slope is 492 mV/dec when X.CHAR is 0nm. It rises to 876 mV/dec when X.CHAR is 16 nm. At the same time, the threshold voltage increases from 0.5V to 3.82V. Therefore, the smear out will degrade the band-to-band tunneling. Therefore, low temperature processes are recommended in the fabrication of high performance TFET.

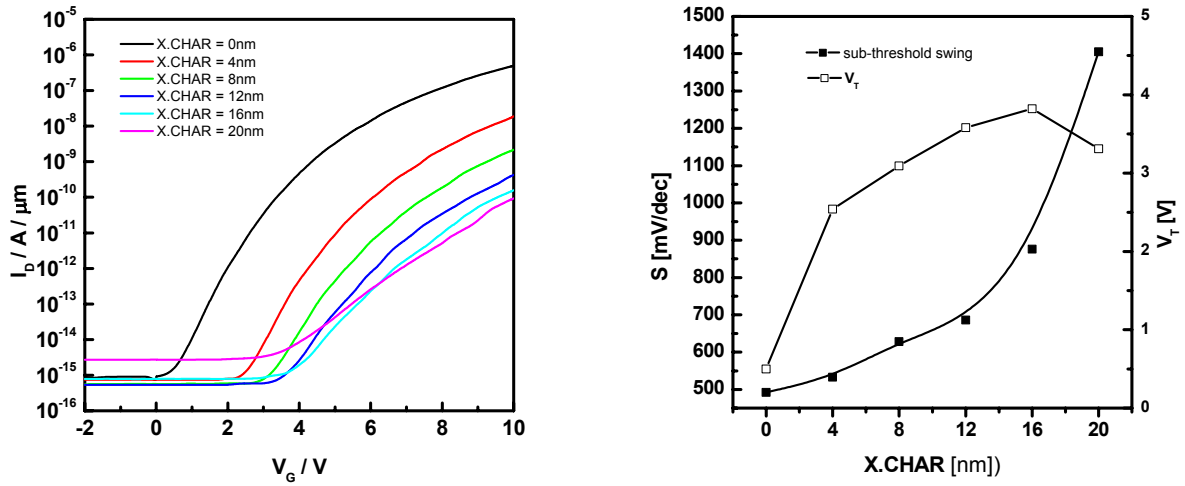


Fig. 3-27 Transfer *I-V* characteristics of the NTFET simulation model with different X.CHAR (left); the dependence of the subthreshold swing and threshold voltage on X.CHAR (right) V_d=0V, V_s =-1V, t_{ox}=20nm

3.3.5 Double gate TFET simulation

In the structural model shown in Fig. 3-13, the tunneling junction in TFET is quite tiny compared to the transistor body. Therefore, the double gate NTFET with the thin silicon body comparable to the tunneling area is simulated in this section. The DG-NTFET characteristics are also compared to the DG-NMOS characteristics.

3.3.5.1 *I-V* characteristics of the double gate NTFET

A double gate TFET is simulated with the BTBT model turned on and the details of the simulated structure are shown in Fig. 3-28. The thickness of thin silicon body (T_{Si}) is 20 nm, the oxide thickness (T_{ox}) is 3 nm, and the gate length (L_g) is 30 nm. The source is heavily p doped and the doping level is $1\times10^{20}cm^{-3}$. The drain is n doped with the doping level of $1\times10^{19}cm^{-3}$. The channel is formed by intrinsic silicon. With the source grounded and the drain positive biased, the simulated transfer *I-V* characteristics of this double gate TFET with the BTBT model turned on are shown in Fig. 3-29. The minimum leakage current can be reduced to 1×10^{-16}A/μm at 1.0 V supply voltage, as can be explained by the band diagram of the off-state TFET. Increasing drain voltage from 0.1 to 1 V, a "DITL" effect as we can see later similar to the DIBL effect in the conventional MOSFET, is observed. The simulated DITL value of this NTFET is 165 mV and the subthreshold swing is 120 mV/ dec. At V_{ds}= V_{gs}=1V, the band-to-band tunneling generation rate and the electron density are plotted in Fig. 3-28.

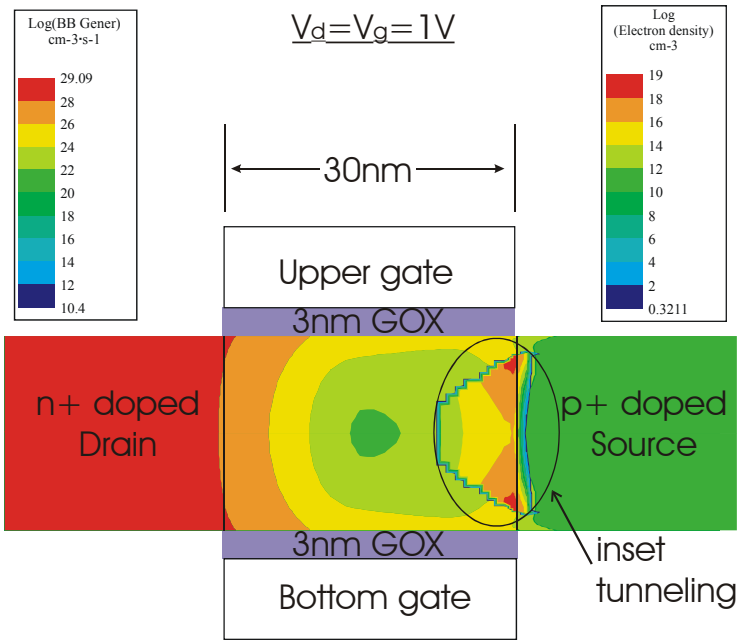


Fig. 3-28 Simulated transistor structural parameter and the contours of band-to-band tunneling generation rate and electron density in the double gate NTFET

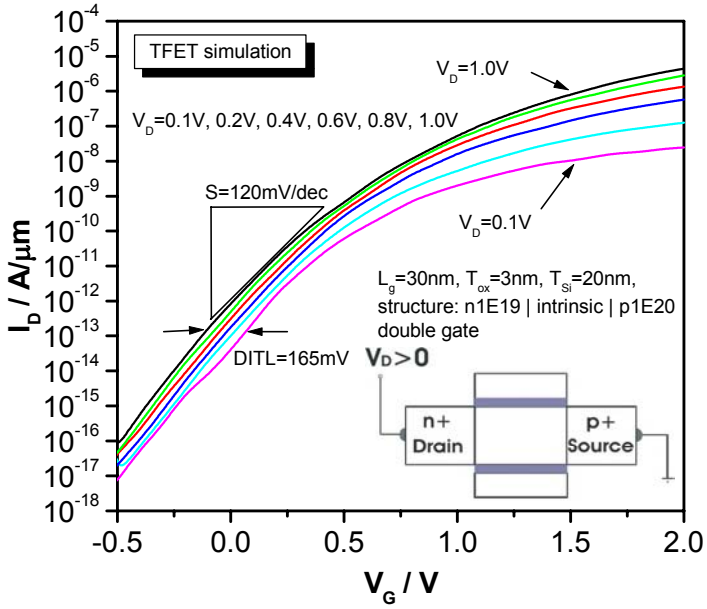


Fig. 3-29 Transfer characteristics of the proposed double gate NTFET with V_{ds} as differing parameter

3.3.5.2 Scaling prospect of the double gate NTFET

Because of the 10nm active region of the tunneling effect shown in Fig. 3-28, the channel length of this transistor should be able to be scaled down to at least 20nm (Fig. 3-26, right). In order to find out the effects during the scaling of TFET, we simulated the double gate TFET and the double gate NMOS with various gate lengths from 100nm to 20nm for comparison. We defined two groups of structures: T_{ox} = 1nm for the structures with T_{si} = 10nm and T_{ox} = 3nm for T_{si} = 20nm. The comparison of V_t roll-off effects in TFET and MOSFET is shown in Fig. 3-30. Our MOSFET simulations are compared to the published data from Wong *et al.* [ref. 32] for confidence. Because of the charge-sharing effect, V_t rolls off with the decreasing channel length in NMOS. It can be seen from the simulation that the V_t roll-off problem can be reduced by using thinner silicon body and thinner gate oxide. Similar to MOSFET, the V_t roll-off effect is observed in TFET. However, the change in the threshold voltage of TFET with the different channel lengths is much smaller. The reason is that the threshold voltage of TFET depends on the band bending in the small tunnel region, but not in the whole channel region. The comparison of DIBL effects of NMOS and DITL of TFET is shown in Fig. 3-31. The high DITL-effect for any channel length in TFET is the disadvantage of TFET.

The minimum leakage current of TFET is also compared to that of NMOS in Fig. 3-32. The significant increase in the leakage current of NMOS with decreasing gate length results from the increasing band-to-band tunneling at the drain-channel junction. The leakage of TFET is much smaller because of the larger barrier of the reversed p-i-n junction.

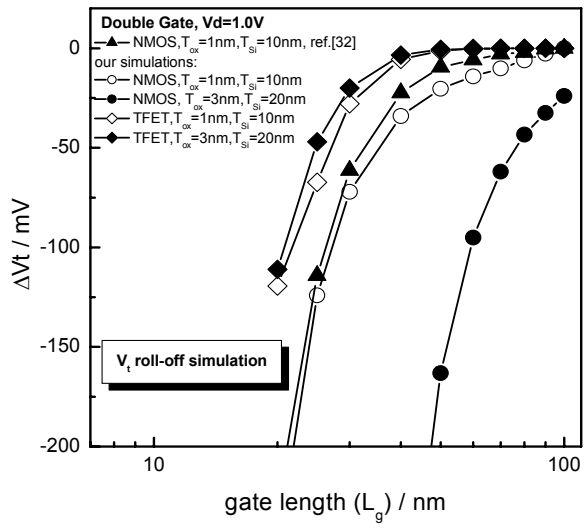


Fig. 3-30 Comparison of V_t roll-off in the double gate TFET and double gate NMOS

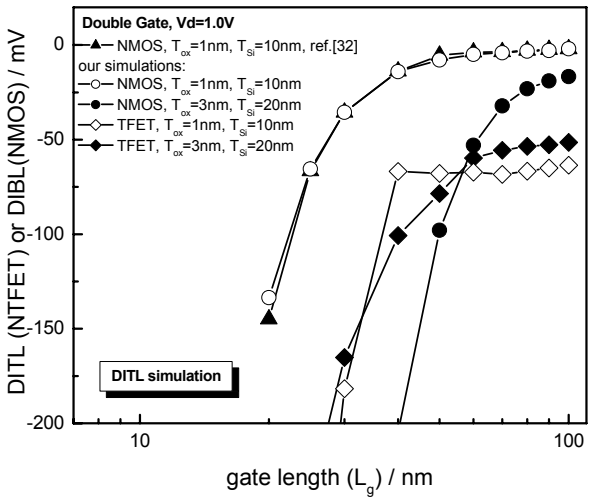


Fig. 3-31 Comparison of DITL in the double gate TFET and the DIBL of double gate NMOS

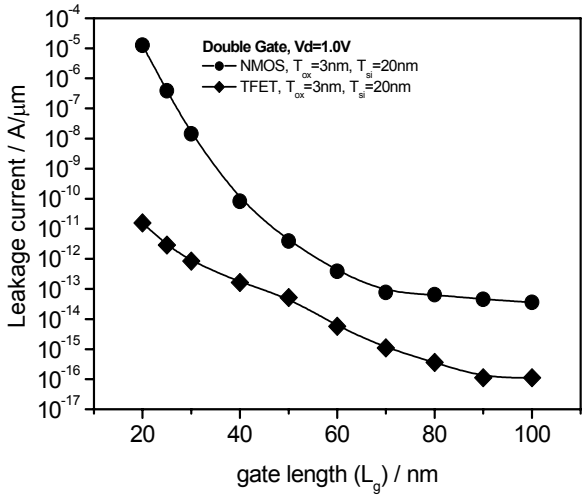


Fig. 3-32 Comparison of the leakage current of the double gate TFET and the double gate NMOS, T_{ox}=3nm

3.4 TFET Process simulation

In order to find out the best conditions for the device fabrication, the process simulations of TFET are performed using the SUPREM simulation. The SUPREM simulator is a process simulation program provided by AVANTI corporation. The simulation of ion implantation, inert ambient drive-in, silicon and polysilicon oxidation and silicidation, epitaxial growth, low temperature deposition, and etching of various materials is possible in this simulator.

3.4.1 Simulation of vertical MBE-TFET

The NTFET fabricated in Uni-Bw München using the MBE method [13-16] is shown in Fig.1-6 and is simulated first. The simulation processes for this TFET are shown in Fig. 3-33. In this simulation, first the n^+ doped silicon substrate is defined. Then, the MBE layers are grown on the substrate at 700°C to form the channel layer, the delta-doping layer, and the drain region. Then, the mesa etching is done to form the silicon pillar. The following processes are the gate oxidation, the poly-si gate deposition, the gate patterning, the Si_3N_4 deposition, and the metallization. The fabrication process sequence is summarized in Fig. 3-34.

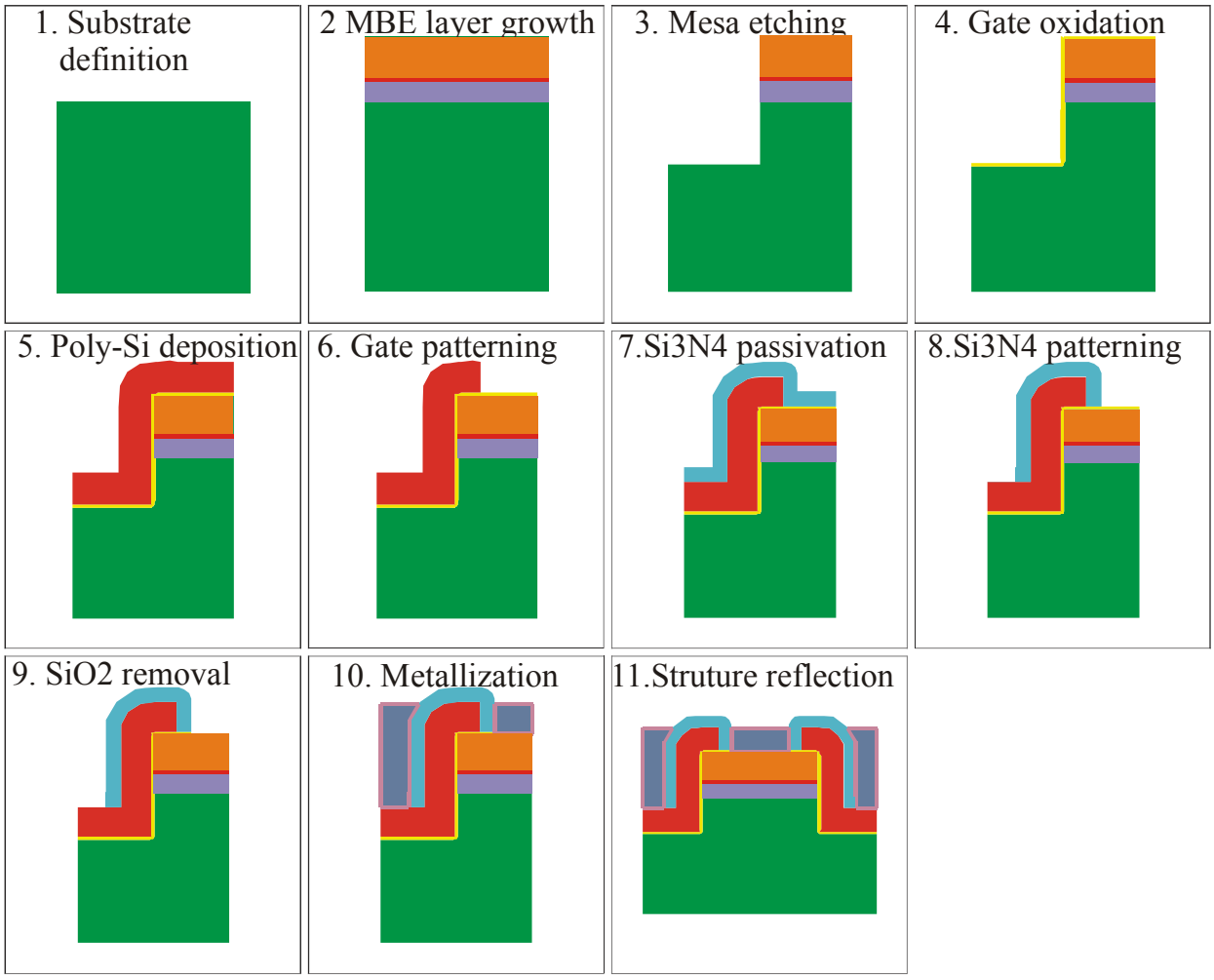


Fig. 3-33 SUPREM simulated TFET fabrication processes

It is found that the doping profile changes due to the high temperature processes. As shown in Fig. 3-35.a, there is a delta doping layer after layer growth. However, this delta doping layer has nearly disappeared after the final process (Fig. 3-35.b). At the same time, the physical channel length decreases from about 90nm to 60nm. The doping profile changes because of the doping redistribution during the high temperature process, which affects the performance of the transistor significantly. As discussed before, the decrease in channel length will induce the increase of the leakage current. Meanwhile, the dopant smear-out will degrade other

electrical properties, such as subthreshold swing and drive current. The redistribution of dopant can be reduced using the small thermal budget processes, such as the low temperature MBE [33-35], the low temperature gate dielectric growth using PECVD or ALCVD [36], and the rapid thermal processing [37].

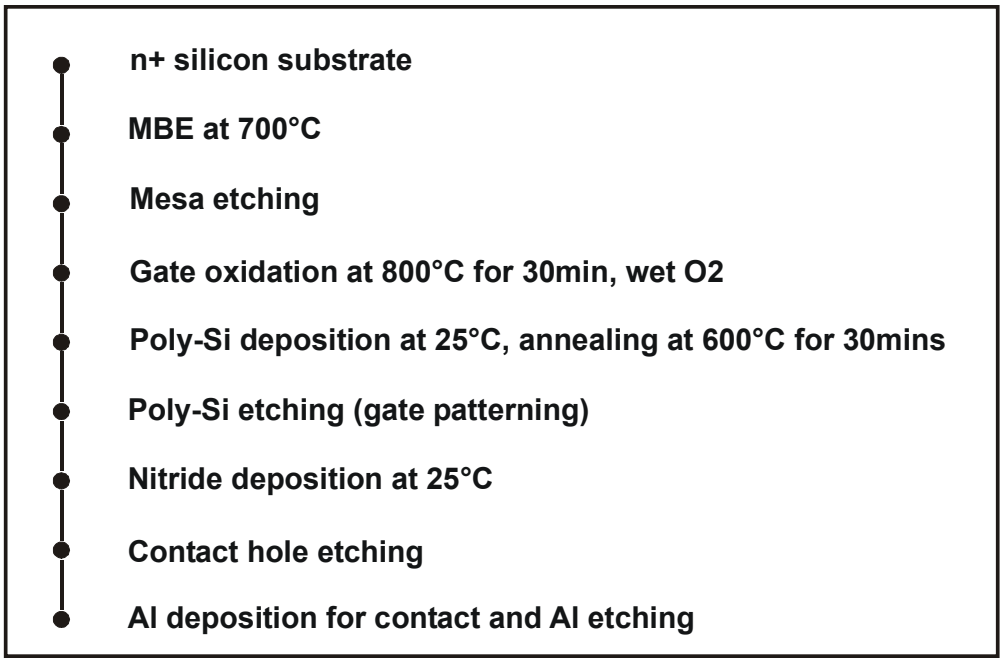
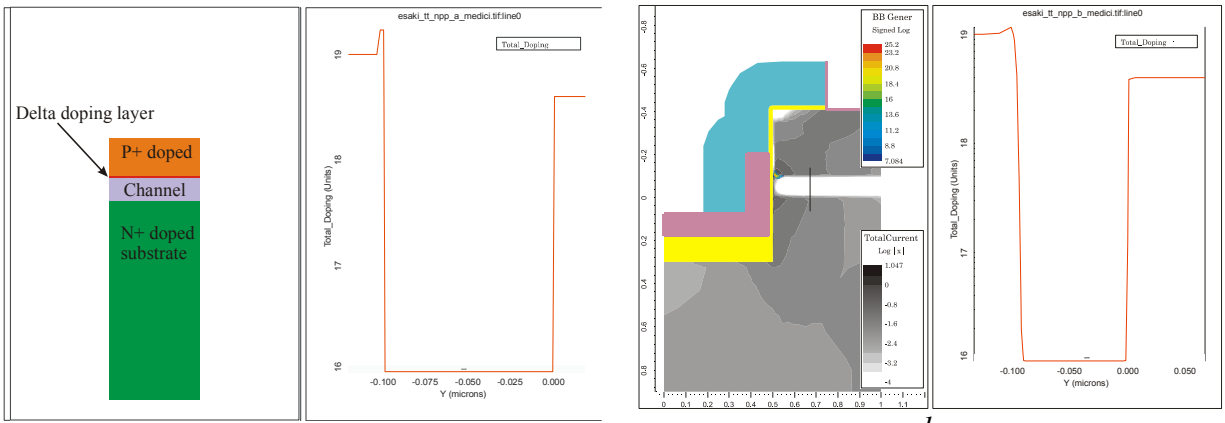


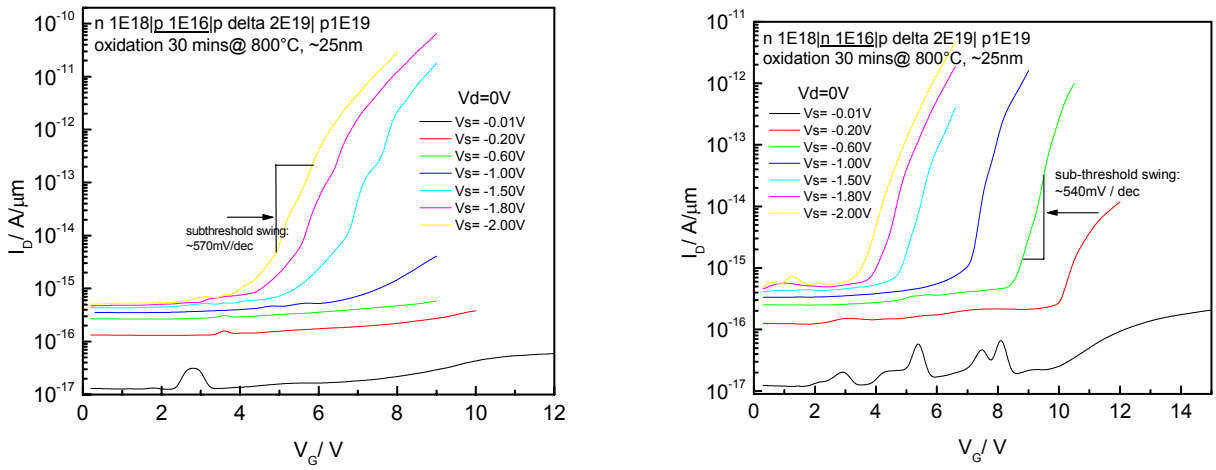
Fig. 3-34 Process sequence of the MBE-TFET fabrication



a *b*

Fig. 3-35 Doping profile after MBE layer growth(*a*) and the doping profile after the final process (*b*) along the vertical cutline

The corresponding transfer characteristics of the transistors with the p or n doped channel are shown in Fig. 3-36. The threshold voltage TFET with the n-doped channel is lower than that of p-doped channel. That means that the threshold voltage can be adjusted by adjusting the channel doping. The limited drive current in these TFETs result from the $1\times10^{19}cm^{-3}$ source doping level which is not high enough.



a *b*

Fig. 3-36 Simulated transfer characteristics of the MBE-TFET with the p type 1×10^{16} cm^{-3} doped channel (*a*) and the n type $1\times10^{16}cm^{-3}$ doped channel (*b*)

3.4.2 Impacts of the oxidation process on the MBE-TFET

The oxidation process is very important in the fabrication of TFET. In this section, the impacts of oxidation on the performance of TFET is investigated by simulation.

In the SUPREM simulator, the oxidation process is specified by defining an oxidizing ambient in a "DIFFUSION" statement. The oxidizing ambient can be O_2, H_2O, or N_2O. Oxidation in the SUPREM simulator is based on the theory of Deal and Grove [38]. The flux of oxidant entering the oxide from the ambient is described as:

$$\vec{F} = h(C^* - C_o)\vec{n}_s \tag{3-18}$$

where h is the gas-phase mass-transfer coefficient, C_o is the concentration of oxidant in the oxide at the surface, $C^* = HP_{ox}$ where H is the Henry's law coefficient for the oxidant in oxide and P_{ox} is the partial pressure of oxidant in the ambient.

The oxide growth rate can be calculated using the following equation:

$$\frac{d\vec{Y}}{dt} = \frac{\vec{F}}{N_1} + r_{thin} \tag{3-19}$$

where $d\vec{Y}/dt$ is the oxidation rate, N_1 is the number of oxidant molecules to form one cubic centimeter oxide. r_{thin} correponds to the rapid growth occur during the first stage of oxidation. Calculating equation 3-18 and 3-19 at each node of the mesh, oxidation can be simulated by the numerical method. There are four types of numerical oxidation models in the SUPREM simulator. They are VERTICAL, COMPRESS, VISCOUS, and VISCOELA. The VERTICAL model is the most simple because only the oxidation in the y direction is simulated. In our simulation, the VISCOUS model is used. The VISCOUS model simulates

the viscous flow of oxide during the oxidation by calculating the 7-nodes finite elements. This model allows accurate stress calculation.

In Fig. 3-37, the NTFETs with different oxidation conditions are simulated. Using a shorter oxidation time and a lower oxidation temperature, a better performance can be obtained. The reason is that the doping profile has great dependence on the thermal processing. Reducing the oxidation thermal budget is a good solution for suppressing the dopant redistribution. In Fig. 3-38, the doping profile changes a lot before and after wet oxidation of 30 minutes at 800°C. The physical channel length of TFET decreases from 90nm to 60nm (the defined channel length is 100nm). That is almost the same to the change in physical channel length shown in Fig. 3-38, where the doping profile after the final process is shown. Hereby, the redistribution of dopant mostly results from the gate oxidation process. With a higher temperature, the oxidation rate increases rapidly and the out diffusion of dopant becomes more significant. If the oxidation temperature is reduced to 700°C, the doping redistribution effect will be suppressed. In Fig. 3-39, almost no smear-out is observed after 20 minutes wet oxidation at 700°C. In this simulation, the quality of low temperature grown gate oxide is not considered. This simulation just shows the tendency of TFET performance with thinner oxidation and smaller thermal budget.

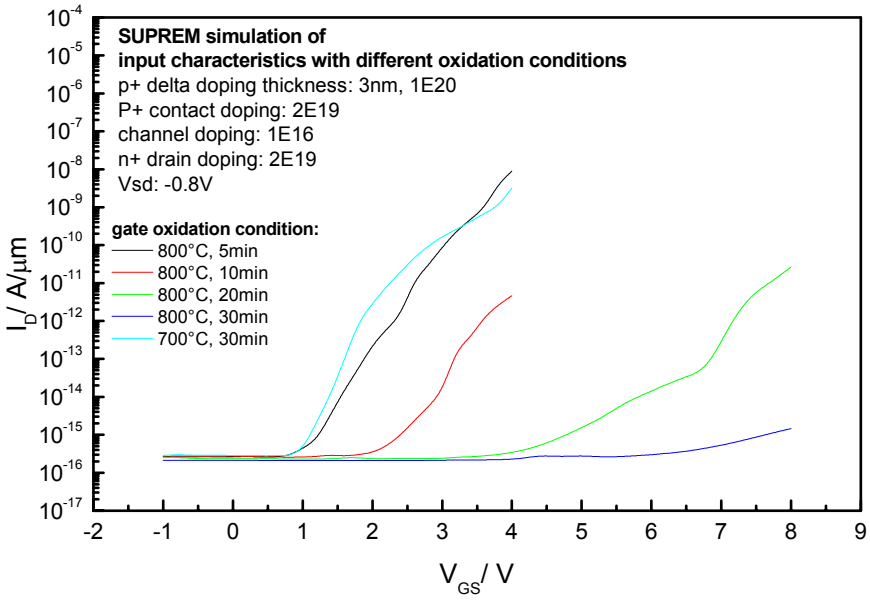
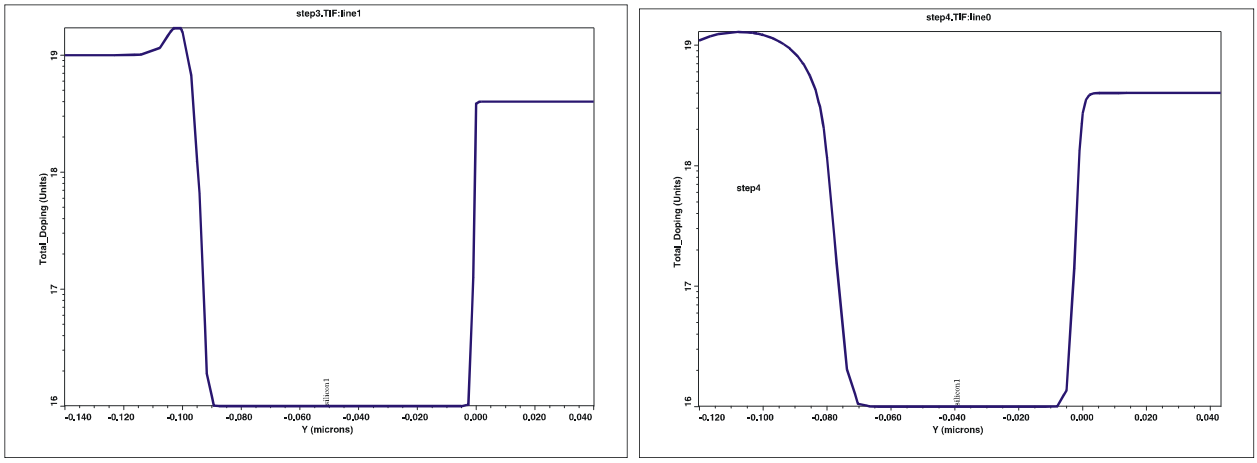


Fig. 3-37 Simulated performance of the MBE-TFET with the different oxidation conditions



a. Doping profile before oxidation. The physical channel length is about 90nm.

b. Doping profile after gate oxidation for 30 min. at 800°C. The physical channel length is about 60nm.

Fig. 3-38 Comparison of the doping profile before and after oxidation for 30 min. at 800°C

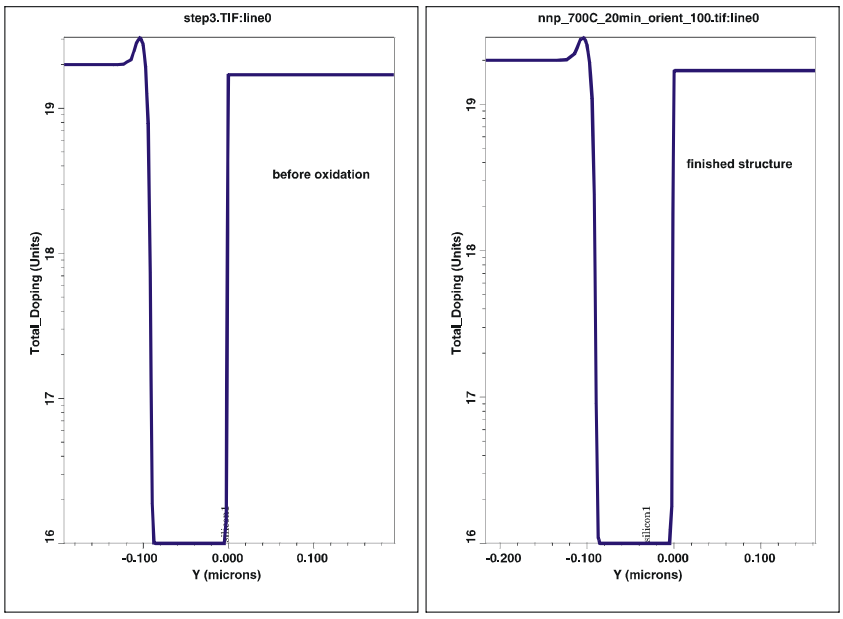


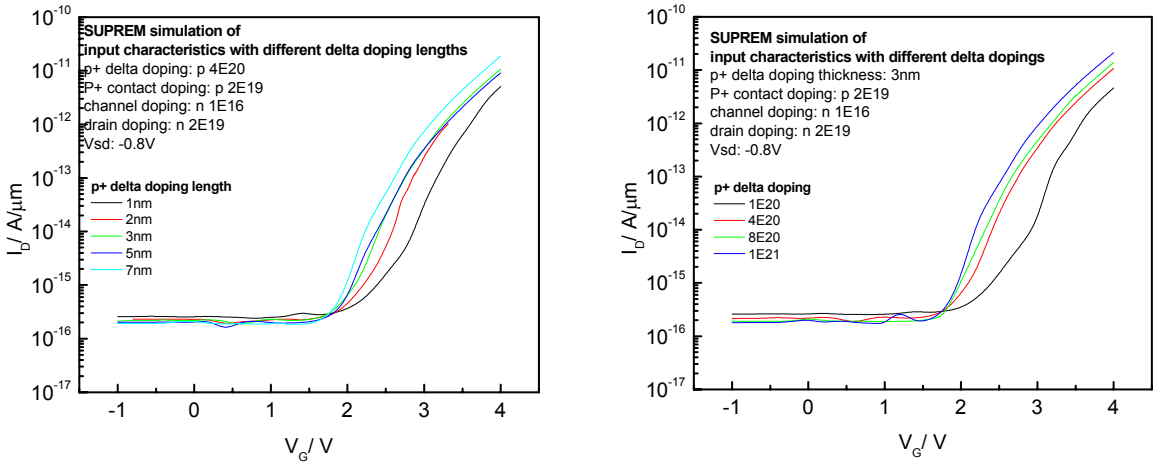
Fig. 3-39 Comparison of doping profile before and after oxidation for 20 min. at 700°C

3.4.3 Impacts of the delta doping layer on the MBE-TFET performance

The heavily doped delta doping layer is popular in the fabrication of the resonant tunneling diodes [39]. In this technology, a very thin (few nanometer) and heavily doped layer is grown. It is also proposed that this layer may improve the performance of vertical TFET [15]. In this section, the impact of the delta doping layer on the performance of vertical TFET will be investigated by simulation.

As shown in Fig. 3-35.a, the delta doping layer is between the channel region and the p^+ doped region. The TFETs with various delta doping layer thickness and doping levels are simulated here. The gate oxidation is done at 800°C for 10 minutes by wet oxidation. The

transfer characteristics of these TFETs are shown in Fig. 3-40. Although the performance can be improved by increasing the delta doping level and thickness, the improvement is very limited. The reason is that the thermal oxidation will degrade the delta doping layer. Therefore, the delta doping layer must be protected using low thermal budget processes.



a *b*

Fig. 3-40 Performance of the MBE-TFETs with various delta doping layer thicknesses (*a*) and doping levels (*b*) after gate oxidation

3.4.4 Impacts of n^+ drain doping level on NTFET

The impacts of n^+ doping level on the performance of NTFET are simulated. As shown in Fig. 3-41, the influence of n^+ doping level on the performance is rather small. Thus, the n^+ doping region is not as important as the p^+ doped region for NTFET. The heavily n doped region is necessary for the ohmic metal-semiconductor contact at the drain of TFET.

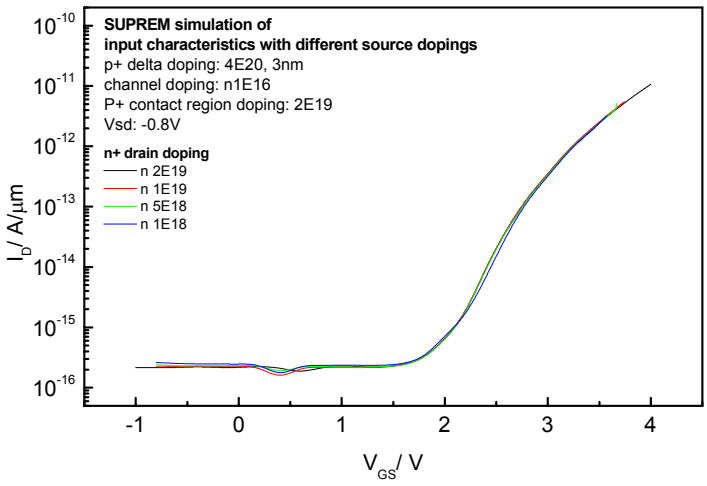
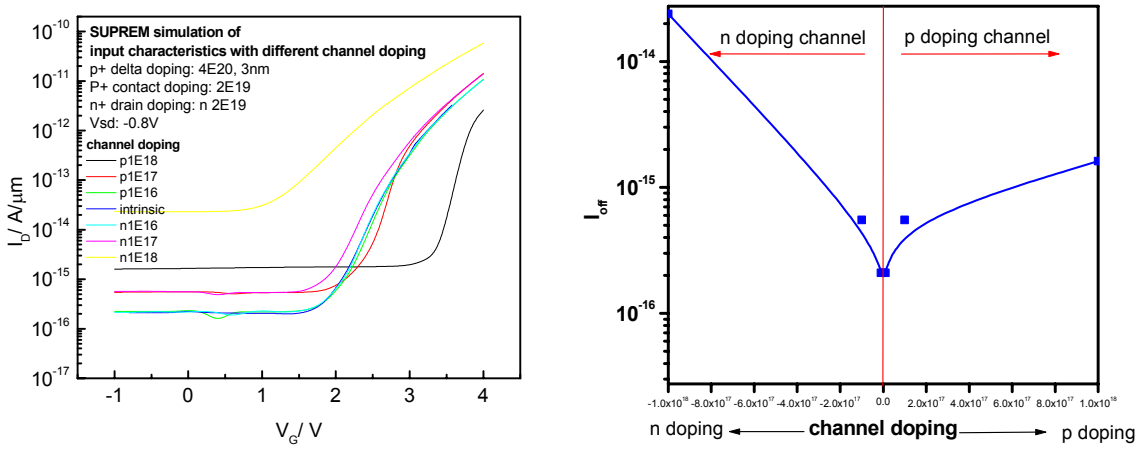


Fig. 3-41 Performance of the MBE-TFET with various n^+ drain doping levels

3.4.5 Impacts of the channel doping on the MBE-TFET

The different MBE-TFETs with various channel doping levels are simulated. The corresponding transfer characteristics are shown in Fig. 3-42. The NTFET with the n doped channel has lower V_t than the p doped channel NTFET. The leakage current increases, when the channel doping level rises.



a *b*

Fig. 3-42 Transfer characteristics of the MBE-TFET with various channel dopings (a); the leakage current of the MBE-TFET with various channel dopings (b).

3.5 Study of tunneling in the simulated MBE-TFET

3.5.1 Two types of tunneling in the MBE-TFET

The doping smear-out will result in the doping redistribution. Therefore, in the SUPREM simulation, the band-to-band tunneling region will be quite different from the device simulated by the MEDICI simulator (without process simulation). Using the process simulation, two types of tunneling are found in the vertical NTFET fabricated using the MBE method. The structural parameters of this simulated NTFET are shown in table 3-3.

Table 3-3 Details of the structure and process

Structure	Doping profile	Models used for calculation
Oxide thickness: 6 nm, oxidation 5min. at 800°C	Drain: n^+ 4E18 cm^{-3}	CONMOB FLDMOB SRFMOB2 CONSRH BTBT IMPACT.I
	Channel : 80nm, n 1E16cm^{-3}	
Silicon Pillar Width: 1000nm	Source: 300nm, p^+ 2E19cm^{-3}	
	Delta doping: 3nm, p^+1E20cm^{-3}	

According to the simulated transfer *I-V* character in Fig. 3-43, the drain current increases from 3×10^{-16} A/μm to 5×10^{-7} A/μm when V_g increases from 1V to 5V. The drain current seems to rise by two steps, which is also observed in the experimental device fabricated in ref. [40]. The band-to-band tunneling contours are shown in Fig. 3-44. With V_g varying from 1V to 3V,

the tunneling occurs at the boundary of p^+ source and n-channel (Fig. 3-44.a). This kind of tunneling is named as the "point tunneling". As V_g increases from 4V to 6V, the tunneling occurs inside of the p^+ drain region (Fig. 3-44.b). In this case, we define this kind of tunneling as the "line tunneling". Both the "point tunneling" and the "line tunneling" are the gate-controlled band-to-band tunneling.

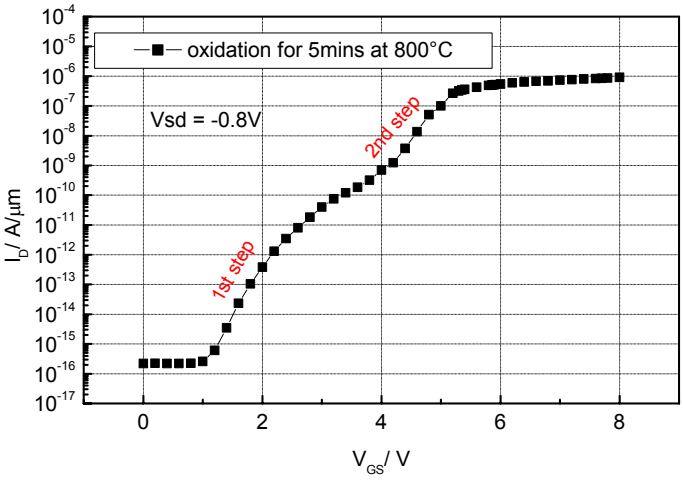
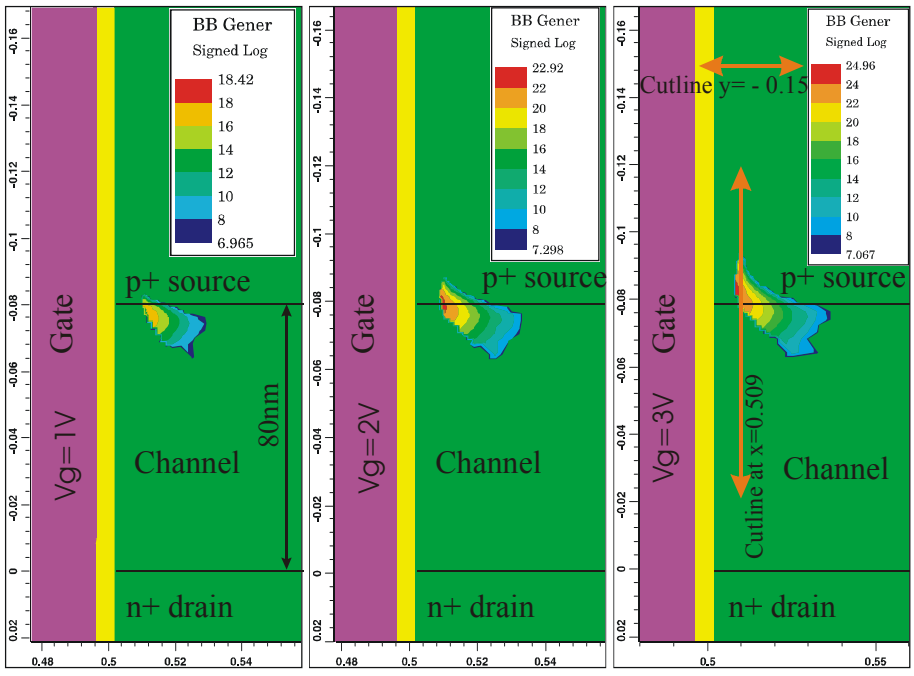
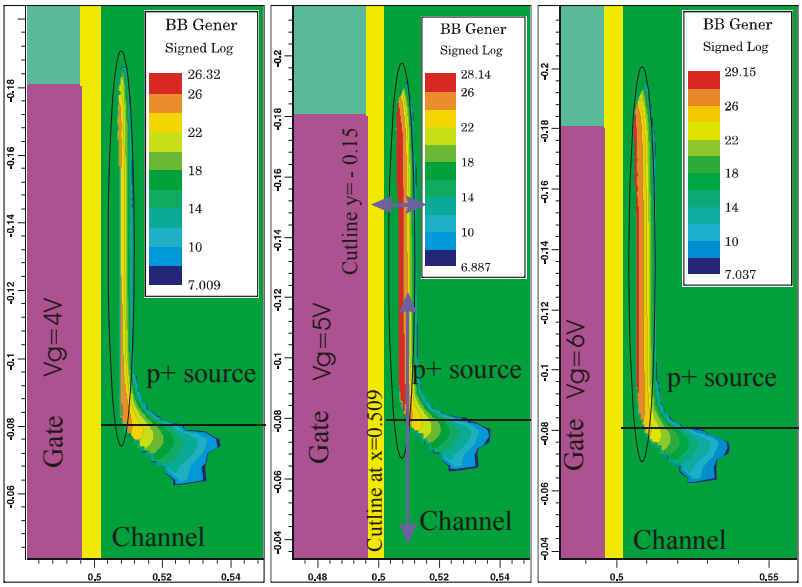


Fig. 3-43 Transfer *I-V* characteristics at V_{sd} = -0.8V in the simulated transistor

The band diagrams are plotted in Fig. 3-45 to illustrate these two kinds of tunneling in this transistor. As shown in Fig. 3-45.b, the band diagram at V_g =3V, V_s =-0.8V indicates that there is almost no line band-to-band tunneling. The band diagrams for the point tunneling at V_g =3V and 5V (Fig. 3-45. a and c) change only a little bit, while the band diagrams (Fig. 3-45. b and d) for the line tunneling change a lot.

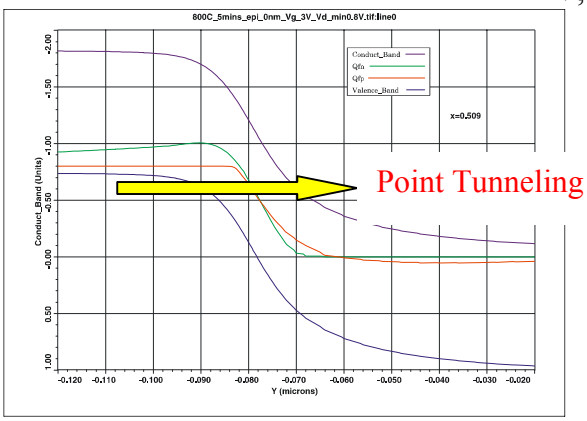


a

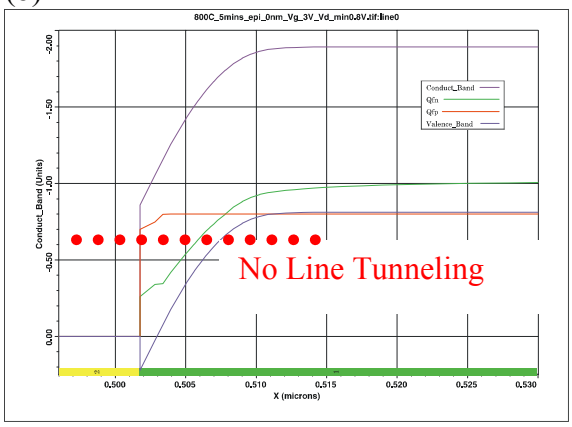


b

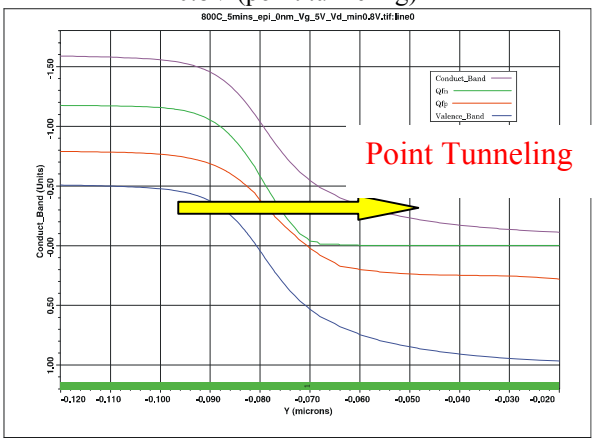
Fig. 3-44. Contour of BB.GENER at V_{sd}=-0.8V, V_g =1V, 2V, 3V (a) and at V_{sd}=-0.8V, V_g =4V, 5V, 6V (b)



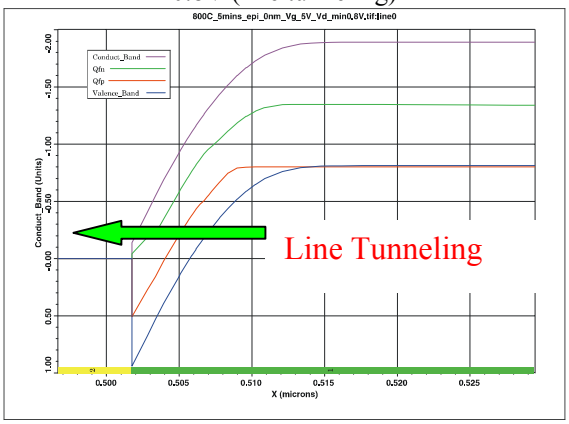
a. Band diagram along cutline at x=0.509 when V_g=3V, V_{sd}=-0.8V (point tunneling)



b. Band diagram along cutline at y=-0.15 when V_g=3V, V_{sd}=-0.8V (line tunneling)



c. Band diagram along cutline at x=0.509 when V_g=5V, V_{sd}=-0.8V (point tunneling)



d. Band diagram along cutline at y=-0.15 when V_g=5V, V_{sd}=-0.8V (line tunneling)

Fig. 3-45 Band diagrams along the cutline at x=0.509 for the point tunneling and the band diagrams along the cutline at y= -0.15 for the line tunneling. The TFET structure can be seen in Fig. 3-33

3.5.2 Application of the "line tunneling" in the vertical NTFET

It is possible to enhance the "line tunneling" in the MBE-TFET by growing a epitaxial intrinsic layer on the mesa. The details of this new structure for simulation are listed in table 3-4. As shown in Fig. 3-46, an additional epitaxial intrinsic layer is grown after the mesa etching. The thickness of the epitaxy layer is varied from 8nm to 12nm. In this transistor, the "line tunneling" in the p^+ doepd source is enhanced due to the junction formed by the n^+ strong inversion channel and the p^+ region. The transfer characteristics with various additional exitaxy layer thickness are shown in Fig. 3-47. As the thickness of the extra epitaxy layer increases, the drain current curve becomes smooth and the subthreshold swing is improved. However, the on-current of this TFET is decreased.

Table 3-4 Details of the proposed structure with an additional epitaxy intrinsic layer grown after the mesa etching

Structure	Doping profile	Models used for simulation
Oxide thickness: 6 nm, oxidation 5min. at 800°C	Drain: n^+ 4e18	CONMOB FLDMOB SRFMOB2 CONSRH BTBT IMPACT.I
	Channel : 80nm, n 1e16	
Epi-Si: 0-12nm	Source: 300nm, p^+ 2e19	
Silicon Pillar Width: 1000nm	Delta doping: no delta doping	

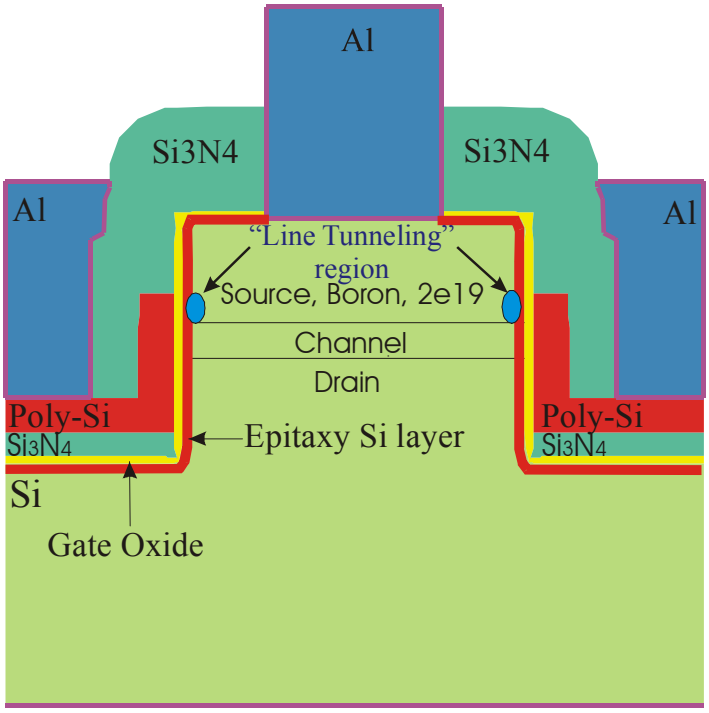


Fig. 3-46 Proposed structure with an additional epitaxial intrinsic layer grown after the mesa etching

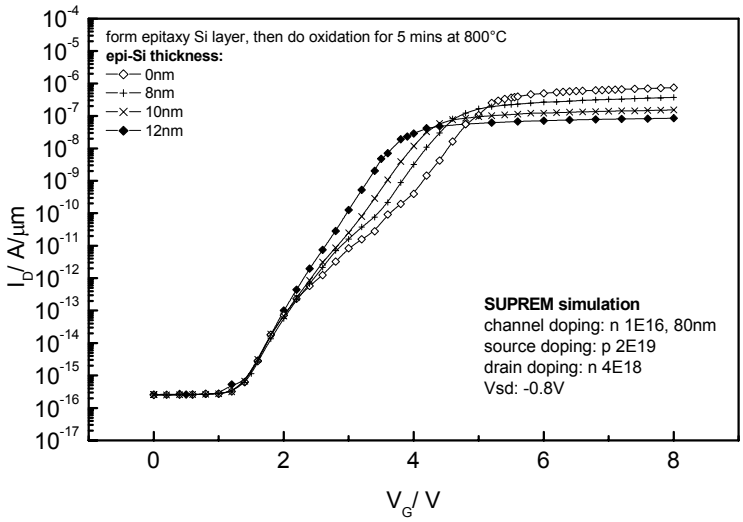


Fig. 3-47 Transfer characteristics with various additional epitaxial layer thickness

3.5.3 Impacts of G-S overlap on the performance of MBE-TFET

In the MBE-TFET simulated before, almost all the p^+ doped source areas are covered by the gate. In order to find out the impacts of G-S overlap on the DC performance of TFET grown by the MBE technology, the transistors with various G-S overlap lengths are simulated by the 2-D simulator. The performances of these transistors are shown in Fig. 3-48. It can be seen that the drive ability is improved by increasing the G-S overlap area. The reason is that the "line tunneling" current increases, when the larger p^+ doped source region is covered by the gate.

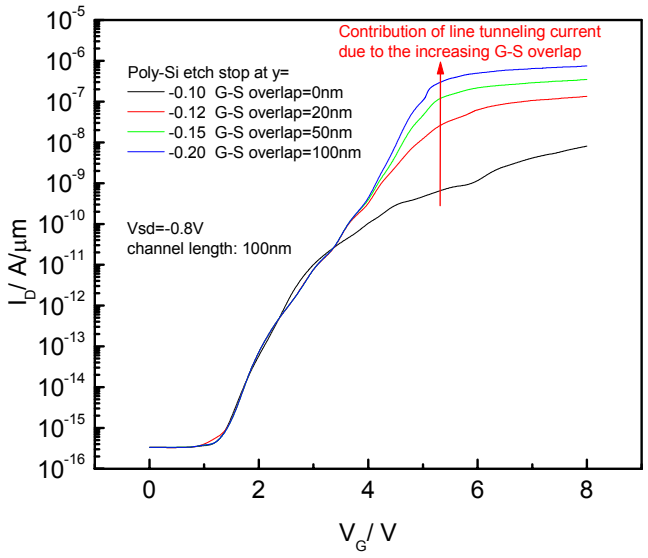


Fig. 3-48 Performance of the MBE-TFET with various G-S overlap lengths

3.6 Simulation of the planar TFET fabricated by diffusion doping

TFET can also be fabricated using the diffusion doping method. The heavily n or p doped region can be formed first by the out-diffusion of the SOD layer. Compared to the MBE doping method, the p surface doping concentration obtained by diffusion is very high (e.g. $2.8 \times 10^{20} cm^{-3}$). In this fabrication process, the starting material is intrinsic doped silicon which is used as the substrate. The n^+ diffusion is performed before the p^+ diffusion in order to limit the smear-out of p dopant. The oxidation process is done after all the diffusion processes. The channel length is 1μm and the gate oxide thickness is 4.2 nm to compare with the experimental devices. Using SUPREM and MEDICI simulation, the transfer characteristics of the planar TFET are obtained. As shown in the simulated transfer characteristics of the planar TFET with the spin on doping process (Fig.3-49), the drain current can be controlled by gate voltage. Compared to the simulated TFET using the MBE doping method, both the leakage current and the drive current of this TFET is higher. The drive current is higher due to heavy p^+ doping concentration. In Fig. 3-50, the contour of BTBT generation rate and electron density are shown. The maximum BTBT generation rate under the gate is 7.94×10^{30} $cm^{-3}s^{-1}$. This simulation shows that TFET can also be fabricated using the diffusion doping method. For the advantages of the heavy p dopant concentration and the compatibility to the CMOS technology, the planar TFET is of great interest for this investigation.

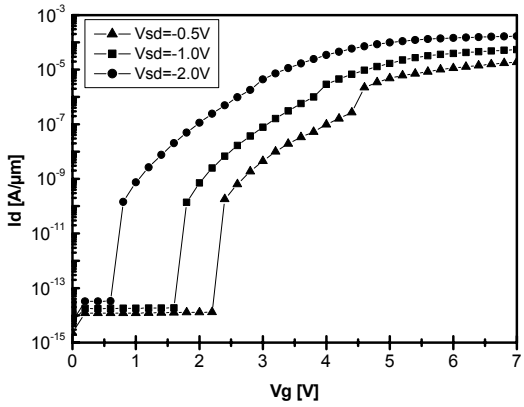


Fig. 3-49 Simulated transfer characteristics of the planar TFET with the SOD process. (Using the connection configuration *c* in table 3-1)

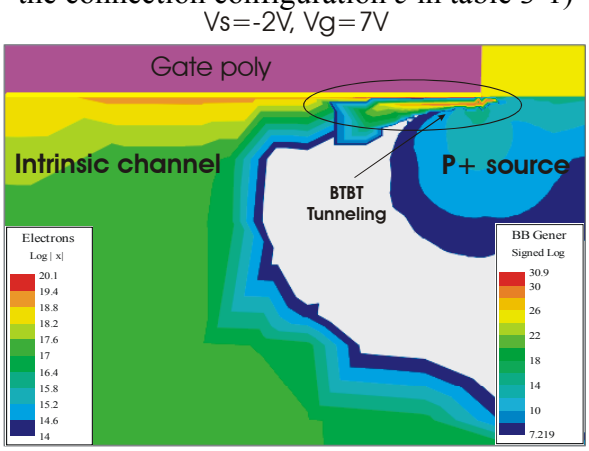


Fig. 3-50 Contour of the BTBT generation rate and the electron density in the on-state planar TFET with the SOD process. t_{ox} = 4.2nm. (the channel length is 1μm)

3.7 Subthreshold swing in TFET

The subthreshold swing (*S*) is an important property of TFET. The smaller *S*, the better dynamic performance. Due to the mechanism of tunneling, TFET may has a smaller *S* than ln(10)·KT/q which is the best *S* value of MOSFET.

The double gate NTFET with the 100nm channel length and the 3nm gate oxide thickness is simulated. The drain is n^+ doped with the doping level of 1×10^{19} cm^{-3} and the p type source doping level is $1\times10^{20}cm^{-3}$. The TFET structure is similar to the double gate NTFET shown in Fig. 3-28. The thin silicon body of 20nm is used which is comparable to the 10nm tunneling area. The simulated transfer characteristics of such a TFET are shown in Fig. 3-51. In a small regime, a very small subthreshold swing of 20.4 mV/dec is observed. When the drain current is higher than 10^{-13} μm/A, the subthreshold swing is 120 mV/dec. In our MOSFET simulation, the subthreshold swing smaller than 60mv/dec is never observed in any region. This simulation proves that the subthreshold swing in TFET is not limited by ln(10)·kT/q.

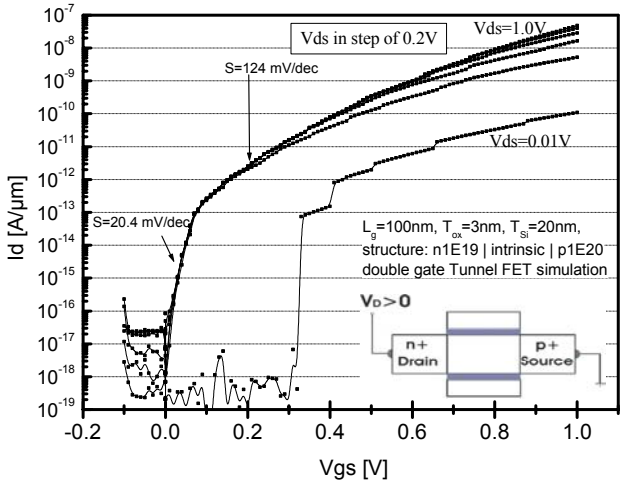


Fig. 3-51 Transfer characteristics of the double gate TFET with 100nm channel length and 3nm gate oxide thickness

The aggressive simulation is carried out to simulate the double gate NTFET with the p^+ source doping level of $10^{22}cm^{-3}$. The channel length is 100nm and t_{ox} =3nm. The subthreshold swing of 15mV/dec is observed due to the tunneling effect (Fig. 3-52). SiGe material may improve the performance of TFET because the boron doping level is higher in SiGe than in silicon. In addition, the dopant smear-out effect can be suppressed by introducing carbon into SiGe [41].

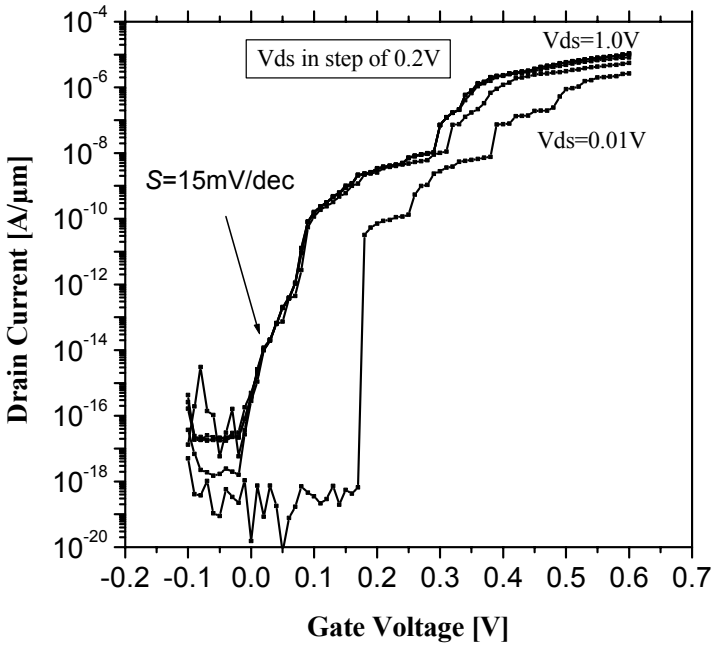


Fig. 3-52 Simulated transfer characteristics of the double gate NTFET with the p^+ doping level of $10^{22}cm^{-3}$

3.8 NTFET vs. PTFET

In principle, the NTFET and the PTFET have the same structure. Both of them are the MOS gated p-i-n structure. The type of TFET is determined by the doping level of source/drain doping level.

For NTFET, the p^+ doping concentration should be higher than the n^+ doping level. The electrons tunnel from the p^+ region to the channel region, when the positive gate voltage is applied. When the negative gate voltage is applied, the tunneling effect at the junction of the channel / n^+ doping region is suppressed because of the lower n^+ doping level in the NTFET. Increasing the n^+ doping level in NTFET, the tunneling effect at the junction of the channel/ n^+ doping region will be enhanced. This TFET behaves as both NTFET and PTFET (shown in Fig. 3-53)

For PTFET, the n^+ doping concentration should also be higher than the p^+ doping level. The electrons tunnel from the channel region to the n^+ region when the negative gate voltage is applied. When the positive gate voltage is applied, the tunneling effect at the junction of the channel/ p^+ doping region is suppressed because of the lower p^+ doping level in the NTFET. If the p^+ doping level in the NTFET is increased, the tunneling effect at the junction of the channel/ p^+ doping region will be enhanced. This TFET behaves as both PTFET and NTFET (shown in Fig. 3-54).

In the TFET with both NTFET and PTFET characteristics, there are two V_g values at the same drain current. Similar to the negative differential resistance in the resonant tunneling diode [42], this property of TFET may be useful for data storage.

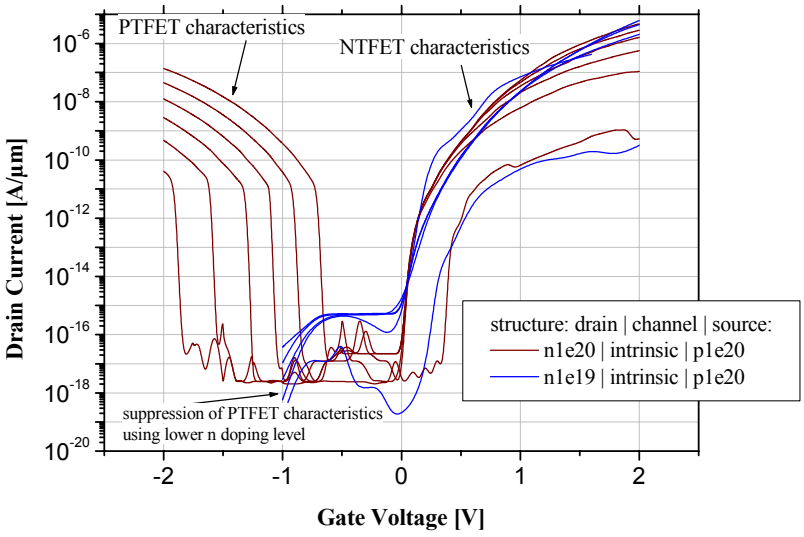


Fig. 3-53 Suppression of the PTFET characteristics using the lower n^+ doping level

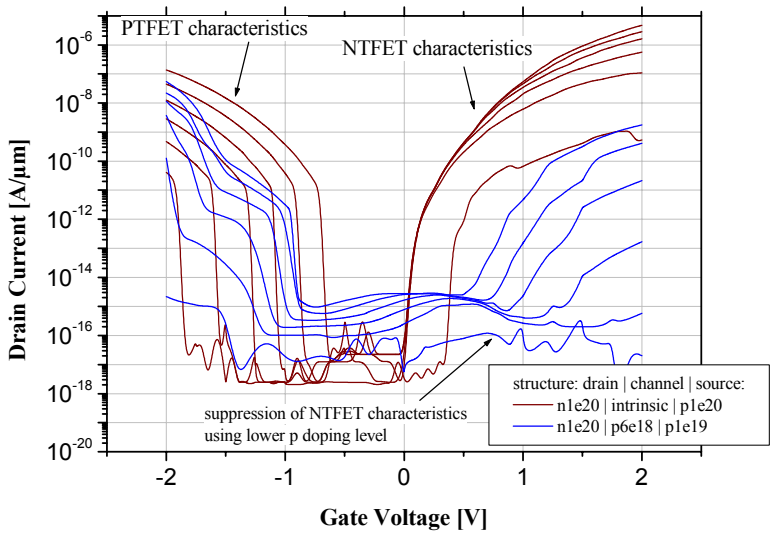


Fig. 3-54 Suppression of the NTFET characteristics using the lower p^+ doping level

3.9 Summary

The Device and process simulation is performed by the MEDICI and SUPREM simulators in this chapter.

In the device simulation, the influences of the doping profile, the oxide thickness and the channel length are investigated. The results of the device simulations are : 1). The high

performance NTFET needs sharp doping profile, thin gate oxide and high p-type doping level. The n^+ doping concentration in the NTFET should be slightly lower (e.g. 1×10^{19} cm^{-3}) to suppress its PTFET characteristics. 2). For the high performance PTFET, thin gate oxide, sharp doping profile, and high n-type doping level are needed as well. The p^+ doping concentration in the PTFET should be slightly lower (e.g. 1×10^{19} cm^{-3}) to suppress its NTFET characteristics. 3). To fabricate the TFET with both the NTFET and PTFET characteristics, both the n^+ and p^+ doping level should be high (e.g. 1×10^{20} cm^{-3}).

Compared to MOSFET, TFET has the advantage of a smaller off-current and a reduced V_t roll-off during scaling. In the 30nm channel length double gate TFET, the off-current is less than 10^{-11} A/μm which is much lower than the projected off-current in the ITRS roadmap 2002. Similar to MOSFET, the threshold voltage of TFET can be adjusted by the channel doping concentration.

The MBE-TFET fabrication processes are simulated using the similar experimental parameters by the SUPREM simulator. The results of the process simulation are: 1). The doping profile is changed after thermal gate oxidation and the TFET performance is degraded. Low temperature and short time oxidation can improve the device performance. 2). In the simulated process with the thermal gate oxidation, the performance improved by the delta-doping layer is not as good. It seems that the doping level of the whole p^+ region should be higher for the better NTFET performance. 3). The G-S overlap area in the MBE-NTFET can improve the drive current although the parasitic capacitance becomes larger.

The NTFET fabricated by the diffusion of SOD layer is also simulated. The drive current is improved in such a NTFET because when diffusion of SOD is used a higher p^+ source surface doping level than that in MBE-NTFET in enabled. This simulation shows the feasibility of the TFET fabricated by diffusion of the SOD layer in this work.

Due to the different working principles in TFET, its subthreshold swing is not limited by 60mV/dec. In the simulated 100nm double gate NTFET, the subthreshold swing of 20.4 mV/dec can be achieved. Increasing the p^+ source doping level to $1\times10^{22}cm^{-3}$, the subthreshold swing can be reduced to 15mV/dec.

Chapter 4

Process Development for the TFET Fabrication

It is obtained from the simulation that high doping, abrupt doping profile, and thin gate oxide are the key requirements for fabricating the high performance Tunneling FET. To achieve these technological requirements, the fabrication technologies should be further improved. In this chapter, all key technologies are tested and improved according to these TFET fabrication requirements.

4.1 Silicon Etching Technology

Silicon vertical etching is the technology needed for fabricating the vertical TFET, the vertical mesa diode, the self-aligned gate, and the shallow trench isolation (STI). The etching of semiconductor materials in the reactive ion beam etching system "TEPLA ECR RIBE 160" is investigated in this work.

4.1.1 Introduction to the etching technology

The etching process can be classified into the isotropic etching and the anisotropic etching dependent on the etching profile. Fig. 4-1 shows the difference between etching profiles of these two types of etching. For the isotropic etching, the substrate material is etched independent of the direction, resulting in the side etching (or the under-cutting) into the substrate. The size variation caused by the side etching on the lateral pattern must be taken into account in the mask design.

According to the etching ambient the etching process can be classified into wet etching and dry etching. Wet etching dominates the IC industry at its beginning. Dry etching is becoming very popular in the present semiconductor manufacturing lines. Table 4-1 compares the characteristics of wet etching and dry etching. In the dry etching system, the material is etched by the reactive plasma [43-46]. Two types of etching mechanisms exist in the dry etching: physical etching and chemical etching. Physical etching stems from the bombardment and sputtering by the accelerated particles in the plasma. Chemical etching results from the reaction of the free radicals generated in the plasma and the atoms on the surface of material. When many interactive gases are introduced into the plasma chamber at the same time, the etching mechanism will be very complex. For example, carbon-based gas and chlorine gas play different roles when they are mixed in the reactive ion etching system to etch the silicon trenches. The chlorine gas is a silicon etcher. The carbon-containing gas provides sidewall

passivation and depresses the undercutting of silicon [47,48]. Moreover, the plasma properties can be well managed by the electrical control in the dry etching systems. That enables a better management of the etching rate and the etching profile.

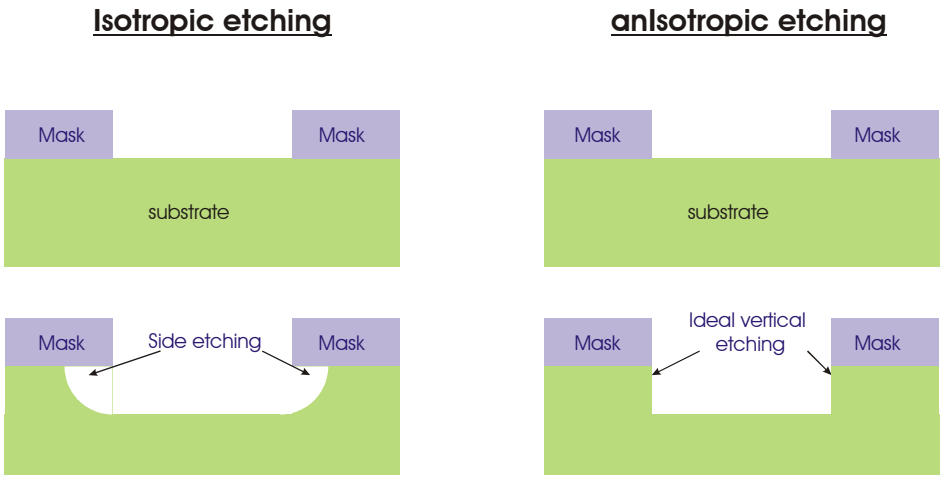
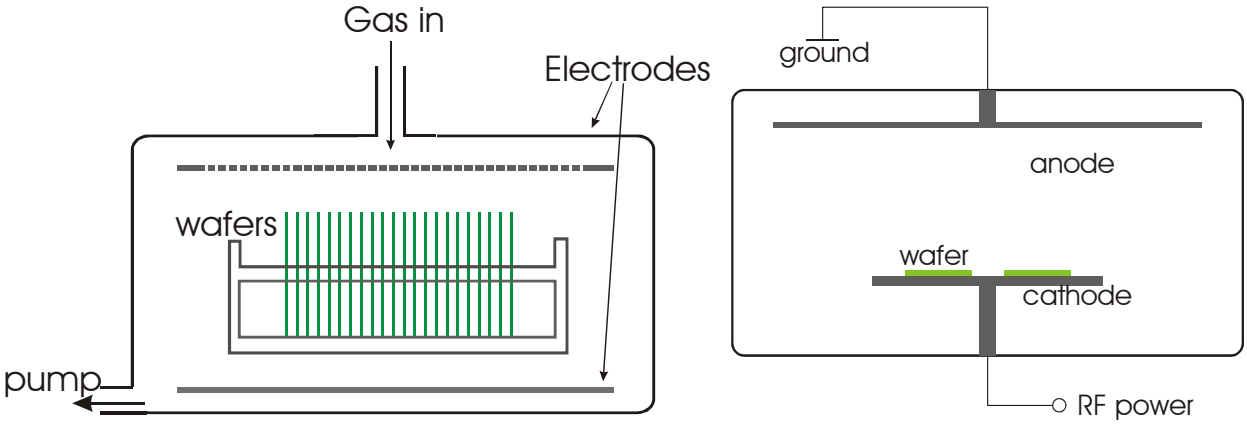


Fig. 4-1 Comparison of isotropic etching and anisotropic etching

Table 4-1 Comparison of wet etching and dry etching

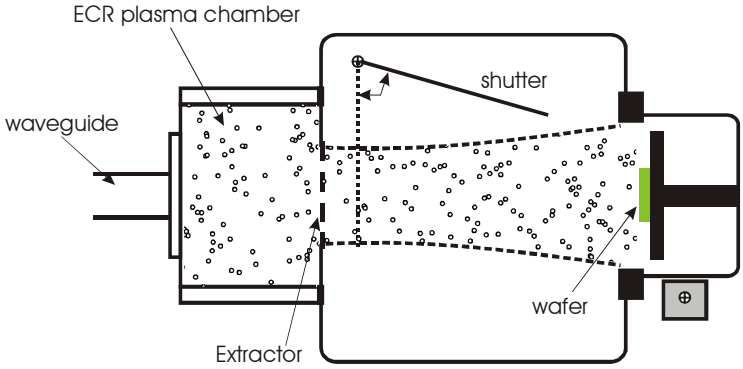
	WET ETCHING	DRY ETCHING
Etching mechanism	Chemical reaction	Chemical + physical reaction
Etching profile	Generally are isotropic	Well controlled etching profile
Equipment	Relatively easy and cheap	Relatively complex and expensive
Throughput	High throughput can be achieved	Comparably low

There are many types of dry etching systems. Fig. 4-2.a shows the barrel reactor with two radio frequency (RF) electrodes in the cylindrical chamber. The working pressure is about 10-600 Pa. The uniformity will be a problem, when the etching process is a diffusion-controlled process. Fig. 4-2b shows the parallel plates reactive ion etcher. This system looks similar to the conventional parallel plates Plasma Enhanced Chemical Vapor Deposition (PECVD) system. However, the area of the anode should be larger than the cathode. The working pressure of such a system is in the region of 2 to 50 Pa. In principle, the voltage drop of the plasma sheath is high during the etching. This high voltage may break down the gate oxide of the transistors. Problems such as the ion bombard induced damage and the etching ion implantation also arise[49]. In the Electron Cyclotron Resonant Reactive Ion Etching (ECR-RIE) system, these problems can be well solved by using the “remote plasma” generated in a remote chamber. As shown in Fig. 4-2c, the plasma is generated by the 2.45G Hz microwave. The magnetic field with the proper intensity is generated in order to obtain the resonance between the electron spin frequency and the external magnetic field frequency. By this, high density plasma can be generated at low pressure. The positively charged ions are extracted from the plasma chamber by a negative bias. The ion energy can be adjusted by changing the accelerating voltage. Therefore, the ion energy can be well managed and the lower ion energy can be achieved in this system [50,51].



a. Barrel reactor with two RF electrodes in the cylindrical chamber

b. Parallel plates reactive ion etcher



c. ECR reactive ion etching system

Fig. 4-2 Different types of plasma etching systems

The silicon high aspect ratio trench etching is becoming more and more important as the dimension of ULSI decreasing. The deep trench is used for etching contact holes, isolating devices and forming the deep trench capacitor of DRAM [52-54]. With a higher aspect ratio, the trench consumes less area so that the circuit density can be improved. The anisotropic property and the selectivity of etching depends on the etching chemicals and the etching system. Table 4-2 lists the etching gas and the etching-stop material for the silicon anisotropic etching. As shown in this table, the halogen-containing etchants are always used in silicon etching. In principle, the electronegativity of halogens obeys the order F>Cl>Br. The bromine-based etchant receives a smaller under cutting during etching. The high reactive rate of F results in the undercut of silicon. However, the F-based chemical such as CF_4 is preferred for etching the silicon trench shallower than 1μm because of its good etching selectivity to photo resist. For the silicon etching in the Cl and Br contained plasma, the silicon oxide can be used as the hard mask with the good selectivity to silicon.

With a very low ion energy, the etching selectivity of Si : SiO_2 can be 50 : 1 at room temperature and 100 : 1 at -30 °C in a pure chlorine beam. It is found that $SiCl_x$ is deposited on the SiO_2 and passivates the etching of oxide at 0°C. With higher ion energy, the sputtering of surface atoms by the ions will degrade the etching selectivity. As regards our measurement, the etching selectivity is only 3:1 in the 500eV energy ion beam of Ar and Cl.

Table 4-2 Etching gases and the etching-stop masks for the silicon selective dry etching

Etching material	Etch-stop material	Etching gas	Reference
Poly-Si	SiO_2	HBr, Cl_2, O_2	[55]
Si	Al	CF_4, O_2	[56]
$Si_{1-x}Ge_x$	Photo resist	CHF_3, H_2	[57]
Si	SiO_2	HBr/SiF_4 /O_2	[58]

In order to improve the etching aspect ratio, the carbon-based chemicals such as CH_3F are incorporated. The carbon passivation layer on the trench side wall can avoid the undercutting. The chemical reaction equations are:

$Cl_2 \rightarrow 2Cl\cdot$ (decomposed by ion bombardment) (4-1)
$Cl\cdot + Si \rightarrow SiCl_x$ (Si etching) (4-2)
$CH_3F \rightarrow C + HF + CH_x$ (Carbon passivation) (4-3)

The CF_4 gas is a popular etcher in the dry etching technology. In the reaction, the CF_4 gas can be broken down in plasma to: $CF_4 \rightarrow CF_3 + F$ and F is very reactive. The etching of Si, SiO_2 , and Si_3N_4 involves the reactions:

$Si + 4F \rightarrow SiF_4$ (4-4)
$SiO_2 + 4F \rightarrow SiF_4 + O_2$ (4-5)
$Si_3N_4 + 12\ F \rightarrow 3SiF_4 + 2N_2$ (4-6)

The etching rates vary, but typically the selectivity ratio is $Si > Si_3N_4 > SiO_2$.

4.1.2 Hard mask for the silicon etching in the TEPLA RIBE 160 system

In this work, the silicon etching in the ECR reactive ion etching system is investigated. In Fig. 4-3, the configuration of the TEPLA ECR RIBE 160 system is shown. The 2.45G Hz microwave is introduced into the ECR chamber by a rectangular waveguide. The Ar gas is used to generate high density plasma at low pressure, e.g. 5×10^{-3}Pa. The flow rates of the Ar gas and the reactive gases are controlled by mass flow controllers (MFC). The reactive gases can be introduced to the sample chamber or the ECR chamber. When they are introduced into the ECR chamber to participate the generation of the remote plasma, this type of etching is named as the chemical assisted ion beam etching (CAIBE). During the normal RIBE etching, the ion beam is extracted from the plasma source and then accelerated to bump the silicon sample. Therefore, the etching process contains both chemical and physical mechanisms. The more physical mechanisms are contained, the more anisotropic etching will be. Although rather vertical etching profile can be achieved by introducing carbon-based gas, carbon redeposition causes contamination. Especially in the vertical MOS or the vertical TFET fabrication, the high quality silicon side wall is needed for the formation of good oxide and low surface leakage current. Therefore, the hard mask with low sputtering yield compared to silicon is preferred. We select the reactive sputtered Al_2O_3 film as the hard mask for the silicon vertical etching. According to table 4-3, the sputtering yield of Al_2O_3 is about 1/12 of silicon when bombarded by 500eV Ar^+ ions.

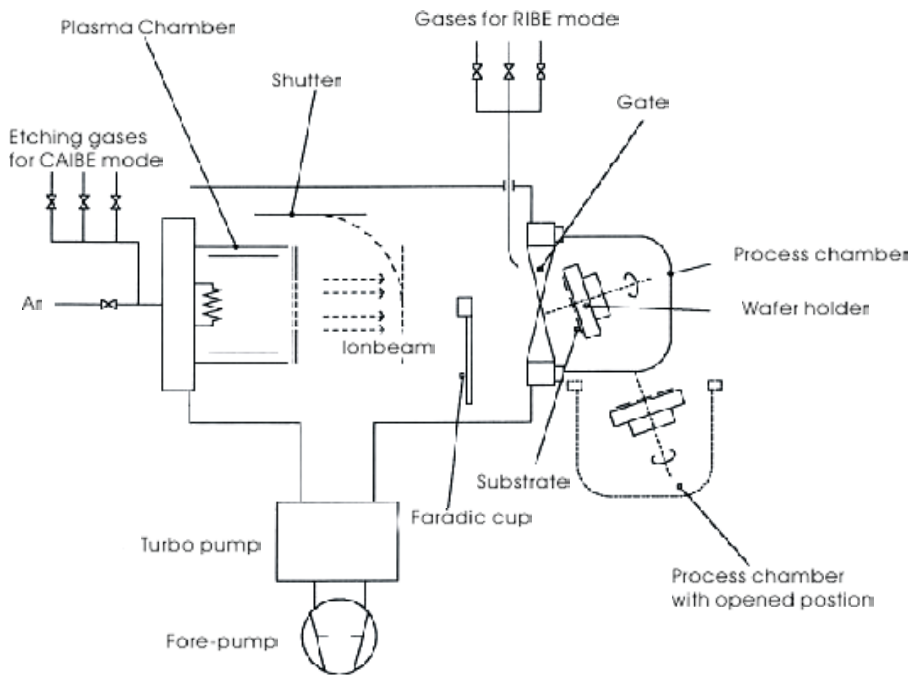


Fig. 4-3 Schematic structure of the TEPLA ECR-RIBE 160 system

Table 4-3 Sputtering yield of the different materials using 500eV Ar^+ ion bombardment

Sputtering yield η_s [atom/ion]. Ion Energy=500eV, Ion: Ar^+					
Target material	Si	Al_2O_3	SiO_2	C	Cr
Sputtering yield	0.50	0.04	0.13	0.12	1.18

Four types of hard masks are tested for the vertical etching. They are: the sputtered silicon oxide, the sputtered silicon nitride, the sputtered Al_2O_3 without heating, and the sputtered Al_2O_3 at 400°C. The experimental results are shown in table 4-4.

Fig. 4-4 shows the etching rates of Si and SiO_2 with the 5sccm Cl_2 flow rate in the ECR-RIE system. The etching rate of both Si and SiO_2 increase exponentially with the increase of the accelerate voltage. The etching rate of SiO_2 is about 1/3 of Si.

As shown in table 4-4, the etching selectivity of silicon to Al_2O_3 can be as high as 10.3 : 1. Therefore, the Al_2O_3 thin film is studied as the hard mask for the silicon vertical trench etching. The Al_2O_3 thin film is deposited by the reactive sputtering at room temperature. The sputtering rate is 3nm/min. The Al_2O_3 thin film is patterned by the wet etching. Two chemical etcher are tested: a). Mixture of H_3PO_4, HNO_3, and DI-H_2O with ratio of 80: 4: 16. b) Buffered HF with HF: DI-H_2O= 84: 16. The pattern after the buffered HF etching is shown in Fig. 4-5. Crystals of AlF_3 are deposited on the silicon surface which will result in the micro-mask effect for plasma etching. This problem can be solved using the mixture of H_3PO_4 and HNO_3 as the etcher. The temperature of this wet chemical etching is between 50°C and 60°C. A higher temperature may destroy the photo resist.

Table 4-4 Etching selectivity and etching rate of the hard masks for silicon vertical etching

Material	Layer growth	Etching rate at 500V [Cl_2] 4 sccm	Etching selectively to Si
Reactive Sputtered SiO_2	Sputter, 200W, 25°C	14.5 nm/min	2.84
Reactive Sputtered Si_3N_4	Sputter, 200W, 25°C	19.2 nm/min	2.15
Reactive Sputtered Al_2O_3	Sputter, 200W, 25°C	4 nm/min	10.3
Reactive Sputtered Al_2O_3	Sputter, 200W, 400°C	4 nm/min	10.3
Si substrate	--	41.2nm/min	--

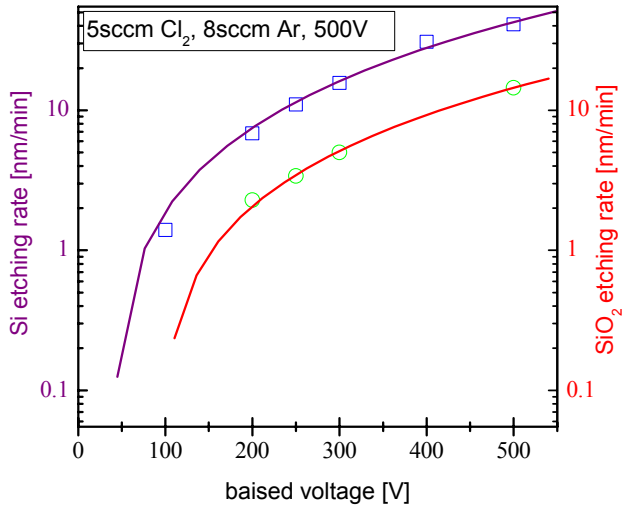


Fig. 4-4 Etching rate of silicon and silicon oxide in the RIBE 160 system using the Cl_2 gas

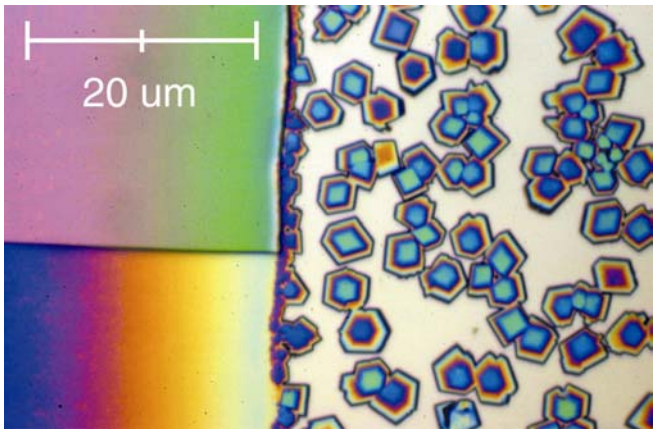


Fig. 4-5 Pattern of Al_2O_3 after the buffered HF etching, AlF_3 are created after etching.

Table 4-5 Properties of Al_2O_3

Formula:	Density	Melting Point	Thermal Expansion	Dielectric Constant
Al_2O_3	3.98 g/cm^3	2052° C	5.4 x 10^{-6} K^{-1}	9.4

4.1.3 Silicon trench etching

Using SiO_2 as the hard mask, the silicon trench is etched with the Cl_2 plasma. The focused ion beam (FIB) system is applied to view the silicon profile. In Fig. 4-6, the slope of edge is 74°. This slope is transferred from the isotropic wet etching of the oxide hard mask. The edge is rough because of the limited quality of the emulsion mask.

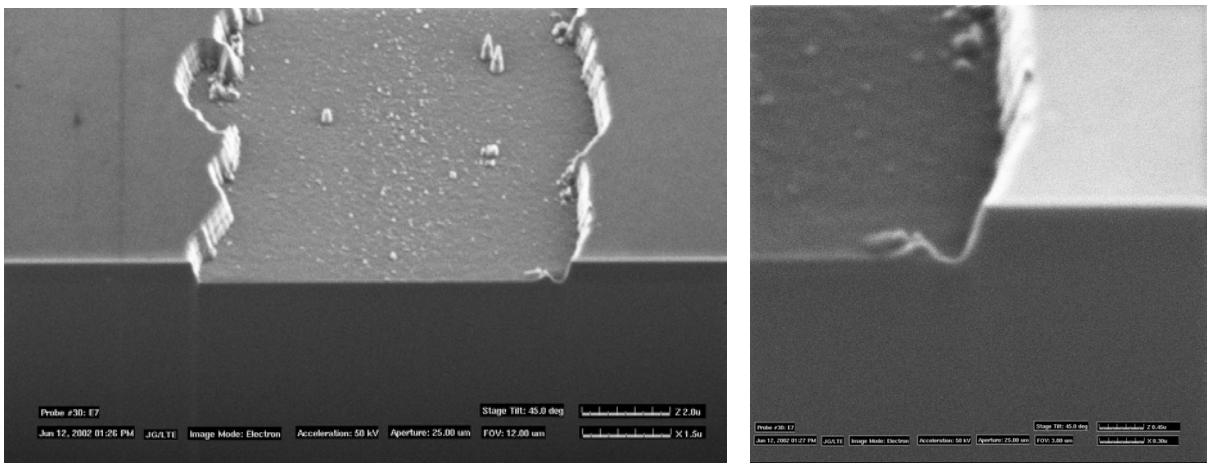


Fig. 4-6 Silicon trench formed by the Cl_2 reactive ion etching.

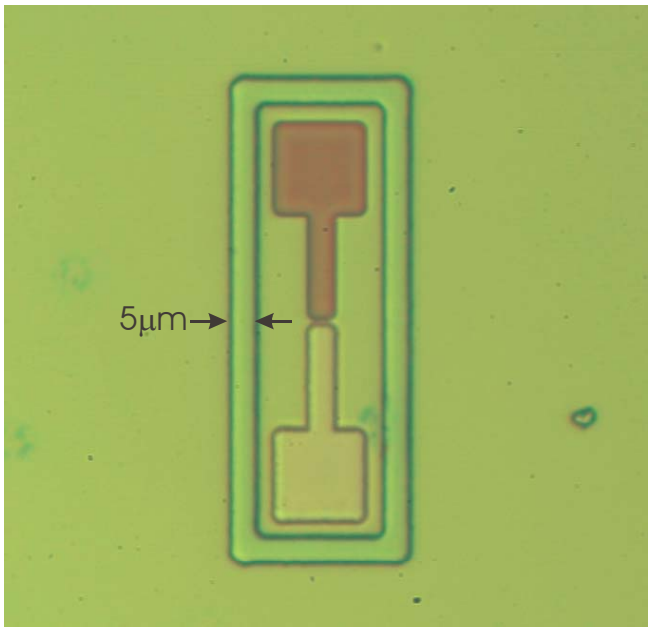


Fig. 4-7 STI used to suppress the surface leakage and to separate the devices.
The chromium mask is used in this etching and the edge is smooth after etching.

The silicon shallow trench isolation (STI) technology [59,60] is developed to suppress the surface leakage current and to separate the devices. As shown in Fig. 4-7, a 1μm deep STI structure is formed around the device. The active area can be determined by this STI structure. Combined with Silicon on Insulator (SOI) technology, the STI can separate the devices completely. The leakage current and the parasitic capacitance will also be reduced extremely.

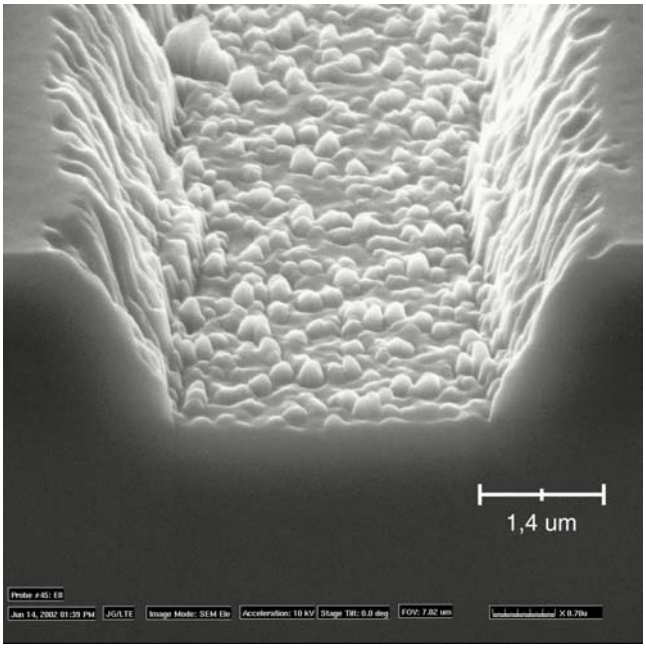


Fig. 4-8 Silicon trench etched using Al_2O_3 as the hard mask.

Silicon trench is also formed using Al_2O_3 as the hard mask. There is a micro-mask effect because of the non-volatile $AlCl_3$ product (Fig. 4-8). Therefore, Al_2O_3 is used when the deep trench is etched because the etching selectivity is good. When the trench is etched less than 1μm deep, SiO_2 film is used as the hard mask.

4.2 Doping technology

There are many doping methods such as ion implantation, thermal diffusion, MBE technology etc.. [61-65] Ion implantation is the main doping method used in the semiconductor industry. It has the advantages of implant depth, direction control and a reduced thermal budget. However, the annealing process is needed to heal the damage caused by the implantation of the high energy ion beam and to activate the doping atoms. The channeling effects during the implantation and the void assisted diffusion during the annealing process make the doping profile more complex. The MBE doping method can achieve very sharp doping profile and it is widely used in the fabrication of tunneling devices. In this work the diffusion doping is used to fabricate the tunneling transistor. The doped spin on doping glass (SOD) can be used as the doping source. The advantage of SOD is that the ultra-shallow junction can be formed using the rapid thermal diffusion. In addition, with the special process design, the distinctive doping profile can be formed.

4.2.1 Mechanism of the spin on diffusion

The SOD precursor is a dopant containing sol-gel. After the volatilization of the solvent, the SOD film similar to silicon oxide can be formed. The primer of SOD can be obtained from the industry. In this work SOD P507 for the p-type doping and SOD B150, SOD B155 for the p-type doping is used. Table 4-6 shows the information of these precursors. Fig. 4-9 shows the chemical structure of the silicon dioxide and the phosphorous-containing SOD. [66]

Table 4-6 Details of the SOD precursors for n and p type doping

	Doping type	Dopant concentration (%)	Application
SOD P507	N-type	4% phosphorous	Heavy n doping
SOD B150	P-type	0.4% boron	Light p doping
SOD B155	P-type	4% boron	Heavy p doping

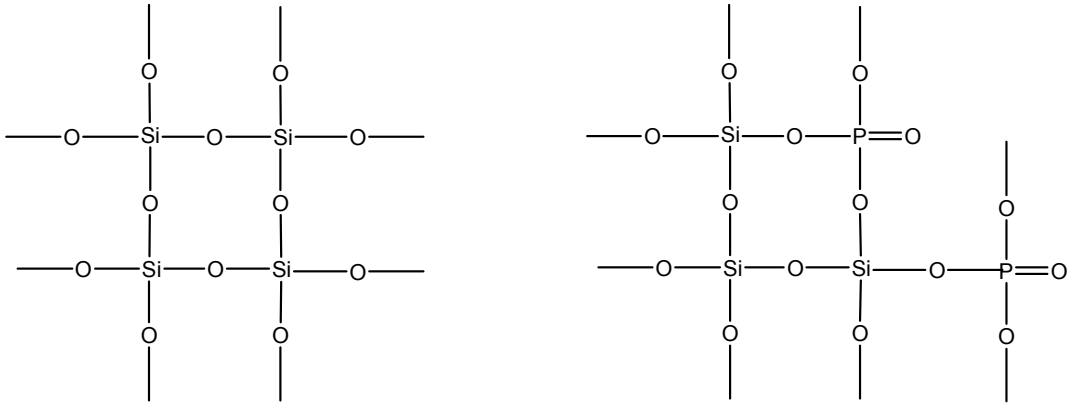


Fig. 4-9 Chemical structures of the silicon dioxide (left) and the phosphorous-containing SOD (right)

When the wafer covered by SOD is heated up to 900°C-1100°C, the silicon will react with the SOD film. During this reaction, the phosphorous or boron atoms will diffuse into the silicon substrate. The chemical reaction equations for the phosphorous and boron diffusion are shown in the equations 4-7 to 4-11. The equations 4-8, 4-10 and 4-11 show that there is the probability for the SOD film to form the volatile species by the reaction with the moisture in the atmosphere. Therefore, the diffusion process should be immediately done after the spin-on process.

Phosphorous diffusion:

$$2\ P_2O_5 + 5\ Si \rightarrow 5\ SiO_2 + 4\ P \quad (4\text{-}7)$$

$$P_2O_5 + 3\ H_2O \rightarrow 2\ H_3PO_4 \text{ (volatile, 400°C)} \quad (4\text{-}8)$$

Boron diffusion:

$$2\ B_2O_3 + 3\ Si \rightarrow 3\ SiO_2 + 4\ B \quad (4\text{-}9)$$

$$B_2O_3 + 3\ H_2O \rightarrow 2\ H_3BO_3 \text{ (volatile, 300°C)} \quad (4\text{-}10)$$

$$\text{or } B_2O_3 + H_2O \rightarrow 2\ HBO_2 \text{ (volatile)} \quad (4\text{-}11)$$

The SOD layer should be baked before the diffusion process to eliminate water and other solvents in the solution. The thickness of SOD will shrink after baking. For the SOD B150 film and the SOD B155 film, the baking time is not critical when diffusing in the normal diffusion oven, because there is no water in the SOD B150 film or the SOD B155 film. When using the RTP system for the diffusion process, the vacuum may pump away both the solvent

and the boron dopant. Some bubbles will be formed after the pumping. This problem can be solved by increasing the baking time.

The thickness of the SOD P507 film after baked at 160°C for 5 minutes is investigated. As shown in Fig. 4-10, the thickness of the SOD P507 film decreases from 160nm to 110nm as the spin rate is increased from 3000 to 8000 round per minute. The thickness control of SOD P507 is calibrated for the special process, such as the vertical self-aligned TFET fabrication (shown in Fig. 5-10) and the proposed planar self-aligned TFET process (shown in Fig. 5-66).

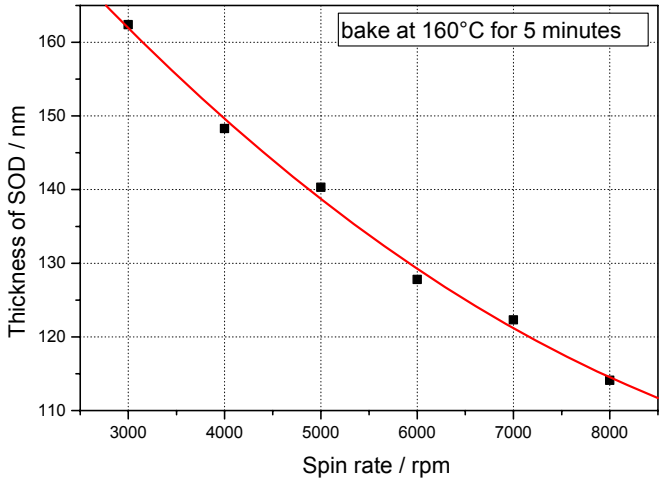


Fig. 4-10 Thickness of the SOD P507 film vs. the spin rate, baking condition: 160°C 5min

4.2.2. Electrical results of SOD diffusion

Some problems still exist for the SOD diffusion. First, as mentioned in the last section, the volatile products such as H_3PO_4, H_3BO_3 will decrease the diffusion concentration. Therefore, the diffusion process should be started immediately after the spin on process. Second, a boron-rich silicon borides SiB_x can be formed when excessive boron exists on the silicon surface. This layer has the thickness of a few hundred angstrom and looks dark. Because of its poor electrical conductivity, this layer must be removed to ensure good contact. It is difficult to remove it using the wet chemical etching. In our process, it is removed using Cl_2 gas in the reactive ion etching (RIE) system.

4.2.2.1 N diffusion using SOD P507

The n and p type SOD diffusion are investigated. For the n-type doping, first SOD P507 is spun on with 3000 rpm rotation rate and baked at 160°C for 5 minutes. Then follows the diffusion process. The diffusion process is performed at 1000°C for various times. The sheet resistance of the diffused samples is measured using the 4-point measurement. In the 4-point measurement, four electrodes with the same space "*s*" are put on the silicon. The current is provided by the two outer electrodes and the voltage difference between the two inner

electrodes is measured. When *s* is much smaller than the wafer size *d* (*d*/*s* >40), the sheet resistance can be expressed as:

$$Rs = 4.53 \cdot V_{diff} / I \tag{4-12}$$

This method overcomes the contact problem of the metal electrodes on the silicon samples in the two-point measurement. Another advantage of the four-point sheet resistance measurement is that it is a non-destructive measurement. However, this measurement is more precise for measuring the heavily doped layer on the lightly anti-doped layer (e.g. n^+ layer on p^- layer). Here, this measurement is used to give a qualitative test on the sheet resistance of the n-type diffusion on the lightly n-type wafer. The measurement results of the n-type diffused wafers are shown in Fig. 4-11. Many samples are diffused and characterized, and there has never been a problem in the n type diffusion using SOD P507. The n-type diffusion is much easier than the p-type diffusion. Hence, the investigation is emphasised on the p-type diffusion using SOD B150 and SOD B155.

From the Secondary Ion Mass Spectrometry (SIMS) measurement, the surface concentration of n diffusion using SOD P507 at 1000°C is $2 \times 10^{20} cm^{-3}$.

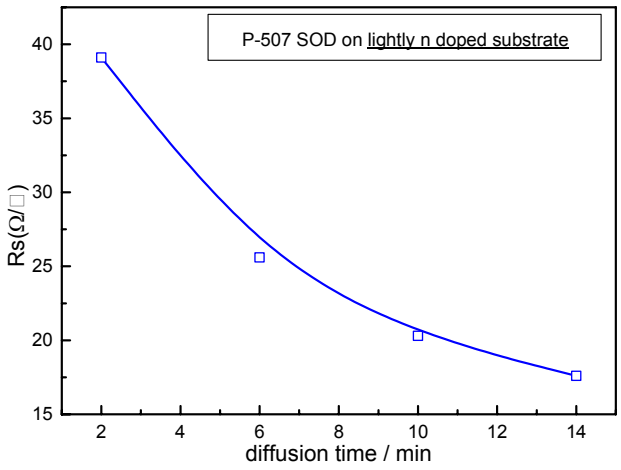


Fig. 4-11 Sheet resistance of the wafer doped using SOD P507 diffusion at 1000°C

4.2.2.2 P-type diffusion using SOD B150 and SOD B155

4.2.2.2.1 Diffusion using SOD B150

Experiments are designed for the p type diffusion on the n type wafer. The diffusion using SOD B150 is studied first. After spun on, the wafer is diffused at temperature of 900°C, 1000°C and 1100°C. The flow rates of N_2 and O_2 during the diffusion are 0.5 and 0.2 l/min, respectively. The diffusion time is varied from 2 minutes to 60 minutes. For the low boron atom concentration in SOD B150 (0.4% at.%), the surface doping level of the samples diffused below 1000°C is low so that the 4-point measurements can not allow repetitive results. The wafer diffused for 60 min. at 1100°C ensures better contact. There is no SiB_x layer observed in this diffusion due to the low boron concentration in the B150 precursor. In

Fig. 4-12, the sheet resistance of the p doped layer is 293Ω/sq. To get a higher surface concentration, the substrate is covered with two or more layers of SOD B150 films. The amount of dopant increases for the thicker SOD layer and the lower sheet resistance is obtained. The sheet resistance of the wafer with twice the SOD B150 spin layer is decreased to 256Ω/sq. However, when the thickness of the SOD layer increases, the difference in the thermal expansion indices between Si and SiO_2 may introduce stress damage at the interface.

The sheet resistance measurement involves a problem when measuring the wafer after SOD B150 diffusion. Sometimes, the resistance of several kΩ is obtained using B150 diffusion at 1100°C for 60 minutes. This problem may be caused by the schottky diode formed between the metal needle and the p silicon when the contact is not good enough. Fig. 4-13 shows the schottky diode measured by contacting the metal needle on the p silicon after SOD B150 diffusion. Fig. 4-14 shows the simulation results of the sheet resistance under different diffusion conditions. From this figure, the surface concentration of the layer with the sheet resistance of 293Ω/sq is around $2\times10^{19}cm^{-3}$ and the wafer with 1kΩ/sq has even lower surface doping concentration. Since lower p doping concentration can be obtained using diffusion of SOD B150, it is used to form p well for fabricating the complementary TFET. To get the heavy boron doping in silicon, the SOD B155 precursor with boron atom concentration of 4% is investigated.

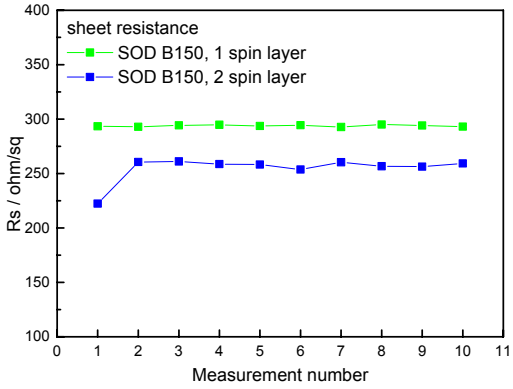


Fig. 4-12 Sheet measured resistance of the sample covered by SOD B150 film. Diffusion parameter: 1100°C for 60 minutes

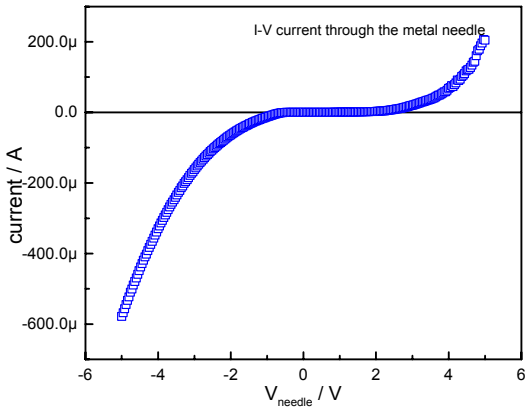


Fig. 4-13 *I-V* curve of the metal-pSi diode shows the Schottky diode characteristic

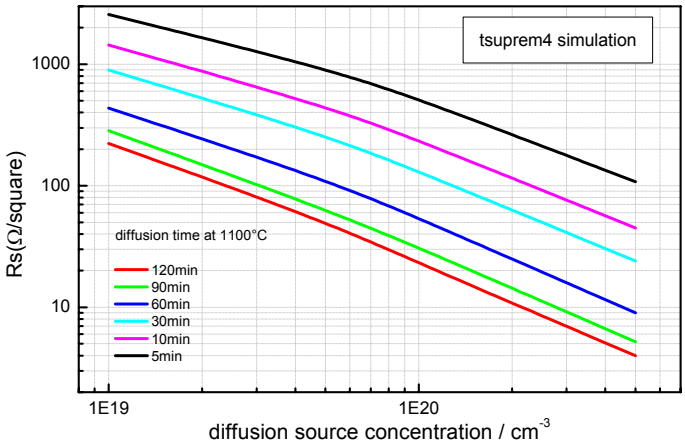


Fig. 4-14 Simulation of the sheet resistance obtained by p-type diffusion doping

4.2.2.2.2 Diffusion using SOD B155

The boron diffusion process is performed using the diffusion of SOD B155 at 1100°C for 30 minutes in the normal thermal diffusion oven. The result of 4-point sheet resistance measurement is shown in Fig. 4-15. The sheet resistance of this wafer is about 17Ω/square. Looking up to Fig. 4-14, 17Ω/square means that the surface concentration is higher than $1\times10^{20}cm^{-3}$. The heavy p doping can be achieved using the diffusion of SOD B155.

Decreasing the diffusion temperature to 1000°C, wafers with diffusion duration of 2, 10, 20 minutes are tested. The sheet resistance measurements of these three wafers are shown in Fig. 4-16. The sheet resistance decreases from 116Ω/square to 24Ω/square when diffusion time is increased from 2 minutes to 20 minutes.

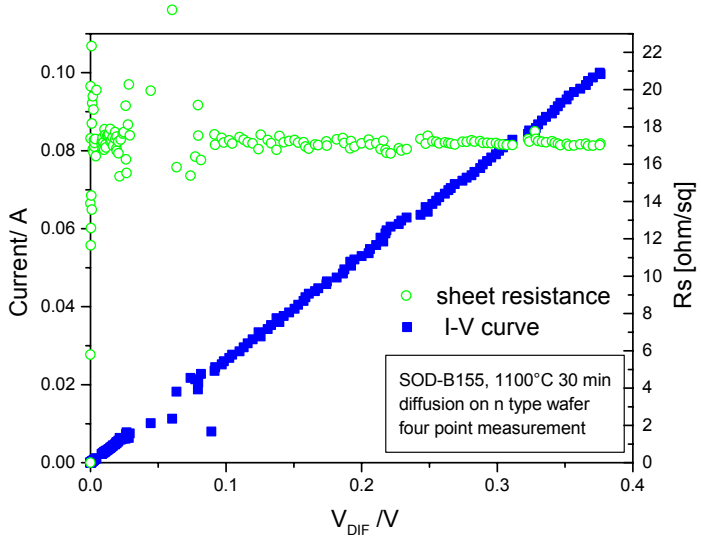


Fig. 4-15 Four-point sheet resistance measurement result of wafer with SOD B155 diffusion at 1100°C for 30 minutes

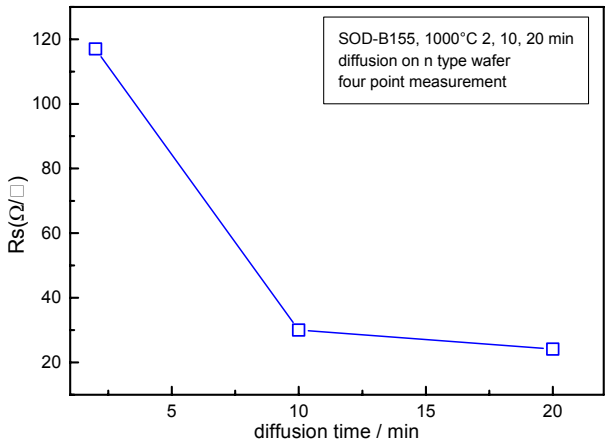


Fig. 4-16 Sheet resistance of the boron doped layer measured by 4-point measurement, diffusion source: SOD B155

The 4-point measurement combined with the RIE is carried out to measure the doping profile of the SOD B155 diffusion at 1100°C and 1000°C. The silicon surface layer is removed by the RIE silicon etching with an etching rate of 20 nm/min. After the etching, the sheet resistance is measured. Comparing the resistance difference before and after the etching, the resistance of the removed layer can be calculated. Converting the sheet resistance to the resistivity by Equation 4-13, the electrical active doping concentration can be calculated as well. (shown in Fig. 4-17)

$$R = R_{square} \cdot t \tag{4-13}$$

where R is the resistivity of the doped layer, R_{square} is the square resistance of the silicon layer etched away; t is the thickness of the etched layer.

$$R_s = R_{s1} * R_{s2} / (R_{s1} + R_{s2})$$

$$R_{s2} = R_s * R_{s1} / (R_{s1} - R_s)$$

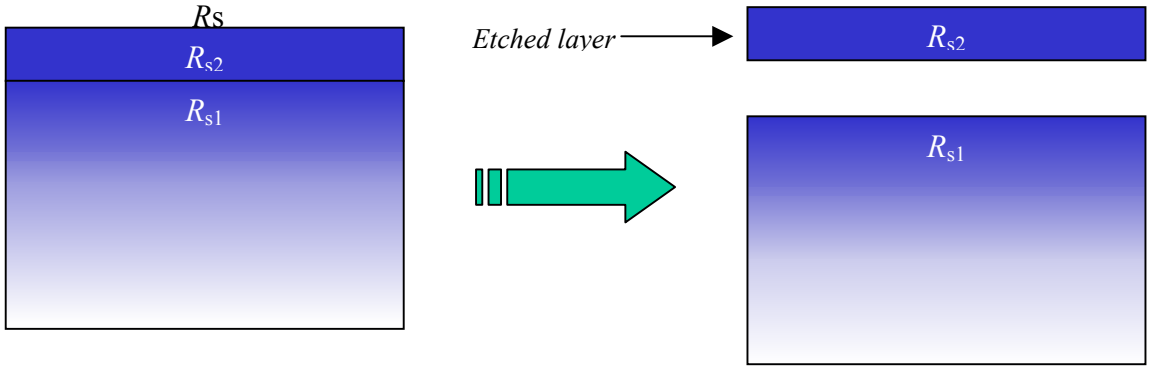


Fig. 4-17 Calculation of the sheet resistance of the removed layer

The <100> n- doped silicon is used as the substrate for the SOD B155 diffusion. Two wafers are diffused in the normal diffusion oven at 1100°C for 30 minutes and 1000°C for 20 minutes respectively. Fig. 4-18 and 4-19 show the four-point measurement results for these two kinds of wafers. The four-point measurements indicate that the sheet resistance increases if more heavily p doped silicon is etched away. For the wafer diffused at 1100°C for 30 minutes, the change in sheet resistance is small because the diffusion junction is very deep. The sheet resistance difference after etching is larger for wafer #90, which is diffused at 1000°C for 20 minutes. The doping concentration is calculated for wafer #90.

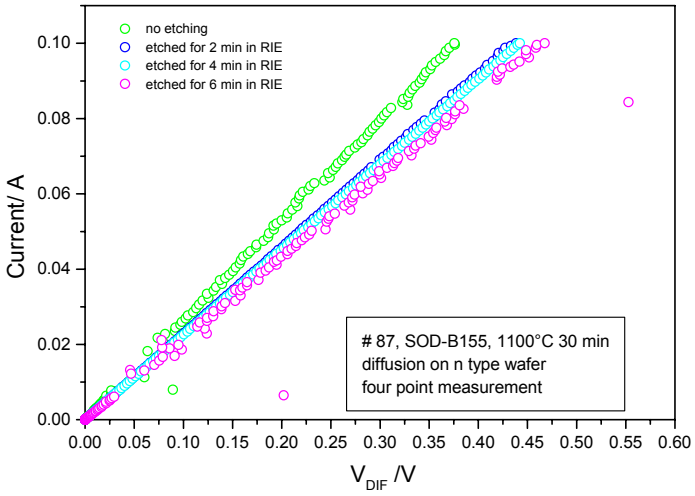


Fig. 4-18 Sheet resistance measurement results of wafer #87 after RIE with an etching rate of 20nm/min

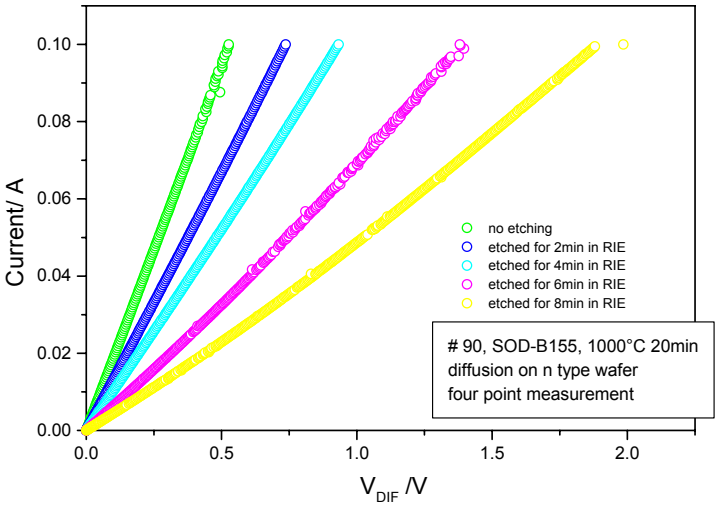


Fig. 4-19 Sheet resistance measurement results for wafer #90 after RIE with an etching rate of 20nm/min

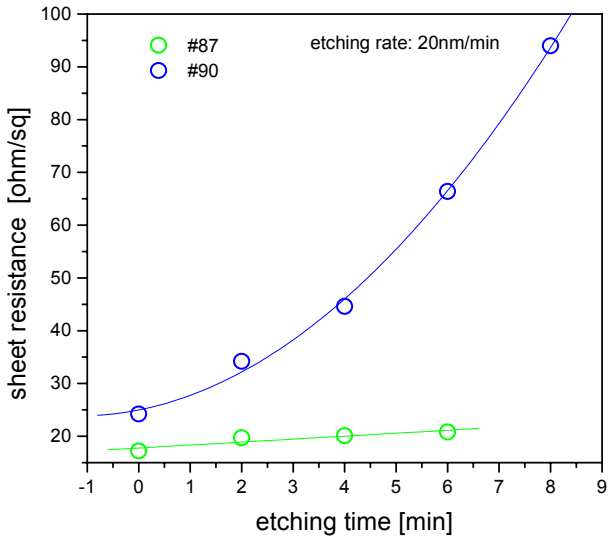


Fig. 4-20 Sheet resistance vs. etching time for wafers #87 and #90
The sheet resistance increases with an increasing etching time.

In table 4-7, the measured sheet resistance and the etching depth are placed in the first two columns. The sheet resistance of the etched layer with thickness of 40nm can be calculated by the equations shown in Fig. 4-17. The third column is the depth of the middle of the etched layer. The fourth column is the resistivity of the etched layer calculated from the sheet resistance using equation 4-13. The fifth column is the p type doping concentration calculated using the doping concentration calculator at "http://www.solecon.com/sra/rho2ccal.htm". The calculated doping profile for the wafer diffused at 1000°C for 20 minutes using SOD B155 is shown in Fig. 4-21. The electrical active boron doping concentration on the silicon surface is around $2.8\times10^{20}cm^{-3}$.

Table 4-7 Calculation of doping concentration for wafer #90

Depth / nm	R_{square} of the 4-point measurement / Ω/square	Depth / nm	R_{square} of the etched layer / mΩ·cm	Calculated concentration / cm^{-3}
0	24.8			
	⇒	20	0.420	2.76E20
40	32.45			
	⇒	60	0.441	2.63E20
80	46			
	⇒	100	0.597	1.94E20
120	66.5			
	⇒	140	0.908	1.27E20
160	94.07			

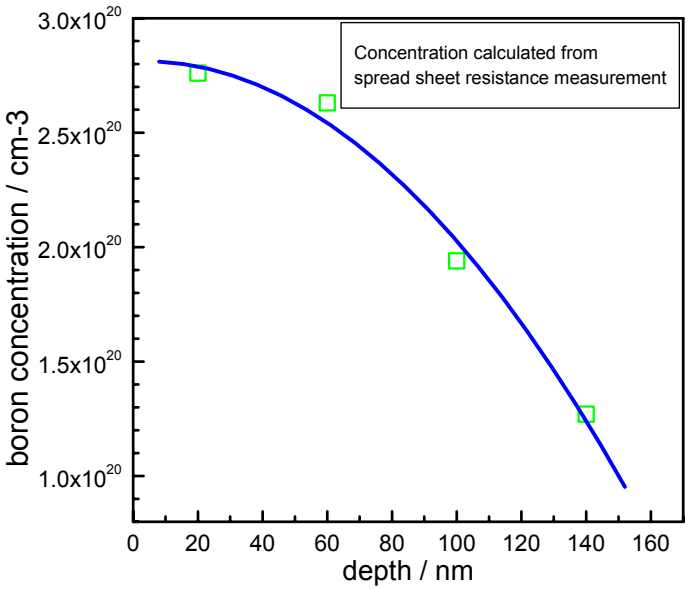


Fig. 4-21 Calculated doping profile of wafer #90 with the SOD B155.diffusion at 1000°C for 20 minutes

The diffusion process using SOD B 155 results in very heavy p doping, that results in a boron-rich silicon borides (SiB_x) layer. This layer looks amorphous and not good for the contact. It can be removed in the RIE system using the chlorine etching. During the etching process, the Ar^+ high density plasma is generated and accelerated to bump the Cl_2 molecule which is adsorbed on the SiB_x surface. The Cl· radicals are generated by the impact of the Ar^+ ions and then react with SiB_x layer. 1.5 minute of treatment in the RIE can remove this SiB_x layer completely. After the removal, the substrate silicon becomes slightly rough.

4.2.3 SOD using the RTP chamber

In order to receive a sharp doping profile and high doping concentration, the n-type and p-type diffusion in the RTP chamber is also calibrated.

A Rapid Thermal Chemical Vapor Deposition (RTCVD) system (JETLIGHT 200) is repaired and investigated in this work. Fig. 4-22 is the picture of JETLIGHT 200, the manual main control panel and the gas control panel with four mass flow controllers are installed after repairing.

Fig. 4-22 Picture of the RTCVD system (JETLIGHT 200)

By absorbing the irradiation of the lamps, the silicon wafer can be heated up very quickly. [67-69] RTP allows a higher temperature so that a higher doping concentration can be obtained. The rapid thermal process can also minimize the thermal budget of process which is essential for the sharp doping profile of TFET. The n^- silicon substrate is used to calibrate the temperature. The heat-up/ down characteristic of RTP system is shown in Fig. 4-23.

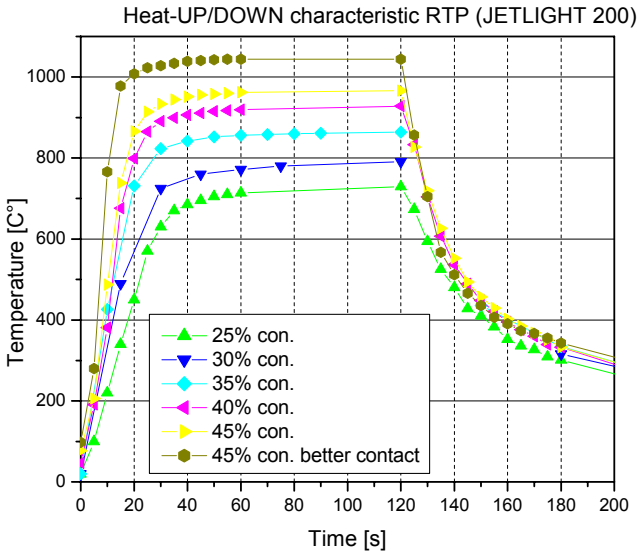


Fig. 4-23 Heat-up/ down characteristic of JETLIGHT 200

This RTP system is installed to investigate the atomic layer deposition for high-k materials, especially the Si_3N_4 /SiO_2 stacks. Thus N_2, O_2, $SiCl_2H_2$, and NH_3 gases are installed. The corresponding reactions are shown in the following:

Si_3N_4 deposition: $3\ SiH_2Cl_2 + 4\ NH_3 \rightarrow\ Si_3N_4 + 6\ HCl + 6\ H_2$ (4-14)

Poly-Si deposition : $SiH_2Cl_2 \rightarrow Si + 2\ HCl$ (4-15)

Oxidation : $Si + O_2 \rightarrow SiO_2$ (4-16)

To achieve a sharp doping profile and a heavy doping concentration on the silicon surface, the rapid thermal diffusion (RTD) of SOD is also investigated.

The n-type diffusion using SOD P507 at 1050°C for 300s, 90s, and at 950°C for 90s is performed. Fig. 4-24 shows the doping profile of phosphorous measured by the SIMS measurement. The phosphorous atoms concentration is calibrated using the relative sensitive factor (RSF) to Si. The RSF used here for phosphorous is 1×10^{22}atom/cm^{-3}.

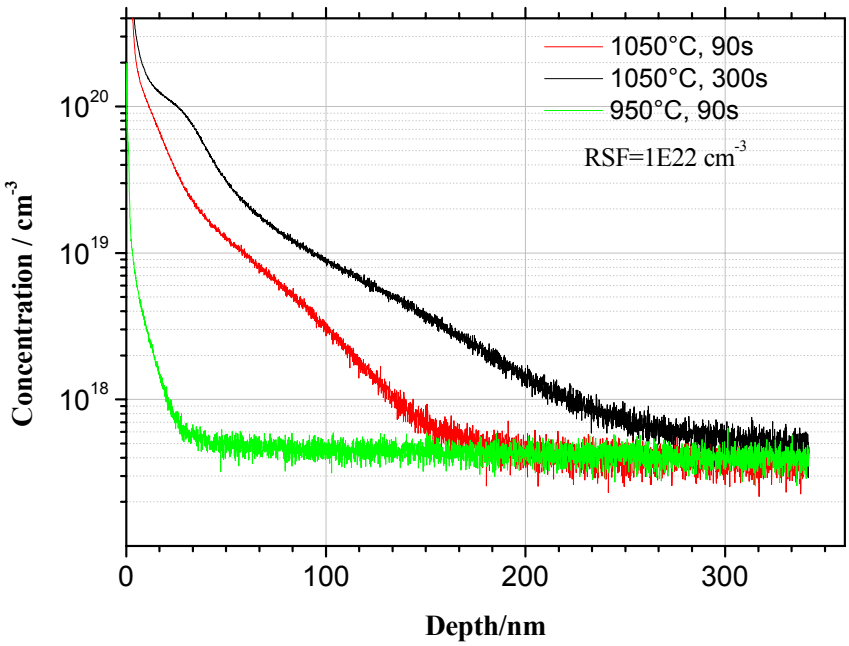


Fig. 4-24 SIMS measured phosphorous depth profile in Si after the RT-Diffusion

The p-type diffusion using SOD B155 at 1050°C for 30s, 60s, 120s, and 180s is performed. Fig. 4-25 shows the doping profile of boron atoms measured by the SIMS measurement. The boron atoms concentration is calibrated using the RSF to Si with the value of 1×10^{20} atom/cm^{-3}. It can be seen that the ultra-shallow junction is formed after the diffusion at 1050°C for 30s. These SIMS measurements prove that the ultra-shallow junctions can be formed by out-diffusion of SOD layers in the RTP chamber.

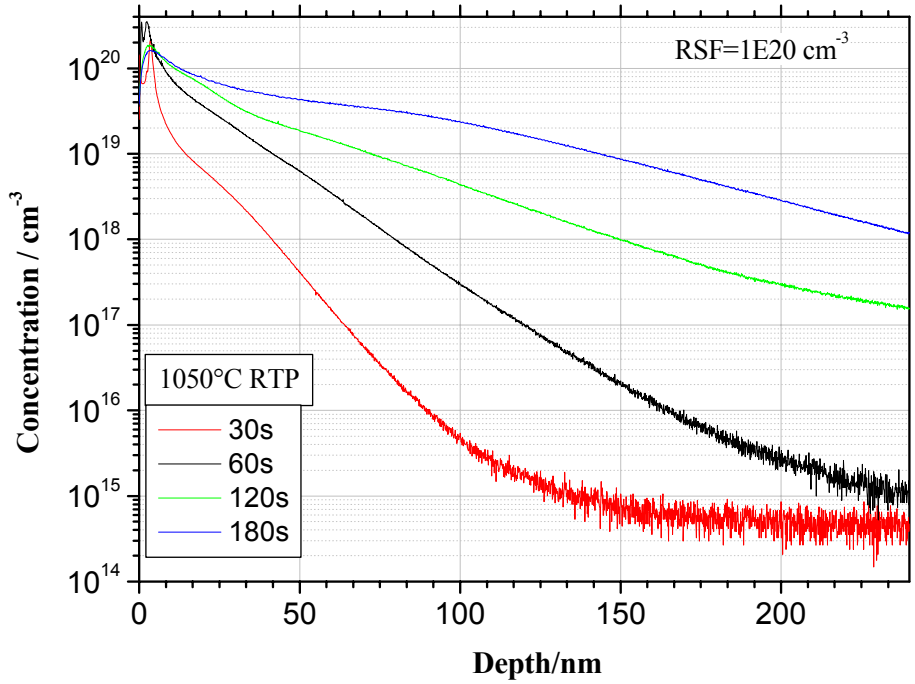


Fig. 4-25 SIMS measured boron depth profile in Si after the RT-Diffusion

The RT-Diffusion character is investigated furthermore by fabricating the silicon Esaki tunnel diode in the RTP chamber. The measurement results will be discussed in chapter 5. For one TFET run, the RTP chamber is used for RTP diffusion. The TFET results show that without RTP, no planar TFET can be fabricated using the SOD diffusion.

4.2.4 Patterning of the SOD layer

To achieve a special doping profile, the SOD layer should be patterned before the diffusion process. In this section, the patterning of SOD P507 and SOD B155 is studied.

Similar to the diffusion process, the SOD P507 is spun on the wafer and baked at 160°C for 5 minutes. Then the primer and the photo resist are spun on in sequence. After exposure and development operation, there is no precise pattern at all. The reason is that the SOD layer still contains some water and the photo resist can not stick on it very well. The SOD layer also absorbs water during the lithography process and form the nodes (see Fig. 4-26). To eliminate the water inside the SOD layer, the samples should be baked for a longer time before the lithography process. Baking times of 30, 45, 60, 90, and 120 minutes are tried before the lithography process. The good patterning is obtained by baking the SOD layer for 120 minutes at 160°C. The patterns of the other samples are not good.

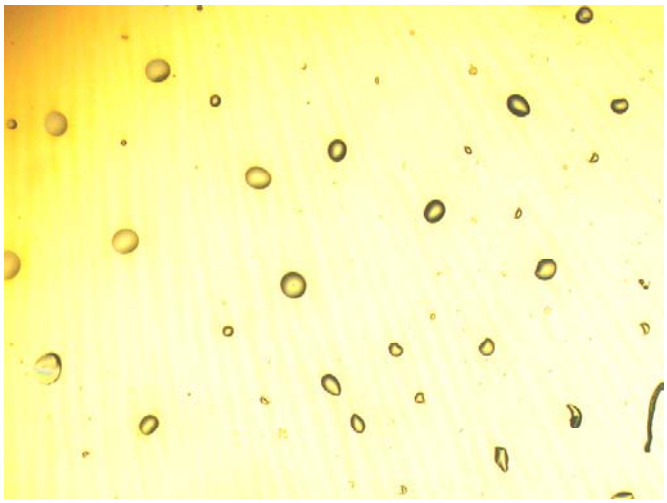


Fig. 4-26 Nodes on the SOD layer after absorbing water
The SOD film surface is rough.

The patterning of the SOD B155 film is studied in the same way as the SOD P507 film. No good pattern can be achieved. The reason is that the SOD B155 film is very sensitive to water and the developer. The patterning of the SOD film is important for the self-aligned planar TFET fabrication proposed in chapter 5.

4.2.5 Application of the SOD in self-aligned TFET fabrication

Spin on dopant layer enables the shallow junction doping. Furthermore, combined with other technologies, the special doping profile can be achieved. Fig. 4-27 shows the application of SOD in the vertical self-aligned TFET fabrication. As can be seen in the final structure of self-aligned TFET, the p^+ doped source and n^+ doped drain are formed simultaneously by diffusion of different types of SOD layers. The channel length can be defined by the etching depth of silicon mesa and diffusion time. The formation of self-aligned gate and n/p diffusion is shown in Fig. 4-27. On the silicon substrate, the N-type SOD is spun on. A n-type dopant drive-in can be processed to get the n diffusion region. The diffusion time depends on the objective junction depth. This means that this diffusion process can be skipped, if necessary. After baking, the silicon wafer is put into the sputter machine and a 200nm Al_2O_3 layer is deposited by reactive sputtering at room temperature. The Al_2O_3 is used as the hard-mask during RIE, and also as the diffusion barrier to separate the n / p SOD when they overlap. Al_2O_3 is patterned using Al etcher at 50-60°C. The Al etcher has etch-stop on the baked SOD P507. RIE is performed to etch the SOD layer and silicon substrate using Al_2O_3 as the hard-mask.

The side wall gate formed using this process is shown in Fig. 4-28. In this process, the SOD layer is used as both the doping source and the passivation layer. The side wall is not straight because of the rough surface of SOD. The formation of side wall gate saves the area for the top contact on mesa.

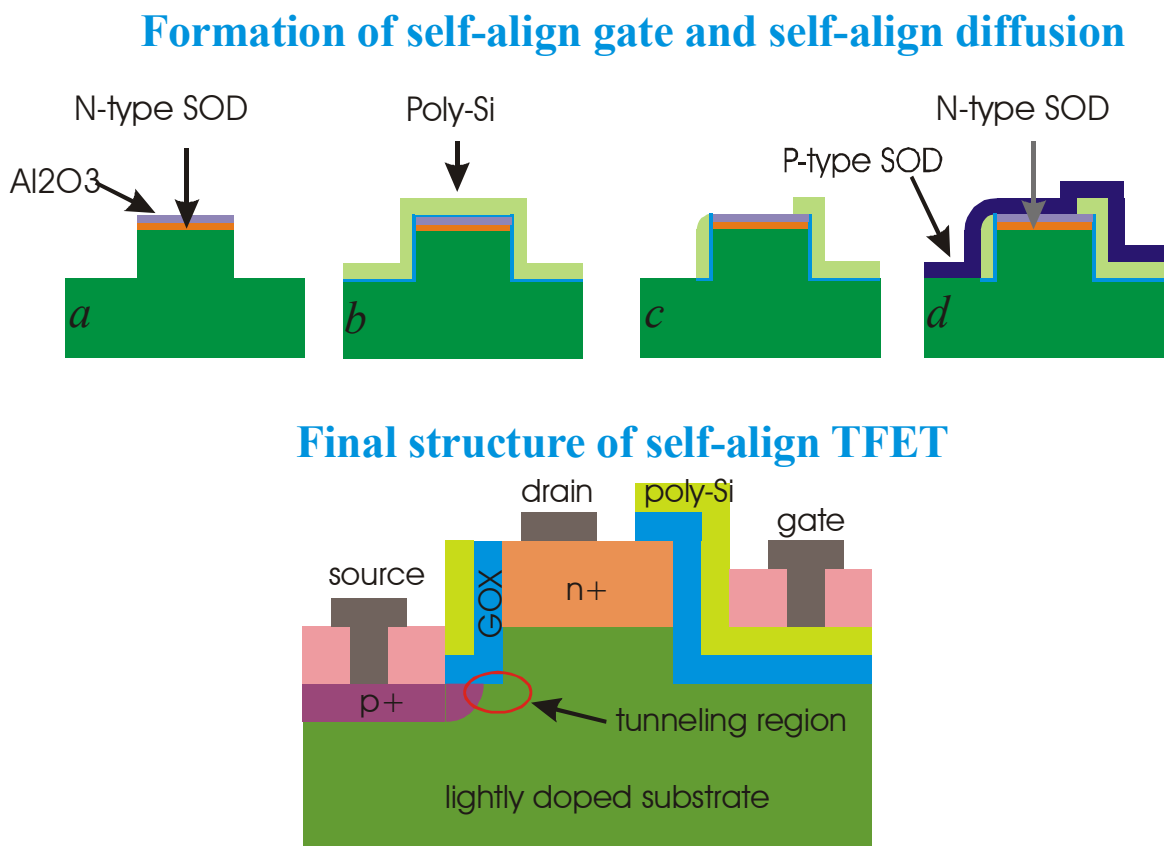


Fig. 4-27 Proposed TFET fabrication processes sequence using SOD diffusion

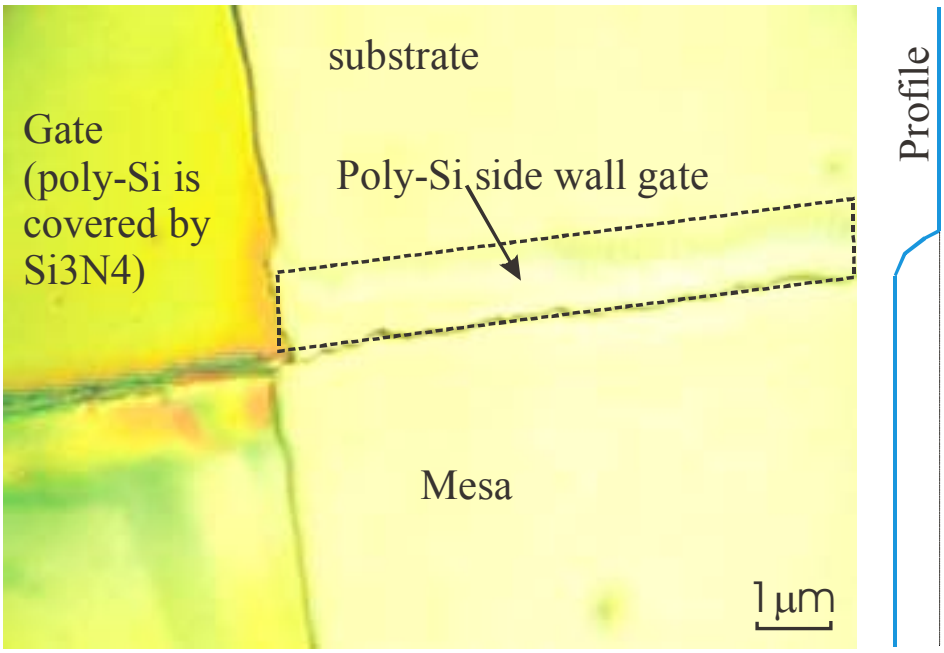


Fig. 4-28 Formation of self-aligned Poly-Si sidewall gate using SOD planarity flow

4.3 Gate oxide formation

The gate oxidation process is essential while fabricating the conventional MOSFET. The properties of the gate oxide determine the threshold voltage, the surface leakage current, and the gate leakage current. According to the ITRS roadmap, the future MOSFET with a channel length below 50nm will need the gate dielectric with equivalent oxide thickness of 1 nm (table 4-8). The reliability problem arises because the silicon oxide become leaky when its thickness is smaller than 3nm. [66] Therefore, the high k materials such as Al_2O_3 should also be investigated for the high performance TFET fabrication.

The gate oxide is traditionally formed by dry thermal growth. The dry oxidation growth rate is much lower than the wet oxidation. Thin silicon oxide with good quality can be grown by this way. The oxidation temperature profile is very important. At a temperature higher than 1000°C, the silicon oxide is flexible and there will be fewer interface charges in it.

In this section, thermal dry oxidation in the normal oxidation oven is investigated. After standard RCA cleaning and the HF dip, the silicon oxide is grown on the n <100> wafer and the thickness of oxide is measured by the ellipsometer. The experimental and the simulated oxidation rates are shown in Fig. 4-29. The experimental results match with the simulated results very well. From this figure, the 3 nm silicon oxide can be formed at 950°C for 1 minute. However, the electrical strength of such an oxide layer is not as good. From the figure for the *I-V* characteristics of oxide with various thicknesses grown at 950°C (Fig. 4-30), the soft breakdown starts at the lower voltage for the thinner oxide. For the 3.2 nm oxide, the soft breakdown starts immediately with the applied voltage. The 6.33 nm and the 5.03 nm gate oxide is reliable in this case.

The gate oxidation at around 900°C (the temperature setting scale of the oxidation oven is "50") for 4 minutes is also tried. The oxide with 5-6nm thickness is obtained which is used as the gate oxide in the second version planar TFET.

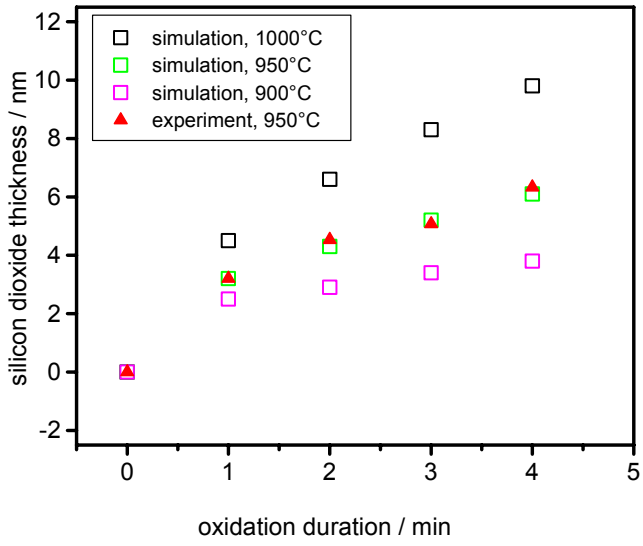


Fig. 4-29 Experimental and simulated oxidation rates in the normal thermal oxidation oven

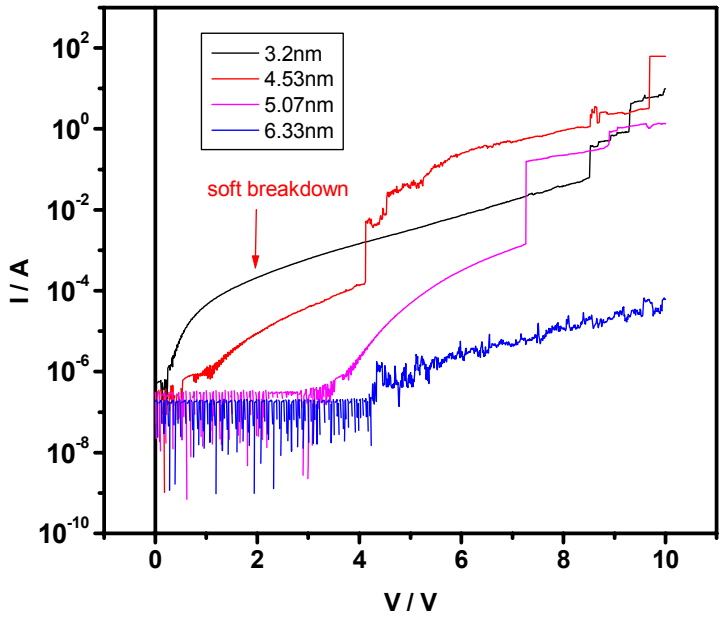


Fig. 4-30 *I-V* characteristics of the oxide with various thicknesses grown at 950°C

Table 4-8 Roadmap for the gate dielectrics technology, from ITRS 2000

Proposed Year of First Product Shipment Technology Node (A1)	1999 180 nm	2000	2001 130 nm	2002	2003	2004 90 nm	2005	DRIVER
MPU/ASIC Gate Length (nm)	120	100	90	85-90	80	70	65	MPU/ASIC
Final Physical Bottom Gate Length after Etch, Proposed (nm)[A2]	120	100	90	80	70	65	60	MPU/ASIC
Equivalent physical oxide thickness T_{ox} (nm) [A]	1.9–2.5	1.5-1.9	1.5–1.9	1.5–1.9	1.5–1.9	1.2–1.5	1.0–1.5	MPU/ASIC
Gate dielectric leakage at 100°C (nA/μm) High-performance [B]	7	8	10	10	13	16	20	MPU/ASIC

4.4 Summary

As described in the simulation results (see Chapter 3), heavy p / n doping concentration, thin gate oxide, and sharp doing profile are the keys for fabricating a high performance TFET. After the required process development described in this chapter, the following technologies are prepared for the fabrication of TFET:

1) The vertical silicon trench etching is developed for fabricating the vertical TFET, the vertical mesa diode, the self-aligned gate, and the shallow trench isolation (STI).

2). Heavy n and p doping concentration can be achieved by the diffusion of SOD layers. The surface concentration of both n and p doping is higher than 2×10^{20} cm^{-3}. Using the RT-diffusion, the ultra-shallow junction can be obtained. The sharp doping profile can also be achieved by the RT-diffusion.

3). The dry gate oxidation at 900°C and 950°C is investigated and the stable 5nm gate oxide is fabricated.

4). The patterning and thickness control of the SOD layers is realized which will be helpful for the development of the self-aligned TFET fabrication process.

Chapter 5

TFET Fabrication and Characterization

Parallel to the process development, the vertical mesa diode, the vertical TFET, and the planar TFET are fabricated. In this chapter, the fabrication and the characterization of the diodes and TFETs will be discussed.

In this thesis, four versions of TFETs are fabricated including the vertical TFET and the planar TFET. As shown in table 5-1, the first version "transistor" is without doping because at that moment the SOD process is not calibrated. This run was to test the compatibility between the TFET device and fabrication processes. The second version TFET also is a vertical transistor. The dopant diffusion is realized by the SOD out-diffusion and a self-aligned process is developed. Both the third and the fourth versions are planar transistors. In the fabrication of TFET versions 1 to 3, the RTP system is not available. Therefore, the p and n type diffusion is processed in the normal thermal diffusion oven. When the RTP process has been finished, the fourth version TFET is launched and finally the planar TFETs with good performance are fabricated.

Table 5-1 Overview of four versions of TFETs fabricated in this thesis

	Version 1	*Version 2*	*Version 3*	*Version 4*
TFET type	Vertical TFET	Self-aligned vertical TFET	Planar TFET	Planar TFET
Mask design	4-mask process, emulsion masks	4-mask process, emulsion masks	6-mask process, emulsion masks	8-mask process, chromium masks
Diffusion difference	Without dopant diffusion process	SOD diffusion in the normal thermal oven	SOD diffusion in the normal thermal oven	RT-Diffusion
Motivation	Calibrate the process for the vertical TFET fabrication	Develop the self-aligned process to reduce the mesa area	Improve the gate oxide quality by avoiding the boron inter-diffusion problem	Fabricate the high performance complementary TFET

5.1 Silicon tunnel diode fabrication

In order to calibrate the rapid thermal diffusion of SOD, the vertical silicon tunnel diodes are fabricated. Fig. 5-1 is the schematic structure of the vertical diode fabricated using the out-diffusion of the SOD films. The silicon substrate is p^+ doped (<5mΩ·cm). Two steps of rapid thermal diffusion are performed. First, the wafer covered by SOD B155 film is diffused for 5

minutes at 1050°C to enhance the p^+ doping. Then, the SOD P507 diffusion for 45 seconds at 1050°C is used to form the n^+ silicon layer. The mesa etching is done by the RIE to isolate the diodes. For the *I-V* measurement, the top metal is also patterned. The p^+ substrate is used as back contact. The electrical characteristics of the diode J-2 (diode wafer #14) are shown in Fig. 5-2a. Although the negative differential resistance is not observed, the band-to-band tunneling is observed in the reversed diode. As shown in equation 3-1, the band-to-band tunneling can be verified by the linear plot, when using $\log(I/V^2)$ as the Y axis and 1/V as the X axis. Fig. 5-2b shows the linear fitting of $\log(I/V^2)$ vs. 1/V for diodes. When the diode is reverse biased, $\log(I/V^2)$ is proportional to 1/V. The band-to-band tunneling is verified. By using different diffusion sequences of n / p type SOD films, several diode wafers are fabricated. The electrical characteristics and the BTBT tunneling current linear fitting for the diode #7-C5 is shown in Fig. 5-3. The band-to-band tunneling is observed as well.

In the normal diode, the reversed current is much lower than the forward current. However, in the diode with heavy n and p doping at both sides of the p-n junction, the band-to-band tunneling will result in a large backward current. As shown in Fig. 5-3, the backward current caused by band-to-band tunneling current is almost of the same order of magnitude as the forward current. That means the doping concentration at both sides of junction is quite high. Therefore, for the TFET fabrication, a lightly doped or intrinsic region is needed to separate the heavy n and p regions to suppress the backward leakage current.

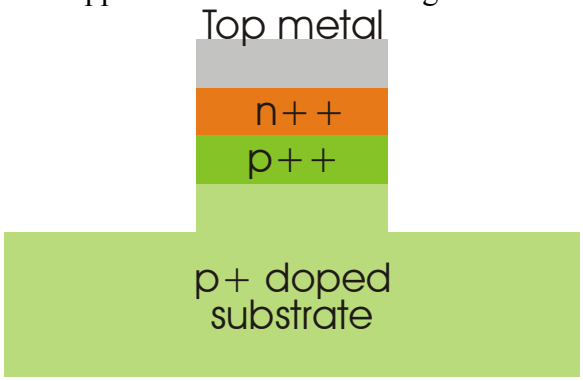
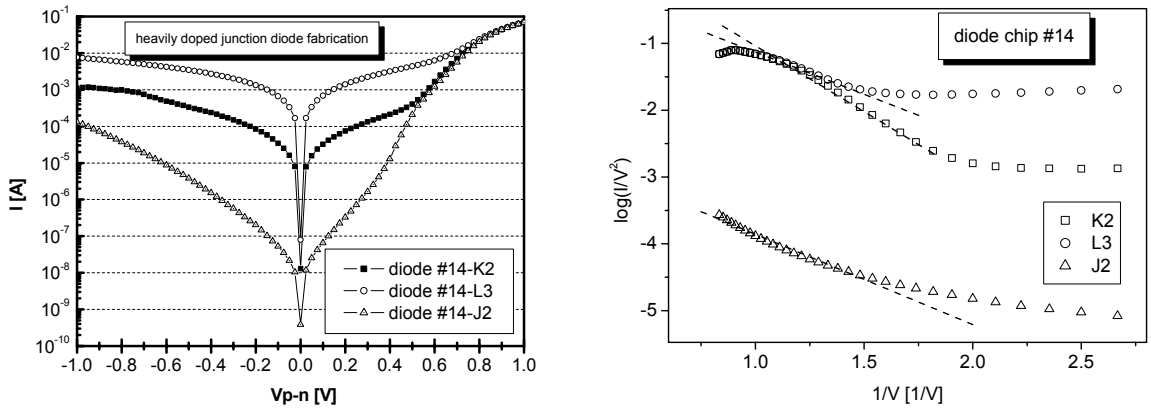


Fig. 5-1 Schematic structure of the vertical diode fabricated using the out-diffusion of SOD



a b

Fig. 5-2 Characteristic of several diodes fabricated in the RTP chamber using p and n type diffusion on p^+ substrate (left); Plot using $\log(I/V^2)$ as the Y axis and 1/V as the X axis, data are derived from the reversed diode region (right). (from diode wafer #14)

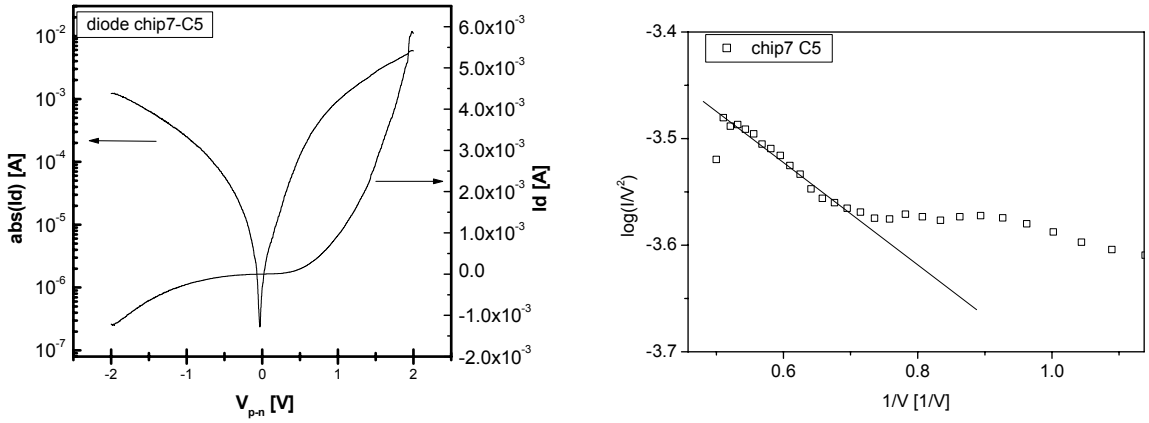


Fig. 5-3 Electrical characteristics and linear fitting using $\log(I/V^2)$ as the Y axis and 1/V as the X axis. (diode #7-C5)

5.2 Vertical TFET fabrication

Based on the different doping methods in TFET fabrication, TFETs can be classified into three categories: the MBE doped TFET, the implantation doped TFET, and the diffusion doped TFET. In principle, the best characteristics can be achieved in the MBE doped TFET because of the sharp doping profile and the heavy p-type doping in the MBE layers. The diffusion doping method enables very high doping levels at the silicon surface. Combined with the rapid thermal process, the shallow doping junction with the high doping level is possible. The implantation doped TFET was tested by Reddick *et al.* [70]. In the summary of their work, the MBE doping method and the RTP technology are suggested.

In this section, the vertical MBE-TFET and the vertical SOD-TFET fabrication will be discussed. The high performance MBE-TFET was fabricated in Uni-Bw München using the MBE thechnology. [13-16] Here, we fabricate the SOD-TFET to compare it with the MBE TFET fabricated in Uni-Bw München. Therefore, the first version vertical TFET has no doping, but fabricated with the similar process to the MBE-TFET. In this way, the mesa etching, gate oxidation, passivation and other processes can be tested for process improvements. Developed from the first version vertical TFET, the vertical self-aligned SOD-TFET is fabricated.

5.2.1 4-mask vertical TFET fabrication for process calibration

The working vertical MBE-TFET was fabricated by nano & micro technologies in Uni-Bw München. The structural design of the vertical MBE-TFET is shown in Fig. 5-4. As mentioned in ref. [13-16], the process for the vertical TFET fabrication is described as: after the MBE layer growth, the oxidation is done and the gate poly-Si is patterned. In the MBE doping TFET, the defects caused by heavily doping may increase the excess leakage current. A larger mesa area will result in a larger leakage current. A larger gate to source overlap area results in a larger gate leakage and parasitic capacitance as well.

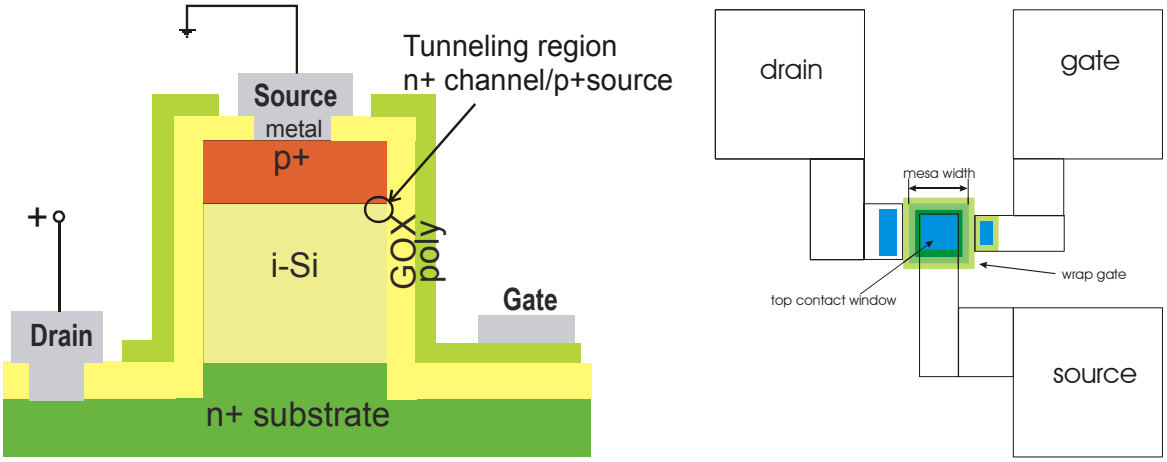


Fig. 5-4 Structural design of vertical MBE doping TFET

Here the similar process is developed to fabricate the similar vertical TFET, but with SOD diffusion in our clean room at TUM. A 4-mask process is designed for the vertical TFET fabrication. The process sequence and the corresponding patterns are shown in Fig. 5-5. After the RCA cleaning, the silicon mesa is patterned by RIE. Then gate oxide is formed by dry oxidation at 1000°C. Next, the gate poly-Si is sputtered and patterned using RIE. After the Si_3N_4 passivation layer deposition, the contact window etching and metallization are done. As the doping process was not calibrated at the beginning, the "transistors" without doping were fabricated just to test the process, but the electrical characteristics were not measured.

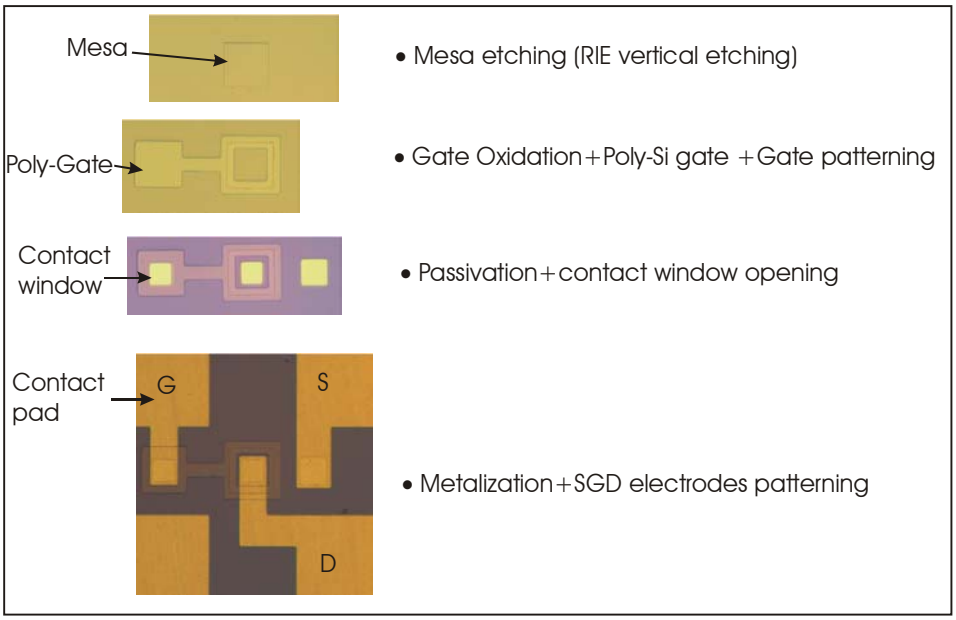


Fig. 5-5 Process sequence and corresponding patterns in the fabrication

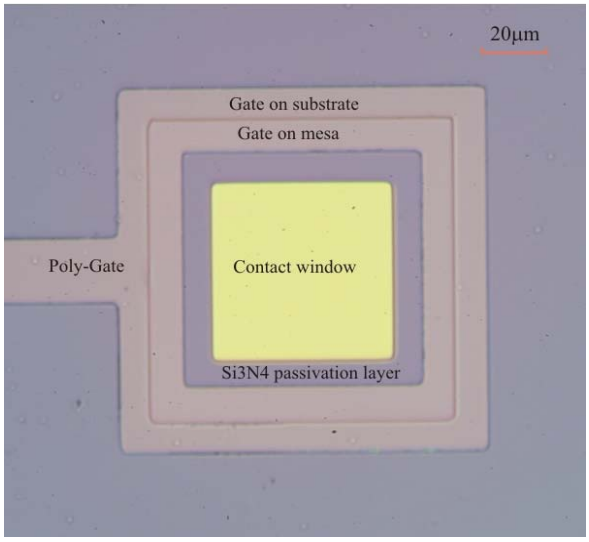


Fig. 5-6 Structure of the vertical TFET mesa

Fig. 5-6 shows the structure of the vertical TFET mesa. Around the mesa is the poly-Si gate. The overlap is necessary to cover the side of the mesa. The contact window is opened in the middle of the mesa top. Thus, the large top mesa area is needed to allow enough space for the contact hole and gate overlap. The gate material is sputtered Si using silicon as target. 200nm thick Si is sputtered at 200W onto the gate oxide. The quality of sputtered Si is not so good. As can be seen in Fig. 5-7, the sputtered Si thin film has several cracks and cannot stick onto the substrate very well. In addition, the high energy of 200W sputtering may damage the gate oxide. Thus, LPCVD poly-Si and evaporated Al are suggested to be the gate materials.

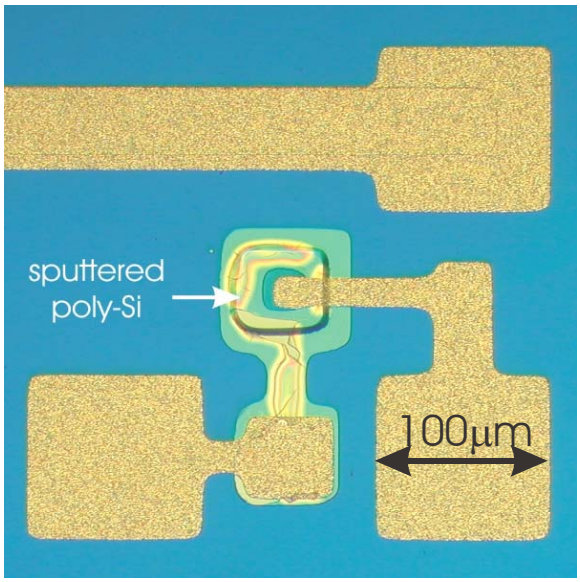


Fig. 5-7 Device with poor quality sputtered Si gate

In the first fabrication design, there are some technological problems to be solved. 1). The G/S and G/D overlap should be reduced to suppress the gate leakage current and the D-S leakage current. As mentioned in Ref. [16], the drain-source leakage current can be reduced by shrinking the mesa area. 2). LPCVD Poly-Si or metal gate should be applied as gate material.

5.2.2 4-mak self-aligned gate vertical SOD-TFET

5.2.2.1 Fabrication details

In this TFET fabrication run, the n and p type SOD films are used to form the n and p doped regions. The self-aligned process is also developed to minimize the mesa area.

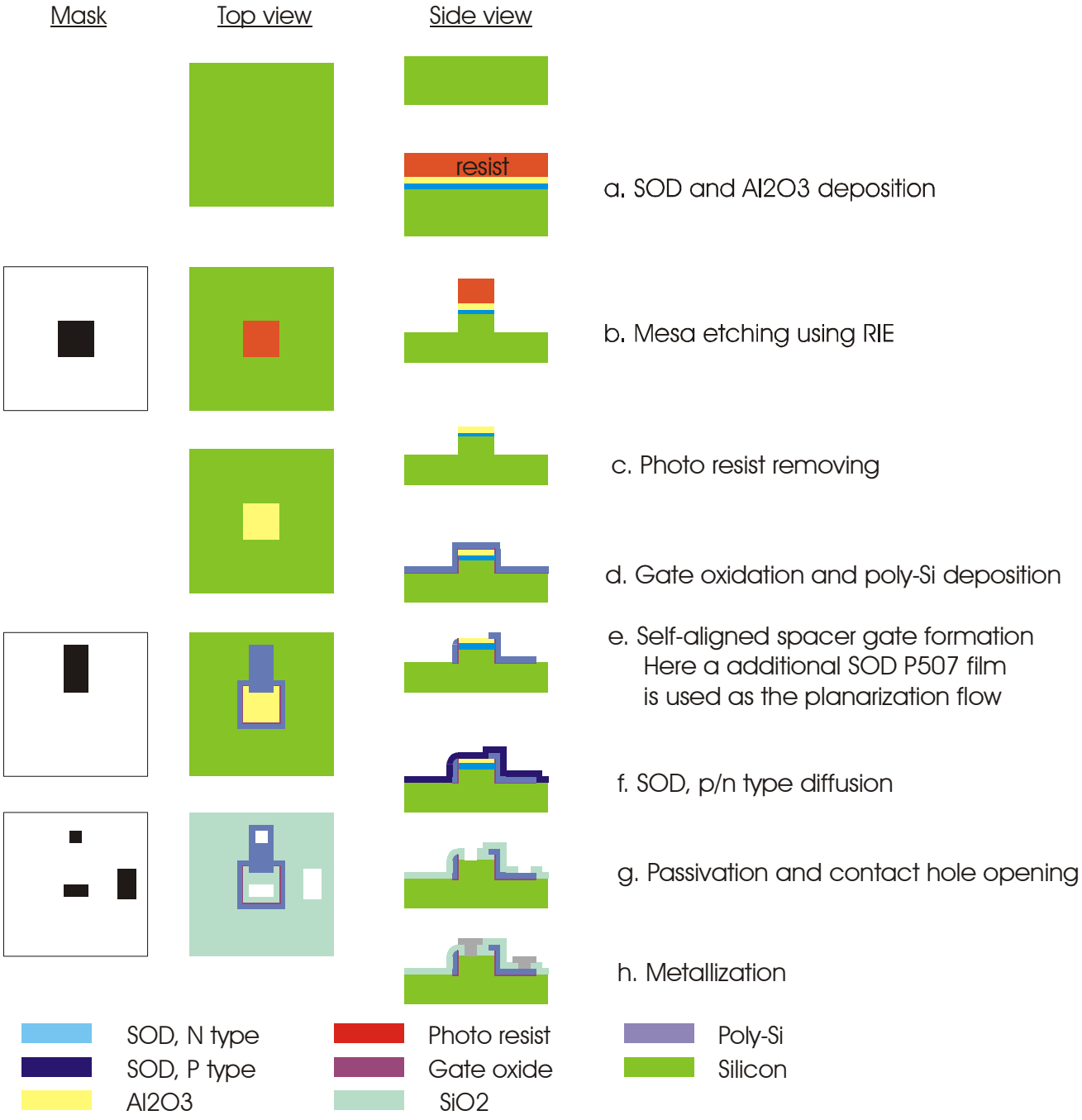


Fig. 5-8 4-mask process sequence of the vertical self-aligned SOD-TFET

The fabrication process sequence of the vertical TFET using the SOD diffusion is shown in Fig. 5-8. The starting material is a lightly n doped <100> silicon wafer. After RCA cleaning, the SOD P507 precursor is spun on to the silicon substrate. The thickness of the SOD P507 film is 160nm. An Al_2O_3 layer of 270nm thickness is sputtered at room temperature onto the SOD layer to form the hard mask, also as the diffusion barrier for n/p SOD films. Al_2O_3 is patterned by wet etching. The mesa etching is done by RIE with a Cl_2 flow rate of 6sccm for 30 minutes using the Al_2O_3 layer as the hard mask. The etching depth into silicon is 1000nm. The gate oxidation is done in the normal oxidation oven at 950°C for 4 minutes. Then, a poly-Si layer is deposited using the LPCVD as the gate material. A planarity process is done using SOD P507 film. As shown in Fig. 5-9, the spacer surrounding the vertical mesa is formed after the planarity process. After the lithography process for the gate patterning is finished, the wafers are placed into the RIE chamber for vertical etching. The etching back in the RIE system will result in a self-aligned spacer gate. After p-type diffusion using SOD B155 and SOD removing, the self-aligned gate and the self-aligned source/drain can be formed. The diffusion is performed at 1000°C for 7.5 minutes in the normal diffusion oven. As shown in Fig. 5-10, the G-D and G-S overlap are reduced because of the self-aligned process. The p^+ and n^+ doped regions are also separated by the self-aligned gate. The vertical TFET with the 5μm mesa width is fabricated using the emulsion mask. Fig. 5-11 shows the device after the passivation layer deposition and the contact window lithography. The schematic final structure of this kind of vertical TFET is shown in Fig. 5-12. The source and drain are also self-aligned. There is no poly-Si gate on the mesa top. The overlap of G-D and G-S can be reduced using this process design. The channel length of this TFET depends on the depth of the mesa vertical etching, the width of spacer, and the diffusion smear-out length. In this process, the channel length is less than 2μm because the mesa height is 1μm and the spacer width is also about 1μm.

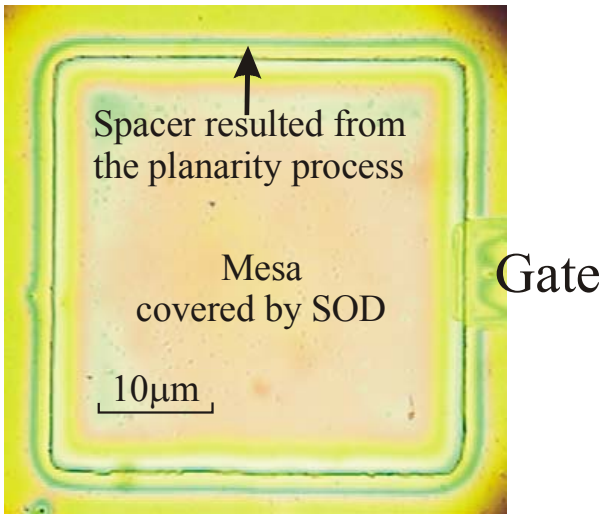


Fig. 5-9 Spacer surrounding the vertical mesa after the planarity process

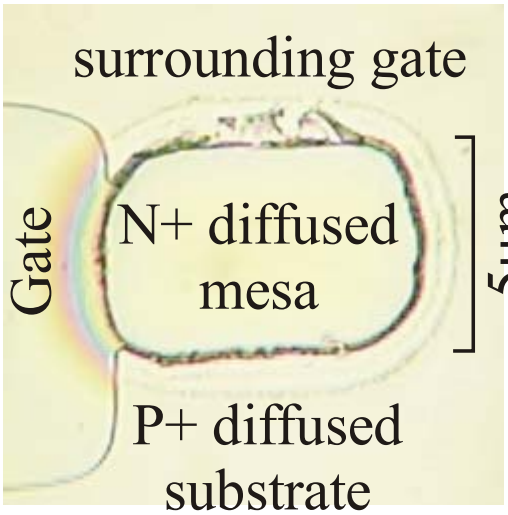


Fig. 5-10 Self-aligned gate and the self-aligned S/D after the etching back and the diffusion process

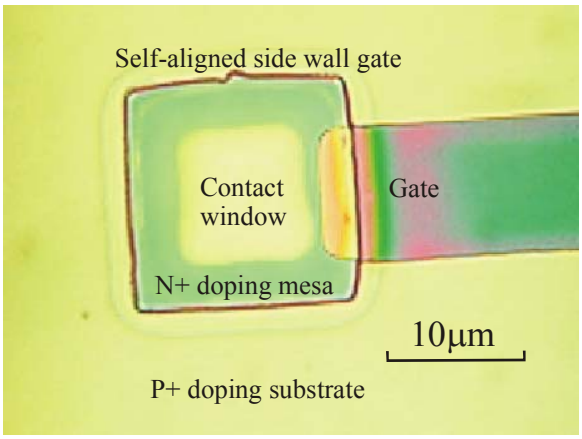


Fig. 5-11 Self-aligned device after passivation layer deposition and contact window lithography

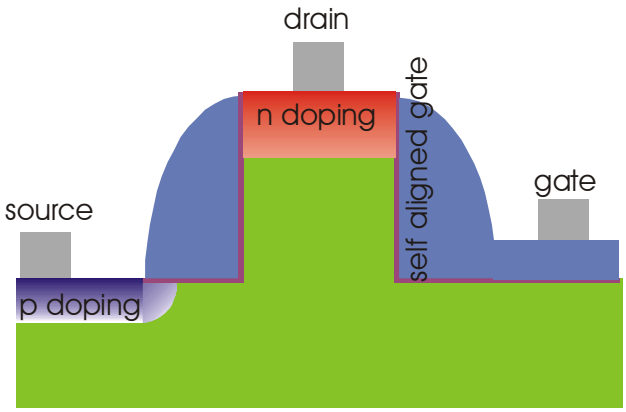


Fig. 5-12 Schematic final structure of the vertical transistor with the self-aligned spacer gate

5.2.2.2 Electrical measurements

The electrical characteristics of the self-aligned vertical SOD-TFET are measured. In Fig. 5-13, the transfer characteristics of a vertical TFET fabricated using the SOD diffusion are shown. The weak gate control with one or two decade I_{on}/I_{off} is observed at low supply voltage. With V_{ds} increasing, the leakage current increases rapidly. The output characteristics of the transistor are shown in Fig. 5-14. The shift of the current valley is caused by a gate leakage. The gate leakage current vs. V_g for this TFET is shown in Fig. 5-15. The high gate leakage current is observed. The soft breakdown starts immediately with the increasing gate voltage. Thus, the gate oxide quality should be improved.

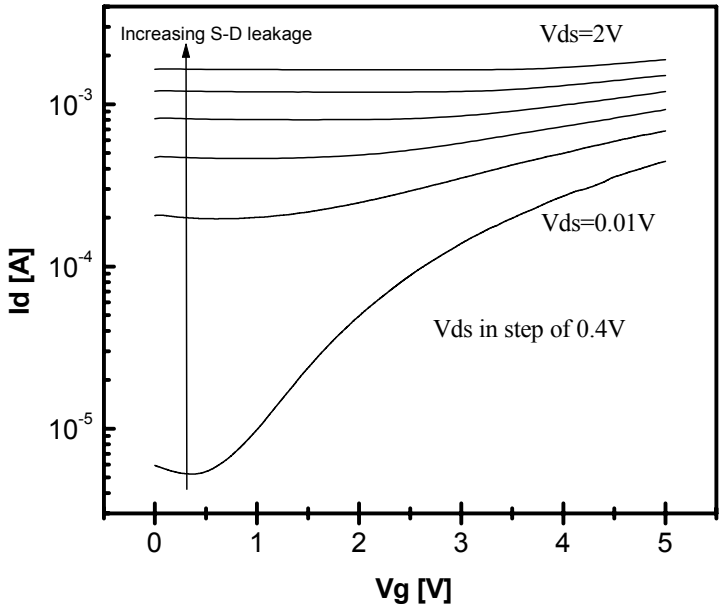


Fig. 5-13 Transfer characteristics of a vertical SOD-TFET

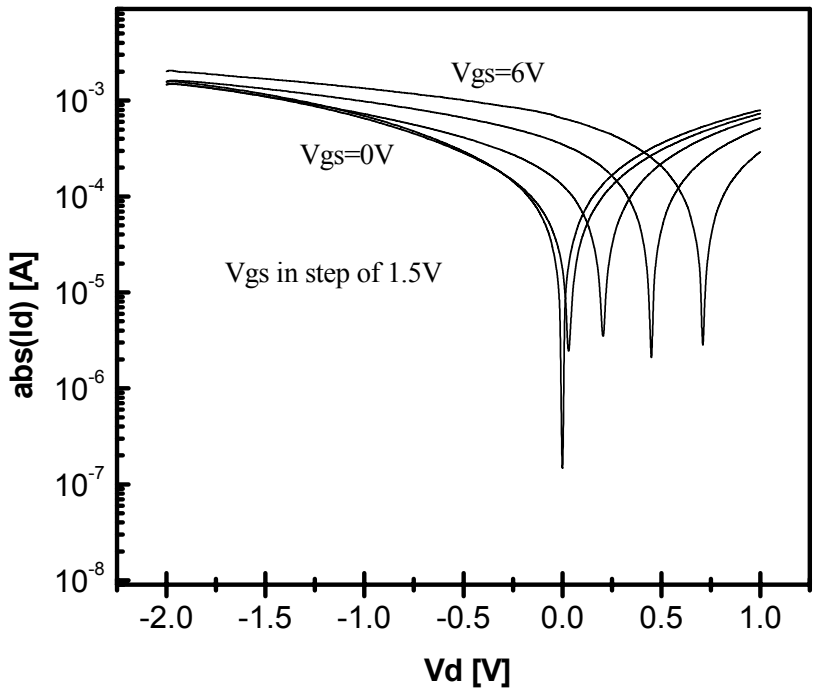


Fig. 5-14 Output characteristics of a vertical SOD-TFET

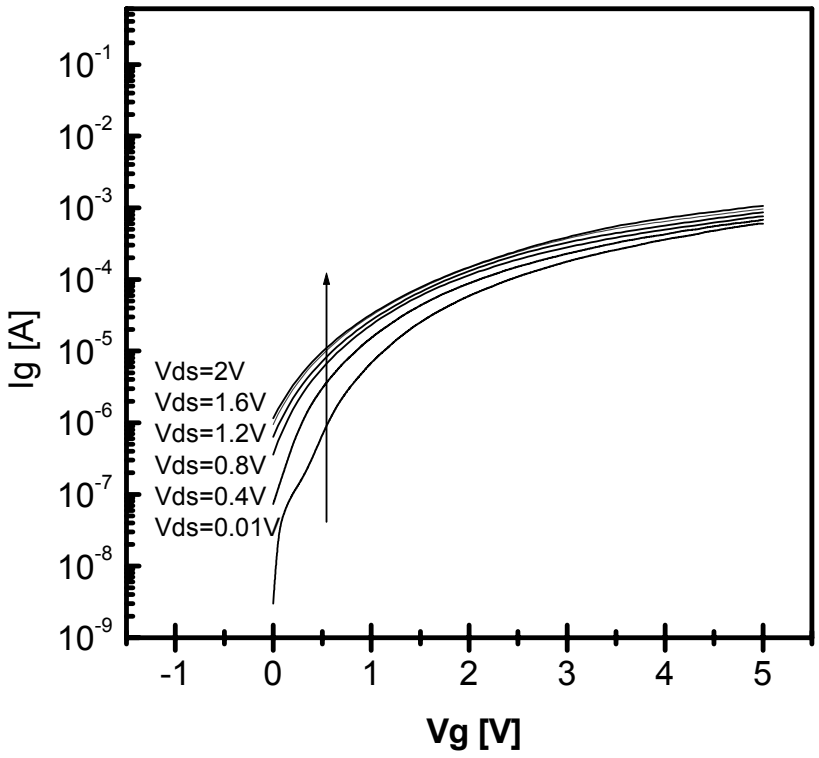


Fig. 5-15 Dependence of the gate leakage current on V_g. The gate oxide is formed at 950°C for 4 minutes.

5.2.3 Discussion on the self-aligned vertical SOD-TFET

In the self-aligned vertical SOD-TFET, the poly-Si gate is patterned by vertical etching by the RIE. Using the SOD P507 film as planarization flow, the spacer gate length is about 1μm. Without the SOD P507 flow, the width of the poly-Si spacer gate can be smaller than the mesa height (Fig. 5-8). Adjusting the mesa height and the etching profile, the width of the physical channel length of TFET can be adjusted and the fabrication of the deep sub-micron SOD-TFET is possible. However, the p-diffusion is performed after the gate oxidation process. The boron atoms will diffuse into the thin gate oxide and degrade the gate oxide [71]. To avoid this problem, an additional wet oxidation process should be introduced just after the gate poly-Si deposition. On the other hand, the planar TFET where the gate oxidation is done after all the diffusion processes can overcome this problem. Therefore, the planar TFET is designed and fabricated in the following section.

5.3 6-mask planar SOD-TFET fabrication

As illustrated by simulation in section 3.6, the planar TFET fabricated by the out-diffusion of SOD is possible. Therefore, the planar SOD-TFET is designed and fabricated.

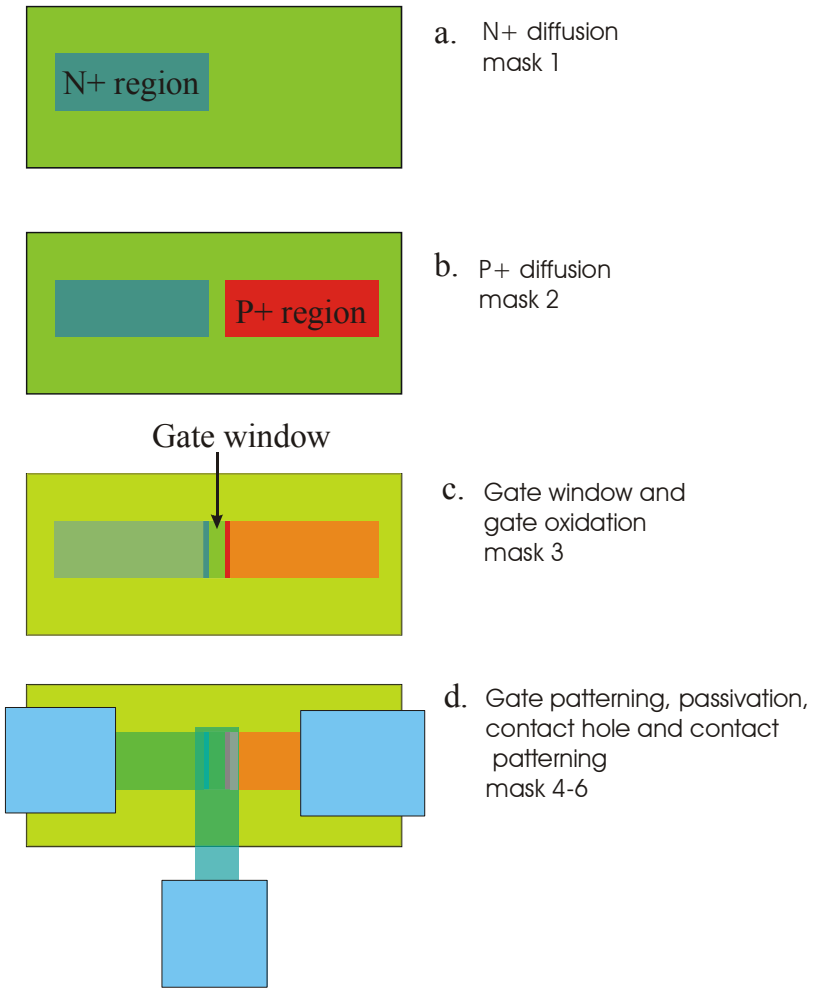


Fig. 5-16 6-mask fabrication process of the planar SOD-TFET

5.3.1 Details of the device fabrication

The planar TFET is designed as a transistor with the n and p diffusion regions standing side by side on a n^- doped substrate. As shown in Fig. 5-16, after the RCA cleaning, the wafers are placed into the oxidation oven. The first LOCOS of 620nm is grown at 1200°C for 30 minutes by wet oxidation. The windows are opened for the n-type diffusion. After the n diffusion and the SOD film removal, the secondary LOCOS of 370nm thickness is grown at 1000°C for 30 minutes by wet oxidation. Then, the windows for the p-type diffusion are opened. The p^+ doping is processed in the normal diffusion oven at 1000°C for 10 minutes. Next, the SOD layer is removed and a gate window is opened for thermal gate oxidation. The gate oxide is formed at 950°C for 5 minutes. The Pt metal with 200nm thickness is used as gate material in these transistors. The S/G/D metal is a combined layer of 10nm Ti and 200nm Pt. Because of the inert chemical character of the noble metals, the accelerated Ar^+ ion beam in the RIE system is applied to etch these metals.

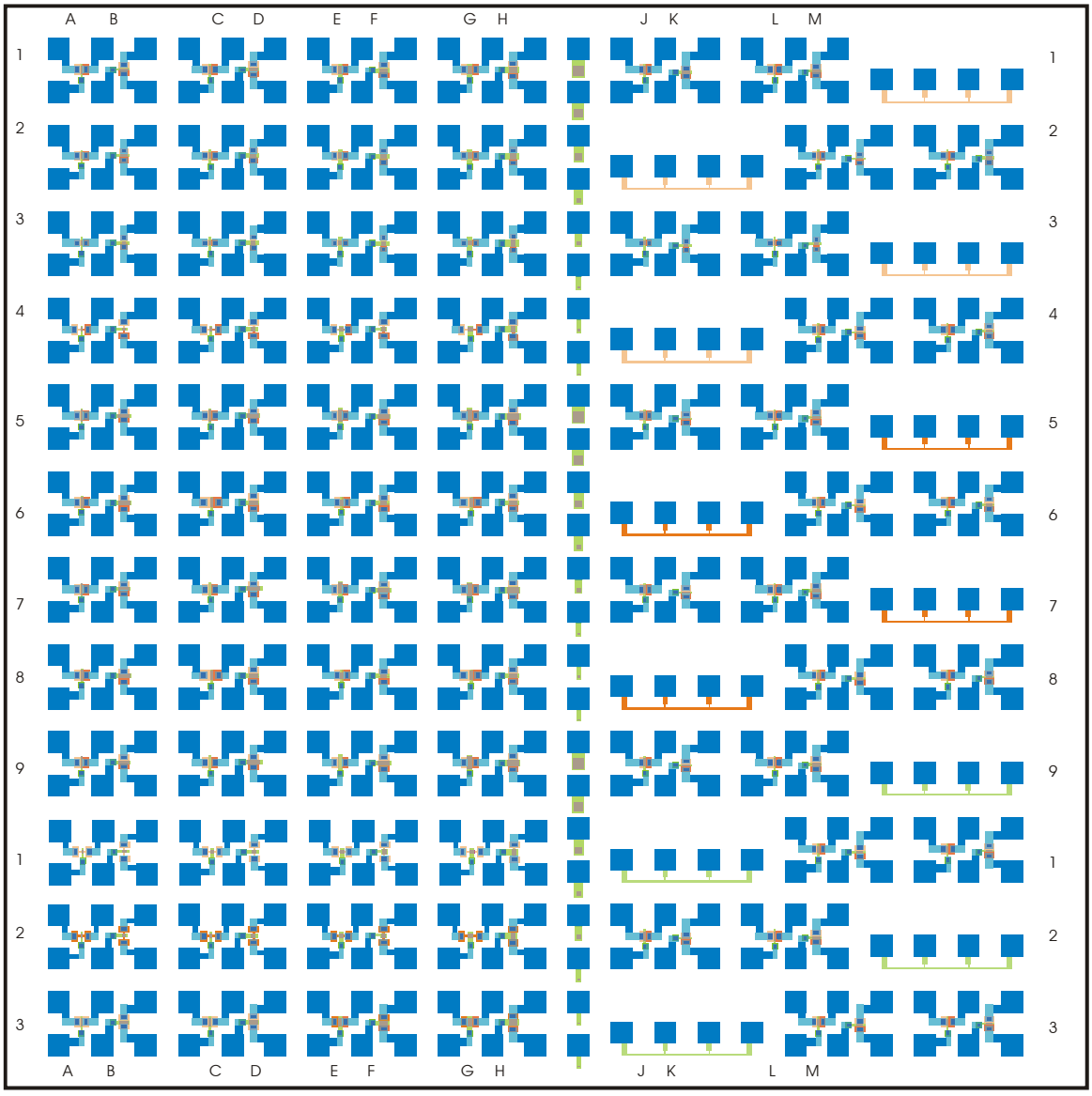


Fig. 5-17 Mask set designed for the 6-mask planar SOD-TFET fabrication

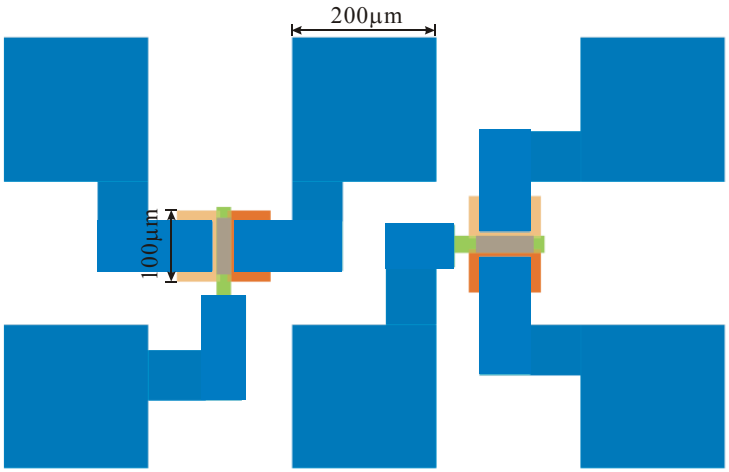


Fig. 5-18 Plot of the planar TFET in the mask set

In this fabrication, 6 masks are used in total. Fig. 5-17 shows the mask set designed for the first version planar TFET. Fig. 5-18 is the plot of the planar TFETs inside this mask. The contact pad size is 200µm×200µm. The channel length varies from 10µm to 100µm.

5.3.2 Device characterization and discussion

The planar TFETs are measured with the positive biased n^+ doped region and the grounded p^+ doped region. The huge leakage source-drain leakage current is measured. As an example, Fig. 5-19 shows the transfer characteristics of the fabricated planar TFET. A tremendous leakage current was found. There is only a very weak current control. From the gate characteristics shown in Fig. 5-20, the gate leakage current is rather low. The good quality gate oxide can be fabricated using this design.

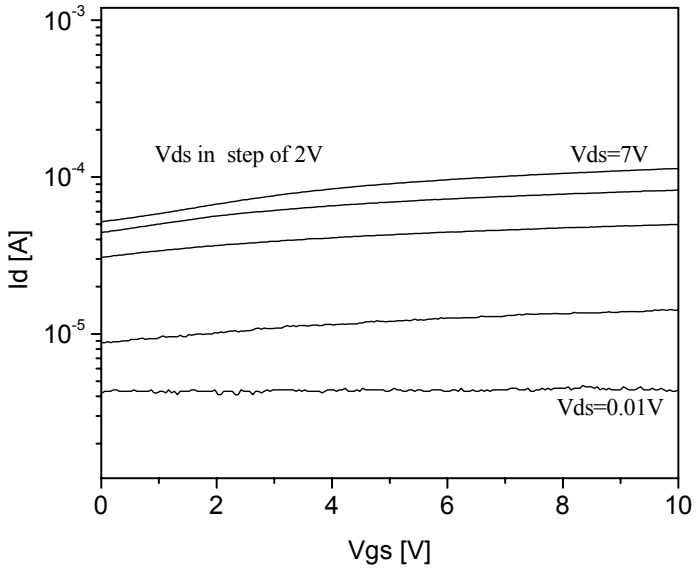


Fig. 5-19 Transfer characteristics of the planar TFET fabricated using 6 masks

The high S / D leakage current may be caused by the surface leakage current or the thermal-generation current from the n^- substrate. The problems in this run are: 1) The sputtered SiO_2 passivation layer may cause the surface leakage current due to low resistance and surface stress. 2) The diffusion time is too long and the dopant goes through the barrier LOCOS into the channel region. In order to suppress the surface leakage current, a Shallow Trench Isolation (STI) mask is designed in the second version planar TFET. The Rapid Thermal Diffusion (RTD) technology is also developed to reduce the thermal budget. In addition, the fabrication process and the mask set without the passivation layer are designed.

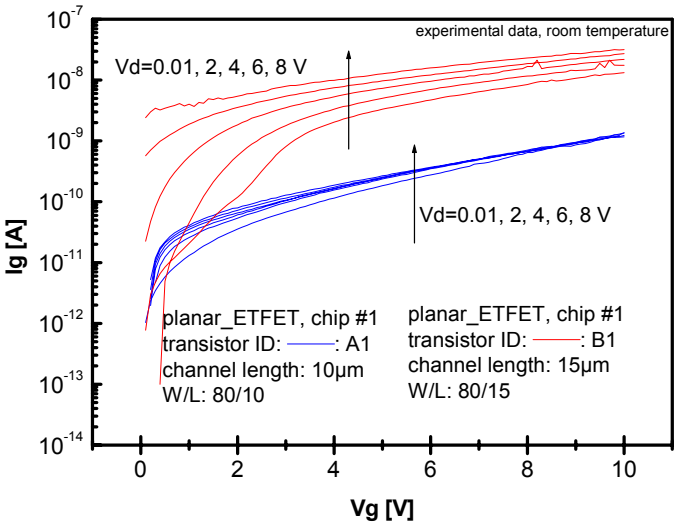


Fig. 5-20 Gate leakage current of the 6-mask planar TFET

5.4 8-mask planar SOD-TFET fabricated using RTP

5.4.1 Mask design

In the second version planar TFET, a STI mask is designed to suppress the leakage current. If we use this STI design on the SOI wafer, the leakage current will be extremely low. In addition, a p-well mask is added in order to obtain a complementary planar TFET circuit. Therefore, an 8-mask process is designed and tested. The overview of this mask for the planar TFET is shown in Fig. 5-21. This mask is drawn using "Mentor Graphics" in the Institute of Physics, Uni-Bw München. In this mask, the TFET with the single metal gate and the split metal gate are designed. In addition, the diode, PMOS, NMOS, and many electrical test structures are designed. On the top right corner of this mask, there are the single stage and the 3-stage inverters composed by TFET and PMOS.

The design of the single planar TFET is shown in Fig. 5-22. The layout of the single TFET is similar to the first version planar TFET. Some TFETs are surrounded by STI rings to suppress the surface leakage. The PTFETs are designed by placing the TFETs in the p-well.

The dimension variation of the TFETs design across the mask is shown in table 5-2. The normal design is with 2µm security design and the gate window is wider than the diffusion

windows. For security, 5µm security width is used for some TFETs. The TFETs with a gate window narrower than the diffusion windows are also designed. The details of the security width and other structural variations on this mask can be found in appendix B.

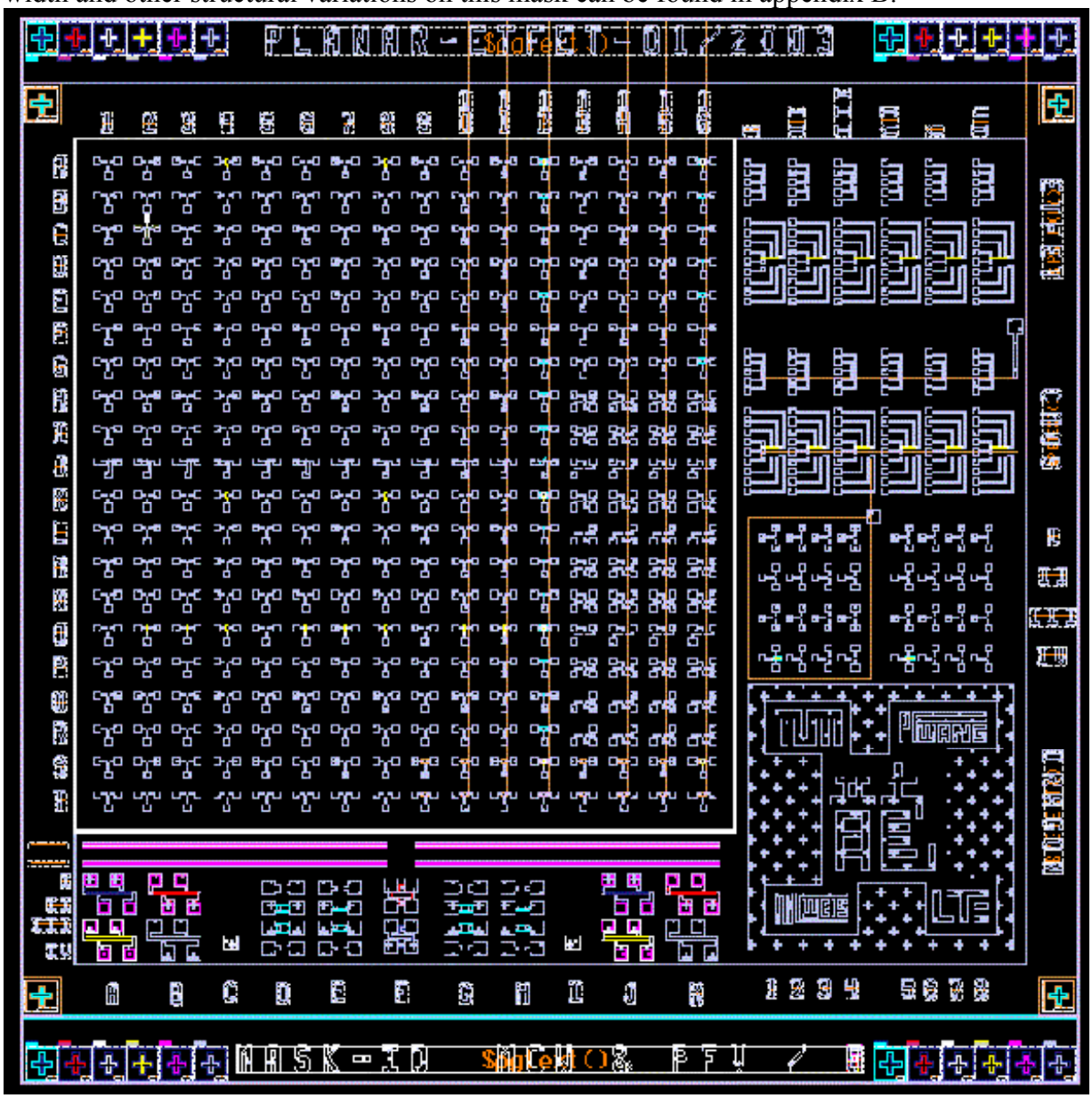
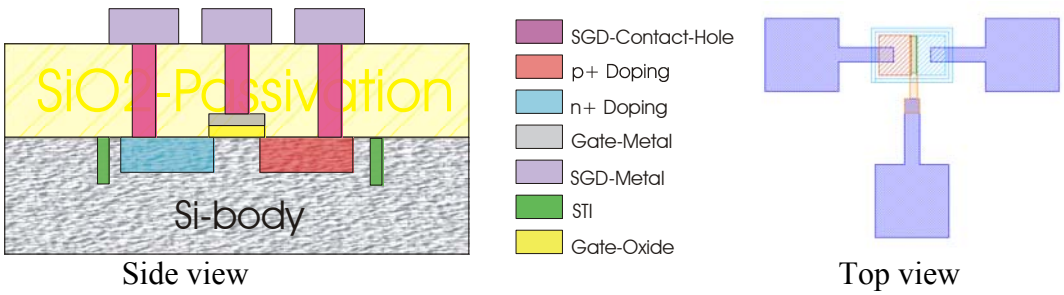


Fig. 5-21 Mask set for the planar TFET with STI and TFET circuits



Side view Top view

Fig. 5-22 Single planar TFET with STI

Table 5-2 Planar TFET design rules in the second version planar TFET chromium mask

	Group 1-4, (5-8 are a repetition of 1-4)	Group 9-12 are a repetition of 1-4. But 9-12 is with STI)	Group 13-16
A to F	1μm<W<50μm, 1μm<L<50μm (2μm security)	1μm<W<50μm, 1μm<L<50μm (2μm security, with STI)	1μm<W<50μm, 1μm<L<50μm (2μm security; with STI)
G	P and N regions overlap	P and N regions overlap	Large W/L, short channel
H			Split gate
I	Large W/L, short channel	Large W/L, short channel	
J	45° rotation	45° rotation	
K L M N	6μm<W<50μm, 2μm<L<50μm (5μm Security)	6μm<W<50μm, 2μm<L<50μm (5μm Security)	
O P Q	Doping region is narrower than gate window	Doping region is narrower than gate window	
R			P and N overlap
S T	Special design	20μm<W<50μm, 6μm<L<50μm (2μm Security)	20μm<W<50μm, 6μm<L<50μm (2μm Security)

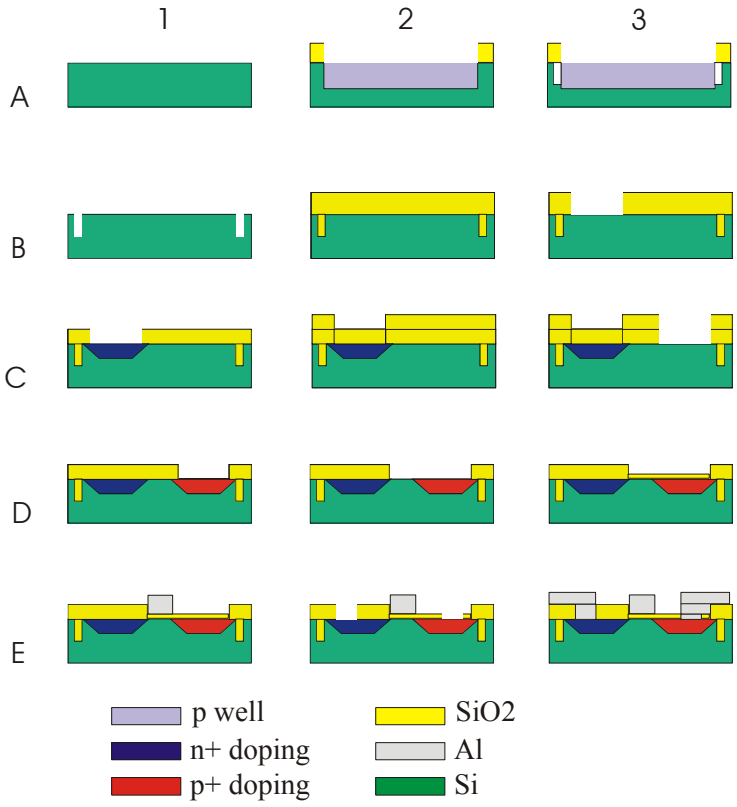


Fig. 5-23 Process sequence for the second version TFET fabrication

5.4.2 Process sequence design

The process sequence of this version planar TFET is similar to the 6-mask planar SOD-TFET fabrication. However, the p-well diffusion is added here to obtain a complementary TFET. As shown in Fig. 5-23, the mask oxide is formed and the region is defined to perform the p-well diffusion (process A1-A2). Then, a second wet oxide is formed as a hard-mask for the STI etching and results in the pattern A3. For NTFET, the p-well is not needed. In this case the STI etching will result in a pattern like B1. The n^+ diffusion (B2-C1) and the p^+ diffusion (C2-D1) regions are formed sequentially. Steps D2 to E1 correspond to the gate window opening, the gate oxidation and the gate metal patterning. After the contact windows opening and the metallization (E2-E3), the device fabrication is finished.

5.4.3 Experimental details of fabrication

The second version planar TFET is fabricated on the n^- doped substrate with the resistivity of 30.0 -37.0 Ω·cm. The first oxidation is performed at 1000°C for 70 minutes in the new oxidation oven (ATV). The silicon oxide thickness of 540nm is measured by the ellipsometer. The p-well is formed using the diffusion of SOD B150 at 1100°C for 60 minutes in the normal thermal diffusion oven. After the removal of SOD B150 glass, the secondary LOCOS oxide is formed by wet oxidation at 1200°C for 35 minutes. This layer is used as the hard mask for the STI etching in the RIE system. The STI with 1μm depth is formed at 500V voltage for 25 minutes with 4sccm Cl_2 gas. The third LOCOS is formed at 1200°C for 60 minutes. The N diffusion window is opened and N diffusion is performed by the diffusion of SOD P507 in the RTP chamber at 1050°C (45% power) for 5 minutes. The fourth LOCOS is formed by the wet oxidation at 950 °C for 15 minutes. Then, the p-type diffusion windows are opened by the buffered HF. We executed several some variations in the p-type diffusion process. The p-type diffusion is realized by the out-diffusion of SOD B155 in the RTP chamber at 1050°C for various times of 30, 45, 60, 90, 180 seconds. After the removal of SOD B155 glass, the wafers are put into the RIE system to remove the SiB_x layer resulted from the SOD B155 diffusion. 90 seconds of Cl_2 RIE at 400V is used to remove this layer. Next, as shown in Fig. 5-23 (step D2), the gate window is opened for gate oxidation. The gate oxidation is dry oxidation, at a temperature of 900°C for 4 minutes. This oxidation condition results in a gate oxide of 5nm to 7nm. For some wafers (# 2, 4, 7), this gate oxide is also used as the passivation layer for p^+ region metal contact. That means that the sputtered SiO_2 passivation step used in the first planar version TFET is skipped. That is because this mask set is designed without the passivation process before metallization. Both the 170nm of evaporated Al and 100nm of sputtered Pt are tested as the gate metal. Al is patterned using the wet etching by Al etcher. Pt is patterned using the accelerated Ar^+ beam in the RIE system. The passivation layer of the sputtered SiO_2 is deposited on the wafers #1, #3, #5, and #6. After the contact window opening and the metallization, these wafers are ready for the electrical measurements.

For the process calibration, the experimental conditions vary from wafers #1 to #7. The variations of the experimental parameters are shown in table 5-3. It seems that the p^+ diffusion process is the most important. The measurement results show that the wafers with p^+ diffusion at 1050°C for 90 seconds achieve the best performance. The other wafers have no TFETs with good performance.

Table 5-3 Process parameters variations for wafer #1 - #7

	p^+ diffusion time at 1050°C	Gate oxidation time at 900°C	Sputtered SiO_2 passivation layer	G/D/S metal
#1	30 s	5 min	200 nm	Sputter Pt
#2	45 s	5 min	No passivation	Sputter Pt
#3	60 s	5 min	200 nm	Sputter Pt
#4	90 s	4 min	No passivation	Evaporate Al
#5	180 s	4 min	200 nm	Sputter Pt
#6	90 s	4 min	200 nm	Evaporate Al
#7	180 s	4 min	No passivation	Sputter Pt

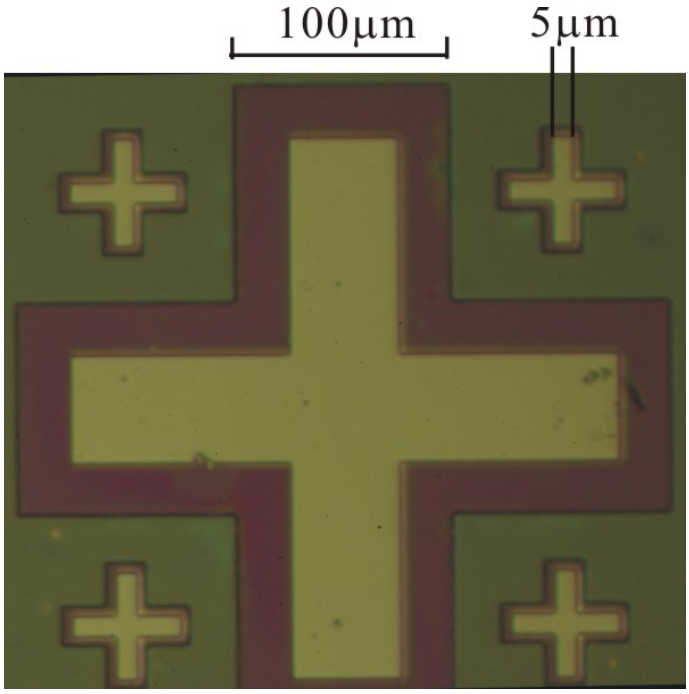


Fig. 5-24 5-crosses alignment for Karl Süss MJB-55 alignment machine
The misalignment is rather small.

The mask alignment machine used here is Karl Süss MJB-55. A 5-cross alignment is used for mask adjustment. As shown in Fig. 5-24 where the smaller metal crosses overlap the larger oxide crosses, the misalignment is rather small. The fabrication of TFET is also compatible with fabrication of standard CMOS technology. In Fig. 5-25, the CMOS inverters after the n^+ diffusion window-opening process are shown. NMOS sits in the p-well which is formed by SOD B150 diffusion. PMOS is on the n^- substrate. For the lightly n doped silicon substrate, the PMOS in these wafers has high leakage because the barrier for holes is not high enough.

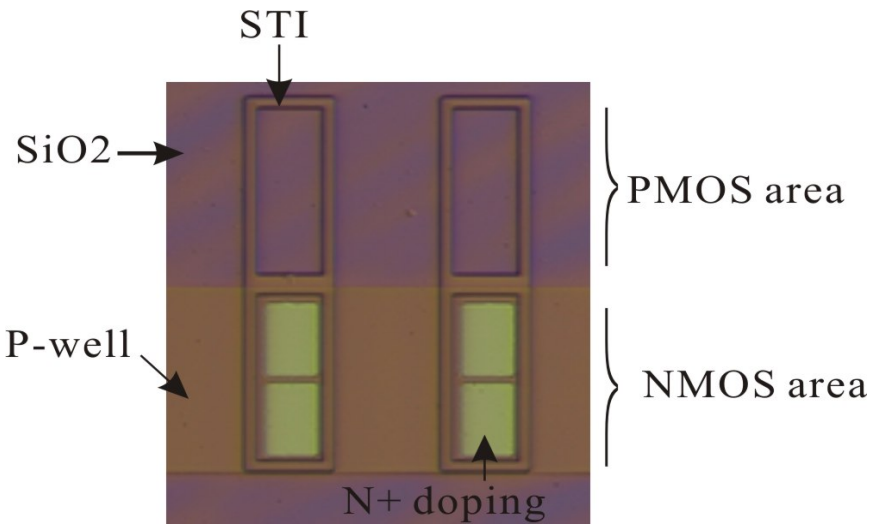


Fig. 5-25 Structure of the inverters composed by NTFET and PMOS (not finished structure)

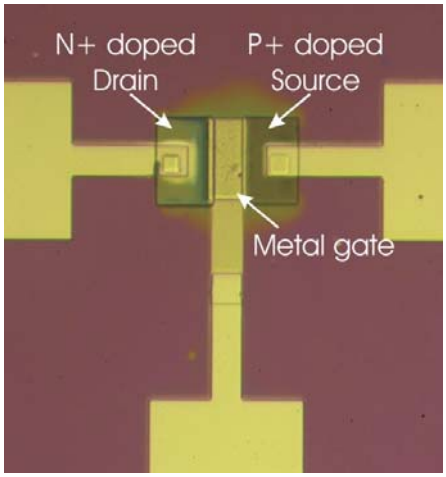


Fig. 5-26 Final structure of a NTFET without STI

In Fig. 5-26 a final structure of NTFET without STI is shown. The n^+ and p^+ doped regions stand side by side. The gate/source/drain material is Al. Although many working transistors are fabricated, the fabrication is faced with some technological problems. One problem is that the oxide alignments can be etched away easily by the buffered HF (BHF). Therefore, the etching rate and the etching time of the thermal oxide in BHF must be precisely controlled. The second problem occurs during the SOD B155 diffusion in the RTP chamber. Some small bubbles appear after the SOD B155 diffusion at a pressure of 14 mBar. The reason is that the solvent may not be completely evaporated by baking before diffusion. This problem can be solved by increasing the baking time and baking temperature before diffusion. Increasing the pressure in the RTP chamber is also a possible solution. The third problem arises from the sputtered oxide for passivation. This sputtered oxide cannot stick on the wafer very well. If the wafer surface is slightly rough, the under-etching in BHF may lift-off this sputtered oxide. The sputtering process also involves the danger of a gate MOS diode breakdown. The influences of these problems on the fabrication will be discussed in detail after the electrical measurements.

5.4.4 Electrical characterization

The 8-mask TFETs are measured without the substrate contact. Three terminals are used to measure the G/D/S current and voltage. Electrical measurements show that the wafer #4 is the best wafer. On this wafer both NTFET and PTFET are fabricated. On the wafer #6 there are some working TFETs but the yield is lower than the wafer #4. The wafer #5 failed because of the poor quality of the sputtered oxide. The sputtered oxide of wafer #5 is lifted-off during the contact window opening process using the BHF etching.

5.4.4.1 NTFET characteristics

Defining the n^+ doped region as drain and p^+ doped region as source, the measured transfer characteristics of transistor T16 of wafer #4 is shown in Fig. 5-27. (T is the row name, 16 is the column name). This transistor works like a NMOS, so we call it NTFET. More than 5 decades of current gain can be achieved in this NTFET. Fig. 5-28 is the simulated transfer characteristics of NTFET with 5nm gate oxide and diffusion smear-out. The character length of the dopant smear-out X.char for n diffusion is 8nm and for the p diffusion smear-out is 4nm in the simulation. The experimental transfer characteristics is similar to the simulation. From Fig. 5-27 the DITL value is calculated. The DITL at $I_d=10^{-9}$ A is -78.8mV(from V_{ds} =0.1V to V_{ds} =1V). As shown in Fig. 5-27, the thin gate oxide is stable in the planar TFET because the gate oxidation is done after all the diffusion processes. The problem of boron inter-diffusion into the thin oxide is solved in this planar TFET version. The higher drive current in simulation is resulted from a thinner gate oxide, a sharper doping profile and no contact resistance in simulation. The lower leakage current is for the thinner simulated silicon substrate.

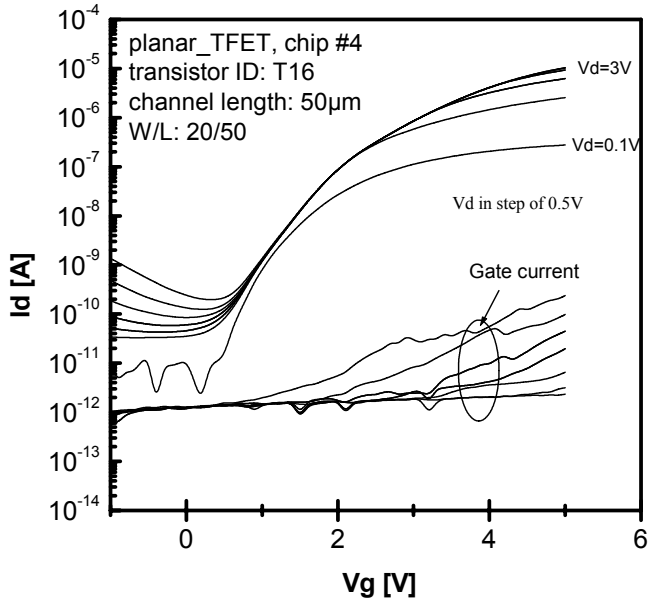


Fig. 5-27 Measured transfer characteristics of the planar SOD-NTFET

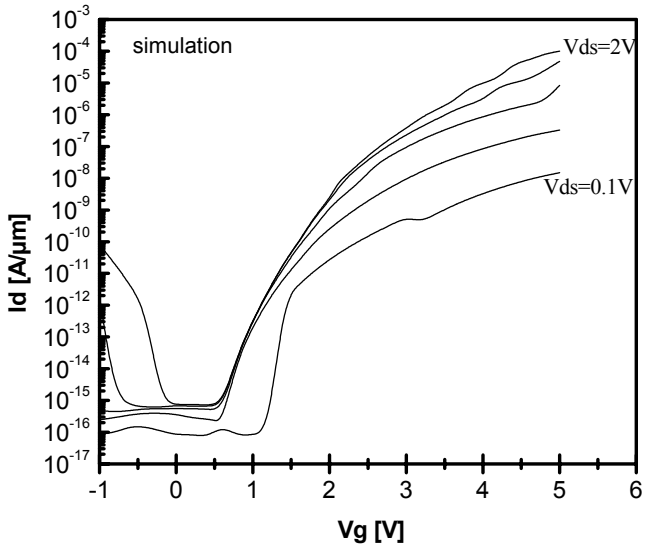


Fig. 5-28 Simulated transfer characteristics of the planar NTFET with 5nm gate oxide

Experimental output characteristics of the transistor T16 are shown in Fig. 5-29. The n^+ region is defined as drain and positive biased, which means the pin diode is forward biased when $V_{ds} < 0V$. In the experimental output characteristics shown in Fig. 5-29, the enhancement of the Esaki tunneling current at V_{ds} between –1V to 0V can be seen. When $V_{ds} > 0V$, the enhancement of the band-to-band tunneling current is controlled by the gate voltage. The off-current at V_{ds} =1V is 1.72×10^{-12} A/μm. The extremely low leakage current enables the planar TFET to be an ultra-low power consumption transistor. In the simulated output characteristics, the off-current of 10^{-15} A/μm at V_{ds} =1V can be achieved for the reverse biased pin diode structure. The off-current in simulation is lower because the silicon crystal quality and the gate oxide leakage current are neglected. A thinner simulated silicon substrate also reduces the leakage current. In the simulated results shown in Fig. 5-30, the forward characteristic is not right because the Esaki tunneling model is missing in the MEDICI simulator. The calculation of the Esaki tunneling current needs a full band computation simulator such as the Monte Carlo device simulator.

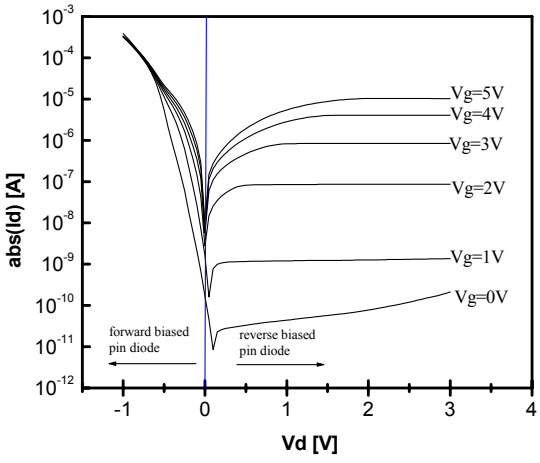


Fig. 5-29 Measured output characteristics of the transistor T16

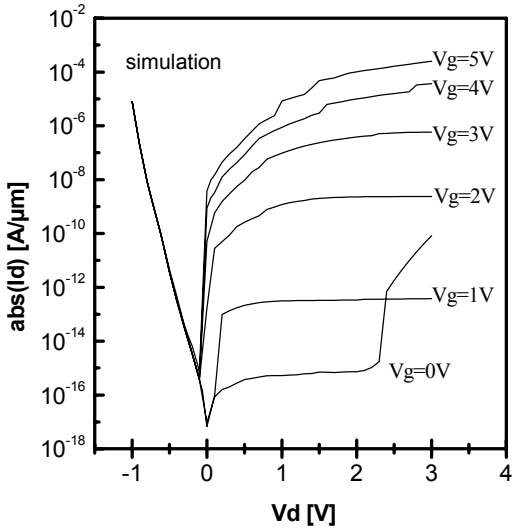


Fig. 5-30 Simulated output characteristics of the planar NTFET with 5nm gate oxide

5.4.4.2 PTFET characteristics

The PMOS-like TFET is also fabricated. This kind of TFET as PTFET. The transistor N3 is a P-TFET. The channel length of transistor N3 is 10µm and the channel width is 6µm. For PTFET, the n^+ source should be grounded and the p^+ drain should be negative biased. Fig. 5-31 shows transfer characteristics of PTFET 4-N3 using the measurement setup for PTFET. In the output characteristics (Fig. 5-32), the drain current increases when the gate voltage becomes more negative. The enhancement of Esaki tunneling current is also observed in the output characteristics of PTFET.

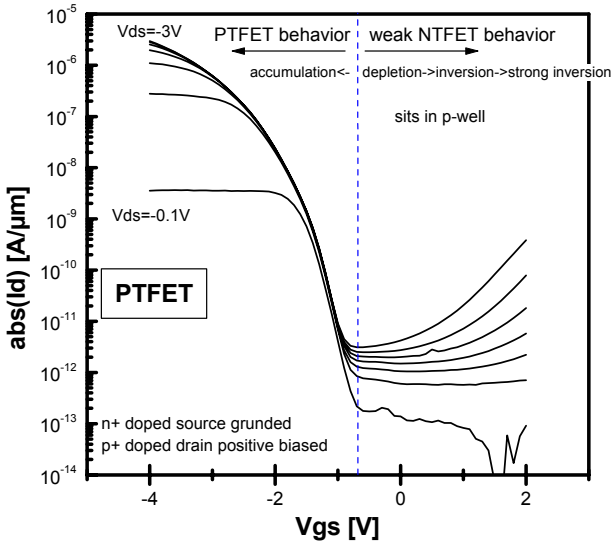


Fig. 5-31. Transfer characteristics of the PTFET with fixed V_s. ID: 4-N3

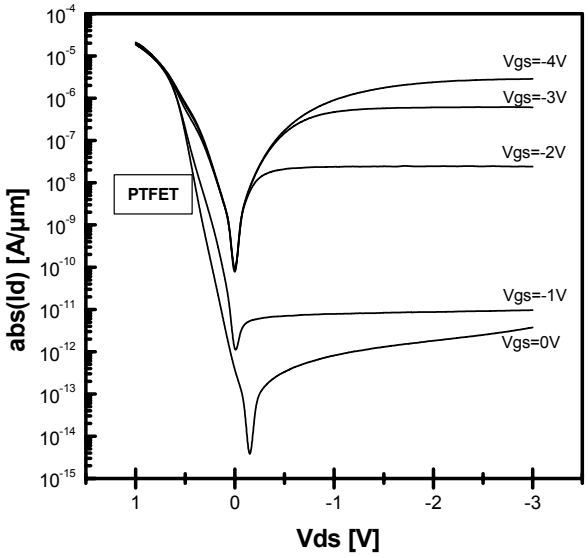


Fig. 5-32 Output characteristics of the PTFET, transistor ID: 4-N3

5.4.4.3 Discussions on the planar SOD-TFET fabrication

5.4.4.3.1 Over-etching problem in the TFET fabrication

In the fabrication process, the p^+ doped region needs to be cleaned in the RIE system to etch away the SiB_x layer. The rough SiB_x layer may result in a heterogeneous doping level on the silicon surface.

Fig. 5-33 shows the transfer characteristics of two TFETs with the same structure. Comparing these two groups of transfer characteristics, we obtain three results: 1). In the forward direction, TFET 4-R8 has a much smaller threshold voltage and a larger current gain than TFET 4-R4. 2). In the backward direction, the drain current increases immediately, when the negative V_{gs} is biased. 3). The same level leakage current of both TFETs is observed. Because the depth of p^+ doped region is smaller than that of n^+ doped region (resulted from the process parameter), the etching of the heavily doped silicon surface will affect the p^+ region more than the n^+ region. It seems that TFET 4-R4 is over-etched so that the p^+ doping level is not as high as that of TFET 4-R8. The over-etching results in a higher threshold voltage and a smaller drive current.

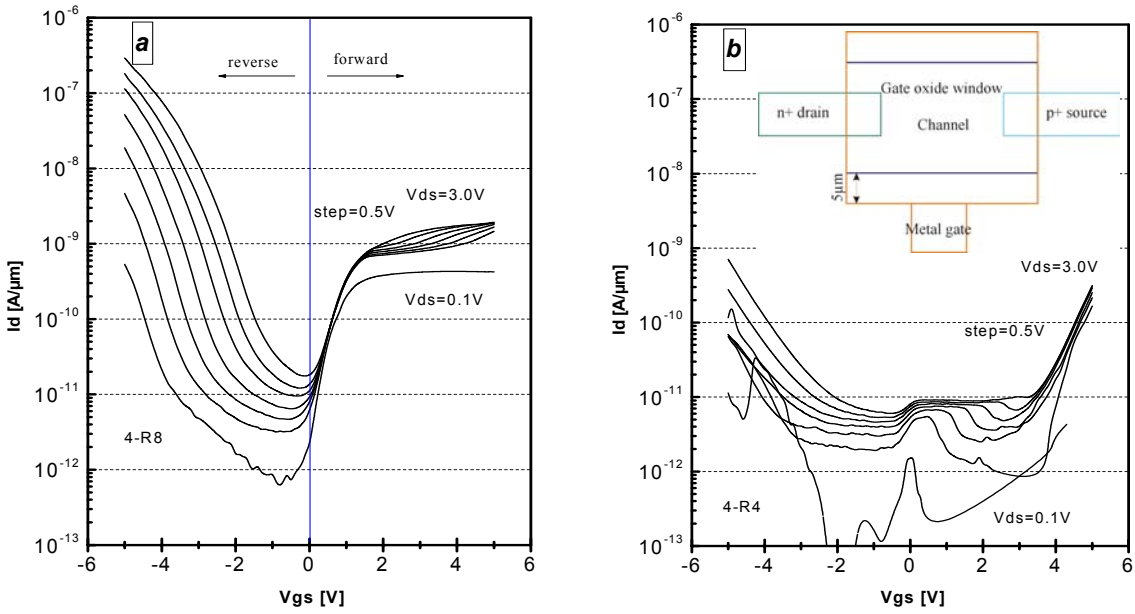


Fig. 5-33 Transfer characteristics of 4-R8 and 4-R4 with the same structures (W/L=6/20, L=20µm, the doping region is narrower than the gate window)

5.4.4.3.2 Influence of the structural design on the TFET performance

Many structural variations are designed to investigate the influence of structural design on the TFET performance. The characteristics of two types of structures are compared. Structural design *a*: 2µm security design, the gate window is narrower than the diffusion windows. Structural design *b:* 5µm security design, the gate window is narrower than the diffusion windows. More details on the security width can be found in appendix B.

5.4.4.3.3 Planar TFETs with various channel lengths

The performance of TFETs with 1µm, 2µm, 4µm, 6µm, 10µm, 20µm, and 50µm channel lengths is investigated. Fig. 5-34 shows the transfer characteristics of TFET with 1µm channel length. The gate has a weak control on the drain current. The leakage current of this TFET is much higher than the TFETs with a longer channel length. It seems that the p^+ doped region already touched the n^+ doped region because of the under-etching of the mask oxide (diffusion barrier). The characteristics of the TFETs with the longer channel length are better. From Fig. 5-35 to Fig. 5-40, the transfer characteristics of the TFETs with the channel length of 2µm, 4µm, 6µm, 10µm, 20µm, and 50µm are shown. Two points are summarized from these figures: 1) Due to the non-self aligned process, the fabrication of TFETs with the channel length shorter than 4µm is not stable. The self-aligned process must be developed. 2) The overlap of p^+ and n^+ doping regions results in the higher leakage current. Therefore, the lightly doped or intrinsic silicon region is needed to separate the n^+ and p^+ doping regions and to suppress the leakage current.

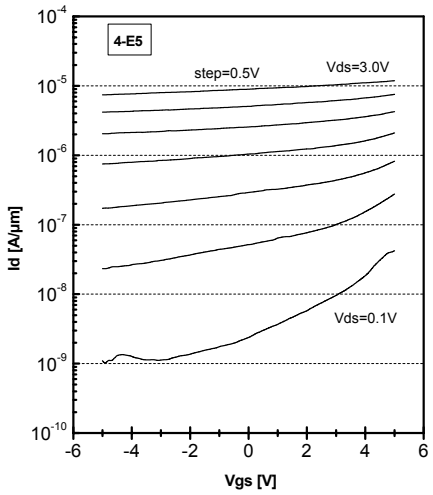


Fig. 5-34 Transfer characteristics of the TFETs with 1μm channel length

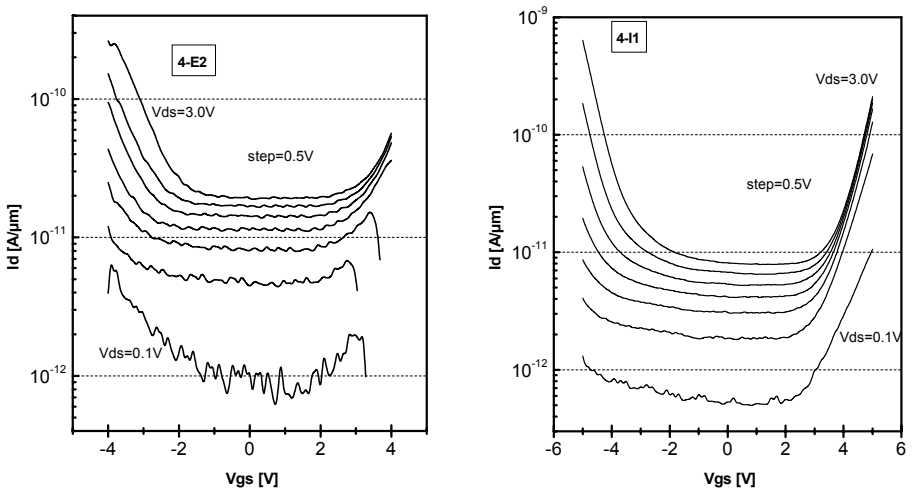


Fig. 5-35 Transfer characteristics of the TFETs with 2μm channel length

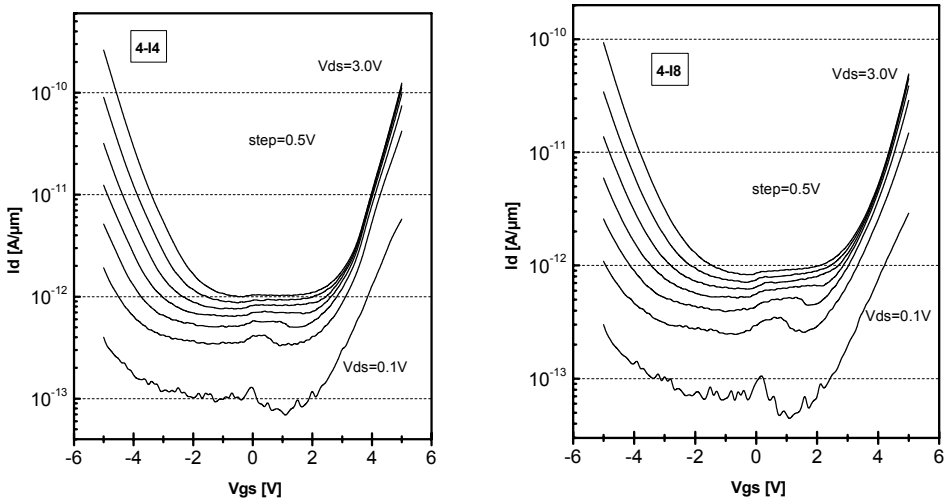


Fig. 5-36 Transfer characteristics of the TFETs with 4μm channel length

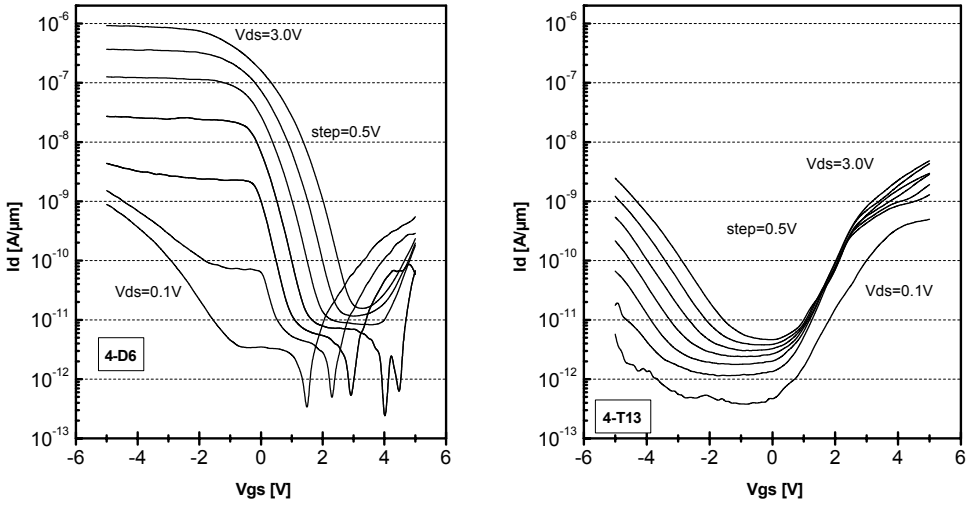


Fig. 5-37 Transfer characteristics of the TFETs with 6μm channel length

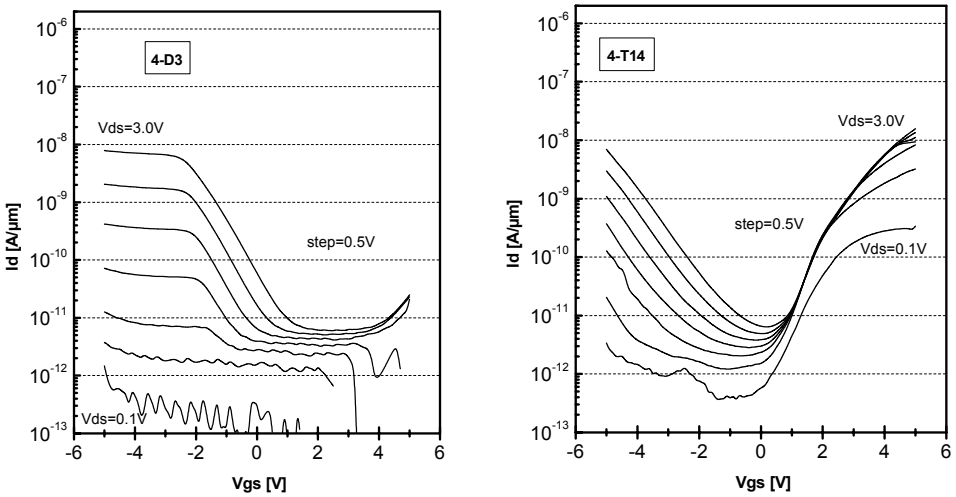


Fig. 5-38 Transfer characteristics of the TFETs with 10μm channel length

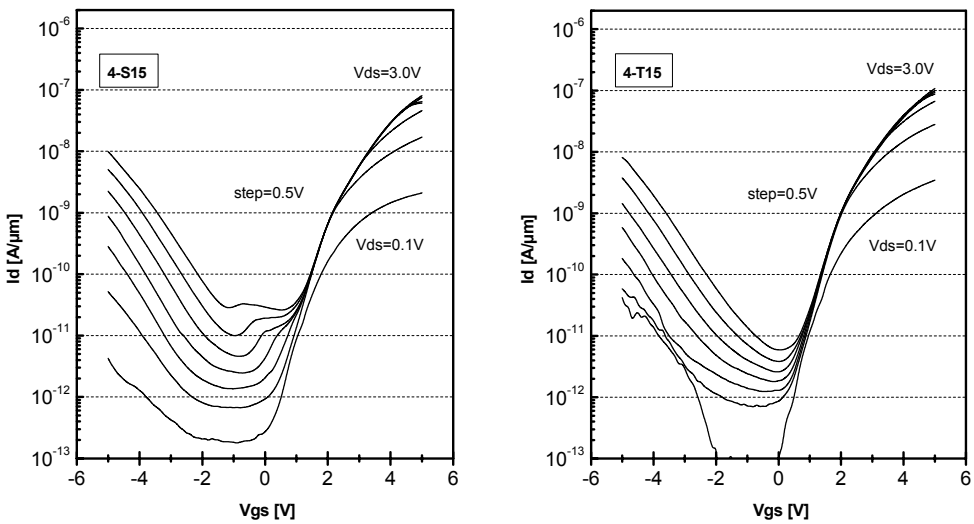


Fig. 5-39 Transfer characteristics of the TFETs with 20μm channel length

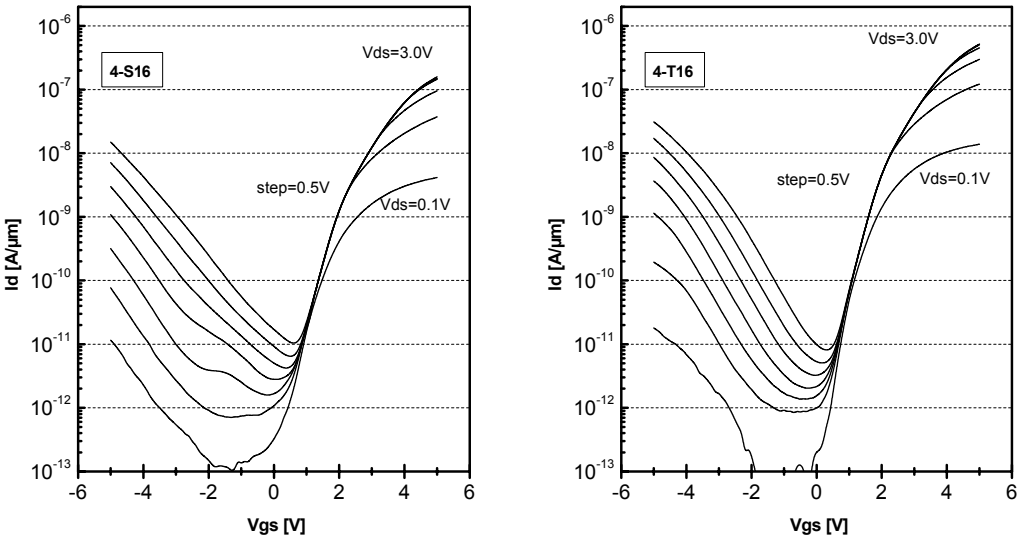
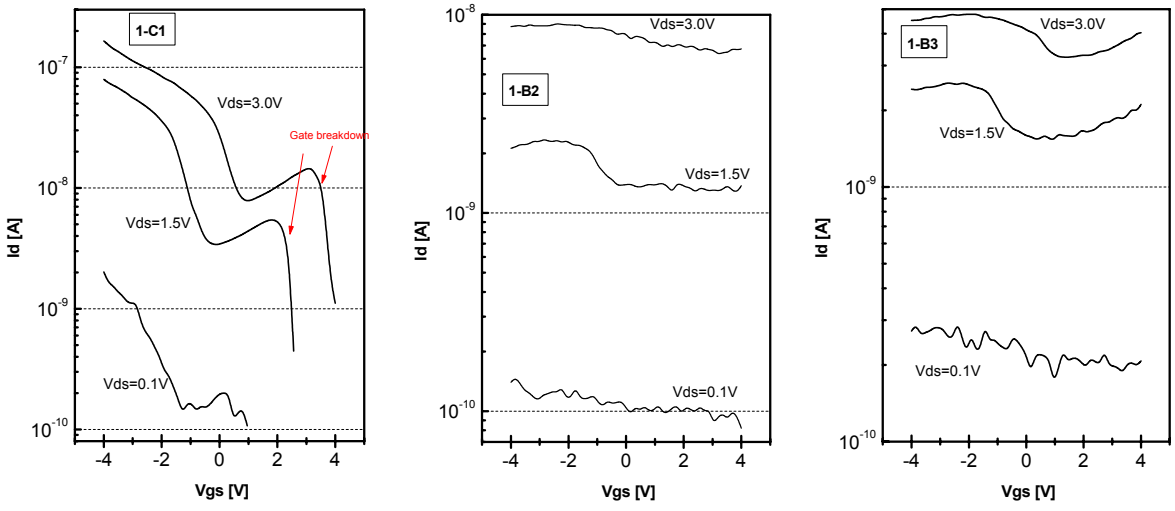


Fig. 5-40 Transfer characteristics of the TFETs with 50µm channel length

5.4.4.3.4 Effects of p^+ diffusion time on TFET

The p^+ diffusion time is essential for the TFET characteristics. Wafer #1 is fabricated with 30 seconds p^+ diffusion. For the 30 seconds p^+ diffusion, the tunneling current at positive V_{gs} is rather low (Fig. 5-41.a, b and c). Compared to Fig. 5-40 where TFET is fabricated using 90 seconds of p^+ diffusion, the drive current density and the current gain are much smaller using 30 seconds p^+ diffusion. That means that the p^+ diffusion time is not sufficiently long. Mean while, the TFET production yield of the wafer #1 is also rather poor comparing to the wafer #4.



a b c

Fig. 5-41 Gate breakdown is observed in the transfer characteristics of TFET 1-C1 (a); Transfer characteristics of TFET 1-B2 (b); Transfer characteristics of TFET 1-B3 (c)

The fabrication conditions of the wafer #6 are nearly the same of wafer #4 except for the fact that a sputtered SiO_2 layer is used to passivate the transistor. The transfer characteristics of several working TFETs are shown in Fig. 5-42. Wafer #6 also uses 90 seconds of p^+ diffusion time. Summarized from the measurement results, the p^+ diffusion process at 1050° for 90 seconds is a feasible parameter for planar SOD-TFET fabrication.

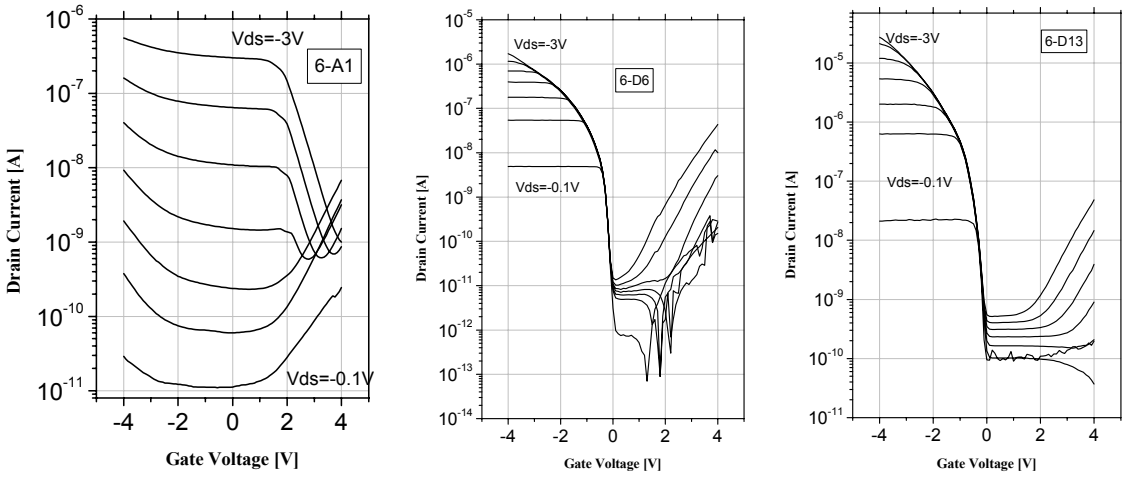


Fig. 5-42 Transfer characteristics of several working TFETs in wafer #6

5.4.4.3.5 Effects of the sputtering processes on TFET

Two sputtering processes are tested in the experiments. Pt is used as the gate metal for the wafers #1, #2, #3, #5, #7 because of it stable chemical properties against BHF. Pt is deposited by 50 W sputtering. The wafers #3 and #5 have a sputtered SiO_2 passivation layer. The SiO_2 layer is sputtered with 200W power. It is found that the sputter process degrades the gate oxide. The gate oxide in the wafers without sputtering process has a higher breakdown voltage and a lower leakage current (See Fig. 5-41.a). Comparing Fig. 5-42 with Fig. 5-40, the source-drain leakage current of TFET with sputtered SiO_2 on wafer #6 is higher than the TFETs without sputtered SiO_2 layer in wafer #4. The sputtering process also decreases the production yield of wafer #6.

The poor adhesion of the sputtered material also causes serious problems. It can be seen from table 5-3 that wafers #2 and #7 have a sputtered Pt gate but no sputtered SiO_2 passivation. Because the adhesion of Pt on SiO_2 is not good enough, some Pt gates are lifted away (Fig. 5-43). This results in a low yield. For the wafers with the evaporated Al gate, the adhesion is good and no Al gate is lift away.

Because a number of small bubbles are created after the diffusion of SOD B155 film, the quality of sputtered SiO_2 on such a rough surface is not reliable. During the SiO_2 wet etching using BHF, the sputtered SiO_2 is lifted off and results in a damaged surface. That causes a lot of problems in the subsequent processes such as the contact window opening process and the metallization process. The S/D/G contact is very poor for this reason.

Therefore, the sputtering processes are strongly recommended to be replaced by the CVD techniques in the planar TFET fabrication.

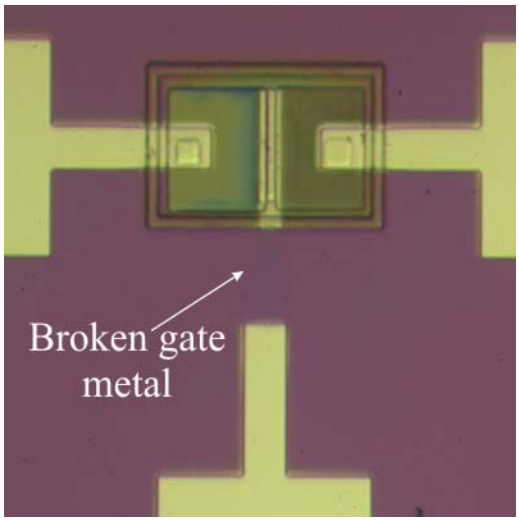


Fig. 5-43 Pt gate metal is lifted away during the process because of the poor adhesion on SiO_2

5.4.4.3.6 Problems caused by STI

STI is designed to separate devices and to suppress the leakage current. In the industrial process, the chemical mechanical polishing (CMP) is applied to planarize the trench resulted by STI. In our TFET fabrication there is no CMP planarization process. Therefore, the trench break some of the metal lines (shown in Fig. 5-44). Hence, the STI process must be improved here.

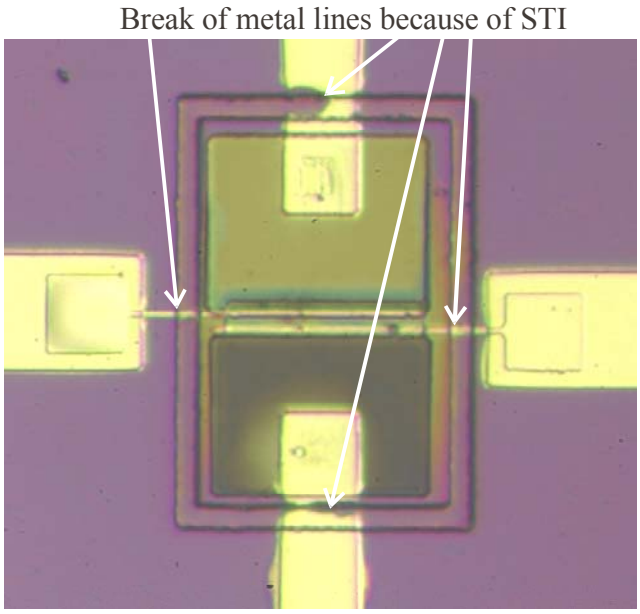


Fig. 5-44 A defect TFET because STI causes break of metal lines

5.4.4.4 Yield of TFET on one wafer

The measurement shows that wafer #4 has the best performance. The process parameters of wafer #4 are shown in table 5-3. The yield of TFET on this wafer is investigated. Table 5-4

shows the measurement results map for wafer #4. The dimension is featured as W/L in µm. The TFETs from A1 to C4 are damaged by the high V_{gs} setup in the measurement. In the STI block no working transistor is found because of the break of metal lines through the 1µm deep trench (Fig. 5-44).

Table 5-4 Measurement results map for wafer #4. (columns 5-8 repeat 1-4)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	Measurement setup error. Gate oxide is broken down when –7V < V_{gs} <7V															
B																
C					10/6	10/10	10/20	10/50	STI causes break of G/D/S metal line							
D	6/2	6/6	6/10	6/20	6/2	6/6	6/10	6/20								
E	2/1	2/2	2/6	2/10	2/1	2/2	2/6	2/10								
F	1/1	1/2	2/6	2/10	1/1	1 /2	2/6	2/10								
G	10/6	10/10	10/20	10/50	10/6	10/10	10/20	10/50								
H	6/2	6/6	6/10	6/20	6/2	6/6	6/10	6/20	STIs cause break of G/D/S metal line				Split gate structures for test			
I	10/2	20/2	50/2	50/4	10/2	20/2	50/2	50/4								
J	10/6	10/10	10/20	10/50	10/6	10/10	10/20	10/50								
K	50/6	50/10	50/20	50/50	50/6	50/10	50/20	50/50								
L	20/6	20/10	20/20	20/50	20/6	20/10	20/20	20/50								
M	10/6	10/10	10/20	10/50	10/6	10/10	10/20	10/50								
N	6/2	6/6	6/10	6/20	6/2	6/6	6/10	6/20								
O	50/6	50/10	50/20	50/50	50/6	50/10	50/20	50/50								
P	20/6	20/10	20/20	20/50	20/6	20/10	20/20	20/50								
Q	10/6	10/10	10/20	10/50	10/6	10/10	10/20	10/50								
R	6/2	6/6	6/10	6/20	6/2	6/6	6/10	6/20								
S	(10-30)/6	(10-50)/10	(30-50)/5	(10-50)/4	(10-30)/6	(10-50)/10	(30-50)/5	(10-50)/4	50/6	50/10	50/20	50/50	50/6	50/10	50/20	50/50
T	(30-10)/6	(50-10)/10	(50-30)/5	(50-10)/4	(30-10)/6	(50-10)/10	(50-30)/5	(50-10)/4	20/6	20/10	20/20	20/50	20/6	20/10	20/20	20/50

(Wafer #4. Dimension: W/L in µm, no sputtered passivation layer)

#4 defect 1-2 dec 3 dec 4-7 dec

Table 5-5 Summarization of Table 5-4

Total TFETs	Working TFETs	Defect TFETs	1-2dec TFETs	3dec TFETs	4-7dec TFETs
156	85	71	59	18	8

2µm security TFETs yield	5µm security TFETs yield	1µm W TFETs	Best L region		
16 of 28	14 of 32	All defect	6µm to 50µm		

From the measurement map displayed in Table 5-4, the analysis results (shown in table 5-5) are:

1). In total 156 TFETs are measured. 85 TFETs are working. The yield is 85/156=54.5%.
2). The minimum working TFET dimension is W/L=2/1 with L=1µm.

3). No working TFET with W=1μm is found.
4). The TFETs with a current gain larger than 3 orders of magnitude are with L from 6 to 50μm.
5). 2μm security width is enough for the planar TFET design.

5.5 Discussion on the TFET properties

Based on the electrical measurements, the properties and applications of TFET will be discussed in this section.

5.5.1 Moving tunneling junction in TFET

TFET has a different tunneling junction location inside of TFET when positive or negative V_{gs} is applied. For the PTFET behavior, the tunneling junction is at the n^+ region-channel junction. V_{gs} - V_{n+} > $V_{t'}$ is necessary to switch on the tunneling junction. Where V_{n+} is the potential of n^+ region and $V_{t'}$ is the switch-on voltage of the surface tunneling junction. The variation of potential in the n^+ region will affect the switch-on point of the tunneling current. This effect can be seen in Fig. 5-45 where the measurement is carried out using differing n^+ region potential and the fixed p^+ region potential. When V_{gs} <0V, the drain current curves moves in the same direction and almost with the same step length as V_{ds}. The shift of drain current curves is much smaller when V_{gs} >0. The reason is that the tunneling junction now moves to p^+ region-channel junction and the variation of V_{ds} cannot affect the switch-on voltage of the tunneling junction so much. However, a similar effect to the DIBL effect in MOSFET is observed here. In fact, in TFET this effect is due to the different mechanisms. When V_{ds} increases, the slope of energy bands in the tunneling junction of the on-state TFET (Fig. 3-16) will be steeper so that the tunneling barrier is lowered. Therefore, it is should be named as the Drain Induced Tunneling-barrier Lowering (DITL) effect. The measured transfer characteristics of NTFET measured by varying the p^+ source voltage and ground the n^+ drain potential are shown in Fig. 5-46. The shift of current curves with the differing V_s proves that the tunneling junction is at the p^+ source-channel junction in NTFET.

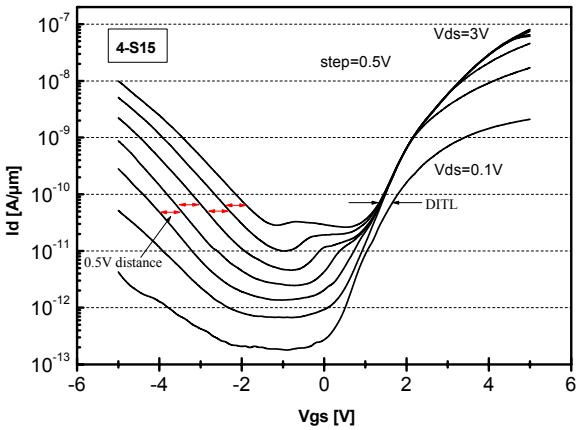


Fig. 5-45 Transfer characteristics of TFET measured using the n^+ region as drain and the p^+ region as source. (source is grounded)

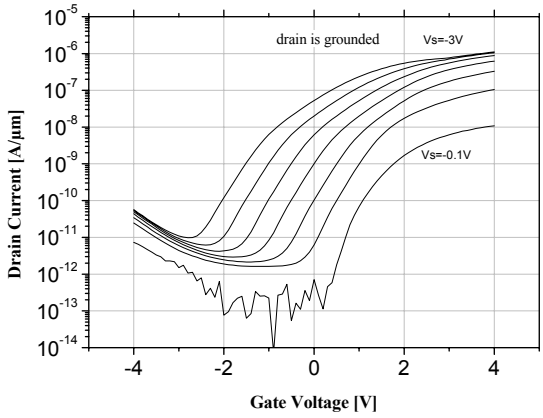


Fig. 5-46 Transfer characteristics of a NTFET measured with a grounded n^+ drain and different source voltages. The shift of current curves with V_s variation is observed

A series of PTFET transfer characteristics is measured with various V_s (Fig. 5-47), the threshold voltage shifts with V_s. This result also proves that the tunneling junction is at the n^+ region-channel junction in PTFET.

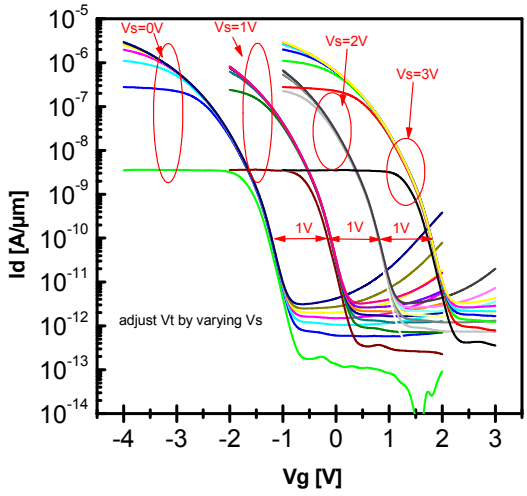


Fig. 5-47 Transfer characteristics of the PTFET with various V_s

5.5.2 Current saturation in TFET

As shown in the output characteristics of NTFET and PTFET (Fig. 5-29, Fig. 5-32), drain current saturation is observed. The fitting simulation result also shows this drain saturation phenomenon. The physical mechanism of the drain current saturation in TFET is of interest for investigation.

Fig. 5-48 shows the linear plot of one experimental NTFET output characteristics. The saturation current at V_{gs} =3V is about 0.75 μA (channel width is 6μm). In the measured PMOS output characteristics, a slightly saturation behavior of the drain current is also observed (Fig. 5-49). Although this PMOS is fabricated on the TFET wafer, the drive current

of this PMOS is 70μA/μm which is more than 2 decades higher than that of NTFET. That means that the saturation current is not limited by the MOS channel, but by the tunneling junction in TFET.

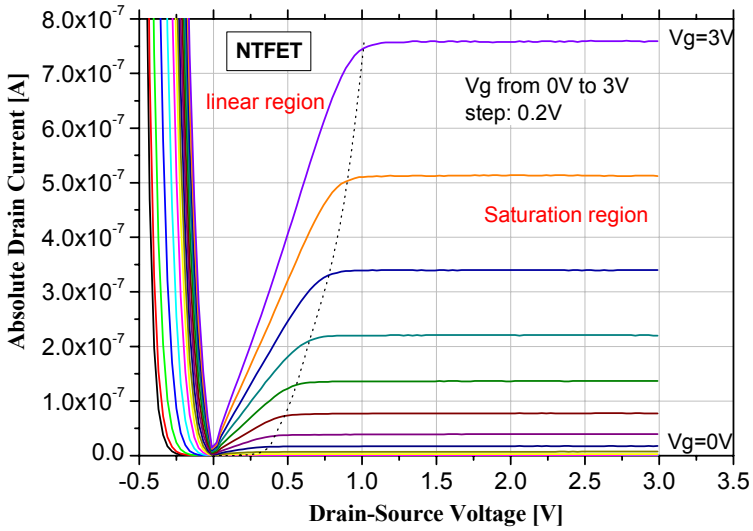


Fig. 5-48 Linear plot of one measured NTFET output characteristics

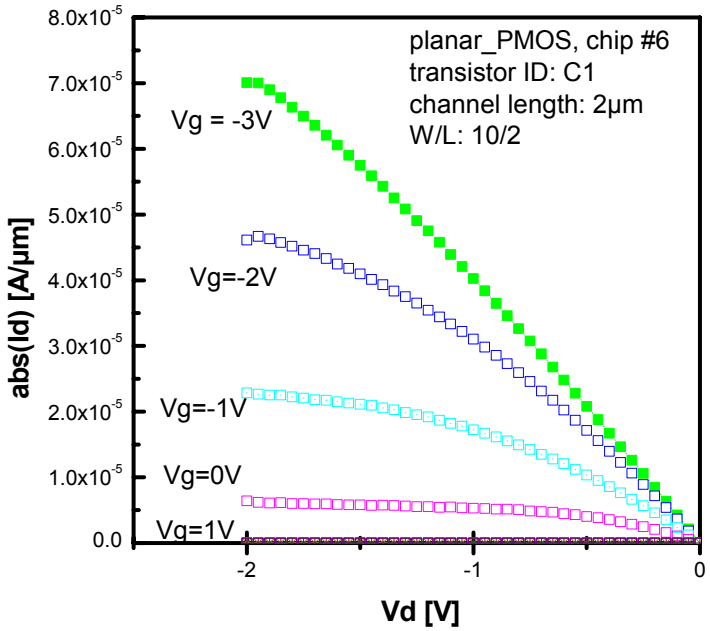


Fig. 5-49 Linear plot of the measured on-wafer PMOS output characteristics

A series of band diagrams of the simulated device with the characteristics shown in Fig. 5-30 is plotted in Fig. 5-50. With the drain voltage increasing, the potential drop in the channel also increases. Comparing the band diagrams of V_{ds} =2V and V_{ds} =3V, the band structure at the tunneling remains almost the same, but the band slope in channel increases. At the same time, the electron quasi-Fermi level moves against the conduction band. This behavior is similar to

the pinch-off effect in MOSFET where the pinch-off starts when V_{gs} - V_t = V_{ds}. The channel pinch-off is observed in the simulated NTFET. Fig. 5-51 shows the electron density in a NTFET with V_{ds} =3V and V_{gs} =2V. The channel at the drain-channel junction is pinched off. When the pinch-off starts, the increase of the drain potential cannot change the voltage-drop at the tunneling junction which is at the channel-source junction and the drain current is saturated.

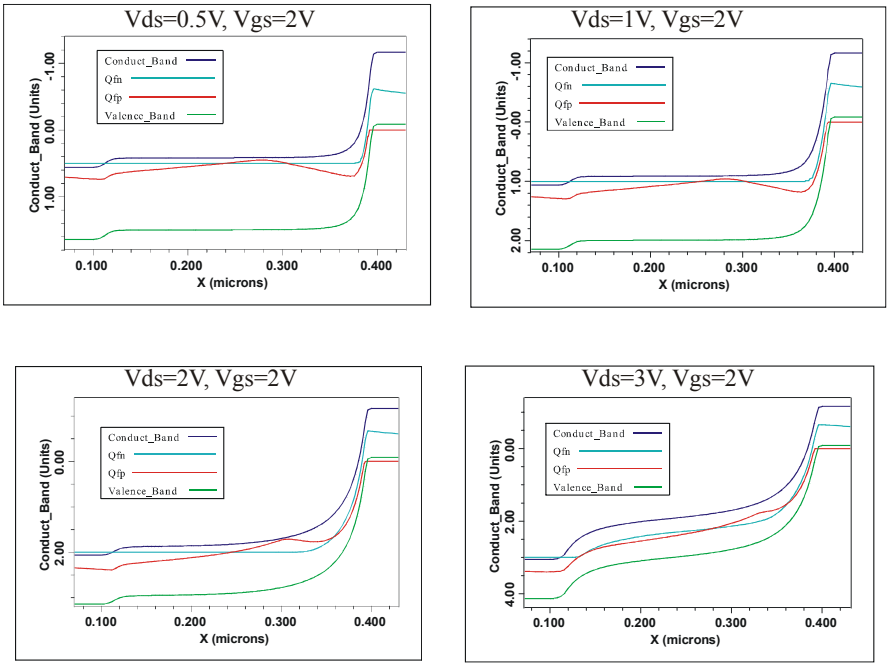


Fig. 5-50 Band diagrams of NTFET along the cutline 5nm beneath the gate oxide

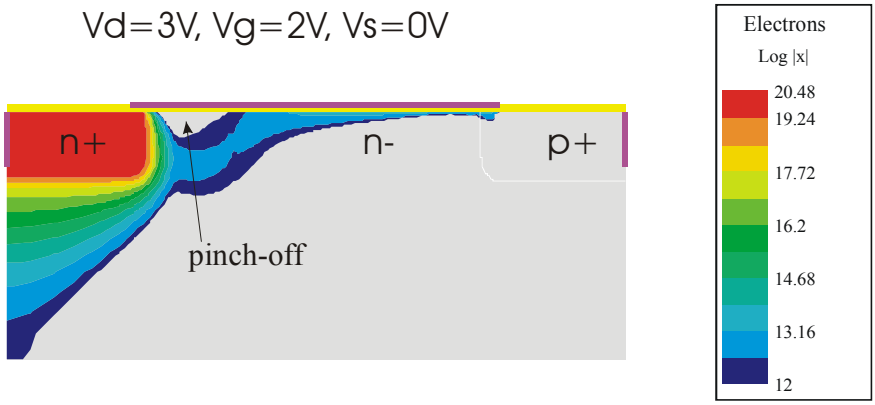


Fig. 5-51 Pinch-off of the channel in a TFET

Comparing the conductivity of MOS channel and tunneling junction, it is obvious that the tunneling junction has a higher resistance and is the bottleneck of the drain current. Therefore, although the saturation of the drain current in TFET is caused by the pinch-off of the MOS channel, the saturated current density is determined by the tunneling effect. For this reason, the channel length modulation in the pinch-off effect only has very low effects on the drain current of TFET. The saturation behavior of TFET is better than that of MOSFET. As shown

in Fig. 5-52, the band-to-band tunneling generation rate remains the same, when the drain current is saturated at V_{ds} =2V and V_{ds} =3V.

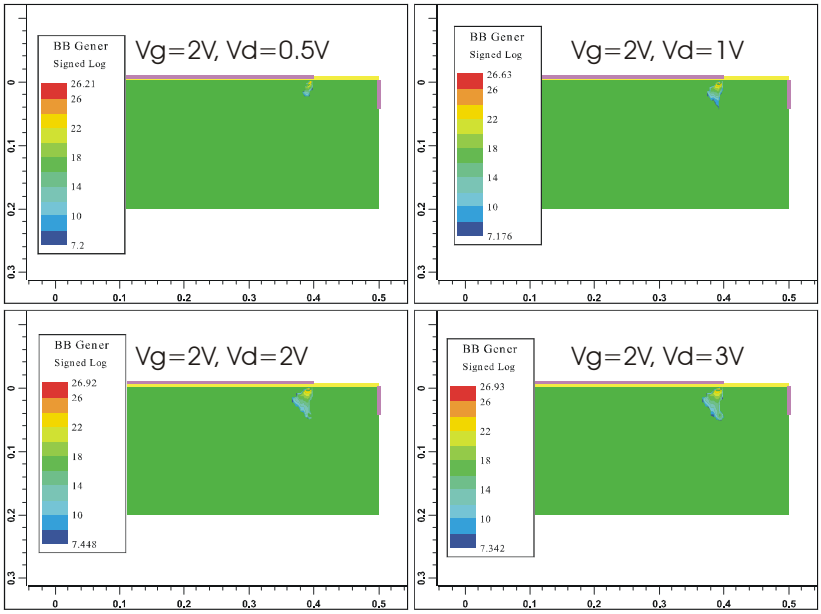


Fig. 5-52 Band-to-band tunneling generation rates in TFET, when V_{ds} is increased from 0.5V to 3V (V_{gs} remains 2V).

However, the former simulated NTFET output characteristics in chapter 3 has no drain current saturation. When the connection setup is using the grounded drain and the different negative biased source potentials, the channel pinch-off effect cannot occur. The reason is that the n^+ drain is grounded so that $V_{ds} < V_{gs} - V_{t(mos)}$. Here $V_{t(mos)}$ is the threshold voltage of the MOS channel, it is different from V_t of TFET.

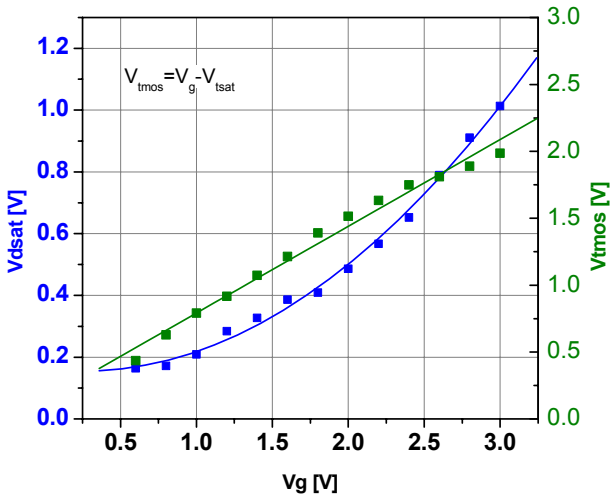


Fig. 5-53 Dependence of V_{dsat} and V_{tmos} on V_{gs} in NTFET

The dependence of the saturation drain voltage V_{dsat} and the assumed MOS threshold voltage V_{tmos} on the gate voltage at the saturation point is shown in Fig. 5-53. It seems that the

assumed MOS threshold voltage is not as constant as that of MOSFET. One reason is the existence of the tunneling junction in TFET which has the interaction with the MOS channel. Another reason is that the channel region is depleted so that the assumed MOS threshold voltage can be modulated by V_{dsat} because of the charge sharing effect.

5.5.3 Punch-through and avalanche in TFET

For MOSFET, the punch-through effect occurs, when the depletion zones around source and drain touch each other (Fig. 5-54). The field underneath the gate then becomes strongly dependent of the drain-source voltage. The increasing drain-source voltage will result in a rapidly increasing current in the punch-through effect. It limits the maximum operating voltage of MOSFET.

The TFET channel is fully depleted by drain voltage because of the low channel doping (e.g. n type $1\times10^{14}cm^{-3}$). Because of the reverse biased p-i-n structure, there is no punch-through effect in TFET. In the measured NTFET and PTFET output characteristics, the off-current remains several pA/μm when V_{ds} increases from 1V to 3V.

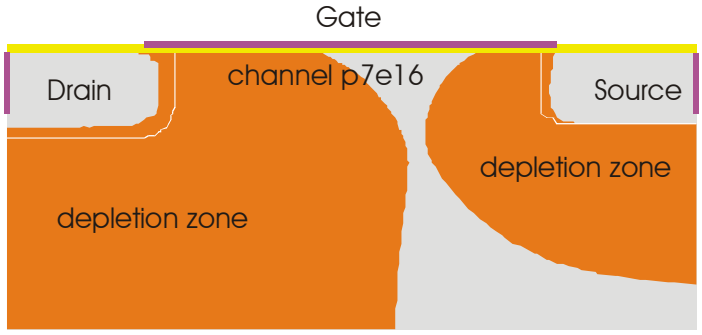


Fig. 5-54 A simulated NMOS before punch through. V_{ds} =3V, V_{gs} =-1V with Al gate

The avalanche in MOSFET depends on the electrical field in channel and the parasitic bipolar behavior. In NMOS, the potential is concentrated at the drain-channel junction (shown in Fig. 5-55 right). The increasing electrical field at the channel-drain junction will result in the hole and electron generation by the impact ionization. The parasitic bipolar behavior will amplify this current resulted from the impact ionization and the avalanche breakdown voltage of NMOS is lowered.

In NTFET shown in Fig. 5-55, the electrical field in channel is concentrated at the source-channel junction. The impact ionization is caused by the injection of tunneling electrons coming from p^+ source. The current density is low and there is no parasitic bipolar behavior to amplify the generated carriers. When the gate voltage is off, the electric field in the channel will be decreased a lot (see the off-state band diagram in Fig. 2-2). That means that not only the tunneling current, but also the impact ionization current is controlled by the gate voltage. Therefore, although the impact ionization contributes to the total drive current of TFET, the avalanche breakdown is more difficult to happen in TFET than in MOSFET.

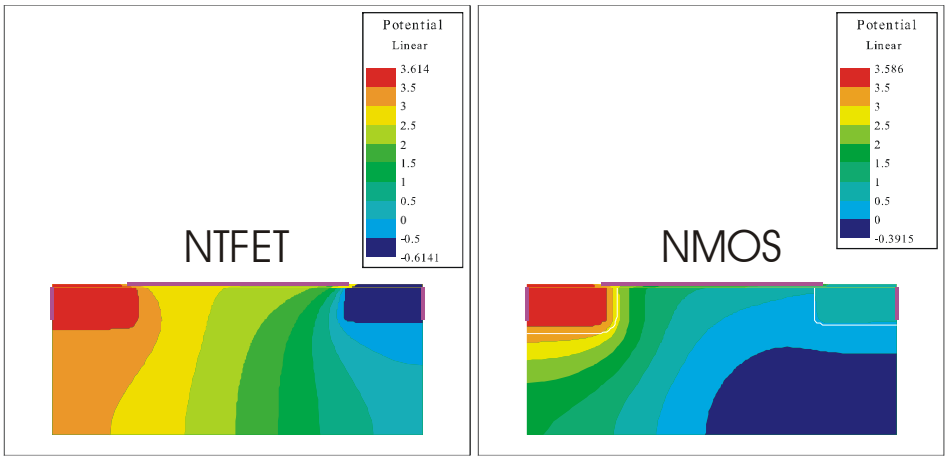


Fig. 5-55 Fermi-level potential of NTFET and NMOS with the same structure. V_{ds} =3V, V_{gs} =2V

5.5.4 Ballistic electron transport in TFET

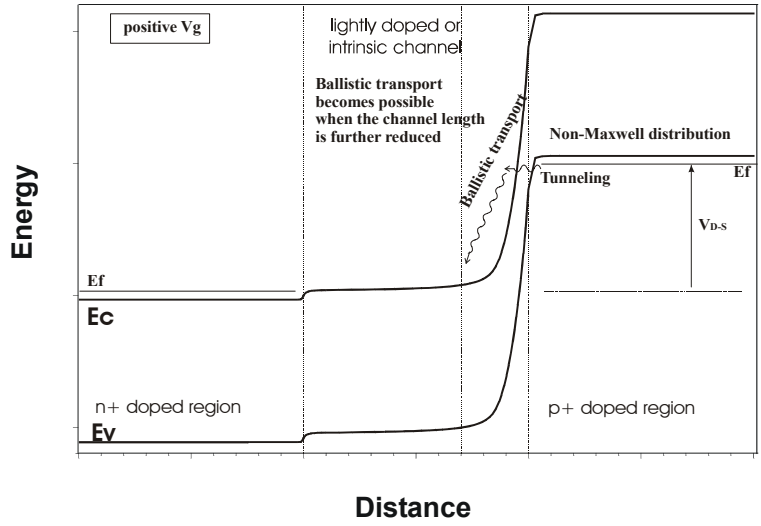


Fig. 5-56 Band diagram of on-state NTFET. The hot electron injection and the ballistic transport in channel is shown

TFET is also a hot electron device where the electrons are injected into the channel region through the tunneling barrier. Due to the short and intrinsic channel, the ballistic electron transport can be realized in TFET, when its channel length is further reduced. Fig. 5-56 shows the band diagram of the on-state NTFET. The distribution of electrons energy in the p^+ doped region is non-Maxwell. The average energy of the injected electrons depends on V_{ds}. The portion of the ballistic transport will increase with the increasing V_{ds}.

Similar to bipolar device, the operating speed of TFET is determined by the transit time through the channel region and the product of parasitic capacitance and source/drain resistance. In TFET, both source and drain are heavily doped, the device operating speed can be improved for the short electron transit time through the channel.

5.5.5 Gate-controlled Esaki-Tunneling current in TFET

When the p-i-n diode is forward biased, the increasing gate voltage will enhance the Esaki-tunneling current at the surface. In order to investigate this effect, the bulk diode current is subtracted from the forward biased p-i-n diode current with the positive gate voltage. The result of this treatment is shown in Fig. 5-57. It is obvious that the surface Esaki-tunneling current is controlled by the gate voltage. A similar behavior is also observed in the MBE TFETs fabricated at Uni-Bw München. These humps can not be observed in the MEDICI simulated *I-V* characteristics of TFET because the Esaki-tunneling model is not implanted in the simulator.

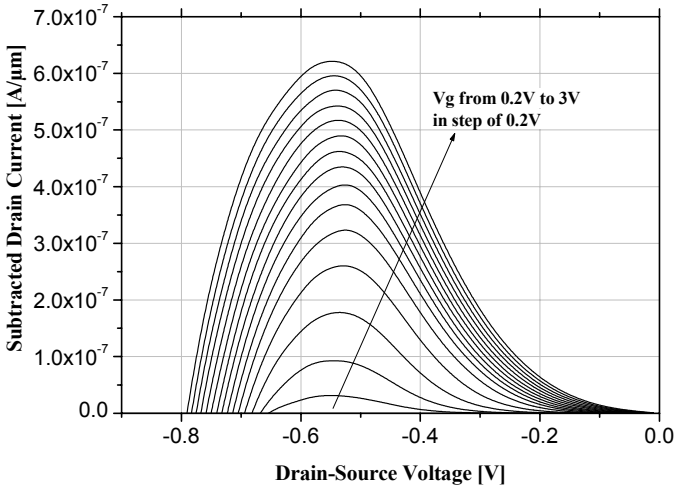


Fig. 5-57 The extracted surface tunneling in the forward biased pin diode (from an example transistor)

The peak-current shown in Fig. 5-57 is at about V_{sd}=0.52V which is higher than the normal Esaki tunnel diode in silicon. The shift of this peak-voltage is due to the existence of series resistance such as the channel resistance and the metal-silicon contact resistance. This can be proved by calculating the *I-V* characteristic of the Esaki tunnel diode in silicon.

Using equations 2-31 to 2-34, the *I-V* characteristics of the Esaki tunnel diode without series resistance can be calculated. The calculated tunneling current, excess current, thermal current, and total current are shown in Fig. 5-58. The peak voltage V_p of the hump is set as 0.06V and the peak current I_p is set as 6.4×10^{-7} A.

An additional potential-drop on the series resistance must be considered when calculating the *I-V* characteristic of an Esaki tunnel diode with series resistance. The calculated *I-V* curves of the Esaki tunnel diode with various series resistances are shown in Fig. 5-59. This calculation only provides a simple estimation that how the peak voltage depends on the series resistance in an Esaki tunnel diode. It can be seen in Fig. 5-59 that the peak voltage moves from 0.06V to 0.62V with the series resistance increasing from 0ohm to 800 kilo-ohm. Therefore, in the

experimental TFET, it is possible for the contact series resistance and the channel resistance to increase the peak voltage to 0.52V.

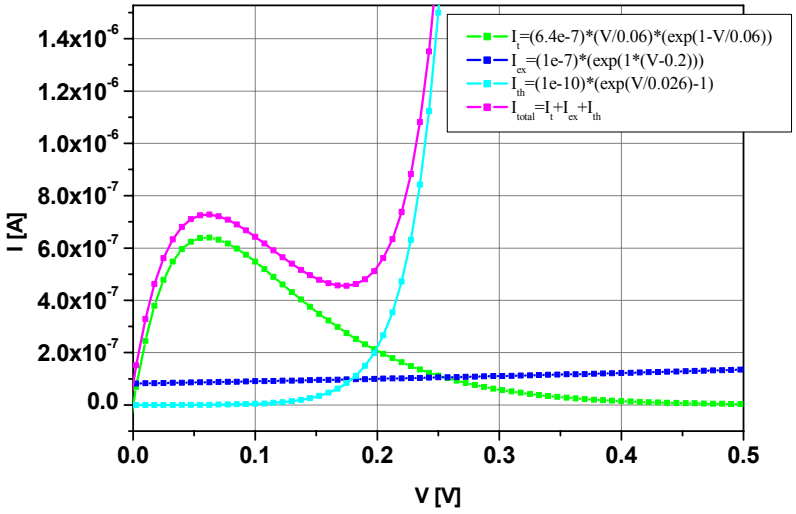


Fig. 5-58 Calculated tunneling current, excess current, thermal current, and total current in an Esaki tunnel diode

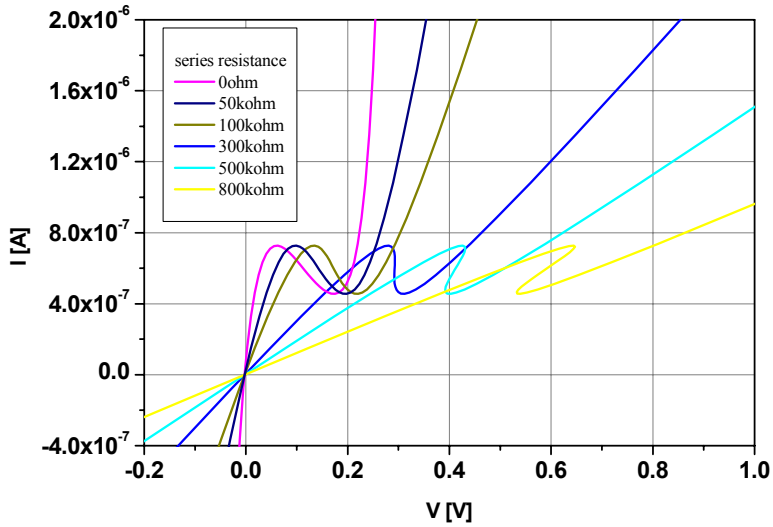


Fig. 5-59 Dependence of the peak voltage of an Esaki tunnel diode on the series resistance

5.5.6 Flat region in the TFET transfer characteristics

As shown in Fig. 5-60, there is a flat region in transfer characteristics of TFET. This flat may be useful for data storage because there are two gate voltage values corresponding to one drain current. If the threshold voltage can be well adjusted, TFET can configure the edge detector using only one TFET. In Fig. 5-61, TFET is connected to a passive or active load in the inverter connection. The input signal is a series of pulses. Because with both low and high

gate voltages except for the flat region TFET is switched on, this circuit creates impulses at both rising and falling edges. The frequency of output signal is double the input signal.

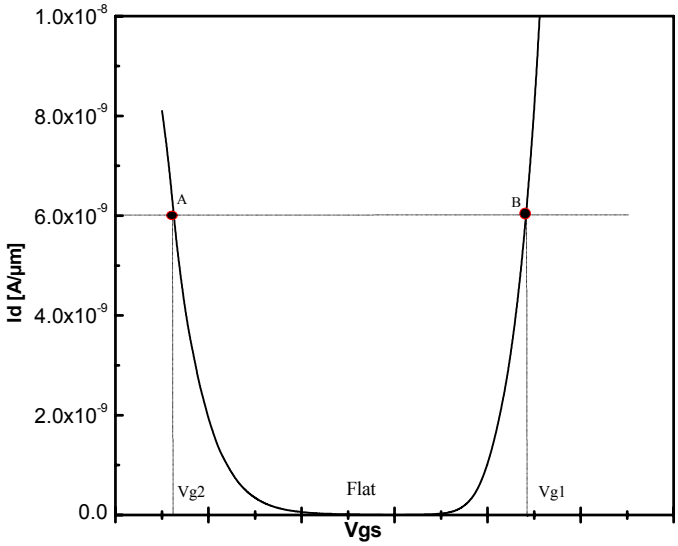


Fig. 5-60 Flat in the experimental TFET transfer characteristics (linear plot)

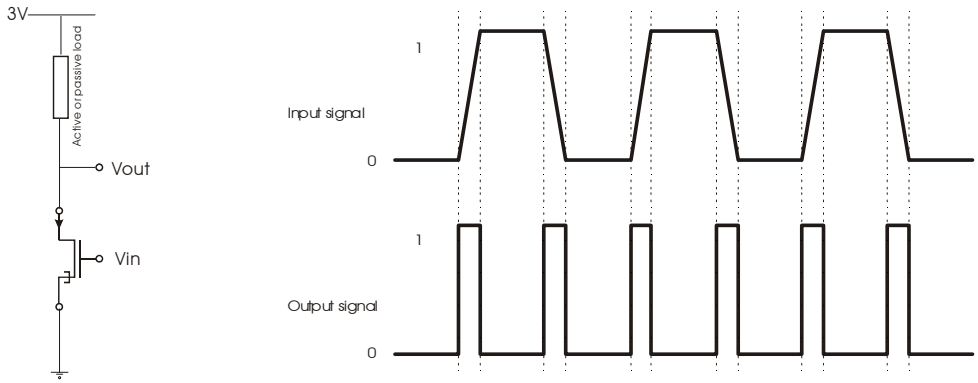


Fig. 5-61 Configuration of the TFET edge detector and the expected transfer characteristics

5.5.7 Integrated complementary TFET (CTFET) inverters

In order to test the static and dynamic performance of TFET in the integrated circuits, the integrated 1-stage and 3-stage inverters are designed and fabricated on silicon wafers. The designed 1-stage and 3-stage inverters are shown in Fig. 5-62. PMOS are used here to be the load. The measurements of a 3-stage inverter need a needle card with 100-200μm space between each needle. This measurement for a 3-stage inverter is still under development. It is possible to compose a 1-stage CTFET inverter by connecting PTFET and NTFET using bonding or by the special connection of needles.

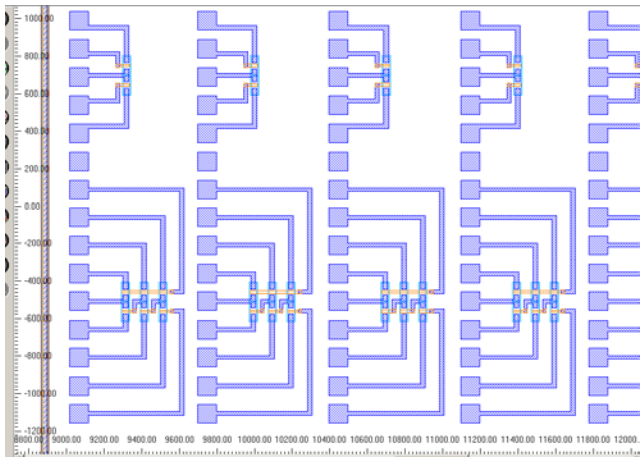


Fig. 5-62 Integrated 1-stage and 3-stage inverters. The neighbour transistors are separated by STI

Since the CTFET invertors shown in Fig. 5-62 are surrounded by STI, the gate metal contacts are broken. Therefore, the inverter characteristics are derived from the transfer or output characteristics of two complementary TFETs on chip. Fig. 5-63 shows the output characteristics of the complementary TFETs. As shown in Fig. 5-64, the switching of this CTFET inverter is fast and the noise margin is large. The reason is that TFET has better saturation behavior and earlier saturation than the conventional MOSFET. The supply voltage of CTFET inverter can be reduced to below 1V considering its small switching region.

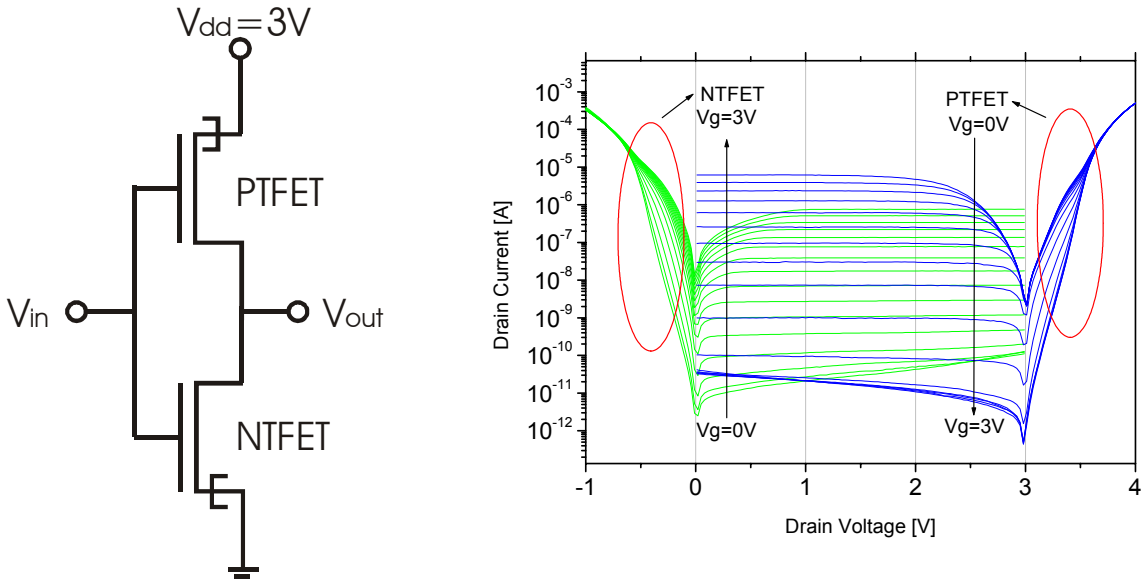


Fig. 5-63 CTFET inverter and the combined output characteristics of two complementary TFETs.

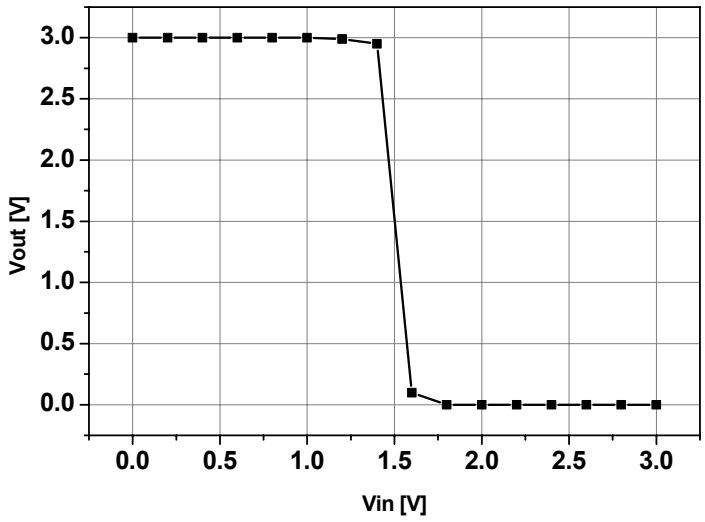


Fig. 5-64 Derived inverter characteristic of a CTFET inverter composed by 4-N3 and 4-T16

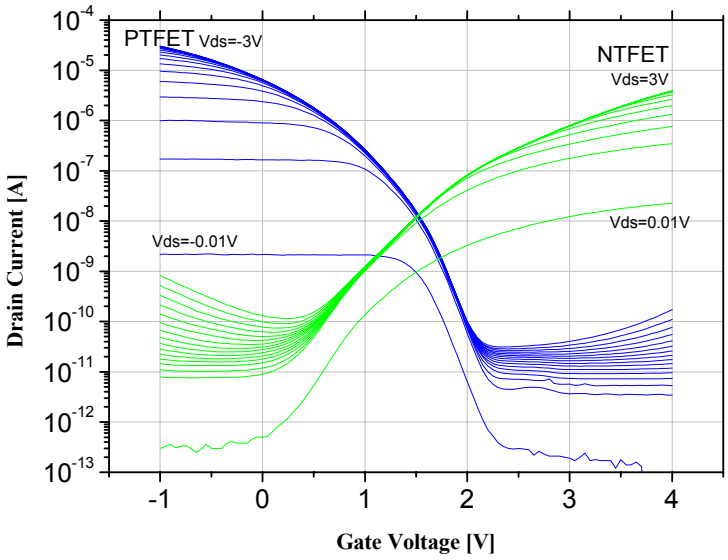


Fig. 5-65 Combined input characteristics of two CTFETs

The CTFET inverter has the advantage of reduced short circuit leakage. As can be seen in the combined input characteristics of two CTFETs (Fig. 5-65), the maximum leakage current in the CTFET inverter is about 15 nA with 3V supply voltage. That means the short circuit leakage current of this CTFET inverter is considerably smaller than that of CMOS inverter. For this reason, the 6-transistor static memory with low stand-by power consumption can be configured using TFETs.

5.6 Conclusion and proposal

5.6.1 Comparison of vertical and planar TFET

After the vertical and planar TFET have been fabricated in our clean-room as well as the vertical TFET in Universität der Bundeswehr München, it is necessary to compare these two types of transistors.

The advantages of the vertical TFET are: 1) The channel length can be defined by the layer growth, especially when MBE technology is applied. 2) The sharp doping profile can be achieved using MBE. The disadvantages of the vertical TFET are: 1) The large G-D, G-S, D-S overlap because the large mesa is needed for the top contact even if the self-aligned gate process is developed. 2) The high quality thin gate oxide is difficult to be fabricated surrounding the vertical mesa. For the planar TFET, the advantages are: 1) Very heavy p and n doping concentration at silicon surface ($> 2\times10^{20}$ cm^{-3}) can be realized. This enables a higher drive current. 2) The smaller G-D, G-S, D-S overlap, especially when the ultra shallow junction is developed using the RT-Diffusion process. 3) Compatible with the CMOS logic circuits and easy for separation and interconnection. 4) When the transistors are fabricated on the SOI wafer, an extremely low leakage current can be achieved. Two challenges are the development of an extreme sharp doping profile and a self-aligned gate process.

5.6.2 TFET properties and applications

Using the CMOS technology compatible process, the complementary NTFET and PTFET are integrated on the silicon wafer. The low leakage current and the room temperature tunneling are observed in the experimental TFET. As a novel semiconductor device, many effects in TFET such as the drain current saturation, the punch-through and avalanche effects, the ballistic electron transport are investigated. The distinct properties of TFET ensure it many advantages, such as the low power dissipation character and the high operating frequency. As an example, the invertor configured by CTFET has a faster switch and a reduced short circuit power consumption than CMOS invertor. Due to the gate-controlled tunneling and the hot electron transport, TFET is suitable for high frequency circuits.

5.6.3 Proposed self-aligned process for the planar TFET fabrication

In order to shrink the channel length, a self-aligned process is proposed for deep sub-micron planar TFET fabrication. The principle of the fabrication process is illustrated in Fig. 5-66. In step 1, a thick LOCOS is grown to define the active region for device fabrication. Here the first mask is needed. This LOCOS is very important because it acts as the diffusion barrier and the dielectric to separate G/D/S from silicon substrate. A SOD P507 layer is deposited and patterned using the vertical etching in the RIE system (step 2). The second mask is needed here to create many straps of P507 film. The etching profile should be vertical for creating a self-aligned spacer gate. In the third step, gate oxidation is performed and the poly-Si film is deposited on the thin gate oxide by LPCVD. One etching-back process in the RIE system will result in a side-wall spacer poly-Si gate. With the third mask, the gate contact pad with a larger pad area is formed. In this step, the gate length is determined by both the vertical etching depth and the thickness of SOD P507. The thickness of SOD P507 film is determined

by the spin-on rotation rate. The details of patterning and thickness control of SOD P507 can be found in chapter 3. The next step is the spin-on of SOD B155 film, the RT-diffusion process and the SOD film removal process. The pattern is shown as step 4 in Fig. 5-66. In this step, no mask is needed due to the self-aligned design. After the thermal diffusion, the n^+ and p^+ doped regions are separated by the side-wall gate. In the fifth step, one mask is needed to separate the poly-Si gate. After this step, two masks are needed for the standard passivation, the contact window opening process, and the contact patterning process. Therefore, in total 6 masks are necessary for the fabrication of deep sub-micron planar TFET. In order to obtain a complementary TFET and complete separation, two additional masks to form p-well and STI can be implanted. Then, 8 masks are needed.

For the narrow spacer gate, a TFET with a channel length shorter than 100nm can be created. The repetition of NTFET and PTFET blocks in this design will make it easier for CMOS-like circuits design. In a word, this process may improve the integration of TFET in silicon wafer remarkably.

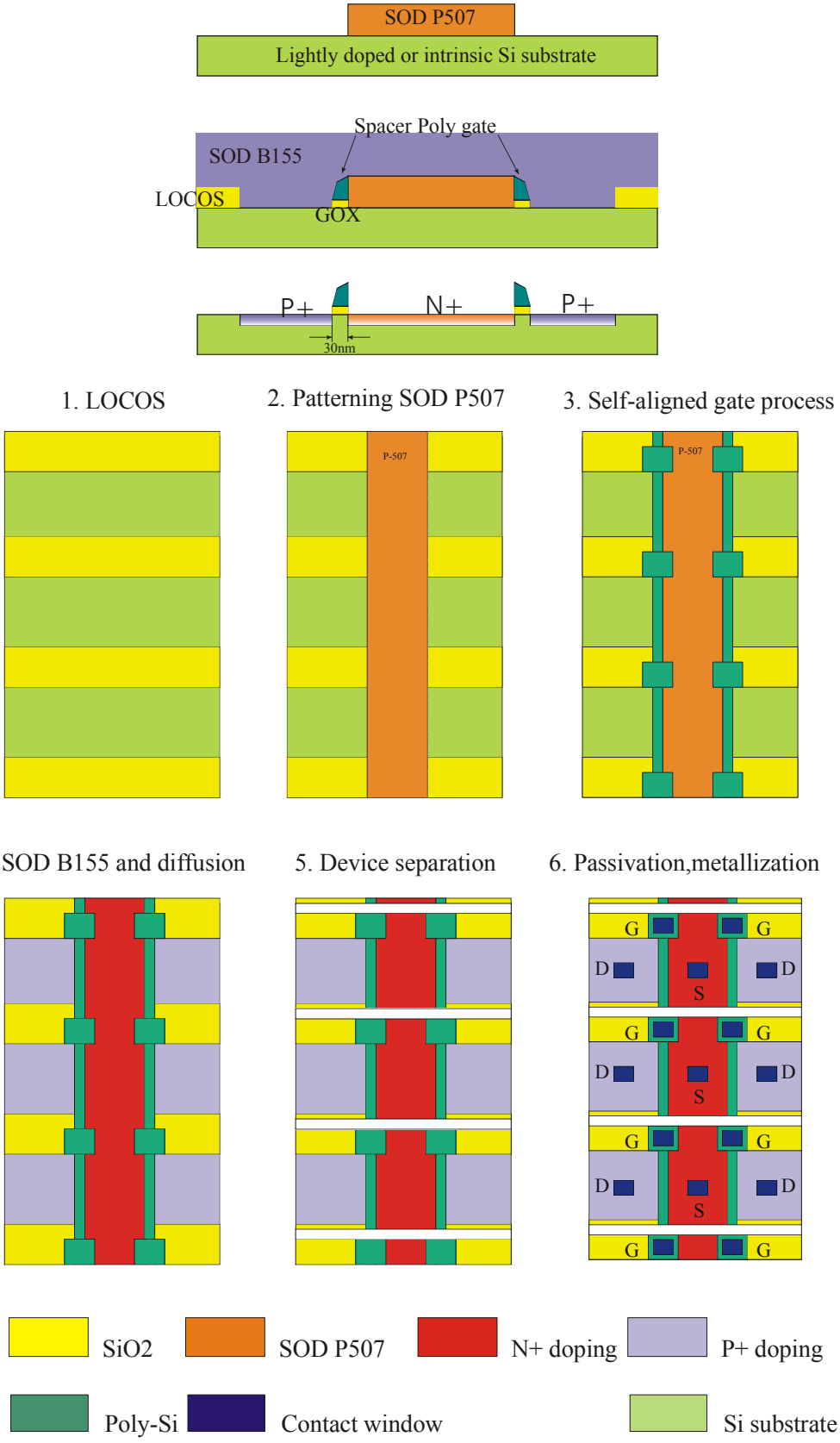


Fig. 5-66 Proposed self-aligned process for the deep sub-micron planar TFET fabrication

Chapter 6

Summary

As a novel transistor, TFET is investigated in detail both in theory and fabrication. In the theory part, the physical principle, the optimized conditions, the future structure, and the comparison to MOSFET are investigated using the MEDICI and SUPREM simulations. To achieve the technological requirements predicted by simulation, the necessary fabrication technologies are improved and investigated. Parallel to the process developments, 6 mask sets were designed and four versions of TFET were fabricated, including the vertical and planar designs. Finally, both NTFET and PTFET were fabricated simultaneously on the n- doped <100> substrate. The experimental characteristics are similar to the simulation.

6.1 Results obtained from the simulation

In the device simulation, the future deep sub-micron NMOS is simulated. The contribution of the band-to-band tunneling current to the leakage current is observed in the vertical NMOS with the heavy channel doping. Even in the double gate / fully depleted (FD) MOS, the band-to-band tunneling leakage still exists when the transistor is turned off. The investigation of the MOSFET band diagram shows that the band-to-band tunneling leakage current cannot be avoided in MOSFET due to the n-p-n or p-n-p structure. In the proposed 100nm TFET with p-i-n structure, where the gate-controlled band-to-band tunneling current is used as the drive current, the leakage current can be remarkably reduced.

In order to fabricate high performance TFETs, the MEDICI simulation of TFET is performed to investigate the impacts of the doping profile, the gate oxide thickness and the source / drain doping level on the device performance. It is obtained from the simulation that fabricating the high performance NTFET needs a sharp doping profile, thin gate oxide and high p-type doping level. For a high performance PTFET, the thin gate oxide, sharp doping profile, and high n-type doping level are needed as well.

The comparison between the simulated TFET and MOSFET indicates the advantages of TFET: a) Attractive for low power application for the lower leakage current due to a higher barrier of the reversed p-i-n junction. b) The active region (band-to-band tunneling region) is about 10nm in such a transistor. The simulation shows that this transistor can be shrunk down to at least 20nm gate length. c) The good performance can be achieved with a 3 nm gate oxide, which circumvents the need of high-k dielectrics. d) The tunneling effect and the velocity overshoot will enhance the device operating speed. e) Much smaller V_t roll-off while scaling. The disadvantages of TFET are: a) Limited drive current which is 2 decades lower than MOSFET. b) In simulation, the 20nm channel length TFET is possible, but the self-

aligned process must be developed for the transistor fabrication. It is a big challenge to fabricate 20nm channel length TFET by diffusion of SOD.

To improve the drive current the following points may help:
1) High p^+ doping (for NTFET) or high n^+ doping (for PTFET). For the planar TFET fabrication, the diffusion should be performed at a higher temperature, but for the shorter diffusion time. Here, as proposed for MOSFET, introducing Ge in S / D will allow high doping levels at lower temperature.
2) Thin equivalent gate oxide thickness. The low temperature atomic layer deposited Al_2O_3 can be applied.
3) Sharp doping profile. The thermal budget in the transistor fabrication should be reduced.
4) Application of the compound materials such as SiGe. If SiGe is applied, the drive current can be improved, but the leakage current may increase as well.

6.2 Process development results

According to the simulation results, the required technologies are developed. The reactive ion etching technology, the heavy boron doping diffusion and the rapid thermal diffusion technology are developed and calibrated in this work. The heavy n-type diffusion process and the gate dry oxidation process are also calibrated.

The semiconductor materials etching in the ECR reactive ion etching system is investigated. The hard masks for the vertical etching, the etching rates of Si, SiO_2, and Si_3N_4 are studied. This technology is applied in the fabrication of the vertical TFET, the vertical mesa diode, the self-aligned gate and the shallow trench isolation (STI) for the device separation.

The n and p type diffusion of SOD is investigated. For n^+ doping, a surface concentration of 2×10^{20} cm^{-3} can be achieved. For p^+ doping, the active surface concentration of boron is about 2.8×10^{20} cm^{-3}. The patterning of SOD P507 is studied in order to form the distinctive doping profile. The patterning and thickness control of SOD P507 makes the self-aligned TFET fabrication process possible. In addition, the SOD B150 precursor is calibrated to form the p-well which enables the fabrication of the complementary TFET on the single n^- doped wafer.

Thin gate oxide fabricated in the normal thermal oxidation oven is studied. The stable 5nm and 6 nm oxide is fabricated at 950°C by dry oxidation. The gate oxidation at 900°C is also studied and applied in the second version planar TFET. The electrical measurements show that using dry oxidation at 900°C for 4 minutes can also ensure good quality thin gate oxide.

The rapid thermal processing is developed and calibrated in this work. The RT-Diffusion can form the ultra-shallow junction. In the second version planar TFET fabrication, the RT-Diffusion is applied to form the n^+ and p^+ regions by the diffusion of SOD films. The fabricated TFETs have a much better performance than those fabricated by the normal thermal diffusion oven.

6.3 TFET fabrication results

In this work, four versions of TFET are fabricated including the vertical TFET and the planar TFET. The self-aligned process in the vertical TFET fabrication is developed. In the fourth version TFET, the RT-Diffusion process is applied to form the n^+ and p^+ regions by the diffusion of SOD films. The planar TFETs with the better performance are fabricated.

Two types of TFETs, PTFET and NTFET are realized on the same substrate. As promised in the simulation, very low leakage current in both NTFET and PTFET is found (e.g. 1.72×10^{-12} A/μm at V_{ds} =1V). Meanwhile, the experimental results match the simulation results very well. The realization of NTFET and PTFET makes it possible to fabricate complementary TFET (CTFET) circuits. The CTFET inverter characteristics are derived. This CTFET inverter indicates the advantages of a larger operation window and a smaller short circuit leakage current than the CMOS inverter.

In order to shrink the channel length, a self-aligned process is proposed for the short channel planar TFET fabrication. For a narrow spacer gate, the TFET with a channel length shorter than 100nm can be created. The repetition of NTFET and PTFET blocks in this design will make it easier for CMOS-like circuits design. This process may improve the integration of TFET in silicon wafer remarkably.

6.4 Conclusions and outlook

The NTFET and PTFET with a very low leakage current are fabricated on the same substrate. This novel transistor has three distinct features: 1) The tunneling current is controlled by the gate voltage. 2) The device is a MOS-gated reverse biased p-i-n structure. This structure results in the low off-current. 3) The tunneling current is achieved at room temperature in silicon.

As shown in the simulation, the leakage current around 1×10^{-16} A/μm can be achieved in the double gate fully depleted NTFET. The fabricated TFET has an off-current of about 1×10^{-12} A/μm which is higher than the simulated off-current due to the bulk leakage. With the SOI wafer and the STI design, the bulk leakage can be further reduced. For the low leakage current, the CTFET circuit is attractive for ultra-low power applications. Although the maximum drive current for TFET is 1.7×10^{-5} A/μm by now, the drive current can be further improved as mentioned in section 6.1. In the simulation, the TFET channel length can be scaled down to 20nm. With such a short channel, the tunneling effect will shorten the electron transition time in the TFET channel remarkably. The gate-controlled tunneling current and the low off-current make TFET attractive in some applications such as low power and microwave circuits.

Appendix A

Medici, Suprem and Taurus Simulation

A.1 TFET device simulation using Medici

MEDICI is a powerful device simulation program for MOS and bipolar transistors and other semiconductor devices. In this work it is used for TFET device simulation.

Following is an example for 2-dimensional TFET device simulation without the electron and hole energy balance equations self-consistent calculation.

```
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

TITLE     sub-Micron NTFET

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

COMMENT   Medici_example.inp
COMMENT   18/4/01
COMMENT   structure: 200nm n+ (1e20) | 100nm p (1e17) | 200 nm p+ (1e20)
COMMENT   Si depth: 100nm
COMMENT   abrupt doping profiles at n+p and pp+ junctions
COMMENT   gate characteristics. Vg: 0V -> +4V
COMMENT   d_oxide=10nm

$----------------------------------------------------------
COMMENT     Specify a rectangular mesh

MESH        SMOOTH=1

X.MESH      WIDTH=0.2  H1=0.02 H2=0.001
X.MESH      WIDTH=0.01  H1=0.001    H2=0.002
X.MESH      WIDTH=0.09  H1=0.006    H2=0.001
X.MESH      WIDTH=0.08  H1=0.003 H2=0.009
X.MESH      WIDTH=0.12  H1=0.009 H2=0.02

Y.MESH      N=1   L=-0.010
```

```
Y.MESH      N=3   L=0.
Y.MESH      DEPTH=0.10 H1=0.001 H2=0.02


ELIMIN      ROWS  X.MAX=0.18  IY.MIN=4
ELIMIN      ROWS  X.MIN=0.305 IY.MIN=4

ELIMIN      COLUMNS     Y.MIN=0.04  X.MIN=0.21  X.MAX=0.29

$-----------------------------------------------------------------------
COMMENT     Specify oxide and silicon regions

REGION      OXIDE    IY.MAX=3
REGION      SILICON     NAME=SILICON1     X.MIN=0.0  X.MAX=0.2    IY.MIN=3
REGION      SILICON     NAME=SILICON2     X.MIN=0.2  X.MAX=0.3    IY.MIN=3
REGION      SILICON     NAME=SILICON3     X.MIN=0.3  X.MAX=0.5    IY.MIN=3

$-----------------------------------------------------------------------
COMMENT     Electrode definition

ELECTR      NAME=Gate     X.MIN=0.0  X.MAX=0.5  TOP
ELECTR      NAME=Drain    IY.MIN=3  LEFT
ELECTR      NAME=Source   IY.MIN=3  RIGHT

$-----------------------------------------------------------------------
COMMENT     Specify impurity profiles and fixed charge

PROFILE     N-TYPE      N.PEAK=1E20       UNIFORM     REGION=SILICON1
PROFILE     P-TYPE      N.PEAK=1E17       UNIFORM     REGION=SILICON2
PROFILE     P-TYPE      N.PEAK=1E20       UNIFORM     REGION=SILICON3

$-------------------------------------------------------------
COMMENT     Plot the doping profile, mesh and structure

PLOT.2D     GRID  TITLE="Initial Grid"  FILL  SCALE
PLOT.1D     DOPING      Y.LOGARI    X.START=0   X.END=0.5
+           Y.START=0.01      Y.END=0.01  TITLE="DOPING PROFILE"

$-------------------------------------------------------------
COMMENT     Regrid on doping

REGRID      DOPING  LOG  IGNORE=OXIDE  RATIO=2  SMOOTH=1

$-------------------------------------------------------------

COMMENT     Specify contact parameters
CONTACT     NAME=Gate  N.POLY

COMMENT     Specify physical models to use
MODELS      CONMOB  FLDMOB  SRFMOB2

COMMENT     Symbolic factorization, solve, regrid on potential
SYMB        CARRIERS=0
METHOD      ICCG  DAMPED
SOLVE

REGRID      POTEN  IGNORE=OXIDE  RATIO=.2  MAX=1  SMOOTH=1

$---------------------------------------------------------------
COMMENT     Solve using the refined grid, save solution for later use
```

```
SYMB        CARRIERS=0
SOLVE       INITIAL          V(Gate)=0   V(Source)=-0.01

COMMENT     Use Newton's method and solve
SYMB        NEWTON  CARRIERS=2
MODELS      CONMOB  FLDMOB  SRFMOB2 CONSRH BTBT IMPACT.I BGN

COMMENT     Setup log file for IV data
LOG         OUT.FILE=example_abrupt_oxide_10nm_drain_min0.01v_Ids_vs_Vg.1d

COMMENT     Solve for Vsd=-0.01 and then ramp gate
SOLVE       V(Source)=-0.01
SOLVE       V(Gate)=0  ELEC=Gate  VSTEP=0.1  NSTEP=40

COMMENT     Plot Ids vs. Vgs
PLOT.1D     Y.AXIS=I(Drain)  X.AXIS=V(Gate)  POINTS  Y.LOGARI COLOR=2
+           TITLE="Vsd=-0.01V"
+           OUT.FILE=example_abrupt_oxide_10nm_drain_min0.01v_Ids_vs_Vg.dat

COMMENT     save the results in a TIF file.
SAVE        OUT.FILE=example_abrupt_oxide_10nm_drain_min0.01v_Ids_vs_Vg.tif
+           TIF ALL
```

For the 2-demensional TFET simulation with energy balance models, the carriers temperature should be calculated. Following is a simulation input file example with the energy balance calculations. A 3-step loop is used to regrid the mesh on the band-to-band tunneling generation rate. SiGe materials can be simulated using this input file, when the corresponding statements for REGION definition are activated.

```
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

TITLE     50nm TFET with Energy-Balance Models

$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

COMMENT   TTEB.inp
COMMENT   12/2/03
COMMENT   structure: 100nm n+ (1e20) | 50nm| 100nm p+ (1e20)
COMMENT   Si depth: 25nm
COMMENT   doping gauss profiles at n+p and pp+ junctions
COMMENT   d_oxide=1nm
COMMENT   Vds=1V


COMMENT   Specify a rectangular mesh
MESH      SMOOTH=1
X.MESH    WIDTH=0.1  H1=0.01 H2=0.003
X.MESH    WIDTH=0.05  H1=0.003 H2=0.003
X.MESH    WIDTH=0.1  H1=0.003 H2=0.01

Y.MESH    N=1   L=-0.001
Y.MESH    N=3   L=0.
Y.MESH    DEPTH=0.025 H1=0.003 H2=0.002



COMMENT   Specify oxide and silicon regions
REGION    SILICON
$ REGION  SiGe    X.MOLE=1    NAME=Ge     X.MIN=0.1  X.MAX=0.15
$+        Y.MIN=0 Y.MAX=0.025
REGION    OXIDE    IY.MAX=3



COMMENT   Electrode definition
ELECTR    NAME=Gate      X.MIN=0.1  X.MAX=0.15  TOP
ELECTR    NAME=Source    IY.MIN=3  LEFT
ELECTR    NAME=Drain     IY.MIN=3  RIGHT

COMMENT   Specify impurity profiles and fixed charge
$PROFILE  N-TYPE  N.PEAK=1E16  UNIFORM
PROFILE   P-TYPE  N.PEAK=1E20   X.MIN=0.0  X.MAX=0.1
+         Y.MIN=0 Y.MAX=0.1 X.Char=0.002 Y.Char=0.001
PROFILE   N-TYPE  N.PEAK=1E20  X.MIN=0.15  X.MAX=0.25
+         Y.MIN=0 Y.MAX=0.1 X.Char=0.002 Y.Char=0.001

PLOT.2D   GRID  TITLE="Initial Grid"  FILL  SCALE

COMMENT     PLOT THE DOPING PROFILE DATA
```

```
PLOT.1D     DOPING      X.START=0   X.END=0.25  Y.START=0.01      Y.END=0.01
+           Y.LOGARI    POINT COLOR=2     TITLE="DOPING PROFILE"
+           OUT.FILE=dop_pro.dat

COMMENT     Regrid on doping
REGRID      DOPING  LOG  IGNORE=OXIDE  RATIO=2  SMOOTH=1   OUT.FILE=1.grid

COMMENT     Regrids on band-to-band tunneling rate with Vd=1v, Vg=1v
LOOP        STEPS=3
ASSIGN      NAME=INITIAL L.VALUE=(T,F,F)
SYMB        CARRIERS=0
METHOD      ICCG DAMPED
IF          COND=@INITIAL
SOLVE       V(Gate)=1 V(Drain)=1 INITIAL
ELSE
SOLVE       V(Gate)=1 V(Drain)=1
IF.END
ASSIGN      NAME=BBRATE N.VALUE=(26,28,30)
REGRID      BB.GENER IGNORE=OXIDE LOG ^CHANGE RATIO=@BBRATE
+           SMOOTH=3

L.END

PLOT.2D     GRID  TITLE="Initial Grid"  FILL  SCALE
COMMENT     Specify contact parameters
CONTACT     NAME=Gate  N.POLY

COMMENT     Specify physical models to use
MODELS      CONMOB    SRFMOB2

COMMENT     Symbolic factorization, solve, regrid on potential
SYMB        CARRIERS=0
METHOD      ICCG  DAMPED


COMMENT     Solve using the refined grid, save solution for later use
SYMB        CARRIERS=0
SOLVE       V(Drain)=1 V(Gate)=0
REGRID      II.GENER  IGNORE=OXIDE  LOG RATIO=1  MAX=1  SMOOTH=1

PLOT.2D     GRID  TITLE="Initial Grid"  FILL  SCALE
COMMENT     Calculate gate characteristics
MODELS      CONMOB  CONSRH  IMPACT.I
SOLVE       INITIAL V(Drain)=0.1 V(Gate)=0
COMMENT     Use Newton's method and solve

MODELS      CONMOB  CONSRH  IMPACT.I BTBT TMPDIF TMPMOB II.TEMP
+           TEMPERAT=400
SYMB        NEWTON  CARRIERS=2 ELE.TEMP

COMMENT     Solve for Vds=1 and then ramp gate

SOLVE       V(Drain)=0.1 Elec=Drain Vstep=0.1 Nstep=9
SOLVE       V(Gate)=0 ELEC=Gate  VSTEP=0.1  NSTEP=14
$SOLVE      Continue Elec=Drain C.Vstep=0.2 C.AUTO C.Toler=0.1 C.Vmin=0.1
$+          C.Vmax=2
COMMENT     Plot Ids vs. Vgs data
PLOT.1D     Y.AXIS=I(Drain)  X.AXIS=V(Gate)
+           OUT.FILE=oxide_1nm_drain_1v_intrinsic_EB_Xchar2nm.dat
```

```
+           POINTS  Y.LOGARI COLOR=2
+           TITLE="Vds=1V"

COMMENT     save the results in a TIF file.
SAVE        OUT.FILE=oxide_1nm_drain_1v_intrinsic_EB_Xchar2nm.tif TIF ALL
```

A.2 TFET process simulation using Suprem

Suprem is a computer program for simulating the processing steps used in the manufacture of silicon integrated circuits and discrete devices. In this thesis the fabrication process of MBE-TFET and SOD diffusion TFET are simulated using this program. Following is an input file example for the vertical MBE-TFET 2-dimensional process simulation.

```
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$
$ TITLE     MBE-TFET PROCESS SIMULATION
$
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$


$           PART ONE, SIMULATION OF DEVICE FORMATION
$           TSUPREM4 FILE
$           Step 1
$           Initial structure definition
$           Specify X mesh
$           Specify x mesh
LINE  X     LOCATION=0     SPACING=0.1    TAG=LEFT
LINE  X     LOCATION=0.5   SPACING=0.0007
LINE  X     LOCATION=1.0   SPACING=0.1    TAG=RIGHT

$           Specify y mesh
LINE  Y     LOCATION=0     SPACING=0.001  TAG=SITOP
LINE  Y     LOCATION=1     SPACING=0.2    TAG=SIBOTTOM

$           eliminate superficial rows
ELIMINATE   ROWS X.MIN=0.6
ELIMINATE   ROWS X.MIN=0.6

$           eliminate superficial columns
ELIMINATE   COLUMNS X.MIN=0.3  X.MAX=0.6  Y.MIN=0.4
ELIMINATE   COLUMNS X.MIN=0.4  X.MAX=0.55 Y.MIN=0.4

$           Define silicon substrates

REGION      SILICON     XLO=LEFT    XHI=RIGHT   YLO=SITOP   YHI=SIBOTTOM
INITIALIZE  <100>       ANTIMONY=2E19

$           change solubility of boron
IMPURITY    IMPURITY=BORON    SS.CLEAR SS.TEMP=700    SS.CONC=1.00e21

$           Plot
SELECT      Z=1   TITLE="mesh 1"
PLOT.2D     GRID  Y.MIN=-1    Y.MAX=1     SCALE       C.GRID=2
SAVEFILE    OUT.FILE=step1.TIF      TIF

$           Step 2
$           Discription of epitaxy layer
EPITAXY    ANTIMONY=2E19      THICKNESS=0.04  TIME=6.67  TEMP=700 +
```

```
           SPACES=10   YDY=0.04   DY=0.001
EPITAXY    ANTIMONY=1E16      THICKNESS=0.04  TIME=6.67  TEMP=700 +
           SPACES=10   YDY=0.04   DY=0.005
EPITAXY    ANTIMONY=1E16      THICKNESS=0.02  TIME=3.33  TEMP=700 +
           SPACES=10   YDY=0.02   DY=0.001
EPITAXY    BORON=4E20     THICKNESS=0.003 TIME=1     TEMP=700 +
           SPACES=3    YDY=0.003  DY=0.001

EPITAXY    BORON=2E19     THICKNESS=0.3   TIME=50    TEMP=700 +
           SPACES=15   YDY=0.3    DY=0.001

SELECT      Z=1   TITLE="mesh 2"
PLOT.2D     GRID  Y.MIN=-1    Y.MAX=1     SCALE C.GRID=2
SAVEFILE    OUT.FILE=step2.TIF      TIF

$           Step 3
$           Mesa etch
ETCH        SILICON     LEFT  P1.X=0.5    P2.Y=0.3

SELECT      Z=1   TITLE="mesh 3"

PLOT.2D     GRID  Y.MIN=-1    Y.MAX=1     SCALE C.GRID=2
SAVEFILE    OUT.FILE=step3.TIF      TIF

$           Step 4
$           OXIDATION

METHOD      VISCOELA
DIFFUSE     TIME=10     TEMP=800    WETO2

SELECT      Z=1   TITLE="mesh 4"
PLOT.2D     GRID  Y.MIN=-1    Y.MAX=1     C.GRID=2    SCALE
SAVEFILE    OUT.FILE=step4.TIF      TIF

$           Step 5
$           Nitride deposition

DEPOSIT     MAT=NITRIDE       THICK=0.1   TEMP=25

SELECT      Z=1   TITLE="mesh 5"
PLOT.2D     GRID  Y.MIN=-1    Y.MAX=1           SCALE C.GRID=2
SAVEFILE    OUT.FILE=step5.TIF      TIF

$           Step 6
$           Nitride Etching

ETCH        MAT=NITRIDE LEFT  P1.X=0.5    P2.Y=0.22

SELECT      Z=1   TITLE="mesh 6"
PLOT.2D     GRID  Y.MIN=-1    Y.MAX=1     SCALE C.GRID=2
SAVEFILE    OUT.FILE=step6.TIF      TIF

$           Step 7
$           Polysilicon deposition

DEPOSIT     MAT=POLYSILI      ANTIMONY=1E20     THICK=0.1   TEMP=25
DIFFUSE     TIME=10     TEMP=600

SELECT      Z=1   TITLE="mesh 7"
PLOT.2D     GRID  Y.MIN=-1    Y.MAX=1           SCALE C.GRID=2
```

```
SAVEFILE    OUT.FILE=step7.TIF      TIF

$           Step 8
$           Poly etching

ETCH        MAT=POLYSILI      LEFT  P1.X=1      P2.Y=-0.18

SELECT      Z=1   TITLE="mesh 8"
PLOT.2D     GRID  Y.MIN=-1    Y.MAX=1           SCALE C.GRID=2
SAVEFILE    OUT.FILE=step8.TIF      TIF

$           Step 9
$           Nitride deposition

DEPOSIT     NITRIDE     THICK=0.2   TEMP=25

SELECT      Z=1   TITLE="mesh 9"
PLOT.2D     GRID  Y.MIN=-1    Y.MAX=1           SCALE C.GRID=2
SAVEFILE    OUT.FILE=step9.TIF      TIF

$           Step 10
$           Nitride etching

ETCH        NITRIDE     LEFT  P1.X=0.25
ETCH        NITRIDE     RIGHT P1.X=0.75

SELECT      Z=1   TITLE="mesh 10"
PLOT.2D     GRID  Y.MIN=-1    Y.MAX=1           SCALE C.GRID=2
SAVEFILE    OUT.FILE=step10.TIF     TIF

$           Step 11
$           OXIDE etching

ETCH        OXIDE RIGHT P1.X=0.75

SELECT      Z=1   TITLE="mesh 11"
PLOT.2D     GRID  Y.MIN=-1    Y.MAX=1           SCALE C.GRID=2
SAVEFILE    OUT.FILE=step11.TIF     TIF

$           Step 12
$           Metal deposition

DEPOSIT     MAT=ALU     THICK=0.4
ETCH        MAT=ALU     RIGHT P1.X=0.75   P2.Y=-1.0
ETCH        MAT=ALU     LEFT  P1.X=0.75   P2.Y=-0.5

SELECT      Z=1   TITLE="mesh 12"
PLOT.2D     GRID  Y.MIN=-1    Y.MAX=1           SCALE C.GRID=2
SAVEFILE    OUT.FILE=step12.TIF     TIF


$           STRUCTURE

STRUCTURE   REFLECT

$           define electrodes
ELECTROD    BOTTOM      NAME=Source
ELECTROD    X=0.1 Y=-0.3      NAME=Gate
ELECTROD    X=1   Y=-0.5      NAME=Drain
```

```
SAVEFILE    OUT.FILE=channel_length_60nm_oxide_10nm MEDICI
SAVEFILE    OUT.FILE=channel_length_60nm_oxide_10nm.tif TIF
$Ploting

$           screen plot

SELECT      Z=DOPING    TITLE="final structure"
PLOT.2D     SCALE Y.MIN=-1    Y.MAX=1
COLOR       SILICON     COLOR=11
COLOR       OXIDE       COLOR=7
COLOR       ALU         COLOR=5
COLOR       POLY        COLOR=3
COLOR       NITRI       COLOR=1
```

To simulate the planar TFET fabricated using the diffusion of SOD instead of the MBE technology, another input file is written for 2-dimensional process simulation. Following shows this input file to simulate the planar TFET with diffusion doping.

```
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$
$
$     PLANAR TFET using DIFFUSION DOPING
$
$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$

$           PART ONE, SIMULATION OF DEVICE FORMATION
$           TSUPREM4 FILE
$           Step 1
$           Initial structure definition
$           Specify X mesh
$           Specify x mesh
LINE  X     LOCATION=0     SPACING=0.2    TAG=LEFT
LINE  X     LOCATION=5   SPACING=0.05
LINE  X     LOCATION=10   SPACING=0.2   TAG=RIGHT

$           Specify y mesh
LINE  Y     LOCATION=0     SPACING=0.02  TAG=SITOP
LINE  Y     LOCATION=5     SPACING=0.5   TAG=SIBOTTOM

$           Define silicon substrates

REGION      SILICON     XLO=LEFT    XHI=RIGHT   YLO=SITOP   YHI=SIBOTTOM
INITIALIZE  <100>       PHOSP=1E17

$           change solubility of boron
IMPURITY    IMPURITY=BORON    SS.CLEAR SS.TEMP=1000   SS.CONC=1.00e22

$           Plot
SELECT      Z=1   TITLE="mesh 1"
PLOT.2D     GRID  Y.MIN=-2    Y.MAX=5     SCALE       C.GRID=2
SAVEFILE    OUT.FILE=step1.TIF      TIF

$           Step 2
$           LOCOS1

DIFFUSE     TIME=30     TEMP=1200   WETO2
SELECT      Z=1   TITLE="mesh 2"
PLOT.2D     GRID  Y.MIN=-2    Y.MAX=5     SCALE       C.GRID=2
SAVEFILE    OUT.FILE=step2.TIF      TIF

$           Step 3
$           LOCOS1 window
ETCH        OXIDE LEFT  P1.X=4

SELECT      Z=1   TITLE="mesh 3"

PLOT.2D     GRID  Y.MIN=-2    Y.MAX=5     SCALE       C.GRID=2
SAVEFILE    OUT.FILE=step3.TIF      TIF

$           Step 4
$           N-SOD Diffusion

DIFFUSE     TIME=20     TEMP=1000   PHOSP=5E20
```

```
SELECT      Z=1   TITLE="mesh 4"
PLOT.2D     GRID  Y.MIN=-2    Y.MAX=5     SCALE       C.GRID=2
SAVEFILE    OUT.FILE=step4.TIF      TIF

$           Step 5
$           LOCOS2
DIFFUSE     TIME=30     TEMP=1000   WETO2
SELECT      Z=1   TITLE="mesh 5"
PLOT.2D     GRID  Y.MIN=-2    Y.MAX=5     SCALE       C.GRID=2
SAVEFILE    OUT.FILE=step5.TIF      TIF

$           Step 6
$           LOCOS2 Etching

ETCH        OXIDE RIGHT P1.X=6
Diffuse     TEMP=1000   TIME=10     BORON=5E20
SELECT      Z=1   TITLE="mesh 6"
PLOT.2D     GRID  Y.MIN=-2    Y.MAX=5     SCALE       C.GRID=2
SAVEFILE    OUT.FILE=step6.TIF      TIF

$           Step 7
$           SiO2 sputtering

DEPOSIT     MAT=OXIDE   THICK=0.5   TEMP=25

SELECT      Z=1   TITLE="mesh 7"
PLOT.2D     GRID  Y.MIN=-2    Y.MAX=5     SCALE       C.GRID=2
SAVEFILE    OUT.FILE=step7.TIF      TIF

$           Step 7.1 Open window and oxidation
Etch        Oxide       START X=4   Y=-2
Etch        Continue    X=6   Y=-2
Etch        Continue    X=6   Y=6
Etch        Done  X=4   Y=6
DIFFUSE     TEMP=1000   TIME=5      DRYO2

SELECT      Z=1   TITLE="mesh 7.1"
PLOT.2D     GRID  Y.MIN=-2    Y.MAX=5     SCALE       C.GRID=2
SAVEFILE    OUT.FILE=step7.1.TIF    TIF

$           Step 8
$           Poly sputtering
Deposit     Poly  THICKNESS=0.5     PHOSP=5E20  TEMP=25

ETCH        MAT=POLYSILI LEFT P1.X=3      P2.Y=3
ETCH        MAT=POLYSILI Right      P1.X=7      P2.Y=3
SELECT      Z=1   TITLE="mesh 8"
PLOT.2D     GRID  Y.MIN=-2    Y.MAX=5     SCALE       C.GRID=2
SAVEFILE    OUT.FILE=step8.TIF      TIF


$           Step 9
$           Nitride deposition

DEPOSIT     NITRIDE     THICK=0.4   TEMP=25

SELECT      Z=1   TITLE="mesh 9"
PLOT.2D     GRID  Y.MIN=-2    Y.MAX=5     SCALE       C.GRID=2
SAVEFILE    OUT.FILE=step9.TIF      TIF
```

```
$           Step 10
$           Nitride etching

ETCH        NITRIDE     LEFT  P1.X=2
ETCH        NITRIDE     RIGHT P1.X=8
Etch        NITRIDE     START X=4   Y=-6
Etch        Continue    X=6   Y=-6
Etch        Continue    X=6   Y=4
Etch        Done  X=4   Y=4
ETCH        OXIDE
SELECT      Z=1   TITLE="mesh 10"
PLOT.2D     GRID  Y.MIN=-2    Y.MAX=5     SCALE       C.GRID=2
SAVEFILE    OUT.FILE=step10.TIF     TIF

$           Step 11
$           Metal deposition

DEPOSIT     MAT=ALU     THICK=0.4
Etch        ALU   START X=2   Y=-6
Etch        Continue    X=4   Y=-6
Etch        Continue    X=4   Y=4
Etch        Done  X=2   Y=4

Etch        ALU   START X=8   Y=-6
Etch        Continue    X=6   Y=-6
Etch        Continue    X=6   Y=4
Etch        Done  X=8   Y=4

SELECT      Z=1   TITLE="mesh 11"
PLOT.2D     GRID  Y.MIN=-2    Y.MAX=5     SCALE       C.GRID=2
SAVEFILE    OUT.FILE=step11.TIF     TIF

$           define electrodes
ELECTROD    X=1   Y=0.1 NAME=Source
ELECTROD    X=5   Y=-0.5      NAME=Gate
ELECTROD    X=9   Y=0   NAME=Drain

SAVEFILE    OUT.FILE=Planar_TFET_1000C_10min MEDICI
SAVEFILE    OUT.FILE=Planar_TFET_1000C_10min.tif TIF
$Ploting

$           screen plot

SELECT      Z=DOPING    TITLE="final structure"
PLOT.2D     SCALE Y.MIN=-2    Y.MAX=5
COLOR       SILICON     COLOR=11
COLOR       OXIDE       COLOR=7
COLOR       ALU         COLOR=5
COLOR       POLY        COLOR=3
COLOR       NITRI       COLOR=1
```

A.3 TFET 3-dimensional process simulation

Taurus Process & Device is a multidimensional process and device simulation program. On the process side, it simulates the fabrication steps used to manufacture semiconductor devices. On the device side, it simulates complete electrical and thermal characteristics of semiconductor devices. In this thesis, the input file for TFET 3-dimensional Taurus process simulation is written. The following is this 3-D simulation input file for TFET process simulation.

```
##################################
#
# 0.18 um TFET with STI isolation.
#
##################################

Taurus {process}

DefineDevice (Name=STI,
xSize=1um,
ySize=0.6um,
zSize=0.5um,
boron=1.0e16,
AmbientHeight=1.um,
Regrid(MinDelta=1um),
regridinteration=0)
# Calculate strain in silicon for strain induced bgn in device simulation
# Physics (Global (Global (KeepStressHistory)))
# STI
Deposit (Material=TEOS, Thickness=0.1um, Regrid(MinDelta=1um),
regriditeration=0)
Etch (Thickness=0.4um,
Angle=95,
Regrid(MinDelta=1um),
regriditeration=0,
MaskPolygon(Point(x=0.1um, y=-0.11um, z=-0.3um),
Point(x=0.9um, y=-0.11um, z=-0.3um),
Point(x=0.9um, y=-0.11um, z= 0.45um),
Point(x=0.1um, y=-0.11um, z= 0.45um))
)
Save (MeshFile=sti00.tdf,
MeshFile=sti00.tree, AnalyticFile=sti00.dope)

#------N doping----------
Deposit (Material=teos, thickness=0.1um, Regrid(MinDelta=1um),
regriditeration=0)
Etch (material=teos,thickness=0.4um, Regrid(MinDelta=1um),
regriditeration=0,
Maskpolygon(Point(x=0.1um, y=-0.11um, z=-0.3um),
Point(x=0.4um, y=-0.11um, z=-0.3um),
Point(x=0.4um, y=-0.11um, z= 0.4um),
Point(x=0.1um, y=-0.11um, z= 0.4um)),Negative
)
Diffuse (time=20min, temperature=1000C,
Phosphorus=5E20)
Save (MeshFile=sti02.tdf,MeshFile=sti02.tree,
AnalyticFile=sti02.dope)
```

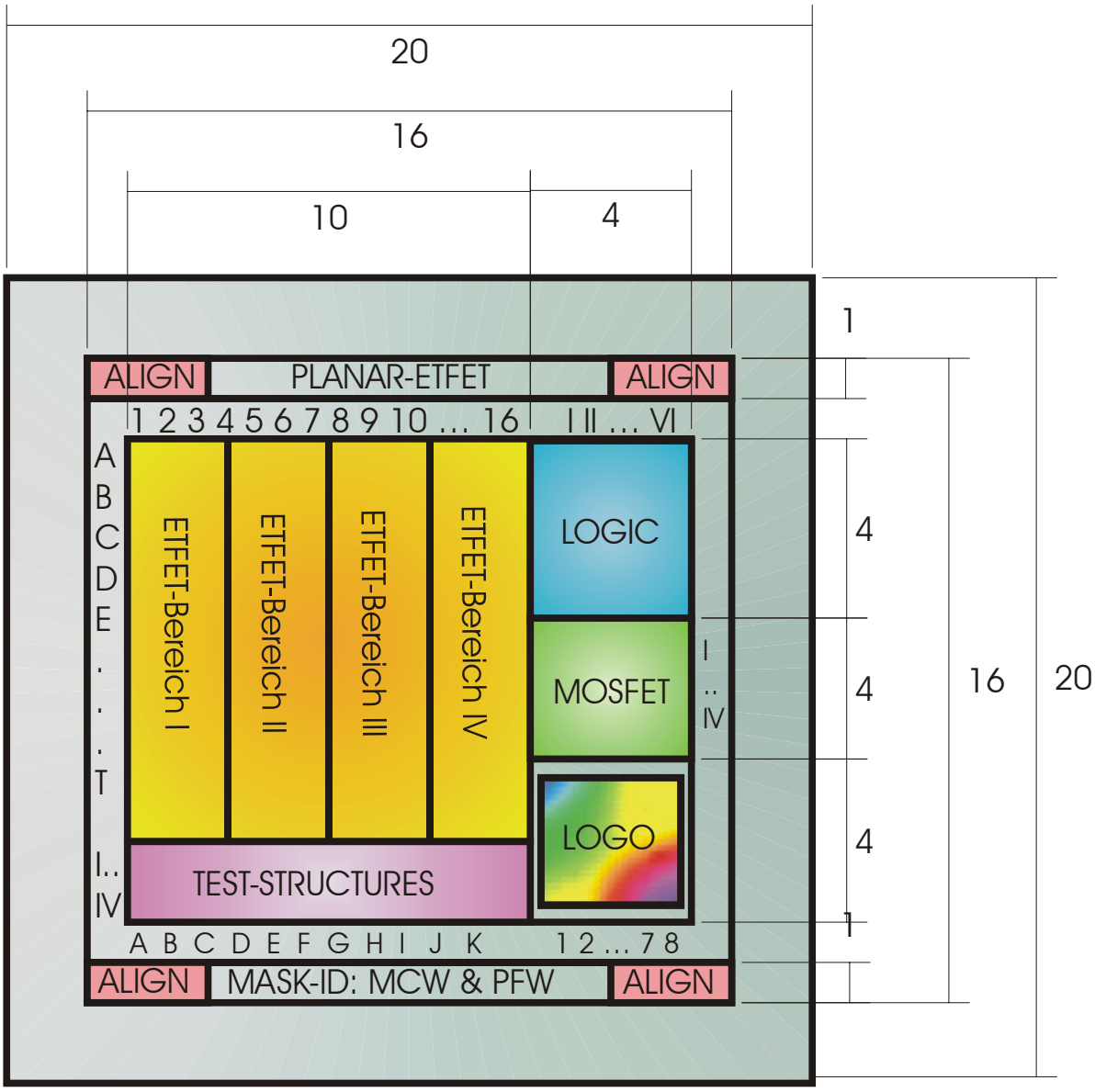
```
#-----P doping----

Deposit (Material=teos, thickness=0.1um, Regrid(MinDelta=1um),
regriditeration=0)

Etch (Material=teos,thickness=0.3um, Regrid(MinDelta=1um),
regriditeration=0,
Maskpolygon(Point(x=0.6um, y=-0.61um, z=-0.3um),
Point(x=0.9um, y=-0.61um, z=-0.3um),
Point(x=0.9um, y=-0.61um, z= 0.4um),
Point(x=0.6um, y=-0.61um, z= 0.4um)),Negative
)
Diffuse (time=10min, temperature=1000C, Boron=5E20)
Save (MeshFile=sti2.1.tdf,MeshFile=sti2.1.tree,
AnalyticFile=sti2.1.dope)

#----gate window
Deposit (Material=teos, thickness=0.1um, Regrid(MinDelta=1um),
regriditeration=0)
Etch (Material=teos,thickness=1um, Regrid(MinDelta=1um),
regriditeration=0,
Maskpolygon(Point(x=0.4um, y=-0.61um, z=-0.3um),
Point(x=0.6um, y=-0.61um, z=-0.3um),
Point(x=0.6um, y=-0.61um, z= 0.4um),
Point(x=0.4um, y=-0.61um, z= 0.4um)),Negative
)
Save (MeshFile=sti2.2.tdf,MeshFile=sti2.2.tree,
AnalyticFile=sti2.2.dope)

#------gate oxide--
Diffuse (Time=5min, Temperature=950C, DryO2)
Save (MeshFile=sti03.tdf,MeshFile=sti03.tree,
AnalyticFile=sti03.dope)

#---Metal gate----
Deposit (Material=Aluminum, Thickness=0.1um, Regrid(MinDelta=1um),
regriditeration=0)
Save (MeshFile=sti04.tdf,MeshFile=sti04.tree,
AnalyticFile=sti04.dope)
Etch
(
Material=Aluminum, Regrid(MinDelta=1um),
regriditeration=0,
MaskPolygon
(
Point(z=-1um, y=-1, x=0.4um),
Point(z=-1um, y=-1, x=0.6um),
Point(z=1um, y=-1, x=0.6um),
Point(z=1um, y=-1, x=0.4um)
)
)
Save (MeshFile=sti05.tdf,MeshFile=sti05.tree,
AnalyticFile=sti05.dope)

#----passivation--
Deposit (Material=oxide, Thickness=0.1um, Regrid(MinDelta=1um),
regriditeration=0)
Save (MeshFile=sti06.tdf,MeshFile=sti06.tree,
AnalyticFile=sti06.dope)
```

```
#---- Contact windows (use negative etching logic)
Etch
(
thickness=0.6um, Regrid(MinDelta=1um),angle=90,
regriditeration=0, negative, anisotropic,
MaskPolygon
(
Point(z=-1um, y=-1, x=0.1um),
Point(z=-1um, y=-1, x=0.3um),
Point(z=0.3um, y=-1, x=0.3um),
Point(z=0.3um, y=-1, x=0.1um)
)
)
Etch
(
thickness=0.6um, Regrid(MinDelta=1um),angle=90,
regriditeration=0, negative, anisotropic,
MaskPolygon
(
Point(z=-1um, y=-1, x=0.7um),
Point(z=0.3um, y=-1, x=0.7um),
Point(z=0.3um, y=-1, x=0.9um),
Point(z=-1um, y=-1, x=0.9um)
)
)
Etch (Material=teos)
Save (MeshFile=sti07.tdf,MeshFile=sti07.tree,
AnalyticFile=sti07.dope)
# Aluminum
Deposit (Material=aluminum, Thickness=0.25um, Regrid(MinDelta=1um),
regriditeration=0)
Save (MeshFile=sti08.tdf,MeshFile=sti08.tree,
AnalyticFile=sti08.dope)
Etch
(
Material=aluminum, Regrid(MinDelta=1um),
regriditeration=0,
MaskPolygon
(
Point(z=-1um, y=-1, x=-1um),
Point(z=-1um, y=-1, x=0.3um),
Point(z=0.3um, y=-1, x=0.3um),
Point(z=0.3um, y=-1, x=-1um)
)
MaskPolygon
(
Point(z=-1um, y=-1, x=0.7um),
Point(z=0.3um, y=-1, x=0.7um),
Point(z=0.3um, y=-1, x=2um),
Point(z=-1um, y=-1, x=2um)
)
)
Save (MeshFile=sti09.tdf,MeshFile=sti09.tree,
AnalyticFile=sti09.dope)
Stop ()
```

Appendix B

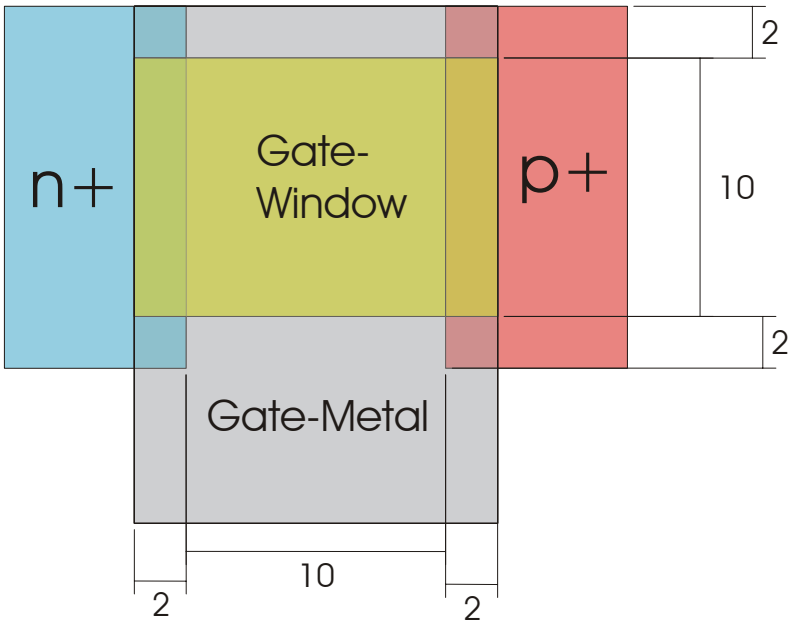
2nd Version Planar TFET Mask

B.1 Overview of the mask for the 2nd version planar TFET

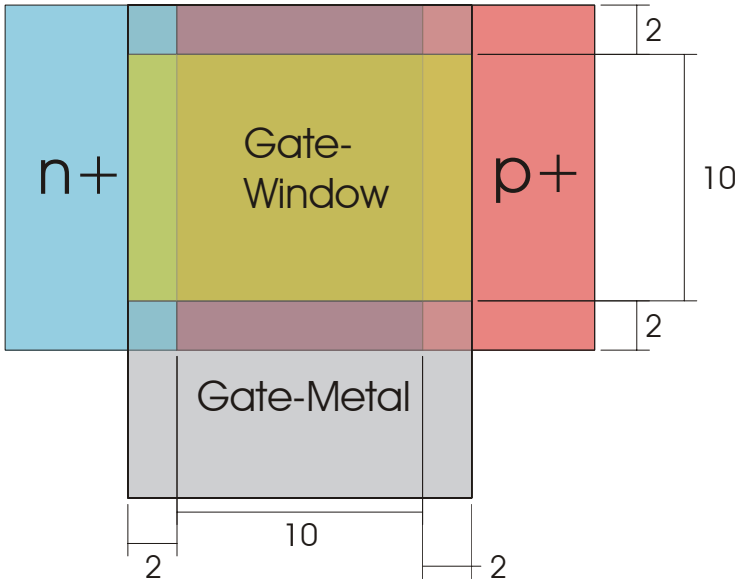


B.2 Different TFET structural designs

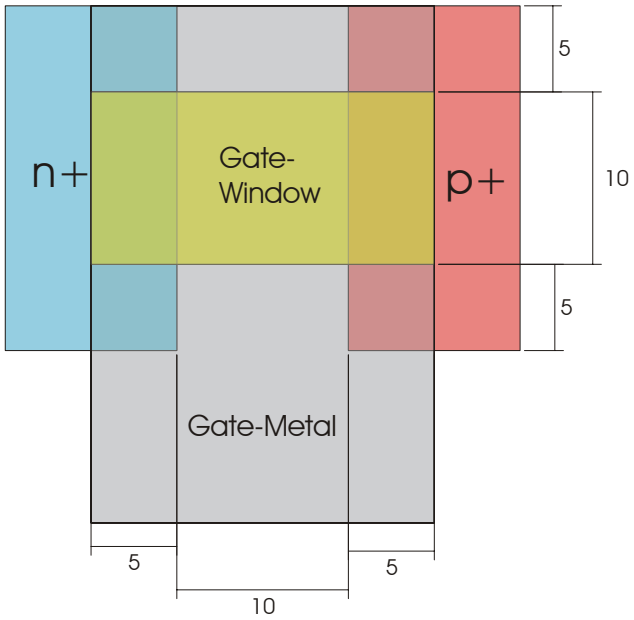
a) Structural information: 2µm security design; the gate window is narrower than the diffusion windows; no S / D overlap.



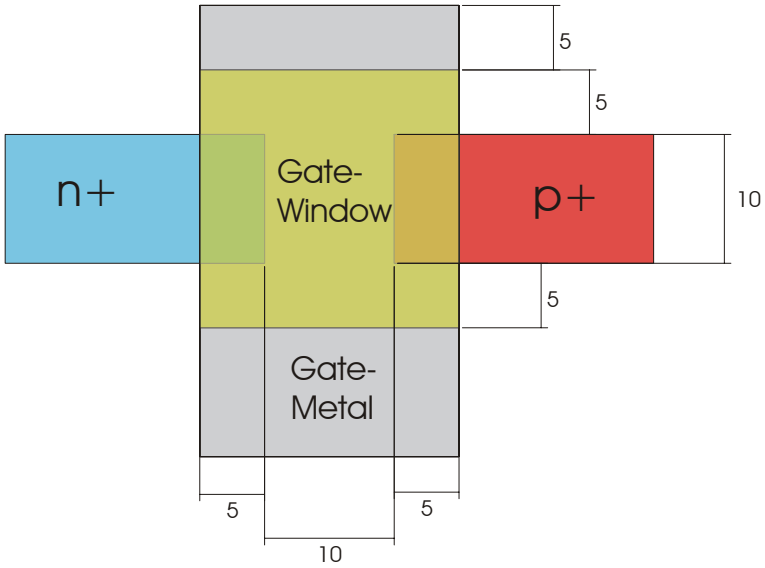
b) Structural information: 2µm security design; the gate window is narrower than the diffusion windows; with S / D overlap.



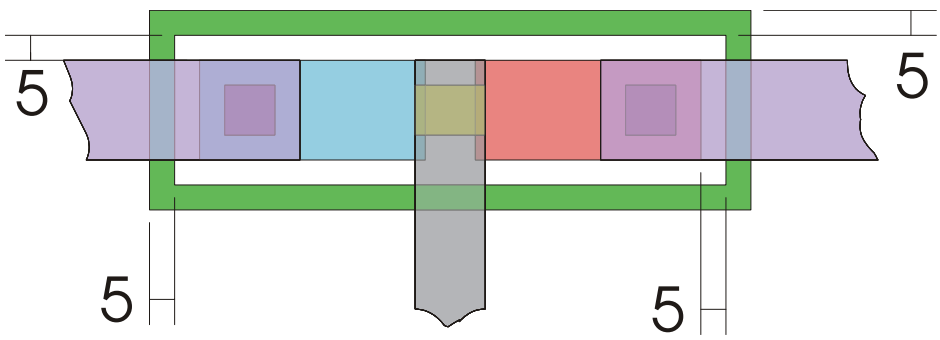
c) Structural information: 5µm security design; the gate window is narrower than the diffusion windows; no S / D overlap.



d) Structural information: 5µm security design; the gate window is wider than the diffusion windows; no S / D overlap.



e) TFETs with the surrounding STI.



Appendix C

List of Symbols and Abbreviations

Symbols	Description
C	Capacitance
E_V	Top of valance band
E_g	Energy band gap
E_{Vaccum}	Vaccum energy level
G_n	Electron generation rate
G_p	Hole generation rate
I	Current
m_e^*	Effective mass of electron
m_h^*	Effective mass of hole
N_A	Concentration of accepter
N_C	State density in the conduction band
N_D	Concentration of donor
N_V	State density in the valance band
S	Subthreshold swing
T	Temperature
t_{ox}	Oxide thichness
V	Voltage
V_t	Threshold voltage
$X.CHAR$	Characteristic length “X” in the Gaussian function
Ψ_{bulk}	Bulk potential
μ_n	Electron mobility
μ_p	Hole mobility

Abbreviations	Description
ALD	Atomic layer deposition
BB.GENER or G.BB	Generation rate of band-to-band tunneling
BGN	Band gap narrowing model
BHF	Buffered HF solution
BTBT	Band-to-band recombination-generation
CONMOB	Concentration dependent mobility model
CTFET	Complementary TFET
DIBL	Drain induced barrier lowering
DITL	Drain induced tunneling-barrier lowering
ECR	Electron cyclotron resonance
EOT	Equivalent oxide thickness
FD-MOS	Fully depleted MOSFET
FLDMOB	Parallel field mobility model
GIDL	Gate induced drain leakage
GOX	Gate oxide
II.GENER or G.II	Generation rate of impact ionization
ITRS	International technology roadmap for semiconductors
LOCOS	Local oxide for separation
LPCVD	Low pressure chemical vapor deposition
MBE	Molecular beam epitaxy
MOSFET	Metal-oxide-semiconductor field effect transistor
PECVD	Plasma enhanced chemical vapor deposition
RTD	Rapid thermal diffusion
RTP	Rapid thermal processing
RIE	Reactive ion etching
RTCVD	Rapid thermal chemical vapor deposition
SCE	Short channel effect
SIMS	Secondary ion mass spectrometry
SOD	Spin-on-doping
SOI	Silicon-on-insulator
SRFMOB2	Enhanced surface mobility model
SRH	Shockley-Read-Hall (recombination-generation)
STI	Shallow trench isolation
TFET	Tunneling field effect transistor

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