LOW-POWER DA-CONVERTERS FOR DISPLAY APPLICATIONS USING STEPWISE CHARGING AND CHARGE RECOVERY

C. Saas, A. Wróblewski and J.A.Nossek

Munich University of Technology, Institute for Circuit Theory and Signal processing
Arcisstr. 16, D-80298 München
chsa@nws.ei.tum.de

ABSTRACT

The application of adiabatic switching for driving high capacitive loads encountered on the column lines of flat panel displays is investigated. A new digital-to-analog converter using stepwise charging is proposed to minimize power dissipation. Most of the energy stored on the charged column lines can be recovered. The proposed DAC is capable of driving the high capacitive load without any bias current. Therefore, both dynamic and static power dissipation are reduced to a large extent. Simulations of the proposed architecture are compared with a lower bound for the power dissipation based on a simplified model of a conventional implementation demonstrating the potential of the new approach.

1. INTRODUCTION

In applications where a back-light panel is not always required, the control and driving circuits of a flat panel display consume a significant part of the dissipated power [8]. It has been shown [5], [9] that adiabatic switching provides promising results when used for high capacitive, simple logic and low speed applications. All of these requirements are fulfilled when driving column lines in a flat panel display. The investigations presented in this paper are applicable to most kinds of flat panel displays regardless of the actual display element. Nevertheless, the obtained results are based on models for active matrix LCD and OLED displays.
The principle of stepwise charging for driving displays has already been presented in [2], but its use was limited to the polarity change necessary in a LCD display. In this work stepwise charging is applied to actually charge the capacitance to the desired voltage level. There are two distinct problems present in this application. First of all the row lines have to be charged to a fixed supply voltage to open the pass transistors of a pixel row. This is comparable to driving the output pad of an integrated circuit [5, 6] and will not be covered in this paper. Second, the charging of the column lines is a difficult task as a certain voltage level depending on the actual image content has to be reached. This voltage level represents the brightness of the pixel and therefore has to be maintained accurately. In Section 2 a conventional approach is described, which serves as a reference for comparison, while in Section 3 the new approach is outlined. In Section 4 simulation results are presented followed by a conclusive Section 5.

Stepwise charging

Stepwise charging is a method to reduce the power dissipated during the charging of a capacitance. The voltage ramps required for adiabatic switching are approximated by a number of rectangular steps. When a linear capacitance C is charged by a voltage step U the dissipated energy is

$$E = \frac{1}{2}CU^2. \tag{1}$$

Using stepwise charging the voltage step is only $\frac{U}{N}$, where N is the number of steps used. Of course this step occurs N times, but it can easily be calculated that this leads to a power reduction of $\frac{1}{N}$ with respect to a full voltage swing

$$E_{stepwise} = N\frac{1}{2}C(\frac{U}{N})^2 = \frac{1}{N}E. \tag{2}$$

Therefore the higher the number of steps the bigger the power savings. The calculations made here are only valid if the time between the steps is long enough for the system to settle. Stepwise charging involves like all adiabatic techniques a trade off between power and speed.

2. CONVENTIONAL APPROACH

The architecture of a conventional column driver is depicted in Fig. 1. It consists of a single DAC, an analog shift register ASR and analog drivers for each line. The digital pixel stream is decoded for the DAC in the decoder L. In this structure the DAC consumes only a small part of the area and the power. A lot of effort has to be made to realize the highly precise analog shift register. The main source for energy dissipation are the drivers.

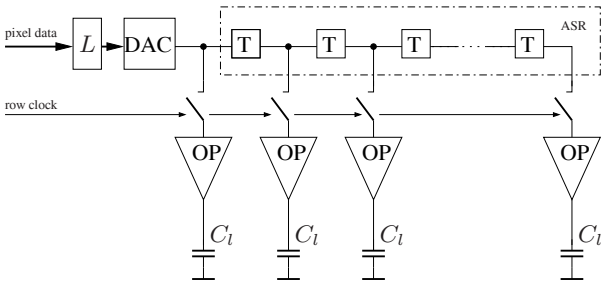

Fig. 1. Architecture of a conventional column driver

Power estimation

Due to a large number of available operational amplifier designs simulations have not been performed on a reference design up to

now. Instead, we estimated the dissipated power by means of analytical formulae. In the line driver there are two main sources for energy dissipation. The first one is rather obvious and results from the charging and discharging of the line capacitance. As there is no charge recovery the energy dissipated during one cycle is given by

$$E_{dyn} = CU^2 \tag{3}$$

where C is the capacitance of the column line and U is the voltage difference between the off level and the desired pixel value. All other parasitic capacitances can be considered to be small with regards to C and have been neglected.
The second one results from the bias currents in the operational amplifiers. Their value can be estimated from the specifications regarding load and performance. For a Miller OTA the overdrive voltage is given by [7]

$$u_{overdrive} = \frac{SR}{GBW}.$$

The slew rate SR and the gain band width GBW are given by the performance requirements. The second pole has to be located at $p_2 = 3 \cdot GBW$ to fulfill stability criteria for a full feedback configuration. The resulting transconductance g_m is given by:

$$g_m = 3 \cdot GBW \cdot C_L.$$

To obtain this transconductance a bias current of

$$I_{BIAS} = g_m \cdot u_{overdrive} \tag{4}$$

is needed. Please note, that only the bias current for the last stage has been taken into account and the significantly smaller current for the input stage has been neglected.
Both, P_{BIAS} and $Pdyn$ are based on ideal models and therefore don't take any leakage or resistive losses into account. All simplifications and assumptions made reduce the calculated power consumption. Therefore P_{BIAS} and $Pdyn$ can be regarded as a lower bound for the dissipated energy. The calculated values for the regarded environment can be seen in Table 1.

Voltage	4.2 V		
number of rows	1200	$P_{dyn}(010)$	$2.88e-05W$
display-height	20 cm	$P_{dyn}(110)$	$2.60e-04W$
line capacitance	$1\frac{fF}{\mu m}$ [4]	$P_{dyn}(111)$	$3.53e-04W$
image refresh	60 Hz	P_{Bias}	$4.80e-04W$
row clock	100kHz		

Table 1. given and calculated values for the used environment

3. PROPOSED APPROACH

The proposed architecture (Fig. 2) implements as many components as possible in the digital domain as to minimize the effort in power and area for analog components. The presented DA converter is capable of driving the lines and therefore there is no need for analog line drivers. The digital registers consume significantly less energy than the analog counterpart. Although the new logic L' is slightly more complicated and one DAC is needed at each line, the power consumption is negligible with respect to the bias currents of the conventional line drivers.

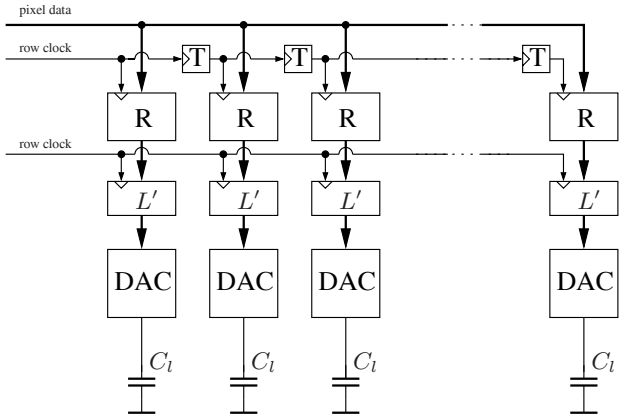

Fig. 2. Architecture of the proposed column driver

To keep the explanation simple only a 3 bit DAC is evaluated, which is on no account a limitation. Improvements like cascading can be applied by introducing mere modifications to the logic L'. Therefore it should be no problem to extend bit depth even further on. Nevertheless when, as in most cases, more bits are required a multi stage hybrid DAC might be useful. Evaluations regarding this topic are currently going on.

3.1. Stepwise charging with fixed reference voltages

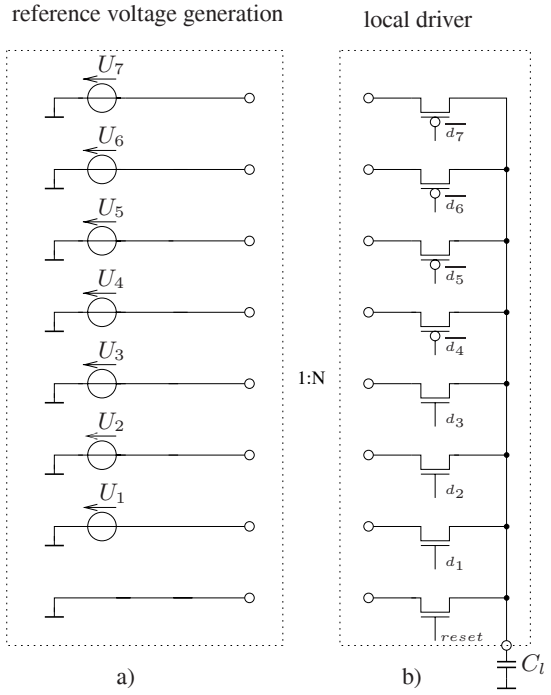

Fig. 3. Schematic for FR-DAC

The basic idea of stepwise charging is demonstrated on the example of the fixed reference DA converter (FR-DAC) in Fig. 3. It

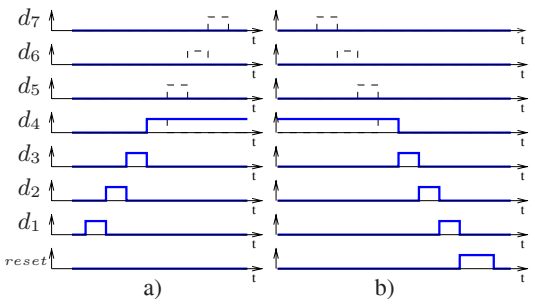

Fig. 4. Input bits for a digital value of 100 a) charging b) discharging of CR-DAC

is able to reduce dissipated energy and maintain high accuracy at the same time. To obtain the FR-DAC only small modifications to a standard resistor string DA converter is needed. Each line is driven by one FR-DAC in which the dynamic losses due to capacitive load are dissipated. Stepwise charging is realized by applying a digital control signal, which will switch the output to the next higher value for each time step until the desired voltage level is reached. An example for the control signal can be seen in Fig. 4a. They are calculated by the logic block L' from the digital pixel value obtained from the register. A similar decoder is also present in the conventional DAC. Both decoders have as many outputs as the DAC can produce voltage levels. In the FR-DAC however, instead of setting the pin corresponding to the desired voltage level to high all pins with lower values will be set to high one after another. This will result in a stepwise charging of the output up to the desired voltage level. To benefit from the possible power savings it is important to ensure that an intermediate voltage level is almost reached before the next clock edge. The clock used in this domain of the circuit will be called DAC clock. It has to be at least N times faster than the row clock of the display where N is the number of voltage levels. This does not present any problems as the row clock is usually not time critical. The DAC clock can be derived from the pixel clock.

This solution will generate an area overhead by introducing a DA converter for every line. The area overhead is reduced by avoiding the analog shift register and the output drivers at each column. Despite the area overhead there is a significant reduction in power consumption. The reduction is only achieved during charging of the output. All energy stored on the charged output capacitor is lost during discharging. No stepwise discharging has to be applied, a simple reset switch is enough to realize distinct voltage peaks. In certain cases some of the energy can be saved by not resetting the output, but starting at the voltage level of the last pixel. Most of the time this is not possible due to pixel inversion.

3.2. Charge recovery during discharging

A significant part of the energy on the line can be recovered by applying some technique of charge recovery. In several publications [1, 3] charge recovery using resonant RLC circuits in a flat panel display is limited to recover energy during the change of polarization. In this work large capacitors are used to temporarily deliver energy and to recover the charge when driving analog output voltages.

In Fig. 5a the schematic of the reference voltage generation circuit for the charge recovery DA converter (CR-DAC) is shown. There is one large source capacitor C_s per reference voltage. It is charged by reference voltage sources to the appropriate voltage level during the reset period. Afterwards the whole DAC is powered from the capacitors.

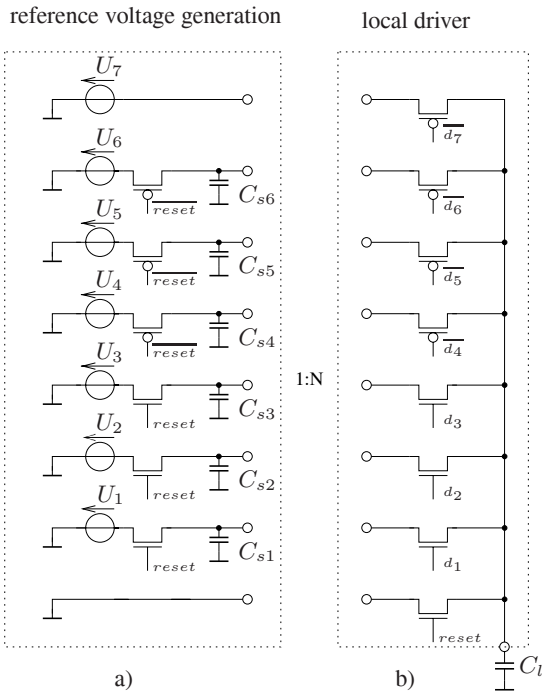

Fig. 5. Schematic for CR-DAC

Connecting the line capacitance C_l to the source capacitor C_{s1-6} will result in a voltage equalization. The line voltage will increase whereas the voltage of the source capacitor slightly decrease. As the resulting voltage level U is given by

$$U = \frac{C_s}{C_l + C_s} U_s + \frac{C_l}{C_l + C_s} U_l \tag{5}$$

the source capacitances have to be large. The error of the line voltage with respect to the desired voltage depends on the size of C_s. Please note, that this is a systematic offset error which can easily be compensated by calibration. As there is only one reference voltage generator per display, the source capacitors could be realized as external elements.

During charging of the output the CR-DAC works like the FR-DAC. The reference voltages are connected one after another to the output thus charging it up in small steps. During discharging most of the energy can be transferred back onto the C_s. The output is discharged stepwise by connecting the load to the appropriate reference voltages. Thus every clock cycle the output voltage is decreased by $\frac{U}{N}$. When the output is connected to the next lower reference voltage level some of the charge is transfered back to C_s and the corresponding reference voltage across C_s is nearly restoring the initial value. Of course, there can be no energy transferred to the highest voltage level. The amount of energy taken from this reference voltage is prorated on the charging and discharging of the single steps. In the following reset the losses are compensated by connecting C_s to the appropriate reference voltage. It can

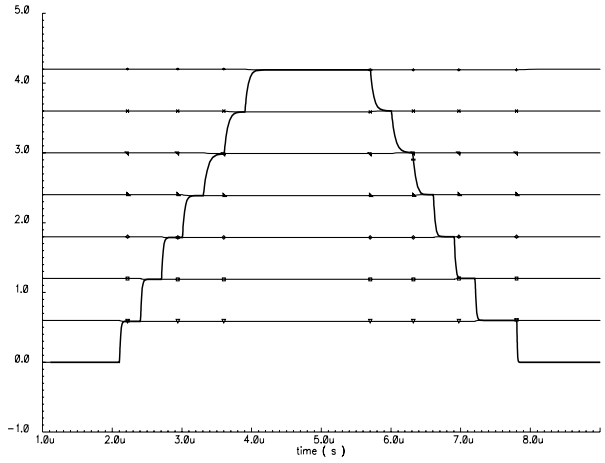

Fig. 6. Output voltage and reference voltages of the CR-DAC

easily be calculated that in theory all but the highest source capacitors C_{smax} recover charge up to their original voltage value. The energy which has been dissipated and thus has to be replaced in C_{smax} is given by

$$E_{smax} = \frac{U}{N} \cdot U_{max} \cdot C_l \tag{6}$$

where U_{max} is the voltage the line was charged up to and C_{smax} the corresponding source capacitor.
Currently research is done on the realization of low impedance reference voltage sources. As a final solution has not been chosen up to now power dissipation in the reference voltage generation has not been considered.
Using the precharge already present on the line is investigated. We do not expect results in power dissipation to change significantly, as most of the charge is recovered in the CR-DAC. Anyhow this would only be applicable if it is compatible to the pixel inversion scheme.

4. SIMULATION RESULTS

Figure 6 shows the simulated output transition for a pixel value of 111. The operation of the circuit can clearly be observed. Stepwise charging is working as expected. The voltage drop on the reference voltages is very small. The simulation results given in table 4 demonstrate a significant reduction in energy dissipation. For a value of 111 the power consumption is reduced to only 5%. As expected the dominant part of power dissipation occurs on the reference voltage corresponding to the desired output level as there is no charge recovery. The dissipated energy scales linearly with the pixel value. Therefore P_{dyn} benefits more from the reduced voltage for lower pixel values, but even in the extreme case, where the pixel value is 000, there is still a reduction to 9% due to the reduction of bias currents.

5. CONCLUSION

In this work the concept of stepwise charging has been applied to the field of display drivers. A novel digital analog converter has been proposed. It is capable of recovering most of the charge stored on the line capacitance during discharge and can be directly connected to the line thus avoiding the need for power intensive operational amplifiers. The resulting new architecture may lead to some area overhead but consumes significantly less energy.
Further work has to be done on increasing the bit depth by applying a second DAC stage. Probably this second stage is also capable of correcting the small error introduced by the CR-DAC. Different realisations of low impedance reference sources have to be evaluated.
Overall this concept seems to be very promising to dramatically reduce power consumption of flat panel display drivers with an acceptable overhead.

pixel value	010	110	111
P_{smax}	1.44e-05	4.32e-05	5.04e-05
$P_{V1}[W]$	-1.03e-08	-1.51e-07	-1.51e-07
$P_{V2}[W]$	1.45e-05	2.26e-08	2.27e-08
$P_{V3}[W]$	-4.31e-10	-1.16e-09	-1.36e-09
$P_{V4}[W]$	-4.55e-10	-8.00e-08	-9.29e-08
$P_{V5}[W]$	8.61e-10	6.75e-07	-4.71e-08
$P_{V6}[W]$	1.15e-09	4.35e-05	9.07e-07
$P_{V7}[W]$	-8.72e-10	-7.80e-10	5.06e-05
$P_{ges}[W]$	1.45e-05	4.39e-05	5.13e-05

Table 2. Simulated power dissipations for the CR-DAC

6. REFERENCES

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