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Device Aging in Analog Circuits for Nanoelectronic CMOS Technologies

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Chapter 1

Summary

This work covers an elementary study on the emerging topic of device degradation and the impacts on CMOS analog circuits. Thereby, aging effects are considered leading to a time and stress dependent drift of device characteristics but not to a destruction of the device itself. In fact, parameter drift can also lead to a circuit fail due to a violation of specification. The considered degradation effects are known as Bias Temperature Instability (BTI) and Hot-Carrier Injection (HCI). Different from the numerous investigations on the aging effects themselves, this study starts from the circuit point of view, taking into consideration typical circuit related device design constraints and arising operation states. To provide results valid for future circuit design in latest CMOS processes, the used CMOS technology provides an advanced 32nm high-κ, metal gate process. This approach reduces occurring device aging for most of the cases to a domination of area independent BTI effects due to the typical large area devices used to provide accurate analog signal processing. Distinct investigations on elementary analog circuitries like current-mirrors, reference circuits, amplifiers and oscillators gave a fundamental insight into the individual sensitivity of these circuits towards the aging of incorporated devices. Studies are performed on exemplary state-of-the-art circuitry and the found results are generalized so that they are universally valid and mostly transferable to other circuit implementations. The focus is on the circuit dependent performance parameter with largest impact by device degradation, which is used as circuit aging output monitor, but also accompanying second order effects on other circuit characteristics are studied. With analytic approaches to describe circuit aging dependent on critical operation states, a new circuit reliability concept is developed, providing deeper insight into circuit aging than all other state-of-the art reliability tools do up to now. This forms the basis for the development of new concepts and approaches to provide equivalent but accelerated circuit level aging for test and the usage of the built-in circuit's analog signal processing to measure degradation effect behavior, which is not included in today's degradation modeling. But also countermeasures are derived by profiting from general effect behavior on circuit level for an aging suppression, that even offers new design approaches with respect to area requirements given by matching specifications. All relevant findings are approved by stress measurement on hardware built in the high-κ, metal gate CMOS process. The universal validity of the found results provides circuit designers the knowledge about aging criti-

cal circuit blocks and operation states. Furthermore, recommendations for aging aware circuit design and outlooks to future circuit aging behavior in novel CMOS processes are provided in this work.

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Chapter 2

Introduction

2.1 Motivation

Since the early days of microelectronics, integrated MOSFET (Metal Oxide Semiconductor Field Effect Transistor) technology has been continuously advanced by dimension shrink. Via the equivalent scaling of relevant processing parameters - channel area, oxide thickness and supply voltage - the fundamental device characteristic keeps the same with less area and power consumption. This general feature forms the basis of today's triumph of microelectronics and the initiation of the information era.
But CMOS (Complementary Metal Oxide Semiconductor) - the processing of n- and p-type MOSFETS on one chip - technology scaling has to face some inheritable problems like device noise and process fluctuations, that are given by semiconductor physics, processing imperfections and its atomic limitations. For example, the circuit relevant SNR (Signal to Noise Ratio) reduces for every technology step as voltage headroom is reduced with decreased supply voltage, but device noise contributions remain constant. Since the 0.1 um regime, CMOS processing migrates to the *non-constant field scaling* approach, by keeping the supply voltage at higher levels than would be required by the scaling factor, while all other parameters are scaled in the usual way. Here, raised electric fields in MOS devices are accepted at the cost of increased wearout, thus worsening device reliability but maintaining sufficient SNR. At the same time, higher integration rates with increased chip complexity demand for an enhanced device reliability to maintain a stable and reliable system, which has to be further provided by the CMOS processing. In the past, this was achieved by the continuing optimization of the chip processing, but the gap between the optimization window and limiting semiconductor physics reduces and device aging mechanisms come to the fore.
Condensed operation of MOSFET devices at only slightly reduced supply voltages further leads to increased on-chip operation temperatures, that even worsen device wearout. On the other hand, reduction in voltage headroom increases circuit sensitivity towards device aging. Advanced CMOS processing options like the inclusion of novel high-κ materials into the MOS gate stack lowers gate leakage, but further debuts device aging effects that were nonexistent in classic SiO_2 or $SiON$ based CMOS technologies. The general shrink

of channel length further induces novel aging effects, that even occur for switched off devices. Increased circuit sensitivity and growing appearance of aging effects in magnitude and number involve the reliability topic as an emerging concern in today's and future CMOS microelectronics [1, 2].
The impact of device wearout on circuit level was only rudimentary studied in the past, as occurring minor device parameter drifts were covered by design techniques like *guard banding* or mitigated by the operation in *safe operation area*. Contrary to the inherently robust digital circuits, where device wearout mainly leads to an increase of switching delay, analog circuitry is more sensitive towards a change of device characteristics like drive current, transconductance or noise behavior. The requested compliance of numerous circuit performance specifications to maintain proper system functionality makes reliability proofs for analog circuits more challenging. With the increased appearance of device aging effects in advanced CMOS technologies, their impact on circuit level demands for future research effort [3]. But also circuit level reliability measurement proofs arise as a challenging task, as an accelerated stress methodology to exactly reproduce equivalent end-of-lifetime states is still missing.

2.2 State-of-the-Art in Circuit Reliability Research

Previous circuit design mostly treated device aging as a side effect, that is covered by design margins applied for balancing PVT (Process Voltage Temperature) variations. Nowadays, device aging obtained an individual status as growing source of device variability in the extension to PVTA (Process Voltage Temperature Aging) variations. Growing interest on device degradation lead to several studies on the impact of device aging on circuit level. For *digital* logic circuits the general aging induced weakening of the device characteristic increases logic gates' switching delay and so induces a time dependent degradation of the data evaluation. This increase of propagation delay can lead to a time dependent violation of timing constraints in the critical path and so to failure of the circuitry [4, 5, 6]. Several detection and sensing approaches, for example using replica circuits to provide a kind of aging odometer [7], are developed and countermeasures are proposed [8]. A general approach to detect and compensate for PVTA variation induced logic errors is treated in [9]. Another relevant field of research is the digital SRAM (Static Random Access Memory), as reliable data storage has to be guaranteed with minimum feature size devices for millions of cells. Reliability investigations revealed, that device degradation in the asymmetric storage state varies SRAM cell stability [10, 11]. Due to the minimum feature size devices, process variations and variations in the degradation effect as well play an important role for the reliability of the storage system. Transient components in device degradations additionally include a time dependent component for the cell stability [12].
For analog and mixed-signal circuits, performance characteristics and thus device aging impacts are more complex [13]. Especially for circuit designs in advanced high-κ CMOS nodes, the aggravated device aging demands for novel and detailed studies [14]. For analog circuits, a most essential constraint is device matching, that can be changed by the device degradation [15, 16] and can be seen as another source of variation additional to

process variations [17, 18]. The investigation of Agostinelli on a differential amplifier revealed that asymmetric stress operation induces device mismatch and thus induces circuit offset [16]. In the study on selected amplifiers of Martin-Martinez, variability is identified as the major concern for advanced CMOS technologies, which is accompanied by aging induced drift contributions. Variability in the aging effect itself was found to be of minor concern. The study further reveals that aging impacts amplifier gain and GBW (Gain Band Width) dependent on the circuit topology [19]. A detailed investigation on the effect variability for the used devices as well as a general statement on aging sensitive topologies is still missing. In the fundamental work of Thewes, a state-of-the-art differential amplifier is used to study analog circuit reliability according to numerous aging effects. From the point of view of distinct circuit operation states, occurring device stress and resulting aging effects are determined. Aging effects are again expected to degrade circuit performance in offset, gain, noise and linearity. Here, BTI (Bias Temperature Instability) effects, induced by high oxide fields, are expected to arise as the most prominent challenges in future robust circuit design [20]. In the work of Kawasumi, HCI (Hot-Carrier Injection) is beneficially used to perform calibration of an SRAM sense amplifier [21].
With an automated reliability simulator, an ADC (Analog to Digital Converter) circuit is studied with respect to the impact of device aging by Yan [22]. Several countermeasures like device sizing for improved HCI degradation or a reduction of power consumption to reduce NBTI (Negative Bias Temperature Instability) aging are evaluated. Nevertheless, a deep understanding of the interaction between device degradation and circuit behavior is still missing.
In [23], Jha investigated the impact of NBTI on selected basic analog circuit blocks like current mirrors, amplifiers and a current-steering DAC (Digital to Analog Converter). The study showed that device aging impact strongly depends on the circuit topology. For the current mirror circuits for example, huge differences in general aging sensitivity can be seen. Investigations on amplifier circuits reveal large aging induced offset generation for open-loop comparator operation. Due to stable current biasing, transconductance of the circuit remains stable and further impact on performance parameters like gain or GBW are small. For the current-steering DAC, NBTI degradation is expected to induce considerable gain errors, but only minor impact on its linearity. This study shows that sensitivity of the analog circuit strongly depends on its configuration. However, universal rules for aging robust circuitry are not provided.
Further analog circuit types, that are in the focus of reliability investigations, are LC based VCO (Voltage Controlled Oscillator) circuits. This is mainly due to the high voltage swings during circuit operation [24, 25]. In his study, Lin revealed considerable VCO performance degradations related to HCI device degradation [26]. Sadat showed in [27] that degradation of active bridge devices impacts oscillation amplitude and thus the effective value of the tank capacitance, that further modifies oscillator Phase Noise and startup behavior. Current-reusing CMOS VCO designs are determined to be the most reliable oscillator topologies due to amplitude limitation by the voltage supply. In [28], Reddy reported a significant VCO Phase Noise degradation in the close-in region related to a NCHCI (Non-Conductive Hot-Carrier Injection) induced worsening in device flicker noise - a device characteristic, that is typically not considered in todays aging prediction models.

Several studies in the past years showed the increasing impact of device aging on analog circuit blocks and further brought up the most critical analog circuit types. Nevertheless, a throughout and universal study performed on state-of-the-art analog circuit designs, providing insight into the mechanisms of the circuit related impact of device aging, is still missing. Analog circuit related device aging taking into consideration typical device dimensions and operation states has to be investigated in detail for advanced CMOS technologies, to reveal analog related degradation behavior as well as expected variations of the aging mechanisms. Selected circuit designs have to be investigated with respect to their general aging sensitivity to establish approaches for future robust circuit designs. Novel circuit aging modeling approaches, expanding results from circuit reliability simulations, will provide deep understanding of device aging and circuit interaction and will break new ground for aging countermeasures and circuit stress testing as well.

2.3 Contributions of this Work

In this work a detailed overview over major device aging effects, leading to parametric drifts of device characteristics, but not to a hard destruction of the device is provided. Most recent findings on distinct effect physics and resulting aging prediction model approaches are discussed. Options for consideration of device degradation in classic circuit simulations are reviewed with respect to analog circuit simulation suitability.
Device aging for typical analog operation scenarios for an advanced CMOS process technology is studied by simulation and stress measurements. In doing so, analog related device aging - not entirely covered by state-of-the-art modeling - is investigated in detail, taking into consideration typical operation states, device dimensions and analog relevant effect properties. Operation modes like accumulation, which are not considered so far and potentially occur during circuit standby, are shown to be another significant reliability issue. Further investigations on aging effect variability as well as transient recovery reveal the need for novel aging models, that are close to the basing physics. Additionally, it is shown that degradation effects can be beneficially used also for passive reliability improvement.
Throughout investigations on device aging impact on a wide area of analog circuit building blocks are the foundation for a general overview of major circuit aging monitors and the behavior dependent on the operation state. For instance, current mirror circuits experience current mismatch, amplifiers offset and oscillators power degradation. Further case studies on distinct device and circuit types like varactors and reference generation circuits showed a minor impact of device wearout.
Circuit level aging is very complex, due to the simultaneous interaction of distinct device degradation effects and distinct dominant effects are not per se detectable. A general methodology to accurately predict aging on circuit level is performed via fully analytic modeling of circuit behavior, that further provides a deep insight into major effect contributions. This approach allows to derive further aging related design concepts and to easily account for circuit level degradation in future CMOS process technologies.
Via circuit degradation models, a methodology to accurately determine end-of-lifetime equivalent circuit states for accelerated stress test is developed and validated via mea-

surement for selected circuit types. Furthermore, customized circuit type specific stress testbenches are developed and described providing the ability to stress and measure circuit performance in one test setup. This novel approach allows to use analog circuits' signal sensitivity for further aging effect characterisation, like device flicker noise degradation in oscillator Phase Noise behavior or short-time recovery in fast amplifier circuits. Design related aging countermeasures for reliable analog circuit operation are proposed and evaluated. Furthermore, a novel method to suppress device aging and simultaneously use the induced device parameter drift for circuit calibration is proposed and verified via measurements. From the overall findings and circuit investigations, guidelines for design of reliable analog circuits are established.

The throughout and general investigation on the complex impact of device degradation in state-of-the-art analog circuitry provides together with the proposed circuit aging modeling, stress test evaluations and countermeasures a novel and fundamental basis to handle the emerging reliability topic for analog circuit design.

Chapter 3

Aging Physics

3.1 CMOS Device Wearout

As most technical products, also integrated CMOS devices suffer from wearout due to their usage in electronic devices. High integration in today's ICs (Integrated Circuits), with billions of MOS transistors on one die, demands MOS (Metal Oxide Semiconductor) insulator thickness of a few nanometers between the controlling gate and the channel. Electric fields across the oxide reach MV/cm although operating in the 1V regime. Those lead to a time dependent wearout of insulators' properties inducing changes in the device characteristics or in worst case to its breakdown. As mentioned in 2.1, technology scaling by inducing non-constant field scaling and inclusion of new materials in the gate stack worsens this wearout from technology node to node.
Aging mechanisms can be separated in two groups: mechanisms leading to drift of device characteristics, but not to an immediate malfunction of the transistor - the so called *non-destructive* aging mechanisms, including BTI and HCI effects. And the *destructive* mechanisms like TDDB (Time Dependent Dielectric Breakdown)[29, 30] leading to a permanent malfunction of the device. Precursors to the TDDB are the SBD (Soft Breakdown) effects inducing a temporary breakdown of the device. After stress removal, device is working again.
Our investigation on analog circuit aging addresses the *non-destructive* aging mechanisms, as those are able to change circuit behavior during lifetime operation. In advance to a dielectric breakdown a huge amount of parameter drift occurs, also acting as a precursor to the hard breakdown. From the system point of view it is not only the hard breakdown of an incorporated device leading to malfunction, but also drifts in performance specifications of the analog circuit can lead to failure of the overall system.

3.2 Impact on Device Parameters

All *non-destructive* aging mechanisms have in common that insulator wearout is due to inclusion of charge into the insulator region. This additional charge changes device

characteristic in several ways. As derived in lots of semiconductor textbooks, *threshold voltage* V_{th} of an exemplary nMOS (see fig. 3.1) with zero Bulk-Source voltage $V_{BS} = 0$ is defined as the inversion mode Gate voltage where electron (minority carrier) density in the inversion region is equal to hole (majority carrier) density of the bulk in thermal equilibrium [31, 32].
The physical representation of the threshold voltage condition is given by

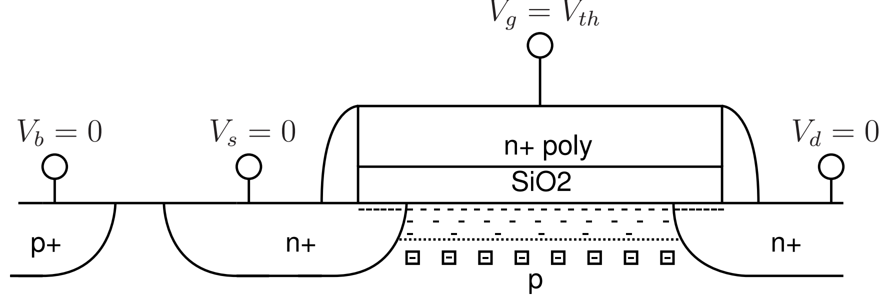

Fig. 3.1: nMOS: threshold voltage virgin device

$$V_{th} = V_{FB} + 2\Phi_F + \gamma_n\sqrt{2\Phi_F} \tag{3.1}$$

with V_{FB} the flatband voltage, Φ_F the Fermi level from intrinsic Fermi level and γ_n the Body factor for a nMOSFET, that is dependent on the bulk doping and the dielectric constant of the insulator.
A uniformly distributed charge Q_{deg} in the interface to the insulator, as depicted in fig.

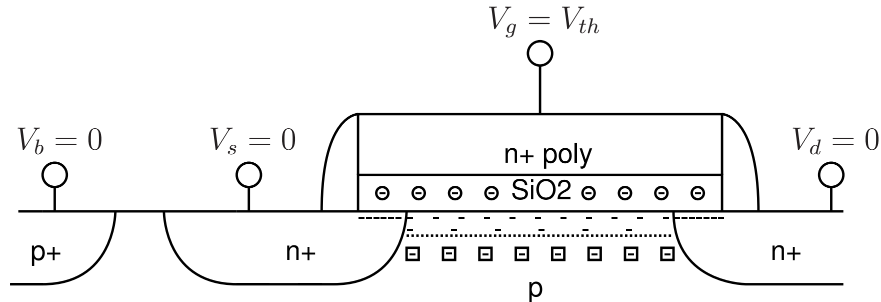

Fig. 3.2: nMOS: threshold voltage degraded device

3.2, would shift the flatband voltage to

$$V_{FB} = \Phi_{MS} - \frac{Q_{deg}}{C_{oxide}} \tag{3.2}$$

with Φ_{MS} the workfunction difference between gate material and bulk and C_{oxide} the gate oxide capacitance. Depending on the amount of generated charge, V_{FB} and so V_{th} is shifted by

$$\Delta V_{th,n} = \Delta V_{FB} = -\frac{Q_{deg}}{C_{oxide}}. \tag{3.3}$$

Equation (3.3) also shows that the direction of the V_{th} shift depends on the polarity of the generated charge.
Furthermore, induced oxide charges also impact field dependent effective channel mobility μ_{eff}. Equation (3.4) shows the relation of μ_{eff} with respect to device operation condition.

$$\mu_{eff} = \frac{\mu_0}{1 + \Theta(V_g - V_{th,n})} \tag{3.4}$$

with μ_0 the low field surface mobility, Θ the mobility degradation coefficient and V_g the gate voltage. Equation (3.4) reveals a direct relation of μ_{eff} to a drift in threshold voltage [33]. But also μ_0 can be affected by oxide charges at the $Si - SiO_2$ interface acting as Coulomb scattering centers and changing the interface roughness and hence μ_0 and Θ [34]. The often discussed degradation of further device parameters as *drain current* I_D, *transconductance* g_m, *subthreshold swing* SS or MOS $C - V$ characteristic can be related to the drift of basic MOS parameters V_{th} and μ_0. These general impacts of device wearout were derived for an exemplary nMOS device, but are also valid for the pMOS counterpart.

3.3 Bias Temperature Instability (BTI)

NBTI for pMOS as well as PBTI (Positive Bias Temperature Instability) for nMOS transistors are derived from the typical inversion mode operation of CMOS devices and their degradation behavior under elevated temperatures. Both effects lead to a general weakening of the transistor characteristic. BTI degradation is strongly dependent on the oxide field given by eq. (3.5) for strong inversion,

$$F_{el,ox} = \frac{V_g - V_{FB} - 2\Phi_F}{t_{ox}} \tag{3.5}$$

with V_{FB} the flatband voltage, Φ_F the Fermi Potential defined by the well doping and the lattice temperature and t_{ox} the insulator thickness. As shown by eq. (3.5), V_g and t_{ox} are key parameters for the BTI degradation.
BTI effects, especially the NBTI in pMOS transistors, were already observed in the early days of MOSFET development [35]. In this decade NBTI was not concerned as a major reliability issue as impact on the formerly buried channel with n+ poly gate for the pMOS was small. Due to *constant field scaling* in CMOS technology development, that means a similar scaling of V_g and t_{ox}, NBTI was well controlled. Changeover to surface channel p+ poly gate pMOSFET increased the NBTI sensitivity. Particularly, the introduction of *non-constant field scaling* in sub-0.1μ CMOS technologies, typically keeping or slightly decreasing V_g but scaling t_{ox} in the classic manner, enhanced NBTI as one major degradation mechanism. A corresponding PBTI for nMOS transistor was negligibly small for SiO_2 based oxides, but emerged with the introduction of high-κ materials in advanced CMOS technologies also for the nMOS transistor [36].

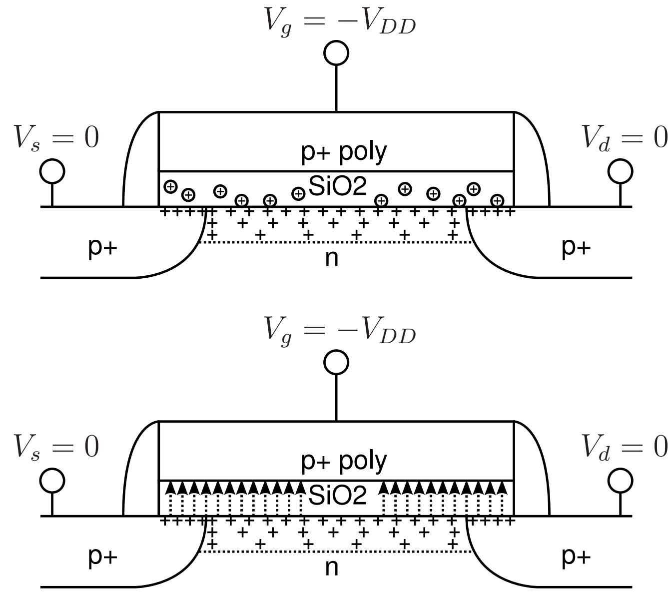

Fig. 3.3: pMOS in triode operation: NBTI stress generated defects and arising electric field under NBTI stress

3.3.1 NBTI in pMOSFETs

Figure 3.3 shows the inversion mode NBTI stress condition and the resulting oxide degradation for an exemplary pMOSFET - the transistor's deep triode region with zero voltage drop over the channel. Source, Drain and Substrate are connected to ground and V_g is set to a high negative value inducing an inversion layer in the n-well and an accumulation layer in the Source and Drain overlap regions. The electric field in the insulator on the inverted channel is given by eq. (3.5). Under high $F_{el,ox}$, oxide quality degrades by the trapping of charge. Insulator degradation also happens in the Source/Drain overlap regions, but with minor impact due to the distance to the controlled inversion channel. Fig. 3.4 shows the situation for a pMOS device in saturation region. Also in this operation mode NBTI degradation occurs, but due to the decreasing electric field from the Source to the Drain region with smaller total degradation [34].
Lots of literature on NBTI and its involved mechanisms for differing CMOS gate stacks is available. Due to strong sensitivity towards processing and included materials, lots of differing degradation numbers and effect explanations exist. The general accepted mechanisms are the generation of *interface states* at the substrate oxide interface and the electric activation of *oxide charges*, that is due to the activation of pre-existing defects or generation of new defects in the insulator [37]. According to one theory, an interface state is created by the release of hydrogen saturating an open Si bond at the substrate oxide interface. The remaining *dangling bond* is an electrically active defect with an energy distribution throughout the *Si* bandgap. It can be occupied by an electron or hole, but for pMOS in inversion mode it is positively charged [38]. The electric field induces a diffusion of the remaining hydrogen through the insulator. As this interface state generation process was believed to be the dominant NBTI contributor, the widely-used RD (Reaction Diffusion) model was developed for NBTI prediction [39]. More recently, oxide

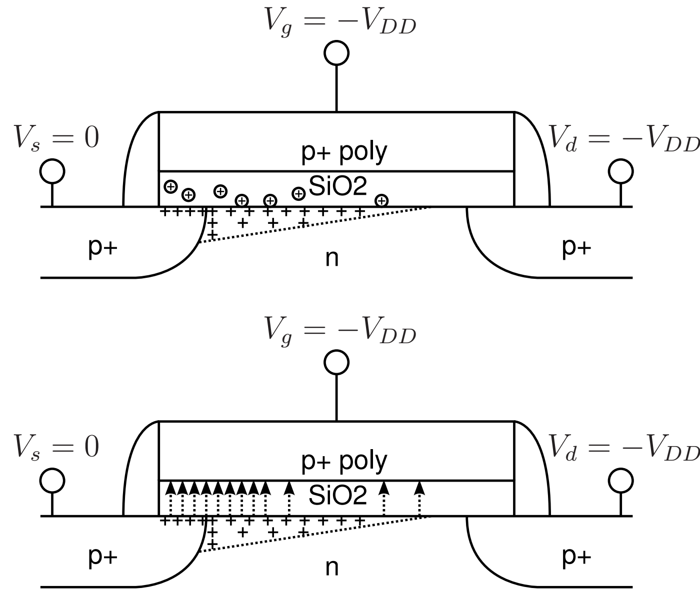

Fig. 3.4: pMOS in saturation operation: NBTI stress generated defects and arising electric field under NBTI stress

charges were believed to be dominant to NBTI. These traps are neutral when discharged and are positively charged when occupied by holes. Former modeling explained positive oxide charge is due to trapping of H^+ from the RD process, but recent findings revealed that hole traps and their precursors already exist in the oxide before stress is applied [40].

NBTI *recovery* was controversially discussed for long times, but its investigations revealed a deeper understanding of NBTI degradation mechanisms. As recovery immediately sets in when stress is removed, the time delay between stress and aging monitor measurement is very important. This undefined delay in published NBTI data is also one origin of the lack in NBTI understanding. In recent years a lot of effort was performed measuring degradation during stress to find the whole amount of contributing effects [41, 42, 43, 44]. Early understandings divided NBTI characteristic into two components, a *recovering* one and a *permanent* part. Controversial results assigned effect recovery to passivation of interface traps [45] or hole detrapping [42]. Also investigations for enhanced recovery under accumulation mode did not reveal a distinct recovery origin [46, 47]. Reisinger's ultra-fast V_{th} measurement method to monitor recovery after stress, revealed for small dimension devices a stepwise recovery curve indicating the discharge of single defects with differing contributions in step size, which can be related to the random position of channel dopants and insulator defects. In a large area device this single defect recovery is masked by the huge number of defects and the small impact of each defect recovery to the overall device V_{th}, leading to the classic log(t) NBTI recovery behavior, which is incompatible with the RD model [48]. Defect relaxation behavior was related to the model of *low frequency noise/flicker noise* or its manifestation as RTN (Random Telegraph Noise) and extended to the BTI timing range with individual capture and emission times for each defect [49, 50, 48]. With the adapted RTN characterisation technique TDDS (Time Dependend Defect Spectrocopy) from Grasser, it was shown that general BTI is

due to a thermally activated capture and emission of holes and electrons in oxide traps - called SOT (Switching Oxide Traps) [40, 51]. Capture and emission time constants are vastly distributed from nanoseconds to months or even longer. Investigations revealed that metastable states of these defects contribute an additional noise portion and scaling to nanometer devices can lead to very large induced variations due to high defect step sizes of a very small number of defects per device.
Changing the insulator materials from SiO_2 to $SiON$ or high-κ stacks also changes the NBTI degradation. For $SiON$ devices nitrogen portions should be located rather to the Gate/insulator than to the substrate/insulator interface for improved NBTI degradation [38]. High-k based gate stacks also show similar NBTI degradations compared to SiO_2 and $SiON$ data [52]. Fernandez showed that NBTI is strongly DF (Duty Factor) dependent, but shows a flat AC degradation behavior up to the GHz range [53], which is in line with SOT model from Grasser. From recent findings, Kaczer proposes to migrate to SiGe buried channel pMOSFETs to guarantee limited NBTI/pMOS degradation in future CMOS technology nodes [37].

3.3.2 PBTI in nMOSFETs

Corresponding to pMOSFET's NBTI, a PBTI arise in nMOSFETs in inversion operation. PBTI degradation was negligibly small in SiO_2 and $SiON$ technologies, but arises with similar orders of magnitudes in high-k technologies. Fig. 3.5 shows the inversion

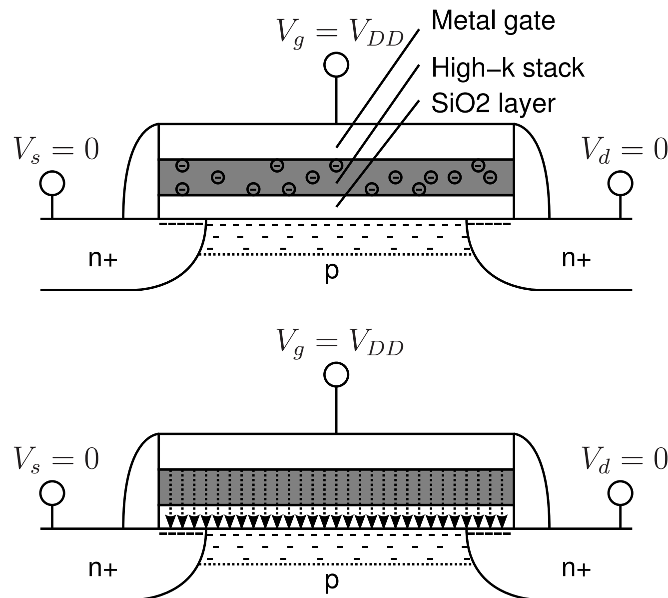

Fig. 3.5: High-κ nMOS in triode operation: PBTI stress generated defects and arising electric field under PBTI stress

mode stress condition and its degraded insulator in deep triode region for an exemplary high-κ nMOS. Contrary to classic pMOS/NBTI, oxide degradation occurs in the high-κ portion of the Gate stack [36]. Due to intermediate SiO_2 layers at the substrate insulator interface, nMOS/PBTI degradation is located in a certain distance from the inversion

channel, thus mainly impacting threshold voltage V_{th} with almost no effect on channel mobility μ_0 [54]. Similarly to NBTI/pMOS degradation, also PBTI/nMOS shows a concentrated degradation near the Source in saturation operation resulting in a reduced total degradation compared to the deep triode region operation (see fig. 3.6).
As nMOS/PBTI in high-κ processes compared to pMOS/NBTI is a very new type of

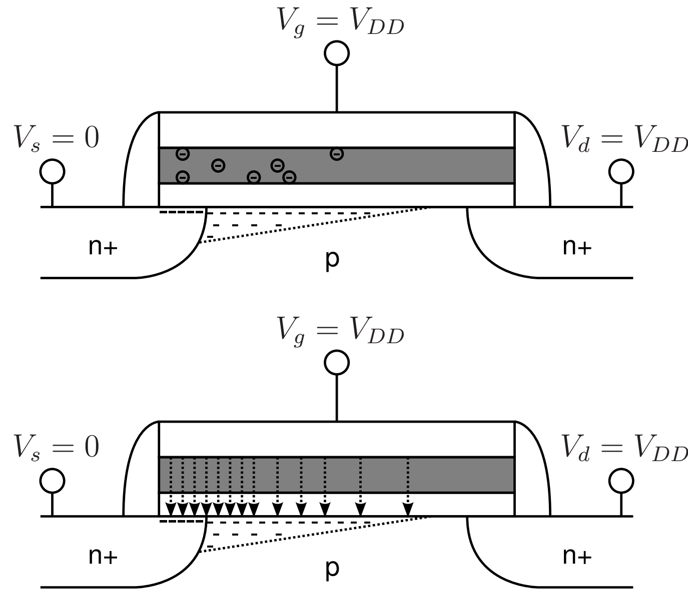

Fig. 3.6: High-κ nMOS in saturation operation: PBTI stress generated defects and arising electric field under PBTI stress

degradation mechanism and due to the controversial discussion and explanation for the classic pMOS/NBTI, most BTI related investigations concentrate on a deeper understanding of pMOS/NBTI. Nevertheless, there is a general consensus that nMOS/PBTI degradation is due to charge trapping in the high-κ or related capping layers [55, 56, 57, 36]. High-κ CMOS processing - especially the gate stack with its specific arrangement of interface and capping layers - is a very confidential matter of semiconductor companies. Due to specific processing, differing nMOS/PBTI degradation results are available. Some investigations report a PBTI *turnover* phenomenon - an enhancement or weakening of the nMOS characteristic as a function on time depending on the bias and temperature stress condition. This observation indicates a multiple polarity defect trapping [58, 59]. Recent results for HfO_2 based high-κ processes linked the major parts of PBTI degradation to electron trapping at oxygen vacancies [37]. Early investigations on nMOS/PBTI tried to model PBTI degradation with an adapted RD explanation from NBTI modeling, but neglected PBTI relaxation phenomena [58]. nMOS/PBTI relaxation is similar to pMOS/NBTI behavior, showing defect relaxation in a vast timescale from sub-microseconds to months. The promising SOT approach also fits well for PBTI degradation, its relaxation behavior and AC voltage stress degradation dependency [40, 55].
A possible option to reduce nMOS/PBTI degradation in HfO_2 based processes is the inclusion of group III elements to passivate oxygen vacancies [60].

3.3.3 PBTI/pMOS and NBTI/nMOS

The *accumulation* mode is very uncommon for CMOS devices, as this operation does not exhibit a Gate controlled current flow from the Drain to the Source node and requires a reverse sign of the Gate to substrate voltage. In classic CMOS digital logic, accumulation mode does not appear, but can arise in analog circuits. Due to its rarity, accumulation mode aging is rated as a minor reliability issue by the device reliability community and only small numbers of investigations exist.
Fig. 3.7 and fig. 3.8 depict exemplary SD MOSFETs in accumulation operation. Negative

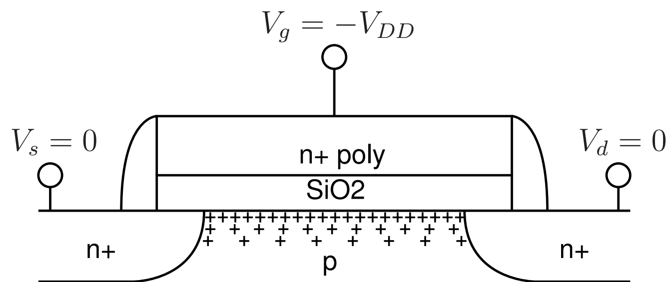

Fig. 3.7: nMOS in accumulation NBTI stress mode

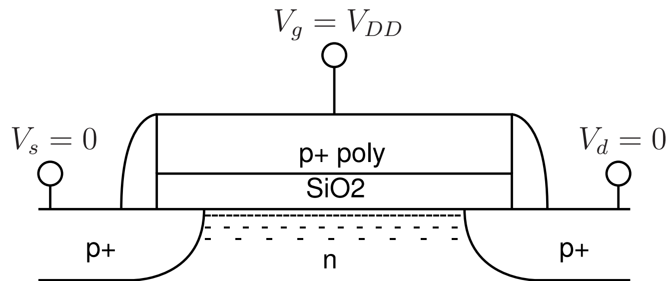

Fig. 3.8: pMOS in accumulation PBTI stress mode

Gate voltage for the nMOS and positive voltage for the pMOS induce an electric field over the oxide and majority carriers form an accumulation layer under the Gate. As shown in [42] and [61], also accumulation mode causes device degradation. A detailed investigation on NBTI aging results for equal negative voltage bias on nMOS and pMOS devices is given in [38]. Proposed explanations for the differing degradation magnitudes are related to different surface potentials and its dependence on interface traps charge, differing hydrogen diffusion or the different work functions for pMOS and nMOS. Accumulation mode is still used in BTI relaxation measurements to accelerate defect recovery and separate between distinct defects [62]. Nevertheless, involved microscopic mechanisms and detailed impacts on device characteristic are poorly understood.

3.4 Hot-Carrier Injection (HCI)

Hot-Carrier degradation affects both transistor types, nMOSFETs and pMOSFETs. It is the corresponding degradation effect to BTI where a high vertical electric field induces insulator wearout. For HCI it is the lateral electric field causing the degradation, so it arises for high Drain-Source voltages V_{DS} in combination with short Gate lengths L. In contrast to BTI degradation, HCI induces an asymmetric insulator wearout concentrated in the Drain region and thus makes degradation modeling more challenging. The name *hot-carrier* is historically grown. It describes the acceleration of carriers under an electric field gaining kinetic energy higher than the lattice in thermal equilibrium: these carriers are called *hot*. Hot carriers exhibit enough energy to induce *impact ionisation*, generation of *interface states* or even surmount the insulator barrier and generate *oxide defects* or get *trapped* [63]. Injection rates are typically measured via substrate current I_B, induced by impact ionisation, or Gate current I_G. Only a small part of the hot carriers get trapped and contribute to the intrinsic HCI degradation. A sufficient high lateral electric field for hot carrier generation emerges in MOSFET saturation region between channel pinch-off and drain junction. Hot carrier degradation in this operation is called CHCI (Conductive Hot-Carrier Injection). The CHCI generation condition is given in fig. 3.9 for an exemplary nMOS device. The degradation generating lateral electric field is generally related to the device channel length L_{eff} and the voltage difference between the drain node and the pinch-off point. Voltage stress conditions are more complicated for HCI than for the BTI effects as the lateral field depends on both, the Drain-Source voltage V_{DS} and the channel controlling Gate-Source voltage V_{GS}, defining the pinch-off point with $V_{DSAT} = V_{GS} - V_{th}$ [32]. Furthermore, V_{GS} to V_{DS} relations control directions of the oxide field in the drain region and so the polarity of defect trapping. CHCI degradation can generate different polarities of charge at the same time. The measured total degradation is defined by the dominant effect or the resulting combination of all generated defects.

Hot-Carrier degradation became a major reliability issue for nMOS devices in the late

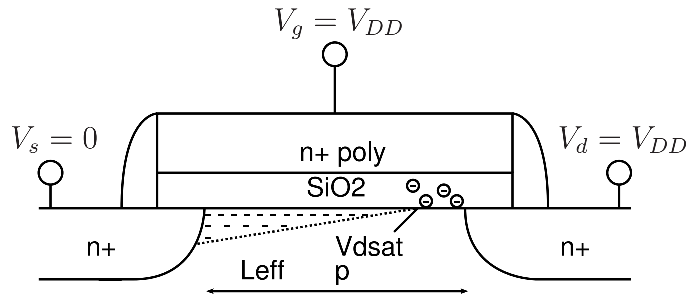

Fig. 3.9: nMOS in saturation inducing CHCI degradation

1970s and a lot of research was conducted in the 1980s. In these days the commonly used LEM (Lucky Electron Model) was developed, which is still used in lots of reliability simulation tools [64]. It provides the correct prediction of CHCI degradation down to the $0.25\mu m$ range. With further scaling the LEM reaches its limitations and is no longer valid to describe measured hot carrier degradations. For example, for $V_{DS} < 1.3V$, LEM does not predict impact ionization or hot carrier damage anymore, although both are

proven by measurements. To describe hot carrier behavior for the nanoscale regime, the EDM (Energy Driven Model) was proposed, including further acceleration effects like electron-electron scattering [65]. For extremely short channel lengths of a few 10nm a NCHCI emerges between Source and Drain junction even for switched-off devices caused by hot-carriers in the sub-threshold current (see fig. 3.10).
HCI counteractive process developments - generally known as *drain engineering* - reduce

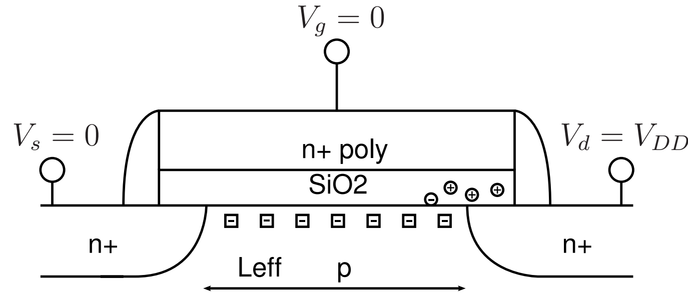

Fig. 3.10: nMOS in off-state inducing NCHCI degradation

electric fields in the Drain region and result in well controlled CHCI degradations. The commonly used LDD (Lightly Doped Drain) technique (see fig. 3.11) reduces peaks in the lateral electric field via inclusion of low doped n- regions at the Drain and Source junction, but at the expense of higher Drain-/Source resistance [66].
One challenging part of hot carrier stress characterisation is the simultaneous generation of BTI induced degradation - especially at high temperatures - and their further separation. Shifts of peak CHCI degradations to high V_{GS} aggravates BTI contributions, making hot carrier characterisation more challenging. Similar to BTI measurements, effect recovery was also observed in CHCI investigations, but is mostly related to BTI included components [67, 68].

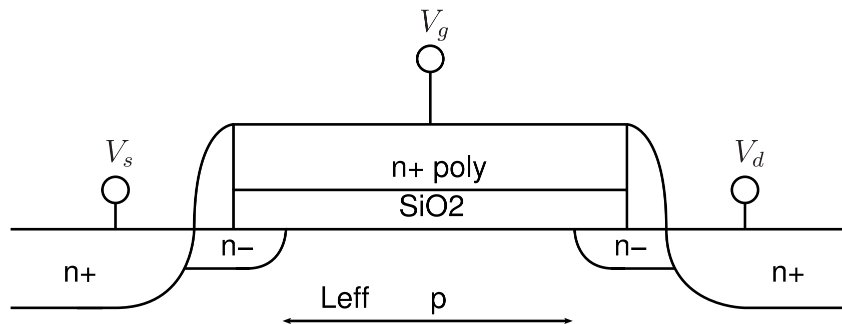

Fig. 3.11: Cross-section of an exemplary LDD nMOSFET

3.4.1 Conductive Hot-Carrier Injection in nMOSFETs

CHCI degradation for SiO_2 nMOSFETs can be separated in three regimes depending on the gate bias V_{GS} and the resulting oxide field condition in the Drain region - V_{DS} is

expected to be high. In all regimes hot carriers generate interface states with a peak at $V_{GS} = \frac{1}{2}V_{DS}$. Their impact on device characteristic interfere with the other parameter shifting mechanisms. For low $V_{GS} \approx V_{th}$ the oxide field in the Drain region assists hole trapping as can be seen in fig. 3.12. In the mid-range $V_{th} < V_{GS} < V_{DS}$ hole and electron

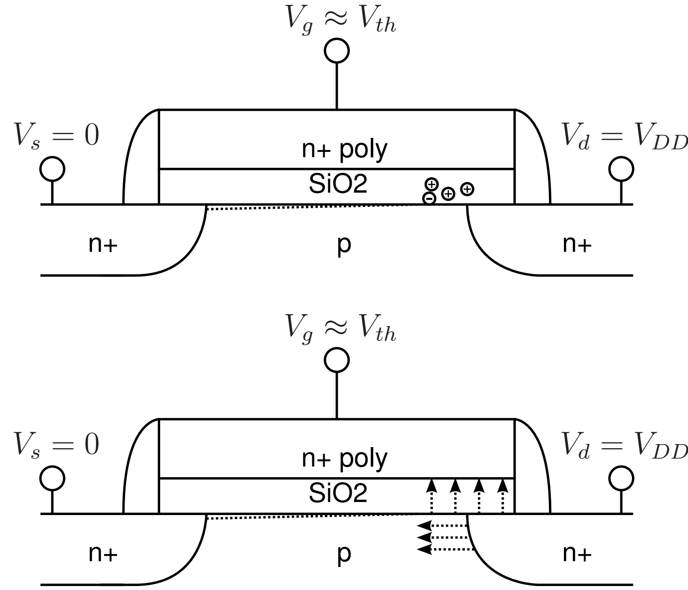

Fig. 3.12: nMOSFET CHCI with $V_{GS} \approx V_{th}$ and $V_{DS} = V_{DD}$

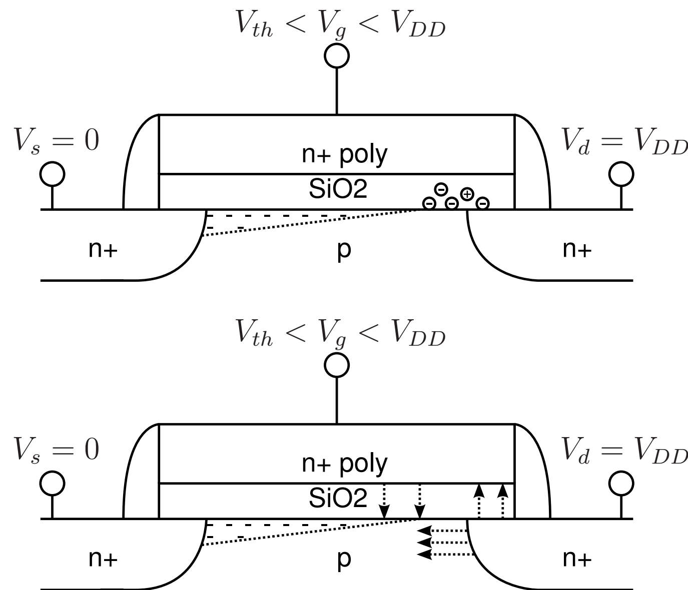

Fig. 3.13: nMOSFET CHCI with $V_{th} < V_{GS} < V_{DS}$ and $V_{DS} = V_{DD}$

injection interfere and partially compensate (see fig. 3.13). For high $V_{GS} \approx V_{DS}$ electron injection forms the major part (see fig. 3.14). For recent technologies the role of the charge injection drops and interface state generation becomes the dominant mechanism [63]. Furthermore, scaling shifts the interface state generation peak to $V_{GS} = V_{DS}$ due to

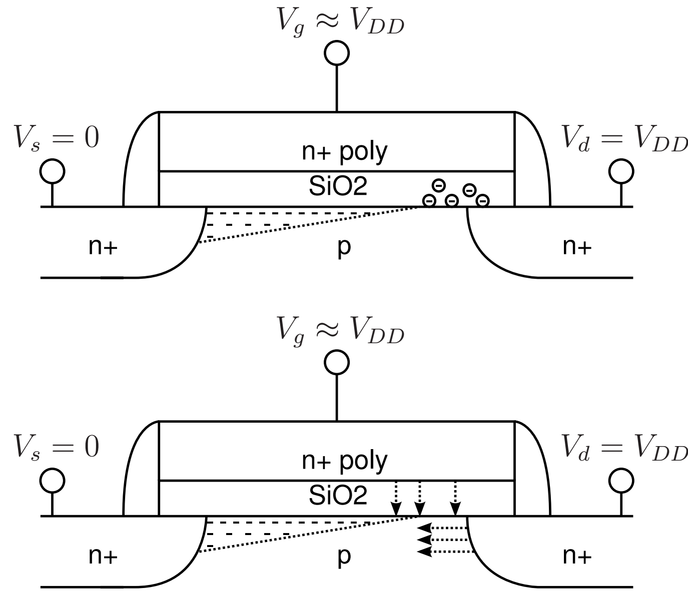

Fig. 3.14: nMOSFET CHCI with $V_{GS} = V_{DS}$ and $V_{DS} = V_{DD}$

energy related 'short channel' effects, like increased electron-electron scattering [69]. Changeover to high-κ gate materials does not change the intrinsic nMOS/CHCI behavior, but due to peak value shifts to the high V_{GS} range additional PBTI components arise, that have to be separated from the intrinsic CHCI effect [70].

3.4.2 Conductive Hot-Carrier Injection in pMOSFETs

CHCI situation for classic SiO_2 pMOSFETs is very similar to the nMOS degradation, but with differing mechanism contributions. As electric fields are only inverse to the nMOS, a schematic visualisation is omitted. For pMOS major CHCI contributions are related to generated interface states peaking at $V_{DS} = V_{GS}$. For high V_{DS} and $V_{GS} \approx V_{th}$, electron trapping is induced in the Drain region by filling of pre-existing defects in the oxide. For recent technologies this is more and more reduced as thin oxides are less sensitive for electron trapping. In the region $V_{GS} < V_{th}$, hot holes become the dominant mechanism inducing hole trapping in the oxide and the generation of interface states [63].
Device scaling further emerges a secondary effect that gets dominant for DC stress conditions. The so-called LSHA (Local Self-Heating Activated) NBTI is an local enhanced NBTI degradation due to self-heating at the Drain side under CHCI stress conditions [71, 72]. A distinct model for the LSHA effect does not exist until today due to the lack of understanding of the involved self-heating time constants.
Early investigation on pMOS/CHCI for high-κ technologies showed an increased device degradation, but with similar V_{GS} and V_{DS} behavior compared to ultra-short SiO_2 counterparts. Larger degradation is related to the lower quality of the interfacial oxide layer [68] and should be improved during further process development.

3.4.3 Non-Conductive Hot-Carrier Injection in nMOSFETs and pMOSFETs

NCHCI or *off-state* degradation occurs for a switched-off MOSFET, that means $0 \leq |V_{GS}| < |V_{th}|$ and high $|V_{DS}|$. The NCHCI scales with the gate length and arise as a significant reliability issue in nanoscale technologies [73]. Surprisingly, there exists only a small number of published investigations on this emerging topic. The source of the observed degradation is the gate length dependent channel leakage current. Drain diode leakage current has proven to have minor impacts [74]. For both device types oxide degradation occurs in the drain region [74, 75]. In [76], Muehlhoff reported for nMOS devices hole trapping in the middle of the channel and electron trapping near the Drain, dependent on the oxide thickness. For thin oxides the hole trapping mechanism disappears. In contrast, Hofmann reports interface state generation and electron trapping resulting in a negative charge buildup [75]. But also for pMOS transistors under off-state stress electron trapping is reported leading to a current increase [74].
The NCHCI investigations and their differing results show the typical aging effect individuality of measured device degradations. Their involved mechanisms and contributions are strongly related to the investigated CMOS process technology and result in individual aging behavior. So, a very general assignment of device wearout to an inducing mechanism can not be performed and has to be investigated for each CMOS process individually.

3.5 Aging Effect Modeling

Aging effect modeling can be divided into two fields: the aging effect degradation *prediction* and the subsequent *integration* for circuit simulators. Aging prediction models try to map aging physics in more or less complex model equations depending on the aging stress parameters voltage V or current I, temperature T and time t as well as further technology or design related parameters like equivalent oxide thickness t_{ox} or device dimensions W and L.
For circuit level reliability simulations, the evaluated parameter shifts have to be integrated into classic circuit simulator netlist descriptions. The two common state-of-the-art approaches are depicted in fig. 3.15. For the first one, evaluated degradation for each device in the circuit is mapped in an individually adapted model card. The second approach bases on the usage of an individual sub-circuit to reproduce degraded device characteristic via the two additional sources mapping a ΔV_{th} and a ΔI_D. The inserted $R_{sense} = 0\Omega$ resistor is used to sense the Drain current to control the feedback current source. The sub-circuit approach is limited to a general shift on the x-axes (ΔV_{th}) and an adaption of the current slope (ΔI_D) of the transistor characteristic. Compared to the model card adaption approach, a sub-circuit model provides less degrees of modeling freedom in terms of the number of affected MOSFET parameters. On the other hand it provides a more simple and comprehensible way of simulation level inclusion for the circuit designer. The given implementations in fig. 3.15 only support permanent degradations. Contrary to the

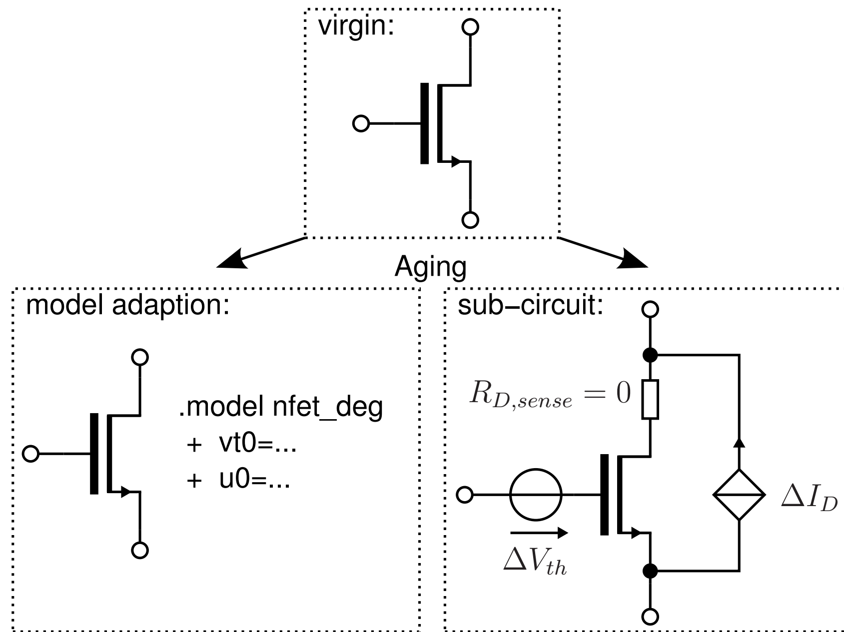

Fig. 3.15: Device aging modeling approaches for circuit simulation: device model card adaption or sub-circuit model.

sub-circuit model, the model card adaption approach is strictly limited to permanent drifts, whereas the sub-circuit can be easily extended to support for both permanent as well as transient recovering parts of degradation effects. Especially for the BTI effects (see sec. 3.3.1 and 3.3.2), those recovering contributions can form major parts of the overall parameter drifts. For advanced effect modeling, recovery has to be considered in the circuit level models, which is only supported by an adapted sub-circuit approach.
Another challenging topic in circuit level modeling is the consideration of locally confined degradations, as generated by HCI aging. Fig. 3.16 sketches for an exemplary nMOS, CHCI impact on the output characteristic (I_D/V_{DS}) in dependence of the current bias direction. For the forward case, stress and characterisation were biased in the same direction. For the reverse biasing, Drain and Source nodes were swapped. CHCI degradation in forward biasing degrades Drain current and the slope of the output characteristic, acting as another increase of channel length modulation factor λ. In reverse bias, the same CHCI generated charge impacts the fully inverted channel leading to the classic V_{th} or I_D shift. As shown in this example, a throughout correct circuit level aging modeling can arise as a challenging task. In the majority of cases, circuit level models are kept simple due to complexity reasons.
In general, circuit reliability simulations may end up in large and overloaded simulation runset files, as for each incorporated device an individual model card or sub-circuit model has to be included into the simulation netlist. For AgeMOS™ compatible models, degradation is an integral part of the model card and can be considered by providing corresponding aging parameters, solving the problem of replacing thousands of transistors by individual degraded model cards or sub-circuit models [77]. Nevertheless, recovery effects are still neglected by this approach.

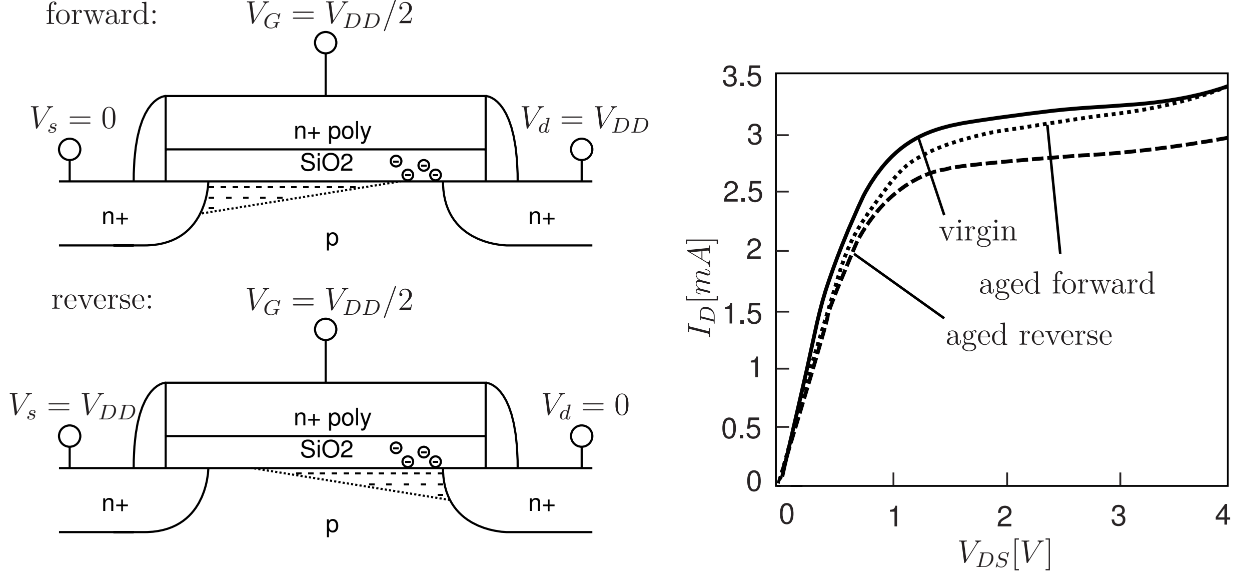

Fig. 3.16: Exemplary CHCI/nMOS degradation measurements and its impact on forward or reverse nMOS operation [63].

3.5.1 Semi-Empirical Models

The most simple way for aging prediction are the *semi-empirical* aging models, that are typically provided by the technology related DM (Design Manual). A very general version of this model type is also given in the JEDEC standard [3]. Semi-empirical models are widely used in circuit reliability investigations, especially if diverse aging effects in the circuit are considered [10, 23, 22, 14]. These models base on general effect related physical assumptions, and are further fitted to stress measurement data.
The semi-empirical BTI model predicts degradation as a drift in threshold voltage ΔV_{th}, that is directly related to the generated charge in the MOSFET insulator (eq. (3.3)). The BTI induced drift is given by eq. (3.6)

$$\Delta V_{th} = A \cdot (\frac{V_{GS}}{t_{ox}})^m \cdot e^{(\frac{\Delta E}{kT})} \cdot L^\alpha \cdot W^\beta \cdot t^n, \tag{3.6}$$

with the common known stress parameters: V_{GS} the Gate-Source voltage, T the temperature and t the stress time. ΔE represents the thermal activation energy and k the Boltzmann constant, exhibiting an Arrhenius type temperature behavior. The factor A is a process related prefactor. Exponent m denotes the power law sensitivity towards arising oxide electric fields given by $(\frac{V_{GS}}{t_{ox}})$, with t_{ox} the oxide thickness. m is process dependent and has to be adjusted to the CMOS process. It is typically in the rage of $2 < m < 10$ for current CMOS technologies. In the past, V_{GS} sensitivity was also often modeled with an exponential behavior [78, 23]. BTI effects prove to be inherently dimension independent, as in its worst case scenario in deep triode region, BTI degradation occurs equally distributed over the insulator area. Factor $(L^\alpha \cdot W^\beta)$, with L the gate length and W the width, represents a correction for minimum size devices to consider for boundary effects. Exponents α and β are typically much smaller than 1. The time exponent n is typically in the range of 0.15-0.3, inducing the sub-linear or saturating degradation behavior for

linear time scales [42, 23, 22]. This time exponent n is of special interest, as it major impacts the degradation end-of-lifetime extrapolation quality [79]. The model equation in (3.6) is valid for NBTI/pMOS as well as for PBTI/nMOS in high-κ technologies each with its individual parameter set.
Equation (3.6) only allows aging evaluation of one single stress condition (V, T, t). A change of one of the stress parameters during evaluation is not supported. To account for realistic stress with time varying stress conditions arising in circuit operation, an auxiliary variable AGE has to be defined:

$$\begin{aligned} AGE_{BTI} &= \sqrt[n]{\Delta V_{th}} \\ &= \sqrt[n]{A \cdot (\frac{V_{GS}}{t_{ox}})^m \cdot e^{(\frac{\Delta E}{kT})} \cdot L^{\alpha} \cdot W^{\beta} \cdot t}. \end{aligned} \tag{3.7}$$

AGE_{BTI} implies a linear behavior in time and supports the consideration of individual stress periods by adding up $AGE_{BTI,i}$ values and calculate via eq. (3.7) the total threshold voltage drift.

$$AGE_{BTI,total} = AGE_{BTI,1}(V_1, T_1, t_1) + AGE_{BTI,2}(V_2, T_2, t_2) + \dots \tag{3.8}$$

$$\Delta V_{th,total} = (AGE_{BTI,total})^n \tag{3.9}$$

According to this general concept, circuit reliability simulators like RelXpert™predict device degradation under transient voltage stress [77]. Also here, the accurate derivation of the time exponent n is of major importance to correctly predict device aging.
A similar model equation for HCI aging prediction is given by

$$D_{HCI} = B \cdot V_{DS}^p \cdot e^{(\frac{\Delta H}{kT})} \cdot L^{\delta} \cdot t^q. \tag{3.10}$$

Also for HCI, classic stress parameters, V_{DS} as the Drain-Source stress voltage, T the temperature and t the stress time mainly determine degradation. Temperature behavior is modeled as Arrhenius law with ΔH the activation energy and k the Boltzmann constant. B is the process related prefactor. Exponent p denotes voltage sensitivity and is also process related. Gate length dependency is given by L^{δ}, with $\delta \approx [-4; -2]$. The time exponent q is larger than for BTI and is in the range of 0.2-0.5 [22]. Depending on the model implementation HCI aging is considered as a drift in Drain current

$$\frac{\Delta I_D}{I_D} = D_{HCI} \tag{3.11}$$

or as

$$\frac{\Delta I_D}{I_D} = x \cdot D_{HCI} \quad \text{and} \quad \Delta V_{th} = y \cdot D_{HCI}. \tag{3.12}$$

with $0 < x < 1$ and $0 < y < 1$, separating HCI degradation into the $\frac{\Delta I_D}{I_D}$ and the ΔV_{th} contributions. This general HCI model is used for CHCI and NCHCI in nMOS and pMOS transistors, each with an individual parameter set.
To consider for time varying voltage stress, a corresponding $AGE_{HCI} = \sqrt[q]{D_{HCI}}$, similar

to eq. (3.7) can be defined to support aging integration ability over time.

Circuit level inclusion is typically performed with a sub-circuit model, as BTI and HCI models output ΔV_{th} or $\frac{\Delta I_D}{I_D}$ - the two parameters of the sub-circuit model. Thereby, BTI and HCI degradation are modeled as independent effects, so both aging contributions should be added and combined in the circuit level model.
Semi-empirical models suffer from a few drawbacks that mainly affects the modeling accuracy. Equations (3.6) and (3.10) only consider a 1-dimensional stress voltage dependency - for BTI degradation a V_{GS} and for HCI a V_{DS} dependency. As discussed in sec. 3.3, BTI degradation is mainly driven by the vertical electric field, thus by V_{GS}. But the lateral field, given by V_{DS}, determines device operation region and electric field distribution over the channel. For this reason, V_{DS} also impacts total BTI degradation. A corresponding V_{GS} dependency for HCI effects as discussed in sec. 3.4 is also omitted for the HCI model equation. The general aim of the semi-empirical models is to cover degradation for worst case aging conditions. Another point is the disregard of recovering phenomena, especially for BTI effects. Evaluated degradation is predicted in a fixed, permanent magnitude without indication of ongoing relaxation behavior. Furthermore, the considered recovery state during the model extraction measurement, thus the delay between stress and characterisation measurement is not defined nor denoted. In the end, semi empiric models are limited to two degradation variables ΔV_{th} and $\frac{\Delta I_D}{I_D}$, further reducing modeling quality.
The big plus of the semi-empirical models are their simplicity and dependency of easy accessible stress parameters on circuit level. They prove to be very useful for circuit level inclusion or, as will be shown later, to develop general circuit aging behavioral models. They also provide the possibility to determine effect acceleration according to the stress conditions (V,T,t).

3.5.2 Complex Models

More sophisticated degradation prediction models are incorporated into automatized reliability tools like Cadence RelXpert™ [77] or Synopsys HSIM^{plus} MOSRA™ [80, 81]. Both tools further support the historically grown 'lifetime' approach. Basing on an individual circuit related aging limit, e.g. 10% I_D degradation, the reliability simulator predicts the 'lifetime' of aging effects in each device when this degradation limit will be reached for the given voltage and temperature stress conditions. 'Lifetime' prediction can be considered as a parent approach to parameter drift inclusion into an aged netlist.
Advanced BTI aging prediction models are very similar to the semi-empirical model equation in sec. 3.5.1. Further enhancements consider an additional V_{DS} dependency on the overall BTI degradation.
Particularly for HCI prediction, advanced models, basing on the LEM [64] approach, are incorporated into reliability simulators. LEM models forecast degradation from a certain rate of substrate or gate current. HCI aging for nMOS devices is predicted via

$$D_{HCI,nMOS} = \left(\frac{I_{DS}}{H \cdot W} \left(\frac{I_{SUB}}{I_{DS}} \right)^m \cdot t \right)^n , \tag{3.13}$$

with I_{DS} the Drain-Source current of the device, W the gate width and t the stress time. H is a process related constant. Exponents m and n denotes the acceleration factor and the reaction rate. I_{SUB} monitors the impact ionization rate and is related to the lateral electric field, thus depends on bias conditions V_{GS} and V_{DS} as well as device channel length. I_{SUB} is derived according to the relations given in [82]. For pMOS devices an additional Gate current component is used for aging prediction, as I_G proves to be a more suitable HCI monitor [82],

$$D_{HCI,pMOS} = \left(X \cdot \frac{1}{H_G} \left(\frac{I_G}{W} \right)^{m_G} \cdot t + (1 - X) \frac{I_{DS}}{H \cdot W} \left(\frac{I_{SUB}}{I_{DS}} \right)^m \cdot t \right)^n \tag{3.14}$$

X denotes a weighting coefficient in the range of $[0; 1]$, H_G a process related constant and exponent m_G the acceleration factor. Gate current I_G is further related to I_{SUB}, bias conditions and oxide thickness. The overall derivation of I_G can be found in [82]. Further developments of these models incorporating approaches regarding HCI in nanoscale CMOS processes are given in [83, 84].
HCI aging for time varying stress voltage and current waveforms, that typically occur during circuit operation, can be similarly considered via the integrable AGE approach introduced in sec. 3.5.1.
As the use of complex HCI models demand for elaborate derivations of variables monitoring I_{SUB} and I_G, these model types are typically incorporated and limited to reliability simulator tools. The big plus to perform a more accurate aging prediction due to a elaborate stress bias modeling is clouded by the reduced insight for circuit's aging critical operation points. Here, semi-empirical models with their direct relation to basic design parameters provide a better understanding for design level countermeasures.

3.5.3 Relaxation Model

The introduced models in sec. 3.5.1 and 3.5.2 generally represent degradation as a permanent drift of MOSFET parameters. As already discussed in sec. 3.3.1 and 3.3.2, especially BTI effects exhibit a pronounced recovery behavior when stress conditions are removed, yielding to a transient variation of the induced parameter drifts.
The approach from Huard [10] divides NBTI/pMOS degradation in two independent components: one permanent part, that is related to the generation of interface states and fixed positive charge and a relaxing part due to charge trapping and detrapping. The investigation revealed, that each of these parts exhibit their own voltage and temperature dependency and two separate models for both contributors are derived. Indeed, this approach provides the opportunity to distinguish between two contributing parts, but does not provide information how to model the relaxation behavior in circuit level simulation. Another open point is how to segment NBTI effect recovery, coming along with vast time constants, into a recovering and permanent contributor.
Basing on the SOT approach [40] (see sec. 3.3.1), a general sub-circuit BTI degradation model, reproducing the trapping and detrapping of individual oxide defects was proposed by Kaczer and Reisinger [50, 48]. The implementation is similar to the charge trapping approach from Fulde [85], but covers larger time domains. As depicted in fig. 3.17, the

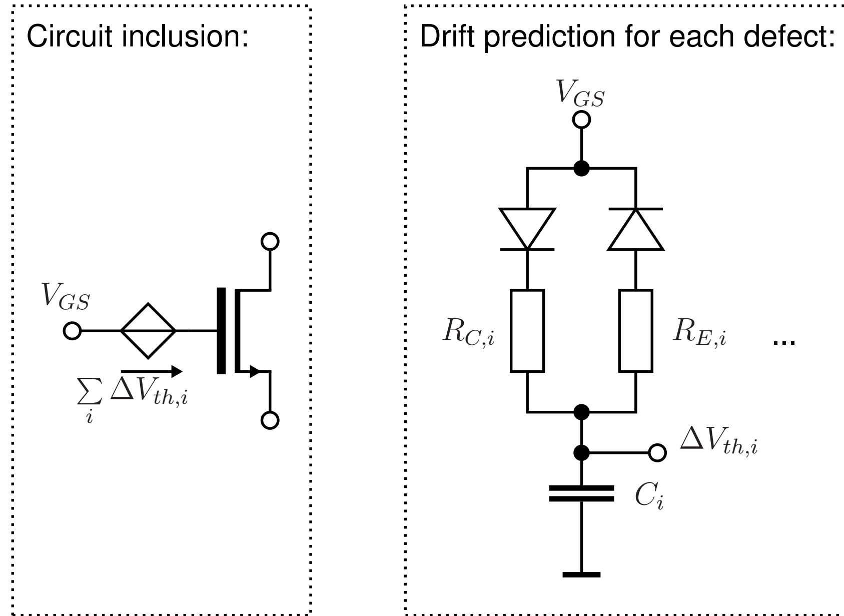

Fig. 3.17: SOT general BTI model considering loading and deloading of single oxide defects

sub-circuit reproduces via two distinct paths for loading and deloading with its individual time constants, the capture and emission of individual defects in the oxide in dependence of the given bias stress V_{GS}. Missing temperature activation is proposed to be modeled by a temperature related change in defects capture and emission paths by shifting the values $R_{C,i}$ and $R_{E,i}$. The probability of the defect charging state and its average contribution to the overall ΔV_{th} drift is given by the voltage condition $\Delta V_{th,i}$ at the capacitor. For large area devices, lots of defects have to be considered resulting in unreasonable number of defect models. Here, a clustering to limit the number of sub-circuit branches has been proven to provide adequate results. Comparisons of simulations and measurements revealed a very accurate aging prediction for AC stress conditions as well as classic effect relaxation after stress [48]. Regarding minimum size devices incorporating a denumerable number of defects each with individual drift contributions, this method provides a powerful ability to account for arising BTI effect statistics. Further developments of the SOT approach are given in [86, 87, 61]

The model combines aging prediction and circuit level inclusion in one approach and uses the circuit simulator to solve the trapping and detrapping behavior. Beside the accurate aging effect prediction, it suffers from an unreasonable increase in simulation complexity for circuits with large numbers of devices. Here, a preceding more general examination via semi-empiric or complex models to find the most dominant aging contributors would be suitable. In a subsequent step the relaxation model should be included for main contributors. This would result in a more efficient aging simulation. The main drawback of the relaxation model method results from the direct inclusion in the circuit simulation. As will be discussed in section 3.6, the missing end-of-lifetime extrapolation ability would end-up in unreasonable large simulation times to reach this aging point. Future implementations of this approach demand for an extrapolation ability to be able to simulate

circuits regarding all recovering effects for end-of-lifetime conditions.

3.6 Circuit Reliability Simulation

The consideration of device aging in SPICE based circuit simulators has to deal with the fact of widespread time domains of circuit simulation and device aging. Whereas transient circuit simulations typically cover timing periods of μs or ms with discrete timing step sizes in the sub-ns range, the classic device aging period is the whole circuit lifetime in the range of several years. Direct inclusion of device aging effect prediction into circuit simulations would result in out of scale simulation runtime and proves to be unfeasible for circuit designers.
A more sophisticated approach is the aging effect extrapolation basing on a representative circuit operation condition. Separate device aging prediction allows to create a circuit netlist to simulate performance in an 'aged' condition. This approach can be performed *manually* or by *automated* reliability tools like RelXpert™[77]. Fig. 3.18 depicts the general approach of the reliability simulator RelXpert™. Here, a representative circuit operation simulation is used to predict arising voltage and current stress on the incorporated devices. According to the simulated voltage/current waveforms, the given temperature and the corresponding age of the circuit, the reliability simulator predicts device aging and extrapolates to the given lifetime. In a second step, an 'aged' netlist, representing the degraded circuit, is output for further simulations on the degraded circuit. Major attention should be turned to the operation voltage/current simulation to cover typical 'use-case' or 'worst-case' operation scenarios.
For the manual approach, aging prediction and generation of the 'aged' netlist has to

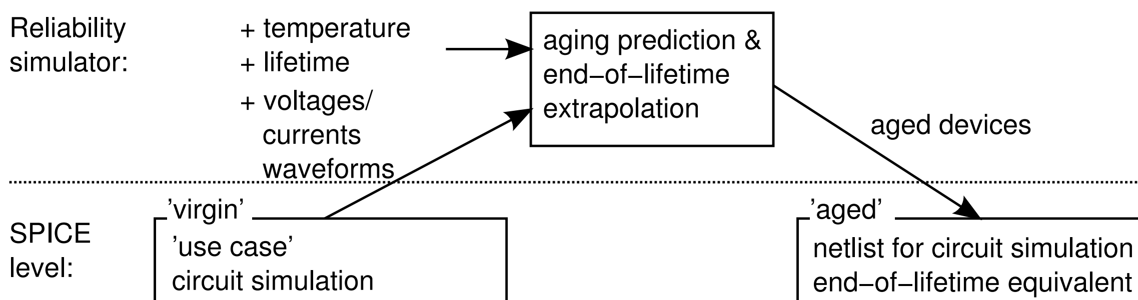

Fig. 3.18: Basic concept to embed device aging into spice circuit simulations

be performed individually for each device 'by hand'. This can be handled for circuits incorporating only few transistors, but gets time-consuming for circuits with more than 20 degrading devices. Furthermore, manual aging prediction models are limited to DC voltage/current operating states or pulsed stress waveforms, that can be predicted by the $\frac{t_{on}}{t_{on}+t_{off}}$ ratio - the so called Duty Cycle. Duty Cycle compatible waveforms typically arise in digital logic circuits, but are not sufficient to map the complex transient analog circuit operation. This limits the reasonable usage of the manual approach to DC operation for analog circuits.

The pro of automatized reliability tools is the ability to include reliability investigation in the common circuit design flow. This provides circuit designers a reliability proof of the circuit design without being an expert in device aging mechanisms. As these tools typically evaluate circuit aging in one distinct point in the aging parameter space (V,T,t), investigation regarding the circuit aging behavior in dependence of stress parameters are getting time-consuming. Here, a more sophisticated method would be an analytical approach using the semi-empirical models. Furthermore, semi-empirical models offer the possibility to derive stress conditions for accelerated degradation testing.

3.7 Reliability Testing

The major challenge of reliability testing consists in the practically unaccessible wearout or breakdown state far ahead in future, that is typically in the range of several years of operation. To fulfill proper process qualification in conjunction with short time-to-market constraints, reliability studies are typically run in a *stress* environment to *accelerate* wearout or breakdown effects in their temporal behavior. In the majority of cases an operation under elevated temperature or supply voltage or a combination of both stress parameters is used to accelerate the distinct effect. Stress tests are also employed to derive general physical behavior of degradation effects by running tests with varying stress parameters [1].
The common approach to accelerate a distinct mechanism in time is to find, e.g. for BTI degradation, a corresponding $V_{GS,stress}$ and T_{stress} according to the end-of-lifetime operation state with $V_{GS,EOL}$ and T_{EOL}, generating equal device wearout:

$$\Delta V_{th,stress}\left(V_{GS,stress}, T_{stress}, t_{stress}\right) = \Delta V_{th,EOL}\left(V_{GS,EOL}, T_{EOL}, t_{EOL}\right) \tag{3.15}$$

To fulfill (3.15), model equation (3.6) can be used to derive stress conditions for the accelerated test. A general definition for aging effect acceleration in time is defined by the AF (Acceleration Factor). Derivations of AF's for BTI and HCI degradation are given in [3]. For the exemplary BTI mechanisms, AF_{BTI} between a stress state and a user-defined operation UC (Use Case) can also be evaluated via eq. (3.6) and results in

$$\begin{aligned} AF_{BTI} &= \frac{t_{UC}}{t_{stress}} \\ &= \sqrt[n]{\left(\frac{V_{GS,stress}}{V_{GS,UC}}\right)^{m} \cdot e^{\left(\frac{\Delta E}{k}\left(\frac{1}{T_{stress}} - \frac{1}{T_{UC}}\right)\right)}}. \end{aligned} \tag{3.16}$$

It is obvious from eq. (3.16) that proper effect acceleration demands for a throughout physical understanding of the accelerated defect. An important characteristic of reliability testing, that has to kept in mind, is: the longer the stress durations, the smaller stress voltages and stress temperatures have to be chosen. Short stress times demand for high stress voltages and temperatures that further debut new defect mechanisms, overlying with the primary wearout mechanism and distort the degradation result. A general rule for proper stress testing can be quoted: the more time spending, the smaller the acceleration stress conditions and the better the accelerated test maps the end-of-lifetime use

case.
During stress testing some practical problems arise. Due to the strong sensitivity of wearout effects towards the stress parameters voltage and temperature, accurate temperature control and stress voltage sources are needed. Temperature sensors should be as close as possible to the degrading device. The best solution would be a on-chip temperature sensor. Especially the quasi-exponential stress voltage sensitivity demands for very accurate stress sources. To guarantee these exact voltage levels, most of the stress tests are run with DC stress voltages as parasitic effects from the test assembly can be minimized. For stress tests with AC stress voltages, an on-chip generation solution should be preferred to guarantee proper waveform magnitudes. But also stress durations have to be well defined for reproducible results. In general, reliability stress tests should always be run in fully automatized stress assemblies. Regarding effect recovery, that immediately sets in after stress removal, one has to keep in mind that only very fast measurement setups can approach the full spectrum of the effect relaxation. For slow measurement equipment, fixed delays between stress and measurements have to be defined and included into the stress programming. One can also consider relaxation annealing steps like off-state, high temperature annealing to decay most of the short time recovering effects. A lot of definitions how to perform stress tests on semiconductor devices and circuitry are summarized in [88] and [89].
The above concept for single mechanism aging acceleration via temperature and voltage rise is also often applied to circuit level stress testing. As will be seen in the following investigations, aging acceleration on circuit level is getting more challenging and demands for a closer look into the circuit's aging characteristic. Thereby, the mixture of several distinct aging mechanisms and the indirect stress voltage application plays an important role.

3.8 End-of-Lifetime Use Cases

Aging investigations in this work restrict to some application relevant EOL (End-of-Lifetime) use cases. Thereby operation conditions representing a typical use case or worst case scenario according to the intended application are assumed and circuit performance is evaluated in the corresponding end-of-lifetime state. For simplicity, only few use cases are used in this work, given in tab. 3.1. A good overview of commonly used ones for industrial applications are given in the JEDEC standard [89].

EOL Use Case	V	T	t
General	V_{DD}	25°C - 85°C	10y
MP (Mobile Phone)	$V_{DD,WC} + 5\%$	85°C	4y
Combined	$V_{DD,WC} + 5\%$	85°C	10y

Table 3.1: Application related aging use cases

3.9 Trend

A reason for the accomplishment of this work can be determined from the following evaluation of aging effects' evolution. Here, major degradation mechanisms and their behavior towards selected stress parameters are depicted and compared for the most recent CMOS technology nodes.
Fig. 3.19 depicts BTI aging behavior for the mobile phone end-of-lifetime use case and

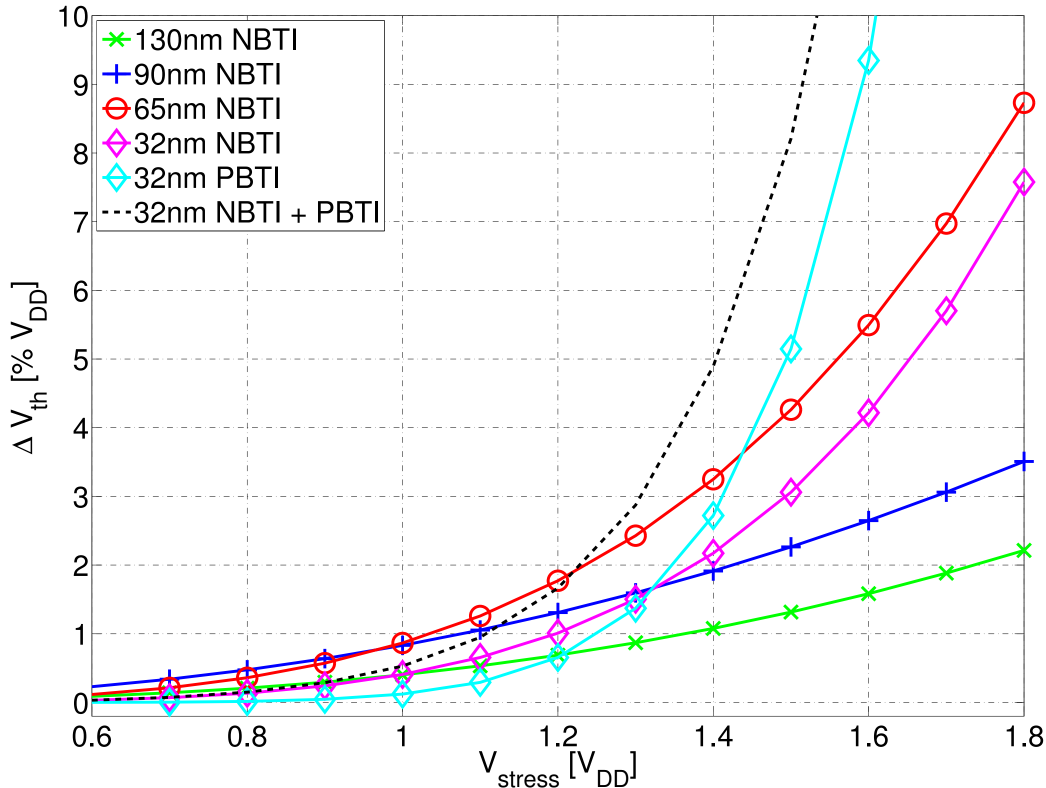

Fig. 3.19: BTI aging behavior for selected CMOS technology nodes for mobile phone end-of-lifetime conditions (see sec. 3.8).

in dependence of the stress voltage. For comparison reasons, stress voltages and ΔV_{th} degradations are given with respect to the corresponding supply voltage given in [2]. Especially for voltages much higher than nominal supply, the effect of the non-constant field scaling transistor design from 130nm CMOS down to 32nm appears in an increased voltage sensitivity: for each technology step, degradation values increase and the slopes of the curves are getting more steep. In the region of nominal supply, process optimization dominates and limits absolute drift values to certain margins. Nevertheless, the 32nm node bases on a high-κ, metal gate process and besides the classic NBTI in pMOS, an additional PBTI in the nMOS device occurs. In fact, in the allowed supply region, single NBTI and PBTI degradations for the 32nm process are smaller than the 65nm NBTI. But from the circuit point of view, NBTI and PBTI drifts have to be summed up as

pMOS and nMOS devices are typically stacked and both contribute to the proper circuit operation. Considering the combined degradation results for 32nm, as depicted in fig. 3.19, a clear trend towards increased impact of device degradation is obvious, especially the sensitivity towards slightly elevated supply voltages.

A similar view can be seen for the CHCI effects in fig. 3.20. Here, CHCI degradations

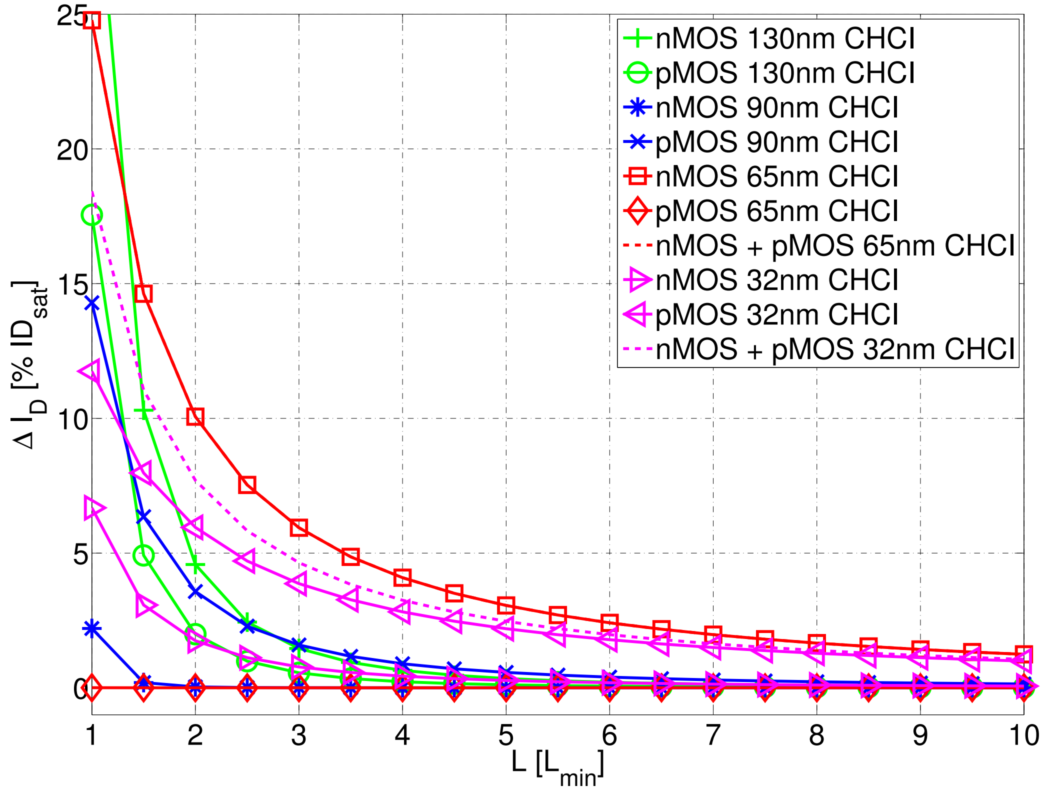

Fig. 3.20: CHCI aging behavior for selected CMOS technology nodes for mobile phone end-of-lifetime conditions (see sec. 3.8).

of both nMOS and pMOS devices for the mobile phone use case condition are illustrated in dependence of the channel gate length. For comparison reasons gate lengths are given in relation to the minimum gate length provided by the CMOS process and degradation values in % of device drain current. The strong gate length dependency reveals why CHCI played a minor role in analog circuits. Here, minimum gate length devices are seldom used, only for special purposes. This generally eliminates CHCI effects in their origin. Furthermore, CHCI effects also suffer from technology scaling inducing increased degradation magnitudes for advanced technology nodes. Whereas, CHCI degradation major impacts nMOS transistors for former CMOS processes, CHCI in pMOS devices plays a major role in the nanoscale regime with arising LSHA [71]. CHCI reduction ability due to gate length increase further downgrades with CMOS shrinking, as can be seen for the 65nm nMOS/CHCI and the 32nm pMOS/CHCI. Total CHCI degradation by summing-up nMOS and pMOS effects for 65nm and 32nm shows a general trend for

CHCI in future technologies towards higher degradation levels.
Aging behavior of the arising effect in the nanoscale regime during off-state is depicted

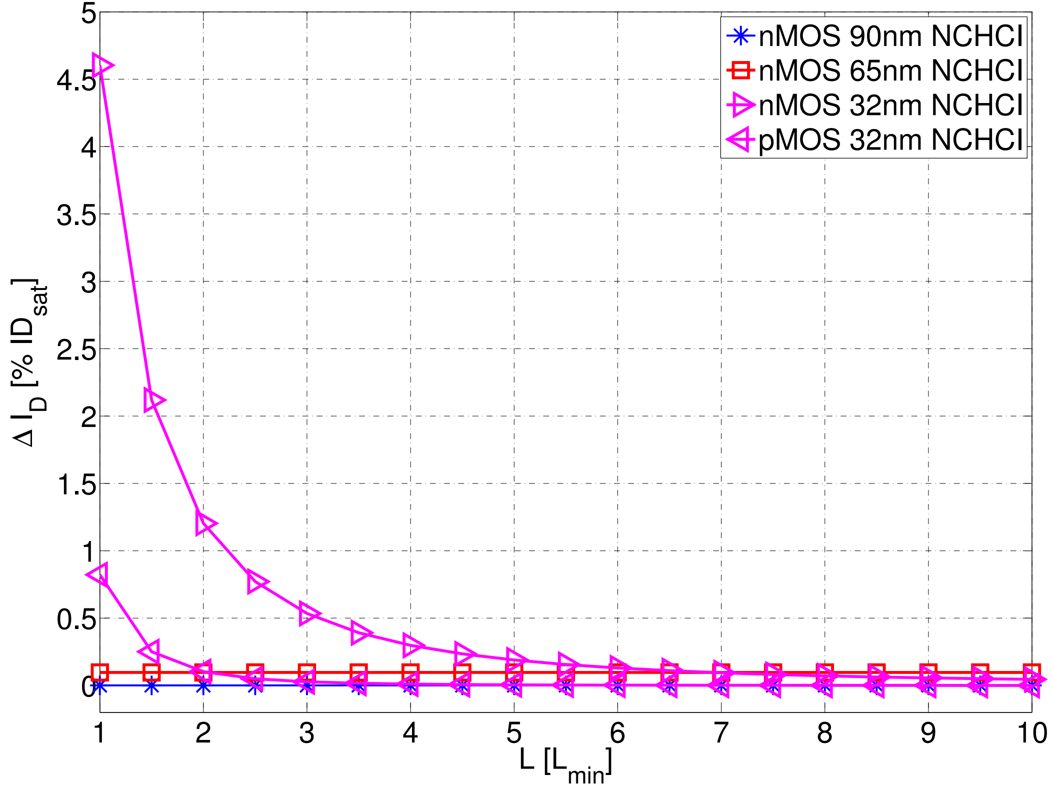

Fig. 3.21: NCHCI aging behavior for selected CMOS technology nodes for mobile phone end-of-lifetime conditions (see sec. 3.8).

in fig. 3.21. Also here, device degradation is evaluated for the mobile phone use case and, for comparison reasons, in dependence of the relative gate length. For the older technologies, NCHCI is modeled as a single worst case degradation value without any gate length dependency, contrary to the recent 32nm technology. Fig. 3.21 reveals a significant increase of the NCHCI degradation from the older CMOS technologies to the advanced 32nm. Furthermore, for the NCHCI in the 32nm process, major degradations occur in the nMOS device. An increase of gate length would drastically reduce NCHCI degradation.
In general, aging mechanisms are under control for allowed voltage region, but drastic increase of BTI aging comes closer and closer towards nominal supply. This demands for careful design, especially for overvoltage shoots. CHCI effects reduction ability due to gate length increase reduces for advance technologies. This will increase its impact also in the analog circuit regime using larger gate length devices. Nanoscale technologies show corresponding off-state NCHCI with dramatic increase, but here better suppression ability as given by using increased gate lengths.

3.10 Summary

This chapter discussed the scientific status quo in modeling and physical explanation of device degradation. Up to now, wearout effects are still not fully understood, which can be related to a strong dependency on the device processing and unspecific stress characterisation. Thus, effect modeling and the consideration for circuit reliability simulation lacks in accuracy. Acceleration approaches via high voltage and high temperature stress, known from single effect testing, is not directly transferable to circuit level due to the interaction of distinct wearout effects. The evaluation of aging effects in recent CMOS processes revealed a general trend: in fact, technology optimization limits wearout to certain margins in the allowed voltage headroom, but a strong increase for elevated supply voltages moves closer to the nominal supply. Furthermore, novel effects like off-state HCI drastically arise by entering nanoscale regime. For circuit designers, this trend demands for proper circuit dimensioning with respect to overvoltage shoots, but also an individual consideration of device wearout during the design phase. Of course, this further requires a correct and accurate effect modeling for circuit simulation integration.

Chapter 4

Device Aging in Circuit Operation

In chapter 3, wearout mechanisms were discussed by treating their physics, modeling, distinct testing approaches and their general evolution over the past CMOS technologies. This chapter starts from the circuit operation point of view with general design properties of typical *analog* and *digital* circuits and the arising stress conditions during their operation. Concentrating on the analog circuit operation conditions, device degradation and the change of transistor characteristic derived by common degradation models is evaluated. Important analog related issues that are still not considered by degradation models are revealed and investigated by stress measurements with a custom test circuit.

4.1 Digital and Analog Circuit Operation

Digital and analog circuits generally differ in their design and operation principle. Due to their general two stage stable operation states, digital circuits are inherently robust against lots of impacts, leading to a limited number of design constraints that are mainly area, speed and power consumption. Analog signal processing in the analog circuit regime demands compliance with a large number of further constraints like device matching, noise behavior or robustness against external interferences [90]. Also operation states and so device aging differ a lot in these two fields. In the following sections, a general aging related evaluation of operation states and arising aging mechanisms is performed on two exemplary circuit structures, each representing their application domain: the inverter for the digital circuits and a simple single-ended OTA (Operational Tranconductance Amplifier) for the analog field. The subsequent chapters will further reveal that this evaluation is universally valid to a large extent and also transferable for more complex circuits.

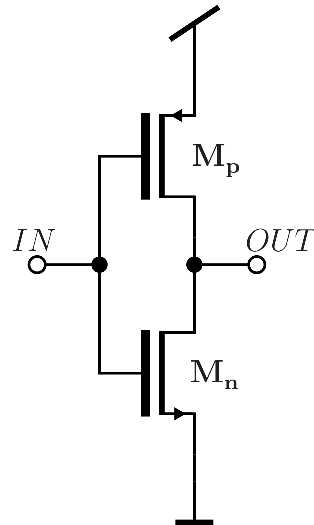

Fig. 4.1: Schematic of digital inverter circuit

4.1.1 Circuit Design Properties

Digital

Digital circuits in CMOS technique are built of logic gates, typically providing transistor stacks of nMOS and pMOS transistors evaluating the logic function. The basic and most simple digital block is the inverter as shown in fig. 4.1. The triumph of digital CMOS can be related to the above mentioned robustness of the circuit due to digital signal processing and the coherent ability of using minimum size devices. This gives rise to high density of digital logic processing and the big profit of CMOS technology scaling. To achieve minimum area consumption, digital logic gates are built with transistors of the minimum gate length provided by the CMOS process. For symmetric switching, the pMOS is built with a larger width than the nMOS to compensate for pMOS's weaker current driving capability.

Analog

The large field of analog circuits incorporates electronic circuitry dealing with an analog processing of voltages and currents. In contrast to the digital domain, the analog signal processing is very sensitive to lots of perturbations. To account for external interferences, process variations, device noise, short-channel effects etc. lots of techniques on circuit level, like differential signal processing, and on device level, like the insertion of large area devices, are used in analog circuit design. With just a few exceptions, analog processing circuits do not incorporate minimum size devices as analog device properties like matching and short channel effects strongly improve for larger gate length and device size. Especially for the exemplary analog circuit, the single-ended OTA in fig. 4.2, intended high amplification can only be achieved by the usage of long channel length devices to fulfill sufficient high small signal output resistance. To limit amplifier's offset, matching of

Fig. 4.2: Schematic of basic single-ended differential amplifier

the input pair ($\mathbf{M_{n1}}$,$\mathbf{M_{n2}}$) and the load ($\mathbf{M_{p1}}$,$\mathbf{M_{p2}}$) is important, which can be improved by increasing device area. But also the current bias source $\mathbf{M_{n3}}$ has to provide a sufficient high output resistance to suppress propagation of common mode input signals.
This very basic evaluation shows that the typical device used in analog circuits is of large area and gate length. As shown in the previous chapter in 3.9, this dimensioning inherently reduces HCI degradation as it strongly decreases with increased gate length.

4.1.2 Operation Conditions

After the evaluation of distinct device properties for both circuit domains, typical device operation is discussed to investigate operation related device aging.

Digital

Fig. 4.3 shows the typical switching behavior for the digital inverter circuit in fig. 4.1. For a high input signal $IN = V_{DD}$, the output switches to $OUT = V_{SS}$ and vice versa. During the steady state, one device of the inverter is fully turned on with $V_{GS} = V_{DD}$ and $V_{DS} = 0V$ and operates in deep triode region. Hence, its counterpart is turned off with $V_{GS} = 0V$ and $V_{DS} = V_{DD}$. So, during the steady state for a high input $IN = V_{DD}$, $\mathbf{M_n}$ sees a PBTI stress condition, whereas $\mathbf{M_p}$ a NCHCI one. For the condition $IN = V_{SS}$, NCHCI is induced in $\mathbf{M_n}$ and NBTI in $\mathbf{M_p}$. During switching, fig. 4.3 shows for a short period the entering of the device, previously stressed in NCHCI condition, into saturation with $V_{DS} \geq V_{DD}$ inducing a CHCI stress condition. Taking into account the results from

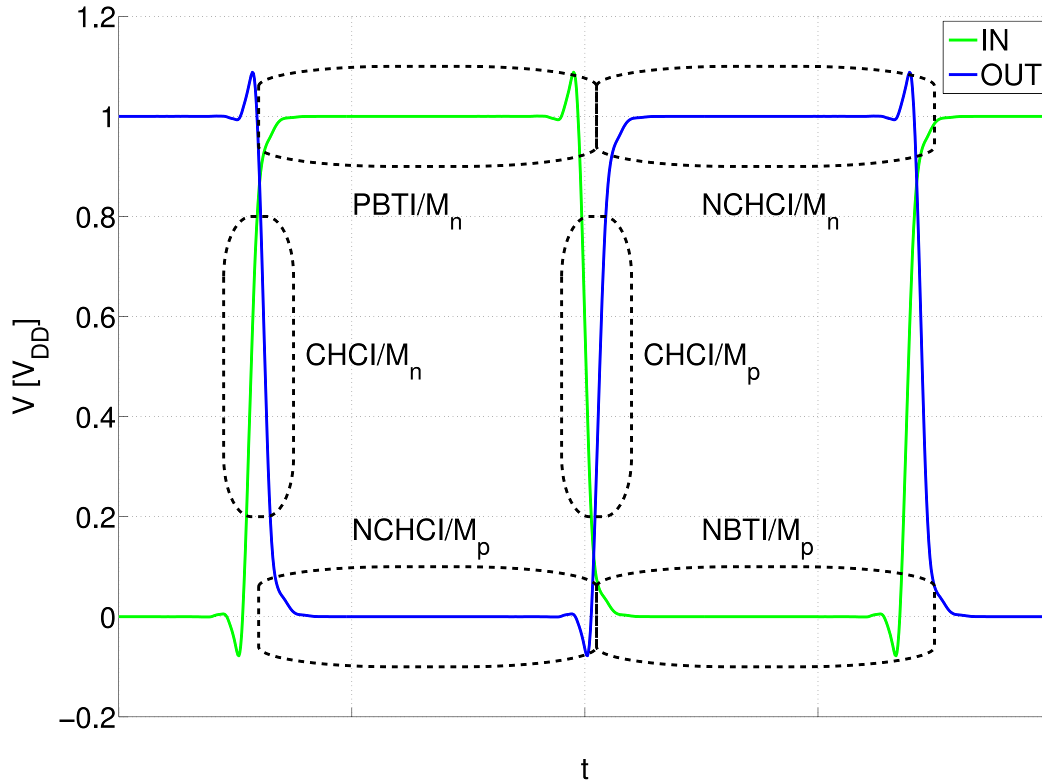

Fig. 4.3: Switching behavior of a digital inverter and arising stress conditions during operation

fig. 3.20 and 3.21, devices in the digital circuit can suffer from high HCI contribution due to their minimum gate lengths.
For the digital circuit domain, aging relevant operation conditions can be summarized to the following stress states. Stress states are named according to the stress voltage drop between the Gate-Source and Drain-Source terminals. During steady state,

- **HL:**[1] BTI stress in deep triode region, with $V_{GS} \approx V_{DD}$ and $V_{DS} \approx 0V$,
- **LH:**[1] NCHCI stress in off-state, with $V_{GS} \approx 0V$ and $V_{DS} \approx V_{DD}$,

and for short periods during the evaluative switching

- **MH:**[1] CHCI stress in saturation region, in worst case with $V_{GS} \approx \frac{V_{DD}}{2}$ and $V_{DS} \geq V_{DD}$.

Analog

For the analog field, most of the aging relevant operation conditions from the digital domain can also be found, but have to be extended to analog circuit operation conditions.

[1] $V_{GS}V_{DS}$ voltages - L:low, M:moderate H:high

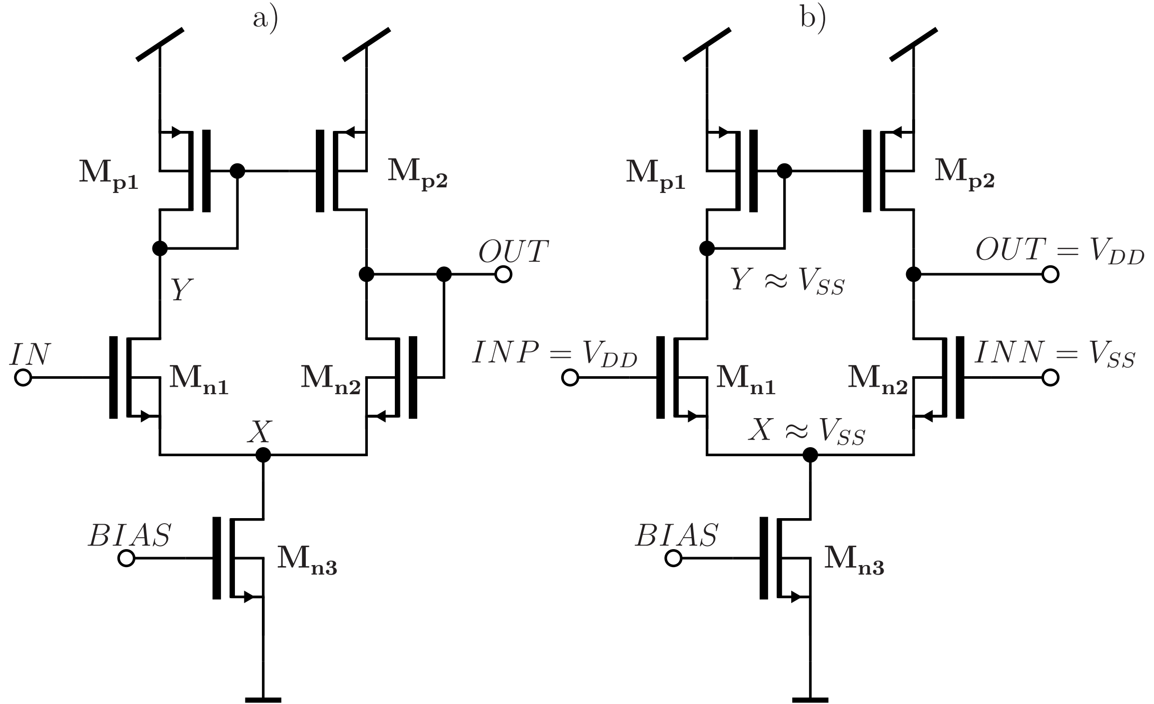

Fig. 4.4: Basic single-ended differential amplifier in closed-loop a) and open loop operation b).

A classic *linear* analog circuit typically evaluates a small change of an input signal around a stable operating point. The circuit in fig. 4.4 a), shows the exemplary OTA in a *closed-loop* voltage buffer configuration. Here, the voltage of the output node OUT follows the one at the input node IN. Input and output signal headroom is limited to a range smaller than the supply headroom as all devices have to operate in saturation region. In this operation state, it can be assumed that devices are biased close to their intended operation point, with $|V_{GS}|$ a few hundred millivolts above threshold voltage V_{th} and a V_{DS} that ensures operation in saturation $|V_{GS}| - |V_{th}| \leq |V_{DS}| < V_{DD}$. For advanced CMOS technologies with the low supply voltages [2, 91], it can be simplified assumed that devices operate around $|V_{GS}| \approx \frac{V_{DD}}{2}$. In this range only minor BTI degradations are induced, and also CHCI degradations - even for high $|V_{DS}|$ - are small due to long channel devices (see fig. 3.20).
Using the circuit in an *open-loop* or *comparator* configuration with full swing at the input (see fig. 4.4 b)), stress conditions similar to the digital operation occur. $\mathbf{M_{n1}}$ operates in deep triode region with $V_{GS,n1} \approx V_{DD}$ and $V_{DS,n1} \approx 0V$, the worst case PBTI stress condition, whereas $\mathbf{M_{n2}}$ is switched-off with full swing at the Drain ($V_{GS,n1} \approx 0V$ and $V_{DS,n2} \approx V_{DD}$) - a NCHCI condition. Current mirror devices $\mathbf{M_{p1}}$ and $\mathbf{M_{p2}}$ operate at $|V_{GS,p1/2}| \approx V_{DD}$ with $|V_{DS,p1}| \approx V_{DD}$ and $|V_{DS,p2}| \approx 0V$. So, both transistors are biased with the same Gate, but with different Drain voltages: $\mathbf{M_{p1}}$ in saturation region and $\mathbf{M_{p2}}$ in deep triode region. In both devices NBTI degradation occurs, but due to the individual operation region with different magnitudes. Depending on the gate length of $\mathbf{M_{p1}}$, an additional CHCI degradation can contribute to the overall device degradation. The bias source transistor $\mathbf{M_{n3}}$ also operates in deep triode region, but with moderate

V_{GS}, so PBTI degradation will be negligibly small.
Another analog related operation state may arise during circuits' built-in standby state. As given in the example in fig. 4.5, circuit block I is connected to the supply, whereas block II is disconnected from the supply and driven in a standby mode. In the worst case scenario the output voltage of block I provides the full swing and $\mathbf{M_p}$ is biased in accumulation mode. This induces an uncommon PBTI condition at $\mathbf{M_p}$. As there is no current flow in accumulation mode, PBTI degradation is equally distributed over the device oxide, similar to the inversion mode triode region BTI degradation.
Aging relevant stress conditions for the analog field in an advanced CMOS technology

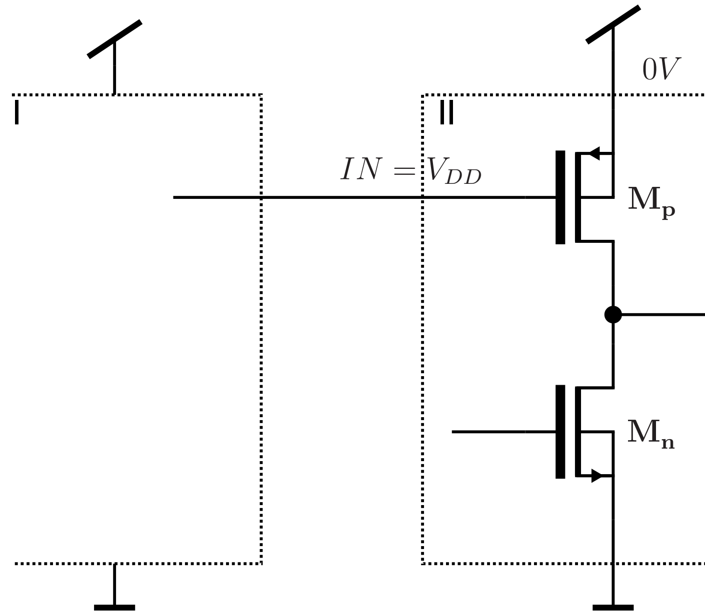

Fig. 4.5: Further stress state during partially standby mode: accumulation operation

and an exemplary nMOS device can be concluded to:

- **MH:**[1] analog operation in worst case saturation, with $V_{GS} \lesssim \frac{V_{DD}}{2}$ and $V_{DS} \approx V_{DD}$,

with expected negligible BTI degradation and CHCI degradation depending on the gate length dimensioning. The known stress states from the digital domain with full swing differential switching:

- **HL:**[1] BTI stress in deep triode region, with $V_{GS} \approx V_{DD}$ and $V_{DS} \approx 0V$,
- **LH:**[1] NCHCI stress in off-state, with $V_{GS} \approx 0V$ and $V_{DS} \approx V_{DD}$.

Degradation during the **LH** stress state further depends on used device's gate length. And finally the worst case operation in a current mirror configuration and the standby accumulation mode:

[1] $V_{GS}V_{DS}$ voltages - L:low, M:moderate, H:high, A: accumulation mode

- **HH:**[1] BTI/CHCI stress in saturation region, with $V_{GS} \approx V_{DD}$ and $V_{DS} \approx V_{DD}$,
- **AL:**[1] accumulation mode BTI stress, with $V_{GS} \approx -V_{DD}$ and $V_{DS} \approx 0V$.

4.1.3 Impact on Device Characteristic

After the general evaluation of design and operation characteristics in the digital and analog circuit domain, the impact of individual device aging is evaluated for a 32nm high-κ, metal gate CMOS technology [91]. Aging simulations base on an implementation of the semi-empiric degradation models from section 3.5.1 for the reliability simulator RelXpert™[77]. The CMOS technology and the degradation simulation approach is also used during the circuit investigations in the following chapters.

Digital

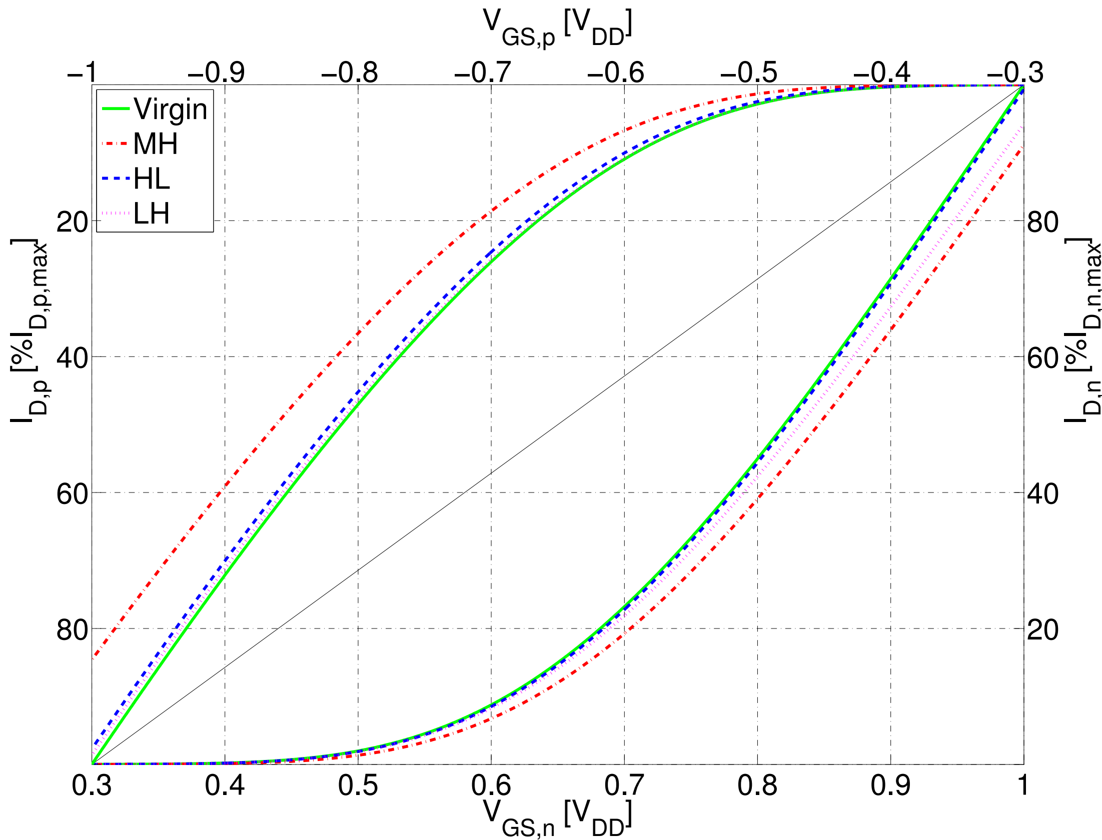

Fig. 4.6: nMOS and pMOS input characteristic in saturation ($V_{GS} = V_{DS}$) for a virgin digital device and after digital circuits' operation related use cases

For digital type devices the three aging related operation conditions are evaluated for the mobile phone use case introduced in section 3.8. For simplicity, operation states

[1]$V_{GS}V_{DS}$ voltages - L:low, M:moderate, H:high, A: accumulation mode

are assumed as DC voltage conditions. This overestimates CHCI degradation for the **MH** state that only occurs for a short time period during digital switching. But taking into account the sublinear aging behavior in time of eq. 3.10, even a significant reduction of the stress period in the **MH** use case to consider the switching event will result in minor reductions of the total CHCI degradation. So, the evaluated degradation in the **MH** state can be assumed as an absolute worst case scenario.

Figure 4.6 shows simulated I_D vs. V_{GS} input characteristics for virgin and aged nMOS and pMOS devices in saturation region ($V_{DS} = V_{GS}$). For nMOS and pMOS devices the **MH** use case arises as one main aging contributor during digital switching operation, which can be related to the strong gate length dependency of the CHCI effect. The **HL** use case with induced BTI degradation only shows moderate contribution to the overall device characteristic. Especially for the nMOS device the **LH** off-state with induced NCHCI degradation shows high degradation values. On the other hand, for the pMOS device NCHCI degradation in the **LH** state is negligibly small.

During digital circuit operation, aging relevant operation states alternate. The effect contributions will add up, but due to missing correlation behavior, exact mechanisms interaction is still unclear. Nevertheless, major aging contributions can be related to the logic gate switching and the induced CHCI degradation.

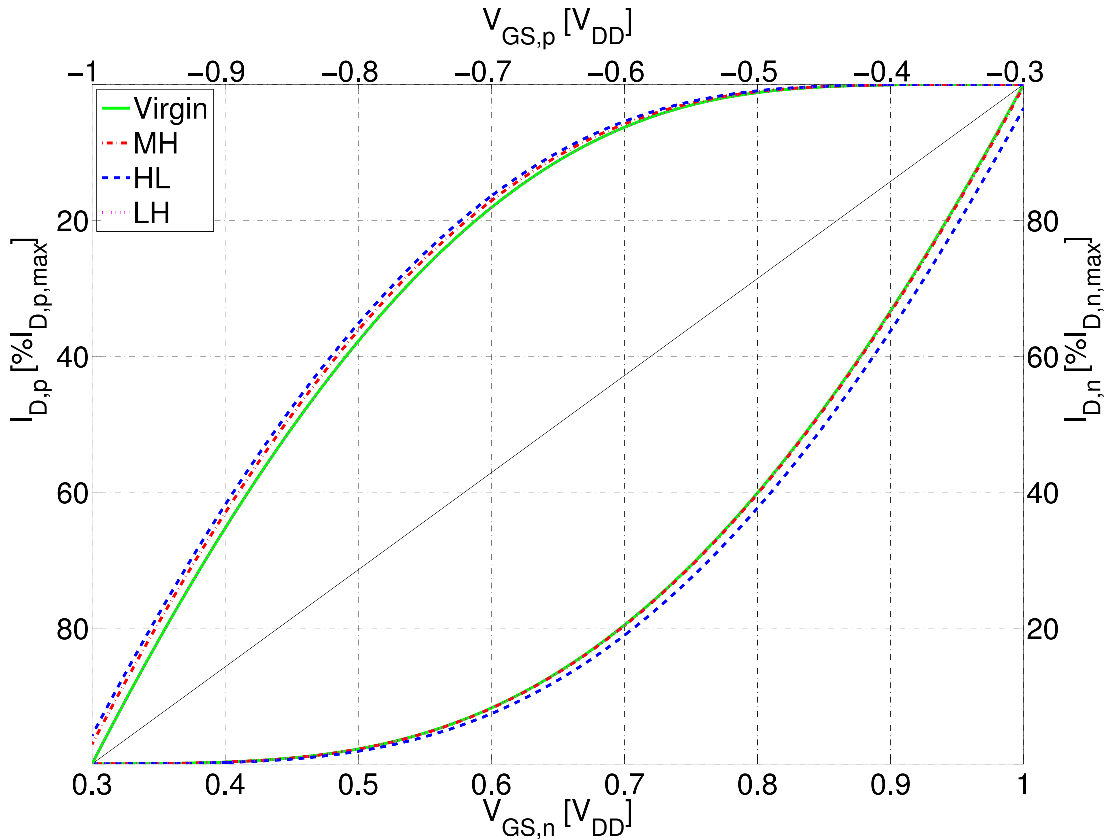

Fig. 4.7: nMOS and pMOS input characteristic in saturation ($V_{GS} = V_{DS}$) for a virgin analog device and after analog circuits' operation related use cases

Analog

For the analog type devices and their operation related aging states, the mobile phone use case is also employed. Operation states are evaluated for the **MH**, **HL** and **LH** states with DC stress voltage conditions, similar to the digital cases. Especially, the **MH** operation state is better predicted in consideration of circuit operation with DC voltage stress, as in analog circuits devices typically operate in saturation region in a stable DC operating point. **HH** is omitted as the important 2 dimensional BTI prediction (V_{GS} and V_{DS} dependent) in saturation is not supported by the model equation in (3.6). An evaluation with the given model implementation would lead to the same results as **HL** and thus to overestimated device degradation. Due to a missing model for the accumulation operation state, an investigation of the **AL** state is also passed over.

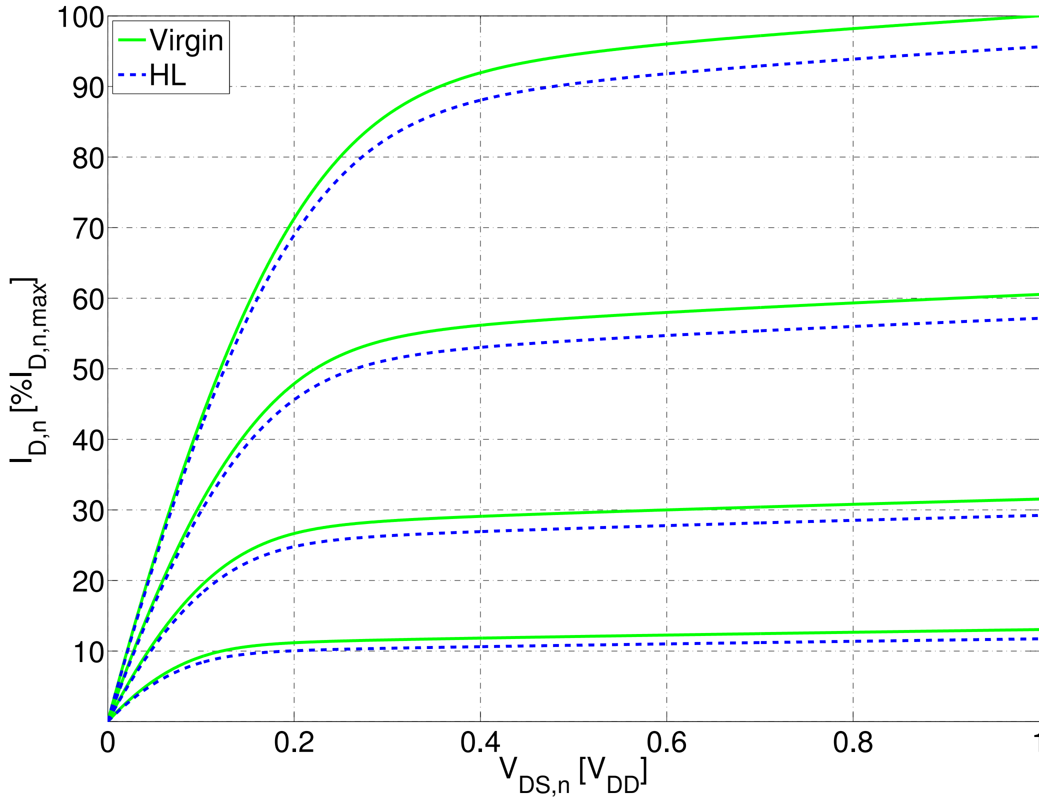

Fig. 4.8: nMOS output characteristic with selected V_{GS} levels for a virgin analog device and after the analog circuit HL operation use case

Fig. 4.7 shows the corresponding input I_D vs. V_{GS} characteristic for a virgin and aged analog type device, providing a typical analog gate length of 6 times the minimum length that is supported by the CMOS processing. Due to the large gate length, both CHCI and NCHCI degradations during the **MH** and **LH** operation cases are limited to small values, except for the **MH** state on the pMOS device. Here, CHCI degradation induces

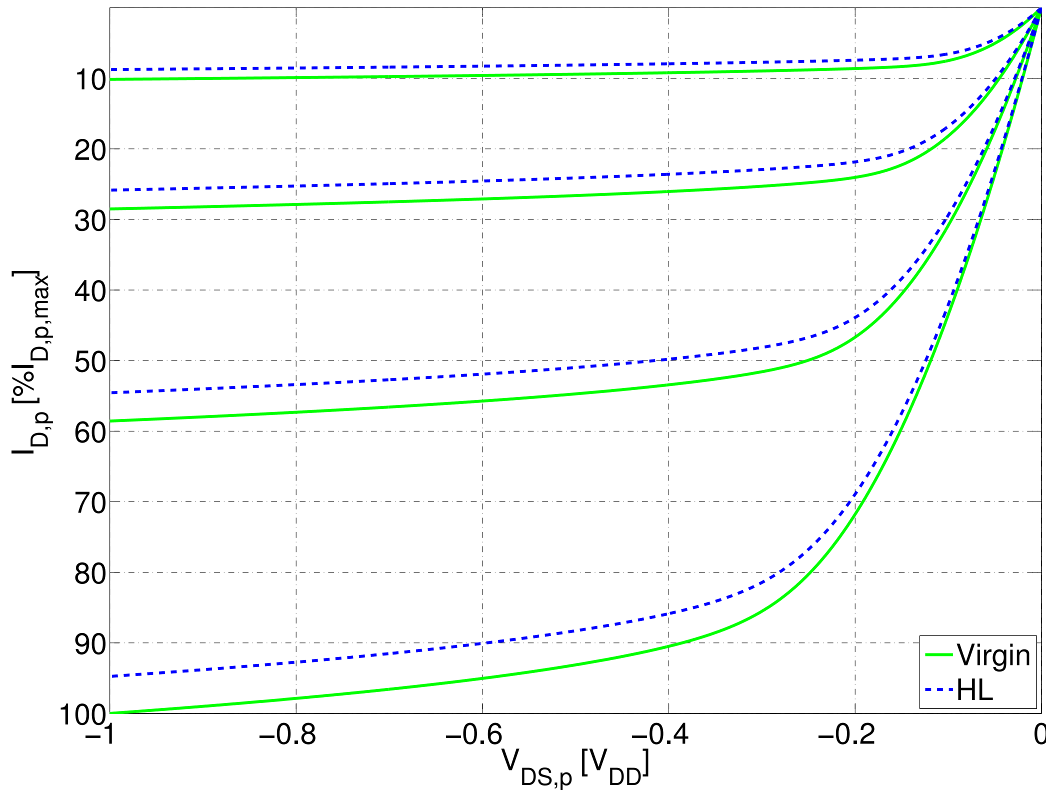

Fig. 4.9: pMOS output characteristic with selected V_{GS} levels for a virgin analog device and after the analog circuit HL operation use case

a significant contribution that can be related to the arising LSHA [71], already discussed in section 3.4.2. For the analog circuit operation, the **HL** operation state induces most of the device degradation contribution due to the area independent BTI degradation. For the virgin and the most significant **HL** operation state, the important analog related I_D vs. V_{DS} characteristic is depicted in fig. 4.8 and 4.9. In saturation region nMOS and pMOS devices act as a V_{GS}-controlled current source for I_D with a high ohmic output resistance. This device behavior provides the basis for analog circuit operation like voltage amplification circuits. The reduction of current driving ability due to aging influences analog circuit behavior in lots of ways.

A very special application of MOSFETs in analog circuits is the usage of the highly non-linear MOS capacitance [32]. In LC based VCO circuits, MOSFET's capacitance and its capacitor tuning ability via the back-biasing effect can be used to perform a controllable oscillation frequency. Such a voltage controlled capacitor is called *varactor* [92]. The typical configuration of a varactor in an oscillator circuit is given in fig. 4.10. V_G is connected to the oscillating LC tank and via V_{tune} on the Source and Drain node, a shift of device's threshold voltage V_{th} and thus a shift in the corresponding C-V characteristic is performed as depicted in fig. 4.11. Also in varactor operation, MOSFETs experience wearout, that is limited to BTI degradation, mostly occurring during oscillation peak state. This corresponds to the previously evaluated **HL** operation, inducing significant

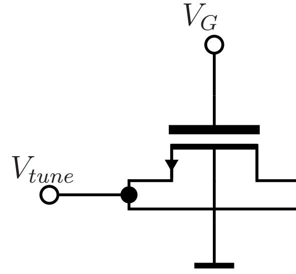

Fig. 4.10: Typical nMOS varactor configuration

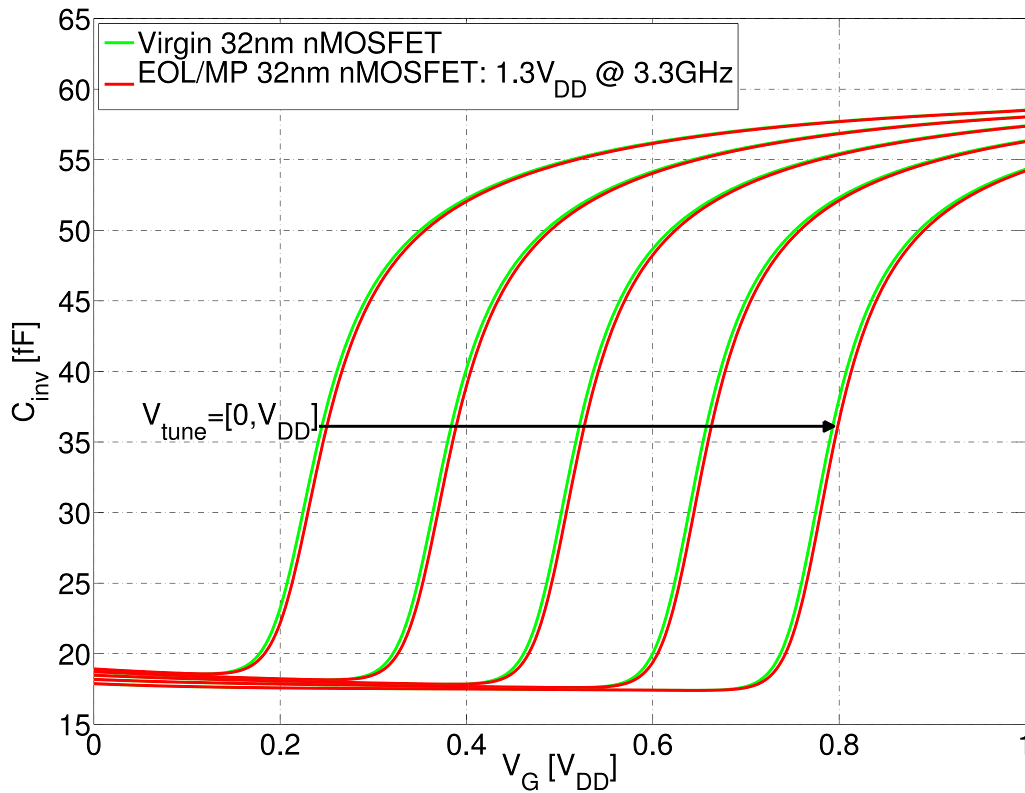

Fig. 4.11: C-V characteristic for a 32nm nMOS varactor in inversion mode: virgin and in end-of-lifetime/mobile phone state with slightly elevated voltage stress condition

BTI degradation for low V_{tune} levels for nMOS and high V_{tune} levels for pMOS varactors. As LC oscillators are typically designed with significant voltage overshoots above the nominal supply [92], BTI induced V_{th} drifts can be large. Due to the shorted Source and Drain terminals, voltage drop across the channel is zero, thus HCI degradation is excluded. Furthermore, fig. 4.11 includes the simulated C-V characteristic for an aged nMOS varactor in an adapted mobile phone end-of-lifetime state, with a slightly elevated voltage swing of $1.3 \cdot V_{DD}$ to account for typical voltage overshoots. Oscillation frequency was set to 3.3 GHz to be conform to the investigations in the subsequent chapter 7. The

graph in fig. 4.11 shows only a slight drift of the aged C-V characteristic even for the applied worst case operation condition. This is mainly due to the strong dependency of C_{inv} values to the gate voltage swing that operates with magnitudes of volts compared to the device degradation that is in the region of millivolts. Nevertheless, device aging further changes MOS varactor's capacitance tuning and thus impacts the oscillator circuit behavior.

4.1.4 General Impact on Circuit Characteristic

For *digital* circuits the exact shape of the transistor characteristic is not as important as for the analog domain. Here, the fast switching of the logic gate demands for an exact turn-on and turn-off of the device with high current driving ability for high V_{GS} and low leakage current for low V_{GS}. The general decrease of current characteristic mainly affects logic gate's switching delay as it is related to the loading of the capacitance at the gate's output node. Works treating digital logic aging can be found in [4, 6, 5, 93].
On the other hand, *analog* circuits behave more complicated towards aging induced parameter drifts as they are sensitive to lots of device properties. Besides speed constraints, further operating point dependent performance parameters like transconductance, output resistance, device noise, but also matching can be affected by the device degradation. Depending on the design, circuit performance parameters like offset, amplification, noise behavior, but also proper start-up ability can be more or less affected by the device aging. Furthermore, frequency tuning behavior in VCOs can be affected by the aging of the used MOS varactors. To get a deeper insight into analog circuit aging behavior and the modeling approach in this work, a more detailed investigation of MOS varactor aging behavior is treated in the next section. In the sequel, open topics of analog related device degradation are treated that are not fully covered by state-of-the-art wear-out modeling.

4.1.5 MOS Varactor Aging Behavior Model: A Case Study

This case study on the varactor aging behavior is an example of the typical modeling approach for the following investigations on more complex analog circuits. As already mentioned in sec. 4.1.3, MOS varactors are typically used in LC VCO circuits to perform a frequency tuning of the oscillator. Due to performance reasons, oscillation amplitude uses the full supply voltage swing or even exceeds this level. During oscillation, the highly non-linear C-V characteristic of the varactor is traversed leading to asymmetric oscillation waveforms. The effective capacitance $C_{eff,inv}$, that defines the oscillation frequency, can be related to the average value of the capacitance in the LC tank. Fig. 4.12 shows $C_{eff,inv}$ in dependence of the tuning voltage V_{tune} for the nMOS varactor of fig. 4.11 for full supply swing oscillation. It can be seen that BTI degradation of the varactor reduces its capacitance tuning range given by

$$\Delta C_{eff,inv,tune} = C_{eff,inv}\left(V_{tune}=0\right) - C_{eff,inv}\left(V_{tune}=V_{DD}\right). \tag{4.1}$$

On the contrary, boosting the oscillation amplitude V_G increases the tuning range (not shown). But this boost is accompanied by enhanced device degradation, again counter-

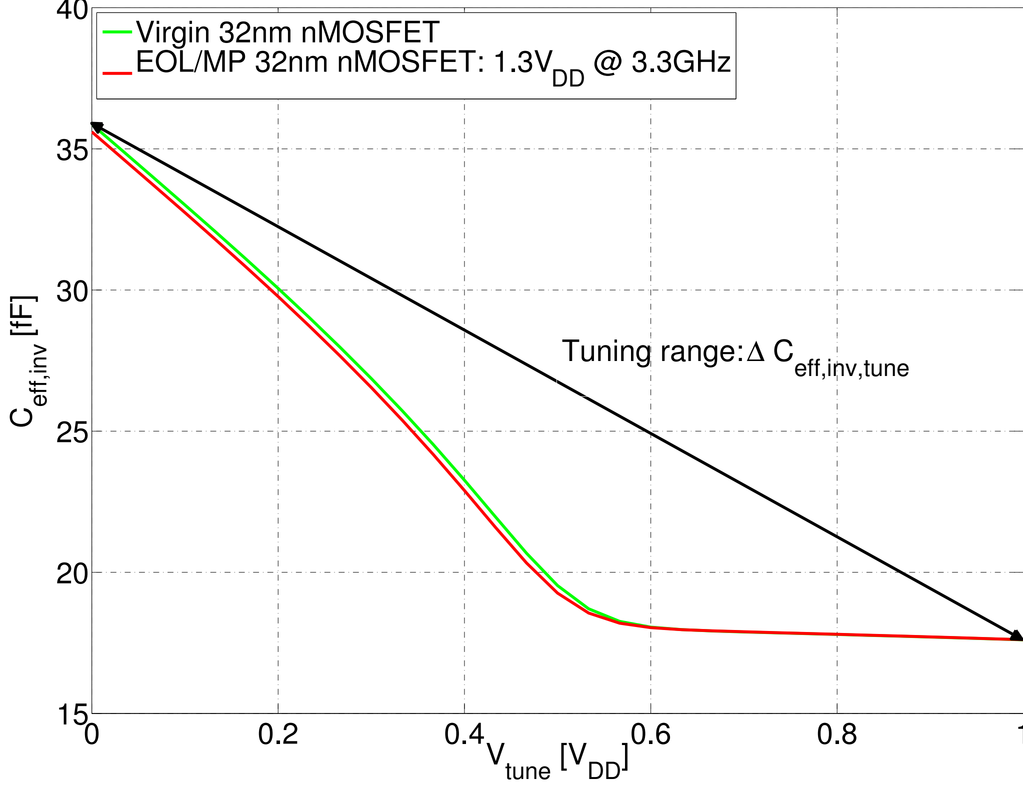

Fig. 4.12: $C_{eff,inv}$ varactor tuning for full swing oscillation for virgin and aged nMOS varactor

acting the $\Delta C_{eff,inv,tune}$ increase. Simulations revealed that sensitivities of $\Delta C_{eff,inv,tune}$ towards threshold voltage drifts and voltage swing boosts show a quite linear behavior for typical degradation and voltage swing ranges. Based on these findings, a linear aging behavioral model is presented, taking into consideration that with boosted voltage swing, $\Delta C_{eq,inv,tune}$ increases, but also varactor degradation increases, that further decreases the tuning range after end-of-lifetime operation. Combining the linear model of the varactor behavior with the BTI degradation prediction model from eq. 3.6 results in model equation 4.2.

$$\begin{aligned}\Delta C_{eff,inv,tune}\left(V_G\right) \quad = \quad & \Delta C_{eff,inv,nom}\left(V_{G,nom}\right) + \frac{\delta \Delta C_{eff,inv,V_{G,max}}}{\delta\left(V_{G,max} - V_{G,nom}\right)} \cdot \left(V_G - V_{G,nom}\right) \\ & + \frac{\delta \Delta C_{eff,inv,V_{th,max}}}{\delta \Delta V_{th,max}} \cdot \Delta V_{th}\left(V_G - V_{tune}, T, t_{eol}\right), \qquad (4.2)\end{aligned}$$

with $V_{G,nom}$ the waveform voltage peak for nominal supply voltage and $\Delta C_{eff,inv,nom}$ the corresponding tuning range value. $\frac{\delta \Delta C_{eff,inv,V_{G,max}}}{\delta\left(V_{G,max}-V_{G,nom}\right)}$ is the linear approximated sensitivity towards oscillation swing increase, $\frac{\delta \Delta C_{eff,inv,V_{th,max}}}{\delta \Delta V_{th,max}}$ the sensitivity towards threshold voltage drifts, T the operation temperature and t_{eol} the end of lifetime operation duration. Degradation for the oscillating stress voltage V_G is predicted via an AC correction factor.

This is obtained from RelXpert simulations for the oscillating circuit via setting in relation the AC degradation behavior to the DC voltage stress case. In the following discussion, a worst case aging scenario with an operation of the varactor with $V_{tune} = 0V$ is assumed. Fig. 4.13 shows the evaluation of the linear varactor model tuning range $\Delta C_{eff,inv,tune}$ in dependence of the oscillation amplitude V_G for the virgin and the MP/EOL use case. The

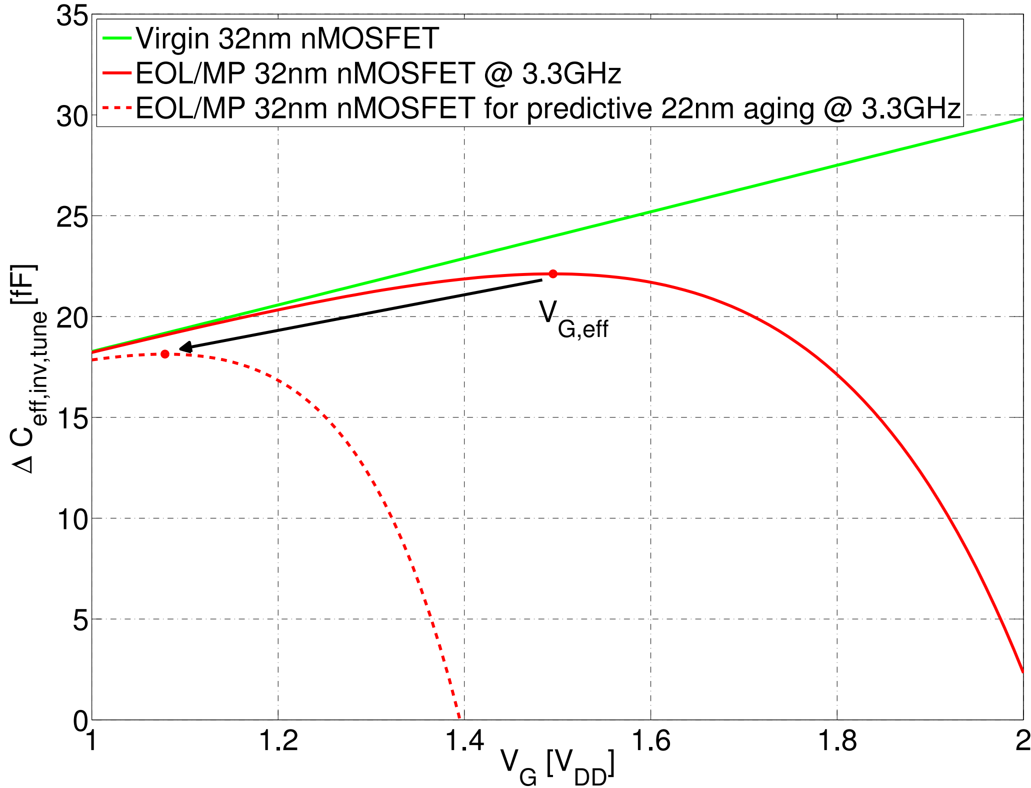

Fig. 4.13: $\Delta C_{eff,inv,tune}$ tuning range behavior for full swing oscillation for virgin and aged nMOS varactor

varactor in virgin state and the benefit of the amplitude increase V_G is given by the green curve, whereas the red curve shows $\Delta C_{eff,inv,tune}$ in the EOL use case. As already stated in the previous sections, the overall impact of the BTI degradation to the tuning range is small for oscillation amplitudes in the region of the nominal supply: $V_G = [V_{DD}, 1.5 \cdot V_{DD}]$. However, for higher voltage amplitudes the impact of the degradation dramatically increases. Here, the characteristic inflection point for $\frac{\delta \Delta C_{eff,inv,tune}}{\delta V_G} = 0$ provides the aging related most efficient oscillation amplitude $V_{G,eff}$ for best tuning range performance over the intended lifetime. For the used CMOS 32nm process this point is in the range of $V_{G,eff} \approx 1.5 \cdot V_{DD}$. Adapting the BTI model equation (3.6) with a predicted 22nm parameter set via scaling the exponent m and the oxide thickness t_{ox} by the factor $\cdot 1.3$ and $\cdot 0.76$ [2], $V_{G,eff}$ moves close to the nominal supply voltage as can be seen in the dotted line in fig. 4.13. For simplicity, this 22nm extrapolation model neglects reliability technology optimisation and assumes the same supply voltage as for the 32nm CMOS process

as well as the same C-V varactor behavior. So, this extrapolation approach provides a worst case scenario trend for upcoming CMOS processes.
This case study on the aging behavior of an exemplary nMOS varactor revealed, that the general approach of combining circuit behavior with device aging effect model equations proves to be a powerful and essential basis to provide insight into aging behavior from the circuit level perspective. Furthermore, this analytical approach opens new opportunities to derive aging related optimum operation points, circuit level aging behavior for future technologies, concepts for accelerated stress testing and many more prospects. Most of the developed concepts in the subsequent chapters base on similar approaches of circuit aging behavior modeling.

4.2 Advanced Analog Related Aging Tests

After the general evaluation of operation related device aging behavior for analog and digital CMOS device types and the exemplary introduction into circuit level aging behavioral modeling, a more detailed investigation on open aging mechanism properties affecting the analog operation field is conducted in the next sections.

4.2.1 Open Analog Related Device Aging Topics

For analog device operation several important facts are only partially or still not covered by the basic degradation prediction model approaches in eq. (3.6) and (3.10). The open questions are:

- **prediction quality:** Is the modeling via a 1-dimensional aging prediction equation accurate enough to consider device aging in analog operation states? Is degradation sufficiently well predicted by the consideration in only one model parameter like ΔV_{th}?

- **variations:** Does device aging induce, in addition to device parameter variations due to global and local process variations or layout induced effects, for analog type devices another relevant source of variations with significant impact on matching behavior?

- **effect recovery:** Aging prediction models provide a fixed degradation value. A great number of works revealed a transient recovery of the device degradation after device stressing, which is not supported by the prediction model. Which state of relaxation is and should be mapped by the prediction model? Does it cover a worst case scenario?

- **accumulation mode device aging:** As this operation mode is still not considered by any degradation model, arising device aging for this operation mode has to be investigated on analog type devices.

Furthermore, device aging behavior investigations for selected sequences of distinct stress periods should answer the following questions:

- **effect saturation:** Degradation model equations predict an effect saturation behavior due to the sub-linear time behavior for the application of several periods of equal stress in inversion mode. How does the recoverable part behave under those stress sequences?
- **mixture inversion and accumulation mode operation:** It has been shown that for accumulation mode, an accelerated recovery of inversion mode induced degradation occurs [62]. How does alternating inversion and accumulation stress affect the general device degradation behavior?

To resolve these open questions, a detailed study with a custom test circuit is conducted in the following sections.

4.2.2 Custom Test Circuit

The basic structure of the test circuit for the further studies is shown in fig. 4.14 for a nMOS version. It provides the ability to measure degradation of several cells, stressed

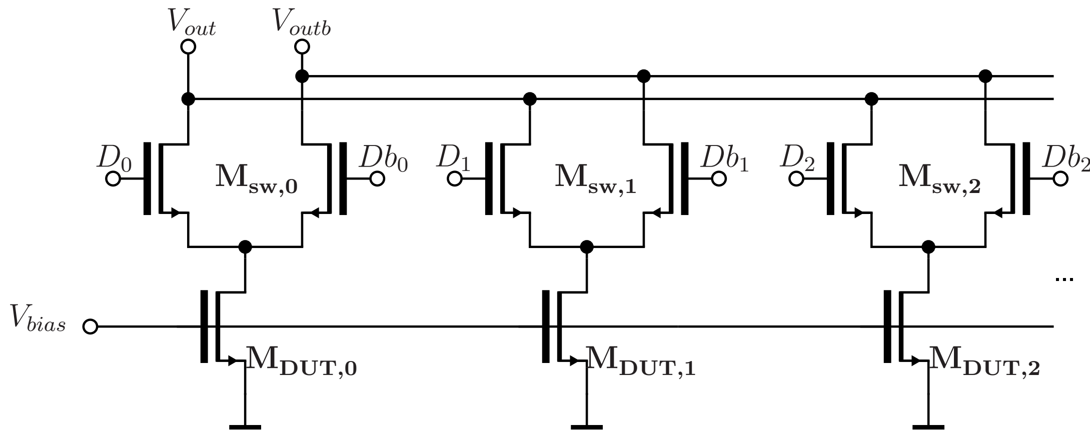

Fig. 4.14: Custom test circuit: nMOS implementation

under equal conditions, before, during and after stress. The idea of this test structure comes from differential stage basics, where the current of the tail transistor $\mathbf{M_{DUT,i}}$ is shared between both pair transistors $\mathbf{M_{sw,i}}$ according to their input voltage. For full swing digital voltages at inputs D_i and Db_i and a sufficiently large pair dimensioning, the current of the tail source can be switched between the outputs V_{out} and V_{outb} with a negligibly small impact of the switch resistance. In the test system, a digital logic block (not shown) generates the control signals D_i and Db_i to connect only one of the cells to V_{out} and in the mean time all others to V_{outb}. This enables the separate measurement of each individual cell current. Via the voltages at V_{bias}, V_{out} and V_{outb}, the operation region of the tail transistor can be adjusted in a sufficiently large interval to apply different stress

modes, while the connections to V_{out} and V_{outb} can be simultaneously switched between the cells to monitor $\mathbf{M_{DUT,i}}$'s current and derive its individual transistor characteristic. This test structure was designed and manufactured as nMOS and pMOS version in a 32nm high-κ metal gate technology [91], providing 16 cells with an 'analog size' tail transistor of $\frac{W}{L} = \frac{8.0um}{2.0um}$. The design in an array structure enables a basic device matching study. Aging simulations revealed that all performed stress tests primarily impact the tail source transistor. Only negligibly small degradation at the switch transistors occurs, which in turn has marginal impact.

4.2.3 Stress Test Approach

Measurement Sequence

Stress measurements on the test circuit are performed according to the scheme in fig. 4.15. The sequence starts with a characterisation of each $\mathbf{M_{DUT,i}}$ in the array by measuring the

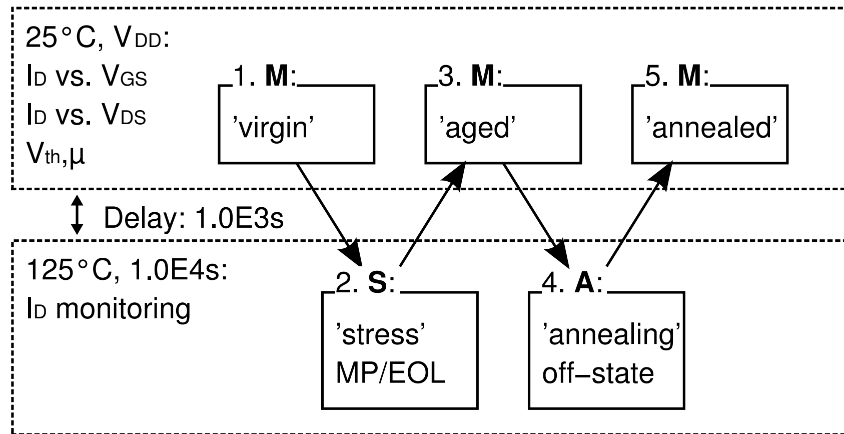

Fig. 4.15: Schematic of the basic test sequence

input I_D vs. V_{GS} ($V_{DS} = V_{GS}$) and the output I_D vs. V_{DS} characteristic (**M**) to determine device's threshold voltage V_{th} of the *'virgin'* device and for nominal operation conditions (25°C, V_{DD}). Then, the test circuit is heated-up to 125°C with a fixed assimilation delay of 1.0E3s. In the second step all $\mathbf{M_{DUT,i}}$ are exposed to the stress condition (**S**) via applying corresponding stress voltages to V_{bias}, V_{out} and V_{outb} for 1.0E4s. During the stress period, currents through the V_{out} and V_{outb} terminals are measured, offering the ability to monitor current degradation of each device during the stress period by switching through the array cells. After the stress period, the test circuit is cooled to 25°C and the device characterisation (**M**) from step 1 is repeated for the *'aged'* devices. Then, the circuit is again heated to 125°C and an annealing step (**A**) for 1.0E4s in off-state is applied to decay fast relaxing drift contributions. Finally, another input and output characterisation (**M**) is repeated to get device characteristic in the *'annealed'* state.

Threshold Voltage Derivation

Derivation of the devices' threshold voltage V_{th} is performed via the commonly used current limit. For nMOS devices this point is set to $300nA \cdot \frac{W}{L}$ and for pMOS devices to $-70nA \cdot \frac{W}{L}$.
Via an approximative model equation, online V_{th} drifts during the stress period can be derived from the measured current degradation of each cell. Starting with the basic nMOS model equation for triode region operation,

$$I_D = \mu C_{ox} \frac{W}{L} \left[\left(V_{GS} - V_{th} \right) V_{DS} - \frac{1}{2} V_{DS}^2 \right]. \tag{4.3}$$

Triode region stress current degradation can be expressed as

$$\begin{aligned} \Delta I_D =& I_{D,virgin} - I_{D,stressed} \\ =& \mu C_{ox} \frac{W}{L} \left[\left(V_{GS} - V_{th} \right) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \\ & - \mu C_{ox} \frac{W}{L} \left[\left(V_{GS} - V_{th} - \Delta V_{th} \right) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \\ =& \mu C_{ox} \frac{W}{L} \Delta V_{th} V_{DS}. \end{aligned} \tag{4.4}$$

Normalization to the stress current in the virgin case leads to

$$\frac{\Delta I_D}{I_{D,virgin}} = \frac{\mu C_{ox} \frac{W}{L} \Delta V_{th} V_{DS}}{\mu C_{ox} \frac{W}{L} \left[\left(V_{GS} - V_{th} \right) V_{DS} - \frac{1}{2} V_{DS}^2 \right]} \tag{4.5}$$

Assuming deep triode region operation, $V_{DS}^2 \approx 0$ and eq. 4.5 reduces to

$$\frac{\Delta I_D}{I_{D,virgin}} \approx \frac{\Delta V_{th}}{\left(V_{GS} - V_{th} \right)} \tag{4.6}$$

A similar approximative model equation can also be derived for a nMOS stressed in saturation operation. A detailed derivation is omitted at this point. The final model equation can be expressed as

$$\frac{\Delta I_D}{I_{D,virgin}} \approx \frac{2\Delta V_{th}}{\left(V_{GS} - V_{th} \right)}. \tag{4.7}$$

A corresponding model equation for the pMOS device considers the opposite sign for the pMOS equations. V_{th} can be determined from the pre-stress extraction of the input characteristic, while its temperature drift during the stress test can be neglected because the overdrive voltage is dominated by the high stress V_{GS}. The critical value is $I_{D,virgin}$ that has to be measured at time zero of the stress phase. Due to equipment timing limitations, the sampling of the virgin stress current can be performed only a few 100 ms after stress application yielding an underestimation of the 'online'-ΔV_{th}.

Device Stress States

In the following study, the circuit is stressed to an equivalent 'mobile phone' EOL state (see sec. 3.8). To cover the most significant aging related operation states, that were evaluated in sec. 4.1.2, $\mathbf{M_{DUT,i}}$ is driven in the **HL** and **HH** state to investigate for BTI degradation in deep triode and saturation region. Furthermore, via the individual V_{bias} stress voltage setting, the **AL** state is also analysed.
Aging simulation for the **HL** and **HH** operation states revealed, that due to the large gate length of $\mathbf{M_{DUT,i}}$ major contributions to the overall device aging are related to BTI. This simplifies effect acceleration for the stress testing. As already given in fig. 4.15, stress temperature is set to $T_{stress} = 125$°C and stress duration to $t_{stress} = 1.0E4s$. Via the acceleration approach given in eq. (3.15), the stress voltage V_{bias} is evaluated to meet the MP/EOL use case. As for the **AL** operation case, a corresponding NBTI/nMOS and PBTI/pMOS aging model equation is missing, the model from the counterpart device is used to evaluate the stress voltage.

Test Assembly

A photograph of the custom stress test assembly is given in fig. 4.16. The custom built

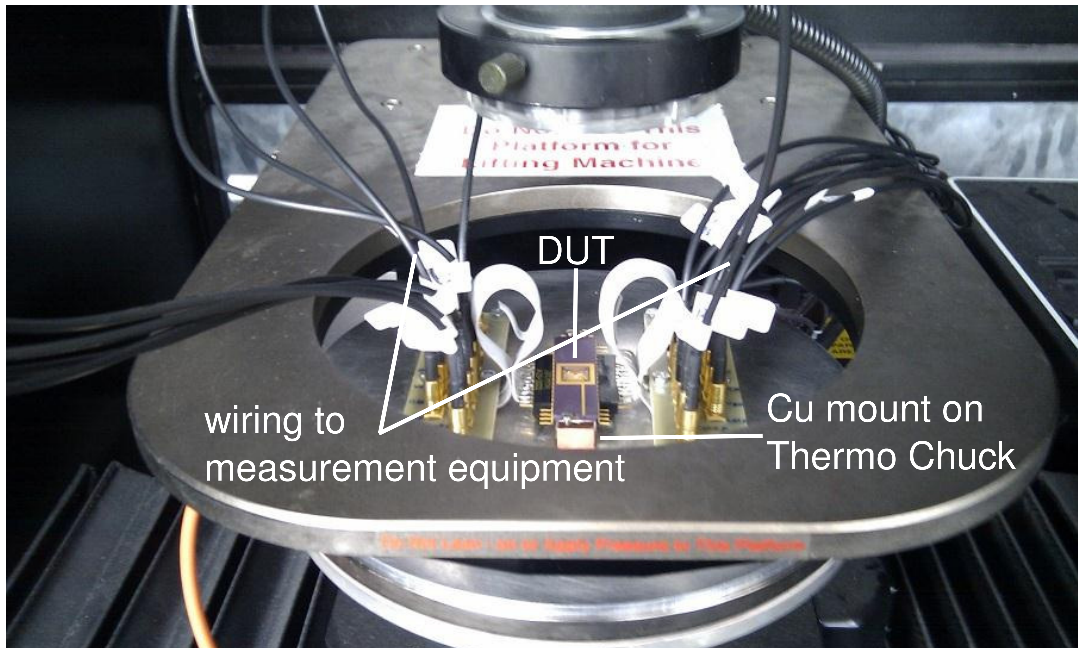

Fig. 4.16: Photograph of the test setup with test circuit used for the stress measurements

sample mount uses the accurate temperature control of a DPO315B ThermoChuck with a Cu sample mount heat conductor. Sample connection is performed via fully shielded SMB cables just to the sample plug. Digital patterns are generated with a PC based custom pattern generator card. For the accurate supply and stress voltage generation as well as for the current measurements, SMU (Source Measure Unit) units of an Agilent 4155B

parameter analyser are used. To guarantee reproducible test results, the measure and stress sequences are fully automated controlled via custom PC based LabView programs.

4.2.4 Stress Test Evaluation

In the following investigations, the stress sequence from fig. 4.15 is applied to the nMOS and the pMOS version of the test circuit (fig. 4.14) for the accelerated MP/EOL use case. Stress periods are performed for **HL** and **AL** operation mode stress condition.

Impact on Device Characteristics

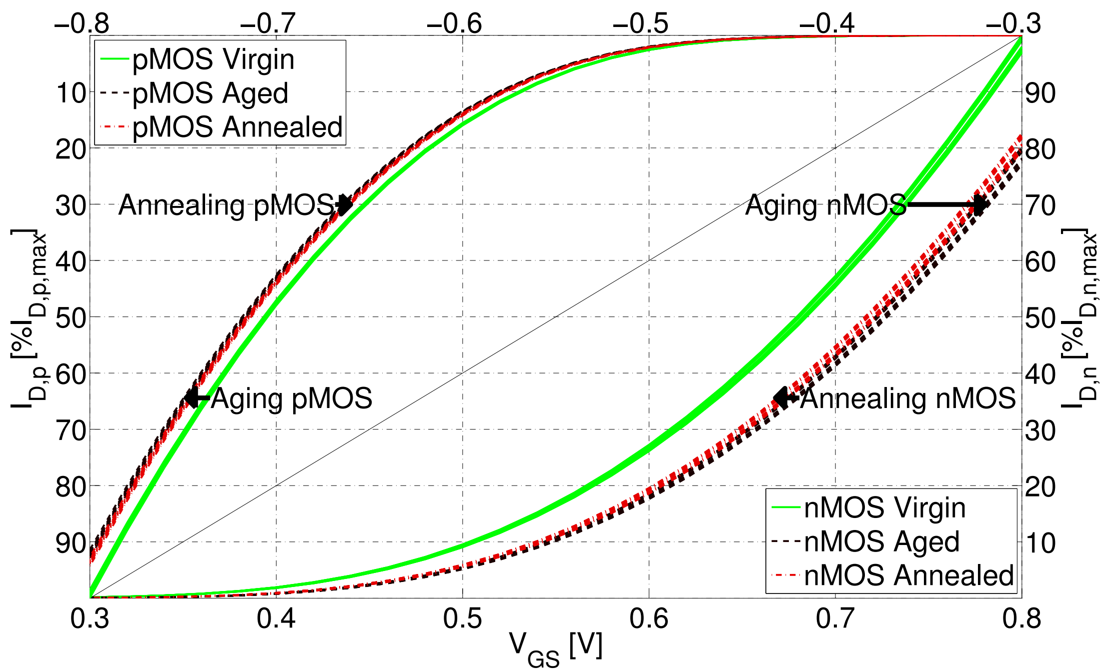

Fig. 4.17: Input characteristic I_D vs. $V_{GS} = V_{DS}$ of nMOS (lower right part) and pMOS (upper left part) test circuit: virgin, after HL operation mode stress and further high-T annealing; all 16 cells at 25°C

Fig. 4.17 shows the input characteristic of the nMOS and the pMOS before stress, after **HL** stress and further annealing in off-state. The three graphs correspond to step 1), 3) and 5) of the test sequence of fig. 4.15. Fig. 4.17 shows that for both device types, the **HL** operation scenario leads to a general weakening of transistor current. For completeness, the output characteristic of the nMOS circuit is also shown in fig. 4.18. Comparing current characteristics after the stress step ('Aged') and the further annealing step ('Annealed'), reveals that aging induced drift partially shifts back which is related to long term relaxation effects. To verify the approach of mapping BTI degradation solely in a drift of threshold voltage instead of a partitioning in ΔV_{th} and $\Delta\mu$, fig. 4.19 depicts the measured input characteristics from fig. 4.17 compensated with the derived threshold

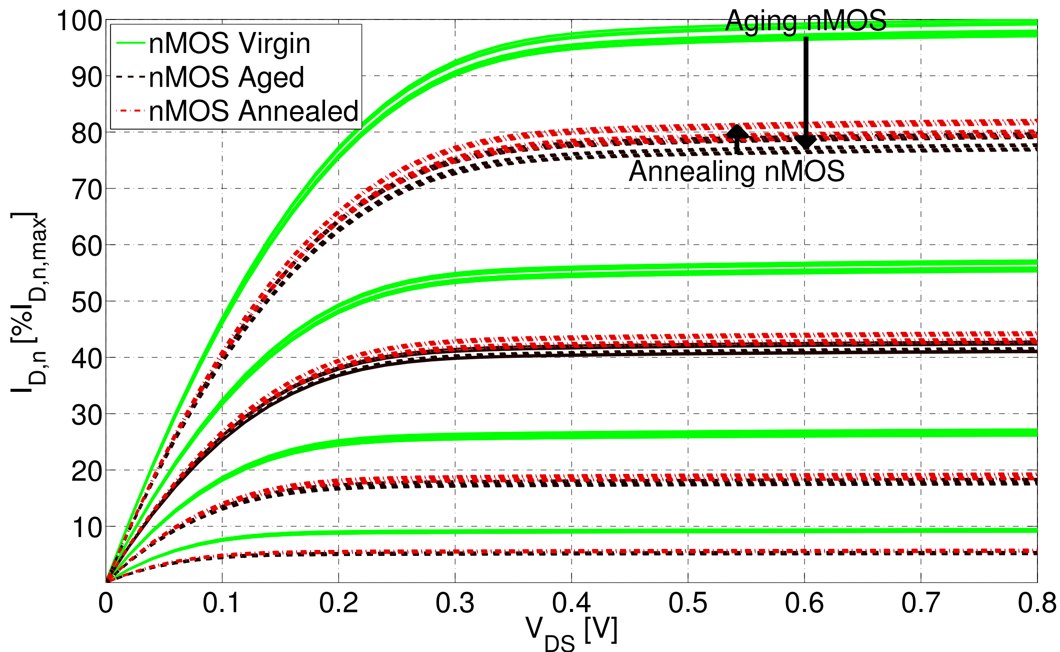

Fig. 4.18: Output I_D vs. V_{DS} characteristic for the nMOS test circuit: virgin, after HL operation mode stress and further high-T annealing; all 16 cells at 25°C

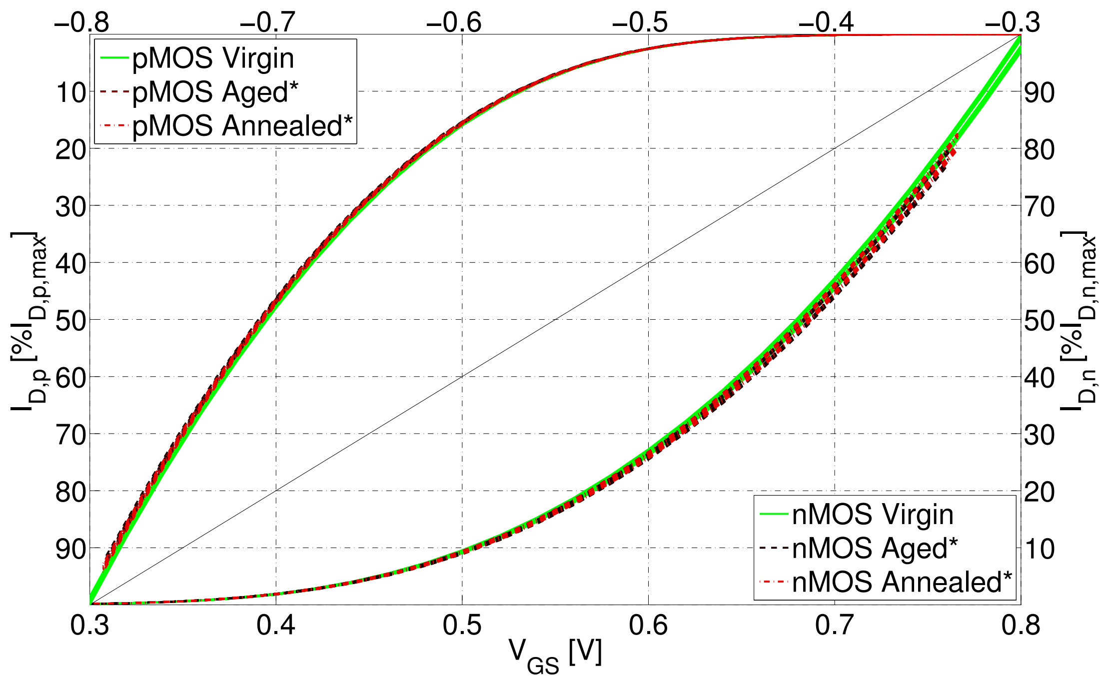

Fig. 4.19: Input characteristic I_D vs. $V_{GS} = V_{DS}$ of nMOS (lower right part) and pMOS (upper left part) test circuit: virgin, after HL operation mode stress and further high-T annealing; all 16 cells at 25°C; *characteristics are shifted for the measured induced threshold voltage drift $\Delta V_{th,i}$

voltage drift $\Delta V_{th,i}$ of each device. After the compensation, curves approximately match each other. Only a very small current weakening can be seen that can be related to a negligibly small mobility degradation. This proves that the mapping of the inversion mode BTI aging to a drift of threshold voltage ΔV_{th} is sufficiently accurate.

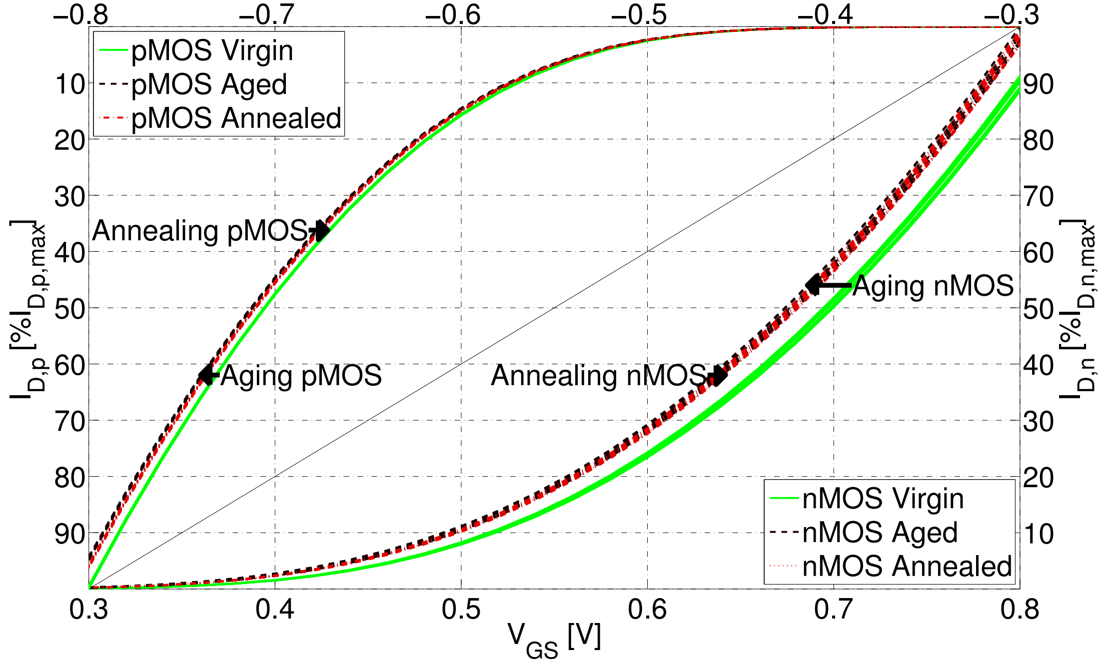

Fig. 4.20: Input I_D vs. $V_{GS} = V_{DS}$ characteristic of nMOS (lower right part) and pMOS (upper left part) test circuit: virgin, after AL operation mode stress and further high-T annealing; all 16 cells at 25°C

Fig. 4.20 depicts the nMOS and pMOS input characteristic for the **AL** operation mode stress case. Contrary to the **HL** operation case, **AL** mode aging of the nMOS leads to a higher on current of the 'aged' device. This is induced by a negative shift in threshold voltage, indicating a formation of positive charge in the dielectric, probably related to the formation of a p-accumulation layer from which holes can be trapped in the insulator. Accumulation mode stress for pMOS, however, shows an opposite behavior. Similar to the **HL** inversion mode operation, drain current is weakened, resulting from an increase of the absolute $|V_{th}|$ in combination with a significant decrease of channel mobility $|\mu_p|$, which is in line with the findings in [61]. This special **AL** mode aging behavior for pMOS devices can be seen in fig. 4.21, showing the input characteristic from fig. 4.20 compensated with the measured threshold voltage drifts $\Delta V_{th,i}$. While for nMOS devices mainly threshold voltage is affected by the **AL** operation stress, pMOS devices show a further mobility degradation, indicated by the improper curve matching after the $\Delta V_{th,i}$ compensation.
Device degradation in **AL** operation mode is still not covered by any prediction models, but significant and complex aging occurs. This demands for further investigations and modeling approaches also for accumulation operation modes to enable proper circuit level reliability estimations. Special features, as the observed improvement ability of **AL** stress for nMOS devices, will be further studied in subsequent combined stress tests.

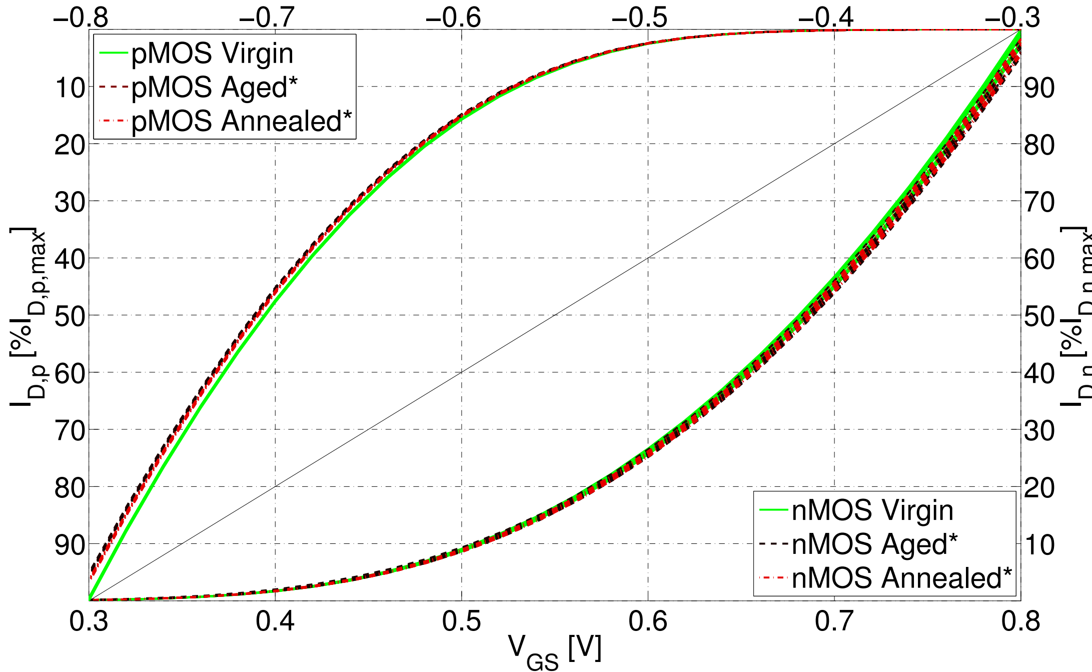

Fig. 4.21: Input I_D vs. $V_{GS} = V_{DS}$ characteristic of nMOS (lower right part) and pMOS (upper left part) test circuit: virgin, after AL operation mode stress and further high-T annealing; all 16 cells at 25°C; *characteristics are shifted for the measured induced threshold voltage drift $\Delta V_{th,i}$

Effect Recovery

Comparing device characteristics for the 'Aged' and 'Annealed' state in fig. 4.17 and 4.20 further reveal that degradations are not stable over time due to recovery of the aging induced drifts. Fig. 4.22 shows the extracted V_{th} of each cell for the 'Virgin', 'Aged' and 'Annealed' circuit for nMOS and pMOS after **HL** operation stress. $V_{th,i}$ values are normalised to the mean threshold voltage of the 'Virgin' test circuit. Comparing $V_{th,i}$ for nMOS and pMOS confirms a larger drift for the nMOS in the equivalent MP/EOL state. This higher nMOS degradation was already expected from the plot in fig. 4.17. For both device types, the high-T off-state annealing step recovers degradation by approximately 20%.

Extracted V_{th} after **AL** EOL operation is depicted in 4.23. Threshold voltages $V_{th,i}$ are also normalized to the mean value of the 'Virgin' test circuit. As already discussed in the previous section, **AL** operation leads to a negative drift of threshold voltage for the nMOS device and to a combination of a small $|V_{th}|$ increase and $|\mu_p|$ decrease for the pMOS device. For comparison reasons, fig. 4.23 only reproduces the threshold voltage drift part for the pMOS device. For the nMOS test circuit a local hot spot, induced by the voltage stress conditions and a protection system arises and distorts threshold voltage drifts for the cells 12-15. Corresponding degradation values are omitted in the following investigations. Also for the **AL** operation recovery occurs after stress removal. Comparing the recovery states 'Aged' and 'Annealed', the longterm effect recovery is generally smaller

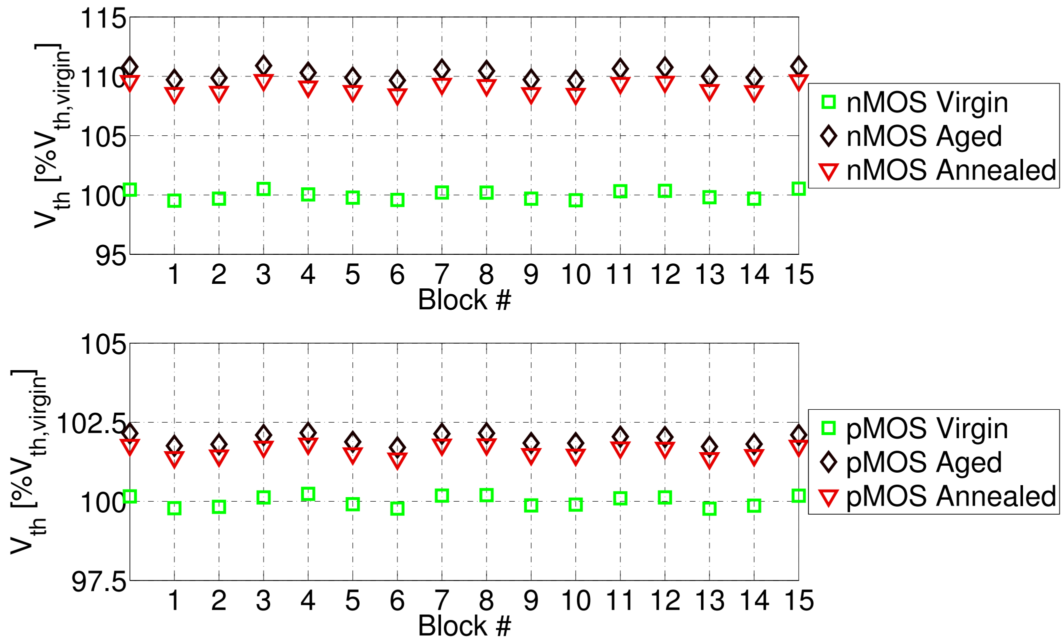

Fig. 4.22: Cell threshold voltage of nMOS and pMOS circuit: virgin, after stress in HL mode and further high-T annealing; all measurements at 25°C

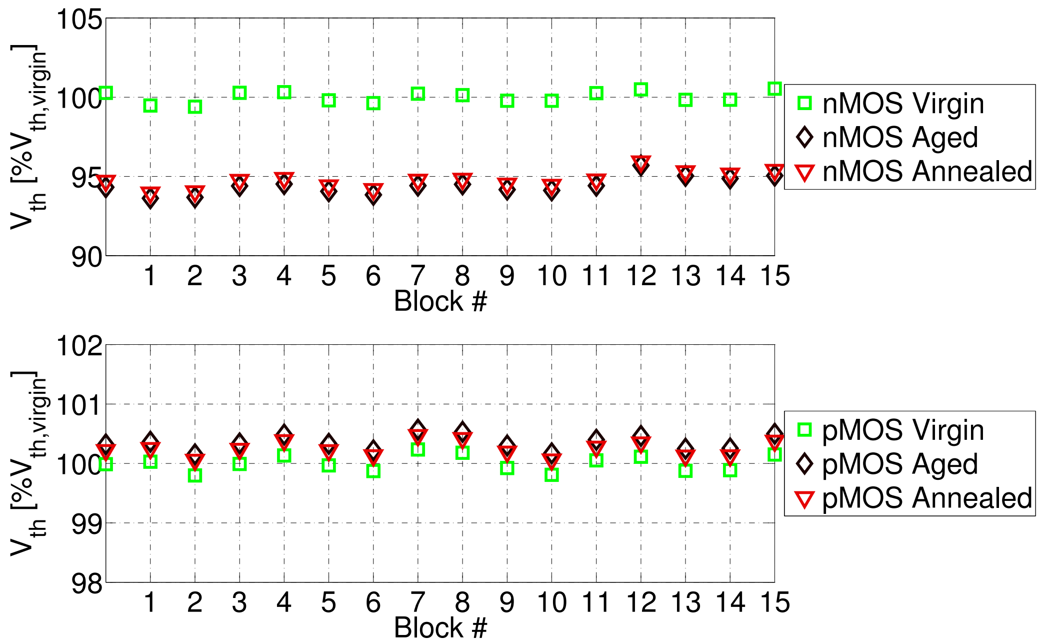

Fig. 4.23: Cell threshold voltage of nMOS and pMOS circuit: virgin, after stress in AL mode and further high-T annealing; all measurements at 25°C

than for the **HL** operation counterpart. A very common behavior of the longterm effect recovery for both device types and operation states, that can be observed in fig. 4.22 and 4.23, is that stress induced drifts generally shift back to the virgin state.

Observing also the fast relaxing components of the threshold voltage drift $\Delta V_{th,i}$ by

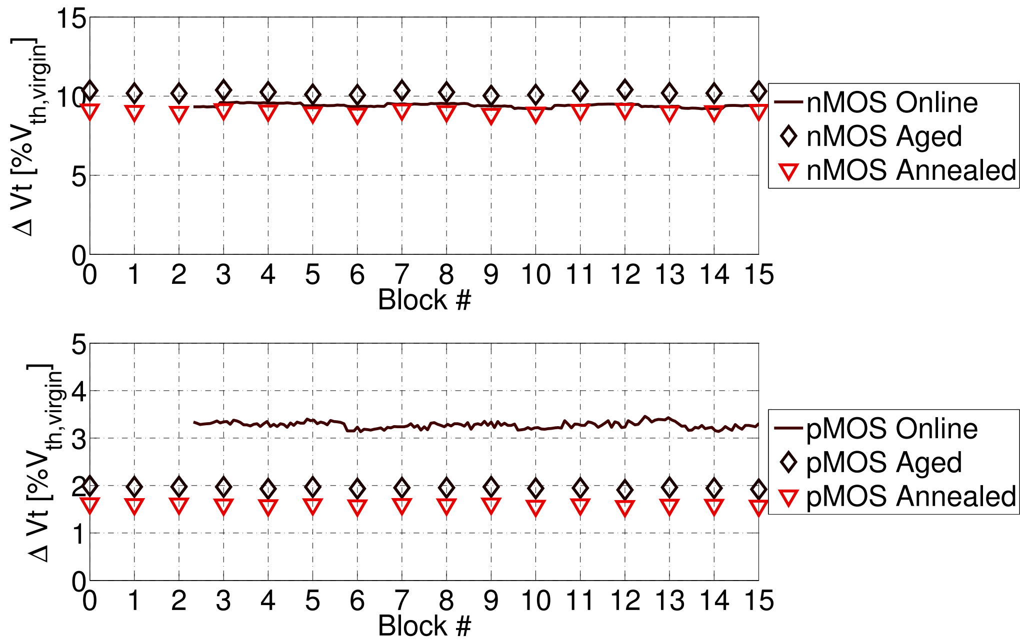

Fig. 4.24: Cell threshold voltage drift of nMOS and pMOS circuit: during HL stress at 125°C, after stress and 125°C annealing at 25°C

estimation of the degradation in the 'Online' state during the stress period can only be performed for the **HL** test, as here a controlled Drain current can be measured. 'Online' ΔV_{th} is predicted according to the approximative equation given in (4.5). Threshold voltage drifts $\Delta V_{th,i}$ for the **HL** operation in the 'Online', 'Aged' and 'Annealed' recovery state are depicted in fig. 4.24. The solid line illustrates the approximated $\Delta V_{th,i}$ levels from the stress current degradation during **HL** operation stress. Due to the mentioned delay in the current measurement, 'Online'-$\Delta V_{th,i}$ levels are not valid for the first three cells and are omitted in fig. 4.24. The nMOS 'Online'-ΔV_{th} reveals to be even smaller than the evaluated value in the subsequent 'Aged' parameter extraction. This can be related to a distinct PBTI short time relaxation behavior, that was also discovered in [94] and will be further investigated in chapter 6. It is assumed this is caused by a two polarity charge trapping during the nMOS **HL** stress, recovering with differing time constants and yielding to the relaxation curve shown in [94]. This explains the smaller 'Online' degradation in contrast to the degradation 15min after the stress. However, pMOS/NBTI 'Online'-ΔV_{th} shows the expected behavior of a higher degradation during stress, as according to common literature only equal polarity charge formation occurs. In this case 'Online'-degradation is even twice the degradation after the annealing step, which has to be considered when performing circuit reliability simulations.
The preceding study on the relaxation behavior of aging induced V_{th} drifts showed a variety in magnitudes and and also in general relaxation behaviors. Due to its vast range of relaxation time constants, a simple consideration of 'permanent' parameter drift to prove circuit reliability reveals to be neither a realistic modeling of device aging nor a suitable one, due to the lack of definition of a 'permanent' drift. A multi-polarity trapping, as observed for the nMOS device in the used high-κ metal gate technology,

makes it even more difficult to measure maximum degradation levels occurring during the complex relaxation characteristic. As a first approach, I propose to consider and distinguish device degradation similar to the preceding investigations:

- 'Online'-degradations without any relaxation occurred,
- drifts after a stress period and relaxation with short time constants in relation to timings of the used circuitry, and
- drifts due to long term relaxation components in the product lifetime region or typical off-state periods.

A more detailed investigation for critical analog circuit blocks like open loop amplifiers or comparators can be performed with an accurate relaxation behavioral model as given in section 3.5.3.

Aging Effect Variations

Comparing figures 4.22 and 4.24 already shows that process or layout dependent variations in the threshold voltage V_{th} are dominant with respect to effect variations in the aging induced drifts ΔV_{th}. To illustrate the statistical data for the investigated aging scenarios, table 4.1 depicts means, upper and lower absolute deviations of the virgin threshold voltages as well as the aging induced drifts for the most stable 'Annealed' states. For comparison, all values are normalised to the virgin V_{th}. Due to a systematic layout dependent 'well proximity effect', V_{th} variations for the nMOS test circuit are higher than those for the pMOS counterpart. The high absolute drift $\Delta V_{th,HL}$ for the nMOS **HL** test also increases its deviations, which are significantly higher than for the pMOS counterpart. As the relation $\frac{D}{(\overline{X})}$ shows similar values for both device types, the same area dependent averaging behavior can be deduced. This also reveals that the built-in systematic V_{th} variation seems to have minor impact on the degradation itself and its variation. For the **AL** stress scenario, relative nMOS variations seem to be even worse

nMOS	$\overline{X}$ in $\%V_{th}$	D^{max} in $\%V_{th}$	D_{min} in $\%V_{th}$
V_{th}	100	0.54	-0.60
$\Delta V_{th,HL}$	9.04	0.13	-0.18
$\Delta V_{th,AL}$	-5.41	0.17	-0.15
pMOS	$\overline{X}$ in $\%V_{th}$	D^{max} in $\%V_{th}$	D_{min} in $\%V_{th}$
V_{th}	100	-0.23	0.24
$\Delta V_{th,HL}$	1.59	-0.03	0.03
$\Delta V_{th,AL}$	0.25	-0.02	0.03

Table 4.1: Comparison of threshold voltage and aging induced drift variations: mean values, upper and lower maximum deviations in % of virgin circuit V_{th}

than for the **HL** mode aging. Due to the measured minor drifts for pMOS in **AL** mode also the induced variations are small.
As a main result this study revealed that induced variations due to aging play a negligible role for minor drifts on 'analog size' devices. However, for large drifts reaching the 10% V_{th} region, tab. 4.1 shows that induced variations can reach the magnitudes of process variations, although the large device area fulfills defect averaging. Especially for cases of large aging drifts in combination with limited area consumption, aging induced variations can get significant and have to be considered according to [63]. Nevertheless, I expect degradation induced variations under symmetric stress conditions to be of minor importance for future analog circuit designs. In fact, especially in the analog circuit regime variations due to asymmetric voltage stress will overcome effect and process variations.

Measurement to Model Correlation

Fig. 4.25 depicts an overall summary of the measured degradation results from the previous sections. It shows mean values of the measured threshold voltages $V_{th,i}$ of the cell

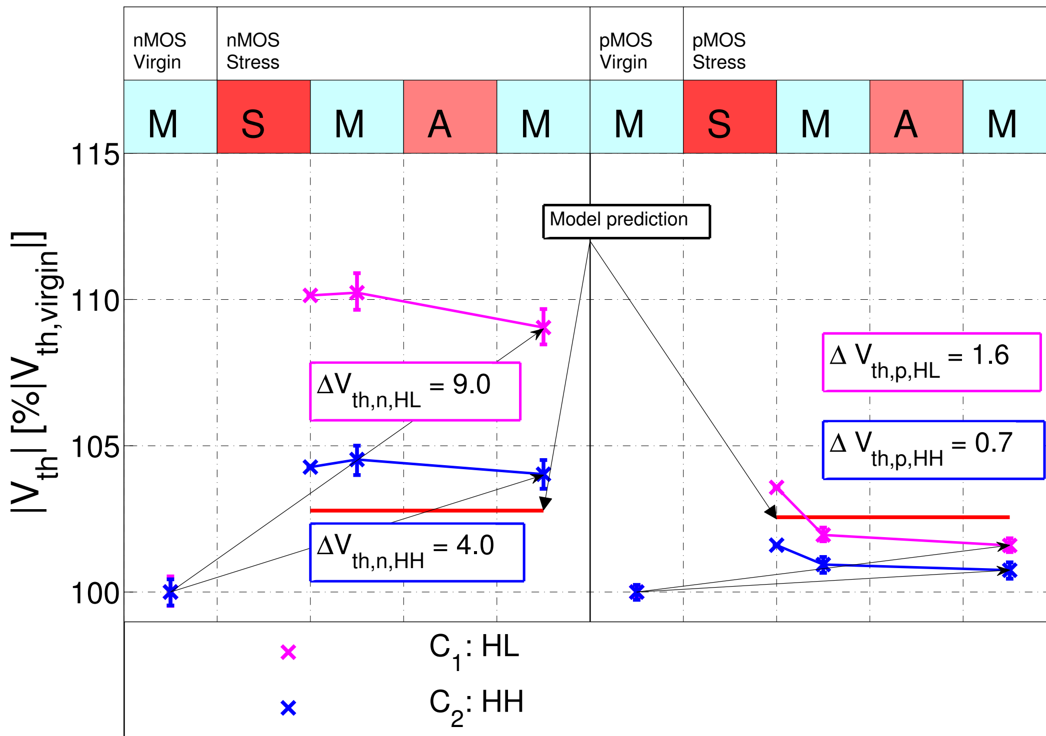

Fig. 4.25: Measured threshold voltage V_{th} behavior of the nMOS and pMOS test circuits for HL and HH operation stress for MP/EOL use case and corresponding degradation evaluated by the prediction model.

array and upper and lower deviations for the nMOS and pMOS test circuits. The processed stress sequence from sec. 4.2.3 is given on top of the graph. The left side of the graph shows the aging behavior of the nMOS and the right side the one of the pMOS test circuit. For comparison reasons, V_{th} for the nMOS and the pMOS are normalised to the corresponding mean V_{th} of the 'Virgin' test circuit. Besides the known stress test in **HL** (deep triode region) operation, also results for a **HH** (saturation region) operation stress are given. For this test, Gate-Source stress bias voltages are equal for both scenarios, only the Drain-Source voltage during stress is adjusted. For the **HL** and **HH** operation state the 1-dimensional aging prediction model in (3.6) evaluates one single degradation value that is also marked in fig. 4.25.
The comparison of the 'Online' degradation at the end of the stress period with the 'Aged' and the 'Annealed' values illustrates the general longterm recovery behavior. The given ΔV_{th} values represent evaluated drifts from the most stable 'Annealed' value compared to the 'Virgin' one. Comparing degradation induced ΔV_{th} values of the **HL** and **HH** scenarios, reveal for both device types a deviance of more than a factor of two whether the device is stressed in triode region or in saturation. Here, the prediction model provides only one value. The bad matching of the measurement with the prediction model for the nMOS/PBTI degradation can be related to differing development states of the hardware used for this study and for the degradation model extraction. Contrary to the nMOS/PBTI, the pMOS/NBTI prediction is in line with the measurement. Comparing the two stress scenarios, the general recovery behaviors of the induced drifts are not significantly changed and reveal a large variation of the degradation values over recovery time. Here, a main drawback of the prediction model can be seen: besides the insufficient degradation prediction ability dependent on the device operation region, it is further not clear which state of effect recovery is mapped by the model. Of course, this depends on the measurement process to extract the prediction model parameters, which is not standardized. Complex recovery behavior, as could be seen for the nMOS/PBTI makes characterisation measurement even more challenging to meet the worst case point - the maximum occurring parameter drift for a given circuit and timing (e.g. clocking, bandwidth,...). Here, new standards for reliability characterisation have to be developed to guarantee at least a worst case prediction. Even more, a reproduction of the effect recovery is not supported by the simple prediction model in (3.6), but will occur in real circuit operation. For proper circuit reliability studies, new approaches for a more accurate modeling and prediction will be needed for the arising device aging topic.

4.2.5 Advanced Stress Test Evaluation

To investigate further analog related properties of aging effects and to treat the open questions from sec. 4.2.1, the stress sequence of the previous sections is used and repeated several times with individual stress conditions. Obtained results are presented in normalized and condensed graphs according to fig. 4.25.

Effect Saturation

To investigate in detail the general BTI property that degradation shows a saturation behavior, the stress sequence from sec. 4.2.3 is repeated with the equivalent MP/EOL stress condition for two times. The obtained measurement results for the nMOS test circuit are depicted in fig. 4.26 and for the pMOS test circuit in fig. 4.27. For comparison reasons, stress measurements for both device types are conducted for the **HL** and **HH** operation use case. The plots also show the results provided by the prediction model. The included ΔV_{th} values derived from the most stable measured threshold voltages after the annealing step generally reveal the saturation of the longterm, permanent parts of the degradation induced V_{th} drifts. In the stress scenarios of both device types, the fast recovering parts are similar in the first and the second step and do not show any saturation behavior. In contrast to the longterm, permanent defects, fast relaxing ones recover in the mean time between the stress periods and are again triggered in the second stress period, leading to the measured degradation behavior. As can be seen in fig. 4.26 and 4.27, the general saturation behavior is also supported by the BTI prediction model in (3.6) via the sub-linear dependency of stress time.
This general saturation property of BTI induced device degradation can be beneficially

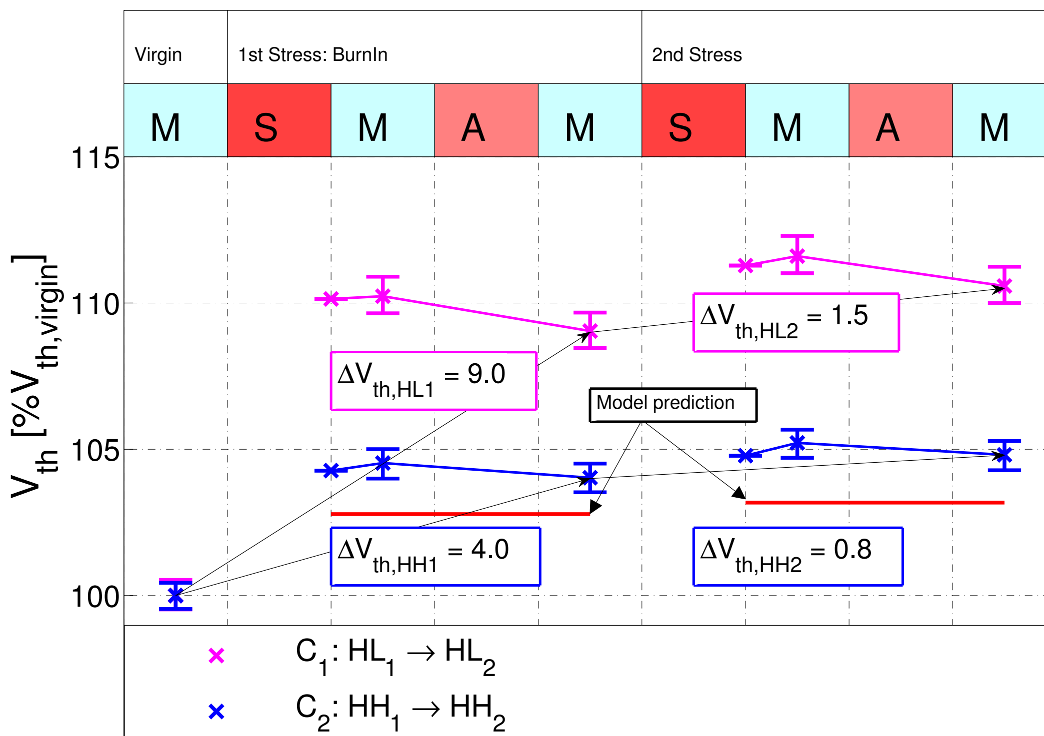

Fig. 4.26: PBTI effect saturation behavior for the nMOS test circuit by application of two times the equivalent MP/EOL stress sequence for HL and HH operation.

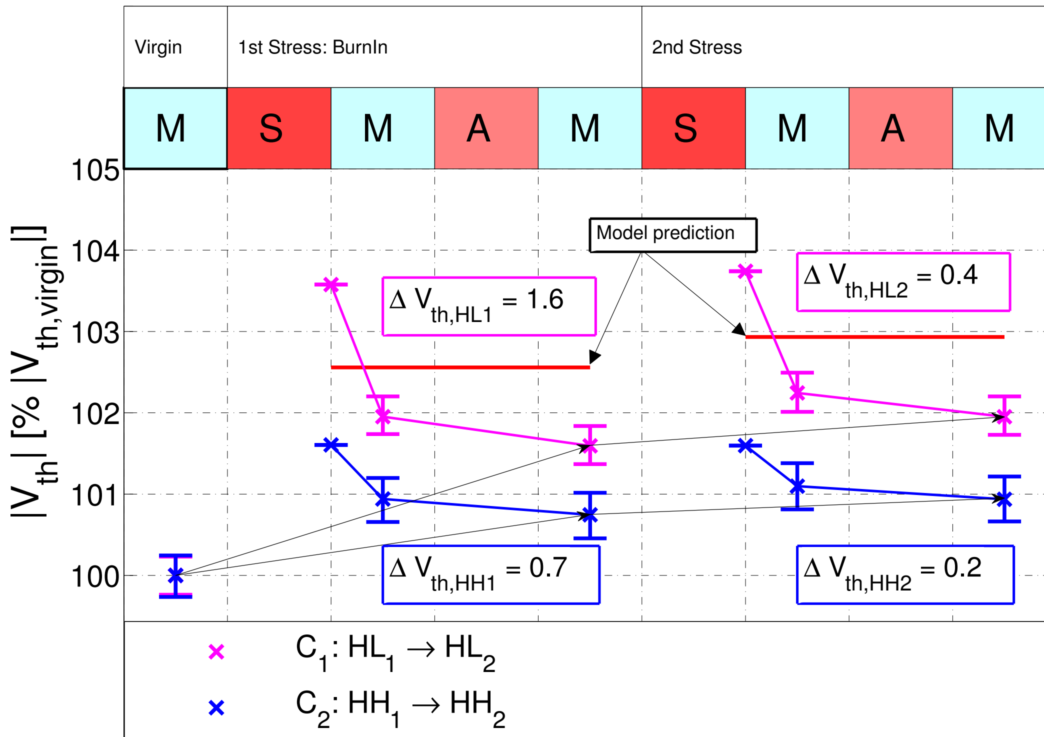

Fig. 4.27: NBTI effect saturation behavior for the pMOS test circuit by application of two times the equivalent MP/EOL stress sequence for HL and HH operation.

used on circuit level to generate a pre-degradation via a controlled 'Burn-In'. Therefore, the 1st stress sequence is also named as 'Burn-In' in fig. 4.26 and 4.27. Due to the pre-degradation, further uncontrollable drifts during circuit operation occur with small magnitudes. So, a passive suppression of device aging could be performed.

Accumulation Mode Effect Recovery

An enhancement of the two stress step approaches from fig. 4.26 and 4.27 is to expand the test with a 3rd and a 4th sequence. With the 3rd sequence an active regeneration of induced degradation via a stress step in **AL** mode is explored and degradation behavior after this regeneration, again in **HL** mode is studied with the 4th sequence. For comparison, a second test performing an **AL** operation stress from the 'Virgin' followed by a **HL** stress is also shown. Measurement results for the nMOS test circuits are depicted in fig. 4.28. On sample C_1, the 4 step stress sequence is applied, while C_3 shows the behavior applying only the last two stress periods. $\Delta V_{th,C1,HL1}$ and $\Delta V_{th,C1,HL2}$ show the well known effect saturation behavior from fig. 4.26 for an application of two times the equivalent **HL** MP/EOL stress case in inversion mode. After this treatment, the

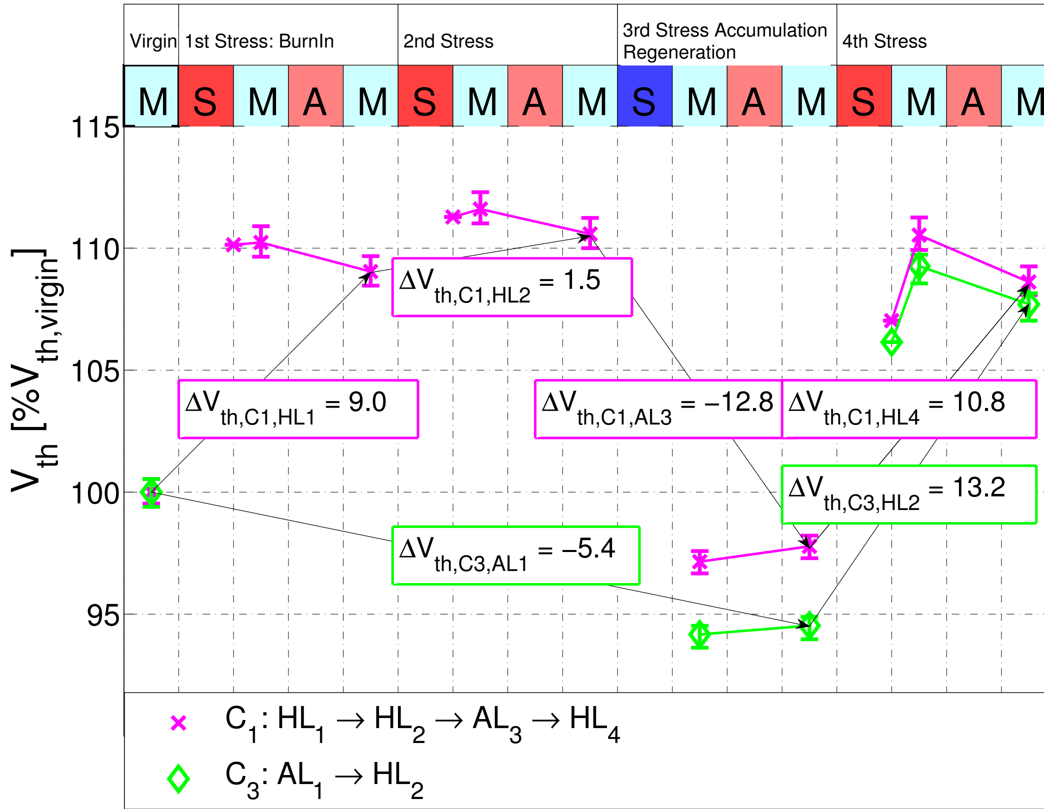

Fig. 4.28: Active degradation regeneration ability via AL operation for the nMOS test circuit. Applied stress conditions correspond to the equivalent MP/EOL use case.

3rd stress step is applied with corresponding **AL** MP/EOL stress conditions. $\Delta V_{th,C1,AL3}$ reveals a full regeneration of the induced drifts from step HL_1 and HL_2. Even more, a further ΔV_{th}-drift in the opposite direction, going below the threshold voltage of the virgin sample is induced by the **AL** stress. The 'Annealing' step also reveals recovery of the **AL** operation mode induced drifts. Applying again **HL** mode stress, as in the 4th step, shows a drift back to V_{th}-levels before the **AL** mode stress. A large absolute drift is induced with $\Delta V_{th,C1,HL4} > \Delta V_{th,C1,HL1}$ and also recovery behavior between the 'Online', 'Aged' and 'Annealed' recovery state has generally changed. As already expected from the results in sec. 4.2.4, applying **AL** stress to a 'Virgin' sample, as given for C_3, shows a negative drift of the threshold voltage $\Delta V_{th,C3,AL1}$. A following **HL** mode stress induces a drift $\Delta V_{th,C3,HL2}$ in opposite, positive direction with a large magnitude. Also here, a changed recovery behavior, compared to $\Delta V_{th,C1,HL1}$ and $\Delta V_{th,C1,HL2}$ can be observed.
The corresponding investigation for the pMOS test circuit is depicted in fig. 4.29. Although, **AL** stress in the study in sec. 4.2.4 showed for the equivalent MP/EOL case only a small impact on V_{th} and a drift in the same direction as in classic inversion mode stress ($\Delta V_{th,C3,AL1}$), **AL** stress after a **HL** sequence also reveal an active regeneration ability ($\Delta V_{th,C1,AL3}$). Stressing again in **HL** operation, shows an active regeneration of the **AL**

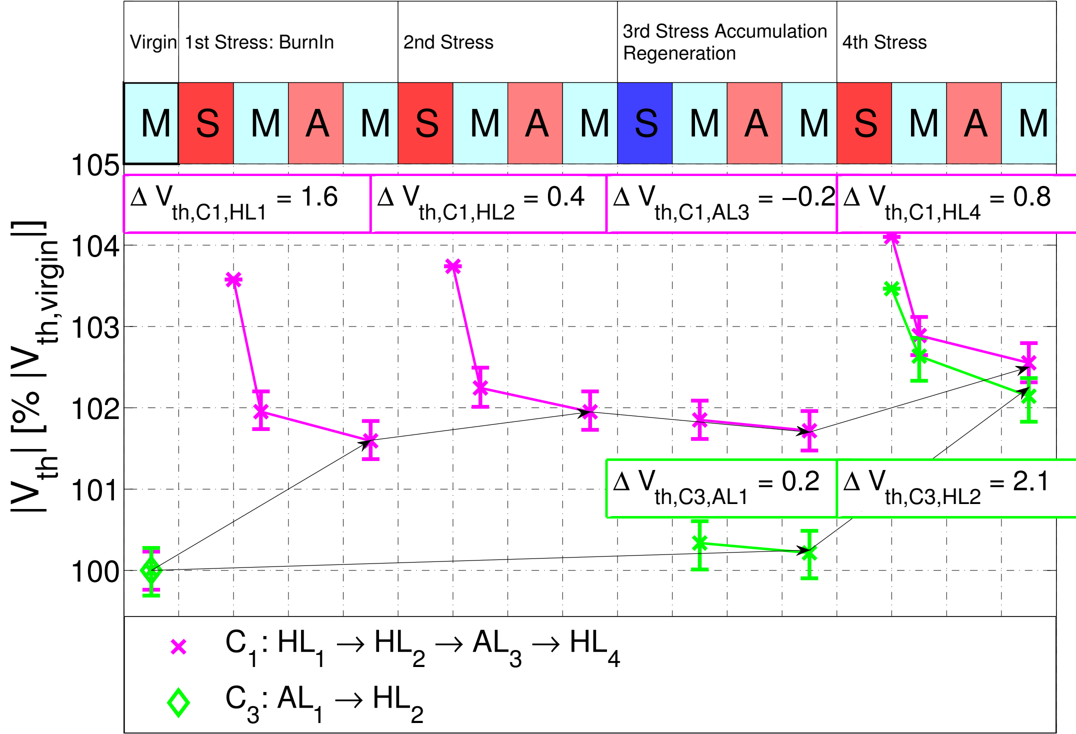

Fig. 4.29: Active degradation regeneration ability via AL operation for the pMOS test circuit. Applied stress conditions correspond to the equivalent MP/EOL use case.

mode induced defects ($\Delta V_{th,C1,HL1}$ vs. $\Delta V_{th,C3,HL2}$), but also impact from the 'Burn-In' sequence, as $\Delta V_{th,C1,HL1} > \Delta V_{th,C1,HL4}$. A general change in effect recovery behavior in the 4th step, as for the nMOS test circuit, cannot be seen.
These stress tests reveal a general regeneration ability, recovering inversion mode induced V_{th}-drifts via an operation in accumulation mode to some extent. The regeneration properties differ in magnitude for the used device types, which might be due to different stress voltages during the accumulation period. Stress conditions were derived according to the MP/EOL use case and prediction models were used from the device counterpart: for nMOS the pMOS/NBTI model and for pMOS the nMOS/PBTI model. Besides the regeneration ability, accumulation mode stress further generates defects, also recovering and inducing a transient V_{th}-drift behavior. This regeneration ability is not a universal remedy, as V_{th}-drifts in inversion operation after the accumulation mode treatment are of large magnitudes ($\Delta V_{th,C1,HL4}$ and $\Delta V_{th,C3,HL2}$). It further partially removes effect saturation from 'Burn-In' treatments ($\Delta V_{th,C1,HL2}$ vs. $\Delta V_{th,C1,HL4}$ and $\Delta V_{th,C3,HL2}$ vs. $\Delta V_{th,C1,HL4}$) and hence a possible degradation suppression. Especially for the nMOS test circuit a significant change of the general effect recovery behavior could be seen, that is further related to the accumulation mode treatment. As can be seen on the error bars in

fig. 4.28 and 4.29, for both test circuits the general variability of the threshold voltages did not significantly change for all test sequences. This can be related to the large area defect averaging and further reveals the minor impact of degradation induced variations on analog devices under equal stress conditions.
A possible application of accumulation mode regeneration in circuits has to be considered with care. Due to expected large V_{th}-drifts in both directions it proves to be unfavorable during temporary calibration sequences. To incorporate accumulation mode during the common circuit operation for active suppression of general device aging via the instantaneous effect recovery might be a promising option. But also here, care has to be taken regarding the circuits' signal distortion due to effect recovery. Furthermore, a very promising approach is to perform a passive aging suppression via a controlled 'Burn-In'. Of course, accumulation mode operation has to be excluded. As this suppression ability only covers the longterm permanent drifts, fast recoverable parts will still occur and have to be considered during circuit design.

4.3 Summary

In this chapter significant differences in device aging for digital and analog circuits were investigated from a general point of view. For analog circuits, the usage of large area devices with high gate lengths reduces the most stress relevant operation mode to the deep triode region - here, a high V_{GS} and a low V_{DS} form a BTI stress condition. HCI effects are mostly suppressed by the convenient device dimensioning, and are only an issue for special cases. On the contrary, for digital circuits HCI effects play an important role. Complex analog operation states like a possible accumulation mode during circuit standby, open new possibilities of device degradation states, which are not covered by any reliability prediction methods yet.
A case study on the aging of a nMOS varactor revealed that device degradation impacts its tuning range but with tolerable effect for operation in the allowed voltage regime. The individual derivation of an analytical circuit behavior model in combination with the aging model equation provides a powerful opportunity to investigate in detail a circuit's aging behavior towards stress conditions and allows to derive advanced concepts or predictions for future technologies. Following circuit level studies in this work are established on this approach of analytical circuit behavior modeling.
Important analog circuit related aging properties, which are not or only partially covered by the prediction model equations, were studied for the found worst case operation scenario in deep triode region. Here, a custom test circuit implementation in the 32nm high-κ metal gate CMOS technology [91] and an individual stress test assembly was used. Device inversion mode operation induced degradation generally lead to a weakening of the device characteristic. The mapping of the BTI degradation in a threshold voltage drift ΔV_{th} proves to be a suitable and accurate parameter. Device aging in accumulation mode shows for the used technology a significant enhancement for the nMOS device and a small weakening of the I_D vs. V_{GS} characteristic for the pMOS device.
Comparing ΔV_{th} results of the simple, 1-dimensional BTI model equation with the measured degradations reveal a difference of a factor of more than 2, whether the device was

stressed in deep triode region or in saturation region. Here, the model only provides one value for both cases. As BTI degradation effects are strongly process dependent, model to hardware correlation depends on the equal state of process development. Occurring effect recovery after stress application leads to transient drifts in V_{th} that are not considered by the prediction model. Here, novel modeling approaches according to [48, 95, 85] have to be introduced. Furthermore, it is not clear which state of recovery is predicted by the model equation. To cover the worst case scenario, the maximum arising ΔV_{th} should be mapped. Here, a standardised model extraction method is necessary. As a first approach for an easy and detailed aging prediction, characteristic states of relaxation should be considered in circuit reliability investigations.

The study further revealed, that induced variations due to degradation effects under equal stress conditions are generally small and mostly negligible for analog devices. This can be related to the large device area defect averaging for analog size MOSFETs. Anyhow, for large absolute drifts, induced variations can enter the regime of process variations. Nevertheless, an asymmetric voltage stress is considered to be much more critical to significantly change device matching.

Further stress tests revealed that effect saturation occurs after a 'Burn-In' procedure. This behavior can also be mapped by the predictive model equation. Basing on this saturation ability a passive aging suppression concept can be developed. The effect saturation incorporates only the longterm, permanent parts of the V_{th}-drift. The fast, recoverable parts are not affected by saturation and will arise with similar magnitudes.

The active regeneration via accumulation mode stress generally recovers induced degradations to some extent, but further induces additional defects. Those can change the general recovery behavior after another inversion mode operation. A further drawback is the large V_{th}-drift in both directions - for the generation during inversion mode and the regeneration via accumulation state. So, this approach is not suitable for a circuit built-in calibration, regenerating from time to time the induced degradation. However, a potential option for a degradation-free circuit design would be an inclusion of device accumulation mode during the circuit's signal processing, leading to an instantaneous regeneration during operation.

From these investigations on general analog related degradation topics two publications, partially reflecting the found results, were released in [96] and [97].

Chapter 5

Current Mirrors and Reference Circuits

5.1 Basics

Current mirror circuits are one of the most fundamental analog circuit topologies. This circuit block is commonly used as biasing circuit, but also for signal processing via their ability to *copy* a current. Reference circuit blocks like *current* or *voltage* references should provide stable quantities for the biasing of further circuit blocks. Here, attention has to be turned on the reliable start-up. The following studies provide a general view on the behavior and sensitivity of the basic current mirror with respect to device degradation occurring during operation. Device aging relevance for reference circuits is condensed in a case study on an exemplary *self-biasing* current reference.

5.2 Current Mirror Fundamentals

5.2.1 Circuit Topology

Fig. 5.1 depicts the fundamental topology of a current mirror implementation in a nMOS and pMOS version. The common device operation mode in a current mirror is the *saturation* region, as here output devices nearly act as a high ohmic controlled current source. In this mode, perturbations from the output, in this case the Drain terminal of $\mathbf{M_{copy}}$, are minimized and device current I_{copy} is only controlled by the input, here the sense node. Device $\mathbf{M_{sense}}$ provides via the diode connection a $V_{GS,s}$ dependent on the current I_{sense} and ensures due to $V_{GS,s} = V_{DS,s}$ the operation in saturation region. As the I_{sense}-dependent $V_{GS,s}$ also drops at $\mathbf{M_{copy}}$, a I_{sense} related current flows through $\mathbf{M_{copy}}$ with minor perturbations from the output node as long as $\mathbf{M_{copy}}$ also operates in saturation region. This has to be ensured by limiting the voltage headroom for $V_{DS,c}$, that has to be supported by the exterior circuitry. Of course, also more sophisticated structures are used in todays analog CMOS circuits, but for simplicity and to provide universal results,

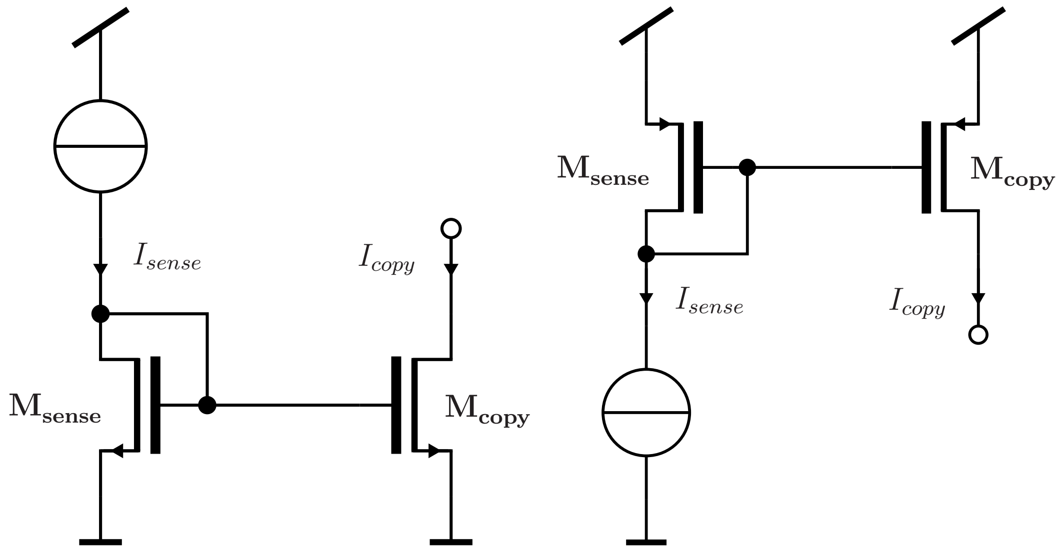

Fig. 5.1: Schematic of a basic current mirror circuit implementation in nMOS and pMOS version

investigations are performed on the basic topologies given in fig. 5.1.

5.2.2 Design Fundamentals

For current mirrors the most important design constraint is the accurate duplication of the reference current. However, I_{copy} can be disturbed by general device mismatch and SCE (Short Channel Effects) [98]. Device mismatch can be induced by layout imperfections, process variations as random dopant fluctuations and also by device degradation. However, global variations play a minor role, as parameter mismatch affecting both devices are canceled by the circuit topology itself. Hence, degradations affecting both devices with the same magnitude are also canceled. The most important short channel effect is the CLM (Channel Length Modulation) resulting in a finite resistive behavior on the Drain side and a resulting impact of $V_{DS,c}$ on the mirrored current I_{copy}.
To reduce device mismatch on layout level, lots of techniques for optimum alignments are evolved and should be considered by the circuit designer [90]. Regarding process variations, the circuit designer can counteract by spending device area for an improved dopant averaging. To reduce the impact of CLM, devices have to be built with long gate lengths L as CLM reduces with $\frac{1}{L}$, which also results in large area devices. Further sources of interference, as device flicker noise, also reduce with device area.
Typically used devices in current mirrors are of large gate length and hence of large area. On the other hand, for the application of signal propagation, input capacitance of the current mirror limits the speed of the circuit. Here, corresponding trade-offs in the device dimensioning during the circuit design have to be found.

5.2.3 Operation Conditions

The typical operation condition of a current mirror is the biasing of the sense device $\mathbf{M_{sense}}$ with few tens or hundred millivolts above V_{th}, that can be simplified and reduced to $V_{GS,s} \approx \frac{V_{DD}}{2}$ for advanced CMOS technologies due to the low supply voltage (see sec. 4.1.2). Also output voltage $V_{DS,c}$ at the copy device $\mathbf{M_{copy}}$ ideally operates around $\frac{V_{DD}}{2}$. Under this operation condition, both devices are symmetrically biased and occurring degradation, that will be very small, is canceled by the topology itself as it equally arises on $\mathbf{M_{sense}}$ and $\mathbf{M_{copy}}$. The aging relevant worst case scenarios arise during an asymmetric operation of this structure, that could also occur during circuit operation. Those can be summarized to the following cases:

- **MH:**[1] worst case scenario during on-state operation with full swing at the output $V_{DS,c} = V_{DD}$ and $V_{GS,s} = \frac{V_{DD}}{2}$,
- **LH:**[1] worst case scenario for the off-state operation of the current mirror, but with full swing at the output $V_{DS,c} = V_{DD}$ and $V_{GS,s} = 0V$ and
- **ML:**[1] a worst case state, where the circuit is not working as a current mirror anymore as $\mathbf{M_{copy}}$ has entered the triode region operation $V_{DS,c} \approx 0V$ and $V_{GS,s} = \frac{V_{DD}}{2}$.

Another aging relevant mode would be the disconnection of the supply voltage for the pMOS or the ground reference for the nMOS $\mathbf{M_{copy}}$ as a partially power down mode. Here, $\mathbf{M_{copy}}$ can be driven into accumulation mode, that might, according the findings in chapter 4, significantly change the V_{th} matching of the device pair. Due to the missing accumulation mode prediction equation, a consideration of this scenario is omitted in the following study, but should be investigated in future work. As a general suggestion, this type of partial shut-down should be omitted by the circuit designer with respect to the unpredictable degradation behavior.

5.3 Current Mirror Aging Model

5.3.1 Analytical Mismatch Derivation

Basing on MOSFET device equations an analytic aging behavioral model can be derived to describe the impact of device aging during worst case operation scenarios of a current mirror circuit. This analytic approach further enables to compare degradation contributions with further relevant mismatch sources like local parameter variations and provides a universal basis for a classification.
Starting with the device equations for $\mathbf{M_{sense}}$ and $\mathbf{M_{copy}}$ under consideration of device

[1] $V_{GS,s}V_{DS,c}$ voltages - L:low, M:moderate, H:high

aging and process variations,

$$I_{sense} = \frac{1}{2}\mu C_{ox}\Big(\frac{W}{L}\Big)_s(1+\lambda V_{DS,s})$$
$$(1-\Delta I_{D,s,CHCI}-\Delta I_{D,s,NCHCI})$$
$$(V_{GS,s}-V_{th}-\Delta V_{th,s,BTI}-\Delta V_{th,s,CHCI}+\frac{1}{2}\Delta V_{th,PV})^2, \tag{5.1}$$

$$I_{copy} = \frac{1}{2}\mu C_{ox}\Big(\frac{W}{L}\Big)_c(1+\lambda V_{DS,c})$$
$$(1-\Delta I_{D,c,CHCI}-\Delta I_{D,c,NCHCI})$$
$$(V_{GS,c}-V_{th}-\Delta V_{th,c,BTI}-\Delta V_{th,c,CHCI}-\frac{1}{2}\Delta V_{th,PV})^2, \tag{5.2}$$

with $\Delta I_{D,CHCI}$ and $\Delta I_{D,NCHCI}$ the corresponding HCI contributions to the current degradation, $\Delta V_{th,BTI}$ and $\Delta V_{th,CHCI}$ the BTI and CHCI contribution to the threshold voltage drift and $\Delta V_{th,PV}$ the expected V_{th} mismatch due to random dopant fluctuations. For simplicity, this model considers process variations only in a variation of the threshold voltage. The current mirror circuit configuration provides

$$V_{DS,s} = V_{GS,s} = V_{GS,c}. \tag{5.3}$$

Transformation of (5.1) results in

$$V_{GS,s} = \sqrt{\frac{2I_{sense}}{\mu C_{ox}(\frac{W}{L})_s(1+\lambda V_{DS,s})(1-\Delta I_{D,s,CHCI}-\Delta I_{D,s,NCHCI})}}$$
$$+V_{th}+\Delta V_{th,s,BTI}+\Delta V_{th,s,CHCI}-\frac{1}{2}\Delta V_{th,PV}). \tag{5.4}$$

Including (5.4) in (5.2) reduces to

$$I_{copy} = \frac{1}{2}\mu C_{ox}\Big(\frac{W}{L}\Big)_c$$
$$\Bigg(\sqrt{\frac{2I_{sense}}{\mu C_{ox}\left(\frac{W}{L}\right)_s(1+\lambda V_{DS,s})(1-\Delta I_{D,s,CHCI}-\Delta I_{D,s,NCHCI})}}$$
$$+\Delta V_{th,s,BTI}+\Delta V_{th,s,CHCI}-\Delta V_{th,c,BTI}-\Delta V_{th,c,CHCI}-\Delta V_{th,PV}\Bigg)^2$$
$$(1+\lambda V_{DS,c})(1-\Delta I_{D,c,CHCI}-\Delta I_{D,c,NCHCI}). \tag{5.5}$$

With the following approximation resulting from linearisation in the operating point

$$(V_{GS,s}-V_{th})|_{OP} = \sqrt{\frac{2I_{sense}}{\mu C_{ox}\left(\frac{W}{L}\right)_s}}\Bigg|_{OP}, \tag{5.6}$$

and simplifications (CLM and HCI aging contributions $<< 1$, PV and aging induced V_{th} drifts are small)

$$\sqrt{(1+\lambda V_{DS,s})(1-\Delta I_{D,s,CHCI}-\Delta I_{D,s,NCHCI})} \approx 1 \qquad \text{and} \tag{5.7}$$
$$(\Delta V_{th,s,BTI}+\Delta V_{th,s,CHCI}-\Delta V_{th,c,BTI}-\Delta V_{th,c,CHCI}-\Delta V_{th,PV})^2 \approx 0, \tag{5.8}$$

as linear terms in the equation dominate, eq. (5.5) would reduces to the well known mismatch equation for current mirror circuits. Here, CLM, process variations [90] and device aging is considered:

$$\frac{I_{copy}}{I_{sense}} \approx \frac{\left(\frac{W}{L}\right)_c (1+\lambda V_{DS,c})(1-\Delta I_{D,c,CHCI}-\Delta I_{D,c,NCHCI})}{\left(\frac{W}{L}\right)_s (1+\lambda V_{DS,s})(1-\Delta I_{D,s,CHCI}-\Delta I_{D,s,NCHCI})} \left(1-\frac{2}{V_{GS,s}-V_{th}}\Big|_{OP} \cdot (\Delta V_{th,s,BTI}+\Delta V_{th,s,CHCI}-\Delta V_{th,c,BTI}-\Delta V_{th,c,CHCI}-\Delta V_{th,PV})\right). \tag{5.9}$$

Including the model equations for the degradation mechanisms in (3.6), (3.10) and (3.12), an analytic prediction model for the current mirror aging behavior, dependent on its operation mode, is provided. Further inclusion of corresponding statistical data for the CMOS process enables to predict $\Delta V_{th,PV}$ and offers a comparison basis between process variations and aging induced mismatch. In doing so, the model evaluates the impact of each V_{th} mismatch source as a function of the operation point $V_{GS,s}$ by the term $\frac{2}{V_{GS,s}-V_{th}}\Big|_{OP}$. Of course, aging induced mismatch contributions are evaluated for their individual aging scenario according to the found worst case operation states in sec. 5.2.3. The following investigation neglects the impact of CLM as it proves to be incompatible with the presentation of mismatch contributions *after* worst case operation, as the CLM component provides the mismatch *during* an asymmetric biasing. For completeness the further used model equation including the aging relevant voltage and dimension sensitivities is given in (5.10)

$$\frac{I_{copy}}{I_{sense}} \approx \frac{\left(\frac{W}{L}\right)_c (1-\Delta I_{D,c,CHCI}(V_{DS,c},L)-\Delta I_{D,c,NCHCI}(V_{DS,c},L))}{\left(\frac{W}{L}\right)_s (1-\Delta I_{D,s,CHCI}(V_{DS,s},L)-\Delta I_{D,s,NCHCI}(V_{DS,s},L))} \left(1-\frac{2}{V_{GS,s}-V_{th}}\Big|_{OP} \cdot \Big(\Delta V_{th,s,BTI}(V_{GS,s})+\Delta V_{th,s,CHCI}(V_{DS,s},L) - \Delta V_{th,c,BTI}(V_{GS,c})-\Delta V_{th,c,CHCI}(V_{DS,c},L)-\Delta V_{th,PV}(W,L)\Big)\right). \tag{5.10}$$

5.3.2 Model Evaluation

As can be derived from the model equation (5.10), sensitivity towards drifts in threshold voltage further depends on the chosen operating point according to $\frac{2}{V_{GS,s}-V_{th}}\Big|_{OP}$. An increase of the bias level $V_{GS,s}$ would reduce the impact of threshold voltage drifts, but also reduces the output voltage headroom for keeping device $\mathbf{M_{copy}}$ in saturation. Choosing the correct operating point for the current mirror is strongly application dependent and has to be determined by the designer. The following model evaluation assumes an operating point of the current mirror of $V_{GS,s}-V_{th} \approx 150mV$ above threshold to perform a

general and commonly used approach [90]. Gate width $W_s = W_c$ and length $L_s = L_c$ is assumed to be equal with a typically width in the region of several microns.
Another interesting fact, that was already mentioned in the previous sections is the cancellation of degradations, symmetrically occurring in the current mirror device pair, by the circuit topology itself. This can also be seen in eq. (5.10) for the BTI induced $\Delta V_{th,i,BTI}$ drifts. As stress voltage V_{GS} for both devices $\mathbf{M_{sense}}$ and $\mathbf{M_{copy}}$ is equal and BTI aging prediction (eq. (3.6)) only considers a V_{GS} dependency without respecting device operation region, equal BTI induced $\Delta V_{th,i,BTI}$ is predicted and drifts cancel. Another source of variation in the BTI aging of both devices can be excluded due to the large area defect averaging of the used devices, which was already observed in sec. 4.2.4. Hence, a custom consideration of individual, operation region dependent BTI aging via a correction factor according to the findings in sec. 4.2.4, whether the device operates in triode region or saturation during stress, is considered for the use case **ML** on device $\mathbf{M_{copy}}$. Expected process variations $V_{th,PV}$ are considered according to Pelgrom's law [99].
Fig. 5.2 compares major mismatch contributions according to eq. (5.10) after the **MH**

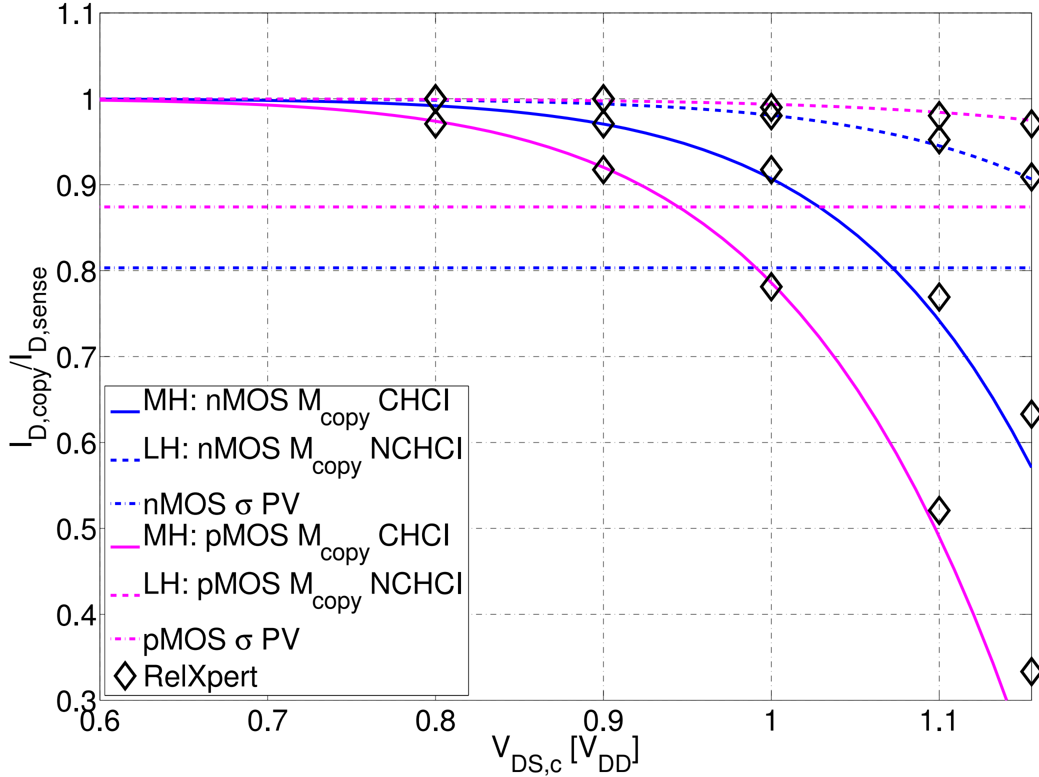

Fig. 5.2: Current mirror aging induced mismatch contributions after MH and LH, 10y, 125°C operation as well as expected 1σ process variation in dependence of MH/LH stress $V_{DS,c}$. Devices are assumed to provide minimum gate length $L = L_{min}$. Mismatch is evaluated in the common operation point with $V_{GS,s} - V_{th} \approx 150mV$

.

use case operation for 10y, 125°C in dependence of the stress voltage $V_{DS,c}$. The evaluation

bases on the 32nm high-κ metal gate technology [91] and is evaluated for the common $V_{GS,s} - V_{th} \approx 150mV$ operating point. Evaluation considers worst case dimensions, so devices of the current mirror are set to minimum gate lengths $L = L_{min}$. Prediction quality of the analytic model approach is proven by the consideration of selected aging scenarios via circuit simulations and RelXpert aging results in fig. 5.2. As can be seen, occurring CHCI degradation for the **MH** use case in $\mathbf{M_{copy}}$ significantly exceed the mismatch levels expected by a 1σ V_{th} process variation for sufficient high $V_{DS,c}$ for both device types. However, for the corresponding **LH** off-state use case occurring NCHCI contribution is minor even for high $V_{DS,c}$ and can be neglected for most of the operation cases. Corresponding

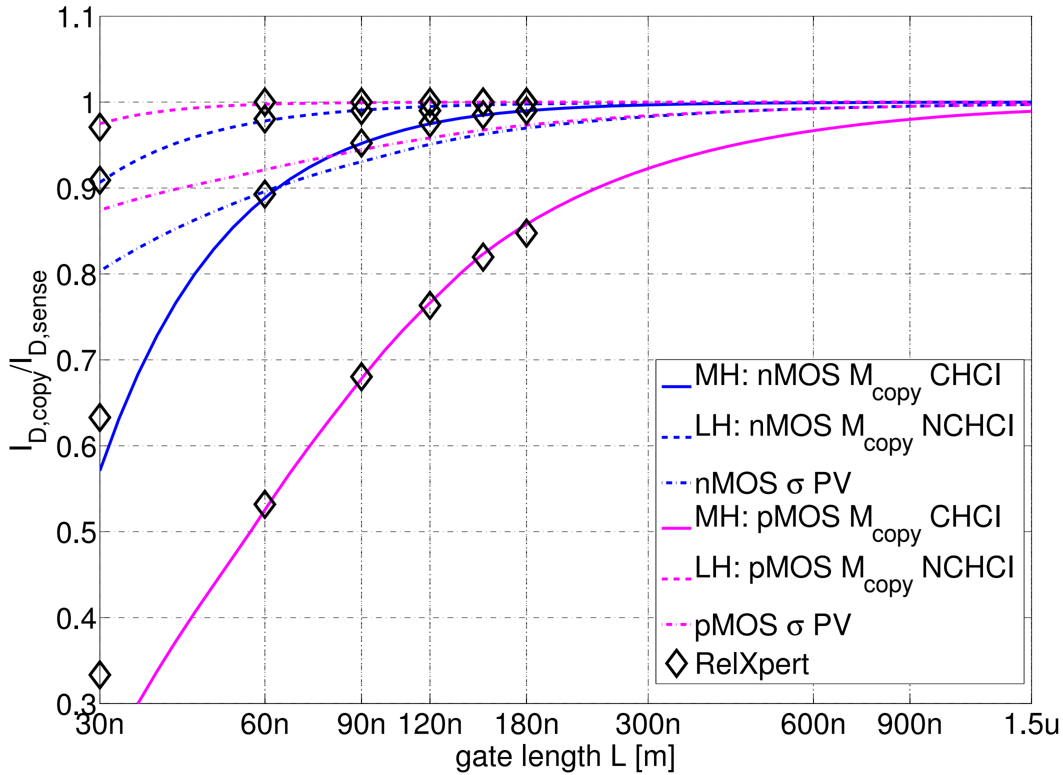

Fig. 5.3: Current mirror aging induced mismatch contributions after MH and LH, 10y, 125°C operation as well as expected 1σ process variation in dependence of device gate length L. MH/LH voltage stress is set to $V_{DS,c} = 1.155V_{DD}$. Mismatch is evaluated in the common operation point with $V_{GS,s} - V_{th} \approx 150mV$

.

behavior in dependence of the gate length L for $V_{DS,c} = 1.155V_{DD}$ is depicted in fig. 5.3. For the current mirror the increased gate length is accompanied by an analogous increase of device width W for proper and comparable operation. Mismatch contributions resulting from $\mathbf{M_{copy}}$ HCI aging and due to expected process variations decrease altogether with the larger device area. For the nMOS device CHCI contributions are major for minimum device lengths, but significantly decrease with increased L and fall below the 1σ PV limit for $L \approx 2 \cdot L_{min}$. For commonly used gate lengths around $L = 6 \cdot L_{min}$ CHCI

contributions are negligibly small and process variations dominate. This is different for the pMOS device in the used technology. Here, the CHCI accompanied LSHA (see sec. 3.4.2) keeps the pMOS/CHCI as the dominant mismatch source for all reasonable device lengths and significantly exceeds the level of the process variations. For the off-state **LH** state NCHCI contributions drastically decrease with increased gate length L and prove to be negligibly small for commonly used dimensions with $L \approx 6 \cdot L_{min}$. Here, process variations are the dominant mismatch source. For comparison, fig. 5.4 shows mismatch sources according to fig. 5.2, but with a commonly used gate length for current mirrors of $L = 6 \cdot L_{min}$. The HCI suppression technique to increase gate length proves to be a suitable method to limit CHCI and NCHCI effects over the whole $V_{DS,c}$ range. Only for the pMOS device in **MH** operation, the accompanying LSHA leads to significant CHCI contributions for high $V_{DS,c}$.

Fig. 5.5 shows mismatch sources due to device aging and 1σ process variations for the

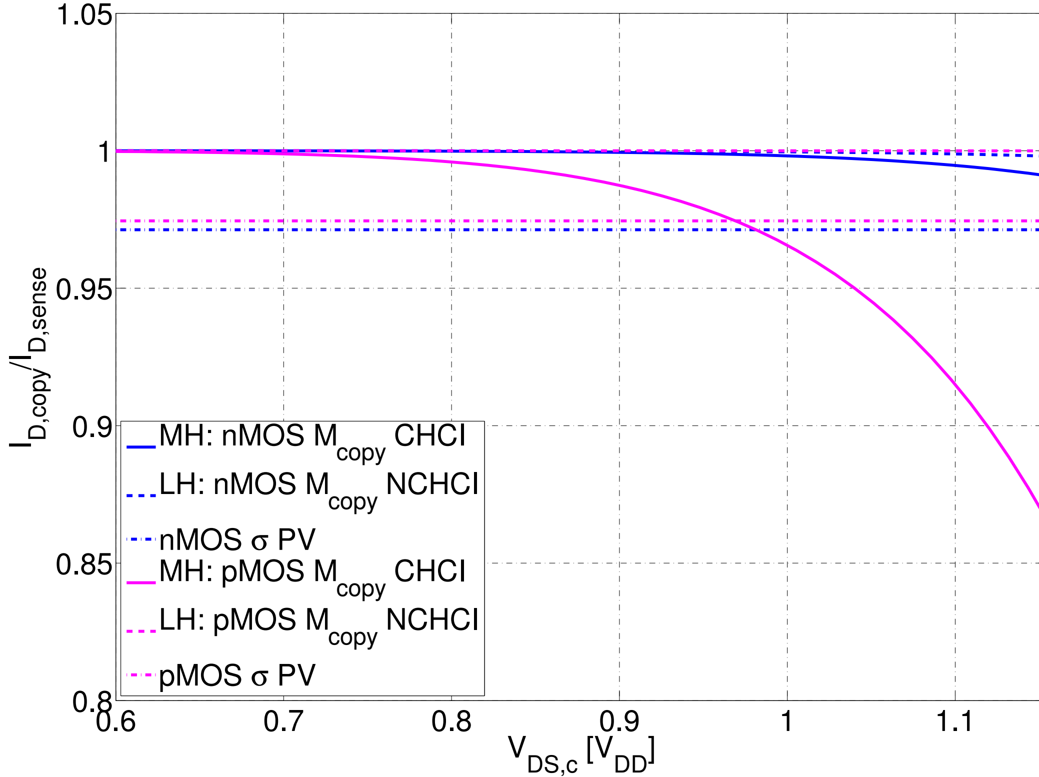

Fig. 5.4: Current mirror aging induced mismatch contributions after MH and LH, 10y, 125°C operation as well as expected 1σ process variation in dependence of MH/LH stress $V_{DS,c}$. Devices are assumed to provide commonly used gate length $L = 6 \cdot L_{min}$. Mismatch is evaluated in the common operation point with $V_{GS,s} - V_{th} \approx 150mV$

.

ML use case in dependence of the bias voltage $V_{GS,s}$. To cover typical current mirror dimensions, device lengths are set to $L = 6 \cdot L_{min}$. As BTI degradation for this special

use case is insufficiently well predicted by the BTI model equation (3.6), the correction factor derived in sec. 4.2.4 is used to consider the individual BTI aging of $\mathbf{M_{sense}}$ in saturation and $\mathbf{M_{copy}}$ in triode region. Here, a considerable mismatch contribution due to the asymmetric BTI degradation of $\mathbf{M_{sense}}$ and $\mathbf{M_{copy}}$ is observed, that even exceeds the contributions of the process variations for bias levels smaller than the nominal supply voltage $V_{GS,s} < V_{DD}$. Further circuit and RelXpert simulations are also omitted due to the insufficient BTI prediction. A very important fact is that the asymmetric BTI contribution can not be suppressed by spending larger device area, that beneficially counteracts mismatch contributions resulting from HCI and process variations. Especially pMOS device aging in $\mathbf{M_{sense}}$ is accompanied by a CHCI portion that counteracts the NBTI mismatch contribution. Nevertheless, typical $V_{GS,s}$ biasing is in the range of $V_{GS,s} \approx \frac{V_{DD}}{2}$, where occurring asymmetric BTI aging contributions are minor. For seldom cases, high $V_{GS,s}$ can occur and a significant mismatch contribution due to the asymmetric BTI aging would not be predicted by the simple BTI model equation (3.6). The same problem can arise for highly accurate current mirrors obtained via large area design. For this case a more complex 2 dimensional BTI model with $\Delta V_{th,BTI} = f(V_{GS}, V_{DS})$ is necessary. For all other studied stress cases, a 1-dimensional BTI aging consideration proved to be sufficiently accurate.

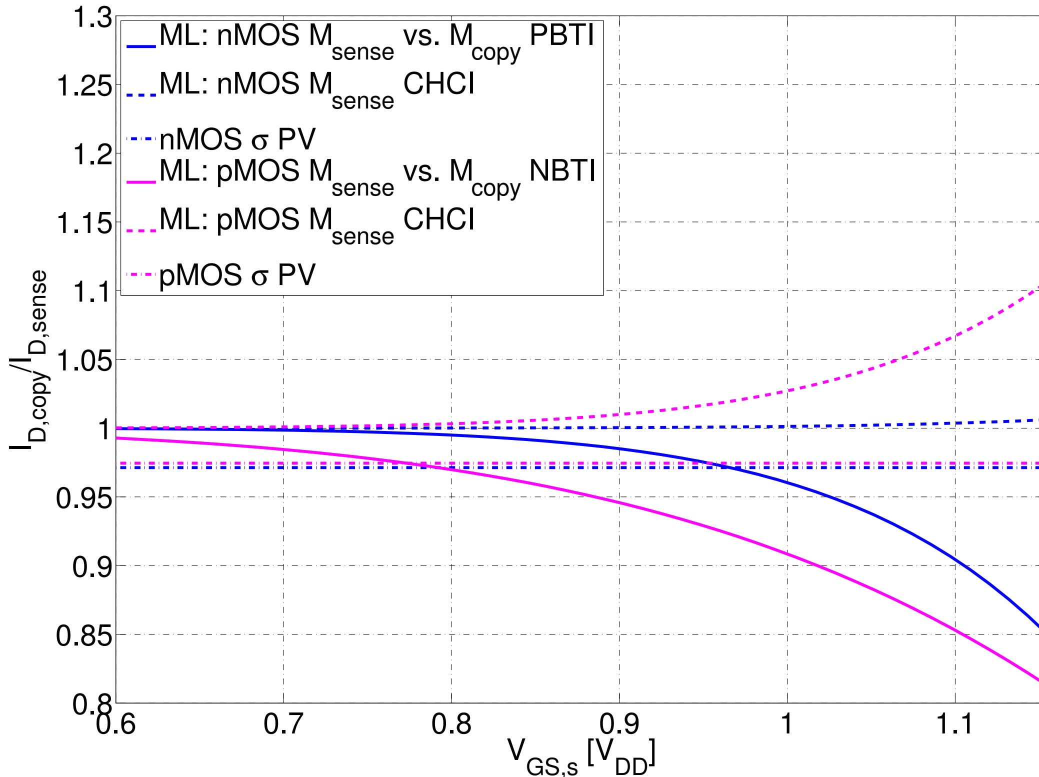

Fig. 5.5: Current mirror aging induced mismatch contributions after ML, 10y, 125°C operation as well as expected 1σ process variation in dependence of ML stress $V_{GS,s}$. Devices are assumed to provide the commonly used gate length $L = 6 \cdot L_{min}$. Mismatch is evaluated in the common operation point with $V_{GS,s} - V_{th} \approx 150mV$

5.4 Reference Circuit Case Study: Self-Biasing Current Reference

For simplicity, detailed investigations on diverse *reference circuit* topologies are omitted and a condensed exemplary case study on a self-biasing current reference circuit is performed. Obtained aging relevant results can be transferred to further reference circuit topologies as this analog circuit type typically provides similar device operation states and mostly incorporates internal stabilisation control loops making the structures robust against perturbations like global parameter, supply voltage or temperature variations.

5.4.1 Circuit Fundamentals

The schematic of the investigated PTAT (Proportional To Absolute Temperature) current reference circuit is depicted in fig. 5.6. This circuit provides a stabilized and tem-

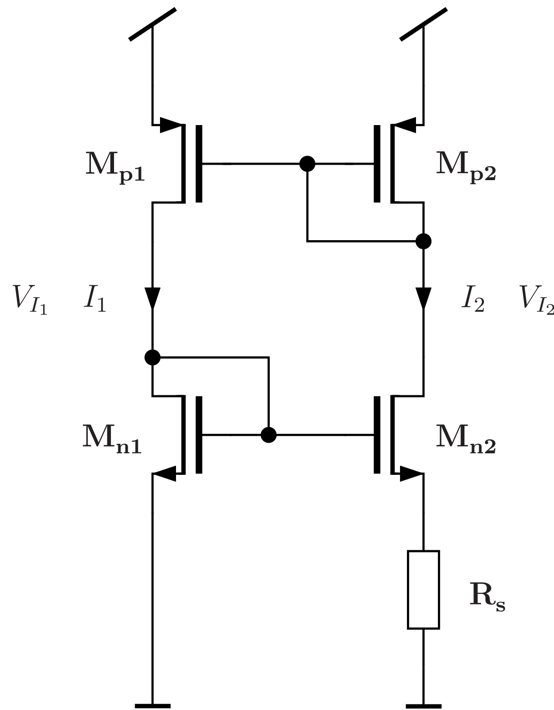

Fig. 5.6: Schematic of the exemplary current reference circuit

perature dependent current output I_1 and I_2 by suppressing impacts of variations in the supply voltage to the output current. This behavior is performed with a closed-loop current control via the *self-biasing* of the two cross-coupled current mirrors ($\mathbf{M_{p1}}$, $\mathbf{M_{p2}}$) and ($\mathbf{M_{n1}}$, $\mathbf{M_{n2}}$). The included $\mathbf{R_s}$ limits the current I_2, yielding to an overall stabilized current I_1 and I_2 [90]. One major task of the design of such a reference circuit is the proper start-up as $I_1 = I_2 = 0$ is also a stable operating point of this structure. To ensure this start-up, lots of exemplary circuitries can be found in literature [98, 90]. For simplicity and to provide universal aging related statements, this study neglects any individual

start-up circuit types and assumes the circuit to operate in the intended operating point. To ensure device reliability also for start-up sequences, studies considering the topology given start-up behavior have to be individually performed by the circuit designer.
Similar to the current mirrors, also in this current reference circuit, devices of large area to ensure enhanced analog device behavior are used. MOSFETs should provide high Drain-Source output resistance to achieve a good suppression of supply voltage perturbations, so devices have to be designed with large gate lengths [90].
During the on-state of the circuit, all devices have to operate in saturation region. This yields to an operating point around $V_{I_1} \approx V_{I_2} \approx \frac{V_{DD}}{2}$ and for the incorporated devices to a general **MM**[1] state during operation with $V_{GS} \approx V_{DS} \approx \frac{V_{DD}}{2}$. For these bias conditions only small device degradations are expected. For the case that the circuit does not start-up, voltages at internal nodes V_{I_1} and V_{I_2} can attain arbitrary levels, leading to a **LH**[1] worst case operation scenario at devices $\mathbf{M_{n2}}$ and $\mathbf{M_{p1}}$. As already discovered in the investigations on the current mirror in sec. 5.3.2, resulting NCHCI on $\mathbf{M_{n2}}$ and $\mathbf{M_{p1}}$ are negligible small, especially for the incorporated large gate lengths. Therefore, off-state with the arising **LH**[1] device state is omitted in the following case study.

5.4.2 Aging Behavior

stress operation: 10y, 125°C		V_{DD}	$1.25V_{DD}$	$1.5V_{DD}$
$\mathbf{M_{n1}}$	$\Delta V_{th,PBTI}$[2]	≈ 0	0.001	0.013
	$\Delta I_{D,CHCI}$[3]	≈ 0	≈ 0	≈ 0
$\mathbf{M_{n2}}$	$\Delta V_{th,PBTI}$[2]	≈ 0	≈ 0	≈ 0
	$\Delta I_{D,CHCI}$[3]	≈ 0	≈ 0	≈ 0
$\mathbf{M_{p1}}$	$\Delta V_{th,NBTI}$[2]	0.307	0.323	0.337
	$\Delta I_{D,CHCI}$[3]	≈ 0	0.07	0.8
$\mathbf{M_{p2}}$	$\Delta V_{th,NBTI}$[2]	0.307	0.323	0.337
	$\Delta I_{D,CHCI}$[3]	≈ 0	≈ 0	≈ 0
nominal operation: V_{DD}, 25°C aging induced ΔI_2[3]		≈ 0	-0.7	-3.4
nominal operation: V_{DD}		25°C	85°C	125°C
temperature drift ΔI_2[3]		≈ 0	$+15.4$	$+26.1$

Table 5.1: Overview over device aging effects and resulting reference current degradation for selected operations scenarios and comparison with temperature variation induced current drifts.

Table 5.1 shows simulation results on the reference circuit in fig. 5.6. It provides

[1] $V_{GS}V_{DS}$ voltages - L:low, M:moderate, H:high

individual device aging ($\Delta V_{th,BTI}$[2] and $\Delta I_{D,CHCI}$[3]) and its influence on the reference current I_2 for selected supply voltages. As operation use case, a period of 10y at 125°C is expected with a supply voltage range of $V_{DD} - 1.5V_{DD}$. This operation use case exceeds the common ones from sec. 3.8 in terms of stress conditions and can be considered as an exorbitant worst case scenario. As given in table 5.1 even for excessive operation conditions only minor device degradations occur due to moderate bias conditions at the devices. Furthermore, for the pMOS devices predicted NBTI degradation via $\Delta V_{th,NBTI}$ cancels due to the current mirror configuration of ($\mathbf{M_{p1}}$, $\mathbf{M_{p2}}$). Hence, reference current degradation, evaluated in the nominal operation point (V_{DD}, 25°C) after the application of the stress conditions, also shows minor drifts. To provide a general classification basis of device aging impact on the reference circuit, I_2 drifts due to temperature variations in the region of common environmental conditions are also evaluated in the lower part of table 5.1. Here, temperature related drifts in I_2 clearly dominate those generated by device aging, which pushes the impact of device degradation for this current reference circuit into the background besides other sources of disturbances. Due to the constant bias operation, high portions of recovering parts for the device aging mechanisms are expected, but will be of minor importance due to the generally small absolute parameter drifts. Also a change of device matching is expected to be negligibly small as defect variations for the aging mechanisms will be sufficiently averaged by the used large area devices and stress conditions are nearly symmetric for matched device pairs resulting in nearly symmetric induced drifts.

5.4.3 Transfer to General Reference Circuits

The observed results on the current reference circuit can be further transfered to other reference circuit types, like *Bandgap* voltage reference circuits. These circuit types also generate a DC reference current or voltage and thus operate in a single DC operating point. Incorporated devices have to operate in saturation region and are typically biased in a **MM**[1] state similar to the investigated self-biasing current reference. Generally, device sizing is of large area to suppress disturbances from the noisy power supply. So, expected device aging during reference generation is small and of minor impact on the reference value. However, the reliable circuit's start-up is individually performed according to the used start-up circuitry. Due to the various options and implementations, design related start-up behavior with respect on device aging is not covered by this study and has to be individually verified by the circuit designer.

5.5 Summary

This chapter provides an insight into the aging behavior of analog current mirrors. Due to their circuit configuration, parameter drifts symmetrically occurring in the sense and

[2] in mV
[3] in $\%I$
[1] $V_{GS}V_{DS}$ voltages - L:low, M:moderate, H:high

copy device are fully canceled via self adjustment in the bias voltage V_{GS}, resulting in an active aging suppression ability. Furthermore, typical biasing of a current mirror is in the range of moderate voltage levels, resulting in small device degradations. However, for asymmetric operation also asymmetric degradation occurs that impacts the pair matching. Here, high output voltages at the copy device can induce, dependent on the device dimensioning, significant mismatch in the on- and minor mismatch in the off-state. Furthermore, a partially off-state by the disconnection of the copy device from the supply induces the accumulation mode for the copy device. Generated device degradation was discovered as a significant mismatch source, but was not investigated due to the missing accumulation mode aging model. Further studies on current mirror matching behavior after accumulation mode off-state have to be conducted with the allocation of accumulation mode degradation models. A derived analytical circuit aging behavior approach, in this case an analytical current mirror mismatch model, including mismatch sources like expected process variations and stress induced parameter drifts, provides a powerful comparison basis for further ratings. Evaluation of the model shows that significant asymmetry is induced by HCI effects especially for the combination of the stress conditions short gate lengths and high output voltages. Increasing the gate length proves to be the suitable countermeasure to reduce the HCI impact. Only for pMOS devices in the used advanced 32nm high-κ metal gate technology, CHCI effects were the major contributor even for large device lengths due to a second order self-heating induced NBTI degradation (LSHA). The pMOS/CHCI contributions exceed the contributions expected by a 1σ process variation to a large extent. Further investigations during on-state, but with low output voltage at the copy transistor, revealed a moderate BTI induced mismatch, occurring due to the asymmetric operation states of the current mirror devices in saturation and triode region. Contrary to HCI induced asymmetries, this one can not be suppressed by increasing the device area and has to be considered as significant mismatch source for highly accurate and large area current mirrors. Furthermore, generated mismatch in this operation state is not covered by the commonly used 1-dimensional prediction models. Here, a more accurate 2-dimensional model, considering device's operation state would be desirable. Anyhow, the 1-dimensional BTI prediction model provided sufficient accuracy for hitherto found aging critical analog operation related aging states.
The case study on a self-biasing PTAT reference current circuit showed that device aging is of minor importance for this circuit type, which is in line with [23]. This is mainly due to convenient device dimensions and moderate stress conditions during the reference generation. Closed-loop circuit control further weakens the impact of the aging induced device parameter drifts. In general, occurring device aging plays a minor role on the reference generation and is pushed into the background besides occurring PVT variations. The methodology and the results of the case study are mostly transferable to other reference circuits like Bandgaps. One important thing that was not covered due to very individual implementations is the aging relevant start-up behavior, which has to be individually proven by the designer.

Chapter 6

Amplifiers

6.1 Circuit Fundamentals

Amplifiers are one of the most basic analog circuit blocks. They are commonly used in many analog and mixed signal integrated systems like AD (Analog to Digital) or DA (Digital to Analog) converters as signal buffers, to decouple sources with low driving ability from the signal processing part, or as accurate signal amplification or comparing element. But also in other fields like IO (Input Output) or RF (Radio Frequency) circuitry, amplifiers play an important role to provide proper signal processing and propagation. Of course, depending on the field of application, performance requirements vary and individual types and topologies are developed for their special field of operation. To provide a universal understanding, this work starts aging investigations on basic amplifier types implemented in the 32nm high-κ metal gate CMOS technology [91]. These findings are generally transferable to advanced amplifier implementations. All further investigations and derivations are performed on a state-of-the-art two stage differential amplifier, designed as a buffer circuit for an AD converter that is further available as real testchip hardware to prove derived concepts.

6.1.1 Amplifier Basics

Amplifying circuits in CMOS technology base on the general input voltage V_{GS} control of output current I_D of MOSFETs, that is in first order approximation independent on the output voltage V_{DS} as long as the device operates in saturation region. Here, MOSFET devices can be approximated as a voltage controlled current source. As saturation region is defined by the V_{GS} to V_{DS} ratio according to $|V_{GS}| - |V_{th}| < |V_{DS}|$, device operation region has to be fulfilled by the proper dimensioning of the *overdrive voltage* $|V_{OD}| = |V_{GS}| - |V_{th}|$ and the corresponding limitation of the output voltage $|V_{DS}|$. In saturation the impact of the output voltage V_{DS} to the output current I_D is provided by CLM resulting in a high ohmic resistive behavior that scales with $\sim \frac{1}{L}$ of the device gate length. For high output resistance large gate lengths have to be provided. The drop of

the input voltage controlled current at the high ohmic output resistance provides a high voltage to voltage amplification ability A_V. Due to the limitation to device saturation region, high amplification can typically be provided in a limited output voltage region much smaller than the supply voltage range. To provide full swing amplification or low ohmic load driving ability, that would destroy the high voltage amplification ability, special output stages can be appended to the voltage amplification output.
Commonly used symbols for amplifying blocks are given in fig. 6.1. Amplifiers can be

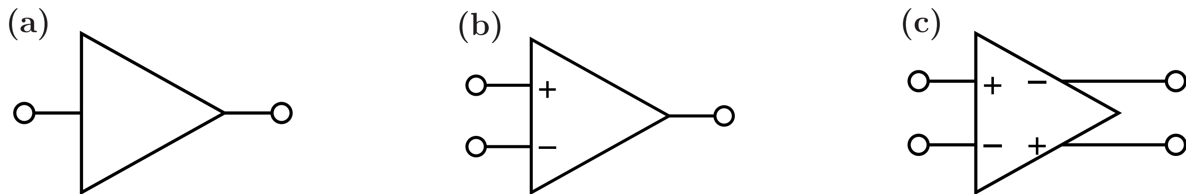

Fig. 6.1: Commonly used block symbols for amplifying circuits: (a) single-ended to single-ended amplifier, (b) differential to single-ended amplifier and (c) fully differential amplifier

generally classified by their way of signal processing and propagation. One distinguishes between *single-ended to single-ended*, *differential to single-ended* and *fully-differential* processing. Integrated analog circuits typically use fully-differential topologies until the final output stage as they benefit from the suppression ability towards external disturbances. Here, couplings affecting both signal branches are canceled by deriving the differential signal [90]. Of course, certain circuit types like *comparators* demand for a differential signal processing, at least at the circuit input, to perform the signal comparison. Amplifiers are usually employed in *closed-loop* configuration, as highly accurate amplification ratios and high linearity can be provided, which are not achievable in *open-loop* modes due to process imperfections. Therefore, high amplification rates are required that are inherently provided by analog CMOS circuitry. To guarantee stable closed-loop control, it is important that amplifiers provide sufficient PM (Phase Margin) until reaching the GBW or unity gain frequency. This particularly concerns amplifiers built of more than one stage and has to be fulfilled by a corresponding *frequency compensation*. Here, *bode* diagrams of the frequency behavior provide the performance information. But also the capacitive driving ability limiting the speed of the circuit, that is further given by the GBW or the SR (Slew Rate) and the suppression ability towards disturbances from the supplies or the noise behavior are important values limiting the performance of the overall system.

6.1.2 Circuit Topologies

In this work amplifier topologies are generally distinguished between two types of biasing: *voltage* biased and *current* biased circuits. This differentiation is done due to the biasing dependent aging impact on circuit performance. Therefore, fig. 6.2 shows two exemplary circuits, that are commonly used as standalone amplifiers or as parts of more complex structures. To provide fundamental and universal results during the following

studies, both circuits are built in their most basic circuit configuration - a voltage to current converting transistor with a resistive load. In advanced versions of these circuits, resistive loads are often replaced with MOSFET loads to achieve higher amplification ratios with fair area consumption. For comparison reasons the amplifiers are designed

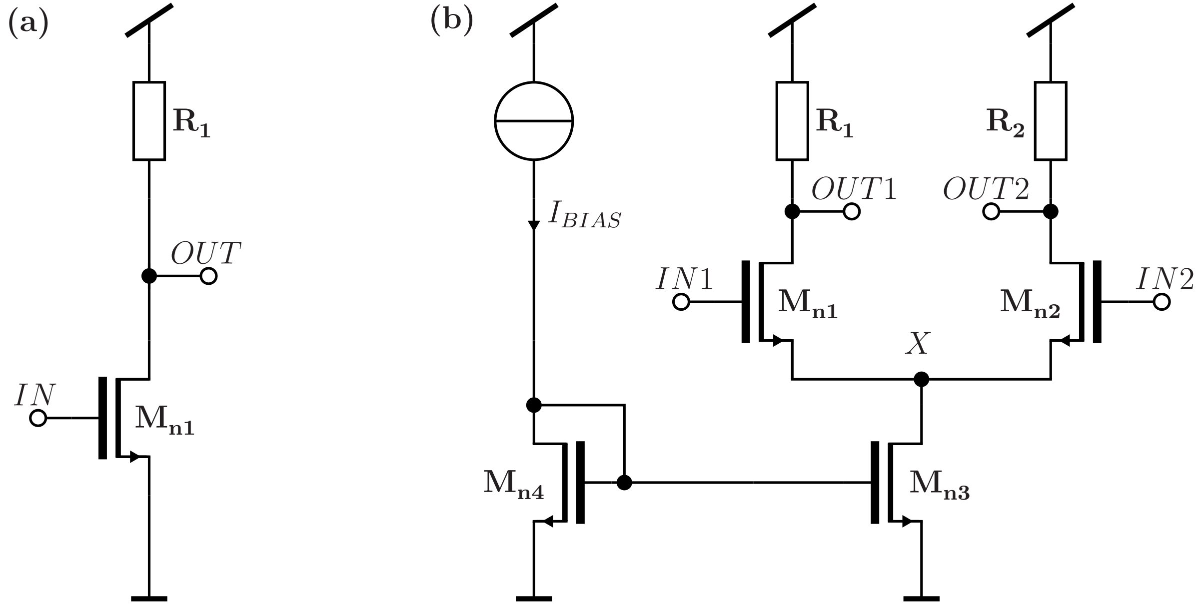

Fig. 6.2: Schematic of a very basic common source amplifier (a) using voltage biasing and a simple differential amplifier (b) with current biasing

to meet performance specifications according table 6.1. The *common source* single stage

A_V	$\sim 20dB$
GBW	$\sim 500MHz$
V_{IN}	$\sim \frac{V_{DD}}{2}$
C_L	$4pF$

Table 6.1: Performance specifications for the exemplary amplifier circuits in fig. 6.2.

amplifier from fig. 6.2 (a) is an example for voltage biasing, as output voltage of $\mathbf{M_{n1}}$ is defined by the DC level of the input signal. Here, the input signal IN provides both, the DC operating point and the signal contribution as well. On the contrary, the operating point of the differential pair in fig. 6.2 (b) is defined via the bias current provided by the current mirror ($\mathbf{M_{n4}}$, $\mathbf{M_{n3}}$). Here, variations in input signal $IN1$ and $IN2$'s DC level are transfered to the voltage level at node X. For a well designed current mirror ($\mathbf{M_{n4}}$, $\mathbf{M_{n3}}$) and as long as $\mathbf{M_{n3}}$ operates in saturation, which of course limits the DC headroom for $IN1$ and $IN2$, the impact on the bias current and thus on the circuit performance is small and in first order independent on the input DC level. Anymore, current biasing demands for a differential signal processing, as provided bias current has to be shared between two matched branches with differential input signals. Further circuit properties

for the common source and the differential amplifier are given in analog circuit design textbooks [90, 98, 100, 101]. For the following study both circuits are used to provide a very universal view on the impact of device aging on amplifying circuit blocks.

6.1.3 Design Fundamentals

To meet speed constraints and the driving ability of significant load capacitances, amplifying circuits have to provide sufficient driving current with MOSFETs, biased under moderate voltage conditions in the operating point. This demands for devices with large gate width. At the same time incorporated devices have to provide sufficient output resistance to fulfill required voltage to voltage amplification, which demands for devices providing large gate lengths. Furthermore, other short channel effects are reduced with increasing gate lengths that favors the analog device operation. Especially differential structures often demand for highly accurate matching of differential pair devices to limit CMOS process given asymmetry, commonly known as *offset*. Here, process induced local variations or improper device layout induce this inherent mismatch in the circuit. Global variations are generally canceled similar to the current mirror circuits. To reduce the impact of local variations, devices of large area are used to reduce standard deviation due to the Poisson distributed number of doping atoms per unit area and so reduce mismatch between two devices. On the other hand, input devices of an amplifier act as a capacitive load of a preceding circuit or sensor. To guarantee the driving ability from the input source, its capacitance should also be limited. Reducing the input capacitance demands for a decreased device area of the input pair, which counteracts the matching, amplification and current driving constraints. Here, a trade-off to find a best fit with the given specifications has to be found by the designer. Dimensioning rules for the current mirror in fig. 6.2 (b) can be derived from sec. 5.2.2. As a rule of thumb, input devices of an amplifier are of large gate width and typically provide a gate length that exceed the minimum available gate length by several times.

6.1.4 Operation Conditions

As already mentioned in sec. 6.1.1, amplifiers typically operate in *closed-loop* configuration to provide accurate and linear signal processing or in *open-loop* configuration as comparator circuit. Hence, two main aging relevant operation use cases can be derived. During closed-loop operation the aging relevant worst case scenario would be a full voltage swing at the output, whereas, due to the amplification of the circuit, the input signal level is slightly above or below the common mode. For single-ended structures (fig. 6.2 (a)) this would induce a **MH**[1] or a **ML**[1] operation state at the input transistor, which simultaneously occur on both input transistors for the differential amplifier (fig. 6.2 (b)). For open-loop operation, full swing can occur at the gate(s) of the input, leading to a **LH**[1] or a **HL**[1] operation state for the single-ended structure and to both states at the input pair for the differential circuit. Current mirror's copy transistor $\mathbf{M_{n3}}$ is driven into

[1] $V_{GS}V_{DS}$ voltages - L:low, M:moderate, H:high, A: accumulation mode

the **ML**[2] state (see sec. 5.2.3) for both use cases. So, aging relevant amplifier operation can be summarized to:

- **CL:** worst case scenario during closed-loop operation with full swing at amplifier's output inducing **MH**[1] and **ML**[1] device operation and
- **OL:** worst case scenario for the open-loop/comparator operation with full swing at the input(s) leading to **LH**[1] or **HL**[1] device operation.

Furthermore, individual standby scenarios can drive input devices into **AL**[1] operation mode. For the differential structure extreme variations of the common mode input level can arise that are transferred to the voltage level at node X and so mainly affect the copy transistor $\mathbf{M_{n3}}$ of the current mirror.

6.1.5 Circuit Aging and Affected Performance Parameters

During the **CL** scenario, the **MH**[1] stress state forms a CHCI condition. Arising device aging is expected to cause minor drifts due to uncritical gate lengths of the used devices. For the **ML**[1] stress state at the input device, only minor BTI contributions will be induced due to the moderate gate bias stress. In summary, for the **CL** scenario only minor overall drifts are expected. However, during **OL** use case, **HL**[1] stress condition will induce significant BTI degradation, whereas occurring NCHCI during the **LH**[1] state will be small due to uncritical gate lengths. Hence, during the **OL** scenario, BTI induced device degradation is expected to provide most significant drift contributions.

The upper part of table 6.2 shows details about the design and simulated performance of the two circuits from fig. 6.2 in the 32nm high-κ metal gate CMOS technology [91]. Reliability simulations with RelXpert™ for MP/EOL use case conditions prove the previously expected drift contributions. The asymmetric voltage stress conditions during **CL** and **OL** use case lead to asymmetric drifts in the devices. This changes amplifier's operating point for the voltage biased common source stage and the pair matching for the differential amplifier. In both cases this can be primarily seen in a change of amplifier's *offset* (comp. [23, 16]). Simulation results for the found use cases are given in the lower part of table 6.2. As expected for **CL** operation, aging induced device drifts are small due to the HCI suppressing convenient device lengths and moderate bias voltages. Therefore, overall induced offsets are small. During **OL** operation, BTI induced drifts occurring during devices' **HL**[1] state form the major contributor and induce significant offsets. This is mainly related to the area independent BTI aging behavior and the high stress voltages. Similar to the low CHCI contributions during **CL** operation based on the uncritical device lengths, NCHCI contributions occurring for the **OL**/**LH**[1] operation are also small even for high Drain bias.

Besides the generated offset due to a change of device characteristic, further operating point dependent parameters can be affected, which mainly depend on the type of biasing.

[2]current mirror $V_{GS,s}V_{DS,c}$ voltages - L:low, M:moderate, H:high

[1]$V_{GS}V_{DS}$ voltages - L:low, M:moderate, H:high, A: accumulation mode

		voltage biased CS single-ended	current biased fully-differential
R_i		600Ω	650Ω
L_i		$6 \cdot L_{min}$	$6 \cdot L_{min}$
I_{BIAS}		$\sim 850uA$	$\sim 1.6mA$
V_{IN}		$0.5V_{DD}$	$0.6V_{DD}$
A_{V0}		$\sim 18dB$	$\sim 16dB$
GBW		$\sim 500MHz$	$\sim 500MHz$
Operation Use Case		$\Delta V_{off,out}[mV]$	$\Delta V_{off,out}[mV]$
CL	**ML**[1]	+0.40	0.05
	MH[1]	-0.51	
OL	**HL**[1]	+68.96	13.28
	LH[1]	-0.62	

Table 6.2: Circuit implementation details and generated output referred offset in mV after corresponding use case operation under MP/EOL stress conditions for the exemplary voltage and current biased circuits. Offset evaluations are performed under nominal operation conditions at 25°C.

For the exemplary voltage biased common source stage, the fixed input bias voltage in combination with a changed device behavior for these bias conditions, changes the operating point of the amplifier and so performance parameters like amplification A_V and GBW, and of course also the SR. However, for the current biased differential amplifier, the aging induced mismatch does not change the operating point characteristic as this is given by the bias current, that is in first order independent on the input pair matching. This holds true as long as generated mismatch does not drive the current mirror copy device $\mathbf{M_{n3}}$ out of saturation region and its device aging is negligibly small. Indeed, the potentially critical **ML**[2] stress arises at $\mathbf{M_{n3}}$ during the **CL** and **OL** use case and is not accurately predicted via the 1-dimensional aging modeling. But as investigations in sec. 5.2.3 revealed, a significant current mirror mismatch and so a change of differential pair's bias current is negligibly small for the applied moderate gate bias voltages. Fig. 6.3 shows the simulated bode diagram before and after the worst case **OL** operation aging with MP/EOL conditions for both amplifier circuits. For the voltage biased common source stage, the drift in operating point further decreases gain A_V and GBW. Both are not affected for the current biased fully-differential structure. Here, virgin and aged bode characteristic nearly match each other. The found results on the two exemplary circuit types were performed on nMOS circuit versions in an advanced high-κ CMOS technology. Of course, the findings are universally transferable to pMOS circuitries and other CMOS process technologies by considering the individual device aging behavior.

[1] $V_{GS}V_{DS}$ voltages - L:low, M:moderate, H:high, A: accumulation mode

[2] current mirror $V_{GS,s}V_{DS,c}$ voltages - L:low, M:moderate, H:high

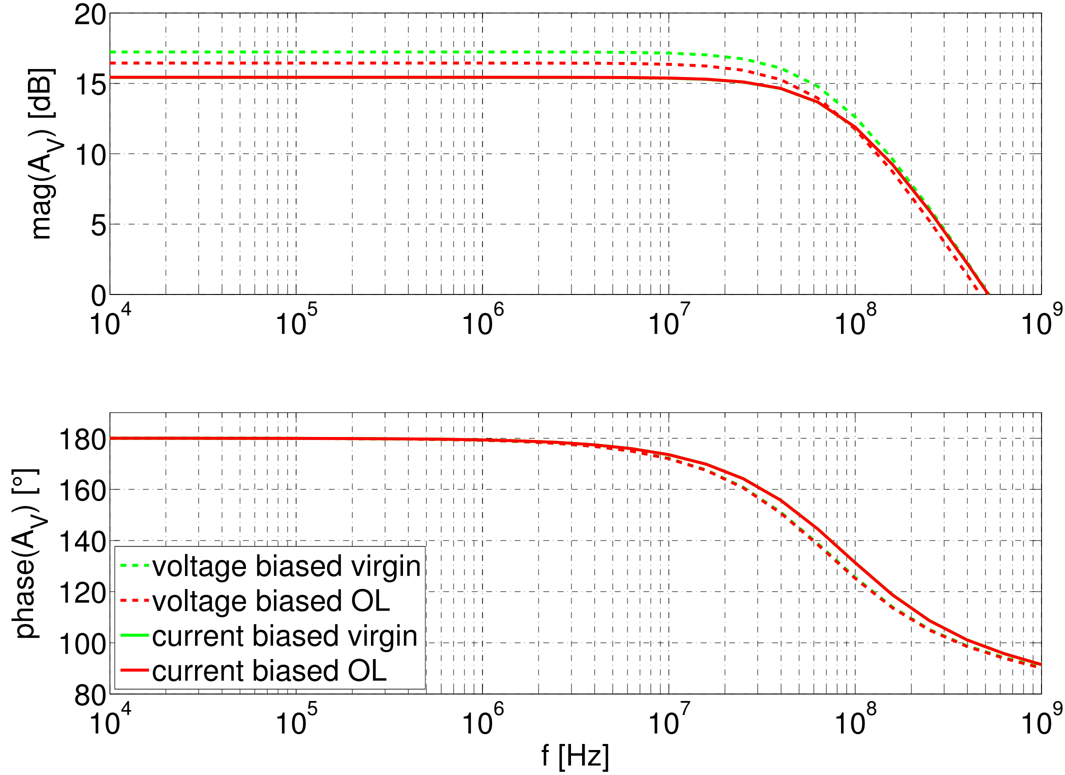

Fig. 6.3: Bode diagram of the voltage biased common source and the current biased differential amplifier in virgin state and after the worst case OL aging scenario. Bode plots are derived under nominal conditions at 25°C.

The previously mentioned operation scenario with extreme upper and lower variations in the common mode level of the differential pair are omitted in this study, as the pair matching is not affected and stress voltage is transfered with diminished voltage levels to the Drain node of the current mirror copy transistor. As already revealed in sec. 5.2.3, the **MH**[2] and the **ML**[2] current mirror use case will not induce significant mismatch in the bias current for the moderate Drain and Gate bias conditions. Even the high CHCI for pMOS devices in the used CMOS technology with the accompanying LSHA is negligibly small for these bias conditions. Due to the missing accumulation mode prediction model, individual standby modes driving input devices into accumulation mode are also omitted. But accumulation mode aging is expected as another significant source of device aging and should be investigated in detail in future work.

6.1.6 Aging Countermeasures

For amplifier circuits the input is one of the most aging sensitive part as here typically high amplification is performed and even small disturbances are amplified to the output. The

[2] current mirror $V_{GS,s}V_{DS,c}$ voltages - L:low, M:moderate, H:high

easiest way to counteract device aging is to ensure moderate device biasing for all circuit operation states. Especially for circuit standby modes, full swing or asymmetric stress states have to be suspended during circuit design. Of course this cannot be ensured for circuit types like comparators. With the previous investigations, the most critical aging contributor arises during **OL** comparator operation and is due to BTI. As for classic SiO_2 and $SiON$ based CMOS process technologies, BTI only significantly occurs as NBTI at pMOS devices, the usage of nMOS input device types would be one option to suppress this major offset contributor for such CMOS technologies.

Another option to suppress device aging impact is to perform a circuit level offset

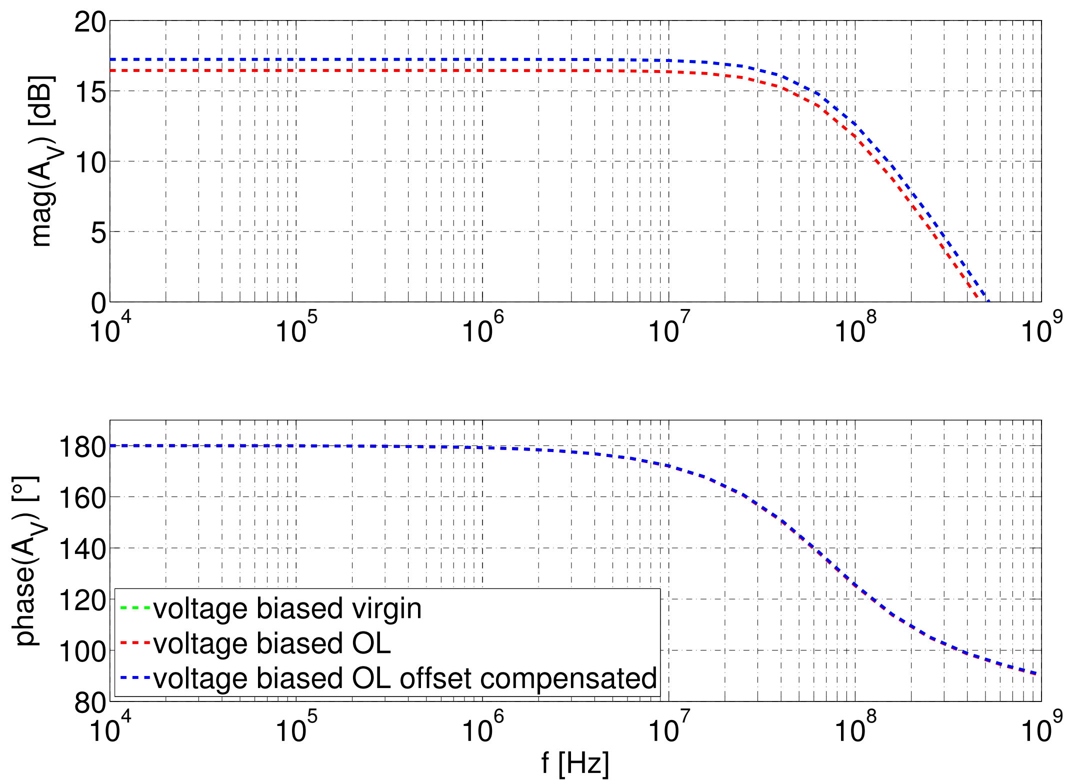

Fig. 6.4: Bode diagram of the voltage biased common source amplifier in virgin state, after the worst case OL aging scenario and after a further compensation of the OL operation induced offset. Bode plots are derived under nominal conditions at 25°C.

cancellation. Lots of compensation circuit implementations and techniques are proposed in common textbooks [90, 101, 98, 100]. To provide an example, fig. 6.4 depicts the bode diagram of the voltage biased common source stage from fig. 6.2 for the virgin, the circuit after **OL** aging and after aging with included offset compensation. The graph shows that the offset compensation completely restores the bode diagram to the virgin state. Another smart option to suppress and compensate aging induced offsets at the same time is the *chopper-stabilisation* technique. Its benefit with regard to amplifier aging is exemplarily studied in [102].

6.1.7 State-of-the-Art Differential Miller Amplifier

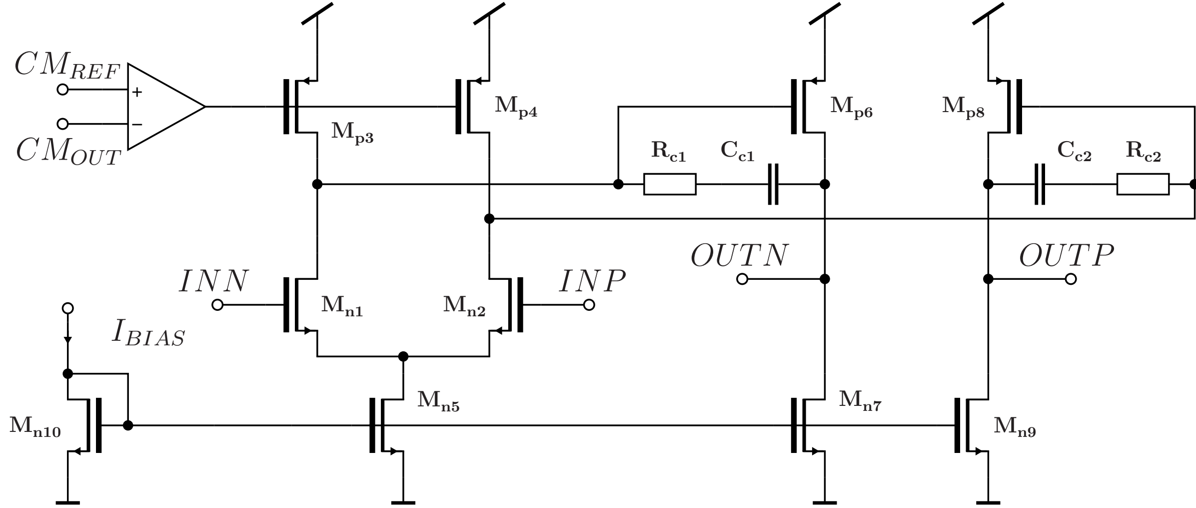

Fig. 6.5: State-of-the-art fully-differential miller compensated amplifier.

For the following investigations a more sophisticated amplifier circuit is used. Fig. 6.5 shows the schematic of a state-of-the-art fully-differential miller compensated amplifier. This two stage amplifier includes both types of previously investigated amplifier versions: the current biased differential stage as input and the common source stage as output stage. Resistive loads are replaced by active MOSFET loads to achieve high gain A_V via their high output resistance. To perform stable biasing a common mode control is included that adjusts output common mode levels according to the external CM_{REF} reference voltage. To guarantee stable closed-loop operation with a phase margin of $\sim 60°$, a RC compensation between the first and second amplifier stage is included. This type of compensation uses the *miller effect*, yielding to much smaller compensation capacitance values to achieve the intended frequency compensation and thus to smaller on-chip area consumption [90]. This amplifier is designed in the 32nm high-κ metal gate CMOS technology [91] for the usage in an AD converter and is further available on testchip hardware as standalone amplifier block. Due to its high current driving capabilities, it offers the characterisation by measurements as standalone amplifier.

The previously found amplifier aging relevant worst case operation states are also valid for this complex two stage amplifier. For the **CL** use case operation condition, a small differential input voltage is applied such that the output stage sees the full swing. This condition is depicted in fig. 6.6. Due to full swing at the output nodes, devices $\mathbf{M_{p6}}$ and $\mathbf{M_{n9}}$ operate in a **MH**[1] state inducing CHCI degradation. Further aging contributions of secondary order are expected from the beginning **HL**[1] stress conditions at $\mathbf{M_{p8}}$, inducing NBTI degradation, and the **MM-MH**[1] condition at $\mathbf{M_{p4}}$ generating CHCI. The last one is expected due to the high CHCI degradation levels for pMOS devices in the used CMOS technology. For the **OL** use case, depicted in fig. 6.7, device stress conditions at the output stage are preserved for $\mathbf{M_{n9}}$. Due to full swing at the input, also the output

[1] $V_{GS}V_{DS}$ voltages - L:low, M:moderate, H:high, A: accumulation mode

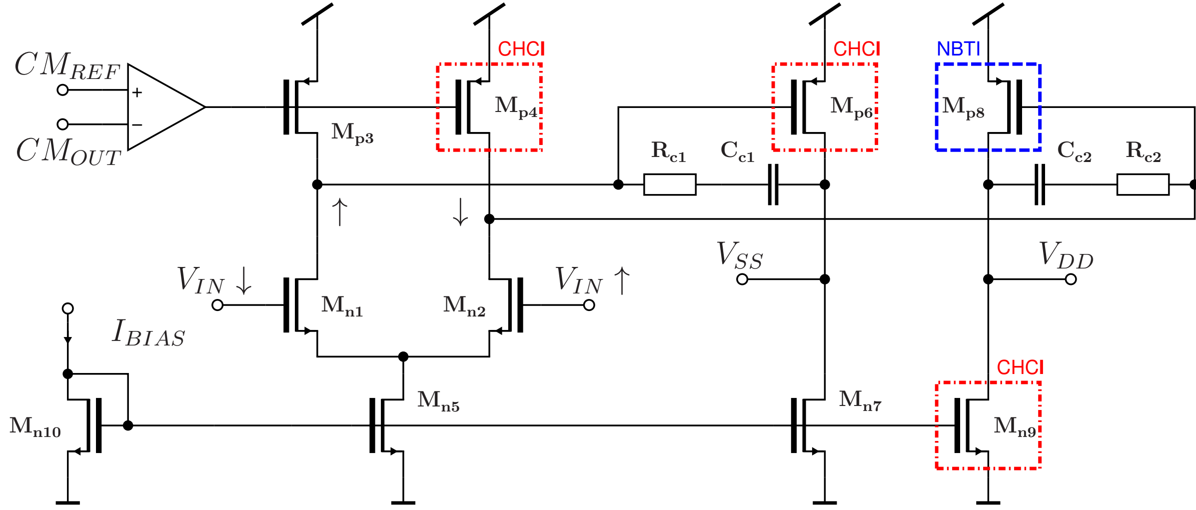

Fig. 6.6: Miller amplifier biased in CL use case: arising stress conditions at internal devices.

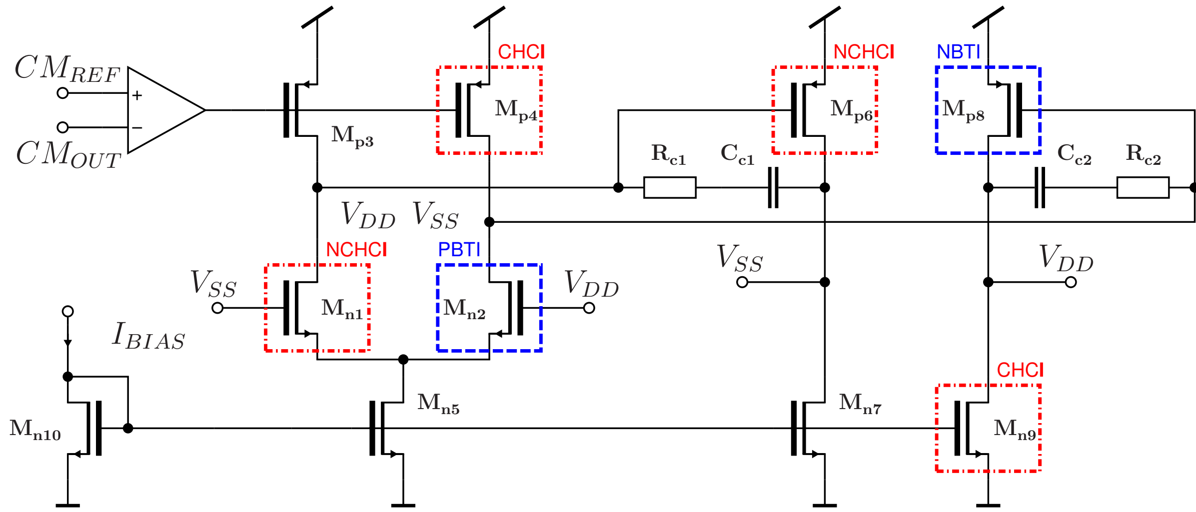

Fig. 6.7: Miller amplifier biased in OL use case: arising stress conditions at internal devices.

of the first stage sees the full asymmetric swing, changing the degradation mechanism for $\mathbf{M_{p6}}$ to NCHCI with the arising **LH**[1] operation condition. NBTI at $\mathbf{M_{p8}}$ and CHCI at $\mathbf{M_{p4}}$ is further enhanced. Additionally, the **HL**[1] condition at $\mathbf{M_{n2}}$ and the **LH**[1] condition at $\mathbf{M_{n1}}$ induce PBTI and NCHCI degradation in the input pair. For both operation use cases, individual BTI aging in the current mirror devices ($\mathbf{M_{p3}}$, $\mathbf{M_{p4}}$) and ($\mathbf{M_{n10}}$, $\mathbf{M_{n5}}$, $\mathbf{M_{n7}}$, $\mathbf{M_{n7}}$) due to distinct operation in saturation or triode region, should be negligibly small due to moderate gate bias voltages.
Reliability simulations via RelXpert™ for both use cases verify the findings from the previous sections. The asymmetric device aging induces mismatch in matched pair devices, leading to an offset in amplifier characteristic. Because of high amplification of the circuit,

[1] $V_{GS}V_{DS}$ voltages - L:low, M:moderate, H:high, A: accumulation mode

output referred offsets are masked by the amplifier's limited output range. In this case, the corresponding *input referred offset* provides a more general view on the generated mismatch and is shown in table 6.3 for MP/EOL conditions. Induced offsets for both use

Use Case	$V_{off,in}[mV]$
CL	0.46
OL	4.47

Table 6.3: Generated input referred offset for the two stage amplifier in fig. 6.5 for CL and OL use case operation under MP/EOL conditions. Offsets are evaluated under nominal supply conditions at 25°C.

cases provide similar results as for the basic structures: small offset generation for the **CL** use case and high induced drifts after **OL** operation. Analog to the previous findings, performance parameters like open-loop gain A_V and GBW are minor affected. Especially after another offset calibration, A_V and GBW are completely restored. At this point, another plot of the corresponding bode characteristic is omitted. Regarding the common mode control circuit for the output level, the findings derived from amplifier's **CL** use case with small induced offset drifts can be assigned as only minor asymmetric voltage stress occurs in the additional amplifier stage. Furthermore, expected small drifts are of minor impact due to the voltage buffer configuration of the control loop and would only slightly shift the output common mode level.
This investigation reveals, that with the number of included devices in a circuit also the number of aging contributors increases. All of them contribute to the total offset, but with individual directions and magnitudes, depending on the position and biasing in the circuit. In this example, BTI mechanisms at $\mathbf{M_{p8}}$ and $\mathbf{M_{n2}}$ lead to an offset drift in negative direction, whereas the HCI mechanisms at $\mathbf{M_{n1}}$, $\mathbf{M_{p4}}$, $\mathbf{M_{p6}}$ and $\mathbf{M_{n9}}$ lead to a positive drift. This means, that aging mechanisms may even counteract each other during circuit operation and the accessible *aging output monitor* during measurements - in this case offset - provides the circuit given weighted sum of all effects. Of course, this interaction depends on the circuit topology and its involved functionality. Here, the problem of *effect masking* arises. Two effects contributing in opposite directions to the aging output monitor can provide large drifts, but the monitor only provides its difference, that can be small compared to circuit's inner drifts. However, functionality may be affected due to shifts of operating points at internal nodes. A general approach to provide detailed information about a circuit's major contributors, their aging behavior and how inner effects interact is still missing in todays' reliability tools. Here, new approaches to provide a detailed *circuit level aging behavior model* have to be performed.

6.2 Amplifier Aging Model

Similar to the analytical aging behavioral model for current mirrors from sec. 5.3, an approach combining circuit behavior with device aging modeling can also be derived for amplifier circuits. This offers a powerful and universally valid circuit level aging model

to predict its aging behavior with respect to variations of stress conditions and provide information about major effect contributors. Furthermore, it opens new opportunities to develop concepts and approaches for accelerated circuit level stress measurements and advanced aging suppression on circuit level.

6.2.1 Analytic Model Derivation

Amplifier circuits typically boost input signals of small amplitudes to larger ones for proper subsequent processing. Amplification factor is typically nearly constant for small input signal ranges. Here, circuit behavior can be approximated by a linearized circuit model called *small signal* model. In doing so, devices in the signal path are replaced by their linear equivalent, providing via *transconductance* g_m the linearized input voltage to output current conversion factor and via r_o the linearized *output resistance* at the Drain node. These small signal parameters are valid in a certain range around devices' biasing points. The overall linearized circuit model provides accurate results for small input amplitudes and is typically used for fast and efficient circuit simulations on amplifiers. Exemplary small signal circuit derivations are treated in nearly every analog related textbook [90, 98, 100, 101]. Typical circuit characteristics that base on small signal simulations are transfer behavior or an amplifier's noise characteristic. As degradation induced drifts of device parameters are in the range of a few mV for ΔV_{th} and a few percentage points of Drain current for ΔI_D, those can be considered as some kind of input signal occurring at each degrading device. Compared to amplifiers supply voltage range, the degradation induced 'signals' are of small amplitude. At this point, the small signal circuit equivalent provides a suitable approach to combine device aging with general amplifier behavior.
Fig. 6.8 shows a block diagram how individual aging of an exemplary inner device $\mathbf{M_i}$ is

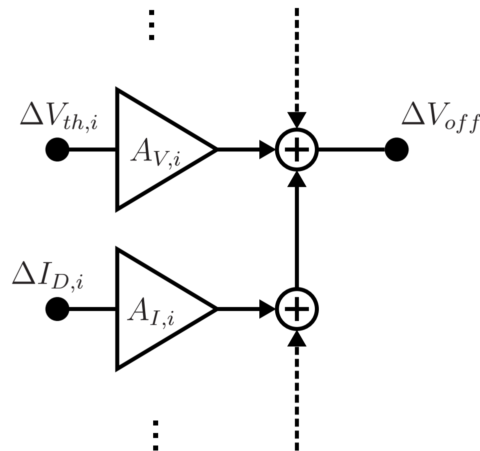

Fig. 6.8: Amplifier aging model: small signal approach considering individual degradation effect contributions of an exemplary inner device.

considered with respect to amplifier's linearized functionality. A drift in threshold voltage $\Delta V_{th,i}$ is amplified via the input voltage to output voltage gain $A_{V,i}$ from device $\mathbf{M_i}$ to the output of the circuit. A corresponding drift in Drain current is considered similarly

with the current to output voltage gain $A_{I,i}$. The small signal approach considers every aging effect to contribute independently to the overall circuit offset, while, in the mean time, the linearized circuit behavior does not change. Via superposition of individual effect contributions, the total generated offset can be predicted.
For the complex two stage amplifier from fig. 6.5, the inner device small signal amplification factors are given by:

$$\mathbf{M_{n1/2}}\text{: } A_V = g_{m,n1/2} \cdot (r_{o,n1/2}||r_{o,p3/4}) \cdot g_{m,p6/8} \cdot (r_{o,p6/8}||r_{o,n7/9}) \tag{6.1}$$

$$A_I = (r_{o,n1/2}||r_{o,p3/4}) \cdot g_{m,p6/8} \cdot (r_{o,p6/8}||r_{o,n7/9}) \tag{6.2}$$

$$\mathbf{M_{p3/4}}\text{: } A_V = g_{m,p3/4} \cdot (r_{o,p3/4}||r_{o,n1/2}) \cdot g_{m,p6/8} \cdot (r_{o,p6/8}||r_{o,n7/9}) \tag{6.3}$$

$$A_I = (r_{o,p3/4}||r_{o,n1/2}) \cdot g_{m,p6/8} \cdot (r_{o,p6/8}||r_{o,n7/9}) \tag{6.4}$$

$$\mathbf{M_{p6/8}}\text{: } A_V = g_{m,p6/8} \cdot (r_{o,p6/8}||r_{o,n7/9}) \tag{6.5}$$

$$A_I = (r_{o,p6/8}||r_{o,n7/9}) \tag{6.6}$$

$$\mathbf{M_{n7/9}}\text{: } A_V = g_{m,n7/9} \cdot (r_{o,n7/9}||r_{o,p6/8}) \tag{6.7}$$

$$A_I = (r_{o,n7/9}||r_{o,p6/8}) \tag{6.8}$$

Individual offset contribution of a degrading device $\mathbf{M_i}$ in the signal path is considered with

$$\begin{aligned}\Delta V_{off,M_i} =& A_{V,M_i} \cdot \Big(\Delta V_{th,BTI,M_i}(V_{GS,M_i}, T, t) + \Delta V_{th,CHCI,M_i}(V_{DS,M_i}, T, t)\Big) \\ &+ A_{I,M_i} \cdot \Big(\Delta I_{D,CHCI,M_i}(V_{DS,M_i}, T, t) + \Delta I_{D,NCHCI,M_i}(V_{DS,M_i}, T, t)\Big),\end{aligned} \tag{6.9}$$

by inclusion of the effect aging model equations (3.6), (3.10) and (3.12). Here, one has to distinguish between circuit's stress state, that is considered in the device stress voltages V_{GS,M_i} and V_{DS,M_i} and circuit's offset evaluation state, given by A_{V,M_i} and A_{I,M_i}, in which the amplifier typically operates in the intended operating point under nominal temperature and supply voltage conditions. So, this model approach maps the influence of device aging *after* a stress period. Total amplifier offset is predicted via superposition of all aging contributing devices in the signal path, taking into account the individual direction of the offset contribution:

$$\begin{aligned}\Delta V_{off} =& \quad \Delta V_{off,M_{n1}} + \Delta V_{off,M_{p4}} + \Delta V_{off,M_{p6}} + \Delta V_{off,M_{n9}} \\ & - \Delta V_{off,M_{n2}} - \Delta V_{off,M_{p3}} - \Delta V_{off,M_{n7}} - \Delta V_{off,M_{p8}}.\end{aligned} \tag{6.10}$$

Depending on the position in the circuit, device voltage stress conditions are mostly only indirectly adjustable via supply and input voltages and even change with variations in environmental temperature. For proper device stress voltage prediction, its characteristic has to be further modeled. For this two stage amplifier model, device stress voltage behavior is modeled with a second order polynomial fit, basing on a set of selected circuit simulations for the **CL** and **OL** operation states under elevated voltages and temperatures. As stress voltages mostly behave linear with supply/input voltage and temperature, a simple linear model fit should also be sufficient for most of the cases. The small signal approach supposes stable biasing to guarantee the valid transfer characteristic. Particularly, this applies for the current biasing of the sensitive input pair. From the previous

findings and the studies in sec. 5.3.2, this can further be ensured for both operation use cases due to the proper dimensioning and the moderate gate bias conditions at device $\mathbf{M_{n5}}$.
This analytic circuit level aging model approach provides besides the prediction of the circuit aging in the output monitor *offset* further information about contributions of individual circuit devices and their distinct aging mechanisms. This offers to decompose the total generated offset in its device and mechanisms contributors and shows the major parts. The fully analytic approach further offers the exposure of circuit level aging behavior, not only in one single stress operation point, as provided by reliability simulators like RelXpert™, but in dependence of the three relevant stress parameters *voltage*, *temperature* and *time*. This gives rise to the development of advanced concepts in the field of stress measurements and aging suppression.

6.2.2 Model Evaluation: Two Stage Miller Compensated Amplifier

The following model evaluation for the two stage miller compensated amplifier assumes a 10y aging scenario of operation under given stress voltages and temperatures for the known operation use cases **CL** and **OL**. Rise in stress voltages, given in V_{DD} factors, are assumed to affect all input voltages, that means all supply and input voltages are increased in the same manner. The effect of aging induced mismatch to circuit's offset after stress is evaluated under nominal supply and bias conditions and at 25°C. Here, the amplifier is biased with an input and output common mode reference level of $\frac{V_{DD}}{2}$. Due to constant current biasing, Gate bias voltage levels at the tail nMOS current mirror ($\mathbf{M_{n10}}$, $\mathbf{M_{n5}}$, $\mathbf{M_{n7}}$, $\mathbf{M_{n7}}$) also stay constant even for elevated supply voltages. The aging behavior model is implemented in MATLAB™ according to the derivations from the preceding section.
Fig. 6.9 and 6.10 show that predicted offsets provided by the analytic aging model

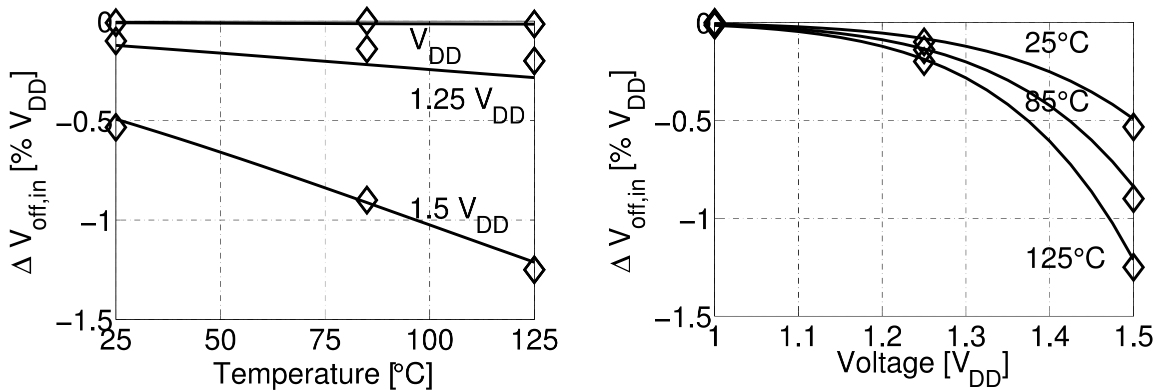

Fig. 6.9: Induced offset in two stage miller compensated amplifier after CL circuit operation with given stress conditions for 10y of aging: Circuit Aging Model (line) vs. RelXpert simulation (diamond). Circuit offset evaluations are performed for nominal circuit operation at 25°C.

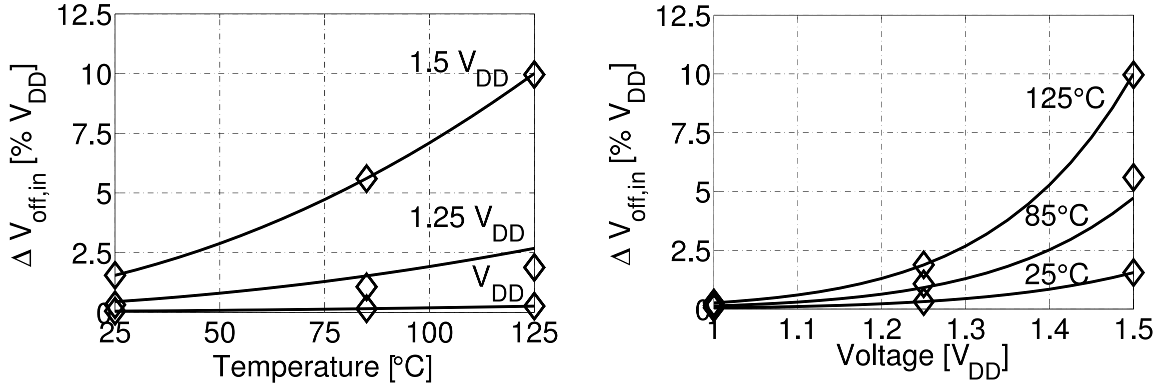

Fig. 6.10: Induced offset in two stage miller compensated amplifier after OL circuit operation with given stress conditions for 10y of aging: Circuit Aging Model (line) vs. RelXpert simulation (diamond). Circuit offset evaluations are performed for nominal circuit operation at 25°C.

compared to results derived with RelXpert™ are in line for both relevant use cases and selected stress configurations. This validates the analytic linearized model approach.
One benefit of the analytic aging model approach is the decomposition ability of generated drifts from contributing aging mechanisms. This is shown in fig. 6.11 for the **CL** and in fig. 6.12 for the **OL** operation use case. As total offset in the amplifier results in the difference of induced drifts in positive direction and drifts in negative direction, effect contributions are normalized to the sum of the absolute offset drifts $\sum_i |V_{off,M_i}|$.
For the **CL** use case fig. 6.11 reveals that the major offset generating contributors are **CHCI/M$_{\mathbf{p6}}$**, **NBTI/M$_{\mathbf{p6}}$** and **CHCI/M$_{\mathbf{p4}}$**, generating a drift in positive direction, contrary to **NBTI/M$_{\mathbf{p8}}$**, inducing a drift in negative direction. However, total generated offset is dominated by **CHCI/M$_{\mathbf{p6}}$** leading to the resulting positive output referred offset (negative for the input referred one).
The corresponding decomposition plot for the **OL** operation use case in fig. 6.12 shows that major offset contributions are from **NCHCI/M$_{\mathbf{n1}}$** and **CHCI/M$_{\mathbf{p4}}$** for positive drifts and **PBTI/M$_{\mathbf{n2}}$** and **NBTI/M$_{\mathbf{p8}}$** for negative drifts. Here, the induced total offset is in negative direction (positive for input referred offsets,) as this type of operation use case is dominated by **PBTI/M$_{\mathbf{n2}}$**.
An adaption of the **OL** operation use case and the arising effect composition is further depicted in fig. 6.13. Here, during **OL** stress condition only the input voltage is increased, while the supply voltage is kept at nominal V_{DD}. A corresponding offset prediction comparison of the model with RelXpert™ also shows a good fit and is omitted at this point. This adapted **OL** use case induces most of the circuit degradation at **M$_{\mathbf{n2}}$** of the input pair, especially for increased input voltage levels. Here, total offset is mainly attributed to **PBTI/M$_{\mathbf{n2}}$**.
The decomposition plots in fig. 6.11 and 6.12 reveal significant roles of CHCI effects in pMOS devices for both types of operation use cases. This can be mainly related to the arising LSHA (see sec. 3.4.2) in the used 32nm high-κ metal gate technology [91]. Especially for the **CL** use case, fig. 6.11 reveals that the observed high induced offsets in

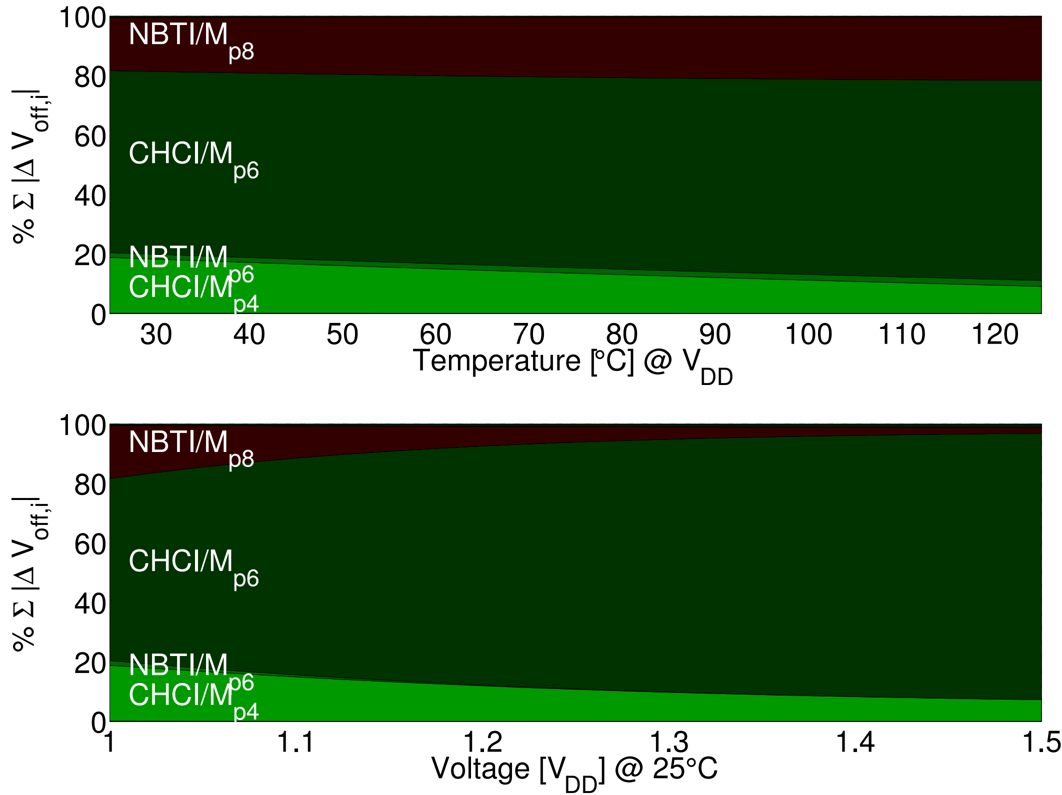

Fig. 6.11: Composition of offset contributing mechanisms in two stage miller compensated amplifier after CL circuit operation in dependence of stress conditions for 10y of aging. Circuit offset contributions are evaluated under nominal circuit operation at 25°C.

fig. 6.9 and table 6.3 are mainly induced by high $\mathbf{CHCI/M_{p6}}$. This shows that CHCI at pMOS devices might arise as another significant reliability issue in modern CMOS technologies. Other HCI contributions from nMOS devices are well controlled and negligibly small due to convenient device lengths.
The analytical model approach further offers to predict aging for diverse AC voltage stress scenarios. Here, aging dominating peak states during the time varying voltage stress can be considered as an equivalent DC stress case by taking into consideration a correction factor for the resulting decreased device degradation. Although, AC voltage stress impact on effect recovery is neglected by this model approach. Predictive AC correction factors can be determined via RelXpert™ comparing device degradation for the time varying and the equivalent peak DC circuit stress state. The derived correction factors can be further included into the analytic model to account for the time varying stress scenarios. Another use case example on this AC approach is omitted at this point.
For the investigated use cases, decomposition plots reveal that a variation of the stress parameters T or V can lead to significant changes in the distribution of offset contributing effects. This opens up a major problem during circuit level stress testing. The proper acceleration on circuit level to end-of-lifetime aging conditions via stress testing demands for the similar composition of aging effects on the circuit aging monitor. Otherwise, accel-

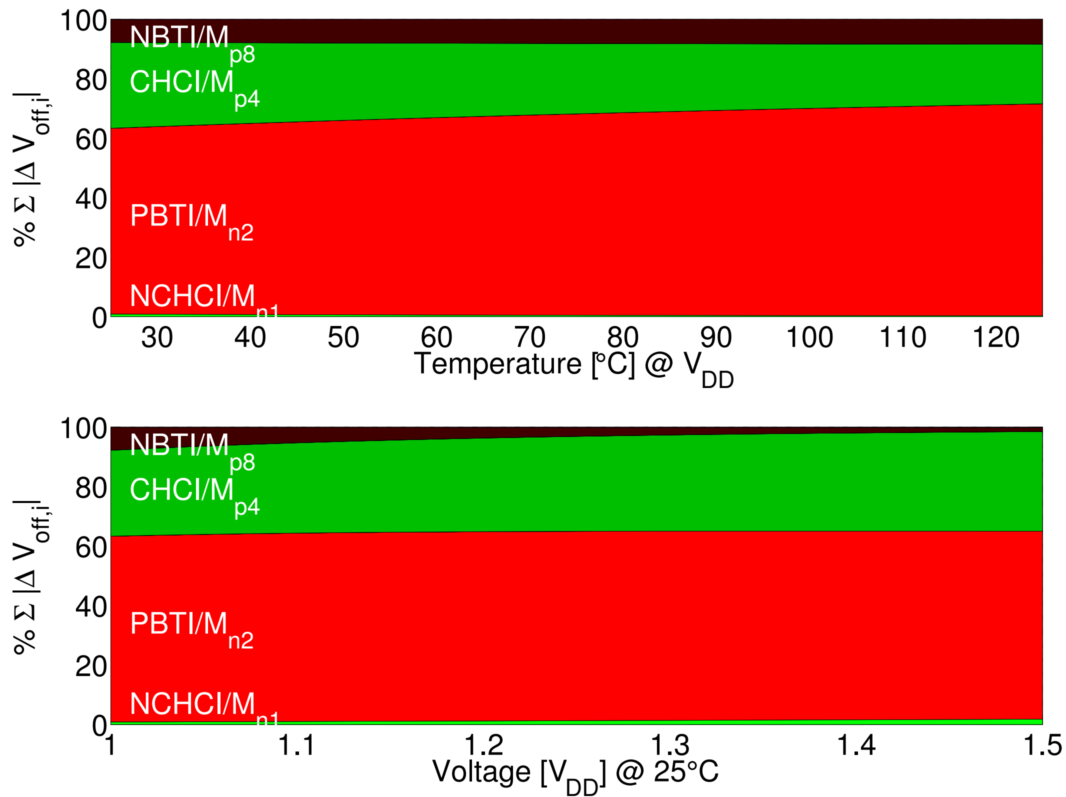

Fig. 6.12: Composition of offset contributing mechanisms in two stage miller compensated amplifier after OL circuit operation in dependence of stress conditions for 10y of aging. Circuit offset contributions are evaluated under nominal circuit operation at 25°C.

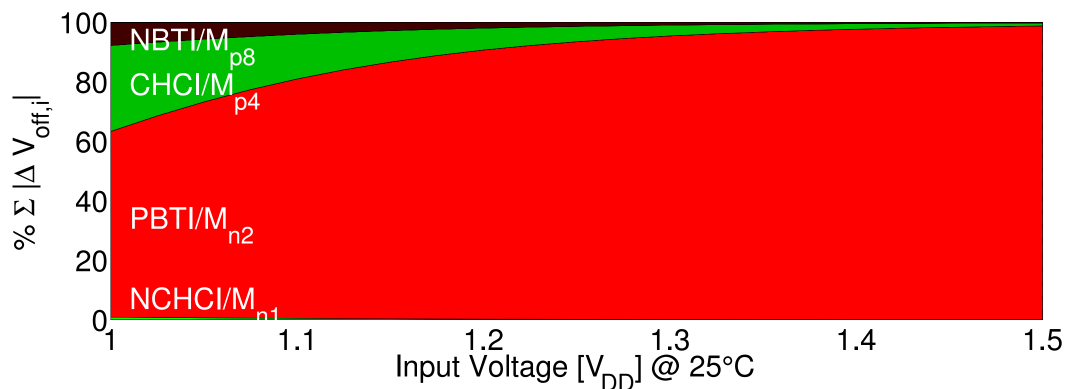

Fig. 6.13: Composition of offset contributing mechanisms in two stage miller compensated amplifier after OL circuit operation, but only increase of input voltage for 10y of aging. Circuit offset contributions are evaluated under nominal circuit operation at 25°C.

erated stress testing reproduces an aging scenario unrelated to the end-of-lifetime state. Here, the analytic model can form the basis to derive individual stress conditions for test related to a realistic end-of-lifetime use case. A corresponding concept approach will be discussed and proven on testchip hardware in the following sections.
The knowledge of circuit's major aging contributors also opens the way for development of specific countermeasure or suppression concepts located at the critical circuit part. An approach of a passive suppression and simultaneous calibration concept for differential amplifiers is treated in the following. Furthermore, PBTI dominance for **OL** operation and the fast signal processing ability of the two stage amplifier offers the possibility to perform PBTI related effect recovery measurements after stress for large time spans, giving new insights into transient effect behavior and its impact on circuit level.

6.3 Stress Testbench

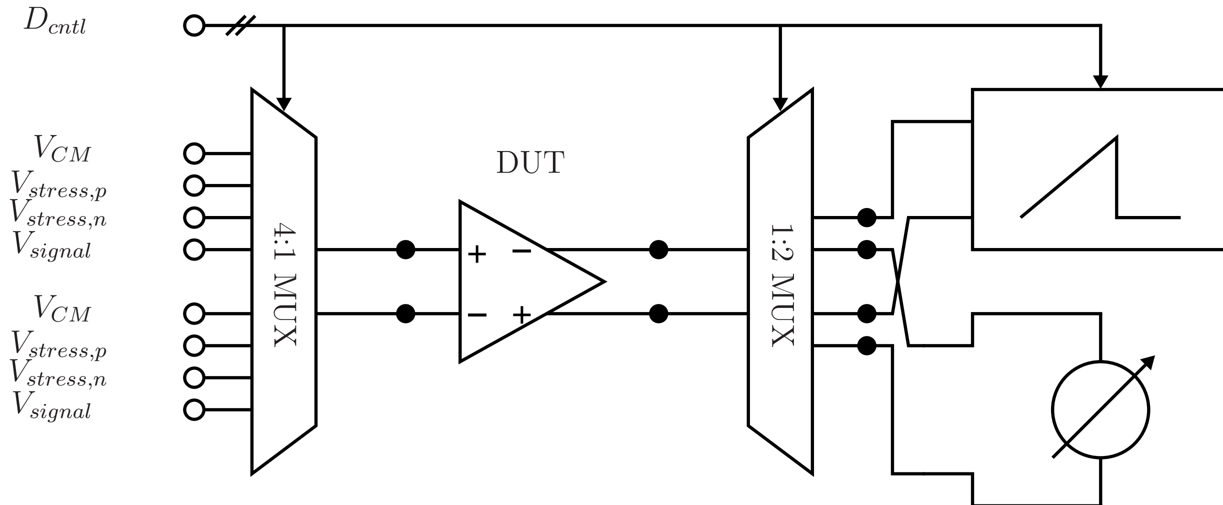

Fig. 6.14: Schematic of the used stress setup to perform stress testing on the two stage miller compensated amplifier.

The stress testbench in fig. 6.14 offers a fast and universal all-in-one measurement setup to perform alternating sequences of circuit level stress and characterisation. Due to limited gain of the DUT, testing is performed in amplifier open-loop configuration. A fast 4:1 MUX at the input of the *DUT* allows to switch two stress states given by $V_{stress,n}$ and $V_{stress,p}$, the V_{CM} option for offset characterisation in common mode operating point and V_{signal} to provide an analog sinusoidal signal to the input for amplifier transfer characterisation. Another 1:2 MUX at the output of the amplifier allows to switch between a fast oscilloscope and a multimeter for slow, longterm offset measurement. For the oscilloscope a four channel version is used to further monitor amplifiers' input signals (not shown). Via digital control signals D_{cntl}, synchronisation between MUXs, generation and acquisition hardware is performed.
The photograph in fig. 6.15 depicts the whole testbench. The necessary accurate temperature control of the *DUT* is performed with a custom built Peltier based device and a

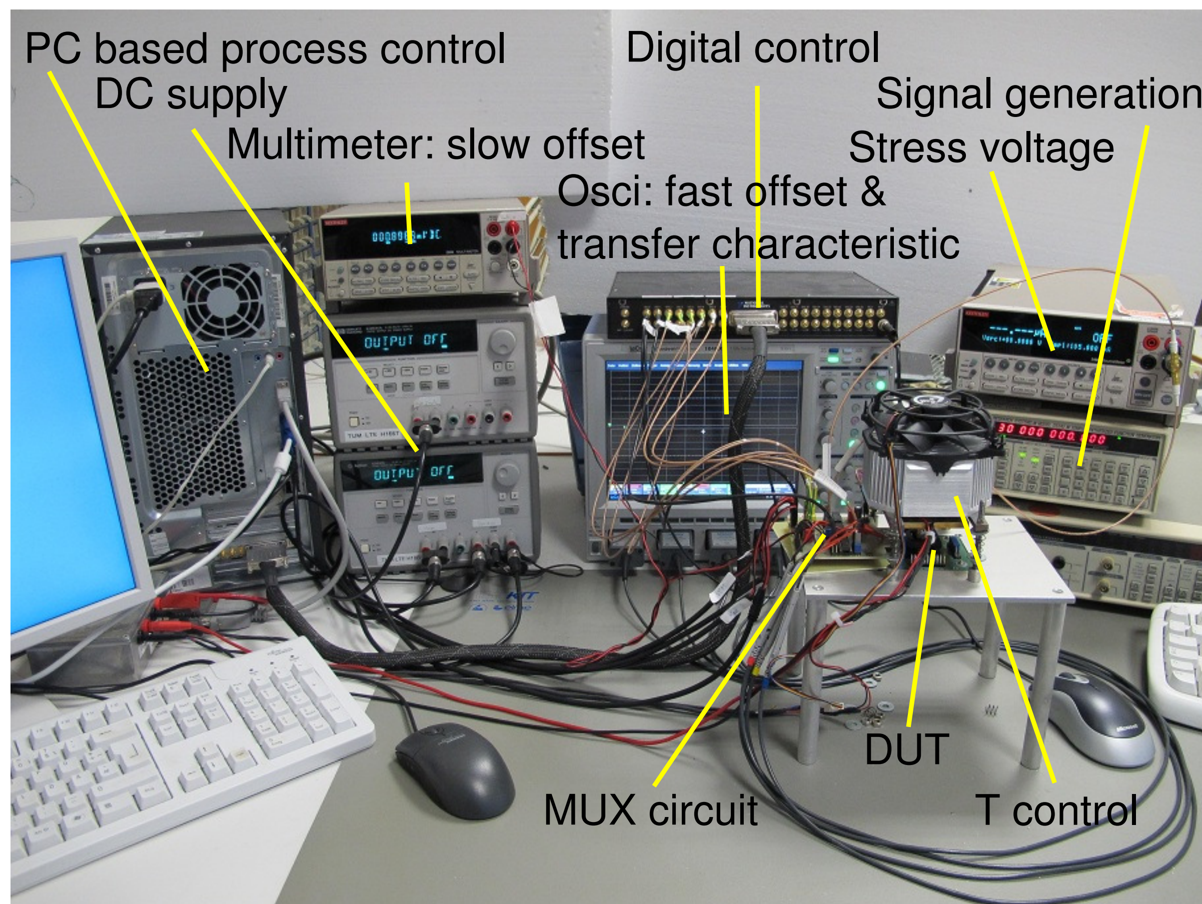

Fig. 6.15: Photograph of stress testbench and used hardware to perform stress tests on two stage amplifier.

programmable temperature control board. The heating and cooling device is positioned on top of the TQFP44 sample package in its measurement socket. The fast MUX circuitry is built as a custom PCB solution, that is directly mounted on the DUT's socket board. Supply voltages for the sample V_{DD} and the MUX $V_{DD,MUX}$ as well as common mode voltage V_{CM} are generated with Agilent E3631 DC Power Supplies. The sensitive input stress voltages $V_{stress,p}$ and $V_{stress,n}$ are generated with a Keithley 2400 Source Meter to provide accurate stress levels. V_{signal} for transfer characterisation is generated with a Stanford Research DS345 function generator. The oscilloscope is a 4 channel LeCroy WaveRunner 104MXi with active probes to minimize loading. Longterm offset measurements are performed with a Keithley 2000 Multimeter. The digital control and synchronisation of the equipment is performed with a PC based NI PCI-6551 digital pattern generator. Stress and characterisation sequences are fully automatized with NI Labview™ to provide reliable and reproducible measurement results.

6.4 Advanced Circuit Level Aging Approaches

The following studies are exemplarily derived for the complex two stage miller compensated fully-differential amplifier from fig. 6.5 and are further verified via stress measurements on available testchip hardware with the testbench from sec. 6.3. Of course, the concepts are universally valid and can be applied to other amplifier types, too.

6.4.1 Accelerated Circuit Level Aging For Test

Aging Acceleration on Circuit Level

As already addressed in sec. 6.2.2, accelerated aging on circuit level via stress measurements is a challenging task due to numerous individual aging affects all contributing to the aging monitor. For a distinct set of stress parameters (V, T, t), circuit aging is unique as every degradation effect appears with its individual acceleration behavior towards the stress conditions. So, an exact accelerated reproduction of an end-of-lifetime circuit state is not possible. Aging acceleration on circuit level is further complicated by the indirect application of device voltage stress via supply and input voltages and the temperature sensitivity of MOSFET devices leading to another circuit dependent impact on device stress voltages.
The insight into the effect contribution behavior via the decomposition plots in sec. 6.2.2 further demonstrates that a realistic end-of-lifetime use case acceleration for test can only be achieved if effect contributions are equal to the EOL case. This cannot exactly be attained due to the unique effect composition for a distinct stress condition (V, T, t). But a best fit can be achieved, if at least the *dominant* aging contributing effect provides the same degradation magnitude in the accelerated stress test and in the realistic EOL use case. Corresponding stress conditions for the circuit can be again derived via calculation with the analytic aging behavioral model.

Aging Use Case

In the following study, the aging relevant **OL** operation use case is exemplarily used to prove the circuit level aging acceleration mapping technique. As end-of-lifetime condition an operation for 10y with nominal voltage supply at 25°C is considered. Predicted input referred offsets after **OL** stress are given in table 6.4 for the 10y/EOL use case and an arbitrary stress setup of ($1.5V_{DD}$, 125°C, 1000s). Corresponding effect composition plots, evaluated via the analytic behavioral model, are given in fig. 6.16. Comparing generated offset levels reveals that the arbitrary stress setup induces mismatch much larger than that for the 10y/EOL operation under nominal conditions. But also effect contributions are different with an increased dominance of the **PBTI/$\mathbf{M_{n2}}$**. It is obvious, that the arbitrary stress configuration does not map the 10y/EOL operation use case accurately.

Use Case: **OL**	$\Delta V_{off,in}[mV]$
(V_{DD}, 25°C, $10y$)	0.69
($1.5V_{DD}$, 125°C, $1000s$)	8.33

Table 6.4: Generated input referred offset (model prediction) for the two stage amplifier in fig. 6.5 in OL operation for 10y/EOL use case and an arbitrary stress condition for 1000s. Offsets are evaluated under nominal supply conditions at 25°C.

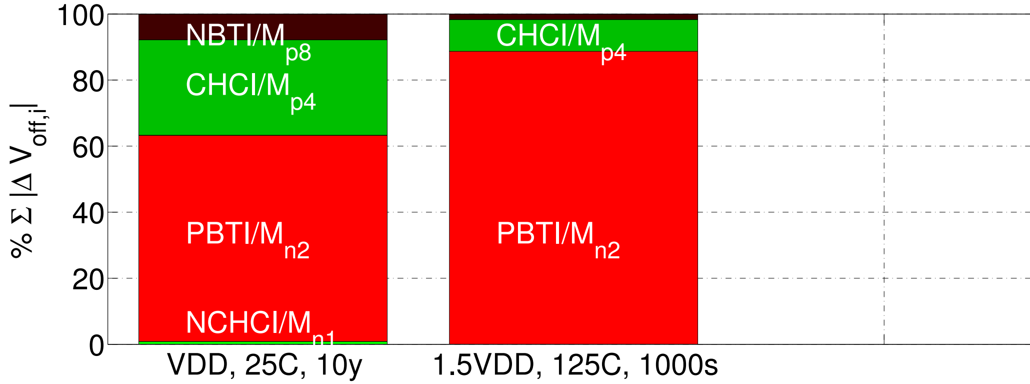

Fig. 6.16: Composition of offset contributing mechanisms in two stage miller compensated amplifier after OL operation with (V_{DD}, 25°C, $10y$) and an arbitrary stress condition ($1.5V_{DD}$, 125°C, $1000s$). Circuit offset contributions are evaluated under nominal circuit operation at 25°C.

Derivation of Stress Conditions

The developed concept to derive an accelerated stress condition corresponding to a realistic EOL operation use case demands for a dominating aging effect on the circuit degradation. For the exemplary **OL** use case, this is the **PBTI/M$_{\mathbf{n2}}$**. Corresponding stress conditions for equal degradation of the dominant aging contributor has to be derived according to

$$\Delta V_{th,PBTI/M_{n2}}(V_{EOL}, T_{EOL}, t_{EOL}) = \Delta V_{th,PBTI/M_{n2}}(V_{stress}, T_{stress}, t_{stress}). \tag{6.11}$$

For the exemplary stress scenario $T_{stress} = 125°\mathrm{C}$ and $t_{stress} = 1000s$ are preliminary chosen to typical values for stress testing. V_{stress} is derived according to eq. (6.11) and corresponding input and supply stress voltage has to be determined via the analytic circuit model. Accelerated stress configuration to map the given **OL** 10y/EOL use case results in ($1.1V_{DD}$, 125°C, $1000s$). In principal, also with several strong contributions a realistic acceleration would be possible, if they would all map in the same relation. But for the different physical effects, this is generally not the case.

Stress Test Sequence

For the following stress test verifications, the universal stress testbench from sec. 6.3 is used. The processed test sequence is given in fig. 6.17. Before stress is applied to

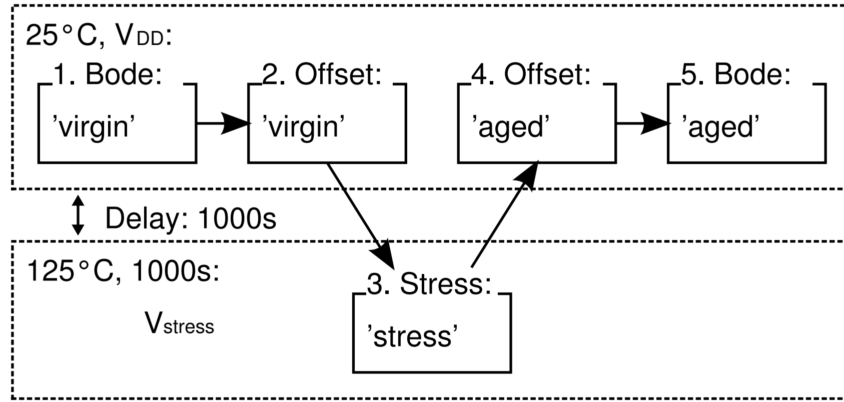

Fig. 6.17: Test sequence for the accelerated amplifier aging.

the amplifier, bode characteristic and offset are determined for the 'virgin' circuit under nominal circuit operation conditions. Heating up the DUT to 125°C is performed with a delay of 1000s for temperature annealing reasons. During stress, circuit's inputs and outputs are monitored. After the stress period, DUT is cooled to 25°C with the delay of 1000s and offset and bode characteristic is again determined for the 'aged' circuit.

Concept Evaluation and Discussion

Fig. 6.18 additionally depicts the decomposition plot for the derived accelerated stress condition ($1.1V_{DD}$, 125°C, $1000s$) - the equivalent for the 10y/EOL use case. Even for the derived stress condition, effect composition is not equal to the 10y aging under nominal conditions. But as given in table 6.5, the derived stress condition induces an offset drift

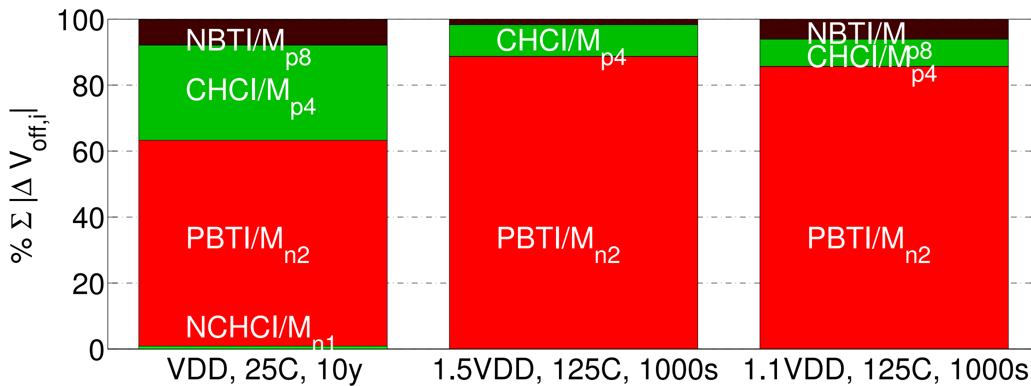

Fig. 6.18: Composition of offset contributing mechanisms in two stage miller compensated amplifier after OL nominal circuit operation for 10y, an arbitrary stress condition and the derived one corresponding to the 10y/EOL use case. Circuit offset contributions are evaluated under nominal circuit operation at 25°C.

that is close to the predicted one for the 10y/EOL use case. This further proves the accurate mapping ability of the stress derivation approach. Measurement data for $\Delta V_{off,in}$

Use Case: **OL**	$\Delta V_{off,in}[mV]$	
	Model	Measurement
(V_{DD}, 25°C, 10y)	0.69	n/a
(1.5V_{DD}, 125°C, 1000s)	8.33	7.03
(1.1V_{DD}, 125°C, 1000s)	0.60	0.59

Table 6.5: Generated input referred offset for the two stage amplifier in fig. 6.5 for OL operation in 10y/EOL use case, an arbitrary stress condition and the derived accelerated stress condition corresponding to the 10y/EOL use case. Offsets are evaluated under nominal supply conditions at 25°C.

after stress further validates the analytic model as well as the derived concept for realistic circuit level aging. Aging induced offset drifts are in the range of the predicted ones. It is obvious, that the quality of a derived equivalent stress configuration depends on the degree of domination of one aging effect in the aging scenario under realistic circuit operation. The higher the contribution of a single aging effect to the circuit aging monitor, the more accurate is the mapping of an equivalent stress configuration. In this case, the unequal acceleration of the other major contributing effects like **CHCI/M$_{\mathbf{p4}}$** and **NBTI/M$_{\mathbf{p8}}$** lead to a smaller absolute offset drift for (1.1V_{DD}, 125°C, 1000s) as for the 10y/EOL use case. If **PBTI/M$_{\mathbf{n2}}$** domination was larger for the 10y/EOL use case, derived stress configuration would provide offset drifts much closer to the realistic use case.

Furthermore, fig. 6.19 shows amplifier's transfer characteristic before and after stress. As already observed via simulations in sec. 6.1.5, transfer characteristic of current biased amplifiers hardly changes due to asymmetric aging. The measurement further confirms that this is also valid for the compound two stage fully-differential amplifier, built of a current biased input stage and a voltage biased output stage.

Besides the verification of the analytic circuit aging behavior model approach, the ability to stress circuits to an equivalent end-of-lifetime state offers the possibility to investigate for further aging induced second order effects coming along with the primary device aging. Analog circuits like amplifiers offer via their sensible signal processing the ability to perform further device based measurements like noise behavior. Especially, the flicker noise regime should be affected by device aging as similar mechanisms are responsible for device aging and flicker noise appearance [95]. Distinct studies on this relation are a promising topic for future work.

The analytic model approach basing on a linearized circuit model was exemplarily derived and verified for a two stage fully-differential amplifier. Of course, this approach is universally valid and applicable to other linear circuit types.

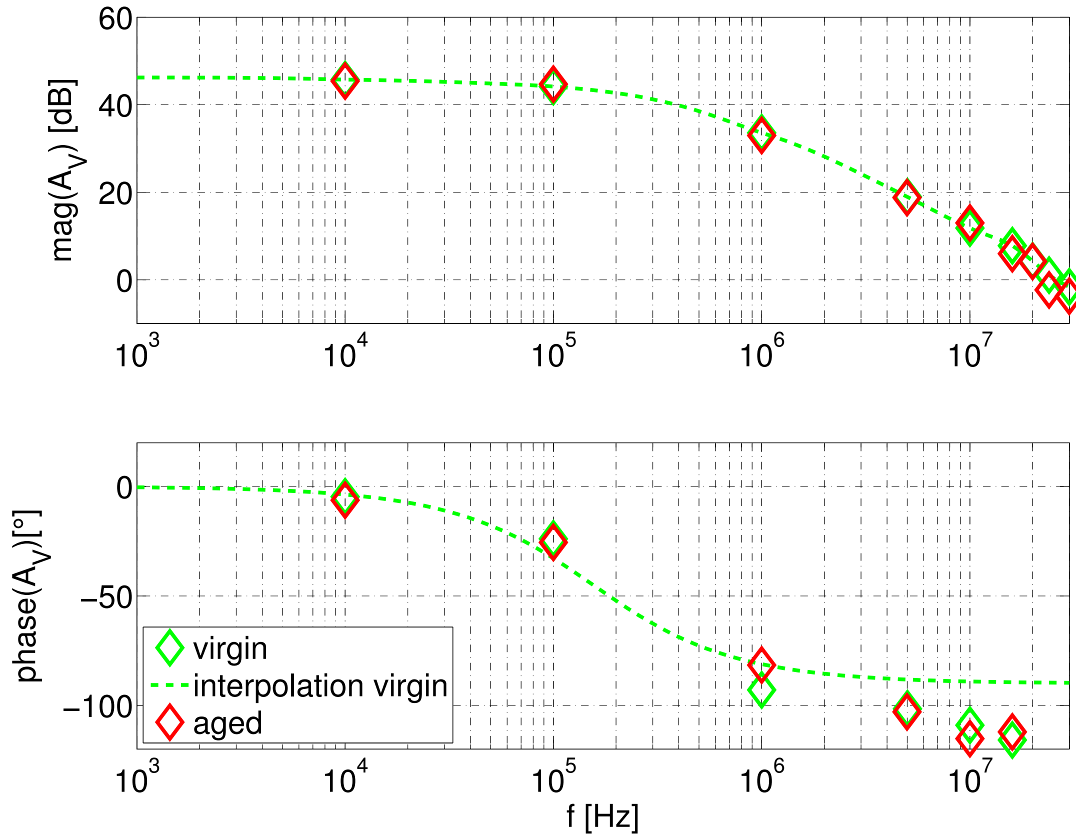

Fig. 6.19: Bode characteristic before ('virgin') and after ('aged') equivalent 10y/EOL operation use case. Measurements are performed in OL under nominal supply conditions and at 25°C.

6.4.2 Effect Recovery Measurements

Amplifier's Analog Signal Processing

As given in the transfer characteristic in fig. 6.19, the two stage fully-differential amplifier provides a significant input signal amplification up to the μs regime in open-loop configuration. As already postulated in sec. 6.2, aging induced device parameter drifts can be handled as signal contributions that are further processed by the amplifier signal propagation characteristic. Of course, this is also valid for transient components in these drifts, occurring as *effect recovery* directly after the application of stress (see sec. 3.3). Limited by the bandwidth of the amplifier, those transients are processed by the circuit leading to a time dependent behavior of the amplifier's offset. As effect recovery is mainly observed for BTI effects, major impacts on the offset are expected for use cases incorporating large BTI contributions. According to our knowledge from evaluations of the analytic circuit model, a transient behavior in amplifier offset is mainly expected to occur after **OL** stress due to high $\mathbf{PBTI/M_{n2}}$ contributions. For the **CL** operation use case, $\mathbf{CHCI/M_{p6}}$ dominates and only minor transients in the output offset are expected.

Operation Use Cases and Stress Configurations

In the following investigation, both the **CL** and the **OL** operation use case are studied with respect to the impact of degradation effect recovery to amplifier's offset. Stress measurements are performed with a stress configuration of (1.25V_{DD}, 125°C, 1000s) for both operation use cases. Predicted *fixed* output referred offset drifts induced by this stress conditions are given in table 6.6. The **CL** operation stress induces a small drift of

stress configuration	equivalent in MP	$\Delta V_{off,out}[\%V_{DD}]$
CL (1.25V_{DD}, 125°C, 1000s)	**CL** ($V_{DD,WC}+5\%$, 85°C, 16h)	+1.81
OL (1.25V_{DD}, 125°C, 1000s)	**OL** ($V_{DD,WC}+5\%$, 85°C, 8d)	-71.63

Table 6.6: Stress test configurations, equivalent age for MP conditions and predicted offset drifts according to the analytic circuit model.

the output referred offset in positive direction, contrary to the **OL** use case, that induces a large drift in negative direction. Furthermore, back calculation via the analytical circuit model provide the equivalent operation scenario under MP stress conditions (see sec. 3.8), which is for the **CL** use case in the range of hours and for the **OL** use case in the range of days. The corresponding decomposition plots for the stress configuration and

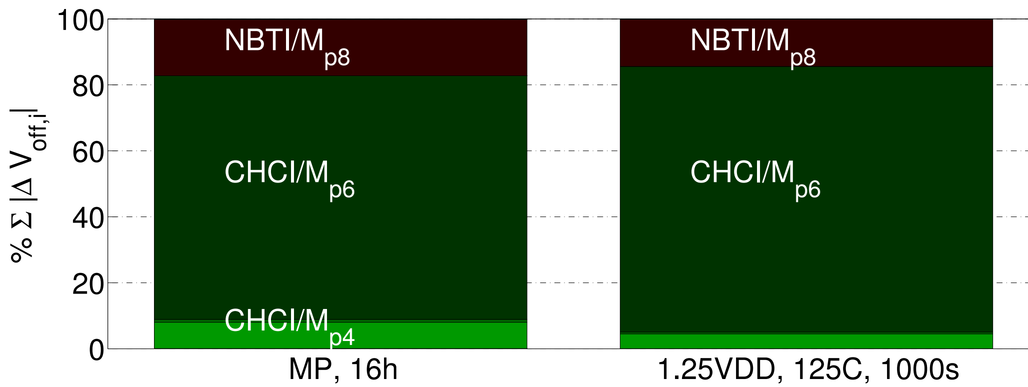

Fig. 6.20: CL effect decomposition for stress test configuration and the equivalent 16h aging for MP operation conditions.

the equivalent for MP conditions are given in fig. 6.20 for the **CL** and in fig. 6.21 for the **OL** operation use case. For both use cases the equivalent aging scenario for MP stress conditions show very similar effect composition. Thus, a good accelerated stress mapping can be assumed.

Stress Test Sequence

Stress tests are again performed via the universal testbench from sec. 6.3. The fast multiplexers at amplifier's input and output enables to measure a huge time span of the offset

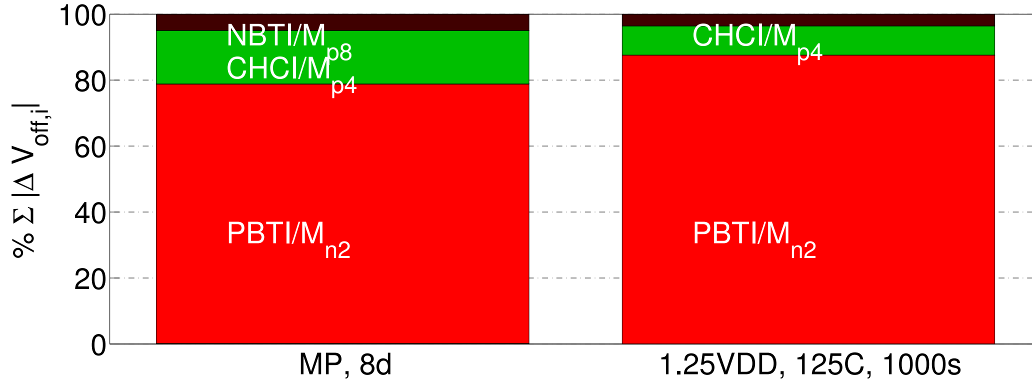

Fig. 6.21: OL effect decomposition for stress test configuration and the equivalent 8d aging for MP operation conditions.

behavior immediately after the application of the stress condition and so the impact of transient effect recovery on the offset. The performed measurement and stress sequence is given in fig. 6.22. After the characterisation of the 'virgin' sample under nominal condi-

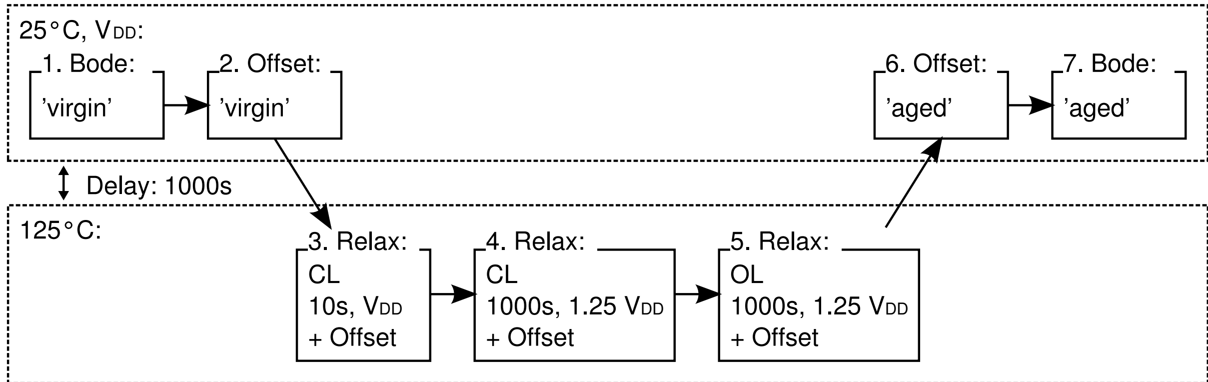

Fig. 6.22: Stress test sequence for amplifier relaxation testing

tions (V_{DD}, 25°C) for offset and bode characteristic, the sample is heated to 125°C stress temperature and a reference stress test for **CL** operation is performed for 10s at nominal supply voltage. It is followed by the immediate offset characterisation by monitoring the switching event from stress to operating point conditions. Short times up to 0.01s are sampled with the oscilloscope and the longterm behavior with the multimeter. The overall offset measurement time is 1000s, the same as the following stress periods. This reference switching behavior provides the switching event at stress temperature, but due to nominal supply and short times without significant aging effect contributions. The next two steps provide the **CL** and **OL** stress tests with $1.25V_{DD}$ stress voltage for 1000s, again followed by the sampling of the switching event. After cooling to 25°C, offset and bode characteristic for the 'aged' sample is derived.

Measurement Results and Discussion

Transient offset measurement results for the reference, the **CL** and **OL** stress cases are depicted in fig. 6.23. General direction and magnitude of induced offset drifts are in

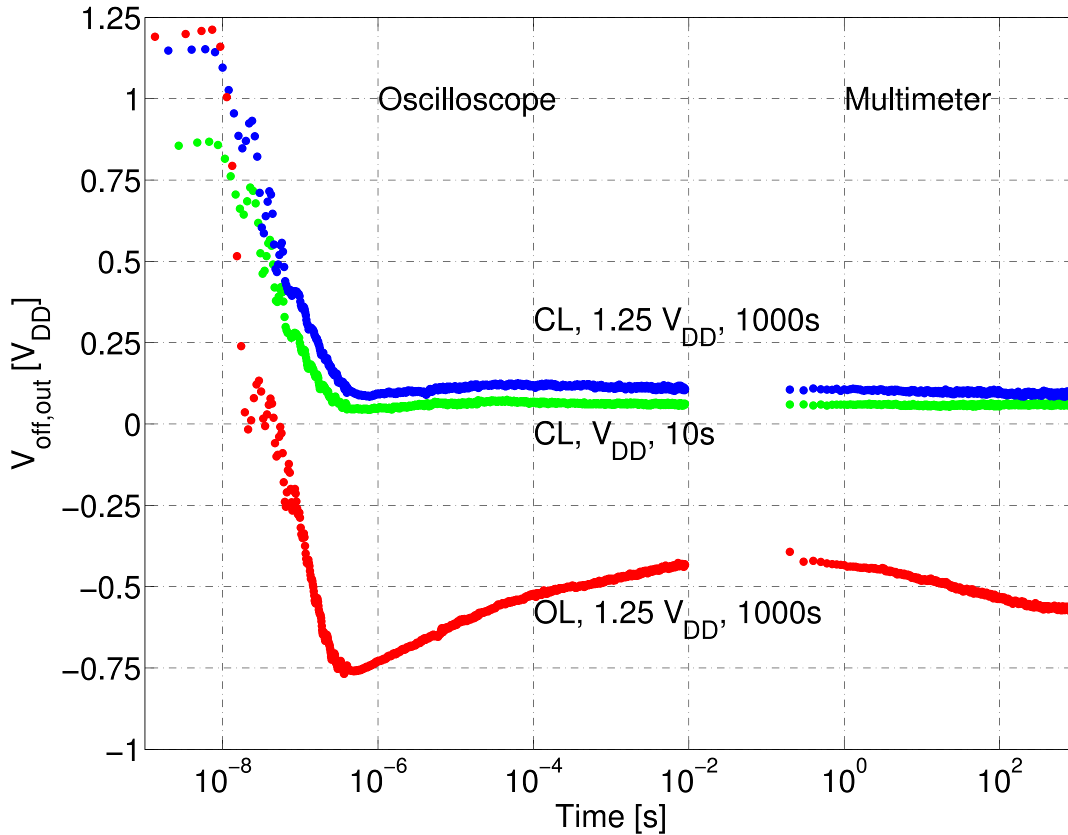

Fig. 6.23: Effect recovery after stress for CL/10s under nominal supply, CL and OL operation use case at elevated supply for 1000s. All offset measurements are performed at 125°C operation temperature.

line with the predicted values from table 6.6. As expected, the reference switching event shows, besides the undershoots resulting from the setup in the μs regime, a stable offset behavior over the whole covered time span. Similarly, offset behavior after **CL** stress provides a stable output voltage with the predicted small absolute drift in positive direction. For long times after stress, a slight recovery behavior can be observed. However, offset after **OL** stress shows a significant transient behavior with high amplitude and in two directions. A strong negative offset relaxes with a short time constant, then the offset increases again more slowly. As predicted by the model derivations and due to the bipolar shape of the offset curve, transient offset behavior can be mainly related to the **PBTI/$\mathbf{M_{n2}}$**. The general shape of the recovery curve is also in line with the PBTI measurements from sec. 4.2.4 and common literature [58, 59].

As fig. 6.23 reveals, amplifying analog circuits are very sensitive towards aging induced

parameter drift with its arising transient components during recovery. From a circuit designer's point of view, aging induced drifts and their recovering component play a significant source of disturbance for baseband processing. But also for modulated signal processing systems, the wide timing span can enter signal's frequency domain and arise as another source of interference. Indeed, common circuit design techniques for interference suppression target a splitting of signal and typical low frequency disturbances, but do not hold for those within the signal frequency. The common modeling of device aging in a constant parameter drift maps BTI aging only from a very basic point of view. For the proper consideration of device aging on sensitive analog circuits, an advanced modeling approach has to be developed, also accounting for the transient recovery behavior. As long as a thorough BTI model is not available, an improvement of the common modeling approach to further predict at least magnitudes for distinct recovery timings should be provided. For tasks, such as the design of a clocked offset compensation solution, the proper consideration of effect recovery will result in a major constraint for the dimensioning of the clocking frequency with respect to tolerable drifts.

6.4.3 Aging Suppression and Calibration Approach

Basics

The studies in sec. 4.2.5 already revealed the general saturation behavior of BTI aging effects with respect to stress duration. This behavior is universal for both BTI and HCI effects and is further considered in the prediction models (eq. (3.6) and (3.10)) with a sublinear time dependency. From the preceding studies on amplifier circuits the **OL** operation arises as the critical aging relevant operation state with major drift contributions due to BTI at the input pair. The following evaluation implies this operation scenario and proposes a concept to benefit from the effect saturation behavior on circuit level.
The approach of an aging suppression bases upon a controlled effect saturation of the BTI effects at both devices of the input pair. This can be achieved by switching the asymmetric **OL** stress condition between both inputs which generates a symmetric stress in the amplifier and thus does not change pair matching. This type of stress condition is called *'Burn-In'* in the following study. Furthermore, via selective asymmetric **OL** stress, a specific parameter *'calibration'* can be performed and offers the ability to compensate for offsets caused by process variations or layout induced asymmetries. The option to perform calibration via inverse polarity voltage stress is discarded as it changes effect relaxation behavior in an uncontrolled way and abolishes the 'Burn-In' induced saturation (see sec. 4.2.5).

Derivation of Burn-In and Calibration Stress Condition

Stress conditions for the Burn-In and the Calibration are derived via the analytic circuit model from sec. 6.2 for the two stage amplifier in fig. 6.5. Due to the domination of **PBTI/**$\mathbf{M_{n2}}$ in the **OL** scenario, it is sufficient to investigate device matching behavior at the input pair $\mathbf{M_{n1}}$ and $\mathbf{M_{n2}}$ and use the analytic model to determine circuit voltage

stress conditions. For the asymmetric **OL** operation use case of fig. 6.7, mismatch at the input pair yields:

$$\begin{aligned}\Delta V_{in,UC} =& \Delta V_{th,M_{n2},UC} - \Delta V_{th,M_{n1},UC} \\ =& \left(AGE_{UC}\right)^n - 0 = \Delta V_{th,M_{n2},UC},\end{aligned} \quad (6.12)$$

as according to sec. 6.2.2, only $\mathbf{M_{n2}}$ is significantly affected by the stress condition. The application of a preliminary symmetric 'Burn-In' stress prior to the asymmetric **OL** stress, inducing k times the AGE level of the use case, results in:

$$\begin{aligned}\Delta V_{in,B+UC} =& \Delta V_{th,M_{n2},B+UC} - \Delta V_{th,M_{n1},B+UC} \\ =& \left((k+1)\cdot AGE_{UC}\right)^n - \left(k \cdot AGE_{UC}\right)^n \\ =& \left((k+1)^n - k^n\right)\Delta V_{th,UC}.\end{aligned} \quad (6.13)$$

As time exponent of (3.6) is approximately $n \approx 0.2$ [79] and for $k > 1$, aging induced mismatch is significantly reduced due to the sublinear BTI behavior (see fig. 6.24).
Furthermore, in addition to the 'Burn-In', a 'Calibration' sequence can compensate for

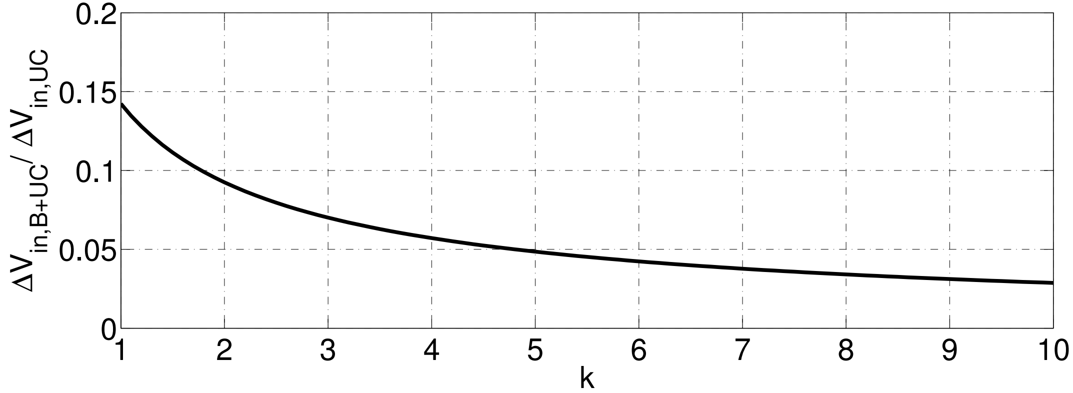

Fig. 6.24: General aging induced offset suppression ability due to preliminary symmetric 'Burn-In'.

preliminary existing mismatch. Via preliminary offset measurement on the virgin circuit and solving (6.14), an asymmetric **OL** stress condition can be found to adjust circuit mismatch via $V_{off,in} = -\Delta V_{in,C}$ of the input pair:

$$\begin{aligned}\Delta V_{in,C} =& \Delta V_{th,M_{n2},B\&C} - \Delta V_{th,M_{n1},B} \\ =& \left(AGE_B + AGE_C\right)^n - \left(AGE_B\right)^n.\end{aligned} \quad (6.14)$$

The found stress conditions at the input pair then have to be transformed to corresponding ones on circuit level via back calculation with the analytic model.

Aging Use Case and Stress Configuration

In the following study a MP/EOL (see sec. 3.8) use case for the amplifier is assumed and concept is evaluated according to this aging scenario. Derived stress conditions for the

ACC (accelerated) MP use case, the 'Burn-In' and the 'Calibration' sequence are given in table 6.7. Similar to the preceding investigations, stress temperature and duration are preliminary set to 125°C and 1000s. Predicted effect contributions to the stress configu-

OL MP	$(105\%V_{DD,wc}$, 85°C, 4y$) \leftrightarrow (1.394 \cdot V_{DD}$, 125°C, 1000s)
Burn-In	$k = 10 \leftrightarrow (1.461 \cdot V_{DD}$, 125°C, 2000s)
Calibration	$(1.461 \cdot V_{DD}$, 125°C, $t_C)$

Table 6.7: Stress conditions for accelerated OL MP/EOL use case, 'Burn-In' with expected factor $k = 10$ and 'Calibration'.

rations are given in the decomposition plot in fig. 6.25. The equivalent acceleration stress

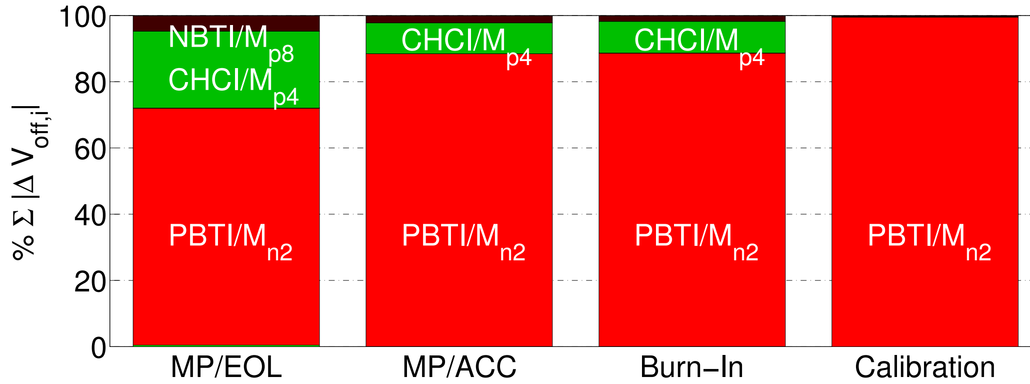

Fig. 6.25: Effect decomposition plot to corresponding stress conditions in table 6.7. 'Burn-In' contributions are given as asymmetric stress affecting only half of the circuit. 'Calibration' assumes a stress duration of 1000s.

condition according to the MP/EOL use case is derived as described in sec. 6.4.1. 'Burn-In' is performed by applying the **OL** operation scenario with a raised supply and input voltage and a stress condition inducing $k = 10$ times the PBTI *AGE* level in the input pair in relation to the MP/EOL use case. This leads to a considerable reduction of aging effects in subsequent use cases, but input pair degradation is still limited such that the tail current source $\mathbf{M_{n5}}$ safely operates in saturation region. As given in fig. 6.25, this stress configuration further activates effect saturation in all other devices providing only second order contributions to the overall offset. An alternating switching of the 'Burn-In' stress condition at amplifier's input generates the needed symmetric stress configuration and all matched pairs degrade equally. Therefore, 'Burn-In' duration is doubled to 2000s. So, all induced drifts are canceled by the circuit itself and zero generated offset is expected. For the 'Calibration' stress, only one input voltage is rised and the supply is kept at nominal V_{DD}. As already revealed in fig. 6.13 and given in fig. 6.25 for the derived stress configuration, this adapted **OL** stress condition mostly affects the input pair. This is needed to perform an accurate offset calibration only via directed drifts at the input pair. For the 'Calibration' sequence the same input stress voltage as for the 'Burn-In' is used. Individual drift calibration is performed via adjusting stress time.

Burn-In and Calibration Stress Sequence

Fig. 6.26 shows the stress processing for the 'Burn-In' and 'Calibration' approach. After

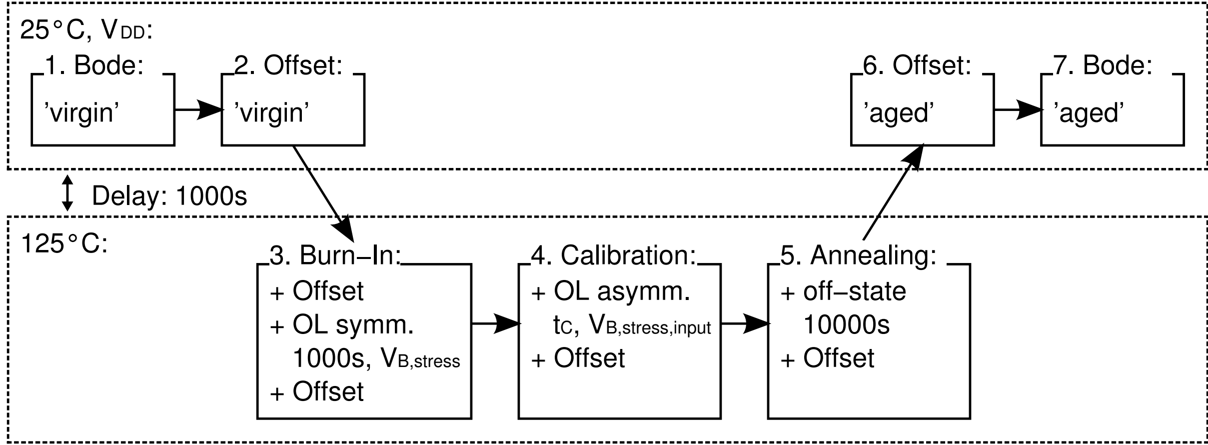

Fig. 6.26: Stress test sequence for amplifier Burn-In and Calibration sequence. Each offset measurement is performed for 100s at nominal supply voltage.

a characterisation of the virgin amplifier sample for offset and transfer behavior under nominal circuit conditions, the sample is heated to 125°C with a temperature annealing delay of 1000s. Before 'Burn-In' stress, offset is again measured at elevated temperatures and nominal supply voltage. The 'Burn-In' stress condition is alternated switched between the input pair devices with a frequency of 10 Hz. After 'Burn-In', offset is again evaluated for nominal supply voltage. The following asymmetric 'Calibration' stress is applied to circuit's input according to offset's prefix for the virgin sample and for a calibration duration dependent on its magnitude. After 'Calibration', offset is monitored and a high-T annealing sequence in off-state is applied for decay of considerable relaxing drifts. After annealing, offset is again measured for 125°C and after cooling the sample to 25°C offset and transfer characteristic is evaluated for the aged sample.
Stress processing for the accelerated MP use case performed after 'Burn-In' and 'Calibration' (fig. 6.27) is similar to that in sec. 6.4.1, but with included offset measurements at stress temperature and an additional high-T annealing step in off-state to monitor longterm stable offset drifts.

Concept Verification

The derived approach is approved with tests on 3 samples via the stress testbench from sec. 6.3. Stress testing is performed with a fully-automated implementation of the process sequences from the preceding section. For all 3 samples the asymmetric **OL** MP/ACC use case is applied, while samples S_1 and S_2 are preprocessed with the 'Burn-In'/'Calibration' sequence. The 'Burn-In' and 'Calibration' process diagram for S_1 run is depicted in fig. 6.28. It shows measurements of output referred offset performed for 100s each, between changes of stress conditions. As expected, results show that the symmetric 'Burn-In' stress does not induce further offset, thus does not change matching. A short time after

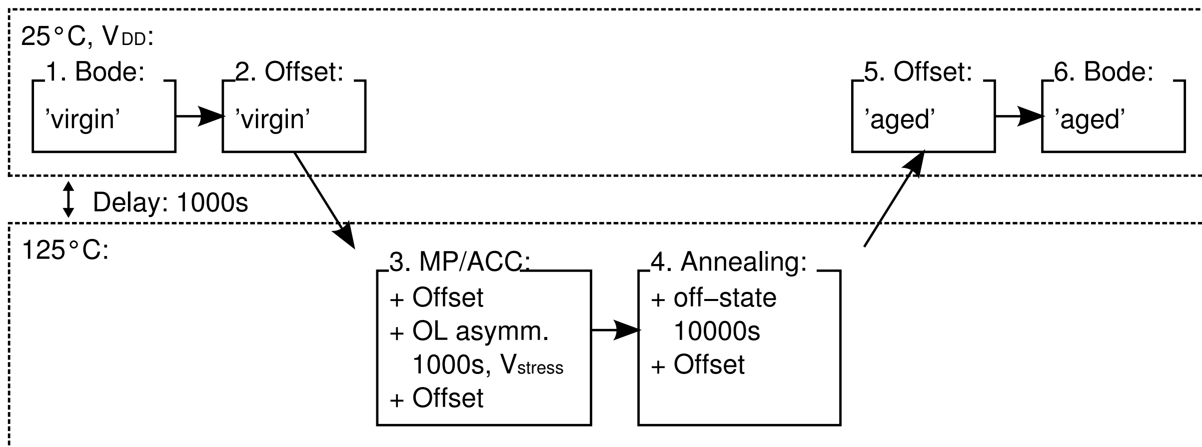

Fig. 6.27: Stress test sequence accelerated OL operation aging. Each offset measurement is performed for 100s at nominal supply voltage.

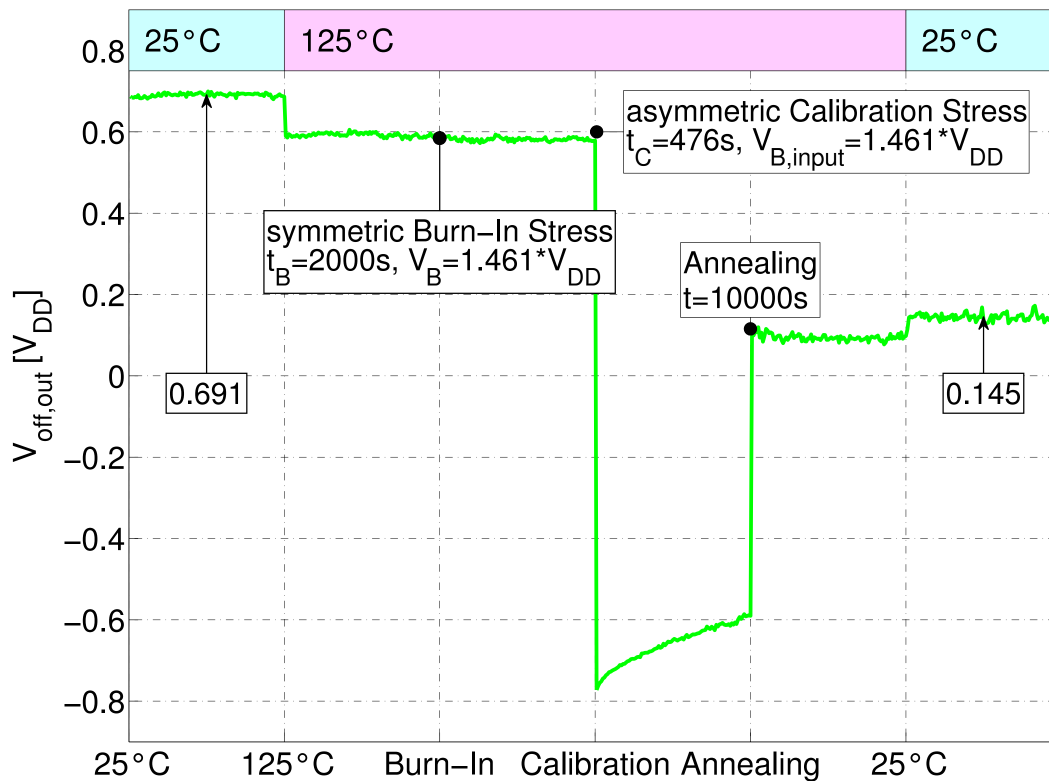

Fig. 6.28: 'Burn-In' and 'Calibration' process diagram: output referred offset measurements of sample S_1 between 'Burn-In', 'Calibration' and 'Annealing' sequences, each for 100s.

'Calibration', offset shows relaxation that decays after the annealing step. The reference measurement at the end of the procedure shows a significant offset reduction. The ben-

efit of 'Burn-In' can be seen in the diagram of fig. 6.29: it compares application of the asymmetric MP/ACC use case to the virgin amplifier S_3 and to the pretreated S_1 one week after 'Burn-In' and 'Calibration'. Comparing the final offset of S_1 in fig. 6.29 with

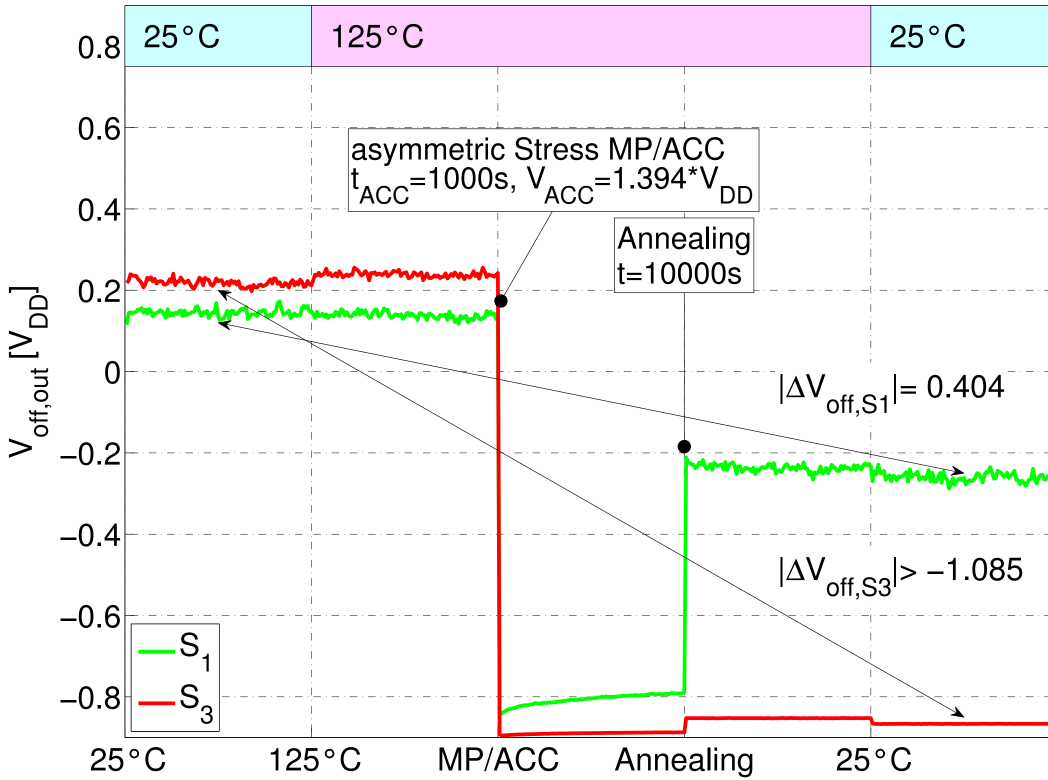

Fig. 6.29: MP/ACC process diagram: output referred offset measurements before and after asymmetric OL stress, each for 100s.

the starting value in fig. 6.28 reveals that this approach generates a longterm stable calibrated offset. Due to the 'Burn-In', accelerated use case stress induces only small offset drifts compared to the virgin S_3, which had no Burn-In. As the amplifier output is driven into saturation, mismatch is partly masked by the amplifier's voltage headroom. Therefore, table 6.8 shows measured input referred offsets, revealing a significant offset generation suppression of nearly 90% in $\Delta V_{off,MP}$ due to the 'Burn-In'. It also shows results of sample S_2, exhibiting a large offset in virgin state. Here, 'Burn-In' and the individual 'Calibration' also reveals a significant offset reduction. The following application of the MP/ACC use case condition provides a similar suppression ability as for S_1, which confirms this approach. Comparing the bode diagram for all 3 samples (not shown) in virgin and after 'Burn-In'/Calibration as well as MP/ACC stress treatment, reveals the expected negligible impact on the transfer characteristic for all use cases.

As already expected from the findings in sec. 4.2.5, these measurement results reveal that the suppression ability is only valid for longterm 'permanent' aging drifts. Fast relaxing

Sample	$V_{off,vir}$	t_C	$V_{off,B\&C}$	$V_{off,MP}$	$\Delta V_{off,MP}$
S_1	0.769	476s	0.170	-0.244	-0.414
S_2	1.255	862s	0.255	-0.117	-0.372
S_3	0.230	—	—	-2.710	-2.940

Table 6.8: Input referred offset (in mV) before and after 'Burn-In' and 'Calibration' (S_1, S_2) and corresponding calibration period. Further offset behavior after application of MP/ACC use case stress condition. All measurements for longterm, stable offsets after annealing and at nominal supply, 25°C.

parts cannot be suppressed by this approach. Thus transient offset drifts after worst case stress conditions has to be covered by design margins. At this point, novel aging prediction models providing all effect contributions and recovery behavior would be preferable for proper and reliable design. Nevertheless, the general ability to calibrate permanent drifts helps to stabilize differential structures in a way that only margins for the relaxing parts have to be covered, and in addition process or layout given mismatch can be calibrated. This ex post calibration offers new opportunities for the choice of smaller device dimensions with respect to matching constraints.
Recovering drift contributions further disqualify algorithmic approaches combining both the 'Burn-In' and 'Calibration' sequence in one asymmetric stress condition, which are applied to the amplifier circuit according to an algorithmic evaluation of instantaneous offset levels. Such a measurement example is given in fig. 6.30. Here, an alternating sequence of 10s asymmetric stress followed by a 20s offset measurement is applied. As total stress duration is expected to be shorter than that from the preceding approach, voltage stress condition is chosen to be higher to generate sufficient effect saturation. As can be seen in fig. 6.30, in the end this approach enables a zero offset scenario, but as the calibration algorithm bases on offset measurement results incorporating recovery transient in the range $> 20s$ recovery time, a longterm stable compensation result cannot be achieved. This can be seen after the off-state, high-T annealing step for 30000s. Offset recovers back towards its virgin level. The wide timing span of recovery effects generally makes this kind of algorithmic approaches unsuitable for an offset calibration via degradation effects. To compensate for longterm stable drift values long recovery timings have to be considered, leading to unreasonable long calibration periods.
This study was proven by experiments using PBTI degradation at an nMOS input pair. Of course it is also valid regarding NBTI for pMOS input stages as both BTI effects show similar degradation behavior.

6.5 Summary

In amplifier circuits aging primarily generates circuit offset due to the change of device characteristics. Offset is mainly induced for open-loop or comparator operation where high asymmetric voltage stress occurs at the input. For common closed-loop operation, feedback control leads to a stabilisation of input voltages to moderate levels. Here, only

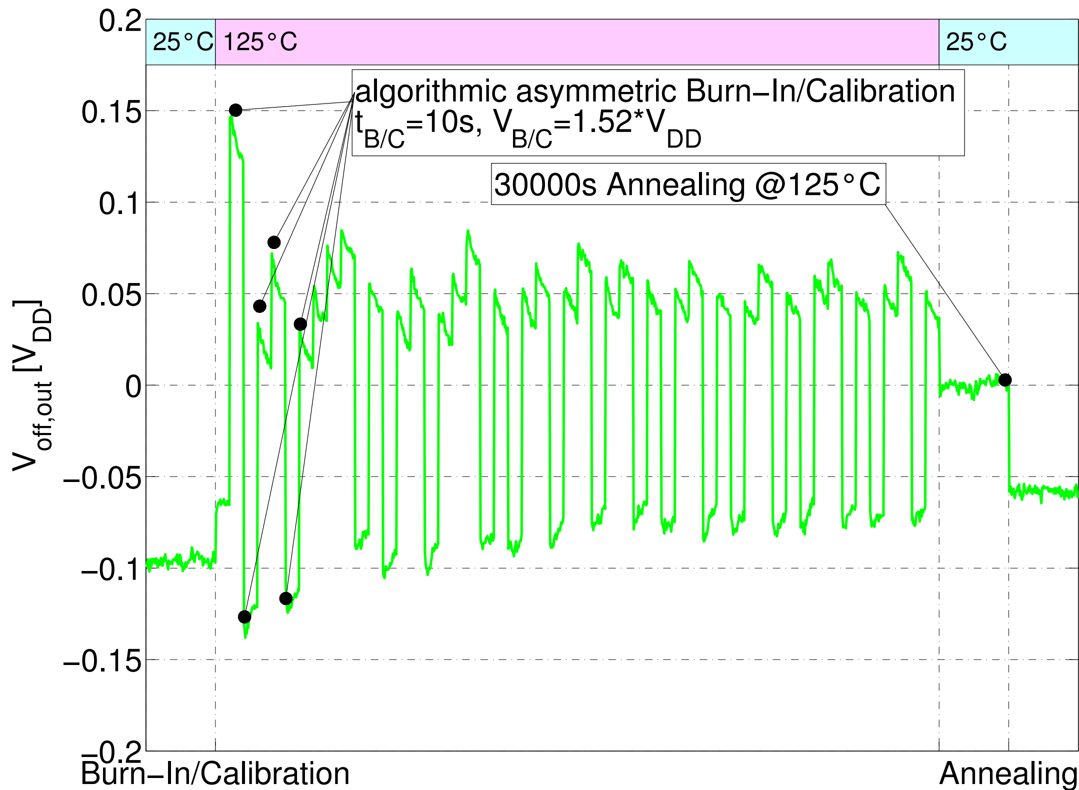

Fig. 6.30: Process diagram of an exemplary algorithmic approach of combined 'Burn-In' and 'Calibration'.

output nodes or output stages can operate at high voltage swing leading to minor induced offset drifts. Anyhow, arising aging effects in advanced CMOS technologies produce increasing offset levels even in closed-loop operation. The general differentiation in voltage biased and current biased amplifier structures revealed a higher sensitivity of the voltage biased topologies towards aging effects. Here, the aging induced drift of operating point further affects other performance parameters as gain or GBW. For current biased structures operating point is stabilised due to current biasing and other parameters besides offset are only minor affected. For both types, the performance characteristic is fully restored after offset compensation. Complex amplifier structures also show a complex aging behavior due to interaction of numerous degradation effects occurring during operation. All effects contribute as a weighted sum to the overall amplifier offset. But also effect masking results due to distinct offset drift directions induced by arising effects, revealing that observable offset must not represent full inner circuit drifts.
The approach of a full analytic description of circuit behavior towards device aging is performed via the small signal circuit equivalent - a linearized description of amplification behavior in the operating point - and resulting degradation values from the aging prediction models as input signals. Nevertheless, arising voltage stress conditions as input for the aging models have to be further modeled with respect to a change of external cir-

cuit stress conditions like supply and input voltages or temperature and circuit operation state as well, as the circuit description evaluates device aging impact in the optimal operating point *after* a corresponding stress operation. Comparisons with large signal circuit simulations revealed a powerful and accurate offset prediction with many advantages in relation to the circuit simulation approach. The model further enables to investigate circuit aging behavior towards changes in stress conditions (V, T, t), to decompose for single effect contributions and to perform back calculation from degradation effect to external circuit stress conditions, offering the development of new circuit level aging concepts. The investigation on a complex, two stage amplifier revealed that in open-loop operation BTI at the input pair acts as the major offset generating contributor.
The model revealed that for complex amplifiers numerous effects contribute to the overall generated offset and circuit aging behavior is unique for a given set of external stress parameters (V, T, t). So an exact aging acceleration via stress testing as it is done for device aging effects is not possible. Anyhow, a best fit can be achieved if at least the dominant aging effect contributor provides the same aging level as for end-of-lifetime conditions. Here, the analytic model approach offers to derive corresponding stress conditions. Stress measurements on hardware with derived accelerated EOL stress conditions proved this concept. This method further offers to use analog signal processing of the circuit to investigate for other impacts of aging on device characteristics like aging recovery behavior or a change of device noise characteristics in EOL states.
Further tests on the impact of effect recovery on the amplifier's offset behavior were performed for closed-loop and open-loop stress scenarios, with equivalent stress conditions in the range of hours and several days. Results revealed that due to vast timing spans, effect recovery can interfere with significant magnitudes in wide bandwidths and thus disturb signal processing. Here, a thorough recovery modeling is needed for proper and reliable circuit design and dimensioning of circuit level countermeasures.
A design level countermeasure to reduce aging impact, suitable for circuits in SiO_2 CMOS processes, is the usage of nMOS input pairs as here major BTI contributions are omitted due to negligibly small PBTI in nMOS devices. Another possibility is derived by a universally valid suppression and calibration approach beneficially using general BTI drift and saturation behavior. A significant suppression of aging induced offsets can be achieved by a preliminary symmetric 'Burn-In' to saturate effects without changing matching behavior. A following directed drift by asymmetric stress can further compensate for process or layout given asymmetries. This concept was derived via the analytic circuit model and proven on hardware. An aging suppression ability of more than 90% and a significant offset calibration were achieved. This ex post suppression and calibration method further offers to choose smaller device dimensions with respect to matching during the design. Here, effect recovery also played a significant role and it was shown that fast recovering degradation parts are not affected by the 'Burn-In' sequence and thus cannot be suppressed and have to be covered by design margins.
Parts of these investigations and findings were published on international conferences [94, 103, 97].

Chapter 7

LC-Oscillators

Oscillator circuits are typically employed as frequency reference or carrier frequency generator. These are mostly built with an adjustable oscillation frequency controlled by an input voltage and are thus called VCO. VCOs are used in free running mode or in a stabilized closed-loop control in a PLL (Phase Locked Loop). For oscillators the most important performance parameter is the stable frequency generation.
Oscillator circuits are in the focus of reliability investigations due to their full swing operation that is often designed to even exceed the supply voltage. Here, high degradation levels of the incorporated MOSFET devices can occur, leading to a shift of circuit performance. Device aging impact related to end-of-lifetime circuit operation is investigated in the following study.

7.1 Circuit Fundamentals

The circuit core of of an LC based oscillator is given in fig. 7.1. It is called *LC-tank* and

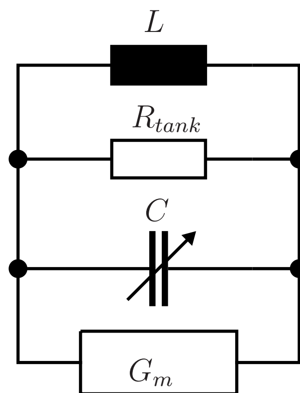

Fig. 7.1: Schematic of the oscillating LC-tank of a LC-VCO.

provides a stable oscillation at the resonance frequency $\omega_c = 2\pi f_c = \frac{1}{\sqrt{LC}}$, if losses in the tank, modeled in R_{tank}, are compensated by an active circuit part G_m. In the stable

oscillation state $G_m = -\frac{1}{R_{tank}}$, thus the active circuit block provides a negative resistance that balance losses and maintains the oscillation. In integrated CMOS processes, losses in an LC-tank are mainly related to the coil. Here, a lot of development effort is put in the design of integrated coils with high quality factors Q_L [104, 92]. For VCOs, the frequency tuning ability is typically performed via variable capacitors called *varactors* (see sec. 4.1.5).
The active circuit to provide the power for oscillator startup and stable operation is provided by a *positive feedback* configuration, that is mostly implemented with a *cross-coupled* MOSFET pair, with or without additional bias current source. This active circuit part is also known as *active bridge*. Two exemplary implementations of an active bridge as *current-biased* nMOS version with nMOS tail current source and a *voltage biased* current-reusing topology are given in fig. 7.2 [92]. As oscillation amplitude for the given

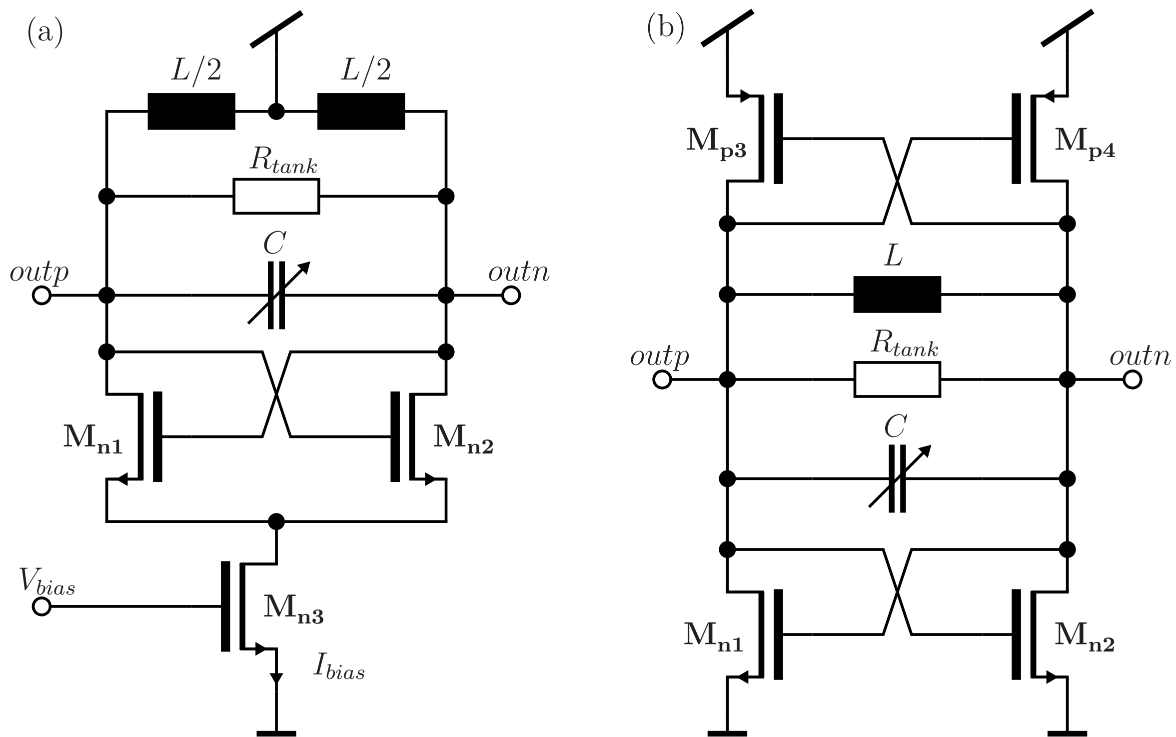

Fig. 7.2: Schematics of two exemplary VCO implementations: (a) nMOS only topology with tail current source for current biasing and (b) CMO current-reusing topology using voltage biasing.

current-biased circuit can reach up to $2 \cdot V_{DD}$, the power supply has to be reduced to a smaller value for reliable operation of the active bridge. However, for the voltage-biased current-reusing topology, amplitude is limited by the given voltage supply. A detailed study on the properties of each topology is treated in [105]. For circuit startup, the cross-coupled pair provides a small signal impedance of $\frac{1}{G_{m,start}} = -\frac{2}{g_{m,n}}$ for the current biased topology and $\frac{1}{G_{m,start}} = -\frac{2}{g_{m,n}+g_{m,p}}$ for the voltage biased circuit. For reliable oscillation startup, $|G_{m,start}| > \frac{1}{R_{tank}}$ has to be chosen to provide larger absolute admittance than that due to the tank losses. For current biased structures $G_{m,start}$ is defined by the bias

current I_{bias}, whereas for the voltage biased structures $G_{m,start}$ is set by the voltage levels for startup conditions, which is in the range of $\frac{V_{DD}}{2}$ for the given current-reusing topology. When oscillation is built up, increasing amplitudes lead to nonlinear operation of the active bridge devices and to a reduction of the effective G_m. A steady state oscillation amplitude is maintained when $|G_m| = \frac{1}{R_{tank}}$ cancels the tank losses, where G_m is the cycle average.

7.1.1 VCO Performance Characteristics

The most fundamental and device aging related VCO performance parameters are briefly introduced in the following sections. Besides the adjustable frequency bandwidth, the purity of the output frequency that can be interfered by the noise of the incorporated devices, is a major performance characteristic. Also perturbations from the noisy power supply (pushing) and design characteristics like chip area and power consumption play an important role for the application in integrated systems.

Frequency Tuning-Range

In integrated CMOS technologies, it is much easier to implement tunable capacitors instead of tunable inductors. As already described in sec. 4.1.5 the highly non-linear MOS capacitance between Gate and Substrate can be used as varactor with a tuning control via the Source/Drain junctions. In inversion mode, the back-biasing effect provides a shift in threshold voltage via the variation of Source/Drain voltage. This impacts the C-V characteristic, leading to a voltage adjustable effective capacitor value [32, 92]. Furthermore, switchable arrays of classic on-chip capacitors are also used to provide a digital controlled *coarse* tuning resulting in a stepwise selection of oscillator frequency.
The parameter *tuning range* describes the regime from the lowest to the highest adjustable oscillation frequency.

Phase Noise

Phase Noise provides information about the spectral purity of the VCO. During oscillation noise interference from incorporated devices impact amplitude and phase, leading to a broadening of the power spectrum around ω_c. In practical oscillator implementations amplitude is limited by circuit nonlinearities and mostly the phase component is affected [106]. Phase Noise is defined as

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{\mathcal{P}_{sideband}(\omega_c + \Delta\omega)}{\mathcal{P}_{carrier}(\omega_c)}\right), \tag{7.1}$$

the single sideband noise power of the output voltage at a given offset frequency $\Delta\omega$ from the carrier ω_c in Hz, normalized to the power of the carrier. It is given in decibels below the carrier $\frac{dBc}{Hz}$. For typical VCO circuits, Phase Noise can be divided into three regions. For high offset frequencies, a constant noise floor is observed that is related to circuitry

in the output signal path. In the medium range $\mathcal{L}(\Delta\omega)$ shows a $\frac{1}{\Delta\omega^2}$ behavior induced by thermal noise components. Close to the carrier $\mathcal{L}(\Delta\omega) \sim \frac{1}{\Delta\omega^3}$, that is dominated by $\frac{1}{f}$-noise of the MOS devices. The most important models to describe Phase Noise in dependence on design related parameters are given by Leeson [107], Craninckx [108], Hajimiri [109] and Rael [110]. Up to now, Phase Noise prediction is a challenging task as some phenomena and relations are still not fully understood.

Amplitude

Dependent on the circuit topology, operation regions can be distinguished. For current biased structures (fig. 7.2 a)), the circuit operates in the *current-limited* region as long as the tail current source is in saturation. Here, oscillation amplitude is directly related to the bias current. For higher amplitudes, current source enters triode region and circuit operates in the *voltage-limited* region. The amplitude is clipped to the maximum level $2 \cdot V_{DD}$ given by the supply voltage. For voltage biased topologies (fig. 7.2 b)) such a distinction cannot be made. For these topologies, amplitude is defined by the current driving ability of the active bridge devices and is hard limited by the supply voltage.

7.1.2 Design Fundamentals

A general rule of thumb to meet Phase Noise limitations can be derived from eq. (7.1). Maximisation of the signal power, thus maximizing signal amplitude, generally yields to reduced Phase Noise levels. Due to this relation, most VCO circuits perform oscillation with maximum amplitude. There are techniques to even exceed the supply voltage limitations and further improve Phase Noise behavior. This implies circuit operation in the voltage-limited or around the supply voltage limit region, leading to inefficient high power consumption. However in these regions, sensitivities of amplitude and Phase Noise towards PVT variations are reduced at the cost of additional power consumption yielding to robust circuit operation [105]. Thus, most practical VCO implementations operate with maximum swing to provide adequate circuit robustness.
Sizing of active bridge devices strongly depends on the used topology, whether a current bias source is used or not and is strongly related to device noise upconversion sensitivity to oscillator Phase Noise. For simplicity, a throughout discussion about 'correct' dimensioning is omitted at this point, which is covered by CMOS LC VCO related textbooks [104, 92]. As a general rule of thumb, cross-coupled pair devices should provide a fast g_m driving ability with minimum loading of the LC tank. This implies the usage of devices providing minimum gate lengths [111, 112]. For tail current source devices typical design constraints for current mirror circuits from sec. 5.2.2 can be used. Sizing of MOS varactors depends on the interpretation of the trade-off between high tunable capacitance values and allowed gate resistance, which reduces the quality factor of the tank. This mostly results in varactor dimensions of wide devices providing gate lengths $L \approx 2 \cdot L_{min}$. Design of integrated coils with high quality factors in on-chip metalisation layers is a challenging and process related task [92] and is not further discussed in this study.

7.1.3 Exemplary Circuit Topologies and Design Flow

To provide a universal VCO aging case study, the two circuit topologies from fig. 7.2 are used to compare and investigate exemplary current and voltage biased VCOs with respect to their individual aging behavior. To consider circuit level aging, circuits are developed in the 32nm high-κ, metal gate CMOS technology [91] with basic thin oxide digital core devices. The findings, revealed by the MOS varactor study in sec. 4.1.5, that device aging negligibly impacts capacitor tuning behavior for operation with amplitudes in the allowed voltage range, implies the design of the oscillator circuits with fixed and linear tank capacitors to solely study the impact of the active bridge aging on the performance parameters.
Both circuits are designed to provide a $G_{m,start} \approx 3 \cdot \frac{1}{R_{tank}}$ for proper startup and stable circuit operation with nearly full swing amplitude. For the current-reusing oscillator nMOS and pMOS devices are designed to provide equal $g_{m,n} = g_{m,p}$ contributions. Supply voltage for the current biased circuit is set to a value higher than $\frac{V_{DD}}{2}$ to provide similar oscillation amplitudes. So, active bridges will degrade in a similar manner, revealing a general aging sensitivity related to the topologies. Both circuits are built with an equivalent integrated coil and are adjusted via adapting tank capacitances to oscillate at 3 GHz. This is necessary as both topologies provide different loading of the tank due to the individual type of active bridge. Further design properties are given in table 7.1.

	current biased	voltage biased
single ended L	409pH	409pH
single ended C	6.6pF	6.3pF
active bridge nMOS	$\frac{70u}{L_{min}}$	$\frac{34u}{L_{min}}$
active bridge pMOS	n.a	$\frac{60u}{L_{min}}$
current source nMOS	$\frac{800u}{4L_{min}}$	n.a.
supply voltage V_{DD}	$0.85 \cdot V_{DD}$	V_{DD}
supply current I_{RMS}	8.8mA	4.4mA

Table 7.1: Design parameters for the circuits in fig. 7.2 used in the oscillator aging study.

7.1.4 Circuit Operation induced Device Aging

After circuit startup, the oscillator provides an enduring oscillation. Fig. 7.3 depicts the exemplary sequence of the current-reusing oscillator from fig. 7.2 b) during stable oscillation. The sequence reveals, that during oscillation devices of the active bridge are exposed to alternating stress conditions. In the region of signal transition, when $V_{outp} \approx V_{outn}$, active bridge devices operate in saturation under **MM**[1] operation. Generated CHCI

[1] $V_{GS}V_{DS}$ voltages - L:low, M:moderate, H:high

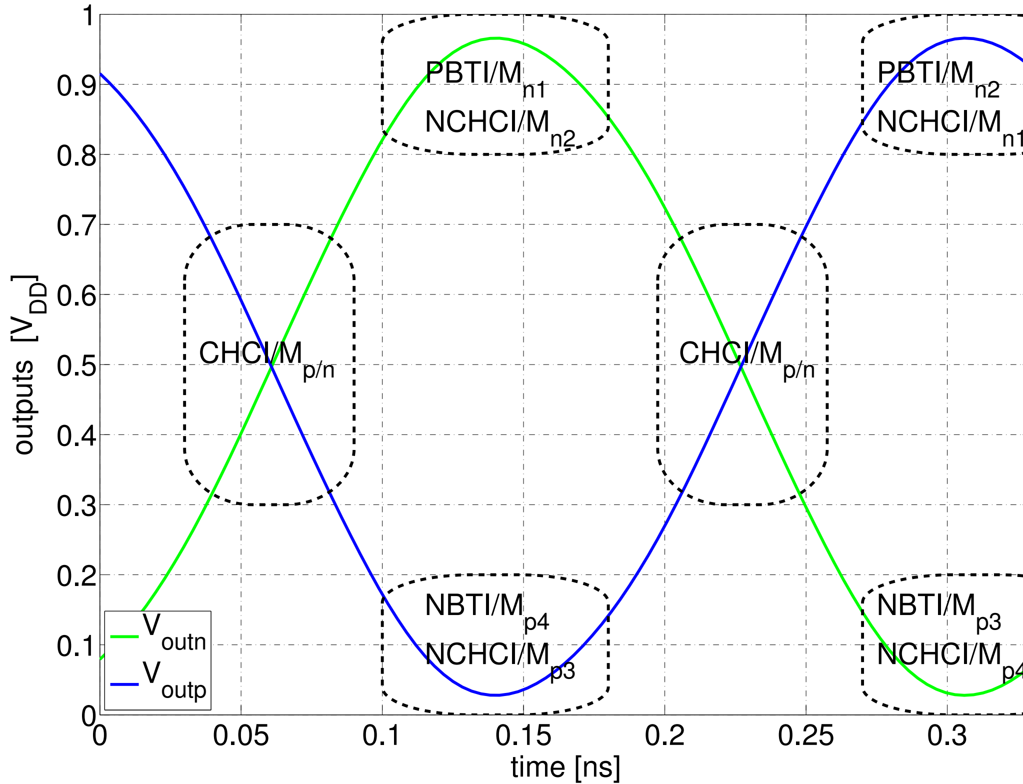

Fig. 7.3: Periodic oscillation sequence of the current-reusing oscillator from fig. 7.2b) under nominal supply voltage and 25°C and arising device stress conditions.

degradation should be negligibly small under these moderate bias conditions despite the small gate lengths. However, when signals reach peak voltage, active bridge devices operate in **HL**[1] and **LH**[1] mode, inducing significant BTI degradation and, due to the small gate length, also significant NCHCI degradation. Expected device aging behavior is similar to digital device operation aging in fig. 4.1, but without the major CHCI contributions due to relaxed sinusoidal transition regions. It is also in the peak voltage state, when MOS varactors are exposed to the BTI relevant **HL**[1] state.
For the current biased topology in fig. 7.2 a) oscillation sequence and active bridge stress states are similar, but limited to nMOS device degradation. Aging of the tail current source $\mathbf{M_{n3}}$ (current mirror topology) is expected to be negligibly small due to the stable **MM**[1] device operation state. Aging relevant operation states, that were studied in sec. 5.3 in detail, will not occur and a relevant degradation of the bias current is not expected.

7.1.5 Circuit Aging and Affected Parameters

For the following circuit aging investigation, the MP/EOL operation use case from sec. 3.8 is assumed. Device aging results and individual impact on the performance of the current and voltage biased oscillator obtained from RelXpert™ simulations in the 32nm

high-κ metal gate CMOS process [91] are given in table 7.2. For both circuit topologies, BTI and NCHCI effects play the major role, whereas CHCI contributions are negligibly small. As already expected, the tail current source device $\mathbf{M_{n3}}$ shows only minor degradations. Small BTI induced ΔV_{th} drifts even cancel due to a current mirror biasing configuration for $\mathbf{M_{n3}}$ (cf. sec. 5.3). So, circuit bias current is hardly affected by device aging and can be considered as stable over lifetime. For both circuit types, absolute de-

	current biased nMOS pair & current source (fig. 7.2 a))			voltage biased nMOS & pMOS pair (fig. 7.2 b))		
	CHCI[1]	NCHCI[1]	BTI[2]	CHCI[1]	NCHCI[1]	BTI[2]
$\mathbf{M_{n1/2}}$	6.6E-3	1.5	1.2	2.4E-2	2.18	2.4
$\mathbf{M_{n3}}$	1.7E-5	0	4.5E-3	n.a.		
$\mathbf{M_{p3/4}}$	n.a.			2.3E-2	5.2E-1	4.1
	circuit performance degradation in %					
$I_{supply,RMS}$	0.07			2.22		
V_{outp}	0.02			0.3		
$\mathcal{L}(3MHz)$	0.02			0.3		
$\mathcal{L}(100kHz)$	0.04			0.6		

Table 7.2: Oscillator performance degradation

vice degradations are of similar dimensions, but general aging sensitivity of performance parameters strongly depends on the topology. In both cases, a major impact of device aging can be seen in the degradation of supply current, which is very small for the current biased circuit and by the way of comparison quite high for the voltage biased oscillator. Both circuits show only small degradation in amplitude and Phase Noise behavior, which can be related to the robust implementation with operation with nearly full swing amplitude [105]. This result is similar to the findings comparing current and voltage biased amplifiers from sec. 6.1.5. Those revealed a high sensitivity of voltage biased structures towards device aging. Also for oscillators, characteristics of the cross-coupled pair devices are stabilized in spite of their degradation via the stable current biasing. So, contrary to the voltage biased oscillators, circuit performance is maintained.
For the voltage biased current-reusing oscillator, device degradation further reduces *startup* ability of the active bridge as $g_{m,n}$ and $g_{m,p}$ are directly affected by the induced device weakening. Considering a supply voltage limit for proper oscillation startup as $V_{DD,start}$, the aging of the cross-coupled pair devices would result in a raised startup supply voltage $V_{DD,start,virgin} < V_{DD,start,aged}$ for the aged circuit. When comparing the circuit aging monitors supply current degradation with the startup supply voltage enhancement, the latter exhibits, besides the easy access during circuit testing, the plus

[1] in $\% I_D$
[2] in mV ΔV_{th}

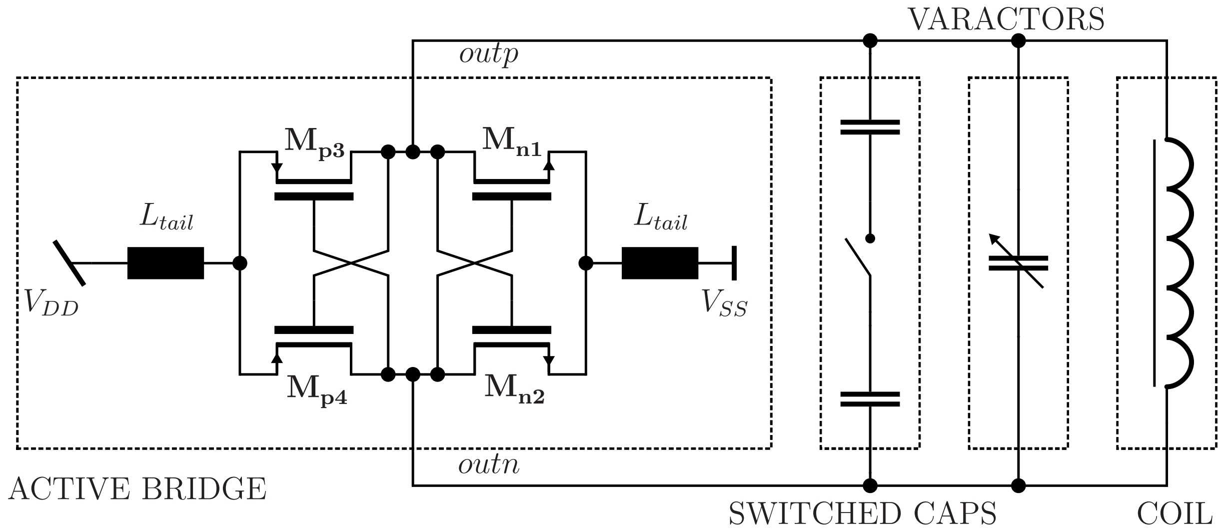

Fig. 7.4: Schematic of the differential GSM LC-VCO implemented in current-reusing topology.

that circuit behavior during startup condition can be described by the well known *small signal* approach, offering novel opportunities for aging behavioral modeling.

7.1.6 State-of-the-Art LC-VCO

For the following aging investigations, a state-of-the-art LC-VCO designed for GSM applications is used. Fig. 7.4 depicts the corresponding schematic of the current-reusing topology. This structure is employed to reduce power consumption, with respect to oscillators with one cross-coupled pair. The circuit is implemented in the 32nm high-κ metal gate CMOS technology providing medium oxide devices [91] to sustain high voltage swing and meet GSM Phase Noise specifications. Tail coils provide high impedance at the supply and ground nodes and maximize voltage swing. The design provides a combined tuning scheme of coarse and analog tuning to achieve the wide tuning range of the 3.0-4.3 GHz band. Further information concerning the design and performance of the VCO can be found in [113, 114]. This VCO is available as standalone hardware in the 32nm high-κ metal gate CMOS technology [91] including low noise on-chip RF output buffers for further stress measurements.
Predicted circuit performance degradations after MP/EOL (see sec. 3.8) operation, evaluated via RelXpert™ are given in tab. 7.3. Operation frequency during reliability simulation was set to the lower limit of 3.0 GHz. RelXpert™ evaluated device degradations showed only relevant BTI contributions as NCHCI is negligibly small for the medium oxide active bridge devices. Circuit simulation results reveal a general minor impact of device aging on important performance characteristics for an operation in the allowed supply voltage regime, which can be mainly related to the robust circuit design. As already expected from the findings in sec. 4.1.5, frequency tuning range is hardly affected by the degradation of the active bridge nor the varactors themselves (not shown). Even the aging monitor $V_{DD,start}$ only shows a moderate degradation value, caused by a well

Aging induced performance degradation in %	
$I_{supply,RMS}$	0.8
V_{outp}	0.6
$\mathcal{L}(3MHz)$ $\mathcal{L}(100kHz)$	0.1 0.2
$V_{DD,start}$	2.2

Table 7.3: 32nm GSM LC-VCO performance degradations due to device aging after MP/EOL operation, evaluated with nominal voltage supply and at 25°C.

controlled aging of the active bridge devices. Of course, $V_{DD,start}$ is also sensitive towards temperature or process variations. For example, a rise in temperature of from 25°C to 125°C would induce a drift in startup supply voltage of $\Delta V_{DD,start} \approx -6.3\%$. Corner simulations of the VCO reveal a variation of startup supply voltage in the range of $-13.3\% < V_{DD,start} < 9.6\%$ induced by process variations. So, for the MP/EOL operation use case on this VCO design, device aging still plays a secondary role besides temperature

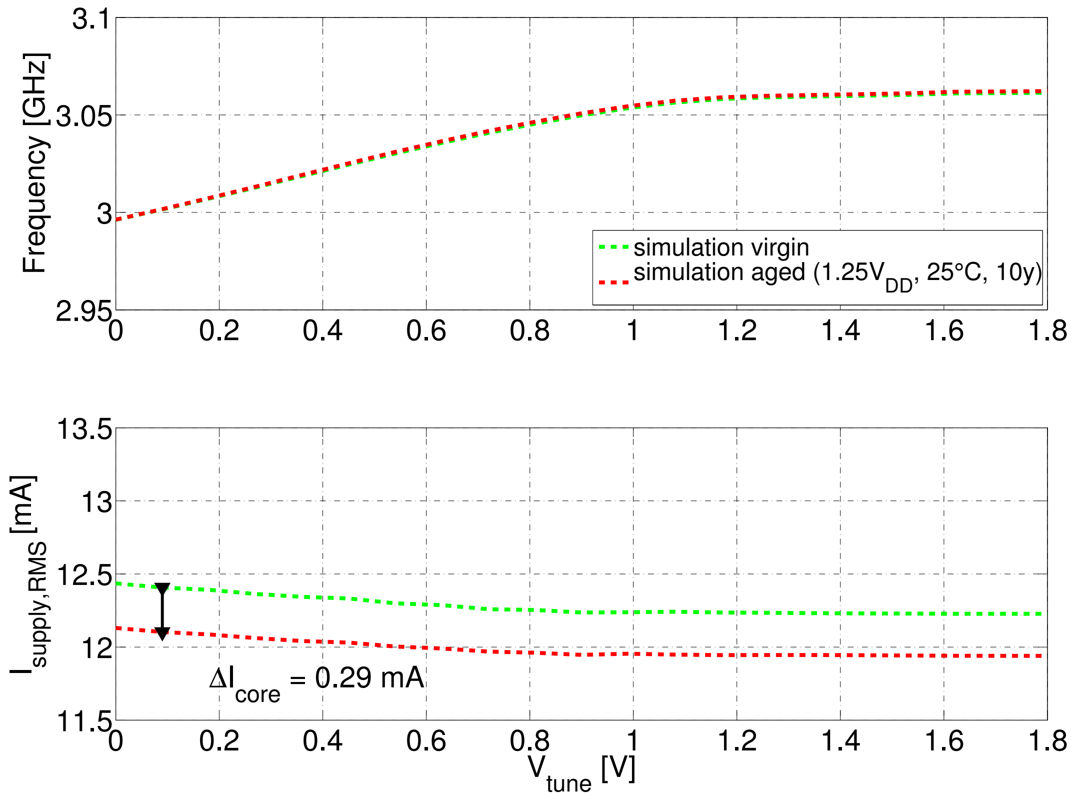

Fig. 7.5: Frequency tuning characteristic and supply current I_{core} before and after ($1.25V_{DD}$, 25°C, 10y) EOL operation. Simulations are performed with nominal supply voltage at 25°C.

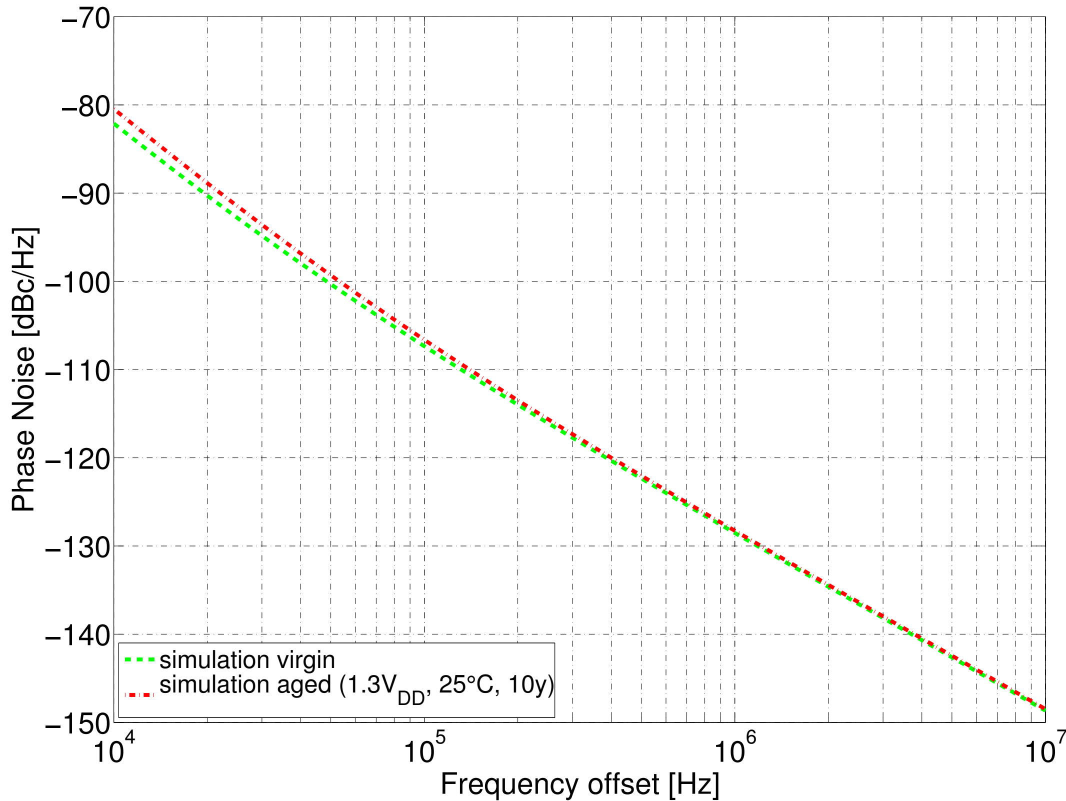

Fig. 7.6: Phase Noise characteristic before and after $(1.3V_{DD}$, 25°C, 10y) EOL operation. Simulations are performed with nominal supply voltage at 25°C.

or process variations.
Anyhow, for operation with increased supply voltage, the impact of device aging increases. For the EOL operation use case of $(1.25V_{DD}$, 25°C, 10y), $V_{DD,start}$ increases by 7.4%. Corresponding supply current degradation and frequency tuning behavior for an analog tuning at the lower bound 3GHz are given in fig. 7.5. As already stated for the MP/EOL operation use case, frequency tuning range is hardly affected by the device degradation, but the significant degradation in supply current is observable. A Phase Noise characteristic plot before and after $(1.3V_{DD}$, 25°C, 10y) circuit operation is depicted in fig. 7.6. For this worsened EOL operation case, $V_{DD,start}$ provides a degradation of 11.6%, but Phase Noise characteristic still shows minor impact. In the thermal region very small degradation of the Phase Noise behavior is observable, whereas in the close-in region Phase Noise degradation slightly increases, which is again the result of the robust circuit design.

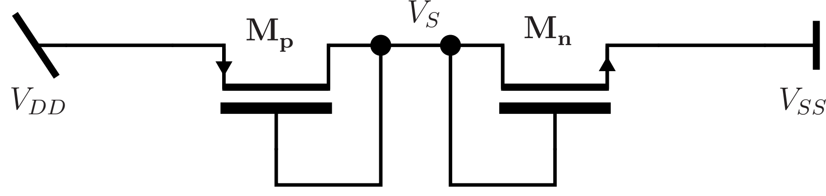

Fig. 7.7: Current-reusing VCO startup model.

7.2 LC-Voltage Controlled Oscillator Aging Model

Similar to the analytic circuit aging model derived via small signal equivalent modeling for amplifiers, a universal aging modeling approach can be derived for voltage biased LC-VCO circuits as well. Although a linearized small signal approach is unusual for oscillating circuits, as for full swing oscillation a linearized circuit model is not able to describe circuit behavior correctly, for circuit startup condition it proves to be suitable.

7.2.1 Analytic Model Derivation

When supply voltage slowly ramps up to start the VCO from fig. 7.4, the incorporated coils act as shorts and $V_{outn} = V_{outp}$. For this condition, one branch of the active bridge can be reduced to the equivalent circuit in fig. 7.7. For the oscillation startup point $\mathbf{M_n}$ and $\mathbf{M_p}$ devices provide a total

$$g_{m,start} = g_{m,n,start} + g_{m,p,start}, \tag{7.2}$$

whereas $g_{m,start}$ represents total G_m of the branch for $V_{DD,start}$, the lowest supply voltage to start oscillation. For startup of a virgin and an aged circuit we have to fulfill that

$$g_{m,start,virgin} = g_{m,start,aged}. \tag{7.3}$$

From (7.2) and (7.3) we can deduce in detail

$$\begin{aligned}
&\mu_n C_{ox}(\frac{W}{L})_n(V_{GS,n,v} - V_{th,n}) + \\
&\mu_p C_{ox}(\frac{W}{L})_p(|V_{GS,p,v}| - |V_{th,p}|) = \\
&\mu_n C_{ox}(\frac{W}{L})_n(V_{GS,n,a} - V_{th,n} - \Delta V_{th,n}) + \\
&\mu_p C_{ox}(\frac{W}{L})_p(|V_{GS,p,a}| - |V_{th,p}| - |\Delta V_{th,p}|)
\end{aligned} \tag{7.4}$$

with $\Delta V_{th,n}$ and $\Delta V_{th,p}$ BTI aging induced ΔV_{th} drifts. Device bias voltages in (7.4) can be expressed as $V_{GS,n,v} = V_S$, $|V_{GS,p,v}| = V_{DD,start} - V_S$, $V_{GS,n,a} = V_S + \Delta V_S$ and $|V_{GS,p,a}| = V_{DD,start} + \Delta V_{DD,start} - V_S - \Delta V_S$. For symmetric bridge design, $\mu_n C_{ox}(\frac{W}{L})_n \approx \mu_p C_{ox}(\frac{W}{L})_p$ and (7.4) reduces to the simple VCO aging model

$$\Delta V_{DD,start} = \Delta V_{th,n} + |\Delta V_{th,p}|. \tag{7.5}$$

For simplicity (7.5) considers only BTI aging of the active bridge (ΔV_{th}), but can be extended to also account for HCI degradation, that is typically predicted in a current degradation ΔI_D. This model is exemplarily derived for the current reusing VCO topology in fig. 7.4. This approach is universally valid and can be expanded to other voltage biased VCO structures, too.

7.2.2 Model Evaluation

For the following model evaluation an EOL circuit operation for 10y is assumed. The derived VCO aging model for the current reusing topology from the previous section is realized in MATLAB™. Furthermore, the model implementation estimates device operation stress voltages - the input for the aging model equations - in dependence of supply voltage and temperature variations via functional fitting to corresponding circuit simulation results. As aging model equations ((3.6) and (3.12)) do not support AC stress voltages, AC factors are derived via comparing RelXpert™ degradation results for the time varying stress with evaluated device drifts for DC stress at peak voltage. The evaluated AC factors are further considered in the VCO circuit model.

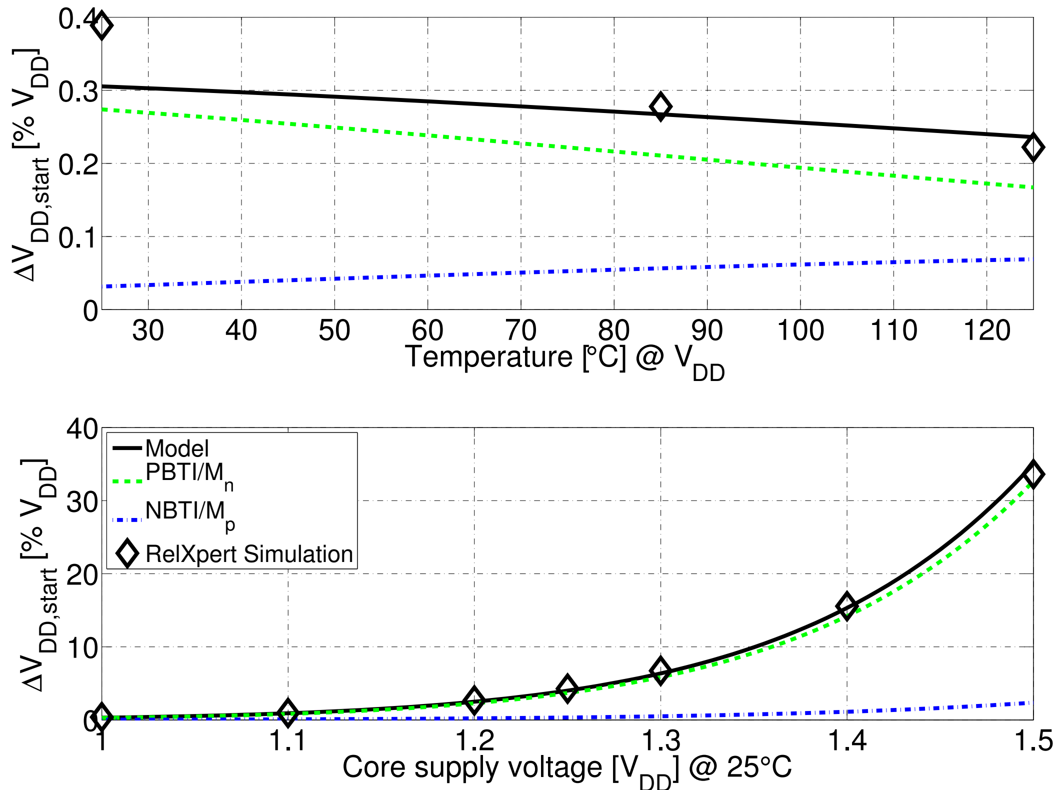

Fig. 7.8: Current-reusing VCO aging model vs. RelXpert™ simulation results for a 10y EOL operation and given stress condition. $\Delta V_{DD,start}$ is evaluated for nominal supply voltage and 25°C circuit operation.

Fig. 7.8 depicts the model based circuit aging prediction for the VCO in dependence of stress temperature and supply voltage. Comparing the results from the model with RelXpert™ based simulations confirms the accurate prediction approach of the model. It further reveals, that considerable circuit aging only occurs for elevated supply voltages. The rise of temperature even reduces degradation of the current VCO design. This can be related to a reduction of voltage amplitude induced by the temperature rise via reduced mobility. A main benefit of this model is the direct access to the effect contributions of the aging monitor $\Delta V_{DD,start}$. Contributions resulting from NBTI at $\mathbf{M_p}$ and PBTI at $\mathbf{M_n}$ are shown in fig. 7.8. Fig. 7.9 illustrates the composition of $\Delta V_{DD,start}$ in dependence of the stress parameters temperature and supply voltage. For both stress cases circuit

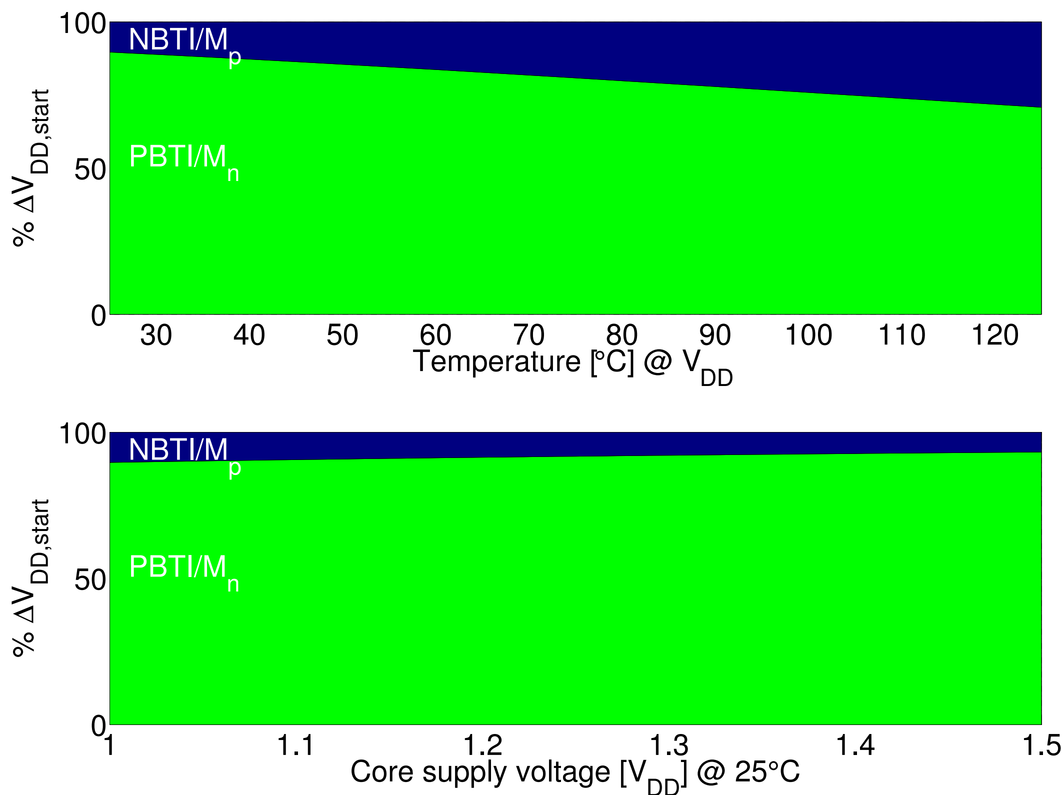

Fig. 7.9: Current-reusing VCO aging model effect decomposition for 10y EOL operation. Composition is valid for 25°C circuit operation.

aging is dominated by PBTI, but for temperature rise the ratio of PBTI and NBTI varies considerably, as the NBTI effect exhibits a larger temperature sensitivity as PBTI.

7.3 Stress Testbench

Stress testing for the verification of the derived concepts on the 32nm VCO hardware is performed via an automatized stress test assembly offering stress operation, frequency

tuning measurements with supply current monitoring as well as Phase Noise characterisation. For the measurements the VCO is bonded on ceramic RF boards and assembled in a shielded setup. Frequency tuning measurement is performed with an Agilent E4440A spectrum analyser. For the Phase Noise characteristics an Aeroflex PN9000 Test System using delay-line technique is employed. The differential to single ended conversion of the VCO RF output is performed with a Kritar 4010124 hybrid junction. For the Phase Noise characterisation a frequency downconversion is necessary to meet the range of the PN9000 system from 2 MHz to 1.8 GHz. This is performed via mixing VCO output with a low noise reference signal from an Agilent E8251A signal generator. Digital coarse tuning signals are generated by a custom PC based pattern generator board. Circuit biasing and analog tuning control voltages are provided by Agilent E3646A power supplies including capacitive filtering to reduce noise contributions. Core voltage supply and corresponding current measurement are performed with an accurate Keithley 2400 source meter. A thermostreamer controls circuit temperature during the measurements. The automatized PC based control of the measurement equipment enables reliable and reproducible stress measurements. Another detailed description of the test assembly is given in [105].

7.4 Accelerated Circuit Level Aging For Test

As already shown for linear amplifier circuits in sec. 6.4.1, an analytic circuit model providing information about single effect contributions offers the possibility to derive accelerated stress conditions for test, equivalent to an EOL operation use case. Such an approach is also applicable to the LC-VCO from fig. 7.4 and its corresponding circuit aging model. The appropriate methodology is evaluated and proven by measurement in the following sections.

7.4.1 Aging Acceleration for LC-VCOs

The general problem of aging acceleration for test on circuit level arises from the appearance of diverse aging effects with individual acceleration towards stress conditions. Their interaction result in a unique circuit aging behavior. As already shown in the amplifier aging acceleration study in sec. 6.4.1, an exact reproduction of an EOL operation use case is not possible. Nevertheless, an analytic circuit aging model approach, providing insight into effect contributions, allows to derive a best fit stress scenario, if at least a dominant aging contributor exhibits the same degradation magnitude as for the EOL operation. In the case of the current-reusing oscillator from fig. 7.4, this dominant aging effect is PBTI at the $\mathbf{M_n}$ active bridge devices (see fig. 7.9). Via

$$\Delta V_{th,PBTI/M_n}(V_{EOL}, T_{EOL}, t_{EOL}) = \Delta V_{th,PBTI/M_n}(V_{stress}, T_{stress}, t_{stress}). \tag{7.6}$$

and back calculation to corresponding supply voltage with the analytic VCO model, an accelerated and EOL equivalent stress condition can be derived.

7.4.2 Aging Use Case and Derivation of Stress Conditions

For the following study, an EOL operation use case of (25°C, 10y) for selected and slightly elevated supply voltages is chosen. As proven by the analytic model and RelXpert™, circuit aging is insensitive towards a rise in temperature due to a simultaneous decrease of oscillation stress amplitude. However, VCO aging strongly relates on the supply voltage. Thus, the following stress tests are performed at 25°C with increased stress supply voltages. Stress duration was set to $t_{stress} = 1000s$. Equivalent EOL stress conditions, derived via (7.6) and the analytic circuit model are given in table 7.4 for three selected EOL operation scenarios. Resulting degradation in the VCO aging monitor $\Delta V_{DD,start}$

EOL operation use case	equivalent accelerated stress
$(1.20V_{DD}$, 25°C, $10y)$	$(2.57V$, 25°C, $1000s)$
$(1.25V_{DD}$, 25°C, $10y)$	$(2.68V$, 25°C, $1000s)$
$(1.30V_{DD}$, 25°C, $10y)$	$(2.78V$, 25°C, $1000s)$

Table 7.4: EOL operation use cases and derived equivalent stress scenarios for accelerated VCO aging.

for the derived stress conditions, predicted by the VCO aging model, are further included in fig. 7.10. The graph shows, that aging results of the accelerated stress conditions are

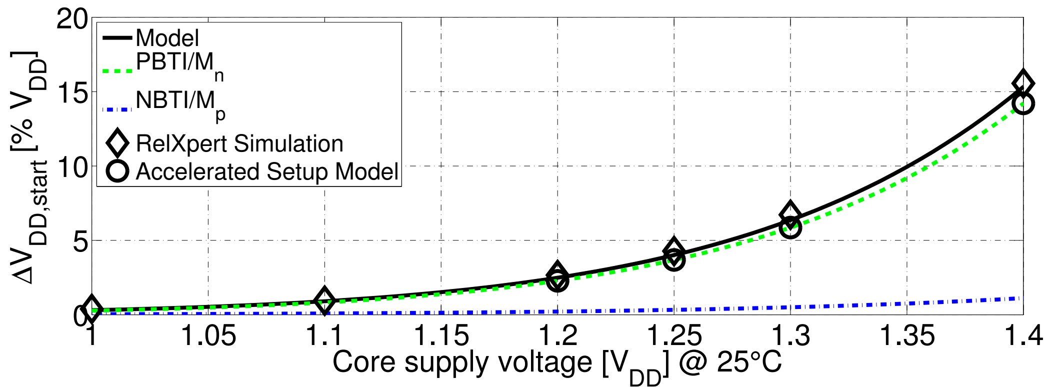

Fig. 7.10: VCO aging prediction for 10y EOL operation and results for the equivalent accelerated stress conditions.

close to the predicted ones for the EOL operation. This confirms the developed LC-VCO aging acceleration approach. Corresponding aging effect contributions occurring during the accelerated stress conditions in comparison to the EOL operation use case are depicted in fig. 7.11. As expected, effect contributions of the EOL and the accelerated stress conditions are not equal but similar. These derived stress conditions open the possibility to perform EOL equivalent aging related LC-VCO characterisations.

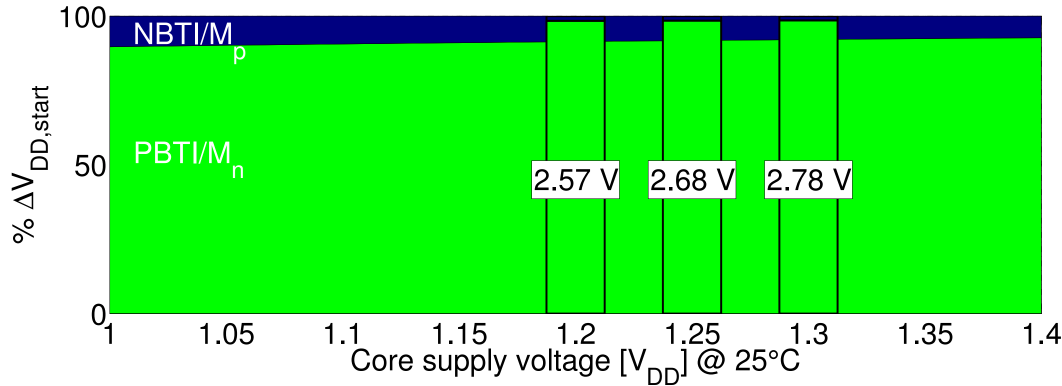

Fig. 7.11: Effect contributions for VCO EOL operation and equivalent accelerated circuit aging.

7.4.3 Stress Test Sequence

The following stress measurements on the LC-VCO hardware are performed according to the test sequence diagram in fig. 7.12. All measurements are carried out at room tempera-

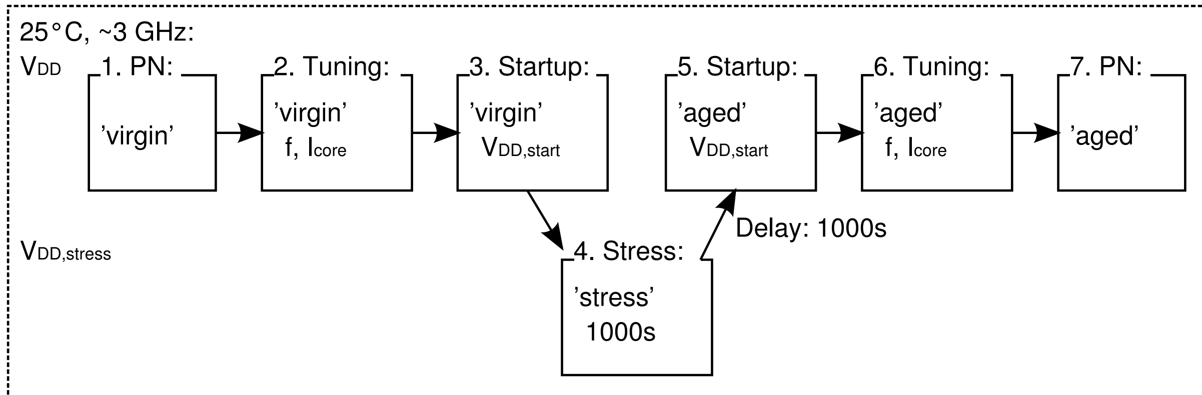

Fig. 7.12: Test sequence for the LC-VCO aging characterisation.

ture 25°C and, except the stress sequence, at nominal supply voltage. Coarse tuning is set to the lowest frequency value around 3GHz. In a first step Phase Noise characterisation is performed via the Aeroflex PN9000 assembly. For the following characterisation and the stress application, the setup has to be manually replugged. Then frequency tuning range for analog voltage tuning, while monitoring core supply current I_{core} and startup supply voltage $V_{DD,start}$ of the VCO is derived. After the characterisation of the 'virgin' circuit, stress supply voltage is applied and the VCO operates in 'stress' mode for a duration of 1000s. After a delay of 1000s in off-state for recovery of fast relaxing drifts, startup supply voltage $V_{DD,start}$ and frequency tuning characteristic including core supply current is determined for the 'aged' circuit. In the last step, after replugging to the PN9000 system, Phase Noise characteristic of the 'aged' circuit is measured.

7.4.4 Concept Evaluation

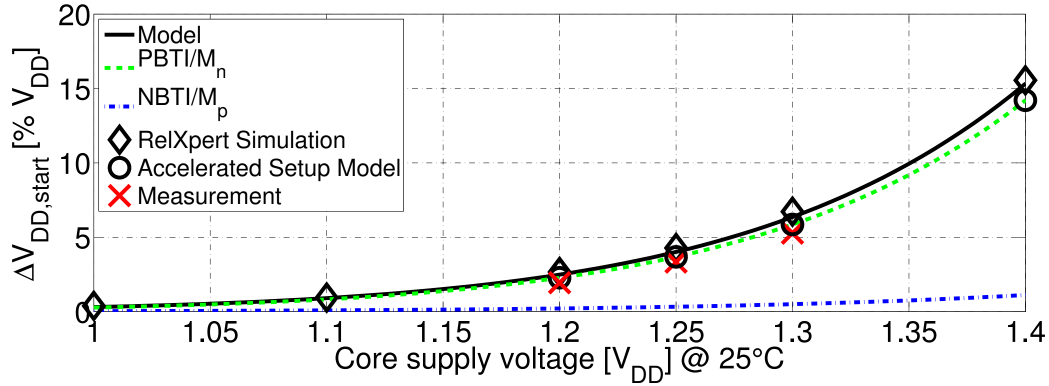

Fig. 7.13: VCO aging prediction for 10y EOL operation, the equivalent accelerated stress scenario and stress measurement results.

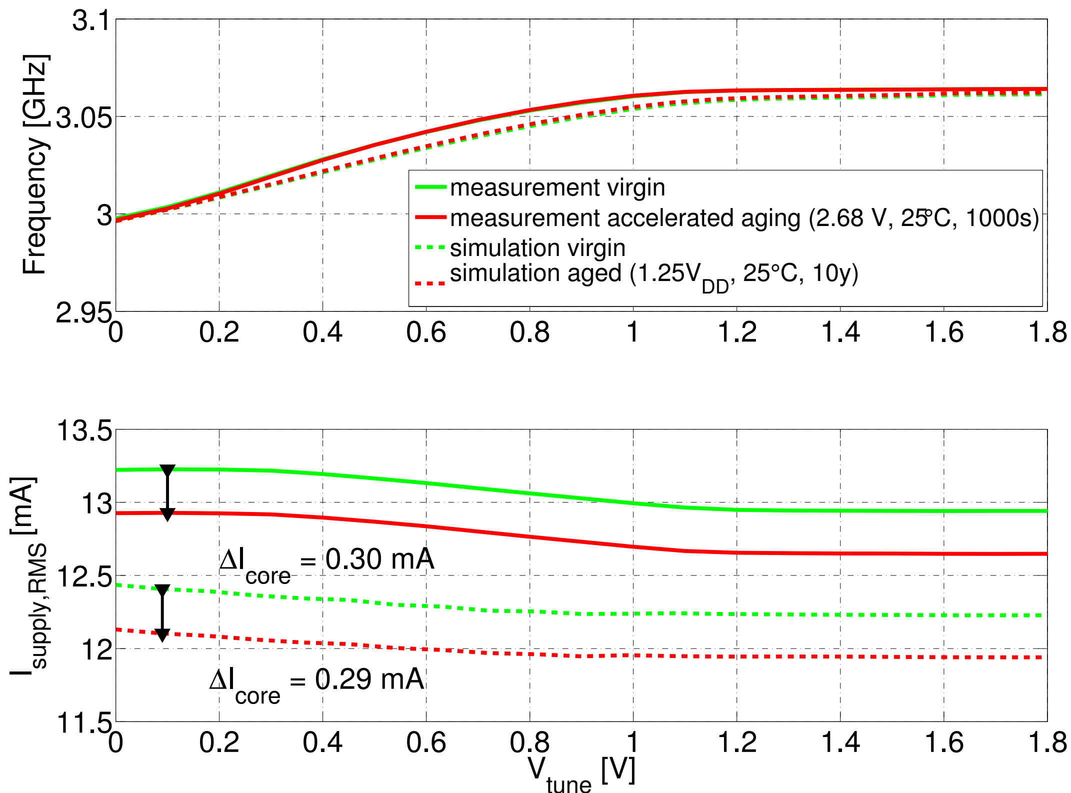

Fig. 7.14: Frequency tuning characteristic and supply current I_{core} before and after ($1.25V_{DD}$, 25°C, 10y) EOL operation and equivalent stress test. Simulations and measurements are performed with nominal supply voltage at 25°C.

Measurement results of the determined drifts in the VCO aging monitor $\Delta V_{DD,start}$ for the three derived EOL scenarios are further included into fig. 7.13. Results in $\Delta V_{DD,start}$

show good agreement of the stress measurement, the predicted accelerated stress scenario and the EOL circuit degradation, validating the developed stress test concept. Measured frequency tuning characteristic in fig. 7.14 shows little degradation impact and is consistent with the (1.25V_{DD}, 25°C, 10y) EOL aging simulation. Absolute values of I_{core} show deviations in simulation and measurement, but the mean values of current degradation ΔI_{core} of the virgin and the aged circuit coincide. The phase noise simulations in fig. 7.15 show good agreement for the (1.30V_{DD}, 25°C, 10y) EOL operation use case and its equivalent accelerated stress setup. Comparing simulation and measurement, good

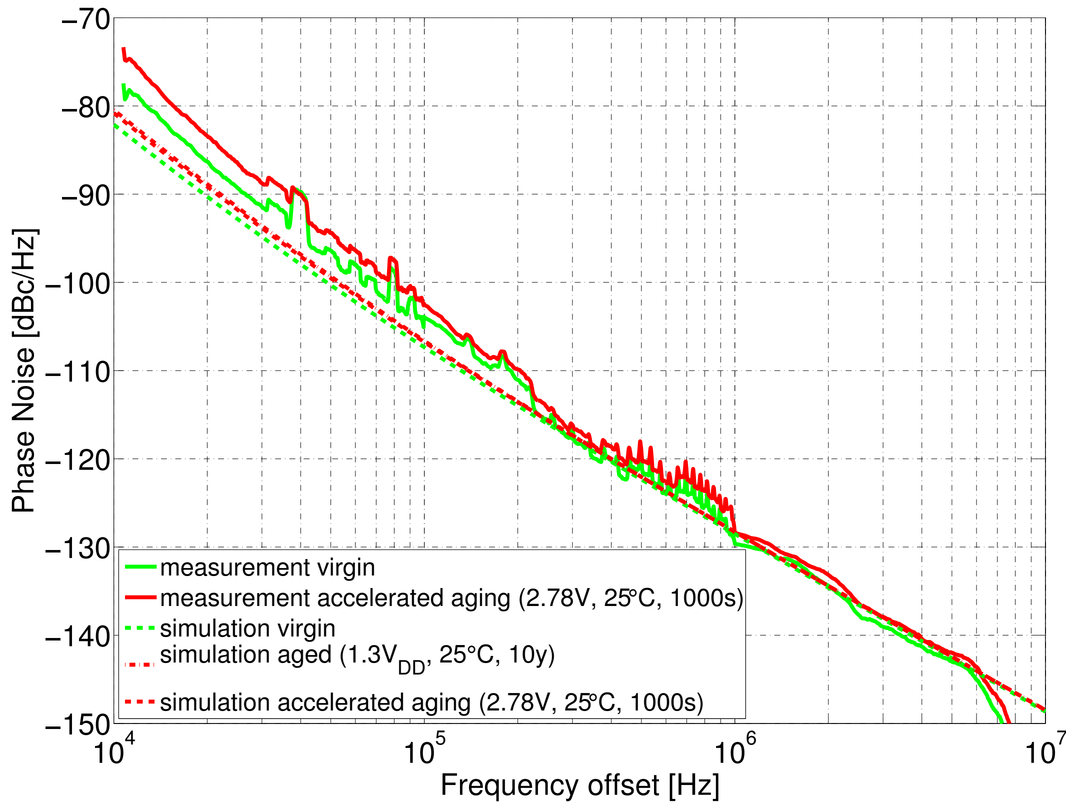

Fig. 7.15: Phase Noise characteristic before and after (1.3V_{DD}, 25°C, 10y) EOL operation and equivalent stress test. Simulations and measurements are performed with nominal supply voltage at 25°C.

matching in the thermal, but general deviance in the $\frac{1}{f}$-upconversion region is observed. This behavior is attributed an underestimation of $\frac{1}{f}$-noise in the device modeling. Furthermore, the measurement of the virgin and the aged circuit shows an explicit larger degradation in the close-in region compared to the simulation. Simulations revealed that $\frac{1}{f}$-noise of nMOS devices in the active bridge is the dominant contributor to the close-in phase noise. Obviously, the PBTI device stress leads to an increase of $\frac{1}{f}$-device noise. A similar degradation induced increase in $\frac{1}{f}$-noise, related to NCHCI, was also reported in [28].

The results on the VCO Phase Noise characteristic further revealed a complex relation of

flicker noise and BTI degradation effects. A general connection of both effects describing BTI degradation with flicker noise fundamental mechanisms is given in [51]. The previous investigation showed that for flicker noise sensitive circuits like VCO's new modeling approaches for BTI degradation close to its physical origins are necessary to correctly predict aging induced impact on circuit performance. Especially, during and for short times after stress a significant increase in flicker noise, as predicted by [51], may result in temporary violations of VCO's Phase Noise constraints and so to unpredictable malfunction of the whole system.

7.4.5 Model Prediction to Future LC-VCO Implementations

To estimate a trend for future low power approaches, the equivalent VCO design from fig. 7.2 b), using thin oxide devices with minimum gate length in the active bridge and correspondingly reduced supply voltage, was designed and an equivalent aging model was derived. This implementation does not use tail coils in the supply paths. Thus, amplitude overshoots above supply voltage do not occur. The predicted stress behavior is depicted

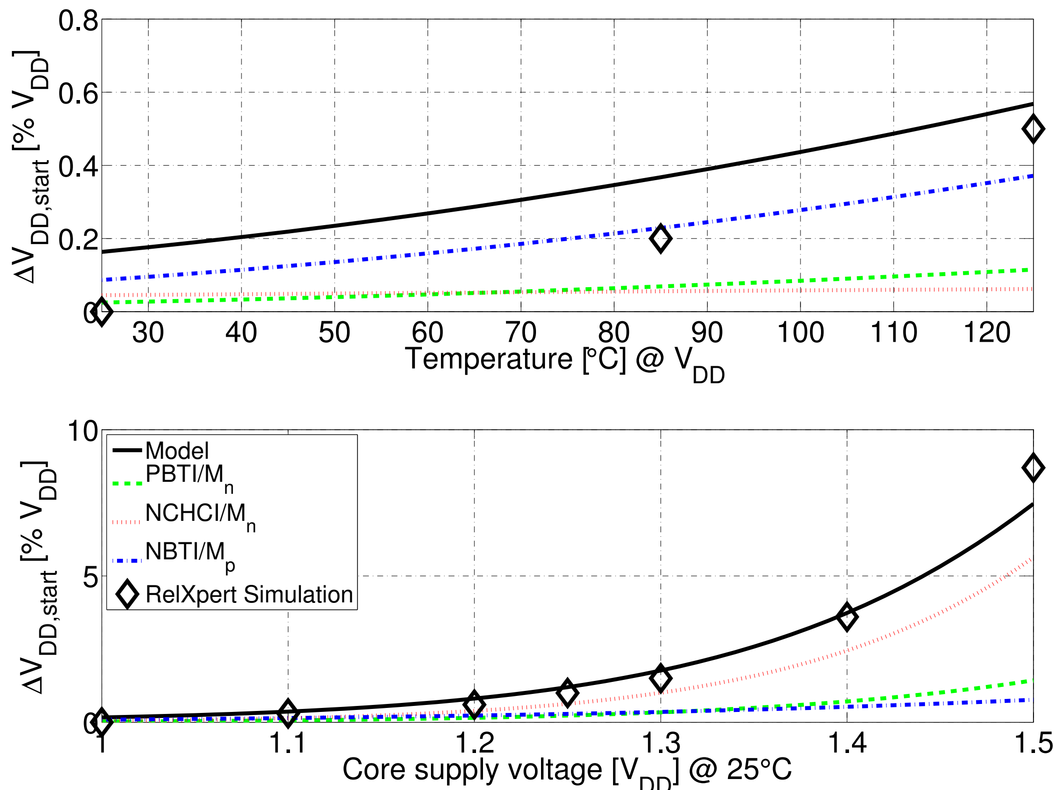

Fig. 7.16: Circuit aging results for a 10y EOL operation under given stress conditions of a current-reusing VCO providing thin oxide core devices: analytic model vs. RelXpert™ simulation. $\Delta V_{DD,start}$ is evaluated for nominal supply voltage and 25°C circuit operation.

in fig. 7.16. With thin oxide devices, NCHCI evolves as a main degradation mechanism that leads to significant supply current degradations for elevated supply voltages. Total degradations are smaller compared to the medium oxide version from sec. 7.1.6, but the circuit is considerably more sensitive, as supply current is related to the transistors' overdrive voltage and voltage headroom is significantly reduced. Contrary to the medium oxide VCO, nominal supply voltage can not guarantee proper startup for drifts of $\Delta V_{DD,start} \sim 10\% V_{DD}$. Here, additional design margins have to be incorporated to cover the increasing degradation sensitivity. The option to increase transistor gate length significantly reduces NCHCI and relaxes circuit degradation. Nevertheless, regarding future design options reliability aspects essentially have to be considered during the design process.

7.5 Summary

This study on the impact of MOSFET device aging on integrated LC-VCO circuits revealed a general degradation of circuit performance, which is still low for circuit operation in allowed voltage regimes and significantly increases for elevated supply voltages. The aging critical circuit part was found out to be the *active bridge*, providing the power for stable oscillation. It was further discovered that degradation of inversion mode MOSFET *varactors* is of minor impact. Here, other second order effects like a variation of signal amplitude further impact the equivalent capacitance and push the impact of varactor aging into the background. However, MOSFET aging of active bridge devices, mainly related to BTI and NCHCI effects, primarily leads to a degradation in supply current, which is small for *current-biased* and high for *voltage-biased* circuit topologies. For the current biased ones, supply current is defined via a current source transistor operating at moderate biasing and thus is not affected by significant device aging and provides stable bias current. However, supply current for voltage-bias structures is only defined by active bridge device characteristics and given supply voltage. Here, the degradation of active bridge devices strongly affects the supply current. Dependent on the current degradation and the robustness of the circuit design, other important performance parameters like amplitude and Phase Noise or startup ability are affected. The VCO frequency tuning range is generally hardly affected.
For voltage-biased structures, another suitable VCO aging monitor is $V_{DD,start}$, the minimum supply voltage for oscillation startup. Circuit degradations can be modeled via an exceptional small signal equivalent circuit approach for the startup operation point combined with aging effect models, resulting in a predictable $\Delta V_{DD,start}$. Furthermore, this analytic circuit aging model provides information about involved effect contributions. The derivation of this model for a state-of-the-art current-reusing LC-VCO for GSM applications revealed, that due to the robust design, temperature rise does hardly affect the circuit aging. For high temperatures, circuit degradation is even reduced, which can be related to a simultaneous decrease in amplitude. However for elevated supply voltages, circuit degradation significantly increases. Another sensitivity study comparing the impact of temperature and process variations as well as device aging on $V_{DD,start}$ revealed a minor impact of aging for operation in the allowed voltage regime, but for slightly

increased supply voltages, device aging arises as the dominant effect.
Basing on the circuit aging model, a universal methodology to derive accelerated stress conditions for test, equivalent to EOL operation state, is developed and validated via measurement on testchip hardware. The approach allows to perform circuit characterisations in an equivalent EOL circuit state. Phase Noise measurements for the aged circuit revealed a significant increase in the close-in region, which can be related to an increase of device flicker noise levels. A relation of BTI aging and flicker noise mechanisms is currently discussed among experts and is thus supported by these results. For future reliable VCO designs, new BTI model approaches, close to their physical origins are needed to correctly predict circuit aging behavior.
The outlook with an adapted circuit model to an advanced low power VCO design including thin oxide devices revealed the emergence of novel dominant effects like NCHCI. In this case, NCHCI impact could be counteracted by increasing active bridge gate lengths. Nevertheless, the study showed that the gap between arising aging induced drifts and voltage headroom dramatically decreases and aging effects will more and more come to the fore. In parts selected findings from this chapter were published in [115].

Chapter 8

Conclusion

CMOS technology progress involves the enforced appearance of device aging effects both in magnitude and in number. At the same time, circuits becomes more and more sensitive towards device degradation due to reduced voltage headroom. Today, analog circuit design in current CMOS technologies is still able to cover device wearout with sufficient design margins. But the opposed behavior of circuit sensitivity and degradation narrows the gap and aging will arise as sudden reliability problem in future. For this reason, a fundamental and throughout framework to handle device degradation in analog circuits is developed and provided in this work.
The overview of the degradation mechanisms showed that effect physics are not fully understood up to now and are still controversially discussed among the scientific community. This lack in understanding can be related to the strong dependency on the MOS processing and insufficient stress characterisation. Recently, novel characterisation techniques and model approaches are able to accurately describe BTI degradation via physically based trapping processes. Nevertheless, well-established semi-empirical prediction models lack in accuracy and are not able to fully map analog significant effect behavior like recovery.
Investigations on operation states occurring in analog circuits revealed that major aging contributions are expected to arise from BTI, generated in deep triode operation region. Different to digital circuits, HCI effects usually play a secondary role, as they strongly relate on the channel length and small length devices are only used in rare cases. Stress tests on custom structures for analog operation scenarios revealed that state-of-the-art degradation modeling does not or only partially cover analog related effect properties. For instance, the 1-dimensional BTI effect modeling predicts one degradation value, whether the device operates in saturation or in triode region, whereas stress measurements revealed a factor of nearly 3 in degradation. BTI degradation recovers within wide timing ranges after stress removal, which is also not covered by the prediction model, only providing a fixed degradation value, but arise as important analog circuit related effect property. It is further not clear which state of recovery is predicted by the aging prediction model. Tests on aging variability showed a minor role due to the analog typical large area devices and related defect density averaging. The general mechanisms' property of saturation can be beneficially used for aging suppression. Another aging critical operation state that can

occur during circuit standby is accumulation, which - revealed by measurement - induces significant degradations that also recover. This is not covered by today's aging models. Furthermore, accumulation mode is partially able to recover previous inversion mode aging, but proves not to be suitable for a stepwise aging compensation in the circuit due to large parameter drifts in both directions. Another possibility would be an alternating operation in inversion and accumulation mode during circuit operation to induce instantaneous regeneration. Despite the need for improvement, basic aging effect behavior is generally modeled via the semi-empiric model equations and form the basis for further circuit level aging related research.

The study on current mirror circuits showed the inherent circuit aging suppression ability as equal degradations cancel in the structure. For typical moderate and symmetric biasing only minor aging impact and a stable current generation is assured. However, for asymmetric biasing and dependent on the device dimensions, significant mismatch in the currents can occur. HCI induced contributions can be well controlled by proper gate length dimensioning, but pMOS/HCI with included Local Self-Heating Accelerated (LSHA) NBTI shows a significant worsening for recent technologies. Additionally, the asymmetric operation of the sense device in saturation and the copy device in deep triode region, may induce mismatch due to asymmetric BTI degradation. This is area independent and so can not be covered by proper device sizing. Furthermore, this mismatch source is not covered by 1-dimensional aging models and so is missed in the circuit reliability consideration.

For reference generation circuits the general moderate device biasing conditions induce only small degradations. Closed-loop control further stabilises the circuit and reduces the impact of arising device parameter drifts. However, circuit startup behavior is very design specific and has to be proven individually.

For amplifying circuits, asymmetric voltage stress primary induces offset. Offset generation is small in closed-loop configuration due to moderate stress conditions at the sensitive input and high in open-loop/comparator usage due to full voltage swing at the input. The study revealed that voltage biased structures are much more sensitive than current biased ones, due to the stable bias current. Contrary to the voltage biased structures, current biasing further suppresses device aging impact on other performance parameters as gain or GBW. An ex-post offset compensation after circuit degradation fully restores the circuit performance.

Studies on LC-VCO circuits and its basic components revealed that device aging on the MOS varactor device negligibly impacts its equivalent capacitance and so the oscillator frequency tuning range. However, degradation of active bridge devices has major impact. Similar to the amplifiers, voltage biased topologies proved to be much more sensitive than current biased ones. Degradation of the active bridge primary lead to a reduction of supply current and dependent on the topology and circuit design to a degradation of relevant performance characteristics like oscillation amplitude, Phase Noise and circuit startup behavior. Instead of the supply current, circuit startup supply voltage $V_{DD,start}$ proved to be a suitable and 'easy to model and measure' aging monitor for voltage biased topologies.

Development of custom and circuit specific testbenches for alternating stress and circuit characterisation turned out to be an essential basis to provide reliable hardware valida-

tions. Particular attention has to be paid to fully-automatized stress and measurement sequences to ensure reproducible results.
Describing circuit aging via an analytic approach, combining circuit behavior with the aging prediction models, provides an essential and powerful methodology to accurately predict and decompose circuit aging with respect to its stress conditions (V, T, t). The effect decomposition ability of the model reveals the complex interaction of the numerous degradation mechanisms, that may even compensate each other during circuit operation as shown for current mirrors and differential amplifiers. This general approach was successfully applied to simple varactor devices, current mirror, a state-of-the-art differential amplifier and an LC based VCO circuit. The new insight into the complex effect interaction on circuit level provides the foundation for advanced concepts. For example, it provides information about dominant effect contributors and the opportunity to perform derivation from device to circuit level stress conditions. Prognostics for circuit designs in future CMOS technologies are further enabled and were exemplary shown for varactors and LC-VCOs. For instance, future LC-VCO designs using the digital core device of the 32nm CMOS technology revealed a dramatic increase of NCHCI effects for future circuit implementations.
Basing on the analytic circuit aging description, a universal methodology to derive accelerated stress conditions for reliability testing on circuit level - equivalent to an end-of-lifetime operation condition - is developed and verified via stress testing. It has been shown, that on circuit level an exact aging acceleration via simple voltage and temperature rise does not map a realistic end-of-lifetime (EOL) case due to the complex interaction of distinct mechanisms, providing individual acceleration physics. However, via a best fit approach, the analytical circuit model description allows to determine accelerated circuit stress conditions close to the EOL aging use case. This methodology was evaluated for linear and non-linear circuits, exemplarily studied on a state-of-the-art differential amplifier and an LC-VCO for GSM applications, and verified by stress measurements. For both circuits, major contributions of circuit degradation were related to BTI aging occurring during a device's deep triode region operation. Especially for the LC-VCO, further characterisation measurements revealed a significant worsening of Phase Noise in the close-in region after stress, which is related to a BTI induced worsening of device flicker noise. This BTI degradation behavior is also expected in recent publications, but still not covered by any modeling. Anyhow, for reliable analog circuit design it is an important and essential parameter.
The fast signal processing ability of a differential amplifier was further used to reveal the significant impact of transient BTI recovery, ranging over a wide time span. Especially, short time recovery contributions in the signal bandwidth are able to violate signal processing and cannot be mitigated by common offset compensation techniques. So, they limit a circuit's accuracy. Due to missing BTI recovery models, a consideration by circuit simulations is not yet supported and arises as a major demand for future reliability prediction tools. As an interim solution, a prediction ability for expected magnitudes in the relevant bandwidths would help the designer to develop BTI recovery robust circuits.
Degradation countermeasures on design level can be summarized to the HCI mitigation via increasing gate length as well as the prevalent application of nMOS devices in older SiO_2 or $SiON$ CMOS technologies due to negligible PBTI. As further shown, the general

mechanism property of drift saturation can be beneficially used to perform a circuit level aging suppression via directed 'Burn-In'. This methodology was exemplarily evaluated and proven via measurement on a differential amplifier circuit. Here, directed BTI induced drifts were used to perform offset calibration, resulting in a remarkably low offset and aging aware amplifier after the stress treatment. This ex-post mismatch calibration offers to exceed matching limited device sizing constraints and provides the opportunity for future low power and high efficient analog circuit design.
This work shows, that today's aging effect consideration and prediction on circuit simulation level lacks in modeling accuracy. Throughout and physics based prediction models arise as a future but challenging task due to the strong dependency on CMOS processing and complex sensitivity to stress conditions. Basing on general aging prediction models, a fundamental and universal investigation on aging relevant analog circuit blocks reveals major degradation effects. Developed methodologies for analytic circuit aging description, circuit level stress testing and mitigation concepts provide a fundamental and universal framework for future approaches to design-in reliability.

Basing on these findings, general *design guidelines for aging aware circuit design* are outlined. Most important and relevant mechanism properties can be summarized as follows:

BTI:
- (a) is in first order gate area independent,
- (b) occurs only as NBTI/pMOS for well-established SiO_2 or $SiON$ based CMOS technologies and as NBTI/pMOS and PBTI/nMOS in high-κ based technologies and
- (c) strongly depends on the vertical electric oxide field, thus is mainly V_{GS} dependent.

HCI:
- (a) strongly scales with $\sim \frac{1}{L}$,
- (b) classic CHCI/nMOS is most relevant, but for advanced technologies CHCI/-pMOS arises as most significant HCI effect due to LSHA side effects with additional worsened $\sim \frac{1}{L}$ scaling behavior and occurring NCHCI in off-state,
- (c) strongly depends on the lateral electric field, thus is mainly V_{DS} and L dependent.

Further analog circuit related properties, that are not covered by today's effect modeling, are found by custom stress measurements:

- (a) transient BTI effect recovery can arise as significant problem for analog circuitry and demands for advanced and physics based modeling,
- (b) effect variations are a minor issue for 'analog size' devices due to defect averaging and
- (c) accumulation mode also leads to device degradation.

Anyhow, state-of-the-art degradation prediction models provide for most cases a fundamental and valid circuit aging prediction. Even simple 1-dimensional versions (only V_{GS} or V_{DS} dependent), prove to provide sufficient accuracy, except for some special cases like an asymmetric operation of current mirrors, that have to be considered individually. *Aging critical analog circuit* operation conditions turned out to occur at structures that

(a) operate at high voltage swings and/or

(b) operate asymmetric at highly matched structures.

Special attention has to be drawn to a circuit's standby state, that devices are not driven into full swing inversion or accumulation mode, where the latter is typically passed over by today's reliability simulation tools. Suitable aging countermeasures can be summarized to:

(a) circuit design and operation ensuring general peak voltage and temperature limitations,

(b) active HCI suppression via increasing gate lengths,

(c) usage of nMOS devices at aging sensitive points for SiO_2 and $SiON$ based technologies,

(d) circuit level calibration techniques and

(e) passive aging suppression via effect saturation induced by 'Burn-In'.

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Abbreviations

ACC .... accelerated
AD .... Analog to Digital
ADC .... Analog to Digital Converter
AF .... Acceleration Factor
BTI .... Bias Temperature Instability
CHCI .... Conductive Hot-Carrier Injection
CLM .... Channel Length Modulation
CMOS .... Complementary Metal Oxide Semiconductor
DA .... Digital to Analog
DAC .... Digital to Analog Converter
DF .... Duty Factor
DM .... Design Manual
EDM .... Energy Driven Model
EOL .... End-of-Lifetime
GBW .... Gain Band Width
HCI .... Hot-Carrier Injection
ICs .... Integrated Circuits
IO .... Input Output
LDD .... Lightly Doped Drain
LEM .... Lucky Electron Model
LSHA .... Local Self-Heating Activated
MOS .... Metal Oxide Semiconductor
MOSFET .... Metal Oxide Semiconductor Field Effect Transistor
MP .... Mobile Phone
NBTI .... Negative Bias Temperature Instability
NCHCI .... Non-Conductive Hot-Carrier Injection
OTA .... Operational Tranconductance Amplifier
PBTI .... Positive Bias Temperature Instability
PLL .... Phase Locked Loop
PM .... Phase Margin
PTAT .... Proportional To Absolute Temperature
PVT .... Process Voltage Temperature
PVTA .... Process Voltage Temperature Aging
RD .... Reaction Diffusion
RF .... Radio Frequency

RTN .... Random Telegraph Noise
SBD .... Soft Breakdown
SCE .... Short Channel Effects
SMU .... Source Measure Unit
SNR .... Signal to Noise Ratio
SOT .... Switching Oxide Traps
SR .... Slew Rate
SRAM .... Static Random Access Memory
TDDB .... Time Dependent Dielectric Breakdown
TDDS .... Time Dependend Defect Spectrocopy
UC .... Use Case
VCO .... Voltage Controlled Oscillator

Symbols

AGE	auxiliary degradation variable	
A_I	low frequency current gain	
A_V	low frequency voltage gain	
C	capacitance	F
$C_{eff,inv}$	effective MOS capacitance in inversion	$\frac{As}{Vm^2}$
$\Delta C_{eff,inv,tune}$	effective MOS capacitance tuning range	$\frac{As}{Vm^2}$
C_{ox}	area related Gate oxide capacitance	$\frac{As}{Vm^2}$
C_{oxide}	Gate oxide capacitance	$\frac{As}{V}$
D_{BTI}	degradation BTI	
D_{HCI}	degradation HCI	
ΔE	thermal activation energy BTI	
f	frequency	Hz
$F_{el,ox}$	oxide electric field	$\frac{V}{m}$
Φ_F	Fermi level	V
Φ_{MS}	workfunction difference metal to semiconductor	V
γ	body factor	$\sqrt{V}$
g_m	transconductance	$\frac{A}{V}$
ΔH	thermal activation energy HCI	
I_B	substrate current	A
I_{copy}	current mirror copy current	A
I_D	Drain current	A
ΔI_D	aging induced drain current degradation	$\%I_D$
I_G	Gate current	A
I_{RMS}	root mean square current	A

I_{sense}	current mirror sense current	A
I_{SUB}	impact ionisation rate	A
k	Boltzmann's constant	$\frac{J}{K}$
L	Gate length	m
L_{eff}	effective channel length	m
L	inductance	H
$\mathcal{L}$	Phase Noise	$\frac{dBc}{Hz}$
μ	channel mobility	$\frac{m^2}{Vs}$
μ_0	low field surface mobility	$\frac{m^2}{Vs}$
μ_{eff}	effective channel mobility	$\frac{m^2}{Vs}$
μ_n	channel mobility nMOS	$\frac{m^2}{Vs}$
μ_p	channel mobility pMOS	$\frac{m^2}{Vs}$
n	time exponent BTI	V
ω	angular rate	$\frac{1}{s}$
Q	electric charge	C
Θ	mobility degradation coefficient	$\frac{1}{V}$
R_{tank}	tank losses	Ω
T	temperature	$^\circ K$
t	time	s
t_{ox}	oxide thickness	m
V	voltage	V
V_b	substrate voltage	V
V_{BS}	substrate Source voltage	V
V_d	Drain voltage	V
V_{DS}	Drain Source voltage	V
V_{DSAT}	saturation Drain voltage	V
V_{FB}	flatband voltage	V
V_g	Gate voltage	V
V_{GS}	Gate Source voltage	V
V_{OD}	overdrive voltage	V
V_s	Source voltage	V
V_{th}	threshold voltage	V

ΔV_{th}	aging induced threshold voltage drift	V
V_{tune}	varactor tuning voltage	V
W	Gate width	m

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