# The Optimal Wire Order for Low Power CMOS

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**Abstract.** If adjacent wires are brought into a simple specific order of their switching activities, the effect of power optimal wire spacing can be increased. In this paper we will present this order along with a prove of this observation. For this purpose, it is shown how to derive the new power optimal wire positions by solving a *geometric program*. Due to their simplicity in implementation, both principles reported substantially differ from previous approaches. We also quantify the power optimization potential for wires based on a representative circuit model, with promising results.

## 1 Introduction

Today it is widely accepted that one of the new key issues in designing CMOS circuits at 130, 90 and 65nm technologies is power. We have to work under power constraints that stem from heat removal, reliability or battery lifetime limitations. It is not possible to benefit from either the integration complexity or performance features of a new technology node without optimizing for a low power consumption at all levels of the design.

**Structure of This Document.** This section continues with a short overview of existing work in the field of wire ordering and wire spacing and of our approach. Also to the Introduction belongs an illustration of CMOS power basics and the current situation for on-chip wires to an extent we will need in subsequent sections. The next section is the description of power optimal wire spacing and ordering. We create a rule for power optimal wire ordering. The rule is mathematically proved in Section 3. All of Section 4 deals with experiments to quantify the optimization potential of wire spacing and ordering. Section 5 will conclude the article together with some future remarks.

**Related Work and Presented Approach.** Wire ordering and spacing both have a long history in Electronic Design Automation. People attempt to space and order bus wires for different objectives like power [7], crosstalk [2] [7], area [4], or timing [8]. The latter work contains a more complete list.

Our approach reveals two basic phenomenons which have not been previously published. First, the wire spacing problem is written as a geometric program rather than developing a heuristic or using exhaustive searching. Taking a step
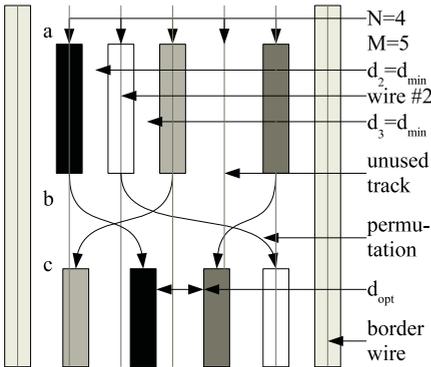
**Fig. 1.** Wires: the darker the more active  **Fig. 3.** Capacitances in a $0.13\mu m$ process
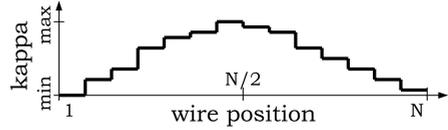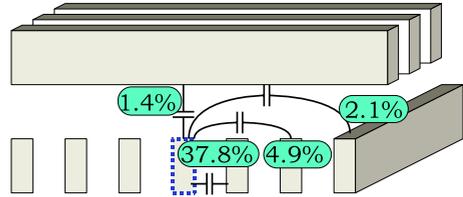
forward, a mathematical formulation for a new globally power optimal wire order is formulated. Figure 1 shows an unoptimized bus (a) with an un-populated routing track. The idea is to place the wires off-grid (c), so that the unused space can be exploited: An individual distance is assigned to each wire pair based on the wire activities. A lower capacitance for highly active wires and vice versa is the result. If the wires are put into the order (b) indicated by Figure 2 beforehand, the power savings increase.

## 1.1   CMOS Power Basics

The power consumption of a CMOS gate is usually decomposed into a static and a dynamic component. The static one is about to reach orders of magnitudes similar to the dynamic one [11]. However, this paper solely deals with part of the dynamic component. More precisely, we try to reduce the capacitive power caused by the edge capacitances to be described shortly. For our purpose we will reduce the capacitive power formula to $\kappa \cdot C$ and provide expressions for $C$ and $\kappa$ in this subsection.

**Capacitance.** One widely known fact in integrated system design is that the average wire capacitances tend to increase when compared to the average gate capacitances [11][5]. The first address for capacitance minimization should therefore be the interconnects.

There has been another important trend in the physics of wires: the demand for ever higher integration densities and yet acceptable sheet resistances required a typical on-chip wire to become physically more thick than wide. This implied that now the edge-to-edge (other terms found in literature: x-coupling, lateral, sidewall) capacitances within one layer dominate [12], as opposed to the past.

Figure 3 shows a capacitance break down simulated with FastCap [9]. The test setup was a wire (dotted) on metal2 of a typical $0.13\mu m$ process embedded into a fully crowded proximity. Note that the bottom layer is not shown. The

ratio between the sum of the two edge capacitances of that wire and all other capacitances of that wire is almost 78%.

Keeping in mind these observations, it is clear that the edge-to-edge capacitances are good candidates for power optimization. We approach the edge-to-edge capacitance of a circuit node $i$ with the plate capacitor formula:

$$C_{\text{edge\_to\_edge},i} \propto l_i \left( \frac{1}{d_i} + \frac{1}{d_{i+1}} \right), \tag{1}$$

where $l_i$ is the length of the wire, and $d_i$ and $d_{i+1}$ the left and right distances to the next metal objects, respectively, cf. wire 2 in Figure 1. Note that for the sake of brevity we assume each net to consist of only one segment. We will also omit the wire length since this paper only deals with the optimization of the distances between two wires. A more general disquisition can be found in [14].

**Switching Activity et al.** The switching activity is a major factor that separates high- from low-power nets. It can represent a probability based on assumptions. Or, it is derived by a simulation on gate level and is related to the simulation time interval. It then represents the actual number of toggles of a node. Since there are more factors which influence the capacitive power, we want to define a variable $\kappa$ that captures all these factors. We call it $\kappa$ because all factors are invariant after synthesis.

**Definition 1.** *Let $\alpha_{01,i}$, $f_i$, and $V_{DD,i}$ of a node $i$ be the switching activity or toggle rate, the frequency of the associated clock domain, and the supply voltage of the driving gate, respectively. We define a power weighting factor $\kappa_i$ for a node $i$ as*

$$\kappa_i := \alpha_{01,i} f_i V_{DD,i}^2 \tag{2}$$

## 2   Power Optimal Wire Spacing and Ordering

Let us now consider N parallel wires of width $w$ routed on $M$ tracks as in Figure 1. By combining (1) and (2) into the well-known formula for the capacitive power dissipation, $P_C = C\alpha_{01} f V_{dd}^2$, we get the objective function of a geometric program:

### 2.1   Wire Spacing

$$P_{\text{edge\_to\_edge},i} \propto \sum_{n=1}^{N+1} \frac{(\kappa_n + \kappa_{n-1})}{d_n} = \text{min!} \tag{3}$$

$$d_n \geq d_{min} \quad \forall n = 1 \dots N + 1 \tag{4}$$

$$\sum_{n=1}^{N+1} d_n \leq \beta \tag{5}$$

At this point it should be noted that we model the whole scenario to be enclosed in between two static wires with the numbers 0 and $N + 1$ to avoid

edge effects which could influence the results. The analogon on a chip could be power or shield wires.

Between the two border wires, now arbitrary wire distances can occur. The only exception is that no wire pair must get closer than a minimum distance $d_{min}$, cf. (4). The value of this minimum spacing is technology dependent. In the second constraint (5), $\beta := (M+1)D_{pitch} - N \cdot w$ was introduced to reflect the chip boundaries. We assume $w + d_{min} = d_{pitch}$ which is the case for many processes. Obviously, if there are no more than $N$ tracks availiable between the above mentioned border wires routed on tracks 0 and $M+1$, there will be no freedom to optimize the distances and thus the power objective. Hence, $M > N$ is the prerequisite to do wire spacing and shall therefore be true for the remainder of the document.

## 2.2   Wire Ordering

Wire ordering is the deliberate assignment between wires and available tracks in the effort to optimize some objective function. For our case, the non-linearity induced by $1/d$ in (3) lets anticipate an influence of the arrangement of $(\kappa_n)$ on the effect of wire spacing for low power.

**Definition 2.** *Given is a set $(\kappa_0, \kappa_1, \ldots, \kappa_N, \kappa_{N+1})$ of $\kappa$-factors of the $N$ nets to be routed as defined in (2). For a permutation $\pi$ of the numbers $\{1 \ldots, N\}$ we call $(\kappa_0, \kappa_{\pi(1)}, \ldots, \kappa_{\pi(N)}, \kappa_{N+1})$ a* wire ordering. *We denote the set of all wire orderings by $\mathbb{K}$. A particular wire ordering is called a* power optimal wire ordering *if the solution for (3) - (5) is minimal over all wire orderings in $\mathbb{K}$.*

An investigation of the problem with different wire orderings revealed the following observation, cf. Figure 2.

**Theorem 1.** *A wire ordering $(q_n) \in \mathbb{K}$ is a power optimal wire ordering if and only if it is constructed in the following way:*

1. *Start with $q_0^{(0)} := q_{N+1}^{(0)} := 0$, $K^{(0)} := \bigcup_{i=1}^{N} \{\kappa_i\}$.*
2. *For $s = 1, \ldots, N$:*
   (a) *Let $q_a^{(s-1)} \leq q_{a+1}^{(s-1)}$ be the two greatest elements of $(q_i^{(s-1)})$ (in theorem 4 we will prove that these have to be adjacent).*
   (b) *Let $c := \min K^{(s-1)}$ and define $K^{(s)} := K^{(s-1)} \backslash \{c\}$.*
   (c) *Define $(q_i^{(s)})$ by inserting $c$ between $q_a^{(s-1)}$ and $q_{a+1}^{(s-1)}$, i.e.*

$$q_i^{(s)} := \begin{cases} q_i^{(s-1)}, & for\ i \leq a \\ c, & for\ i = a+1 \\ q_{i-1}^{(s-1)}, & for\ i \geq a+2. \end{cases}$$

## 3   Proof of Theorem 1

### 3.1   Known Results from Convex Programming

We first state a basic results from convex programming that we shall need in our subsequent considerations. In what is to follow we denote by $u_n$ the n-th unit vector and by $e$ the all-ones vector $(1, \ldots, 1)^T$.

**Theorem 2.** *Let $P \subset \mathbb{R}^n$ be a closed convex subset of the open convex set $C$ and let $f : C \to \mathbb{R}$ be a convex differentiable function. Then $x^* \in P$ minimizes $f$ over $P$ if and only if*

$$-\nabla f(x^*) \in N_P(x^*),$$

*where $N_P(x^*)$ is the cone of the outer normals in $x^*$, defined by*

$$N_P(x^*) := \{c \in \mathbb{R}^n : \max_{x \in P} c^T x = c^T x^*\}.$$

For the proof of this theorem and some background on convex programming, we refer the reader to [10], theorem 27.4. The next lemma is a simple inequality of the square root function, which will be essential for the proof of our results.

**Lemma 1.** *Let $a \geq b \geq 0$ and let $c > 0$. Then $\sqrt{a} - \sqrt{b} \geq \sqrt{a+c} - \sqrt{b+c}$ with equality if and only if $a = b$.*

*Proof.* This follows straightforward from the fact that the function $x \mapsto \sqrt{x}$ is differentiable in $(0, \infty)$ and has strictly decreasing slope. $\qquad\square$

### 3.2    Characterization of the Optimal Distances

For ease of notation let us now denote $\kappa_n + \kappa_{n-1}$ by $\gamma_n$. We first consider the problem of characterizing the optimal $d$-vector of (3)-(5) for a given wire ordering.

**Theorem 3.** *Let $P := \{d \in \mathbb{R}^{N+1} : d \geq d_{min}e \wedge \sum_{n=1}^{N+1} d_n \leq \beta\}$. Then $d^* \in P$ is optimal for (3)-(5) if and only if there exists $\tilde{\gamma} > 0$ that satisfies both*

$$d_n^* = \max\{\tilde{\gamma}\sqrt{\gamma_n}, d_{min}\} \quad \forall n = 1, \ldots N + 1$$

$$\text{and } \sum_{n=1}^{N+1} d_n^* = \beta.$$

*Proof.* Let $d^* \in P$ and $\tilde{\gamma}$ as required by the theorem. We have to show that $-\nabla f(d^*) \in N_P(d^*)$. For this purpose let $I$ denote the index set $I := \{n : d_n^* = d_{min}\}$. We need to find $\lambda_0, \lambda_1, \ldots, \lambda_{N+1} \geq 0$ such that

$$-\nabla f(d^*) = \begin{pmatrix} \frac{\gamma_1}{d_1^{*2}} \\ \vdots \\ \frac{\gamma_{N+1}}{d_{N+1}^{*2}} \end{pmatrix} = \sum_{n \in I} \lambda_n(-u_n) + \lambda_0 e.$$

One can easily calculate $\lambda_0 = \frac{1}{\tilde{\gamma}^2}$ and $\lambda_n = \frac{1}{\tilde{\gamma}^2} - \frac{\gamma_n}{d_{min}^2}$ for $n \in I$. As $\tilde{\gamma} \leq \frac{d_{min}}{\sqrt{\gamma_n}}$ for $n \in I$, the $\lambda_n$ are all nonnegative, so $-\nabla f(d^*) \in N_P(d^*)$ and $d^*$ is optimal by theorem 2.

For the converse, suppose $d^* \in P$ is an optimum for (3)-(5). Let $m := \max\{\frac{\gamma_n}{d_n^{*2}} : n = 1, \ldots, N + 1\}$ and $M := \{n : \frac{\gamma_n}{d_n^{*2}} = m\}$. According to theorem 2 we have $-\nabla f(d^*) \in N_P(d^*)$, hence there are $\lambda_0, \lambda_1, \ldots, \lambda_{N+1} \geq 0$

such that $-\nabla f(d^*) = \sum_{n=1}^{N+1} \lambda_n(-u_n) + \lambda_0 e$. Of course $\nabla f(d^*) \neq 0$ (because $d_n^* \geq d_{min} \ \forall n$), so $\lambda_0$ must attain some value $\geq m$ (note this implies that $d^*$ is on the hyperplane $e^T d = \beta$, hence $\sum_{n=1}^{N+1} d_n^* = \beta$) and $\lambda_n = \lambda_0 - \frac{\gamma_n}{d_n^{*2}}$ for $n = 1, \ldots, N+1$. In case $\lambda_n > 0$ for all $n = 1, \ldots, N+1$, the vector $d^*$ would be determined by the intersection of $N+2$ hyperplanes with normal vectors $-u_1, \ldots, -u_{N+1}$ and $e$, which is clearly impossible as $M > N$. So at least one $\lambda_n$ must be 0, and this can only be the case if $\lambda_0 = m$, which means $\lambda_n = 0 \iff n \in M$. So for $n \in M$ we have $d_n^* = \frac{\sqrt{\gamma_n}}{\sqrt{m}} = \tilde{\gamma}\sqrt{\gamma_n}$ with $\tilde{\gamma} = \frac{1}{\sqrt{m}}$, whereas for $n \notin M$ the value of $d_n^*$ is determined by the intersection of the hyperplanes $-u_n^T d = d_{min}$ with $e^T d = \beta$, therefore $d_n^* = d_{min}$ for all $n \notin M$. Of course, for $i \notin M$ and $j \in M$ the inequality $\frac{\gamma_i}{d_{min}^2} < \frac{\gamma_j}{(d_j^*)^2} = \frac{1}{\tilde{\gamma}^2}$ holds, so $d^*$ is of the form stated above. $\qquad \square$

For the following consideration we assume that the optimal wire spacing $d^*$ is of the form $d_n^* = \tilde{\gamma}\sqrt{\kappa_n + \kappa_{n-1}}$. If one or more distances are at their lower bound, things get a bit more technical, but the result is basically the same. So the objective function (3) is reduced to

$$\tilde{\gamma} \sum_{n=1}^{N+1} \sqrt{\kappa_n + \kappa_{n-1}} = \min!$$

### 3.3   Power Optimal Wire Ordering

Before we prove our main result, we first provide the "building blocks". The basic idea is to make use of the inductive nature of the proposed algorithm. The next theorem provides us with the key ideas for the proof of theorem 1, but first let us formalize the notion of a *unimodal wire ordering*.

**Definition 3.** *Let $(q_n)_{n=0,\ldots,N+1} \in \mathbb{K}$ be a wire ordering of the $(\kappa_i)$. If there exists an index $t, 1 < t < N+1$, such that $q_{n-1} \leq q_n \ \forall \ n \leq t$ and $q_n \geq q_{n+1} \ \forall \ n \geq t$, the wire ordering $(q_n)$ is called a* unimodal wire ordering *with mode $t$.*

**Theorem 4.** *Let $(q_n)_{n=0,\ldots,N+1} \in \mathbb{K}$ be a power optimal wire ordering. Then $(q_n)$ is unimodal. Furthermore, if we denote by $q_t \geq q_s \geq q_r$ the three greatest elements of $(q_n)$, then these can (and in case they are uniquely determined must) be chosen such that one of them is adjacent to both of the others; if $q_t > q_s, q_r$, then $q_t$ is located between $q_r$ and $q_s$, i.e. either $r = t-1 \wedge s = t+1$ or $r = t+1 \wedge s = t-1$.*

*Proof.* To avoid some technical details we only prove the case where all elements of $(q_n)$ are pairwise distinct. Similar arguments can be applied for the general case, but some special instances must be taken care of. We first prove that $(q_n)$ has to be unimodal. To see this, let us assume the existence of a wire ordering $(q_n)$ minimizing (3)-(5) that is not unimodal. Then there exists an index $1 < t < n$ such that $q_{t-1} > q_t < q_{t+1}$, and we choose $t$ to be minimal with that property; we may w.l.o.g. assume $q_{t-1} \leq q_{t+1}$. Let $(p_n)$ be the sequence defined by

$$p_n := \begin{cases} q_n, & \text{for } n \neq t-1, t, t+1 \\ q_t, & \text{for } n = t-1 \\ q_{t-1}, & \text{for } n = t \\ q_{t+1}, & \text{for } n = t+1. \end{cases}$$

Then the objective function for $(p_n)$ differs from that of $(q_n)$ by

$$\sqrt{q_t + q_{t-2}} + \sqrt{q_{t-1} + q_t} + \sqrt{q_{t+1} + q_{t-1}}$$
$$-\sqrt{q_{t-1} + q_{t-2}} - \sqrt{q_t + q_{t-1}} - \sqrt{q_{t+1} + q_t}$$
$$= \sqrt{q_{t-1} + q_{t-2} - (q_{t-1} - q_t)} - \sqrt{q_{t+1} + q_{t-1} - (q_{t-1} - q_t)}$$
$$-\left(\sqrt{q_{t-1} + q_{t-2}} - \sqrt{q_{t+1} + q_{t-1}}\right)$$

As $q_{t+1} + q_{t-1} \geq q_{t-1} + q_{t-2} > 0$ and $q_{t-1} - q_t > 0$ we can apply lemma 1 to see that the objective for $(p_n)$ is less than for $(q_n)$, an obvious contradiction.

For the second claim of our theorem assume again that $(q_i)$ is optimal with maximal element $q_t$ and $q_s$, $q_r$ as defined in the theorem. Again, to avoid some technicalities we assume all elements of $(q_n)$ to be pairwise distinct. Now suppose $q_t > q_r$, $q_s$ is not located between $q_s$ and $q_r$, then due to unimodality both $q_s$ and $q_r$ have to be on the same side of $q_t$, we assume w.l.o.g. that $s, r > t$, therefore $q_{t-1} \leq q_r \leq q_s \leq q_t$. Also due to unimodality, $s = t+1$, $r = t+2$ (there can be no smaller element between them, because $q_t$ is the unique mode of the sequence). Now we can reorder the sequence by changing the places of $q_t$ and $q_s$ without destroying unimodality, hence we define $(p_n)$ by

$$p_n := \begin{cases} q_n, & \text{for } n \neq t, t+1 \\ q_{t+1}, & \text{for } n = t \\ q_t, & \text{for } n = t+1. \end{cases}$$

Then

$$\sum_{n=1}^{N+1} \sqrt{q_n + q_{n-1}} \leq \sum_{n=1}^{N+1} \sqrt{p_n + p_{n-1}}$$
$$\iff \sqrt{q_t + q_{t-1}} + \sqrt{q_{t+1} + q_t} + \sqrt{q_{t+2} + q_{t+1}}$$
$$\leq \sqrt{p_t + p_{t-1}} + \sqrt{p_{t+1} + p_t} + \sqrt{p_{t+2} + p_{t+1}}$$
$$\iff \sqrt{q_{t+2} + q_t - (q_t - q_{t+1})} - \sqrt{q_t + q_{t-1} - (q_t - q_{t+1})}$$
$$\leq \sqrt{q_{t+2} + q_t} - \sqrt{q_t + q_{t-1}},$$

and we use the same argument as above to obtain a contradiction. Consequently, $q_s$ and $q_r$ both have to be adjacent to the maximal element $q_t$. □

From the two statements of theorem 4 we may now deduce our central conclusions. We will prove the induction step separately to make things more concise.

**Theorem 5.** *A wire ordering $(q_n)$ for a problem of size $N+1$ is optimal if and only if the sequence $(q'_n)$ defined by removing a maximal element from $(q_n)$ is an optimal wire ordering for the reduced problem of size $N$.*

*Proof.* First, let $(q_n)$ minimize the sum $v := \sum_{n=1}^{N+1} \sqrt{q_n + q_{n-1}}$ and let $c$ be the maximal element of the wire ordering, $a$ and $b$ the two elements next in size which are both adjacent to $c$ by theorem 4. Then by removing $c$ we define a wire ordering $(q'_n)$ with objective value $v' = v - \sqrt{a+c} - \sqrt{c+b} + \sqrt{a+b}$. Now suppose there is a wire ordering $(p'_n)$ with objective value $w' < v'$. The elements $a$ and $b$ are the two greatest elements of $(p'_n)$, therefore they have to be adjacent and we can define a sequence $(p_i)$ by inserting $c$ between $a$ and $b$. The objective value of $(p_n)$ is $w = w' - \sqrt{a+b} + \sqrt{a+c} + \sqrt{c+b}$, so $w < v$, contradicting the optimality of $(q_n)$.

To see the other direction, let $(q_n)$ be some wire ordering of length $N+1$ with objective value $v$, greatest element $c$ and adjacent elements $a$ and $b$, such that $(q'_n)$ defined by removing $c$ from $(q_n)$ minimizes $v' = \sum_{n=1}^{N} \sqrt{q'_n + q'_{n-1}}$. Suppose $(q_n)$ is not the optimal wire ordering for length $N+1$, then there exists a sequence $(p_n)$ with objective value $w < v$ and we can define $(p'_n)$ with objective value $w'$ by removing $c$ from $(p_i)$. Again, we know $w = w' + \sqrt{a+c} + \sqrt{c+b} - \sqrt{a+b}$ and $v = v' + \sqrt{a+c} + \sqrt{c+b} - \sqrt{a+b}$, so $w' < v'$, contradicting the optimality of $(q'_n)$.                                      $\square$

It is now easy to see that the construction provided in theorem 1 simply formalizes the induction step given in theorem 5. We are finally ready to prove theorem 1.

*Proof (of theorem 1).* We proceed by induction. The construction given in the theorem mimics exactly the statement of theorem 5, so the induction step is clear. For the induction basis, let us examine the case of $n = 3$. Here we have real numbers $0 < d \le e \le f$ and the ordering arising from the construction is either $(0, d, f, e, 0)$ or $(0, e, f, d, 0)$, depending on whether we insert $e$ on the right or on the left of $d$. From theorem 4 we know that the optimal solution has to be unimodal with mode $f$ and $d$ and $e$ have to be adjacent to $f$, so apart from the constructed sequences there are no possible solutions. Furthermore, the objective values of the two possible solutions are equal, so both are optimal.    $\square$

## 4   Experiments

Without proof we propose that there also exists a permutation for which the power is worse than for any other permutation. This will shed light on the benefits expected from power optimal wire ordering. In other words, one who does not consider the actual wire order could abandon power savings anywhere between 0 and the maximum optimization potential. Note that the effect of wire spacing [13] alone is not subject of this document.

In our experiments we are considering $(\kappa_n)$ to be similar to an industrial $\mu$processor [3]. For several values of $N$, we randomly selected a set of $N$ parallel wires. Each of these sets were permuted three times: for power optimal, for
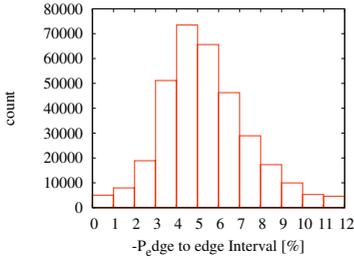
**Fig. 4.** Histogram for N=64, M=65
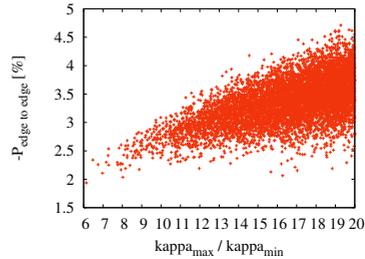


**Fig. 5.** $\kappa_{max} : \kappa_{min}$ vs. $-P$ scatter plot

power worst, and a for a typical ordering found for buses. The latter distribution is simply ordered by $\kappa$. Buses are typically arranged that way, assuming a descending toggle rate from the least to the most significant bit. A geometric program solver [6] is used to find the optimal power optimal values for various $M$s. An outer loop repeated the test some 300,000 times. We related the resulting average worst-case power and bus power values to the best-case power for each $N, M$ combination.

Tables 1 and 2 display the optimization potentials for the worst possible scenario and the bus scenario, respectively. For example, The edge-to-edge power for $N = 64$ wires routed on $M = 65$ tracks could be up to 3.4% worse if wire ordering was not cared for. It is interesting to note that this number is almost the same for any value of $N$, if $M = N + 1$. We further remark that most of the optimization potential can be exploited by adding only limited extra space.

Figure 4 shows the experimental results for $N = 64$ and $M = 65$ as histogram in 1% intervals. For the same parameters we scatter plotted the optimization potential as a function of the fraction of the highest and lowest $\kappa$ appearing in the design, cf. Figure 5. This is an interesting source of information for the system designer. One can make out an upper optimization limit depending on only two circuit properties. The CPU-time to optimize an $N = 256$ (512, 768, 1024) case is $1.2s$ (15.1s, 41.2s, 113.9s) on a 3GHz PC.

## 5   Conclusion

**Future Remarks.** The model does not respect the effect of fringe capacitances and capacitances to other wires on the same layer. However, the applicability of the simpler $1/d$ model for $C$ is shown in [13]. If a more detailed model is desired, capacitance extractions can be done to find fitting functions for $C$. Presuming these fitting functions remain posynomial, a globally optimal solution

**Table 1.** Max. Reduction potential [%]

| $N \backslash^M$ | N+1 | 1.25N | 1.5N | 1.75N |
|---|---|---|---|---|
| 8 | 3.5 | 5.8 | 8.3 | 9.6 |
| 16 | 3.6 | 9.3 | 12.4 | 13.7 |
| 64 | 3.4 | 16.5 | 19.2 | 19.9 |
| 256 | 3.0 | 20.3 | 22.5 | 22.7 |

**Table 2.** Red. potential [%] for buses

| $N \backslash^M$ | N+1 | 1.25N | 1.5N | 1.75N |
|---|---|---|---|---|
| 8 | 2.6 | 4.3 | 6.2 | 7.2 |
| 16 | 2.7 | 7.4 | 9.9 | 10.9 |
| 64 | 2.6 | 14.4 | 17.0 | 17.6 |
| 256 | 2.3 | 19.0 | 21.1 | 21.3 |

exists for the newly created problem [1]. Miller-capacitances and hence crosstalk power and signal integrity issues are not considered in this paper. Furthermore, the effect on timing of the proposed methodology has not been in the focus of this contribution. However, with little modifications in the objective function, targeting the timing problem with the same notion becomes possible.

**Summary.** In this paper a significant step forward was taken from power optimal wire spacing through *geometric optimization* alone. A proof was given for the presence of a power optimal order of wires that increases the effect of spacing. The order can be very simply arranged given the sorted power weighting factors of the involved wires. After ordering, *geometric optimization* delivers the globally best possible result without the use of heuristics.

Extensive investigations show the potential of power optimal ordering. On broad buses, the power values for optimally ordered wires and those for an unoptimized order can differ by a two-digit percentage. Interesting results are further the saturating optimization potential for increased space and the dependency of the expected savings only on the highest and lowest value of $\kappa$.

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