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Highly Reliable Contacts to Silicon Enabled by Low Temperature Sputtered Graphenic Carbon

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ABSTRACT Titanium silicide (TiSi) contacts are frequently used metal-silicon contacts but are known to diffuse into the active region under high current density stress pulses. Recently, we demonstrated that graphenic carbon (GC) deposited by CVD at 1000 °C on silicon has the same low Schottky barrier as TiSi, but a much improved reliability against high current density stress pulses. In this paper, we demonstrate now that the deposition of GC is possible at 100 °C − 400 °C by a sputter process. We show that the sputtered carbon-silicon contact is over 1 billion times more stable against high current density pulses than the conventionally used TiSi–Si junction, while it has the same or even a lower Schottky barrier. SC can be doped by nitrogen (CN) and this results in an even lower resistivity and improved stability. Scalability of the CN thickness down to 5 nm is demonstrated. The finding that there is a low temperature approach for using the excellent carbon properties has important consequences for the reliability of contacts to silicon and opens up the use of GC in a vast number of other applications.

INDEX TERMS Carbon, contact resistance, ESD, graphene, metal-semiconductor, reliability, PVD, Schottky barrier, Schottky diode, silicide, sputterig, TiSi.

I. INTRODUCTION

Metal to semiconductor contacts are essential elements in integrated and discrete electronic devices. Common source and drain contacts in state-of-the-art FinFETs rely on the formation of titanium silicide (TiSi) [1]–[3]. TiSi provides a very low Schottky barrier height (SBH) to silicon, that's why it is also highly appropriate for Schottky diodes in zero bias detector and mixer applications up to THz frequencies [4], [5]. The low barrier height makes TiSi very promising for further contact resistance reductions to NMOS and PMOS devices [6], [7]. However, titanium-based contacts exhibit a low thermal stability [8], [9], which is not suitable for increased Joule heating by large current densities in downscaled devices.

The high current density j during an electrostatic discharge (ESD) event can induce high temperatures in the device as the power P per volume V (power density) in a conductor during an ESD event is given by

$$\frac{P}{V} = j \cdot E = j^2 \cdot \rho. \tag{1}$$

Here, E is the local electric field and ρ is the electrical resistivity of the conductor. The damage to the device and consequently the reliability is mainly influenced by the magnitude of the applied current density, which is why we only consider current pulses in the following. A pulse can hence force a diffusion and migration of the interface material or the top metallization into silicon, which degrades the inherent electrical properties of the interface contact or even cause a complete failure of the device due to a junction burnout [10]–[17].

Graphene [18] still lacks being used in semiconductor devices but is heavily investigated for next generation interconnects. It was demonstrated that copper (Cu) wires encapsulated by graphene [19] and doped individual

multilayer graphene-nanoribbon [20] are very promising in their electrical and reliability properties to improve or replace the predominantly used Cu interconnects. Graphenic carbon (GC) materials [21]–[23] gained already some attraction for their adoption in semiconductor products. Previously, it was utilized as electrodes in DRAM capacitors [24], as switching material for non-volatile memories [25] and as highly stable membranes [26].

We reported earlier [10], [11] that a CVD-deposited GC contact to silicon (CVD-C-Si) has similar electrical properties as TiSi-Si but a much higher temperature stability and a more than 100 million times improved stability against ESD current pulses. Unfortunately, the deposition temperatures of 850 °C – 1000 °C are not compatible with many applications where temperature budget restrictions of about 400 °C for middle and back end of line (MOL/BEOL) of advanced nodes are in place. More recently, we demonstrated that a low temperature sputtered graphenic carbon (SC) is possible and the SC could be doped with nitrogen (CN), which lowers the resistivity. SC and CN showed an enhanced reliability compared to CVD-C-Si and TiSi-Si [27]. In this extended paper, we will discuss these results more thoroughly as we review the carbon deposition process and related electrical properties in much more detail.

II. SPUTTERED CARBON – PROCESS AND PROPERTIES

Sputtered carbon can form a large variety of allotropes, ranging from graphitic/graphenic to diamond-like formations. It heavily depends on the sputtering method and deposition parameters [28]. Our focus is more on the electrical properties of the film where the electrical resistivity ρ was reported to range from $10^{-2}\,\Omega\,\text{cm}$ to $10^{10}\,\Omega\,\text{cm}$ [28]–[34].

We sputtered carbon in a physical vapor deposition (PVD) process from a 4" graphite target (purity 99.999 %) with an RF magnetron plasma source on a non-biased but heated substrate, which was 70 mm away from the carbon target. The base pressure in the sputter chamber, which is equipped with a liquid nitrogen cold trap, was $< 2 \times 10^{-7}$ mbar. The plasma was operated at very low argon (Ar) pressure p (2 µbar to 16 µbar) as such a range is necessary to achieve a very low resistivity [29].

Furthermore, we investigated the nitrogen-doped carbon films, as nitrogen (N) can reduce the resistivity of the carbon film and values $< 10^{-2}\,\Omega\,\text{cm}$ are reported [35]. The N-doping leads to a shift of the Fermi level towards the conduction band, that's why nitrogen acts as electron donor and is considered as n-type doping [36], [37]. We prepared the CN films with the same process setup as for SC, only the nitrogen gas (N_2) was added to the argon gas (Ar). The maximum available gas flow ratio in our setup, restricted by the mass flow controllers, was $Ar/N_2 = 56$. This leads to a concentration of 3.5 at. % N in the plasma. The incorporated content of N in the CN films was measured by XPS to be in the order of 11 at. %. This is different to [38] and [39] as they measured, it stays below 5 at. % at this nitrogen/argon ratio – at least for the unbalanced magnetrons that they were using. All the sputtered films showed very good adhesion to Si, SiO_2 and SiN, as if covalent bonds are formed. The adhesion to the metal parts in the PVD chamber is generally not very strong. A good adhesion is only achievable if the parts are bead blasted or well precoated with titanium.

The deposition of SC and CN was performed on a heatable substrate holder at temperatures T ranging from 20 °C to 400 °C directly on polished silicon with thermal silicon oxide (SiO_2) on top. An additional heating of the sample due to the plasma irradiation was not taken into account. The temperature and pressure are key parameters for the crystallinity of the film [40].

The Raman spectra in Fig. 1(a) highlight that SC sputtered on a substrate with a temperature of 20 °C has no clearly distinguishable D- and G-peak, which is generally observed for amorphous structures [41]. In contrast, a film deposited at 400 °C clearly shows the D- and a dominating G-peak, which indicates that graphenic sp^2-bonds are present. An annealing of a SC film deposited at 20 °C at 550 °C in hydrogen (H_2) for 1 h is necessary to get a Raman spectrum, which shows similar graphenic features. The CN films clearly display a D- and a dominating G-peak at all temperatures showing a higher content of sp^2-bonds [42]. The C≡N peak in the Raman spectrum indicates that sp-bonded N is incorporated into the film, but also sp^2- and sp^3-bonds between C and N are formed during the sputter process.

A surface analysis with an atomic force microscope (AFM), like shown in Fig. 1(b)-(g), underlines that the SC sputtered at 20 °C has a very low surface roughness and no grain boundaries are recognizable as it is more amorphous. At 400 °C substrate temperature, the surface is rougher and polycrystalline graphitic clustering occurs. The CN film features a much smaller grain size at 400 °C associated with a smoother surface. The CN films sputtered at 20 °C exhibit a very similar surface as the film deposited at higher temperature.

III. SCHOTTKY DIODE TEST VEHICLE

The reliability of a metal-semiconductor interface is frequently evaluated with Schottky diodes for high frequency applications. These devices are very prone to any changes at the junction region, which can be enforced by an electrical stress or just by high temperatures [43]–[46]. A damaged or deteriorated diode can be identified by monitoring the characteristics of the Schottky diode at a fixed reverse bias voltage. A degradation of the properties shows up as an increased reverse leakage current [11]. The reliability of the devices, and consequently of the metal-semiconductor interface, is often investigated with a high voltage or current pulse, like shown in Fig. 2(a). The pulses have commonly a width of 100 ns [47] which is similar to the ANSI/ESDA/JEDEC JS-001-2012 Human Body Model [48] and the IEC61000-4-2 test standard [49].

In our experiments we used a vertical Schottky diode structure with an active area of 45.36 µm^2 to evaluate the impact

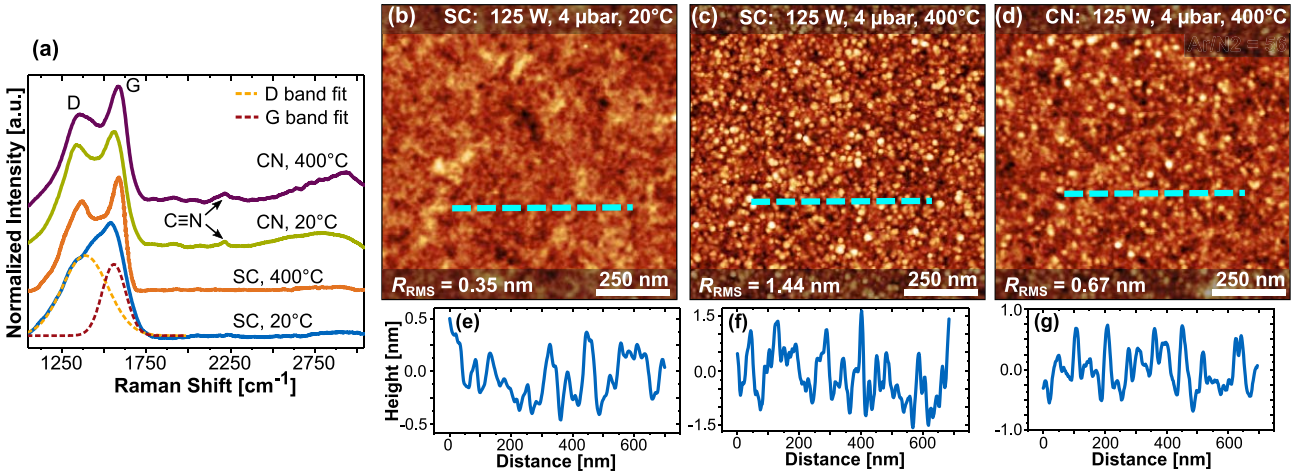

FIGURE 1. **(a) Raman spectra (offset for clarity) of SC and CN films sputtered at a substrate temperature of 20 °C and 400 °C, respectively. The used excitation wavelength is 532 nm. The spectrum of the SC film established at 20 °C is more of amorphous structure as indicated by the higher and wider D-peak than the G-peak of the Gaussian deconvolution of the spectrum. A ratio of ~1 of the fitted D- and G-peak (not shown) was found for CN at 20 °C. The pronounced G-peak is always higher than the D-peak for the films deposited at 400 °C, which indicates the prevalence of graphenic sp^2-bonds. (b)-(g) Comparison of the surface roughness and the corresponding height profile along the dashed line of SC and CN films measured with an AFM. (b) and (e) show the surface and profile of a SC film sputtered at 20 °C. The root-mean-square surface roughness (R_{RMS}) is only 0.35 nm. The profiles of a SC film sputtered at 400 °C in (c) and (f) show a rougher surface and the surface nucleation of carbon leads to a polycrystalline texture. (d) and (g) illustrate the surface and height profile of a CN film deposited at 400 °C. It is smoother than the SC sample deposited at 400 °C as CN seems to have a higher nucleation density and growths more in a nanocrystalline fashion.**

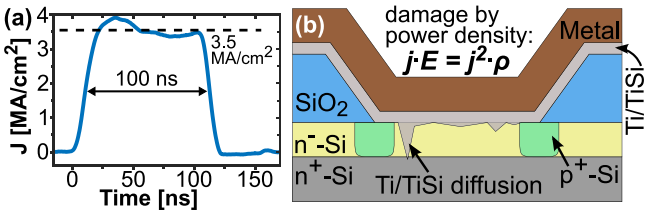

FIGURE 2. **(a) A measured waveform of a 100 ns current pulse with a rise/fall time of < 15 ns and an average current density $j = 3.5 MA/cm^2$, which was measured with a Tektronix CT-1 current sensor. (b) Schematic cross-section of a TiSi-Si Schottky diode where Ti or TiSi diffuses into the n^--Si epitaxial layer and could even reach the highly doped substrate by the application of high current pulses. Adapted from [11].**

of a high current pulse on the reliability of the metal-silicon interface. The used test vehicle is a BAT15 Schottky diode from Infineon [50], a low SBH diode for mixer and detector applications. In its commercial available version it uses TiSi as the interface material to silicon (TiSi-Si) and consists of a thin n^--epitaxial layer with a thickness of 150 nm. This thin layer is very susceptible to degradations in its electrical reverse bias characteristics when contaminations like metal ions enter this epitaxial region. Pulses with high power density can force the diffusion of Ti/TiSi into the epitaxial layer which can short-circuit the diode, like illustrated in Fig. 2(b).

IV. ELECTRICAL CHARACTERIZATION

In Fig. 3(a)-(c), we evaluated the electrical film resistivity ρ by a four probe measurement as a function of the used RF power P, working pressure p and substrate temperature T on silicon substrates with 300 nm of SiO_2 on top. The sputtered films had a thicknesses of 35 nm. From Fig. 3(a), one can conclude that a further increase of power could lead to an even lower resistivity as the slope is quite linear and doesn't converge to a minimum value within the displayed range. The CN film exhibits a 2-times lower resistivity at the same sputter conditions as nitrogen acts as an electron-donor and therefore approaches the value of CVD-C (~ 1 mΩ cm), which was deposited at 1000 °C. A further increase in the power could lead the way to an improved carbon film but we were cautious not to overheat the target.

The sputtered film resistivity is quite sensitive to the pressure and increases for > 8 µbar very rapidly and the minimum ρ might not be located much below 2 µbar, like illustrated in Fig. 3(b). For our electrical evaluations, we used 4 µbar instead of 2 µbar or lower, even if it would lead to a lower ρ, as the surface analysis showed a higher surface roughness at lower pressure.

An increase in the substrate temperature leads to a strong decrease in the resistivity as a graphitization seems to occur at increased temperatures (Fig. 3(c)).

Furthermore, the sputtered carbon films show a negative temperature coefficient (NTC) like the CVD-C, as displayed in Fig. 3(d). At an increased temperature more electrons are populating the conduction band, which is more pronounced in high resistivity samples. The carbon film deposited at 20 °C shows at 200 °C an ~65 % higher conductivity. In contrast, the CVD-C is at room temperature already a good conductor with already more free electrons available and this results in a ~15 % conductivity increase at 200 °C.

When exposed to atmosphere, the resistivity of SC continuously drifts to higher values. The relative drift, which saturates after a few days at about 50 % to 100 % above the as-fabricated value, depends on the sputter process

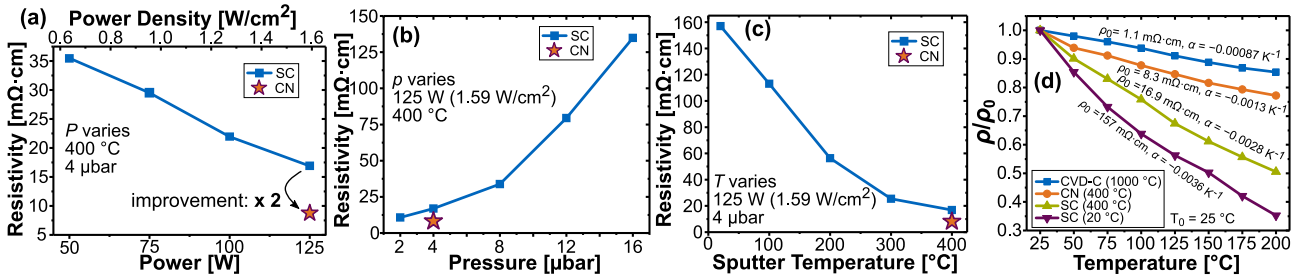

FIGURE 3. **Dependence of the electrical resistivity ρ of SC films on the sputter condition and in comparison with a CN film. The values of power *P*, pressure *p* and the deposition temperature *T* are 125 W (1.59 W/cm²), 4 µbar and 400 °C, respectively, if they were not varied. The ratio of the sputter gas flow for the CN film is $Ar/N_2 = 56$, as a lower ratio leads to higher resistivity. (a) shows ρ of SC for different sputtering power *P* and compares it to the CN film. (b) and (c) show ρ as a function of *p* and of *T*. (d) Measurement of the temperature-dependent relative electrical resistivity ρ/ρ_0 of CVD-C deposited at 1000 °C, CN deposited at 400 °C and SC deposited at 400 °C and 20 °C, respectively. ρ_0 is the initial resistivity at $T_0 = 25$ °C. All of them feature a NTC α, which was fitted for simplicity with a linear behavior over the measured *T* range.**

conditions. Similar findings where previously reported by Broitman *et al.* [35]. In contrast, the CN films was stable at all times and the variation there was below 1 %.

A BAT15 silicon test vehicles with all the same dimensions, dopants and guard ring structure as the commercial available device was used to sputter carbon or nitrogen-doped carbon as "metallic contact" onto silicon, like shown in Fig. 4(a). This enables a direct comparison of SC-Si and CN-Si to TiSi-Si and CVD-C-Si [11]. The substrates were prepared by ultrasonic cleaning in acetone and isopropyl alcohol before a full RCA clean. It is very crucial to have a contamination-free silicon substrate for the reliability tests as every ion or impurity could contribute to a possible degradation of the device. The native oxide on the devices was immediately removed before the sputter deposition by a dip in a 5 % solution of hydrofluoric acid (HF) to get a pure hydrogen-terminated silicon surface on the BAT15 structure and a well defined carbon-Si interface. The time delay between HF-dip and insertion to the sputter chamber was below 3 min. The delay between insertion and deposition was 20 min due to the heating of the substrate to 400 °C before the deposition was started.

The top metallization of the diodes consists of a stack of 50 nm of Ti, 1.2 µm of Cu and 40 nm of Au, which was deposited by electron-beam evaporation through a shadow mask onto SC or CN. No additional annealing of the metal stack was performed after the deposition. The thick Cu acts as additional heat sink and prevents current crowding during the device operation. Finally, the carbon was structured in a H_2 plasma with the top metallization acting as a hard mask so that the carbon is fully removed at the non-covered regions.

The dc characteristics in Fig. 4(b) illustrate that the SC-Si diode prepared at 20 °C results in a non-ideal diode characteristics. The reason for this is not evaluated in detail but it points more likely to the non-metallic Poole-Frenkel emission transport in the carbon film, which is often observed for amorphous carbon [33], [51]. However, a substrate temperature of 100 °C is sufficient to change the dc characteristics to that of a Schottky diode having a low ideality factor as the

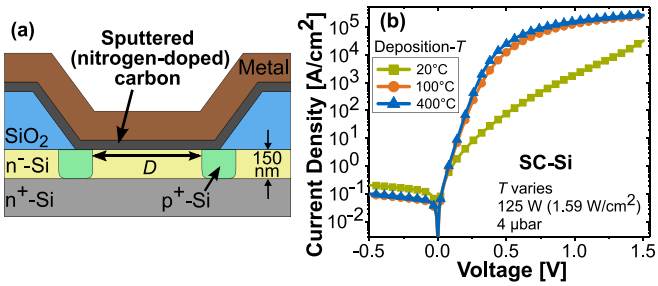

FIGURE 4. **(a) A schematic cross-section of the used Schottky diode with guard ring structure, based on the BAT15 diode, and SC or CN as interface material to silicon. The diameter *D* of the active region is 7.6 µm (area is 45.36 µm²). (b) *J-V* curves of SC-Si diodes sputtered at different sputter temperatures whereas power and pressure were kept constant. The diode sputtered at 20 °C has a lower SBH (0.45 eV) but the forward behavior is far from ideal. A substrate temperature of 100 °C is sufficient to change the conduction properties of the carbon-silicon interface and the diode shows electrical characteristics close to a device sputtered at 400 °C.**

SC gets metallic, graphenic properties. A further increase in the deposition temperature results in a even better characteristics, which results in a slightly better ideality factor and lower series resistance.

The SC-Si diode is even close to the electrical characteristics of a TiSi-Si and a CVD-C-Si diode as it also shows a low Schottky barrier height (SBH) of 0.48 eV (Fig. 5(a)). The CN-Si deposited at a 400 °C substrate temperature exhibits a much lower SBH (0.42 eV), which is beneficial for the creation of low ohmic contacts but the characteristic in forward direction is not as ideal as the TiSi-Si diode. The breakdown voltage and the reverse leakage depend on the SBH of the contact and the used temperature budget, which can induce a diffusion of the dopants (Fig. 5(b)). The CN-Si diode even performs better than a CVD-C-Si diode as it has a lower SBH but the breakdown voltage is the same. It has lower leakage current at $V_r > 1$ V because the CN was deposited only at 400 °C in contrast to the 1000 °C used in the CVD process. No dopant diffusion occurs at low deposition temperatures, which would otherwise change the reverse breakdown voltage.

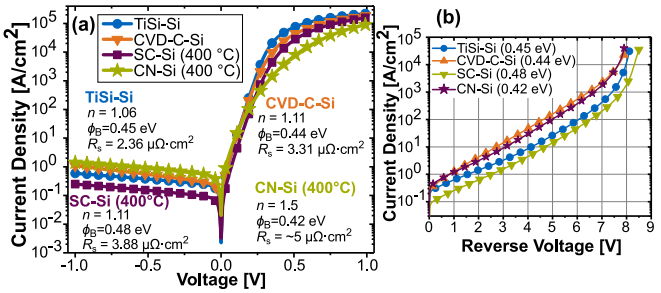

FIGURE 5. Comparison of the dc characteristics of a TiSi-Si, a CVD-C-Si, a SC-Si and a CN-Si diode. The thickness of the CVD-C is 28 nm and of the SC and CN is 35 nm. (a) Ideality factor n, SBH ϕ_B and area-normalized series resistance R_S are displayed. The electrical properties of all types of carbon on silicon are very close to TiSi-Si. The CN-Si has even a lower SBH but an increased ideality factor and higher serie resistance. (b) The reverse current characteristics are shown up to the voltage where the breakdown occurs. The higher the SBH, the higher is the observable reverse breakdown voltage. The CN-Si has a lower SBH but the breakdown voltage is almost the same as for the CVD-C-Si. In addition it shows a lower leakage current at $V_r > 1$ V. The CN was deposited at 400 °C only, where no dopant diffusion occurs. In contrast to this, the 1000 °C of the CVD process reduces the epilayer thickness a bit, which gives rise to an earlier breakdown.

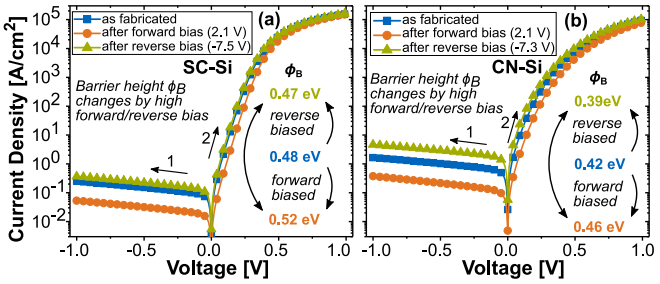

FIGURE 6. Comparison of the dc-characteristics of a SC-diode (a) and a CN-diode (b) as fabricated, after being forward biased with 2.1 V and after being reverse biased with 7.5 V or 7.3 V, respectively. The reverse characteristics were measured before the forward direction at the illustrated curves. The SBH ϕ_B changes according to the applied polarity and is reversible by applying the opposite polarity.

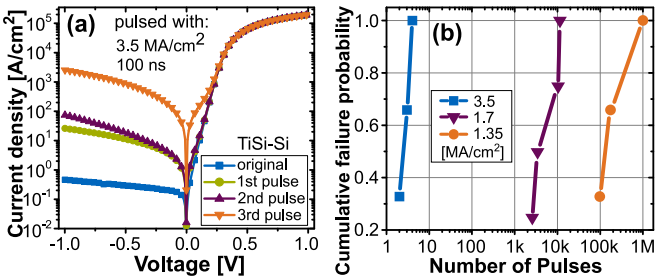

FIGURE 7. The *J-V* curves in (a) show the degradation of a TiSi-Si diode pulsed with $j = 3.5$ MA/cm² and a pulse width of 100 ns. Every single pulse led to a deterioration of the reverse behavior of the diode and after the third pulse the reverse current has increased severely [11]. (b) illustrates the failure probability versus number of current pulses at different current densities for commercial BAT15 diodes with TiSi-Si interface [10]. At least three devices were stressed for a given pulse current density, a pulse width of 100 ns and a duty cycle < 0.0001. The failure of the diode was defined when the diode degrades to a reverse current > 220 A/cm² @ $V_r = 1$ V.

A dc voltage stress with high forward V_f and reverse bias V_r leads to a change in the interface properties of SC-Si and CN-Si, especially in a change of the SBH. The normal or safe operation was defined in $V_r < 4$ V and $V_f < 1$ V were almost no changes in the pristine device properties are detectable. As illustrated in Fig. 6, dc sweeps to $V_r = 7.5$ V or $V_r = 7.3$ V, a voltage level which is at least 0.5 V below the breakdown, leads to a decrease in the barrier height. The CN-Si contact is even decreased to 0.39 V, which paves the way for a "zero-barrier height" as it is about 13 % lower than the TiSi-Si contact. An device operation at higher forward bias $V_f > 1$ V shows the opposite behavior as the SBH increases. After a dc sweep to 2.1 V an about 10 % lower SBH is obtained. Applying a constant high forward or reverse voltage for a much longer duration leads to even higher or lower SBH, respectively. The process hereby is fully reversible as a high SBH can be made smaller and vise versa. A higher SBH is easier to reach as the necessary voltage to force a change is lower. Also repeated dc cycles or constant reverse bias are needed to retrieve the lower SBH. Without an applied bias the SBH is stable over time and doesn't recover back to the start value. The diode behaves as if an interface dipole is present, which is a well-known phenomena in carbon-silicon carbide contacts [52], [53].

V. TISI-SI INTERFACE RELIABILITY

The commercially available TiSi-Si-BAT15 Schottky diode was pulsed at room temperature with a current density j of 3.5 MA/cm² and a degradation can be detected as an increased leakage current at a reverse voltage $V_r = 1$ V, as indicated in Fig. 7. The diode characteristics starts to degrade from the original behavior, as indicated by the over 100x increase of the reverse current (Fig. 7(a)). This signals the inter-diffusion of Ti/TiSi within the epitaxial layer. Furthermore, the device is short-circuited after 3 pulses as a metal or silicide filament might be created, as schematically depicted in Fig. 2. Fig. 7(b) clearly highlights that 2-4 pulses are sufficient to destroy the TiSi-Si junction at 3.5 MA/cm². The current pulse used has a duty cycle < 0.0001 and a waveform as shown in Fig. 2(a). This low duty cycle allows the diode to cool down to room temperature after each current pulse. The condition of the diode was monitored at a reverse voltage of $V_r = 1$ V and the diode is declared as failed if the reverse current reaches a value of 100 μA (220 A/cm²) as the on/off ratio of the diode is then deteriorated by a factor of more than 500. In addition, Fig. 7(b) illustrates that the maximum number of transient stress pulses depends on the current density level used. The probability of a possible damage to the diode is reduced when the pulses have a lower current density as the power density is proportional to j^2 (see in (1)). For 1.35 MA/cm², which is slightly above the permissible pulse load of 1.21 MA/cm² specified by the manufacturer, the diode is able to withstand up to one million events, but the failure probability is spread over a wide range [10], [11].

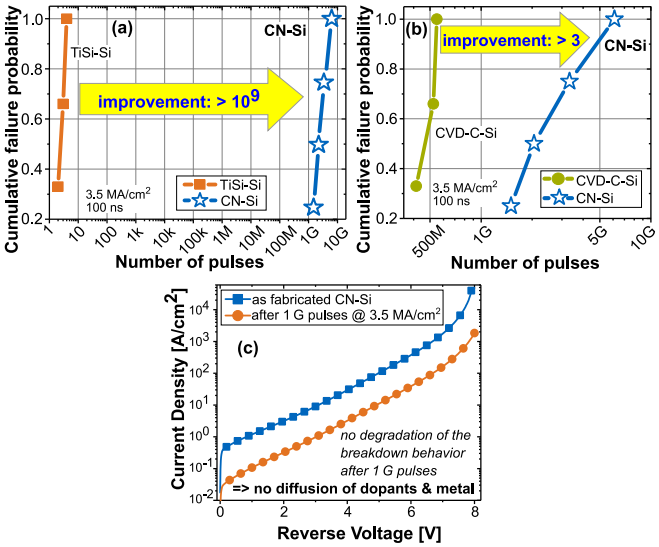

FIGURE 8. **Pulse endurance comparison of TiSi-Si (BAT15) with CN-Si diodes (a), and CVD-C-Si with CN-Si diodes (b) for a current density of 3.5 MA/cm^2 and a pulse width of 100 ns. The CN-Si diodes can withstand at least over 1 billion pulses more than the TiSi-Si diodes and 3-times more than the CVD-C-Si. The CN-Si values are only lower bounds as the pulsing of the CN-Si contact (non-filled stars) has been aborted not due to failure but due to the excessive testing time. The duty cycle was < 0.00015. (c) Reverse dc characteristics of a CN-Si diode as fabricated and after 1 G pulses. The SBH was increased due to the interface reactions due to the high interface temperature induced by the pulse. The reverse blocking capability was improved as the SBH has increased. The onset of the reverse breakdown is not shifted to lower voltages. This would point to a diffusion of dopants as it would decrease the total thickness of the epilayer, or it would point to the creation of a filamentary current by diffused metals.**

VI. SPUTTERED CARBON-SILICON RELIABILITY

The diodes with sputtered carbon of a thickness of 35 nm were stressed with pulses having a current density of 3.5 MA/cm^2 and a duration of 100 ns to allow for a direct comparison with the results obtained from TiSi-Si and CVD-C-Si diodes. The CN-Si-diode outperforms the stability of the TiSi-Si contact by more than a factor of one billion, like illustrated in Fig. 8(a). All the shown values of the CN-Si diodes are lower bounds as the devices did not fail, but the tests were stopped due to accrued testing time of several months. The duration between two subsequent pulses could not be chosen arbitrary small as the device needs a certain time to cool down to room temperature. The CVD-C-Si, deposited at much higher temperature (1000 °C), already showed an over 100 million times better reliability than TiSi-Si [10], [11], which in turn implies that CN-Si outperforms the reliability of CVD-C-Si, as shown in Fig. 8(b), by a factor of over three. This results underline, that the sputtered carbon is in its structure dense enough to act as excellent diffusion barrier for metal. The reason for the enhanced reliability compared to the CVD-C-Si contact might be associated with the slightly higher thickness of 35 nm in contrast to 28 nm acting as a better diffusion barrier. In addition, the CN film has a slightly higher electrical resistivity and according to the FEM simulations in [11], a higher total resistance of the interface metal leads to a more homogeneous heat distribution in the active region during the current pulse.

The reliability test of one diode was stopped after 6.1 billion pulses and it simply showed an increased SBH of about 0.55 eV as all the other tested devices, but it was still fully functional. As a consequence, the reverse leakage is decreased, like shown in Fig. 8(c) for a diode after 1 billion pulses. The breakdown behavior did not deteriorate after so many pulses, which reveals that there was no diffusion of the interface metal or of dopants from the highly doped substrate into the thin epilayer. The change in the SBH might be similar to the results discussed in Fig. 6, as a thermally driven recrystallization or rehybridization at the CN-Si interface, due to the high power density of the pulse, might take place [52], [53]. A reverse voltage of 7.5 V for about 1 min is sufficient to change the SBH to the as fabricated or an even lower value. This indicates that the temperatures close to the melting point of silicon during billions of such ESD events [11] do not lead to a permanent change of the carbon-silicon interface.

In order to achieve the excellent reliability results, it is very important that all parts near the sputtering source and especially the sample holder and shutter are well coated with carbon. In the first test, the shutter was not well coated with carbon as the films adhered very poorly on the polished metal surface and a resputtering of the shutter material in this low pressure range is possible. In addition, a few milliseconds long exposure of a badly coated shutter to the plasma during the shutter operation from closed to opened position or if the shutter is left too close to the plasma source when opened could be enough to deposit contaminants on the silicon active region or in the carbon film. These trace amounts of metal can easily diffuse into the epilayer after a few 100 pulses and act as unwanted recombination centers leading to a deteriorated diode behavior, as shown in Fig. 9(a). After a continued application of pulses to the device two different scenarios are possible. At first, they can induce early failures during the reliability test as they create a local short-circuit. Second, the recombination centers almost disappeared again after several million of pulses, as the ions might react with the silicon and become inactive or they are diffused into the highly doped substrate before a more severe failure occurred.

The reliability results of the tested samples produced in a not well precoated equipment is distributed over a wide range, as highlighted in Fig. 9(c). A contamination-free carbon deposition can only be achieved after a precoating of the whole sputter equipment. Especially the magnetron shutter needs to be coated on all sides. The recombination current free *J-V* characteristics, shown in Fig. 9(b), can only be obtained after thorough precoating of all components. No recombination currents are observed then and only then we get excellent reliability of the CN-Si contact of several billion pulses without deterioration.

For longer pulse duration and the same current density of 3.5 MA/cm^2, CN-Si is not as reliable as CVD-C-Si (Fig. 10(a)). For a width of 300 ns the applied energy is

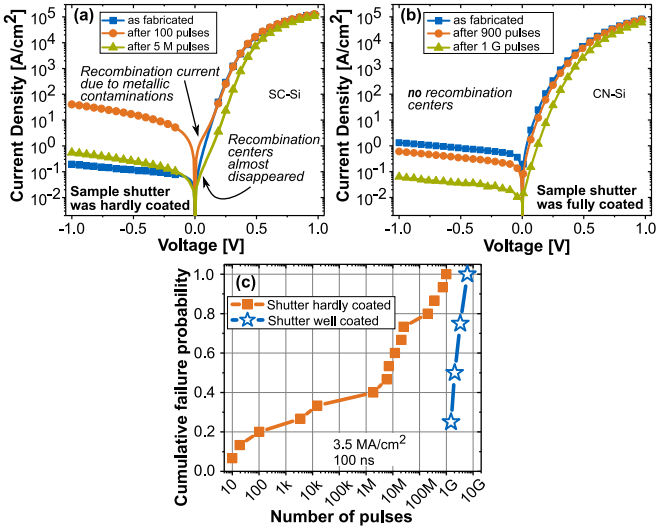

FIGURE 9. **The functionally of the diodes depends heavily on trace impurity contamination introduced from the far-reaching plasma interactions with the metallic components of the equipment and especially the shutter. Initially, the shutter was not well coated with carbon and recombination currents became visible after a few hundred pulses (a). Depending on the degree of contamination, they caused a short over time or they eventually vanished again (a). Initially, the pulse endurance reliability had a wide distribution as indicated in (c). Only after a carbon coating of all sides of the shutter and all components in the proximity to the plasma we were able to achieve a recombination current free *J-V* curve (b) and high pulse endurance (c).**

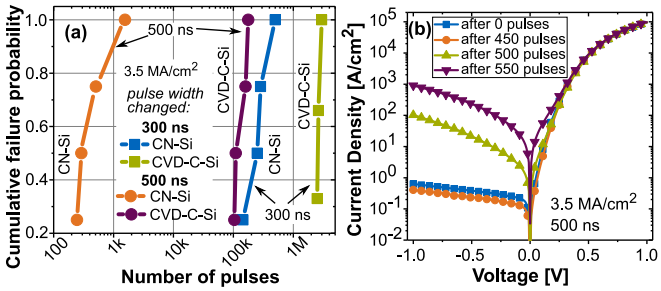

FIGURE 10. **(a) Pulse width dependent stress pulse endurance of CN-Si and CVD-C-Si diodes for a pulse width of 300 ns and 500 ns. The duty cycle was < 0.0001. In contrast to the behavior at 100 ns pulses, the CN-Si diodes fail earlier than CVD-C-Si diodes for longer pulse durations. (b) The J-V curves show the change in the dc-characteristics of a CN-Si diode with after several 100 current pulses (3.5 MA/cm², 500 ns) were applied. The electrical behavior is almost not affected after up to 450 pulses, only the SBH is slightly increased. After 500 pulses, the diode shows a first deterioration and is failed after additional 50 pulses.**

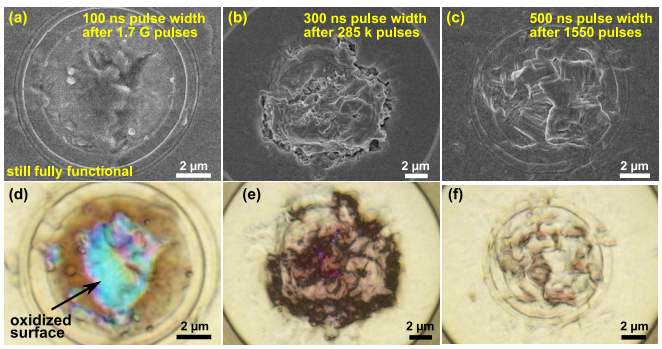

FIGURE 11. **SEM (a-c) and true color microscope images (d-f) of the top view of CN-Si diodes with Ti/Cu/Au as top metallization. All the devices where stressed at a current level of 3.5 MA/cm² while only the pulse length was altered. (a) and (d) show a still fully functional device after 1.7 G pulses of a width of 100 ns where almost no damage in the top metallization is visible. The change in the color indicates most likely that the temperature on the surface was high enough during the two weeks of testing to oxidize the Cu even through the Au capping. The failed diode in (b) and (e) demonstrates the damage of a 300 ns pulse after 285 k pulses where the metal even started to melt as it cracks and piles up. The change in color is despite the strong damage quite low. (c) and (f) show a destroyed sample where the current-induced damage of a 500 ns pulse just slightly melted the surface as the total number of stress events was lower.**

three times higher than in the previous test, but the reliability is still much higher than the TiSi-Si diodes at 100 ns. The device still endures here over 100 thousand pulses. The deviation to CVD-C-Si contact becomes larger for longer pulses (500 ns) but it withstands at least 250 events. Also a much lower duty cycle in the range of 10^{-6} did not lead to change in the pulse endurance. The reason for the reduced reliability might be the higher electrical resistance of the CN film. As the current through the diode is kept constant, more resistance leads to more dissipated power, which could enforce an earlier destruction. Fig. 10(b) illustrates, that a degradation doesn't occur gradually in a continuous fashion. The diode is fully functional after 450 pulses and is also very stable in its dc characteristics. It simply has a slightly higher SBH leading to a lower reverse current. After some more pulses are applied, a degradation of the device takes place as evidenced in the higher leakage current. Finally, the diode failed completely after 550 pulses.

The top metallization of a diode after being stressed with different pulse widths was analyzed with a scanning electron microscope (SEM) (Fig. 11(a)-(c)) and a confocal laser scanning microscope (Fig. 11(d)-(f)). For 100 ns long pulses, a visible damage on the surface is hardly recognizable, only the thermo-mechanical stress at each pulse causes a pile-up of the metal after 1.7 billion pulses. The true color image, however, shows a strong color change to more blueish or rainbow-like appearance, which points to a oxidized surface even through the top Au layer with a thickness of 50 nm. In contrast, a 300 ns long pulse rises the temperature of the metallization to a point where it even can start to melt and it is already cracked and heavily piled up after 285 thousand pulses. As the temperature at the interface must be much higher than at the surface [11], the carbon-Si demonstrates outstanding temperature stability. The 500 ns pulses cause less visible damage to the metal surface, which might be due to the lower number (1550) of stress pulses.

VII. SCALABILITY

In the previous sections we have studied the behavior of carbon layers with a thickness of about 30 nm. However, the interesting question, how thin the carbon layer can be made while maintaining the superb diffusion barrier property has not yet been investigated. A first outlook on the scalability of

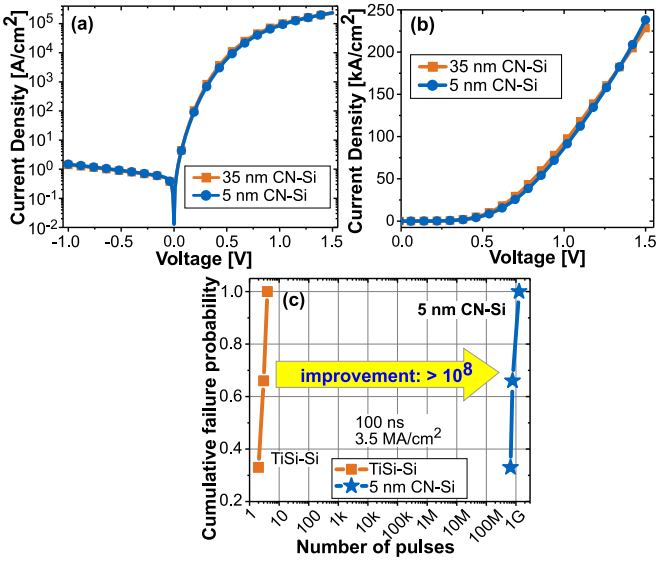

FIGURE 12. Comparison of the dc characteristics of CN-Si diodes with 5 nm and 35 nm thick CN in a semi-log (a) and linear (b) scale. Both curves almost match each other. (c) compares the failure probability of the 5 nm CN-Si to the TiSi-Si diodes under the same test conditions (100 ns, 3.5 MA/cm^2). The devices failed the reliability test within a window of 660 million to 1.28 billion pulses.

nitrogen-doped carbon films is illustrated in Fig. 12, where the behavior of a 5 nm thick CN film is shown. A 5 nm thick CN film has been grown by reducing the sputter time from 11 min (for 35 nm) to 2 min. The surface roughness of this film is $R_{RMS} = 0.35$ nm and therefore almost two times lower than the thicker carbon layer and similar to the SC film deposited at 20 °C. This means that the film grows very homogeneously, without pinholes. The electrical resistivity of the 5 nm thick CN is 8.4 mΩ cm, which is the same value as for the thicker sample.

The thin CN-Si contact gives the same low SBH of 0.42 eV as the 35 nm CN-Si junction (Fig. 12(a)). Both curves are almost identical but there is hardly an improvement in the series resistance of the diode with thinner CN. Therefore, the series resistance is mainly determined by the contacts and less by the thickness of the CN.

The reliability behavior of the thin CN contact is plotted in Fig. 12(c). It shows that even the 5 nm CN contact is superior to TiSi by a factor of over 100 million and can withstand up to 1.28 billion pulses before the diodes fail.

VIII. SUMMARY

We have demonstrated that it is possible to deposition graphenic carbon at temperatures below 400 °C by a sputter process. The carbon-silicon contact can compete in its electrical characteristics with the conventionally used TiSi-Si contact. In contrast to TiSi, it significantly improves the reliability against high current density stress pulses and even outclasses the high temperature-deposited CVD-C-Si contact. A doping with nitrogen improves the resistivity and stability but the optimum ratio of Ar/N_2 needs to be studied in more detail. An further improvement of the electrical properties of SC and CN can be expected by fine-tuning of the sputter conditions supported by proper equipment.

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