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Solid-State Transformer based on the AC-AC Dual Active Bridge Converter

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Abstract

Transformers are used when galvanically isolated energy transfer, i.e. according to the European standard EN61558, is necessary. Conventional low-frequency transformers (LFTs) are heavy and bulky devices and consist 80 % of copper and iron. Their biggest benefit of high reliability, due to their passive nature and low complexity, is, on the other hand, their drawback, which is the inability of control. With the recent grid developments, integration of decentralized renewable energy sources and the smart grid paradigm as such, the demand for controllability and sustainability is becoming increasingly important. Since the 1960s, the demand for refined copper has increased by 250 % from 5 mil tons to 20 mil tons. Due to the increasingly high demand for copper, a continuous price increase in the next years is expected. To guarantee the availability of copper for the next decades and to counteract the expected price increase, it is essential to find resource friendlier alternatives.

Within this work, a promising alternative to conventional low power (LFTs) operating at 50 Hz or 60 Hz and low voltage is investigated. By increasing the operating frequency of the transformer, utilizing power electronic switching networks, the build volume can drastically be reduced. Compared to a multi-stage power conversion system, the presented one-stage conversion system does not incorporate electrolytic capacitors in the power path. The elimination of electrolytic capacitors makes it possible to create a smaller, lighter and resource friendlier alternative to conventional LFTs, without sacrificing the lifetime and reliability significantly.

Based on the analysis of the possible energy conversion systems, the one-stage conversion system based on the Dual-Active-Bridge (DAB) converter is chosen for high efficiency, single-stage isolated power transfer. In **Chapter 2** the proposed DAB converter operated as an DC-DC converter is analysed in detail. The fundamental working principle and the power transfer is explained using the lossless DAB model. The combined modulation scheme is derived, which utilizes both the conventional phase-shift modulation and the advanced modulation schemes and focuses on minimizing the inductor RMS current and thereby increasing the converter efficiency in the low to medium power regions. The lossless DAB model is extended to consider the static losses of the converter. The analytical description of the inductor current is derived, and the optimal modulation parameters of the combined modulation scheme are updated.

In **Chapter 3** the switching behaviour of a MOSFET is detailed. The effect of

the parasitic components of a MOSFET is explained. The hard and soft switching transitions are presented, and the ZVS constraints of the DAB converter are derived.

The DC-DC DAB converter is extended by bi-directional power electronic switches to enable four-quadrant operation. The principle of operation of the AC-AC DAB converter is explained in **Chapter 4**. The optimal modulation parameters derived in Chapter 2 are updated to cater for the additional conduction losses by the bi-directional switches. The active and reactive power operation of the AC-AC DAB converter is discussed, showing the difficulties of the reactive power operation.

To validate the derived combined modulation scheme and the calculated optimal modulation parameters, a steady-state simulation is conducted in **Chapter 5**. Both the DC-DC and AC-AC versions of the DAB converter are simulated and examined in detail.

In **Chapter 6** the 5 kVA prototype converter is detailed. The schematic overview and the design parameters are shown. The main components are calculated and the magnetic components discussed in detail.

The prototype converter is experimentally verified in **Chapter 7**. The DC-DC DAB converter is modulated with the combined modulation scheme, and the calculated optimal modulation parameters are verified; firstly, on the non-isolated version and after that, the effects of the transformer and resonant voltage transitions are investigated. The transient behaviour of the DAB converter is analysed with the main focus on the switching transitions of the MOSFETs. Silicon carbide as a semiconductor material is introduced, and the benefits of the wide band-gap are explained. The switching losses of a silicon and silicon carbide MOSFET are shown and the switching loss-energy compared. The AC-AC operation of the prototype converter is presented. The active and reactive power operation is detailed, and the drawbacks of the reactive power operation emphasized.

The thesis is summarised in **Chapter 8** and the work is concluded with the outlook and future research.

Kurzfassung

Transformatoren werden eingesetzt, wenn eine galvanisch getrennte Energieübertragung, z.B. laut der europäischen Norm EN61558, von Nöten ist. Konventionelle Niederfrequenz-Transformatoren (LFT) sind schwere und großvolumige Geräte und bestehen zu 80 % aus Kupfer und Eisen. Der größte Vorteil der hohen Zuverlässigkeit, aufgrund ihrer passiven Bauweise und geringen Komplexität, ist auf der Gegenseite ihr Nachteil und zwar ihr Unvermögen ihre Ausgangsgrößen zu steuern. Durch die jüngsten Entwicklungen im Versorgungsnetz, vorangetrieben durch die Notwendigkeit der Integration von erneuerbaren Energiequellen und der Smart Grid Denkweise an sich, wird die Forderung nach Steuerbarkeit und Nachhaltigkeit immer lauter. Seit den 1960er Jahren stieg die Nachfrage nach raffiniertem Kupfer um 250 % von 5 Mio. auf 20 Mio. Tonnen an. Die stetig steigende Nachfrage resultiert in einem prognostizierten Preisanstieg in den nächsten Jahren. Daher ist es notwendig eine ressourcenschonendere Alternative zu konventionellen Niederfrequenz-Transformatoren zu erforschen, um die natürlichen Ressourcen zu schonen und um dem erwarteten Preisanstieg entgegenzuwirken.

Im Rahmen der vorliegenden Arbeit wird eine zukunftsträchtigere Alternative zu einem konventionellen 50 Hz beziehungsweise 60 Hz Niederfrequenz-Transformator untersucht. Durch das erhöhen der Betriebsfrequenz des Transformators, mittels leistungselektronischen Schaltnetzwerken, kann die Baugröße drastisch reduziert werden. Im Vergleich zu mehrstufigen Energieübertragungssystemen zeichnet sich das vorgestellte einstufige Energieübertragungssystem dadurch aus, dass kein Energiespeicher in Form von Elektrolytkondensatoren vorhanden ist. Durch die Eliminierung der Elektrolytkondensatoren ist es möglich eine kleinere, leichtere und umweltfreundlichere Alternative zu Niederfrequenz-Transformatoren zu erschaffen, ohne dass die Lebensdauer und Zuverlässigkeit signifikant reduziert wird.

Aufgrund der Auswertung der aufgeführten Energieübertragungssysteme, verspricht das einstufige System basierend auf dem Dual-Active-Bridge (DAB) Wandler am geeignetsten für effiziente, galvanisch getrennte Energieübertragung zu sein. Im **Kapitel 2** wird der vorgeschlagene DAB Wandler im Detail als DC-DC Wandler beschrieben. Das fundamentale Funktionsprinzip und die Leistungsübertragung werden anhand des verlustlosen DAB Modells erläutert. Ein kombiniertes Modulationsverfahren, welches sowohl das konventionelle Phasen-Verschub-Verfahren als auch die erweiterten Modulationsverfahren verwendet, wird hergeleitet. Dieses befasst sich

mit dem Minimierungsproblem des Drossel-Effektivstroms, wodurch der Wirkungsgrad im geringen und mittleren Leistungsbereich erheblich gesteigert werden kann. Das verlustlose DAB Modell wird erweitert, um zusätzlich die statischen Verluste zu berücksichtigen. Eine analytische Beschreibung des Drosselstroms wird hergeleitet und die optimalen Modulationsparameter des kombinierten Modulationsverfahrens werden abschließend neu errechnet.

Im **Kapitel 3** wird das Schaltverhalten eines MOSFETs beschrieben. Der Einfluss der parasitären Elemente des MOSFETs auf das Schaltverhalten wird erläutert. Das harte sowie das weiche Schalten eines MOSFETs wird beschrieben. Das Kapitel schließt mit der Herleitung der Bedingungen, die weiches Schalten gewährleisten.

Der DC-DC DAB Wandler wird durch bidirektionale Schaltelemente erweitert, um den Vier-Quadranten-Betrieb des Wandlers zu gewährleisten. Das Funktionsprinzip des AC-AC DAB Wandlers wird im **Kaptel 4** beschrieben. Die zuvor hergeleiteten optimalen Modulationsparameter werden aktualisiert. Der Betrieb des AC-AC DAB Wandlers mit reiner Wirkleistungsübertragung und weiterhin mit der Übertragung eines Blindleistungsanteils wird beschrieben und es werden abschließend die Einschränkungen des Blindleistungsbetriebs erläutert.

Im **Kapitel 5** wird eine Simulation im stationären Zustand durchgeführt, um die hergeleiteten optimalen Modulationsparameter zu verifizieren. Es wird sowohl auf den DC-DC Betrieb sowie den AC-AC Betrieb eingegangen.

Kapitel 6 stellt das 5 kVA Demonstrationsgerät vor. Die Eckdaten und das Blockschaltbild des Geräts werden präsentiert. Die Hauptkomponenten werden berechnet und mit der Beschreibung der magnetischen Bauteile im Detail abgeschlossen.

Die Messergebnisse, die anhand des Demonstrationsgeräts aufgenommen wurden, werden im **Kapitel 7** vorgestellt. Der DC-DC DAB Wandler wird mit dem kombinierten Modulationsverfahren angesteuert und die berechneten optimalen Modulationsparameter werden verifiziert. Zuerst anhand der galvanisch nicht getrennten Version und danach wird der Einfluss des Transformators und der resonanten Umschwingvorgänge untersucht. Das transiente Verhalten des Wandlers wird beschrieben, wobei der Schwerpunkt auf die Schaltvorgänge der MOSFETs gelegt wird. Silikoncarbid wird als alternatives Halbleitermaterial vorgestellt und die Vorteile der breiten Bandlücke beschrieben. Die Schaltverluste eines Silikon und eines Silikoncarbid MOSFETs werden aufgeführt und die Schalt-Verlustenergie miteinander verglichen. Das Kapitel schließt mit der Beschreibung des AC-AC Betriebs des Demonstrationsgeräts, wobei die Ergebnisse der reinen Wirkleistungsübertragung sowie der Betrieb mit Blindleistungsanteil vorgestellt und beschrieben werden. Es wird schlussfolgernd auf die Problematik der Blindleistungsübertragung eingegangen.

Die vorliegende Arbeit wird im **Kapitel 8** zusammengefasst und mit dem Ausblick und den weiterführenden Arbeiten abgeschlossen.

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1. Introduction

1.1. Electronic Transformer

Transformers are used when voltage scaled, galvanically isolated energy transfer, i.e. according to the European standard EN61558, is necessary. Conventional low-frequency transformers (LFTs) are bulky and heavy devices [1], owing to their low operating frequency of 50 Hz or 60 Hz, depending on the grid frequency. Their benefit of high reliability, due to their passive nature and low complexity, is, on the other hand, their downside, which is the inability of control. The demand for controllability and sustainability is becoming increasingly important in recent grid developments, as renewable distributed power generation systems have to be integrated. Furthermore, controllability is the key requirement of a Smart Grid in general [1] [2] [3].

With controllability being one of the inherent features of power electronic converters, the logical step is to replace LFTs by Solid-State Transformers (SSTs) [1]. SSTs are also known as Electronic Transformers, Power Electronic Transformers, Smart Transformers or Energy Routers in literature [2], where the galvanic isolation is achieved by a medium-frequency transformer (MFT) interfaced by power electronic circuits on the primary and the secondary side. By the significantly increased operating frequency of the transformer, the size and weight are drastically reduced. Furthermore, by the reduction of size, the amount of needed natural resources is decreased.

The first concept of an AC-AC conversion system with isolated power flow was patented by McMurray [4] in 1971. The circuit consists of two bidirectional switches connected to a single-phase grid and feeding a centre tapped transformer on the primary side. The secondary side consists of a similar structure with an inductor and capacitor on the output. By switching the two bidirectional switches in complementary mode and creating a phase-shift between the primary and secondary switch pairs, a sinusoidal current flow is generated. It should be noted that the operation is similar to the Dual-Active-Bridge (DAB) converter later presented by de Doncker [5] in 1991. However, due to the low power rating and low switching speed of semiconductors available, the SST technology could not be implemented in energy conversion systems by that time [6].

The first real considerations though, to replace conventional LFTs by SSTs, were starting to emerge in the early 2000s [2] and were mainly motivated by the reduction in volume and weight for traction applications [7] [8] [9] [10]. Since the allowable weight and volume of traction transformers is limited, these tend to be quite inefficient to achieve the desired power densities [2]. SSTs offer the possibility to reduce the volume and weight by the added degree of freedom of the operating frequency of the transformer. By the introduction of power electronics, the overall efficiency of SSTs can furthermore be increased compared to conventional traction LFTs [10].

With the first endeavours of building smart grids in the early 2000s, SSTs were furthermore considered in the distribution system due to their smart features enabled by their added degrees of controllability [2]. These include voltage regulation, smart protection, VAR compensation, power-factor control and frequency regulation [11] [12] [13] [14] [15]. Up to date, several research projects are or have been dedicated to SSTs in smart grid applications, and several technical feasibilities have been shown.

1.2. Energy Conversion Systems

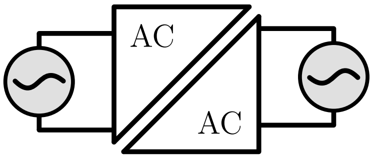
One of the main advantages of SSTs is the increased operating frequency of the transformer, whereby the volume and weight are reduced. The relation between the operating frequency and the overall build volume of a transformer can be approximated by [16]

$$A_w \, A_c \propto \frac{S}{B_m \, f \, j} \tag{1.1}$$

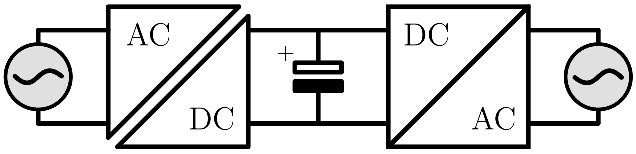
where S to the apparent output power, B_m to the maximum flux density, f to the operating frequency, j to the current density, A_w to the window area and A_c to the core area refers. It should be noted that (1.1) only refers to be build volume of the transformer itself and does not consider the additional power electronic components present in a SST.

The isolated energy transfer of SSTs can be accomplished over different conversion stages, ranging from one to three. The possible power conversion systems are depicted in Figure 1.1. Figure 1.1a shows the one-stage or direct AC-AC conversion, where the energy is directly transferred from the input to the output without energy being stored along the power path. The two-stage power conversion system is depicted in Figure 1.1b, consisting of an AC-DC and a DC-AC converter interfaced by an energy storage. Lastly, the three-stage conversion system consisting of an AC-DC, a DC-DC and lastly a DC-AC converter, each converter interfaced by an energy storage, is depicted in Figure 1.1c.

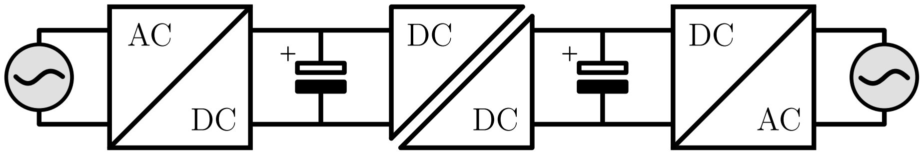
In Sections 1.2.1 to 1.2.3 the different energy conversion systems are studied in detail. In general, it can be noted that with an increase in conversion stages, the number of components, the complexity of the system and the degrees of freedom increase. Therefore by the increased number of components and complexity, the efficiency and the reliability decreases, but the degrees of controllability increase. A trade-off between reliability and controllability exists, and therefore the benefits and drawbacks of each conversion system should be weighed off for the respective fields of application.



(a) One-stage power conversion system



(b) Two-stage power conversion system



(c) Three-stage power conversion system

Fig. 1.1.: Possible power conversion systems

1.2.1. One-stage energy conversion

The one-stage AC-AC energy conversion is characterised by a direct energy conversion without any energy stored along the power path. The system incorporates the lowest number of components, which results in the highest reliability and efficiency of the three possible energy conversion systems. Due to no energy storage being present (in the form of electrolytic capacitors), the lifetime is the longest.

AC-AC Full-Bridge Converter

An AC-AC converter that is based on the full-bridge phase-shift converter is presented in [12]. The two half-bridges on the input are modulated in complementary mode generating a high-frequency square wave that is passed on to the transformer. On the secondary side, the square wave is then rectified with a full-bridge synchronous rectifier. The power transferred can be controlled by adjusting the duty-cycle of the generated square wave. Low switching losses result in a high converter efficiency, however, as with the DC-DC phase-shift converter, a relatively large input and output filter inductor has to be foreseen. This leads to a decreased power density and affects the input power factor [17].

AC-AC DAB Converter

The first direct AC-AC converter based on the DAB converter was presented in [18] and was later verified by a prototype converter in [19]. The converter consists of two full-bridges where the switches are replaced by bidirectional switches making it possible to be connected to alternating voltages. The input and output full-bridges are modulated with a 50 % duty-cycle and a power transfer can be generated by introducing a phase-shift from the secondary to the primary bridge. Compared to a phase-shift converter the filter inductors are not necessary. Furthermore, the DAB is a resonant topology and thus has the ability to ensure zero-voltage-switching (ZVS) on all power electronic switches. The ZVS range can furthermore be extended over the whole operating range with the implementation of advanced modulation schemes by additionally changing the duty-cycle of the full-bridges itself. These are discussed in [20] [21] [22] [23]. The advantage of the AC-AC DAB converter is a high efficiency, a low number of passive components, and three possible control parameters to influence the power flow.

Dyna-C Converter

In [24] a concept of a SST based on a dynamic-current (Dyna-C) topology is presented. The converter consists of two current-source converters interfaced by a MFT. The converter has voltage regulation capability and the input and output can have different frequencies and power factors. The topology is a new breed of isolated power converters [24] and is thus not widely explored.

1.2.2. Two-stage energy conversion

The two-stage conversion is based on an AC-DC isolated converter and a grid forming inverter interfaced by electrolytic capacitors. The main advantage is that by introducing an energy storage, the input and output of the total conversion system are decoupled and thus can be regulated independently. This allows grid stabilising functions on the input regardless of the load connected on the output. Furthermore, in modern smart grid applications, the presence of a low voltage (LV) DC bus is essential, especially for the integration of renewable energies [3]. Only the AC-DC converter is discussed in further detail as the inverter does not form part of this work as has been studied thoroughly in the literature.

The first isolated DC-AC converter based on a DAB converter was presented in

[25]. Although the derivations are for a DC-AC converter, these can directly be applied for AC-DC conversion, due to the symmetry of the DAB converter and the seamless bidirectional power flow. The power flow is controlled by phase-shifting the secondary to the primary 50 % modulated full-bridge. As the input voltage alternates the phase-shift modulation alone only allows ZVS for a limited operating range. By introducing an additional phase-shift in the full-bridge connected to the DC side, the ZVS range can be extended [25] [26] [27]. [28] furthermore varies the switching frequency and thereby achieves ZVS over the whole operating range.

It is apparent that the number of active switches does not increase in the two-staged topology. The main advantage of decoupling the input from the output (by introducing an energy storage) increases the number of passive components and decreases the reliability and lifetime. Furthermore, the control of the AC-DC converter is challenging, as the operating point is changing with the alternating input voltage. Thus the control parameters are non-linear and by furthermore varying the switching frequency increases the electromagnetic interference (EMI) [25] [28].

1.2.3. Three-stage energy conversion

At present, it is possible to replace LFTs by a three-stage energy conversion system, as all three stages are state of the art and commercially available. The system can be described by an active power-factor correction (PFC) and a grid forming inverter interfaced by a DC-DC converter for galvanic isolation. The first two stages form a bidirectional grid-connected battery charger, which is one of the main components of a smart home coupled with an electric powered vehicle.

As PFCs and grid forming inverters are commercially available until power ratings of 8 kVA [29], the key element of the three-staged SST is the DC-DC converter, as it is responsible for the galvanic isolation and the voltage scaling [16]. To overcome the conversion efficiency challenge of SSTs [2], resonant converters are the recommended choice, as they offer the highest conversion efficiency with galvanic isolation. The DAB converter [30] [31], LLC converter [32] [10] [9] and series resonant converter (SRC) [8] are the most common implemented converters in research projects. For bidirectional power flow, the DAB converter is best suited due to its symmetry [20]. Furthermore, the three possible control parameters allow high efficient power conversion over the whole operating range [20] [33] [34] [35] [36] [23].

The disadvantage of a three-stage system is the increased number of passive components making the topology more prone to failure and thus decreasing the reliability, efficiency and lifetime even further. The main advantage though is the proven technology of each of the individual converters and the further added degrees of freedom, as all three stages are decoupled and can be controlled separately.

1.3. Conclusion

The motivations of replacing LFTs by SSTs are discussed, and the possible energy conversion systems are introduced. SSTs have the great advantage to reduce the overall weight and volume compared to a LFT by the significantly increased operating frequency of the transformer (MFT). This is of great advantage in traction systems, where weight has a direct impact on the efficiency of the system. The decreased build size enables a resource friendlier product, as the amount of necessary natural resources is greatly reduced. The amount of winding material and core material decreases, and the iron core (LFT) is moreover replaced by ferrite material (MFT). Also, the necessity of oil as a coolant is eliminated completely. By the introduction of semiconductor devices, smart features and smart protection can be enabled. For a single-stage conversion system voltage regulation, current limitation, smart short circuit protection and ramping of the inrush current can be implemented. Further advantageous can be utilised, when the input and the output are decoupled by a two- or three-staged conversion system. These are frequency regulation, power-factor correction and VAR compensation.

The downside of SSTs, though is the decreased reliability and lifetime by the increased number of active and passive components. With the introduction of an energy storage in two- and three-stage systems, the lifetime and reliability are decreased even further. Furthermore, at the current point of time, the benefits of a SST come at a higher price tag [1]. Further, the high number of passive components in a three-stage system increase the costs even further. No low-power single-phase SSTs being of a two-stage of three-stage conversion system have been published to date. Only Qin et al [18] presented a one-stage low power single-phase SST in 2009 based on the DAB converter. In 2017 Chen et al [24] presented a SST based on the Dyna-C topology, but is not widely explored.

Three-stage three-phase distribution and traction SSTs have been studied in detail, and even a prototype traction SSTs has been mounted on an actual locomotive [10]. With the smart grid paradigm as such the research on SST (with grid stabilising capabilities only) will continue to increase, as a drastic price decrease of semiconductor technology is expected. Especially wide-bandgap semiconductors, allowing higher switching frequencies and increased voltage blocking capabilities, are a promising aspect in the increase of power density and decrease in overall cost.

1.4. Aim of Work and Content

To create a smaller, lighter and resource friendlier alternative to a single-phase low power LFT without decreasing the lifetime drastically, a one staged AC-AC converter based on a DAB converter is investigated in the course of this work. The converter is directly connected to the grid and produces an alternating voltage without storing any energy along the path. Consequently, the one-stage system eliminates the need for electrolytic capacitors increasing the lifetime compared to the two- or three-staged conversion system.

Chapter 2 introduces the proposed converter topology and explains the fundamental working principle and power transfer of a DC-DC DAB converter. This includes the possible modulation schemes that produce the power flow of the converter. Additional to the conventional phase-shift modulation, the advanced modulation schemes are introduced. An optimal combined modulation scheme is derived from the lossless DAB model. Thereafter the DAB model is extended to consider the conduction losses additionally. It is shown that the combined modulation scheme minimises the transformer RMS current and that the zero-voltage switching (ZVS) range is extended.

The switching behaviour of a MOSFET is described in **Chapter 3**, which includes the MOSFET's switching transient and switching losses. The first discusses the reverse recovery of the intrinsic diode, and the latter describes the hard and soft switching transitions of the MOSFET. Lastly, the ZVS constraints for the DAB converter are derived for different power levels and voltage ratios.

In **Chapter 4** the DC-DC DAB converter is extended by bi-directional switches to enable four-quadrant operation. The principle of AC-AC operation is characterised, and the modulation schemes introduced in Chapter 2 are detailed for the lossless DAB model. After that, the ideal parameters of the combined modulation scheme for the model considering conduction losses are derived. The operation of an AC-AC is described in detail discussing the active and reactive power operation.

The steady-state simulation of firstly the DC-DC DAB converter and after that, the AC-AC DAB converter is detailed in **Chapter 5**. The ideal parameters of the combined modulation scheme derived in Chapter 2 are verified and compared to the conventional phase-shift modulation. The reduction in inductor RMS current and enhancement of converter efficiency are shown. In a final step, the reactive power operation is simulated, and the problems of such operation emphasised.

The 5 kVA prototype DAB converter is described in **Chapter 6**, where firstly the design parameters of the proposed AC-AC DAB converter are listed and the schematic overview is shown. After that, the main components are calculated, and lastly, the magnetic components are discussed in detail.

In **Chapter 7** the prototype converter is experimentally verified. The converter is operated as a DC-DC converter first to verify the derived optimal parameters of the combined modulation scheme. Results of a non-isolated and an isolated version are presented, and the results are compared to the theoretical calculations and the steady-state simulation conducted in Chapter 5, where the transformer RMS current and the converter efficiency are listed. The transient behaviour of the DAB converter is analysed with the main focus on the switching transitions of the MOSFETs. The switching losses of a silicon-based MOSFET and a silicon carbide MOSFET are shown, and the turn-on and turn-off loss-energies are compared. After that, the AC-AC operation of the prototype converter is presented, and the active power operation is shown first, followed by the reactive power operation.

Chapter 8 summarises the thesis and the work is concluded with the outlook and future research.

2. Dual Active Bridge (DAB) Converter

The Dual Active Bridge (DAB) converter consists of two active switching networks interfaced by a reactive network consisting of a coupling inductor L_c and a medium frequency (MF) transformer. The circuit diagram of a DC-DC DAB converter is depicted in Figure 2.1.

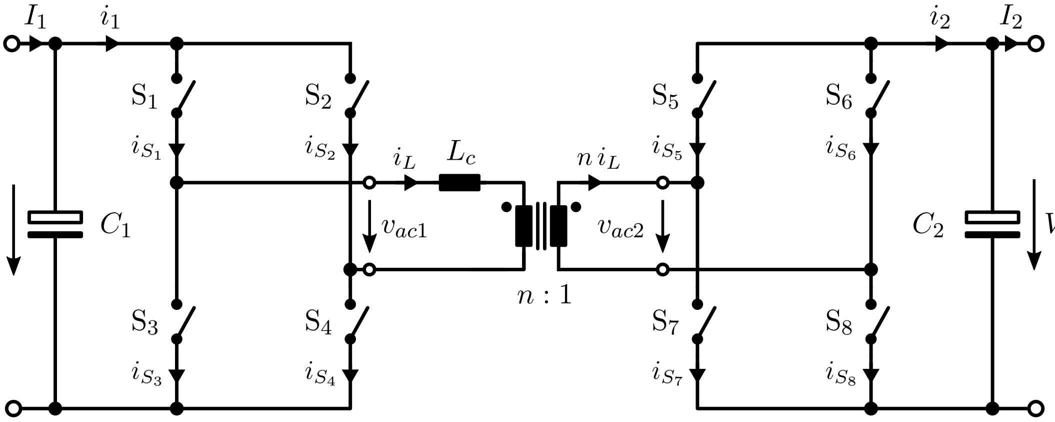


Fig. 2.1.: DC-DC Dual Active Bridge (DAB) converter with ideal switches S_1 - S_8

Each switching network consists of a full-bridge applying an AC voltage (v_{ac1} and v_{ac2}) to the reactive network. The primary referred equivalent circuit of the reactive network is shown in Figure 2.2. The network consists of the coupling inductor L_c, the winding resistances R_1, R_2, the stray inductances $L_{\sigma 1}, L_{\sigma 2}$ and the magnetizing inductance L_M. The primary transformer current i_L is defined as

$$i_L = i_M - i^{'}_{ac2} \tag{2.1}$$

If it is assumed, that the magnetizing inductance is much greater than the stray inductance ($L_M >> L_\sigma$), then the magnetizing current is much smaller than primary inductor current ($i_M << i_L$) and Equation (2.1) results in

$$i_L \approx -i^{'}_{ac2} \tag{2.2}$$

If furthermore all losses are neglected, the winding resistances are no longer present and the reactive network in Figure 2.2 can be replaced by an equivalent inductance according to:

$$L_{eq} = L_c + L_{\sigma 1} + L_{\sigma 2} \tag{2.3}$$

The lossless DAB converter can finally be described by two voltage sources interfaced by the total inductance of the reactive network. The resulting simplified equivalent circuit diagram of a DAB converter is depicted in Figure 2.3.

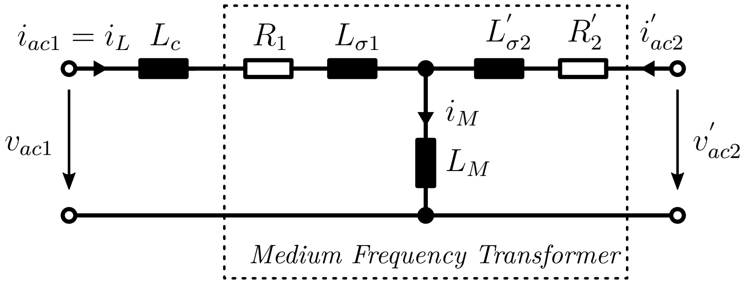


Fig. 2.2.: Primary-referred equivalent circuit of the reactive MF network

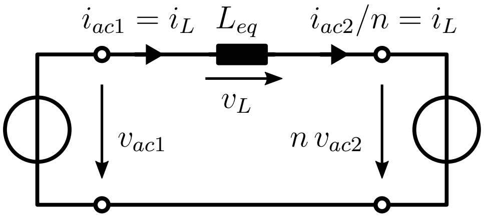


Fig. 2.3.: Primary-referred lossless equivalent circuit of a DAB converter

2.1. Working Principle and Power Transfer

The physical operating principle of the DAB converter can best be described by taking a closer look at the lossless equivalent circuit diagram shown in Figure 2.3. In order to transfer power, a time-varying inductor current has to be generated by applying a time-varying voltage across the inductor:

$$v_L(t) = v_{ac1}(t) - n\, v_{ac2}(t) \tag{2.4}$$

If the two voltages v_{ac1} and $n\, v_{ac2}$ are identical, no current can flow, and thus no power flow is possible. To generate a power flow, the two bridge voltages have to be different. This is achieved by introducing modulation parameters that either change the phase or the shape of the voltages v_{ac1} and v_{ac2}. The possible modulation parameters are depicted in Table 2.1 and the resulting voltage waveforms are presented in Figure 2.4. The current waveform can be manipulated by either shifting the voltage v_{ac2} in relation to v_{ac1} by a time interval $g\, T_s$ or by clamping the primary bridge voltage to zero for a

Tab. 2.1.: Possible modulation parameters

normalised phase shift between v_{ac1} and v_{ac2}	g
normalised zero voltage clamping interval of v_{ac1}	w_1
normalised zero voltage clamping interval of v_{ac2}	w_2
switching frequency	$f_s = {}^1\!/_{T_s}$

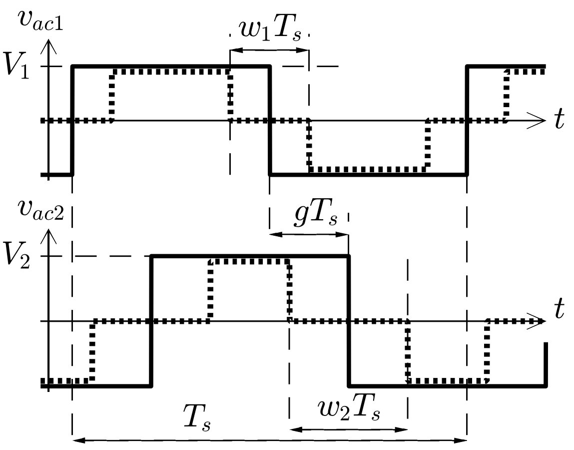


Fig. 2.4.: Possible voltage waveforms v_{ac1} and v_{ac2} depending on modulation parameters g, w_1 and w_2 and $f_s = const.$

time interval $w_1\,T_s$ or the secondary bridge by $w_2\,T_s$ respectively. Additionally, the current can be influenced by changing the period T_s.

Due to the switching networks being full-bridges, four switching states are possible generating three different voltage levels. The switching states and the resulting voltage level for the bridge voltage $v_{ac1}(t)$ are listed in Table 2.2. S_1 through S_4 are referred to the power switches given in Figure 2.1. The secondary bridge voltage $v_{ac2}(t)$ equals to $-V_2$, 0 or $+V_2$, which is generated by commutating the power semiconductors S_5 to S_8 correspondingly.

Depending on the modulation parameters mentioned in Table 2.1 the generated inductor current can be described by

$$\begin{aligned} i_L(t) &= i_L(t_0) + \frac{1}{L_{eq}} \int_{t_0}^{t_1} v_L(t)\,\mathrm{d}t \\ &= i_L(t_0) + \frac{1}{L_{eq}} \int_{t_0}^{t_1} (v_{ac1}(t) - n\,v_{ac2}(t))\,\mathrm{d}t \end{aligned} \tag{2.5}$$

Tab. 2.2.: Possible switching states and corresponding voltage levels for $v_1(t)$

State	S_1	S_2	S_3	S_4	$v_{ac1}(t)$
I	1	0	0	1	$+V_1$
II	1	1	0	0	0
III	0	0	1	1	0
IV	0	1	1	0	$-V_1$

with

$$\begin{aligned} v_{ac1}(t) &= \text{const.} \\ v_{ac2}(t) &= \text{const.} \end{aligned} \quad \text{with} \quad t \in [t_0, t_1] \tag{2.6}$$

The instantaneous power is given by:

$$\begin{aligned} p_1(t) &= v_{ac1}(t)\, i_L(t) \\ p_2(t) &= n\, v_{ac2}(t)\, i_L(t) \end{aligned} \tag{2.7}$$

The average transferable power can lastly be calculated by averaging the instantaneous power given in (2.7) over one switching period T_s

$$\begin{aligned} P_1 &= \frac{1}{T_s} \int_{t_0}^{t_0+T_s} p_1(t)\, \mathrm{d}t \\ P_2 &= \frac{1}{T_s} \int_{t_0}^{t_0+T_s} p_2(t)\, \mathrm{d}t \end{aligned} \tag{2.8}$$

with P_1 referring to the primary side and P_2 to the secondary side respectively.

As the bridge voltages v_{ac1} and v_{ac2} being rectangular shaped waveforms with the three possible voltage levels listed in Table 2.2, the inductor current will result, according to (2.5), in a piecewise linear waveform. For simplicity one switching cycle, $t_0 \leq t < (t_0 + T_s)$, is split into n different time intervals in which the voltage applied across the inductor is constant. The resulting inductor current will consequently be a straight line with a constant slope. The total average power of a DAB converter can therefore be calculated by the sum of each time interval's average power. The only time dependant variable remains the inductor current, thus (2.8) results in:

$$\begin{aligned}P = P_1 = P_2 &= \frac{1}{T_s}\int_{t_0}^{t_0+T_s} p_1(t)\,\mathrm{d}t\\ &= \frac{1}{T_s}\left(V_{L0}\int_{t_0}^{t_1}\left(i_L(t_0)+\frac{V_{L0}}{L}\,t\right)\mathrm{d}t + ...\right.\\ &\left.+V_{L(n-1)}\int_{t_{n-1}}^{t_n}\left(i_{L(n-1)}+\frac{V_{L(n-1)}}{L}\,t\right)\mathrm{d}t\right)\end{aligned} \tag{2.9}$$

where $t_n = t_0 + T_s$.

2.2. Modulation Schemes

2.2.1. Phase Shift Modulation

The most straightforward modulation scheme is the phase-shift modulation (PSM), which was first discussed in [37]. In this modulation scheme the generated waveforms v_{ac1} and v_{ac2} are square wave voltages with a 50% duty-cycle, a constant time period T_s and the amplitudes V_1 and V_2 respectively. The power transfer is solely generated by introducing a phase-shift g between the two bridge voltages v_{ac1} and v_{ac2}. The possible modulation parameters listed in Table 2.1 can thus be simplified and it holds:

$$\begin{aligned}w_1 &= 0\\ w_2 &= 0\\ f_s &= \text{const.}\end{aligned} \tag{2.10}$$

The steady-state waveforms of bridge voltages and inductor current are shown in Figure 2.5. For deriving an analytical description of the current and the transferred power of a lossless DAB converter, the voltage transitions are assumed to be instantaneous.

The steady-state operation of the DAB converter modulated with phase-shift can be split into four time intervals denoted as Regions I-IV in Figure 2.5. During each time interval, the bridge voltages are constant, and therefore the inductor current changes with a constant slope.

Furthermore it is noticeable, that the waveforms of the reactive network repeat themselves each half switching period ($T_s/2$) with negative sign and it holds

$$\begin{aligned}i_L(t) &= -i_L(t+T_s/2)\\ v_{ac1}(t) &= -v_{ac1}(t+T_s/2)\\ v_{ac2}(t) &= -v_{ac2}(t+T_s/2)\end{aligned} \tag{2.11}$$

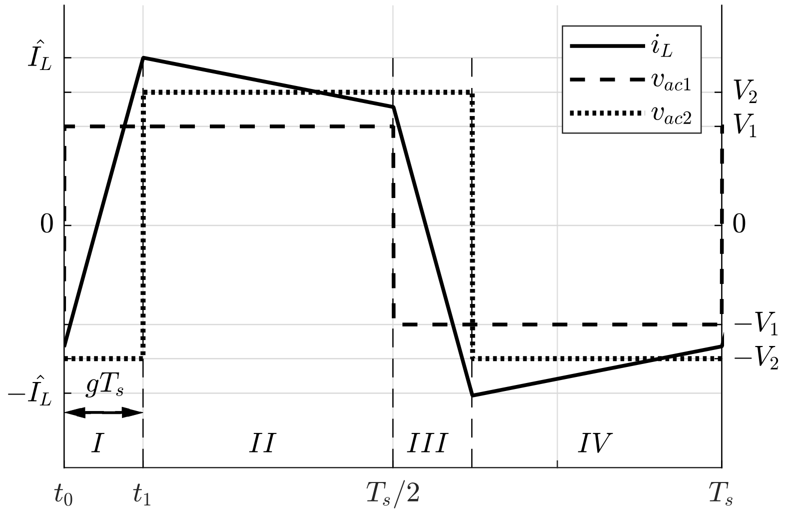


Fig. 2.5.: Steady-state bridge voltages v_{ac1} and v_{ac2} and inductor current i_L with phase-shift modulation

and therefore due to half-cycle symmetry only half of the switching period ($T_s/2$) is considered for calculating the power transfer. Equation (2.8) is thus simplified with $t_0 = 0$ to

$$P_1 = \frac{1}{T_s}\int_0^{T_s} p_1(t)\,\mathrm{d}t = \frac{2}{T_s}\int_0^{T_s/2} v_{ac1}(t)\,i_L(t)\,\mathrm{d}t = \frac{2\,V_1}{T_s}\int_0^{T_s/2} i_L(t)\,\mathrm{d}t \tag{2.12}$$

In order to obtain an analytical expression for the transferred power the inductor current has to be described. Due to half-cycle symmetry only regions I and II are relevant to fully describe $i_L(t)$. Furthermore an initial current $i_L(t_0) = i_{L0}$ is assumed and it holds for Region I:

$$i_L(t) = i_{L0} + \frac{V_1 + n\,V_2}{L}\,t, \qquad \forall \quad t \in [t_0; t_1] \tag{2.13}$$

and for Region II:

$$i_L(t) = i_L(t_1) + \frac{V_1 - n\,V_2}{L}\,(t - t_1), \qquad \forall \quad t \in [t_1; t_2] \tag{2.14}$$

By inserting $i_L(t_1)$ with $t_1 = g\,T_s$ and $i_L(T_s/2) = -i_0$ into Equation (2.14) the expression for the initial current is given by

$$i_{L0,PS} = \frac{n\,V_2\,(1 - 4\,g) - V_1}{4\,f_s\,L} \tag{2.15}$$

Furthermore the inductor current at $t_1 = g\,T_s$ is given by:

$$i_{L,PS}(t_1) = \frac{V_1\,(4\,g - 1) + n\,V_2}{4\,f_s\,L} \tag{2.16}$$

Lastly the expression for the transferred power with phase-shift modulation results with (2.9), (2.15) and (2.16) in

$$P_{PS} = \frac{n\,V_1\,V_2\,g\,(1-2\,|g|)}{f_s\,L} \tag{2.17}$$

with the voltage ratio d

$$d = \frac{n\,V_2}{V_1} \tag{2.18}$$

where $d > 0$ boost and $d < 0$ buck operation represents.

The transferable power of a lossless DAB converter is depicted in Figure 2.6. It is apparent, that the power flow in positive and negative direction is symmetric and that a maximum power transfer occurs. The maximum transferable power is determined by solving $\partial P_{PS}/\partial g = 0$ for g and inserting g into (2.17), which results in:

$$|P_{PS,max}| = \frac{n\,V_1\,V_2}{8\,f_s\,L}, \qquad \text{for} \quad g = \pm 0.25 \tag{2.19}$$

It is apparent, that the transferable power is inversely proportional to the switching frequency f_s and to the inductor L. With the switching frequency kept constant, an upper limit for the inductor exists with respect to a defined maximum power transfer capability $P_{PS,max}$:

$$L_{PS,max} \leq \frac{n\,V_1\,V_2}{8\,f_s\,|P_{PS,max}|} \tag{2.20}$$

By rearranging (2.17) the phase shift can be derived to transfer a desired power level:

$$g = \frac{1}{4}\left(1 \pm \sqrt{1 - \frac{8\,f_s\,L\,|P|}{n\,V_1\,V_2}}\right), \qquad \text{with} \quad |P| \leq P_{PS,max} \tag{2.21}$$

Zero-Voltage-Switching Constraints

To permit zero-voltage-switching, the primary and secondary full-bridges have to be operated under forced commutation [1]. Thereby the current path is interrupted

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[1] Forced commutation implies a positive current flow through the MOSFET channel (reverse biasing the intrinsic body diode) at turn-off. The current is therefore forced to commutate off the conducting channel and into the complementary device of the half-bridge (body diode). This implies a positive current-flow (with respect to the anti-parallel body-diode) through the channel of the conducting MOSFET at turn-off.

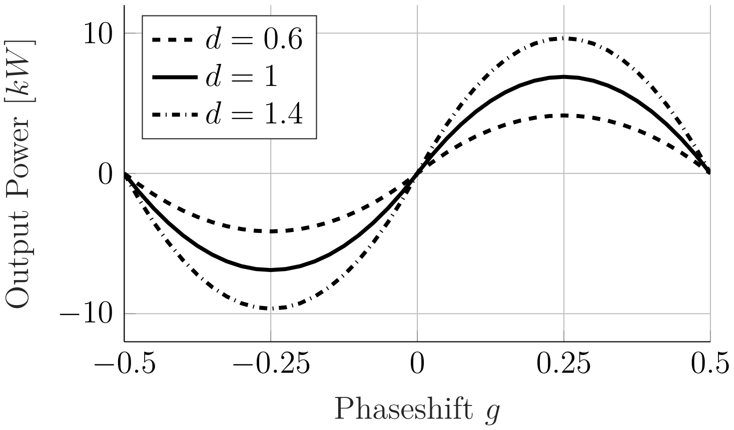


Fig. 2.6.: Transferable output power at $V_1 = 230\,\mathrm{V}$, $L = 24\,\mu\mathrm{H}$, $f_s = 40\,\mathrm{kHz}$ and with voltage ratio d as parameter

and the current commutates to the complementary device of the half-bridge. It is assumed that the switching transitions are instantaneous and that the anti-parallel intrinsic body diode is ideal (no reverse recovery). The constraints for an ideal DAB converter defining the zero-voltage-switching boundaries for the primary full-bridge are defined as

$$i_L(t_0) < 0 \tag{2.22}$$

and

$$i_L(t_1) > 0 \tag{2.23}$$

for the secondary full-bridge respectively.

In order to analyse the commutation of the power electronic switches two different cases have to be independently analysed for $d < 0$ and for $d > 0$ respectively. Figure 2.7 depicts the two possible cases for $d > 0$. It is evident that a situation occurs when the inductor current changes its sign during Region II (Figure 2.7b). The slope of the inductor current during Region II is defined as:

$$\frac{\Delta i}{\Delta t} = \frac{1}{L_{eq}} \left(v_{ac1} - v_{ac2}\right) \tag{2.24}$$

If the inductor current does not change its sign during Region II (Figure 2.7a) the ZVS constraints (2.22) and (2.23) are satisfied and ZVS is ensured on both full-bridge circuits producing only turn-off losses. When on the other hand the current changes its sign (Figure 2.7b), constraint (2.22) is violated and ZVS is lost on the primary full-bridge producing turn-on and turn-off losses. The boundary condition where i_L

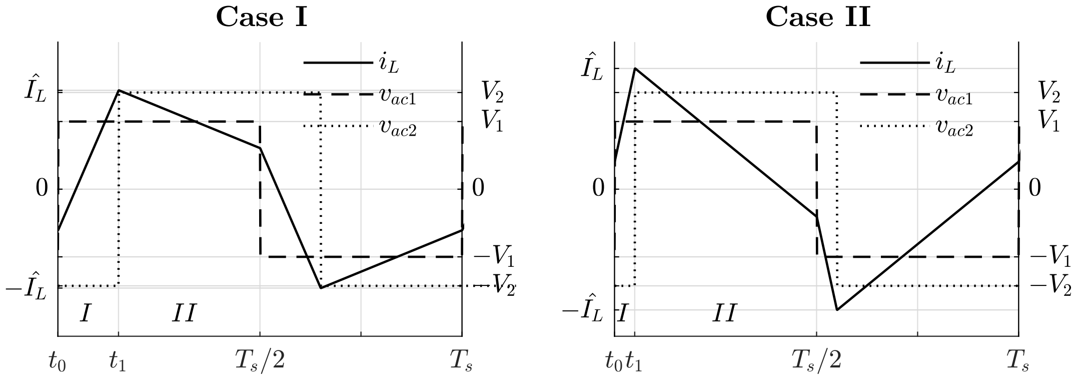
passes through zero is given by:

$$g = \frac{1}{4}\left(1 - \frac{V_1}{V_2}\right), \qquad \text{for} \quad d > 0 \tag{2.25}$$

Considering the two cases for $d < 0$ leads to the boundary condition for the secondary full-bridge:

$$g = \frac{1}{4}\left(1 - \frac{V_2}{V_1}\right), \qquad \text{for} \quad d < 0 \tag{2.26}$$

Figure 2.8 shows the transferred power as a function of phase-shift g with the voltage ratio d as parameter. The boundaries enclosing the ZVS region for the primary and secondary bridge are shown. It can be seen that for $d = 1$ ZVS can be achieved over the whole operation range with $g \in [0; 0.25]$ giving control from zero to full power. Furthermore is is evident, that the ZVS Constraints depend on the voltage ratio and on the transferred power ($i_L(t) = f(d, P)$). Violating Constraint (2.22) or (2.23) leads to natural commutation [2], which results in a loss of ZVS.



(a) $i_L(t_0) < 0 \;\wedge\; i_L(t_1) > 0$ (b) $i_L(t_0) > 0 \;\wedge\; i_L(t_1) > 0$

Fig. 2.7.: Possible current situations with $d > 0$

Figure 2.9 shows the inductor RMS current in relation to the voltage ratio $1/d$ and the transferred power as a parameter. It is evident that the inductor RMS current increases when the difference in voltages increases.

The advantage of the phase-shift modulation is that only one control parameter (cf. (2.17)), the phase shift interval g, has to be adjusted to control a desired output power according to (2.21). Further the phase-shift modulation yields the highest

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[2] Natural commutation implies that the current through the MOSFET channel changes its sign and naturally commutates into the intrinsic body diode of the MOSFET. A turn-off of the MOSFET therefore cannot change the direction of the current flow as the body diode is forward biased.

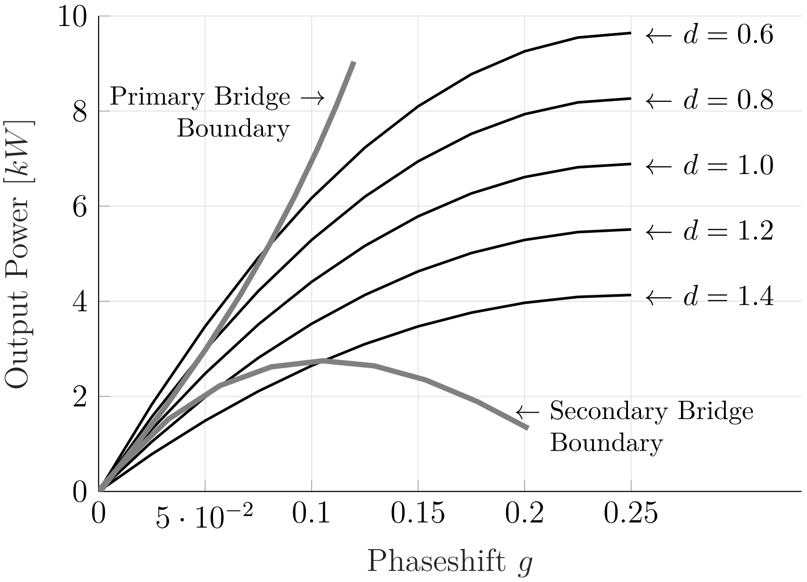


Fig. 2.8.: Transferable output power at $V_1 = 230\,\mathrm{V}$, $L = 24\,\mu\mathrm{H}$, $f_s = 40\,\mathrm{kHz}$ and with voltage ratio d as parameter. Boundaries enclosing the ZVS region for the primary and secondary bridge are shown

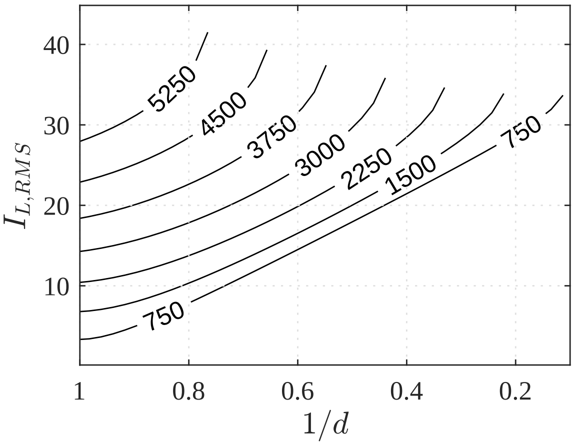


Fig. 2.9.: Inductor RMS current in relation to $1/d$ and the output power as parameter

power transfer possible with the DAB topology. Due to the bridge voltages being rectangular shaped waveforms, the voltages v_{ac1} and v_{ac2} can be generated by using half-bridge circuits. Furthermore zero-voltage-switching (ZVS) is possible on all power electronic switches, if condition

$$V_1 = n\,V_2 \tag{2.27}$$

is satisfied.

The main drawback of the phase-shift modulation is that the inductor current can not be influenced. With the assumption that the switching frequency is kept constant, the only way to influence the inductor current is by changing the turns ratio n or the coupling inductor L_c. Since this is not possible, as these are hardware components, the current shape is solely defined by the input and output voltages (V_1 and V_2) and the phase shift g. Therefore steep slopes of the inductor current in region II and IV will occur if the input voltage differs from the primary referred output voltage and condition (2.27) is violated. This leads to high transformer RMS currents (cf. Figure 2.9) and the loss of ZVS on one bridge depending on d (cf. Figure 2.8). This ultimately results in high losses and poor light-load efficiency.

2.2.2. Advanced Modulation Schemes

The high losses of a phase-shift modulated DAB converter when the input and the primary referred output voltage vary give reason to investigate more advanced modulation schemes, where the additional modulation parameters listed in Table 2.1 are exploited. Thereby the inductor current can be manipulated to achieve the following:

- Minimise switching losses by guaranteeing ZVS under light-load operation and wide input voltage range
- Reduce the RMS currents to minimise conduction losses

Different approaches are presented to improve the operation of a DAB converter. The first investigations to boost the efficiency in light-load, wide input voltage range operations are described in [25]. The proposed modulation scheme extends the ZVS range by utilising one additional modulation parameter $w_1 \in [0; 0.5] \wedge w_2 = 0$ or $w_1 = 0 \wedge w_2 \in [0; 0.5]$ depending on the voltage ratio d and the direction of the power flow.

Modulation schemes employing both clamping intervals $w_1 \in [0, 0.5]$ and $w_2 \in [0, 0.5]$ simultaneously are presented in [38],[39],[22],[20]. The solution of the resulting problem with one added degree of freedom is significantly more complex with regard to maximum efficiency [22]. Therefore a more intuitive approach in [38],[39] is chosen to determine w_1 and w_2, where the shape of the inductor current is defined to follow a trapezoidal or triangular waveform and w_1 and w_2 are calculated accordingly. [38] focuses on satisfying the conditions to warrant zero-current-switching (ZCS). Still, high turn-on losses are generated by the discharge of the output capacitance of the complementary device in the half-bridge. [20] thus extends the trapezoidal or triangular-shaped inductor current to warrant ZVS, but at a greatly increased complexity.

In [21],[23] efficiency enhancements are reported by combining phase-shift modulation and trapezoidal and triangular current modulation depending on the current operating point.

A combined phase-shift and frequency modulation on a prototype power factor correction (PFC) is described in [40]. Additionally to the modulation parameters w_1 and w_2 the switching frequency f_s of the converter is modulated. Due to the complexity of four control variables (g, w_1, w_2 and f_s) the first presented scheme is simplified to only incorporate one clamping parameter w and using a half-bridge circuit on the primary bridge [28].

In [22] it is mentioned that employing clamping to both full-bridges simultaneously has only minimal effect on the reduction of RMS currents. Furthermore, an even higher power level is required to satisfy the ZVS condition when compared to the one-sided clamping only (cf. Chapter 3). Thus simultaneous clamping brings only limited advantages to a single-phase DAB converter but increases the complexity [22]. Further investigation in [22] suggests that employing clamping to both full-bridges simultaneously is only beneficial for very light-load operation with a wide input and/or output voltage range. Moreover, it is mentioned that dual clamping is not useful for high-load conditions.

Taking the above into consideration, the one-sided clamping looks to be the most promising when it comes to the reduction of RMS currents, increasing the ZVS range and keeping the complexity at a moderate level. Therefore the one-sided clamping is investigated and described in the present Chapter in full detail.

The presented modulation scheme only utilizes one additional modulation parameter as follows:

$$w_1 \in [0; 0.5] \land w_2 = 0 \qquad \text{if} \quad V_1 > n\,V_2 \tag{2.28}$$

or

$$w_1 = 0 \land w_2 \in [0; 0.5] \qquad \text{if} \quad V_1 < n\,V_2 \tag{2.29}$$

Hereafter the one-sided clamping interval will be referred to as w only which denotes w_1 if $V_1 > n\,V_2$ and w_2 if $V_1 < n\,V_2$ respectively.

$$\begin{aligned} w = w_1 \land w_2 = 0 \quad &\text{if} \quad V_1 > n\,V_2 \\ w = w_2 \land w_1 = 0 \quad &\text{if} \quad V_1 < n\,V_2 \end{aligned} \tag{2.30}$$

A negative phase-shift ($g < 0$) in a DAB converter operated with the conventional phase-shift modulation denotes a negative power transfer (Figure 2.6). When applying a one-sided clamping interval the direction of power transfer is no longer solely determined by the polarity of the phase-shift g. It is possible to generate a positive power transfer with $g < 0$ and $w > 0$ (cf. Figure 2.12). Thus two different cases have to be distinguished to derive a mathematical description of the one-sided clamped modulation scheme. Furthermore the maximum power transfer occurs at $g = 0.25$ and a further increase in phase-shift decreases the transferred power to zero at $g = 0.5$. This means that a set two possible phase-shift time intervals are able to transfer one power level. As g being the control variable ultimately controlling the output voltage, only an unequivocal solution per transferred output power is allowed. Therefore further study only takes $|g| \leq 0.25$ into consideration.

$$|g| \overset{!}{\leq} 0.25 \tag{2.31}$$

Case I ($g > 0$)

The typical steady-state voltage and inductor current waveforms for the one-sided clamped modulation with $V_1 < n\,V_2$, $P > 0$ and $g > 0$ are depicted in Figure 2.10. It is apparent that the period of one switching cycle can be split into six time intervals. Due to half-cycle symmetry only regions I to III are considered for deriving the mathematical description of the inductor current $i_L(t)$. At $t = t_0$ an initial current

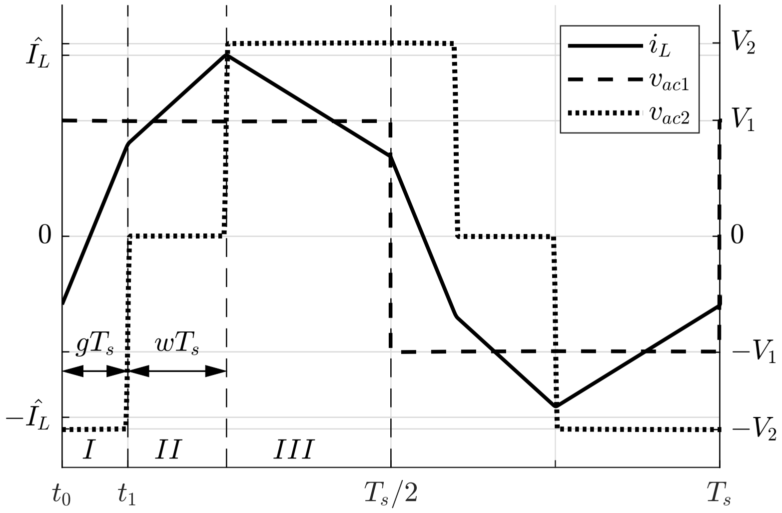


Fig. 2.10.: Transformer voltages and inductor current with $g > 0$

i_{L0} is assumed. Due to a positive phase-shift the full-bridges apply $v_L = V_1 + n\,V_2$ upon the equivalent inductor. Consequently the inductor current increases during Region I ($t_0 \leq t < t_1$) according to:

$$i_L(t) = i_{L0} + \frac{V_1 + n\,V_2}{L}\,t \qquad \forall \quad t \in [t_0; t_1] \tag{2.32}$$

At $t = t_1$ the clamping interval starts and the zero voltage is generated by the secondary full-bridge ($v_{ac2} = 0$), while the primary voltage remains unchanged.

Subsequently the inductor current changes during Region II ($t_1 \leq t < t_2$) with a positive slope according to:

$$i_L(t) = i_L(t_1) + \frac{V_1}{L}\,(t - t_1) \qquad \forall \quad t \in [t_1; t_2] \tag{2.33}$$

At $t = t_2$ the state of the secondary full-bridge changes, applying $v_L = V_1 - n\,V_2$ upon the equivalent inductor during Region III ($t_2 \leq t < t_0 + T_s/2$). Due to $V_1 < n\,V_2$ the inductor will decrease according to

$$i_L(t) = i_L(t_2) + \frac{V_1 - n\,V_2}{L}\,t \qquad \forall \quad t \in [t_2; t_0 + T_s/2] \tag{2.34}$$

until half the switching cycle is completed at $t = T_s/2$. Inserting $t_1 = g\,T_s$, $t_2 = (g + w)\,T_s$ and $i_L(t_0 + T_s/2) = -i_L(t_0)$ into Equations (2.32), (2.33) and (2.34) yields the analytical expression for the initial current i_{L0}:

$$i_{L0,\Diamond} = -\frac{V_1 + n\,V_2\,(4\,g + 2\,w - 1)}{4\,f_s\,L} \tag{2.35}$$

The inductor current at $t = t_1$ and $t = t_2$ is given by

$$i_{L,\Diamond}(t_1) = \frac{V_1\,(4\,g - 1) - n\,V_2\,(2\,w - 1)}{4\,f_s\,L} \tag{2.36}$$

and

$$i_{L,\Diamond}(t_2) = \frac{V_1\,(4\,g + 4\,w - 1) - n\,V_2\,(2\,w - 1)}{4\,f_s\,L} \tag{2.37}$$

respectively. Finally the transferred power of the one-sided clamped modulation with $g > 0$ is given by:

$$P_\Diamond = \frac{n\,V_1\,V_2\,(2\,g - 4\,g^2 + w - 2\,w^2 - 4\,g\,w)}{2\,f_s\,L} \qquad \forall \quad g > 0 \text{ and } w > 0 \tag{2.38}$$

The maximum transferable power can be retrieved by solving $\partial^2 P/\partial g \partial w = 0$ which results in $g = 0.25$ and $w = 0$. With the clamping interval approaching zero ($w \to 0$) the one-sided clamped modulation goes over into the conventional phase-shift modulation transferring maximum power with $g = 0.25$ (cf. Equation (2.19)). Consequently a seamless transition from the one sided-clamped to the phase-shift modulation and vice versa is possible.

Case II ($g \leq 0$)

Figure 2.11 shows the typical steady-state voltage and inductor curent waveforms for the one-sided clamped modulation with $V_1 < n\,V_2$, $P > 0$ and $g < 0$. Due to only

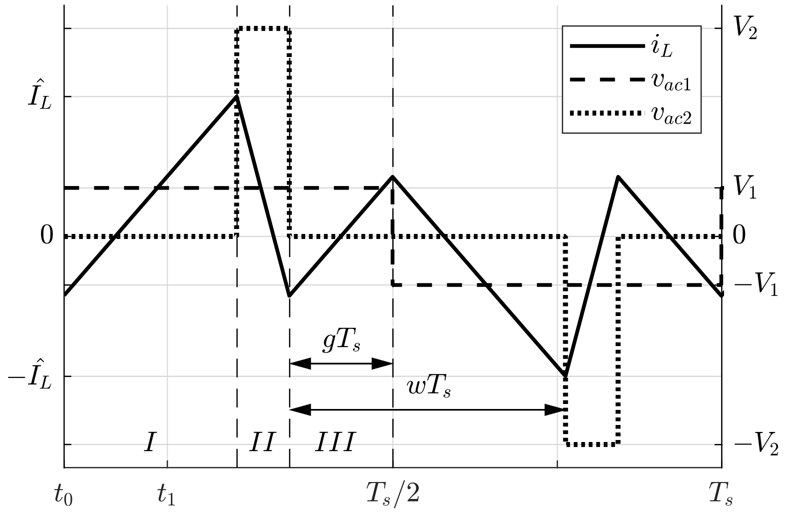


Fig. 2.11.: Transformer voltages and inductor current with $g < 0$

applying clamping to one full-bridge the inductor current can again be spit into six regions of which only three are relevant for further calculations (Regions I to III). It is visible, that the current follows a triangular shape (compared to the trapezoidal shape with $g > 0$).

Again an initial current i_{L0} is assumed and during Region I ($t_0 \leq t < t_1$) the inductor current rises according to:

$$i_L(t) = i_{L0} + \frac{V_1}{L}\, t \qquad \forall \quad t \in [t_0; t_1] \tag{2.39}$$

At $t = t_1$ the voltage generated by the secondary full-bridge changes and the inductor current decreases ($V_1 < n\, V_2$) during II ($t_1 \leq t < t_2$) and it follows:

$$i_L(t) = i_L(t_1) + \frac{V_1 - n\, V_2}{L}\, (t - t_1) \qquad \forall \quad t \in [t_1; t_2] \tag{2.40}$$

During Region III ($t_2 \leq t < t_0 + T_s/2$) the voltage generated by the secondary full-bridge falls back to zero and the inductor current will increase again according to:

$$i_L(t) = i_L(t_2) + \frac{V_1}{L}\, (t - t_2) \qquad \forall \quad t \in [t_2; t_0 + T_s/2] \tag{2.41}$$

The initial current is defined as

$$i_{L0,\Delta} = -\frac{V_1 + nV_2\, (1 - 2\, w)}{4 f_s L} \qquad \forall \quad g < 0, \tag{2.42}$$

the inductor current at t_1 and t_2 as

$$i_{L,\Delta}(t_1) = \frac{V_1\, (4\, g + 4\, w - 1) - n\, V_2\, (2\, w - 1)}{4\, f_s\, L} \qquad \forall \quad g < 0, \tag{2.43}$$

and

$$i_{L,\Delta}(t_2) = \frac{V_1\,(4\,g + 1) + n\,V_2\,(2\,w - 1)}{4\,f_s\,L} \qquad \forall \quad g < 0 \tag{2.44}$$

and the transferred power as

$$P_\Delta = \frac{n\,V_1\,V_2\,(2\,g + w - 2\,w^2 - 4\,g\,w)}{2\,f_s\,L} \qquad \forall \quad g < 0 \text{ and } w > 0 \tag{2.45}$$

respectively.

The maximum power transferable is obtained by solving $\partial^2 P/\partial g \partial w = 0$ and inserting the resulting $g = 0$ and $w = 0.25$ into Equation (2.45). The maximum transferable power of the one-sided clamped modulation with $g < 0$ is finally given by:

$$P_{\Delta,max} = \frac{n\,V_1\,V_2}{16\,f_s\,L}, \qquad \text{with} \quad g = 0 \text{ and } w = 0.25 \tag{2.46}$$

Zero-Voltage-Switching Constraints

As described before in order to ensure ZVS, the full-bridges have to be operated under forced commutation to avoid hard diode commutation[1]. Again the two cases have to be dealt with separately and the boundary conditions for an ideal DAB converter operated with the one sided-clamped modulation can be defined as:

Case I ($g > 0$)

1. $i_L(t_0) < 0$
2. $i_L(t_1) > 0$ (2.47)
3. $i_L(t_2) > 0$

Case II ($g \leq 0$)

1. $i_L(t_0) < 0$
2. $i_L(t_1) > 0$ (2.48)
3. $i_L(t_2) < 0$

2.3. Combined Modulation Scheme

To optimise the steady-state DAB operation with respect to maximum converter efficiency, the modulation parameters have to be continuously updated, depending on the current operating point. The conventional phase-shift modulation is best suited when $V_1 = nV_2$ (cf. Figure 2.8) transferring zero to full power by only changing $g \in [0; 0.25]$. A difference in the input and the primary referred output voltage results in high RMS currents and the loss of ZVS under light-load operation. To decrease RMS currents and ensure ZVS over the whole operation range, the modulation parameter w is introduced. Depending on the voltage ratio d and the power level P the clamping interval w is calculated and $g \in [-0.25; 0.25]$ is changed to transfer the needed power P with respect to maximum converter efficiency. The proposed optimisation for the combined modulation scheme focuses on minimising the inductor RMS current. It is shown that by minimising the RMS current, the range of ZVS is significantly extended, reaching from no to full load. Only the transition between Case I and Case II ($g = 0$) of the one-sided clamped modulation scheme leads to the loss of ZVS as the inductor current approaches zero resulting in a pure triangular waveform. With the phase-shift of zero ($g = 0$) it holds that $i_L(t_0) = i_L(t_1) = 0$ and zero-current-switching (ZCS) is achieved at t_0 producing reduced switching losses. The triangular current mode is described in detail in [38].

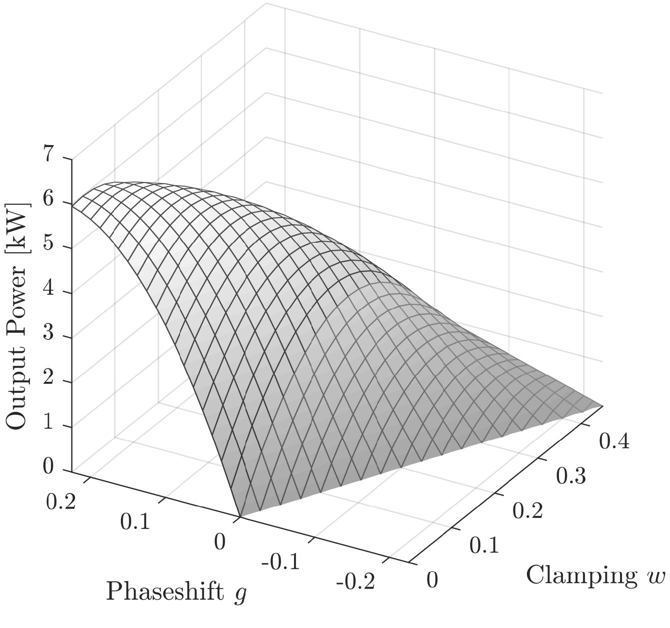


Fig. 2.12.: Transferable power of the proposed combined modulation scheme with $V_1 = 207\,\mathrm{V}$ and $V_2 = 230\,\mathrm{V}$

Figure 2.12 depicts the surface plot of the positive power transfer of the combined modulation scheme in relation to g and w with $V_1 = 207\,\mathrm{V}$ and $V_2 = 230\,\mathrm{V}$. It is visible that with a negative phase-shift ($g < 0$) a positive power transfer ($P > 0$) is present when w does not exceed a certain range. Furthermore, no discontinuity of the surface of the transferred power is present, which suggests that a seamless transition between the modulation schemes is possible.

For the proposed combined modulation scheme, a set of five parameters is required, consisting of V_1, V_2, P, g and w. Depending on the power level P and the voltage ratio d, the optimal clamping interval w and phase-shift g have to be set to minimise the inductor RMS current. The presented optimisation results focus on $V_1 < nV_2$ only, resulting in a voltage ratio of $1/d$ and the clamping intervals $w_1 = w$ and $w_2 = 0$. Due to the symmetry of the DAB converter, the optimal set of parameters can be directly projected to the operation with $V_1 > n\,V_2$ by changing the voltage ratio to d and replacing $w_1 = 0$ and $w_2 = w$. The surface plot of the inductor RMS current in relation to w and $1/d$ with $V_2 = 230\,\mathrm{V}$ and $P = 1000\,\mathrm{W}$ is depicted in Figure 2.13. The valley of the surface plot is highlighted, which denotes the optimal set of parameters that minimise the RMS current at the specific operating point.

Figure 2.14 shows the contours of the inductor RMS current in relation to w and $1/d$ at different power levels ranging from $P = 100\,\mathrm{W}$ (Figure 2.14a) to $P = 5000\,\mathrm{W}$ (Figure 2.14a).

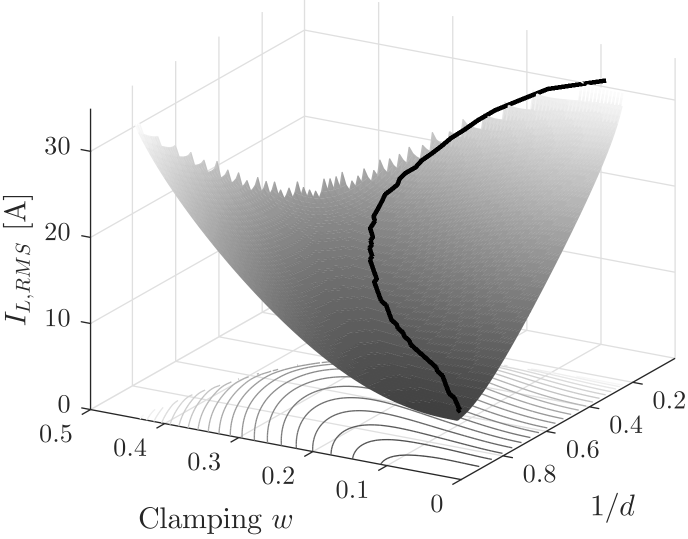
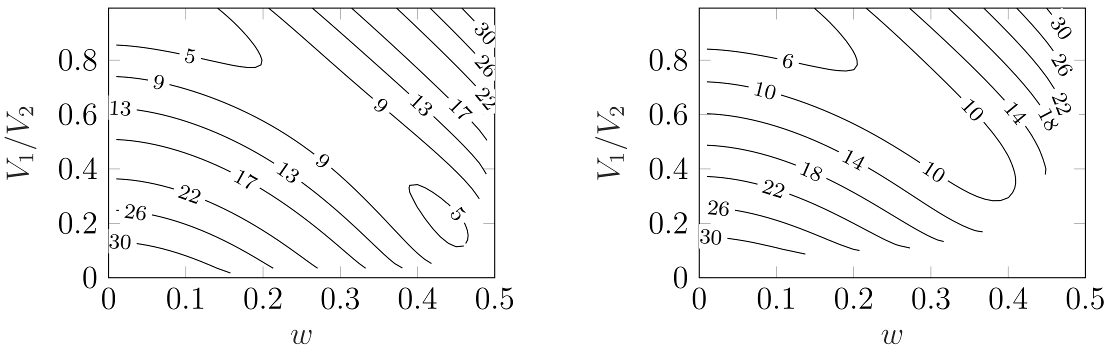
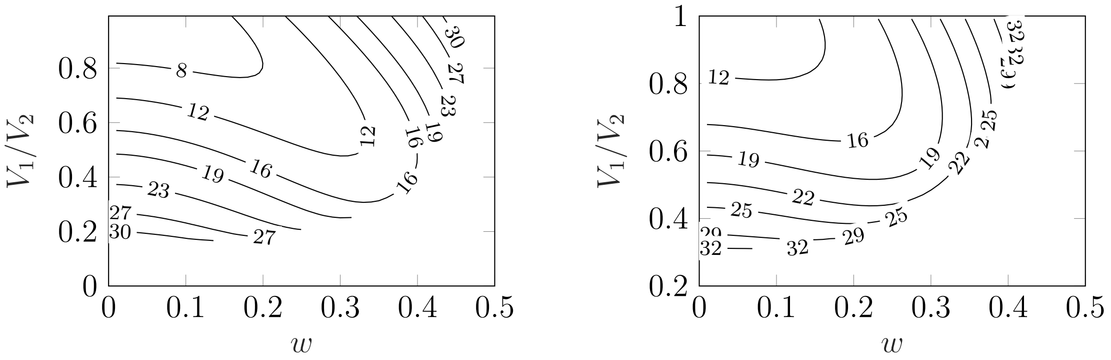


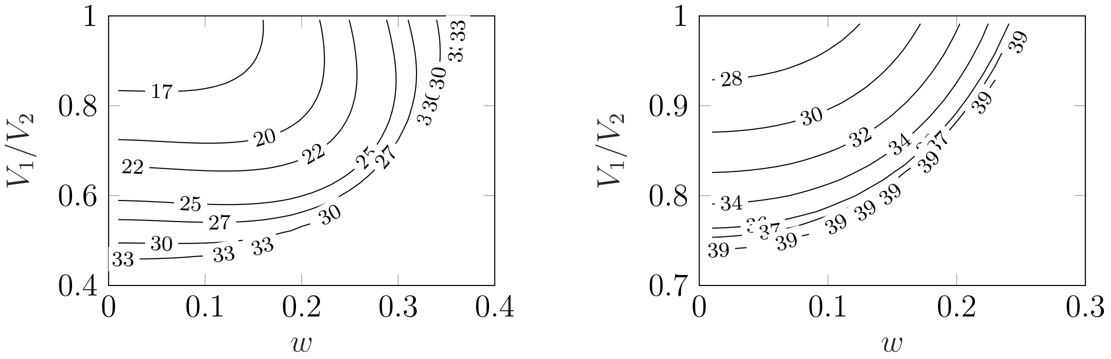
Fig. 2.13.: Surface plot of the resulting inductor RMS current in relation to the clamping interval w and the voltage ratio $1/d$ with $V_2 = 230\,\mathrm{V}$ and $P = 1000\,\mathrm{W}$. The valley (minimum) of the surface plot is shown.



(a) Inductor RMS currents with $P = 100\,\mathrm{W}$ (b) Inductor RMS currents with $P = 500\,\mathrm{W}$



(c) Inductor RMS currents with $P = 1000\,\mathrm{W}$ (d) Inductor RMS currents with $P = 2000\,\mathrm{W}$



(e) Inductor RMS currents with $P = 3000\,\mathrm{W}$ (f) Inductor RMS currents with $P = 5000\,\mathrm{W}$

Fig. 2.14.: Contour plots of the inductor RMS current with $V_2 = 230\,\mathrm{V}, n = 1, f_s = 40\,\mathrm{kHz}$ and $L = 24\,\mu\mathrm{H}$ in relation to the clamping interval w and the voltage ratio $1/d$ at different power levels (a to f)

The clamping intervals w that minimize the contours of the inductor RMS currents plotted in Figure 2.14 are depicted in Figure 2.15. It is apparent that with higher transferred power, the possible influence of the clamping parameter w reduces. This implies that the combined modulation scheme is most effective in the low power region.

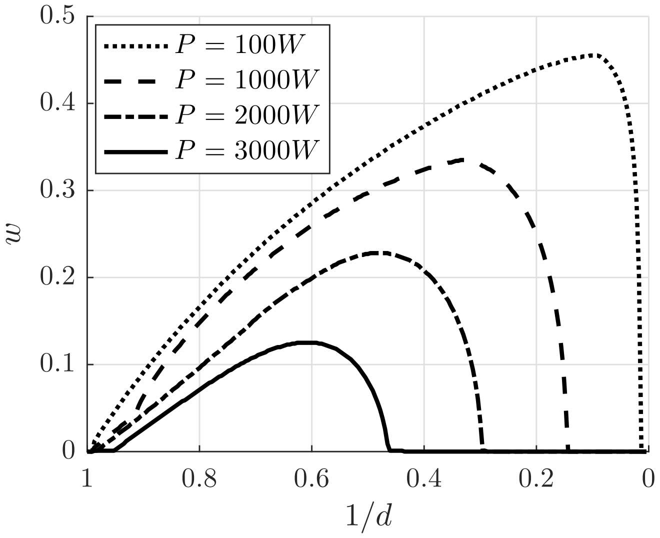


Fig. 2.15.: Optimal clamping interval w of the combined modulation scheme in relation to the voltage ratio $1/d$ and the transferred power P as parameter with $V_2 = 230\,\mathrm{V}$

The optimal operation of the combined modulation scheme can now be derived. Figure 2.16 shows the optimal set of modulation parameters g and w with $V_1 = 138\,\mathrm{V}$ and $V_2 = 230\,\mathrm{V}$. In relation to the transferred power the set of parameter can be split into three different regions. These regions (I to III) refer to the three different modulations (one-sided clamped Case I and Case II and conventional phase-shift) of the combined modulation scheme.

The corresponding inductor current and voltage waveforms for the denoted Regions are depicted in Figure 7.2. At low power operation the one-sided clamped modulation with $g < 0$ is optimal (Region I, Figure 2.17a) until g reaches zero at $P_{\Delta,max}$. Here the transition (Figure 2.17b) to the one-sided modulation with $g > 0$ occurs which is optimal for medium power transfer (Region II, Figure 2.17c). When w reaches zero at $P_{PS,min}$ the conventional phase shift modulation is optimal for high power transfer (Region III, Figure 2.17d) until the maximum transferable power is reached ($P_{PS,max}$).

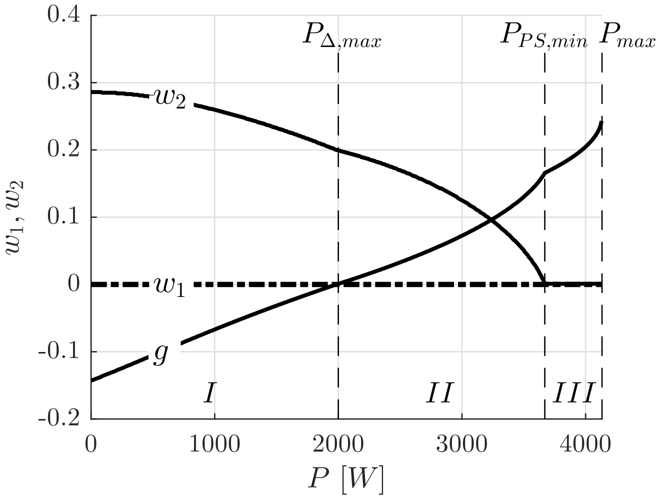
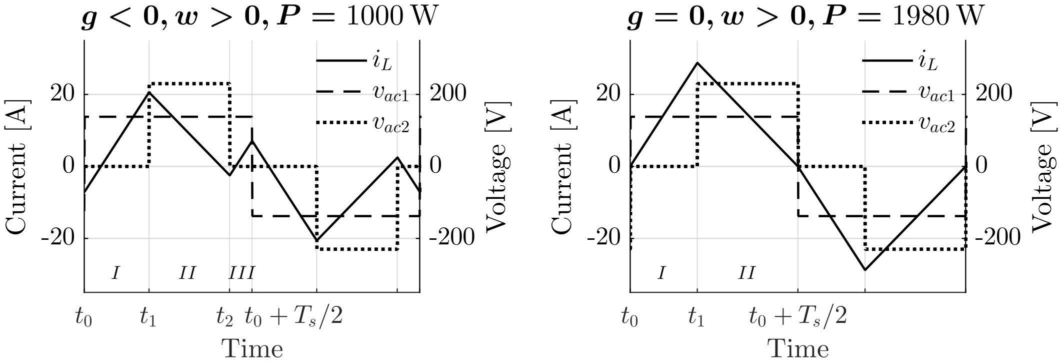
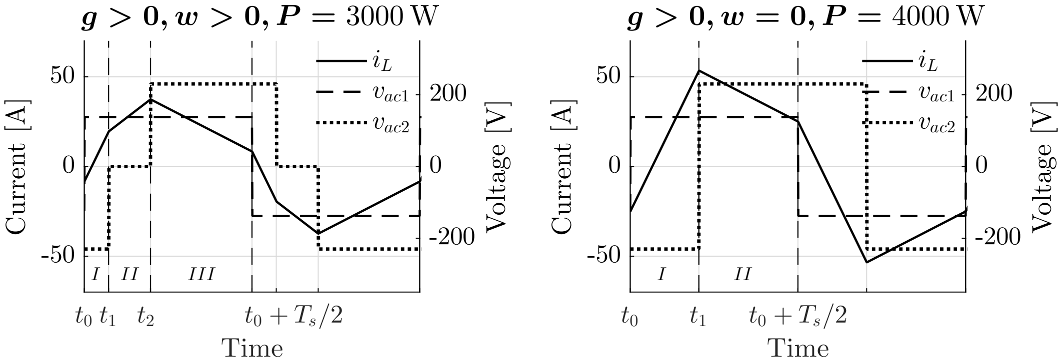


Fig. 2.16.: Optimal modulation parameters (clamping intervals w_1, w_2 and phase-shift g) of the combined modulation scheme in relation to the transferred power P with $V_1 = 138\,\mathrm{V}$ and $V_2 = 230\,\mathrm{V}$. Region I denotes $g < 0$ and Region II denotes $g > 0$ of the one-sided clamped modulation. Region III refers to the phase-shift modulation with $w_1 = w_2 = 0$.



(a) One-sided clamped modulation Case I ($g < 0$)

(b) Transition between Case I and Case II of the one-sided clamped modulation ($g = 0$)



(c) One-sided clamped modulation Case II ($g > 0$)

(d) Conventional phase-shift modulation with $w = 0$

Fig. 2.17.: Possible current and voltage waveforms of the combined modulation scheme with $V_1 = 138\,\mathrm{V}$ and $V_2 = 230\,\mathrm{V}$. ZVS on all power electronic switches in (a), (c) and (d) and ZVS/ZCS in (b).

2.3.1. Zero-Voltage Switching

To analyse the ZVS performance of the combined modulation scheme with the presented set of optimal parameters, the inductor current has to be examined at the switching transition times t_0, t_1 and t_2. For each modulation (one-sided clamped Case I and Case II and conventional phase-shift), the ZVS constraints have to verified separately. The ZVS constraints of the combined modulation scheme are listed in Table 2.3:

Tab. 2.3.: ZVS constraints of combined modulation scheme

Region	ZVS Constraints		
I	$i_L(t_0) < 0,$	$i_L(t_1) > 0,$	$i_L(t_2) < 0$
II	$i_L(t_0) < 0,$	$i_L(t_1) > 0,$	$i_L(t_2) > 0$
III	$i_L(t_0) < 0,$	$i_L(t_1) > 0$	

Figure 2.18 shows the inductor current waveform of the switching times t_0, t_1 and t_2 of the combined modulation scheme in relation to the transferred power. Furthermore the three different modulation regions are denoted I ,II and III. The inductor current waveform for each of the three switching times t_0, t_1 and t_2 can be seen and it holds for t_0

$$i_L(t_0) \leq 0 \qquad \text{for} \quad 0 < P \leq P_{max} \tag{2.49}$$

for t_1

$$i_L(t_1) > 0 \qquad \text{for} \quad 0 < P \leq P_{max} \tag{2.50}$$

and lastly for t_2:

$$\begin{aligned} i_L(t_2) &\leq 0 \qquad \text{for} \quad 0 < P \leq P_{\Delta,max} \quad \text{and} \\ i_L(t_2) &> 0 \qquad \text{for} \quad P_{\Delta,max} < P \leq P_{max} \end{aligned} \tag{2.51}$$

A comparison of the inductor current waveforms for t_0, t_1 and t_2 in Figure 2.18 to the ZVS constraints listed in Table 2.3 shows, that for an ideal DAB converter soft switching is possible over the whole operating range, when the converter is modulated with the presented combined modulation scheme. At low power, when Region I is best suited, the ZVS constraints (cf. Table 2.3) are satisfied resulting in ZVS on all power electronic switches. When g reaches zero the inductor currents hold: $i_L(t_0) = i_L(t_2) = 0$ and $i_L(t_1) > 0$.

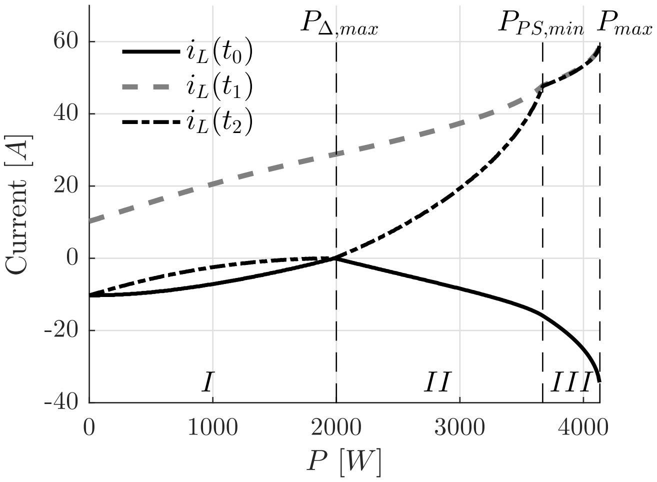


Fig. 2.18.: Inductor current at the switching times t_0, t_1 and t_2 of the combined modulation scheme in relation to the transferred power P with $V_1 = 138\,\text{V}$ and $V_2 = 230\,\text{V}$. Region I denotes $g < 0$ and Region II denotes $g > 0$ of the one-sided clamped modulation. Region III refers to the phase-shift modulation.

This results in ZVS at t_1 and to ZCS at t_0 and t_2. At medium power and full power, all ZVS constraints are satisfied, and ZVS is again ensured on all power electronic switches. Finally, the conditions, the resulting modulation scheme and the corresponding modulation parameters' range of the combined modulation scheme with positive power transfer are listed in Table 2.4.

Tab. 2.4.: Combined modulation scheme with positive power transfer

Condition	Modulation scheme	Molulation parameters
1. $\boldsymbol{V_1 = nV_2}$		
• $P \geq 0$	phase-shift	$w_1 = 0 \wedge w_2 = 0 \wedge g \geq 0$
2. $\boldsymbol{V_1 < nV_2}$		
• $P > P_{PS.min}$	phase-shift	$w_1 = 0 \wedge w_2 = 0 \wedge g > 0$
• $P_{\Delta.max} < P \leq P_{PS.min}$	one-sided clamped	$w_1 = 0 \wedge w_2 > 0 \wedge g > 0$
• $P \leq P_{\Delta.max}$	one-sided clamped	$w_1 = 0 \wedge w_2 > 0 \wedge g \leq 0$
3. $\boldsymbol{V_1 > nV_2}$		
• $P > P_{PS.min}$	phase-shift	$w_1 = 0 \wedge w_2 = 0 \wedge g > 0$
• $P_{\Delta.max} < P \leq P_{PS.min}$	one-sided clamped	$w_1 > 0 \wedge w_2 = 0 \wedge g > 0$
• $P \leq P_{\Delta.max}$	one-sided clamped	$w_1 > 0 \wedge w_2 = 0 \wedge g \leq 0$

2.4. DAB Converter considering conduction losses

The lossless DAB converter model (cf. Chapter 2.3) allows a linear analytical description of the DAB converter. However, due to converter losses, significantly different results may be computed, when compared to measurement results. The overall losses of a power electronic converter are due to conduction losses, switching losses and losses induced in the magnetic components and are analysed in detail in Chapter 5. The influence of the conduction losses is shown in Figure 2.23.

In this Section, the lossless DAB converter model is extended, and the conduction losses of the converter are included in the description of the inductor current. This allows a more accurate description, but still keeping the complexity at a moderate level. The ideal switches in the lossless DAB converter (cf. Figure 2.1) are replaced by MOSFETs depicted in Figure 2.19.

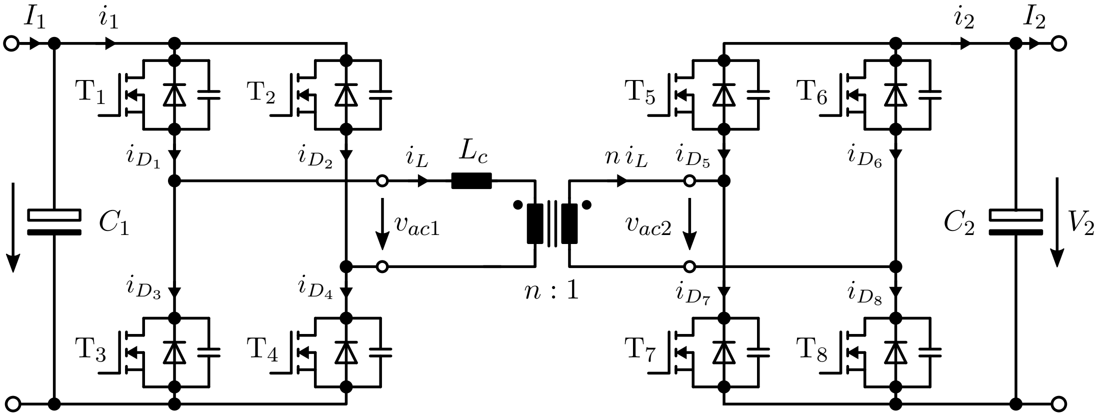


Fig. 2.19.: DC-DC Dual Active Bridge (DAB) converter with MOSFETs

The resulting equivalent circuit diagram of a DAB converter, including all relevant ohmic resistances is shown in Figure 2.20. The resistance of the PCB trace is neglected as it is small compared to the overall resistance in the current path ($R_{PCB} << R_{tot}$). Furthermore, the ESR of the capacitors and the parasitic stay inductance of the components are neglected. Due to the assumption of instantaneous voltage transitions, no dead-time is present, and hence the anti-parallel diodes (cf. Figure 2.19) are never forward biased. As the converter is operated under ZVS (cf. Chapter 3) the conduction losses of the MOSFETs dominate, and the dynamic losses are negligible. Therefore the MOSFETs can be replaced by an ideal switch connected in series to the total drain-source on-state resistance $R_{DS,on}$ of the MOSFET. Furthermore only four switching states (cf. Table 2.2) are considered for each full-bridge. The power path of switching state I is depicted in Figure 2.21 showing the relevant components for the denoted switching state. The total inductance is equal the sum of the coupling inductor and the primary referred stray inductance of the transformer. The primary referred

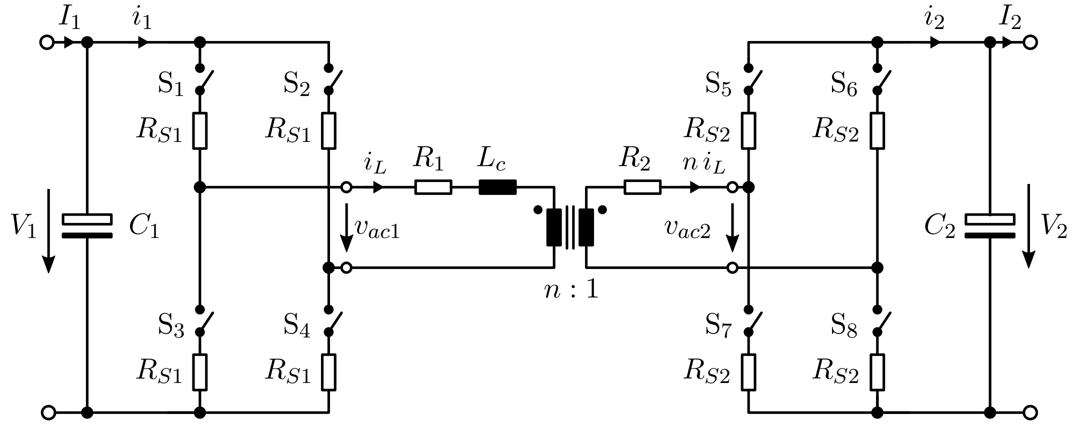


Fig. 2.20.: Equivalent circuit diagram of a DAB converter showing all relevant ohmic resistances. The MOSFETs are replaced by ideal switches connected in series to the total drain-source on-state resistance R_{S1} and R_{S2}. R_{S1} denotes the drain-source on-state resistance of the primary bridge's MOSFETs and R_{S2} the secondary bridge's MOSFETs respectively.

stray inductance of the transformer is measured with a vector network analyser (cf. Appendix C) with the secondary winding shorted and is further referred to L_σ only. Hence the total equivalent inductance equals to:

$$L_{eq} = L_c + L_\sigma \tag{2.52}$$

The resistance R_1 combines the series resistance of the coupling inductor R_c and the winding resistance of the transformer primary winding R_{cu1}. The resistance R_2 refers to the winding resistance of the secondary winding R_{cu2} and it follows:

$$\begin{aligned} R_1 &= R_c + R_{cu1} \\ R_2 &= R_{cu2} \end{aligned} \tag{2.53}$$

For switching state I of the primary full-bridge S_1 and S_4 are turned on generating $v_{ac1} = V_1$ and the current path encloses $2R_{S1}, R_1$ and L_1. For $v_{ac1} = -V_1$ (switching state IV) a similar switch configuration is present. For switching states II and III the current free-wheels ether through the high-side or through the low-side switches, generating $v_{ac1} = 0$, a different switch configuration occurs. Figure 2.20 however shows, that for each switching state configuration equal resistance values result and it holds for the total resistance of the primary side:

$$\begin{aligned} R_{tot,1} &= 2\,R_{S1} + R_1 \\ &= 2\,R_{S1} + R_c + R_{cu1} \end{aligned} \tag{2.54}$$

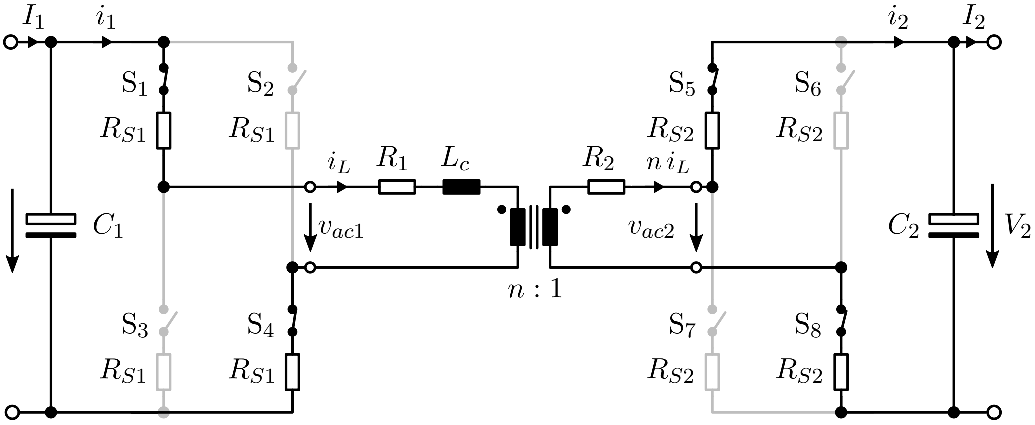


Fig. 2.21.: Equivalent circuit diagram of a DAB converter showing relevant ohmic resistances in the power path with $v_{ac1} = V_1$ and $v_{ac2} = V_2$ (switching state I in Table 2.2)

Analysing the secondary side in the same manner as mentioned above, the current path for each switching state encloses $2\,R_{S2}$ and R_2 and hence the total resistance for the secondary side equals to:

$$R_{tot,2} = 2\,R_{S2} + R_2 \tag{2.55}$$

The primary referred equivalent circuit diagram of a DAB converter considering conduction losses is depicted in Figure 2.22 and the shown total equivalent resistance R_{eq} results with (2.54) and (2.55) in:

$$\begin{aligned} R_{eq} &= R_{tot,1} + n^2\,R_{tot,2} \\ &= 2\,R_{S1} + R_1 + n^2\,(2\,R_{S2} + R_2) \\ &= 2\,R_{S1} + R_c + R_{cu1} + n^2\,(2\,R_{S2} + R_{cu2}) \end{aligned} \tag{2.56}$$

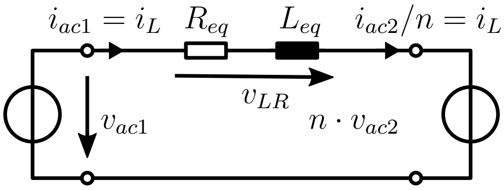


Fig. 2.22.: Primary-referred equivalent circuit of a DAB converter taking conduction losses into consideration

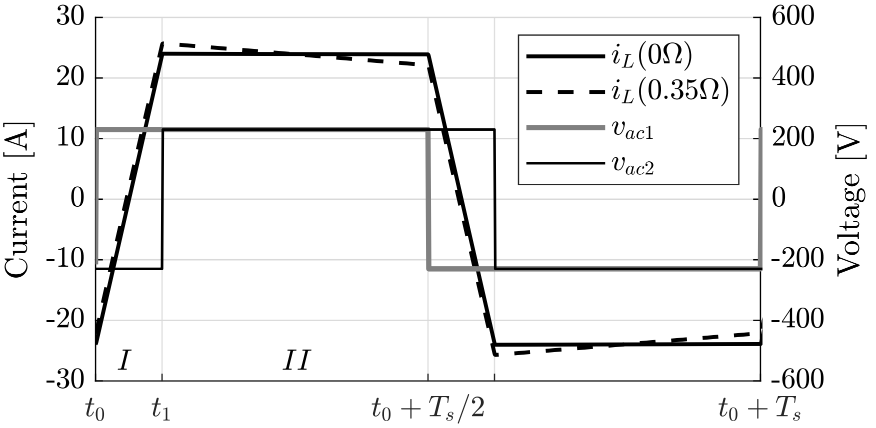


Fig. 2.23.: Influence of ohmic resistance on the inductor current shape with phase-shift modulation of the lossless model (solid line) and the model considering conduction losses with a total resistance (cf. Figure 2.22) of $R = 0.35\,\Omega$ (dashed line) and $V_1 = V_2 = 230\,\text{V}$

2.4.1. Analytical Current Description

To analyse the DAB converter with conduction losses, the inductor current has to be described. The inductor current i_L is generated by the voltage v_{LR} applied to the series connected R_{eq} and L_{eq} shown in Figure 2.22 and is given by:

$$\begin{aligned} v_L(t) &= v_{LR}(t) - v_R(t) \\ &= v_{LR}(t) - i_L(t)\,R \end{aligned} \tag{2.57}$$

The generated inductor current results with (2.5) and (2.57) in:

$$i_L(t) = i_L(t_0) + \frac{1}{L}\int_{t_0}^{t_1} [v_{LR}(t) - i_L(t)\,R]\,\mathrm{d}t \qquad \forall \quad t_0 < t_1 \tag{2.58}$$

In order to obtain a analytical description of the inductor current the first order differential equation of the LR series resonant circuit depicted in Figure 2.22 has to be solved. The differential equation holds

$$L\,\frac{di(t)}{dt} + R\,i(t) - v_{LR}(t) = 0 \tag{2.59}$$

with the solution

$$i_L(t) = i_L(t_0)\,e^{-\frac{t}{\tau}} + \frac{v_{RL}}{R}\,(1 - e^{-\frac{t}{\tau}}) \tag{2.60}$$

assuming an initial current $i_L(t_0)$.

The inductor current at any time $t_1 > t_0$ is given by:

$$i_L(t_1) = i_L(t_0)\, e^{-\frac{t_1-t_0}{\tau}} + \frac{v_{RL}}{R}\,(1 - e^{-\frac{t_1-t_0}{\tau}}) \tag{2.61}$$

with

$$v_{LR} = \text{const.} \qquad \forall \quad t \in [t_0; t_1] \tag{2.62}$$

The transferred power is calculated with

$$P_1 = \frac{2V_1}{T_s}\left(\int_0^{gT_s} i_L(t)\,\mathrm{d}t + \int_{gT_s}^{T_s/2} i_L(t)\,\mathrm{d}t\right) \tag{2.63}$$

and

$$P_2 = \frac{2V_2}{T_s}\left(-\int_0^{gT_s} i_L(t)\,\mathrm{d}t + \int_{gT_s}^{T_s/2} i_L(t)\,\mathrm{d}t\right) \tag{2.64}$$

using piecewise integration shown in (2.9).

Furthermore the inductor RMS current is of interest as the proposed optimisation focuses on minimising the inductor RMS current. The inductor RMS current is again calculated by piecewise integration, which results in:

$$I_{L,RMS} = \sqrt{\frac{2}{T_s}\left(\int_0^{gT_s} i_L^2(t)\,\mathrm{d}t + \int_{gT_s}^{T_s/2} i_L^2(t)\,\mathrm{d}t\right)} \tag{2.65}$$

Phase-Shift Modulation

The inductor current for a DAB converted modulated with the conventional phase-shift modulation at t_0 and t_1 is obtained by inserting $t_1 = g\,T_s$ and $i_L(T_s/2) = -i_0$ into (2.60) and it holds for i_{L0}

$$i_{L0,PS} = \frac{(V_1 - n\,V_2)\left(e^{\frac{g-0.5}{f_s\,\tau}} - 1\right) + (V_1 + nV_2)\, e^{\frac{g-0.5}{f_s\,\tau}}\,(e^{-\frac{g}{f_s\,\tau}} - 1)}{R\,(e^{\frac{1}{2\,f_s\,\tau}} + 1)} \tag{2.66}$$

and for $i_L(t_1)$:

$$\begin{aligned} i_{L,PS}(t_1) = e^{-\frac{g}{f_s\,\tau}}\, &\frac{(V_1 - n\,V_2)\,\left(e^{\frac{g-0.5}{f_s\,\tau}} - 1\right) + (V_1 + n\,V_2)\; e^{\frac{g-0.5}{f_s\,\tau}}\,\left(e^{-\frac{g}{f_s\,\tau}} - 1\right)}{R\,\left(e^{\frac{1}{2\,f_s\,\tau}} + 1\right)} \\ &- \frac{(V_1 + nV_2)\,\left(e^{-\frac{T_s\,g}{\tau}} - 1\right)}{R} \end{aligned} \tag{2.67}$$

The transferred power on the primary side P_1 and on the secondary bridge P_2 is calculated with (2.63), (2.64), (2.66) and (2.67) and it holds for P_1:

$$\begin{aligned} P_{1,PS} =& \frac{2\,V_1}{T_s} \left(\int_0^{g\,T_s} i_L(t_0)\, e^{-\frac{t}{\tau}} + \frac{V_1 + V_2}{R} \left(1 - e^{-\frac{t}{\tau}}\right) \mathrm{d}t \right. \\ & \left. + \int_0^{(0.5-g)\,T_s} i_L(t_1)\, e^{-\frac{t}{\tau}} + \frac{V_1 - V_2}{R} \left(1 - e^{-\frac{t}{\tau}}\right) \mathrm{d}t \right) \end{aligned} \tag{2.68}$$

and for P_2

$$\begin{aligned} P_{2,PS} =& \frac{2\,V_2}{T_s} \left(- \int_0^{g\,T_s} i_L(t_0)\, e^{-\frac{t}{\tau}} + \frac{V_1 + V_2}{R} \left(1 - e^{-\frac{t}{\tau}}\right) \mathrm{d}t \right. \\ & \left. + \int_0^{(0.5-g)\,T_s} i_L(t_1)\, e^{-\frac{t}{\tau}} + \frac{V_1 - V_2}{R} \left(1 - e^{-\frac{t}{\tau}}\right) \mathrm{d}t \right) \end{aligned} \tag{2.69}$$

The transferred input power P_1 and output power P_2 in relation to the phase-shift g with $R = 350\,\mathrm{m}\Omega$ are depicted in Figure 2.23. It is apparent that, due to conduction losses, the input and output power differ ($P_1 \neq P_2$). Furthermore the maximum power transfer occurs at different phase-shift values for P_1 and P_2. Again the phase-shift g_{max} to transfer the maximum output power is derived by solving $\partial P_{PS}/\partial g = 0$ for g which holds:

$$g_{max} = f_s\,\tau\, log \left(\frac{2\, e^{2\,\tau\, f_s}}{e^{2\,\tau\, f_s} + 1} \right) \tag{2.70}$$

The inductor RMS current, shown in Figure 2.25 increases, when compared to the losses model (cf. Figure 2.9). Higher RMS currents occur to compensate the losses caused by the ohmic resistance.

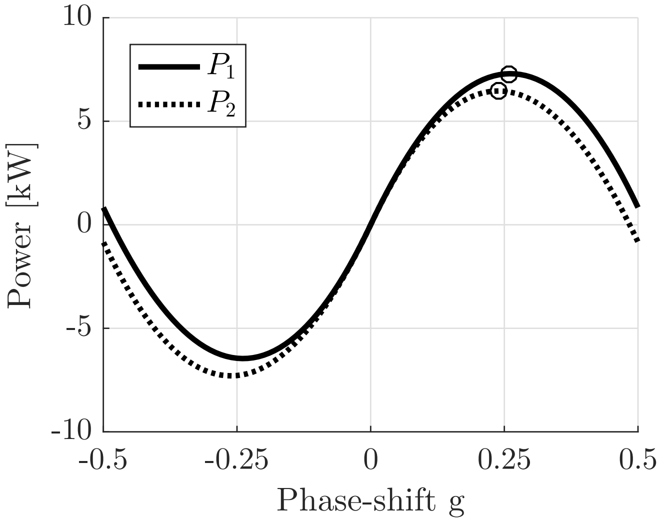


Fig. 2.24.: Transferred power of the DAB converter modulated with phase-shift modulation with conduction losses, $V_1 = 230\,\mathrm{V}, V_2 = 230\,\mathrm{V}, R = 350\,\mathrm{m\Omega}, L = 24\,\mathrm{\mu H}, n = 1$ and $f_s = 40\,\mathrm{kHz}$; $P_{1,max}$ and $P_{2,max}$ are encircled and are different due to conduction losses

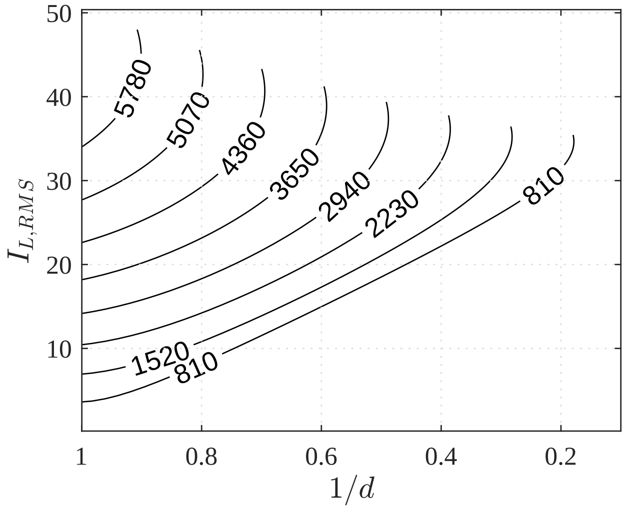


Fig. 2.25.: Inductor RMS current in relation to $1/d$ and the output power as parameter taking the conduction losses of an ohmic resistance of $350\,\mathrm{m\Omega}$ into consideration

Advanced Modulation Scheme

With the one-sided clamped modulation scheme three different time intervals (cf. Figure 2.10, 2.11, denoted interval I to III) are present during one half switching period. Hence the inductor current at the switching times t_0, t_1 and t_2 has to be known in order to calculate the transferred power and the inductor RMS current with piecewise integration. Furthermore the inductor current is necessary to verify the ZVS constraints listed in Table 2.3. As mentioned before, two cases ($g \leq 0$ and $g > 0$) have to be distinguished to derive the mathematical description of the one-sided clamped modulation scheme.

Case I ($g > 0$)

With a positive phase-shift and a clamping interval $w \in [0; 0.5]$ the switching transitions occur at $t_0 = 0$, $t_1 = g\,T_s$ and $t_2 = (g + w)\,T_s$ and are calculated as follows:

$$i_{L,\Diamond}(t_0) = \frac{\sigma_2 \Big(V_1\,(\sigma_3 - 1) + \sigma_3\,(V_1 + V_2)\,(\sigma_1 - 1)\Big) + (V_1 - V_2)\,(\sigma_2 - 1)}{R\,\sigma_4} \tag{2.71}$$

$$i_{L,\Diamond}(t_1) = \frac{\sigma_1 \Bigg(\Big(\sigma_2 \big(V_1\,(\sigma_3 - 1) + \sigma_3\,(\sigma_1 - 1)\,(V_1 + V_2)\big) + (V_1 - V_2)\,(\sigma_2 - 1)\Big)\Bigg)}{R\,\sigma_4} - \frac{(V_1 + V_2)\,(\sigma_1 - 1)}{R} \tag{2.72}$$

$$i_{L,\Diamond}(t_2) = \sigma_3 \left(\frac{\sigma_1\,\Big(\sigma_2 \big(V_1\,(\sigma_3 - 1) + \sigma_3\,(V_1 + V_2)\,(\sigma_1 - 1)\big) + (V_1 - V_2)\,(\sigma_2 - 1)\Big)}{R\,\sigma_4} - \frac{(V_1 + V_2)\,(\sigma_1 - 1)}{R} \right) - \frac{V_1\,(\sigma_3 - 1)}{R} \tag{2.73}$$

where

$$\begin{aligned}
\sigma_1 &= e^{-\frac{T_s\, g}{\tau}}\\
\sigma_2 &= e^{\frac{T_s\,\left(g+w-\frac{1}{2}\right)}{\tau}}\\
\sigma_3 &= e^{-\frac{T_s\, w}{\tau}}\\
\sigma_4 &= e^{-\frac{T_s}{2\,\tau}}+1
\end{aligned} \tag{2.74}$$

The transferred power on the primary side is given by

$$\begin{aligned}
P_{1,\Diamond} = \frac{2\,V_1}{T_s}\Bigg(&-\int_0^{g\,T_s} i_L(t_0)\, e^{-\frac{t}{\tau}} + \frac{V_1+V_2}{R}\left(1-e^{-\frac{t}{\tau}}\right)\mathrm{d}t\\
&+\int_0^{w\,T_s} i_L(t_1)\, e^{-\frac{t}{\tau}} + \frac{V_1-V_2}{R}\left(1-e^{-\frac{t}{\tau}}\right)\mathrm{d}t\\
&+\int_0^{(0.5-g-w)\,T_s} i_L(t_2)\, e^{-\frac{t}{\tau}} + \frac{V_1-V_2}{R}\left(1-e^{-\frac{t}{\tau}}\right)\mathrm{d}t\Bigg)
\end{aligned} \tag{2.75}$$

and on the secondary side by:

$$\begin{aligned}
P_{2,\Diamond} = \frac{2\,V_2}{T_s}\Bigg(&-\int_0^{g\,T_s} i_L(t_0)\, e^{-\frac{t}{\tau}} + \frac{V_1+V_2}{R}\left(1-e^{-\frac{t}{\tau}}\right)\mathrm{d}t\\
&+\int_0^{(0.5-g-w)\,T_s} i_L(t_2)\, e^{-\frac{t}{\tau}} + \frac{V_1-V_2}{R}\left(1-e^{-\frac{t}{\tau}}\right)\mathrm{d}t\Bigg)
\end{aligned} \tag{2.76}$$

Finally the inductor RMS current is calculated according to:

$$I_{L,RMS} = \sqrt{\frac{2}{T_s}\left(\int_0^{g\,T_s} i_L^2(t)\,\mathrm{d}t + \int_{g\,T_s}^{(g+w)\,T_s} i_L^2(t)\,\mathrm{d}t + \int_{(g+w)\,T_s}^{T_s/2} i_L^2(t)\,\mathrm{d}t\right)} \tag{2.77}$$

Case II ($g < 0$)

In the case of a negative phase-shift and a clamping interval $w \in [0; 0.5]$ the switching transitions occur at $t_0 = 0$, $t_1 = (w-g)\,T_s$ and $t_2 = (0.5-g)\,T_s$. The inductor current at switching time t_0 is given by

$$i_{L,\Delta}(t_0) = -\,\frac{(V_2 - V_1\,\sigma_1 + V_1\,\sigma_3 - V_2\,\sigma_2)}{R\,(\sigma_1+\sigma_3)} \tag{2.78}$$

at t_1 by

$$i_{L,\Delta}(t_1) = -\,\frac{V_1\,(\sigma_1-1)}{R} - \frac{\sigma_1\,(V_2 - V_1\,\sigma_1 + V_1\,\sigma_3 - V_2\,\sigma_2)}{R\,(\sigma_1+\sigma_3)} \tag{2.79}$$

and at t_2 by:

$$
\begin{aligned}
i_{L,\Delta}(t_2) = &-\sigma_4 \left(\frac{V_1\,(\sigma_1 - 1)}{R} + \frac{\mathrm{e}^{\frac{T_s\,(g-w)}{\mathrm{tau}}}\,(V_2 - V_1\,\sigma_1 + V_1\,\sigma_3 - V_2\,\sigma_2)}{R\,(\sigma_1 + \sigma_3)} \right) \\
&- \frac{(\sigma_4 - 1)\,(V_1 - V_2)}{R}
\end{aligned}
\tag{2.80}
$$

where

$$
\begin{aligned}
\sigma_1 &= e^{-\frac{T_s\,(w-g)}{\tau}} \\
\sigma_2 &= e^{-\frac{T_s\,(w-0.5)}{\tau}} \\
\sigma_3 &= e^{-\frac{T_s\,(w-g-0.5)}{\tau}} \\
\sigma_4 &= e^{-\frac{T_s\,(0.5-w)}{\tau}}
\end{aligned}
\tag{2.81}
$$

The power transferred on the primary side is calculated by

$$
\begin{aligned}
P_{1,\Delta} = \frac{2\,V_1}{T_s} \Bigg(&-\int_0^{(w-g)\,T_s} i_L(t_0)\,e^{-\frac{t}{\tau}} + \frac{V_1 + V_2}{R}\left(1 - e^{-\frac{t}{\tau}}\right)\mathrm{d}t \\
&+ \int_0^{(0.5-w)\,T_s} i_L(t_1)\,e^{-\frac{t}{\tau}} + \frac{V_1 - V_2}{R}\left(1 - e^{-\frac{t}{\tau}}\right)\mathrm{d}t \\
&+ \int_0^{g\,T_s} i_L(t_2)\,e^{-\frac{t}{\tau}} + \frac{V_1 - V_2}{R}\left(1 - e^{-\frac{t}{\tau}}\right)\mathrm{d}t \Bigg)
\end{aligned}
\tag{2.82}
$$

and on the secondary side by:

$$
P_{2,\Delta} = \frac{2\,V_2}{T_s}\left(\int_0^{(0.5-w)\,T_s} i_L(t_1)\,e^{-\frac{t}{\tau}} + \frac{V_1 - V_2}{R}\left(1 - e^{-\frac{t}{\tau}}\right)\mathrm{d}t \right)
\tag{2.83}
$$

The inductor RMS current can finally be calculated as follows:

$$
I_{L,RMS} = \sqrt{\frac{2}{T_s}\left(\int_0^{(w-g)\,T_s} i_L^2(t)\,\mathrm{d}t + \int_{(w-g)\,T_s}^{g\,T_s} i_L^2(t)\,\mathrm{d}t + \int_{g\,T_s}^{T_s/2} i_L^2(t)\,\mathrm{d}t \right)}
\tag{2.84}
$$

Combined Modulation Scheme

The optimal solution of the combined modulation scheme of the lossless DAB converter was derived in 2.3. In the enhanced model, that considers the conduction losses, the inductor current at the switching transitions t_0, t_1 and t_2, the inductor RMS current $I_{L,RMS}$ and most important the transferred output power P_2 differ from the lossless model. Hence the optimal solution in regard to the transferred output power is revisited.

To minimise the inductor RMS current, analytical expressions of the transferred power P_1, P_2 and the inductor RMS current $I_{L,RMS}$ in relation to the control parameters g, w have to exist. Moreover, an analytical expression of the phase-shift g, required to transfer a desired output power level P_2, has to exist to perform the optimisation algorithm.

For the conventional phase-shift modulation and the one-sided clamped modulation scheme with $g > 0$ no closed-form solution of the phase-shift g to transfer a desired power level exists. For the one-sided clamped modulation scheme with $g < 0$ however a closed form solution can be derived with respect to g to transfer a desired power level. For all three modulation schemes (one-sided clamped Case I and II and conventional PSM) in the combined modulation scheme analytical expressions of the transferred power P_1, P_2 and the inductor RMS current $I_{L,RMS}$ exist and can be calculated with (2.65), (2.68), (2.69), (2.77), (2.75), (2.76), (2.84), (2.82) and (2.83).

To revise the optimization with respect to the minimum inductor RMS current the optimization of the one-sided clamped modulation scheme with $g < 0$ is conducted as described in Section 2.3 as a closed form solution of the phase-shift $g \in [-0.25; 0]$ in relation to the transferred output power $P_2 \in [0, P_{\Delta;max}]$ exists.

The optimisation for the one-sided clamped modulation scheme with $g > 0$ and $P_2 \in [P_{\Delta,max}; P_{PS,min}]$ and for the conventional phase-shift modulation with $g > 0$ and $P_2 > P_{PS,min}$ cannot be conducted as described in Section 2.3 as no closed form solution for the phase-shift g exists. The optimal set of parameters are calculated as follows: The transferred output power P_2 and the corresponding inductor RMS current from all possible combinations of the phase-shift $g \in [0, 0.25]$ and clamping interval $w \in [0, 0.5]$ are calculated. The set of modulation parameters that minimize the inductor RMS current at a specific transferred power are then extracted from the calculated data. Figure 2.26 depicts the optimal control parameters g, w_1 and w_2 in relation to the transferred output power P_2.

It is evident that no discontinuity of the control parameters is present and hence a seamless transition between the individual modulations schemes of the combined modulation scheme still is possible. Measurements show that the higher the transferred power, the lesser the change of the clamping time interval w affects the converter efficiency. Hence the converter efficiency only minimal decreased if the clamping time interval w varies slightly from the optimal value. During the low power region, when the one-sided modulation scheme with $g < 0$ is applicable, an error in the clamping interval w has, however, a significant effect on the converter efficiency. Figure 2.27 depicts the inductor current at the switching times t_0, t_1 and t_2. It is evident that when compared to the optimal solution of the lossless model (cf. Figure 2.18), the transferred output power decreases, due to the conduction losses. Furthermore a slight increase in the inductor current is present.

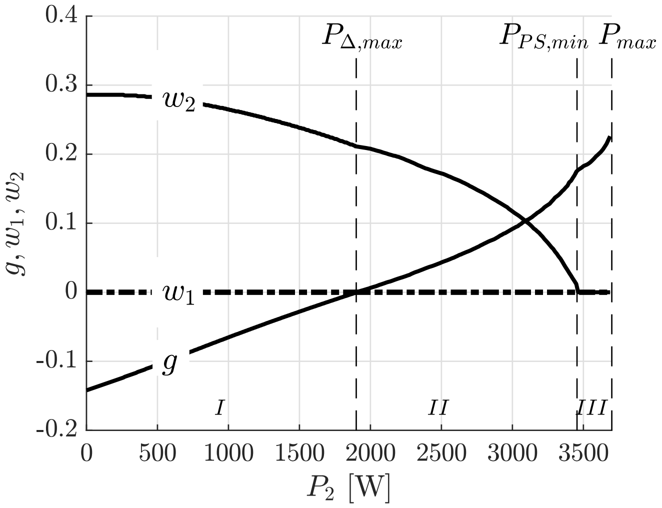


Fig. 2.26.: Optimal clamping intervals w_1, w_2 of the combined modulation scheme with conduction losses in relation to the transferred power P_2, $V_1 = 138\,\text{V}$, $V_2 = 230\,\text{V}, R = 350\,\text{m}\Omega, L = 24\,\mu\text{H}, n = 1$ and $f_s = 40\,\text{kHz}$. Region I denotes $g < 0$ and Region II denotes $g > 0$ of the one-sided clamped modulation. Region III refers to the phase-shift modulation with $w_1 = w_2 = 0$.

2.5. Conclusion

The working principle of a DC/DC DAB converter is explained in this Chapter, and the different modulation parameters are detailed. Various modulation schemes are examined, and a combined modulation scheme is proposed in Section 2.3, optimising the steady-state operation of a DAB converter's efficiency by minimising the inductor RMS current. Two different converter description models are detailed. The lossless DAB model that enables the simplified calculation of transformer current and the transferred power and by which the optimal parameters of the combined modulation scheme are derived. The lossless model is expanded by considering the conduction losses. The effect on the modulation schemes and the transferred power is described, and the combined modulation parameters w_1, w_2 and g accounting for conduction losses are derived in Section 2.4.1.

The presented models facilitate the calculation of the transformer RMS and instantaneous currents. The combined modulation scheme reduces the transformer RMS

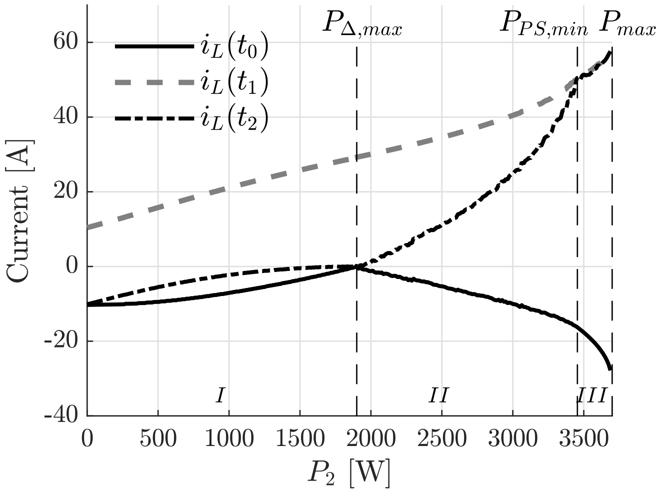


Fig. 2.27.: Inductor current at the switching times t_0, t_1 and t_2 in relation to the transferred output power P_2, $V_1 = 138\,\mathrm{V}$, $V_2 = 230\,\mathrm{V}, R = 350\,\mathrm{m\Omega}, L = 24\,\mathrm{\mu H}, n = 1$ and $f_s = 40\,\mathrm{kHz}$. Region I denotes $g < 0$ and Region II denotes $g > 0$ of the one-sided clamped modulation. Region III refers to the phase-shift modulation.

current and extends the ZVS range of the DAB converter down to no load. The derived combined modulation scheme's parameters form the basis of the modulation of the 5kVA Prototype detailed in Chapter 6.

3. Switching of a MOSFET

The design target of modern power converters is to offer a higher power density and a faster transient response, which is ultimately achieved by high-frequency operation of the power converter. The increase in operating frequency creates two significant difficulties, namely high switching stress and switching loss. The presence of parasitic stray inductances in the power path and the output capacitance C_{oss} of the semiconductor devices result in an inductive turn-off and a capacitive turn-on of the switched semiconductor device. Furthermore, the reverse-recovery-charge present in diodes exerts further switching stress on the semiconductor device, if the current is commutated off a conducting diode at turn-on. When the semiconductor switches off an inductive load, the high di/dt across the leakage inductances induce voltage spikes across the semiconductor. When on the other hand, the switch is turned on at high voltages the discharging of the output capacitance of the complementary semiconductor and the reverse-recovery-current of the diode results in a current spike added to the switched inductor current. Additionally, the energy stored in the output capacitance ($^1/_2 C V^2$) of the turned-on device is trapped and dissipated inside the device [41]. Furthermore turning the semiconductor device on under high voltages induces severe switching noise known as the Miller effect, which is coupled into the drive circuitry [41].

To safely increase the operating frequency, the switching loss energy and consequently, the switching losses have to be minimised. This is achieved through resonant switching, whereby the power electronic switch is turned in favourable conditions on and/or off; ether at zero-current or zero-voltage.

The zero-current-switching (ZCS) technique [42] has proven to achieve high-frequency operation of quasi-resonant converters [43] [44] [45]. The current is shaped by a resonant LC network and creates a zero-current condition for the switch to turn on and off. Although the zero-current-switched quasi-resonant converters seemed to be promising in high-frequency operating, several limitations exist [46]. Namely the undesired capacitive turn-on losses associated with the output capacitance's stored energy dissipated inside the device, the higher VA ratings of the components [47] and the reduced switching frequency at light loads [47].

The zero-voltage-switching (ZVS) technique proposed in [41] proved to overcome the limitations of the ZCS technique by shaping the semiconductor device's voltage so, that the voltage decreases to zero before turn-on. Zero-voltage-switched quasi-resonant converters proved to increase the operating frequency compared to the zero-current-switched quasi-resonant converter [46] [48].

In this Section, the switching transitions of a DAB converter are described. First, the switching transition of a half-bridge circuit with MOSFET semiconductor devices is described under ideal conditions. After that, the additional switching stress inflicted by the reverse recovery of the diode and the output capacitance is introduced, and the effects on the switching transition are examined. Then the switching losses generated during a switching transition are discussed. Firstly the hard switching transition is examined and secondly the resonant switching transition of a DC/DC DAB converter with MOSFETs illustrated in Figure 2.19 (cf. Chapter 2) are analysed. The switching transitions of named converter operated under phase-shift modulation are described. After that, the effect of the advanced modulation schemes on the resonant switching behaviour is analysed.

3.1. Switching Transient of a MOSFET

Half-bridge circuits consisting of two semiconductor switches with anti-parallel diodes are extensively used in modern power applications. Full-bridge circuits utilised in the DAB-converter covered in Chapter 2 consist of two paralleled half-bridge circuits pulsed diagonally and hence each half-bridge circuit can be analysed independently. In this Section the inductive switching transient of a half-bridge circuit consisting of MOSFETs is analysed, and the waveforms of gate-source voltage v_{GS}, the drain-source voltage v_{DS} and lastly the drain current i_D are explained.

3.1.1. Ideal Switching Transient

Figure 3.1 shows the half-bridge circuit consisting of MOSFETs with intrinsic anti-parallel diodes. To better describe the inductive turn-on and turn-off transient of the device under test (DUT) (the low-side MOSFET T_{LS}), in a first step the additional switching stress inflected by the high-side MOSFET and the parasitic inductance in the power path is neglected [1]. Hence the high side MOSFET is treated as an ideal diode. In Section 3.1.2 the added switching stress evoked by the reverse recovery charge Q_{rr} of the diode and the capacitive charging current of the output capacitance C_{oss} is described.

To describe the switching transient of a MOSFET and the losses generated during the process, its parasitic capacitors and the charge associated therewith have to be considered first. To fully describe its switching behaviour it is wise to consider

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[1] the parasitic capacitances of the MOSFET being turned on have to be considered to describe the switching process of the device itself

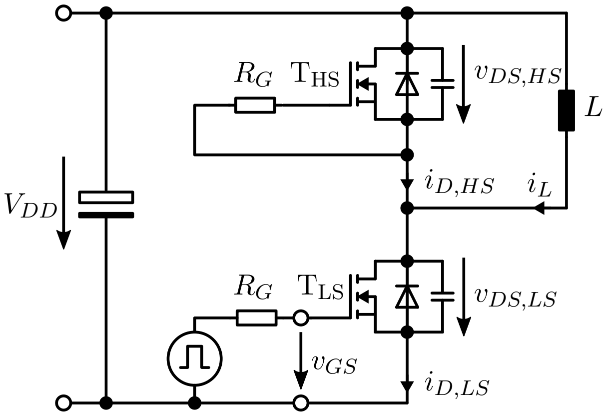


Fig. 3.1.: Half-bridge circuit with MOSFETs

the device in isolation neglecting any external influences [49]. Figure 3.2 depicts a MOSFET with its gate-source, gate-drain and drain-source capacitances. Unlike bipolar transistors, MOSFETs are voltage driven components and therefore it is often assumed, that applying a gate voltage above the threshold voltage ($v_{GS} > V_{GS(th)}$) turns the MOSFET on and results in a change of the $R_{DS(on)}$ from high to low which is specified in the MOSFET's data sheet. But the transition from the off-state to the on-state or vice versa is more complex and should be considered as a process rather than an event [50]. The transition process can best be explained by the gate charge curve shown in Figure 3.3a. The segmented and linearized gate charge curve represents a superposition of two capacitors which are non-linear, have different values, are not connected in parallel and are charged to different voltage levels [50]. The effective capacitance seen from the gate terminal is defined as:

$$C_{iss} = C_{gs} + C_{gd} \tag{3.1}$$

It should be noted that C_{iss} (cf. Figure 3.3b) is not a physical capacitance and the switching transient can not simply be described by applying a voltage to C_{iss}. As mentioned before the turn-on process can be described by the charges associated with C_{iss}.

Figure 3.4 depicts the inductive turn-on transient of the low-side MOSFET (cf. Figure 3.1). Prior to turn on ($t < t_0$) the gate-source capacitance C_{gs} is uncharged and the gate-drain capacitance C_{gd} is charged to $-V_{DD}$ and hence carries a negative charge which has to be removed during the switching transition. At $t = t_0$ a voltage is applied to the gate terminal. During $t_0 < t \leq t_1$ the gate-source capacitance C_{gs} is charged from $0V$ to the threshold voltage $V_{GS(th)}$. No change in drain-source voltage v_{DS} and drain current i_D occurs. At $t = t_1$ the drain current i_D begins to rise and reaches its maximum at $t = t_2$ which is equal to the load current I_L. The gate-source voltage v_{GS} rises to the plateau voltage $V_{plateau}$. After i_D reaches its maximum the

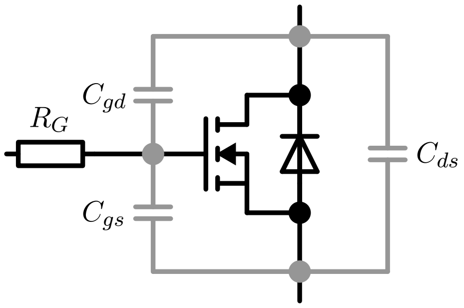
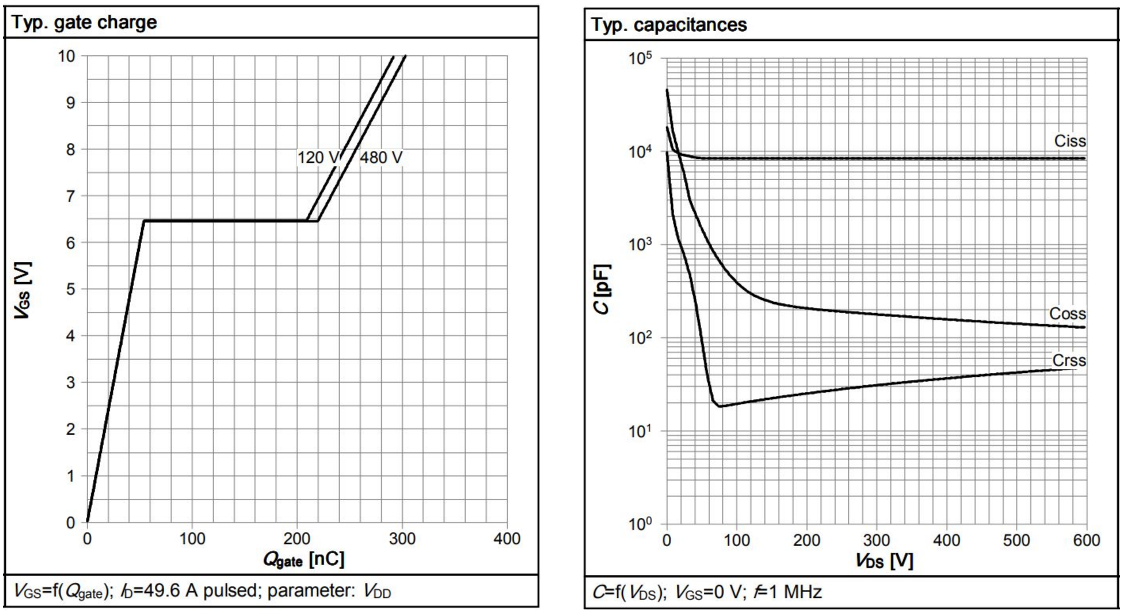


Fig. 3.2.: Parasitic Capacitances C_{gd}, C_{gs} and C_{ds} of a MOSFET



(a) Typical gate charge Q_g with V_{DD} as a parameter

(b) Typical capacitances C_{iss}, C_{oss} and C_{rss}

Fig. 3.3.: Typical gate charge and capacitances of the Infineon IPW65R041CFD extracted from the data sheet

drain-source voltage v_{DS} starts to fall with $t > t_2$ displacing the negative charge of C_{gd} through the gate. While v_{DS} falls from V_{DD} to almost zero the gate-source voltage v_{GS} forms a plateau known as the Miller Plateau, which results from the constant displacement current from C_{gd} and is limited by the gate drive circuitry. At $t = t_3$ after v_{DS} has fallen near to zero the gate-source voltage v_{GS} rises from $V_{plateau}$ to the voltage applied to the gate terminal V_{GS}. During this process the effective on-resistance $R_{DS(on)}$ reduces marginally whereas very little change in v_{DS} occurs and the MOSFET is in its on-state and the transition process is completed.

The turn-off process of a MOSFET shown in Figure 3.5 can be analysed in a similar

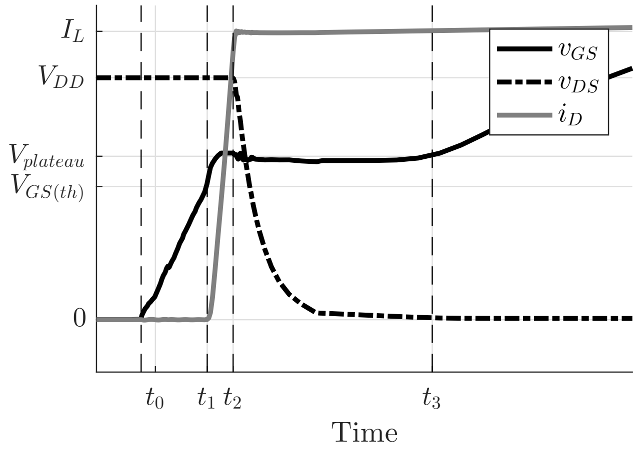


Fig. 3.4.: Simplified turn-on transient of a MOSFET neglecting the parasitic effects of the complementary MOSFETs in the half-bridge circuit

manner, where the same two charges have to be removed from or applied to the gate in reverse order.

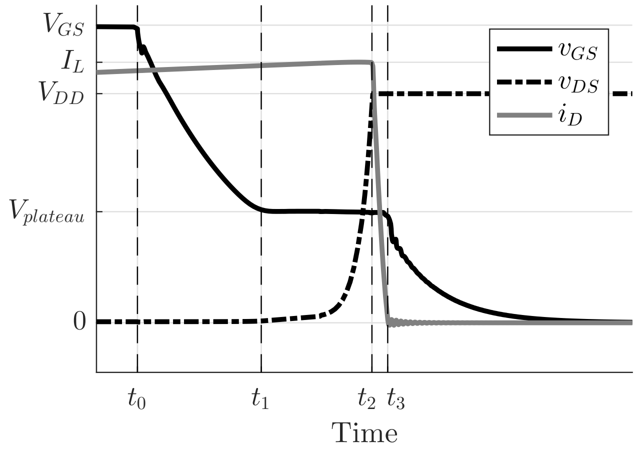


Fig. 3.5.: Simplified turn-off transient of a MOSFET neglecting the parasitic effects of the complementary MOSFETs in the half-bridge circuit

It should be noted that the sum of Q_{gs} and Q_{gd} guarantee the MOSFET to turn on completely, but the gate charge does not guarantee how fast [50]. The slope of voltage and current during transition is determined by the rate at which the gate charges are removed or applied, which is solely a function of the magnitude of the gate current.

3.1.2. Reverse Recovery of Diode

Two phenomena neglected in the above description exert additional stress on the semiconductor devices during a switching transition, namely the reverse recovery of the diode and the output capacitance C_{oss} of the MOSFET.

The reverse recovery of a silicon-based diode occurs, when the diode is forward biased carrying a positive current $I_F > 0$ when the diode is turned off. When the diode transitions from the conducting state to the blocking state, the charge distribution of the p-n junction has to change [51]. The flooded depletion region has to recombine to regain the ability to block voltage. Furthermore, the charge stored in the output capacitance Q_{oss} has to be removed. These movements of charge induce a negative flow of current.

Figure 3.6 depicts the diode recovery waveform [52] defining the reverse recovery process of a diode. Initially, the diode is forward biased and is carrying a positive forward current. After the gate-source voltage v_{GS} of the low-side MOSFET reaches the threshold voltage, the turn off process of the diode is started. The diode current rolls off with a constant slope (di_F/dt) until the current reaches zero. Due to the recombination of the depletion area, the current reverses its direction. After reaching its maximum I_{rrm}, the drain-source voltage v_{DS} starts to rise until it reaches its maximum $V_{DS,max}$ and the reverse current i_{rr} falls back to zero with the slope di_{rr}/dt completing the reverse recovery process. After completion, the diode regains its ability block voltage and returns to its blocking state.

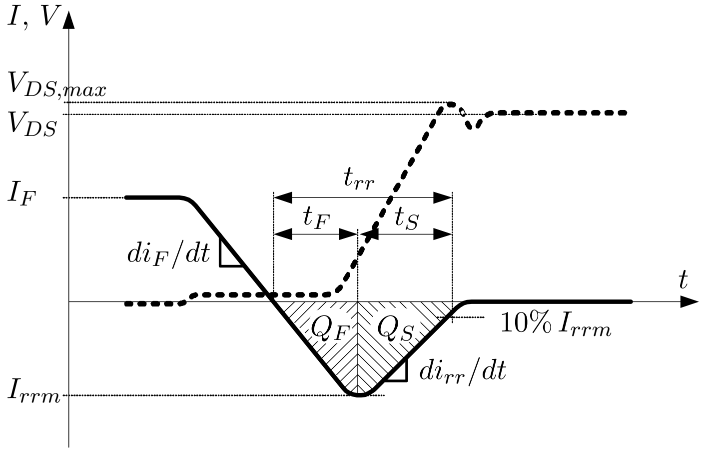


Fig. 3.6.: Reverse recovery of a diode [52]

The reverse recovery charge Q_{rr} is defined by the area under the negative current waveform and the time for the diode to reverse recover and is measured as shown in

Figure 3.6. It follows:

$$\begin{aligned} Q_{rr} &= Q_F + Q_S \\ t_{rr} &= t_F + t_R \end{aligned} \tag{3.2}$$

It should be noted, that the area under the negative current curve contains both the reverse recovery charge Q_{rr} and the charge associated with the output capacitance Q_{oss} of the MOSFET. It is difficult to distinguish what portion of the area is attributed to the reverse recovery as no physical indication exists to indicate when the recombination process completes [52]. [53] shows that the contribution of Q_{oss} is not negligible, but that the current for removing the charge exerts additional stress on the device turned on.

3.1.3. Real Switching Transition

Figure 3.7 shows a simulated switching transition of a half-bridge circuit with two MOSFETs depicted in Figure 3.1. The Figure shows the drain-source voltage v_{DS} and drain current i_D of the high-side MOSFET T_{HS} and of the low-side MOSFET T_{LS} respectively. The forward current of the intrinsic diode of the high-side MOSFET is given as:

$$i_F = -i_{D,HS} \tag{3.3}$$

The gate of the high-side MOSFET of the half bridge circuit depicted in Figure 3.1 is tied to the source forcing the current for flow through the intrinsic diode rather than the channel. Figure 3.7 shows the turn-off transition of the intrinsic diode of the high-side MOSFET and the turn-on transition of the low-side MOSFET under real conditions. Prior to the switching transition ($t < t_0$) the low-side MOSFET is turned off. The inductor current forces the current to flow through the high-side diode and the output capacitance $C_{oss,HS}$ is discharged. At $t = t_0$ the twitching transition process is initiated. As described in Section 3.1.2 the diode current rolls off with a constant di/dt and reverses its direction and reaches its maximum at $t = t_2$. In a half-bridge configuration the direction of the reverse recovery current is in the same direction as the drain current of the low-side MOSFET resulting in a shoot through [52]. Consequently the low-side drain current $i_{D,LS}$ does rise above the inductor current i_L ($t = t_1$) to reach the maximum at $t = t_2$ and it follows:

$$I_{D,max} = I_L + I_{rrm} \tag{3.4}$$

Thereafter the diode current falls back to zero and the low-side drain current carries the inductor current only completing the switching transition at $t = t_3$.

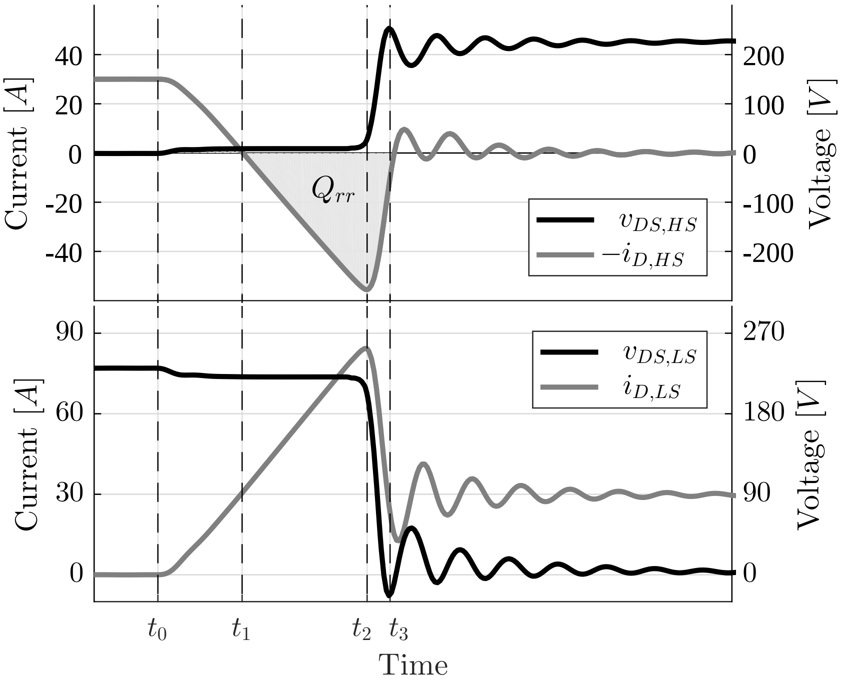


Fig. 3.7.: Simulated real switching transition of a half-bridge circuit with two IPW65R041CFD MOSFETs

3.2. Switching Transitions

3.2.1. Hard Switching

A switching transition, being turn-on or turn-off, is defined as hard when an overlap between drain-source voltage v_{DS} and drain current i_D occurs. The overlap in voltage and current leads to power dissipated in the semiconductor device. The instantaneous power of the transistor p_T is defined by:

$$p_{sw}(t) = v_{DS}(t)\, i_D(t) \tag{3.5}$$

The switching loss energy is defined by the area of the instantaneous loss power and is given by

$$E_{sw} = \int_{t_0}^{t_1} p(t)\, \mathrm{d}t \tag{3.6}$$

with t_0 defining the start and t_1 the end of the switching transition, being either turn-on or turn-off respectively. The average switching losses of the power electronic device can ultimately be calculated by multiplying the switching loss energy E_{sw} by the switching frequency f_s.

$$P_{sw} = E_{sw}\, f_s \tag{3.7}$$

Figure 3.8 shows the hard turn-on transient of a MOSFET in a half-bridge circuit (cf. Figure 3.1) when commutating off an ideal diode (*ideal* substript, described in Section 3.1.1) and when commutating off a the intrinsic diode of a IPW65R041CFD MOSFET (*real* substript, described in Section 3.1.3). The top waveforms show the drain-source voltage v_{DS} and the drain current i_D. The bottom depicts the instantaneous power p_{on} dissipated in during the switching process and the shaded area reflects the turn-on loss energy E_{on}. It is apparent that the real loss energy is much greater, which is caused by the reverse recovery of the intrinsic diode and the output capacitance of the MOSFET. Thus the greater deal of the switching losses of the switched semiconductor device are inflicted by the parasitic elements of the turned off device, rather than the switching of device itself.

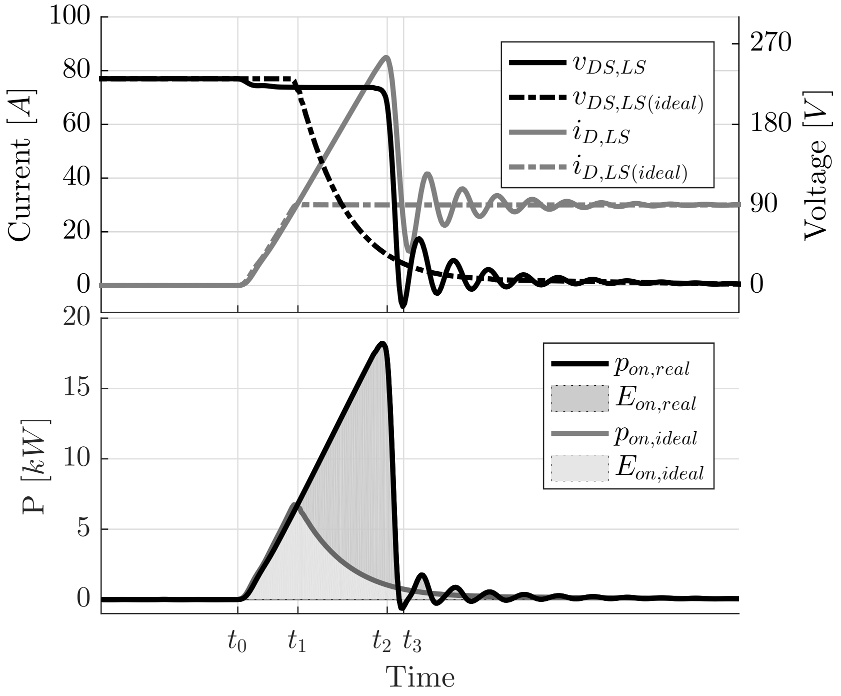


Fig. 3.8.: Comparison of the simulated turn-on transient of a MOSFET commutating of an ideal diode and and a real intrinsic diode of a IPW65R041CFD MOSFET

The hard switching transition exerts additional switching loss and switching stress on the semiconductor devices, which limits the design target of modern power converters. Due to the high losses and the reverse recovery time of the intrinsic diode the operating frequency is limited [54] which ultimately limits the achievable power density.

3.2.2. Resonant Switching

The benefits of ZVS are virtually no switching losses on turn-on transitions which leads to high converter efficiency even at high switching frequencies. Further, due to the resonant charging of the parasitic capacitances during the dead-time t_d, the gradient of the voltage rise is reduced. A lower dv/dt leads consequently to reduced ringing caused by parasitic components and a better high-frequency EMI. Furthermore, the parasitic circuit components, in the form of the stray inductance of the transformer and the output capacitance of the MOSFETs can be utilised. As the output capacitance is discharged during the resonant transition, no current spikes and no losses attributed to its discharging occur. Lastly, lower requirements for gate drive circuitry are needed, because the miller-effect caused by the gate-drain capacitance C_{DS} does not occur.

A switching transition is defined as soft when no overlap in voltage and current is present. This can be achieved by forcing the drain-source voltage v_{DS} to zero prior to turning on the device. The soft switching transition of a DAB converter and the conditions to achieve ZVS are described below.

Phase-Shift Modulation

A typical ZVS transition of a phase-shift modulated DAB converter is illustrated in Figures 3.10a to 3.10d. The switching operation depicts the transition of the secondary bridge voltage v_{ac2} from $-V_2$ to $+V_2$. As the switching duration is small compared to the conducting period of one cycle ($t_d << T_s/2$), the primary side is assumed to be constant during the shown switching operation. Therefore only the switching transition of the secondary full-bridge circuit is analysed in Figure 3.10. The corresponding voltage and current waveforms are shown in Figure 3.9.

During $t < t_0$ MOSFETs T_6 and T_7 are turned on and T_5 and T_8 are off (Figure 3.10a) applying a negative voltage to the reactive network. The inductor current i_L flows in positive direction causing a positive current flow (with respect to the anti-parallel body-diode) through T_6 and T_7. The body-diodes of T_5 and T_8 are reverse biased and therefore the voltage across their output capacitance is equal to V_2.

At $t = t_0$ the switching transition starts when MOSFETs T_6 and T_7 are turned off. The inductor forces the current to commutate from the conducting channels of T_6 and T_7 to the output capacitances C_{oss} of the MOSFETs of the secondary full-bridge circuit. Consequently, the charging the output capacitances causes the voltage across T_6 and T_7 to rise and the voltage across T_5 and T_8 to fall. The output capacitor is disconnected; consequently, no power is transferred.

When the output capacitance of T_5 and T_8 is discharged below the threshold voltage of the body-diodes, the current forward biases the body-diodes of T_5 and T_8 and they

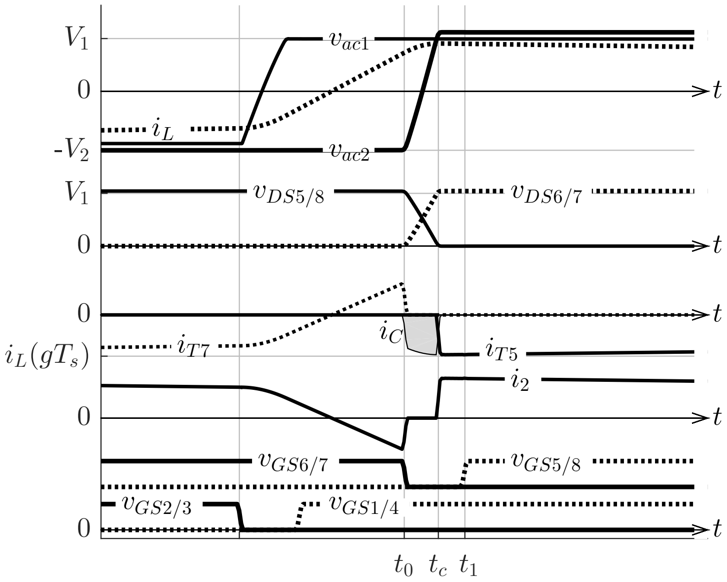


Fig. 3.9.: Current and voltage waveforms of ZVS operation sequence of the conventional phase-shit modulation

start conducting ($t = t_c$). After the dead-time (t_d) passes T_5 and T_8 are turned on with zero voltage across them at $t = t_1$. The switching transition is now completed.

During the switching interval t_0 and t_c (Figure 3.10b) the equivalent inductor and the output capacitance of the four MOSFETs (T_5 through T_8) form a resonant LC circuit. Solving the differential equations of the circuit shows, that during resonance a parallel connection of two output capacitances in series are driven resulting in an equivalent capacitance of $1\,C_{oss}$ only. The resulting equivalent LC circuit is depicted in Figure 3.11.

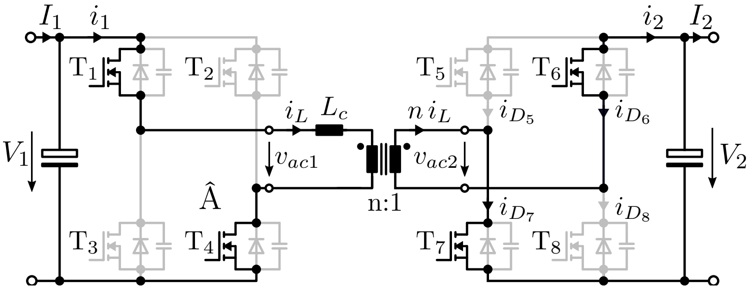
Two conditions have to be met to ensure that the MOSFETs turn on with zero voltage across them.

Condition I: To avoid hard diode commutation, the full-bridges have to be operated under forced commutation. This implies a positive current through the MOSFET channel at turn-off and has been fully described before in Chapter2.2.

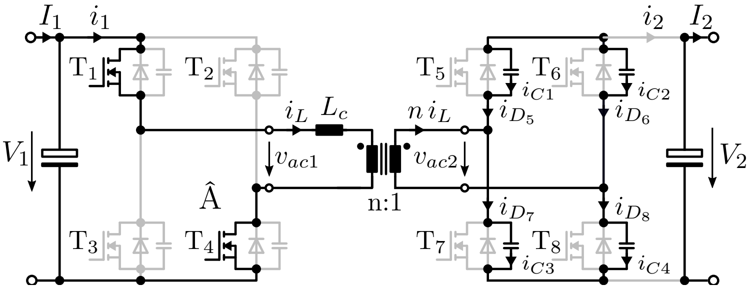
Condition II: To ensure that the switches turn on under ZVS, the energy stored in the inductor must be sufficient to completely charge and discharge the output capacitance of the four MOSFETs during the resonant transition. It follows:

$$\text{inductive Energy } E_L \geq \text{capacitive Energy } E_C \tag{3.8}$$

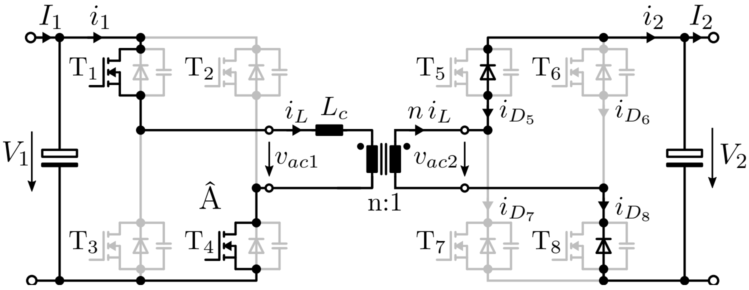
Therefore the total capacitive energy stored during the resonant transitions is given



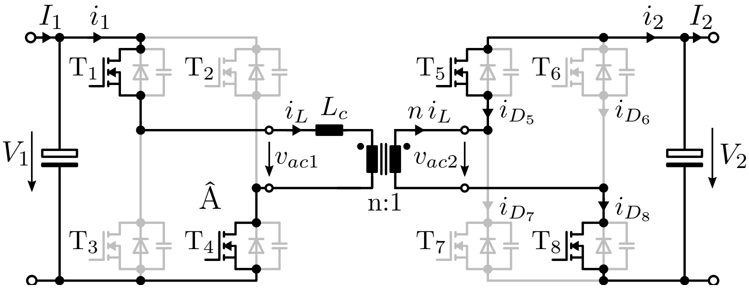
(a) During $t < t_0$ (Fig. 3.9) MOSFETs T_1 / T_4 and T_6 / T_7 conduct yielding $v_{ac1} > 0$, $v_{ac2} < 0$ and $i_L > 0$



(b) At $t = t_0$ (Fig. 3.9) MOSFETs T_6 and T_7 are turned OFF. The inductor forces the current to flow further discharging C_{oss} of T_5 and T_8 and charging C_{oss} of T_6 and T_7



(c) At $t = t_c$ (Fig. 3.9) the drain-source voltages of T_5 and T_8 fall below the threshold voltage of the body-diodes. The body-diodes of T_5 and T_8 become forward-biased and start conducting.



(d) At $t = t_1$ (Fig. 3.9) T_5 and T_8 are turned ON with ZVS

Fig. 3.10.: ZVS transition of the phase-shift modulation

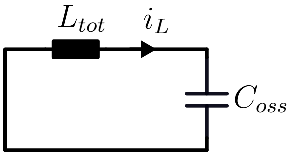


Fig. 3.11.: Resonant LC circuit formed during ZVS transition of the conventional phase-shift modulation

by

$$E_C(t) = \frac{1}{2}\, C_{oss}\, v_{DS}^2(t) \tag{3.9}$$

and the total available inductive energy at the switching transition holds:

$$E_L = \frac{1}{2}\, L_{eq}\, i_L^2(t) \tag{3.10}$$

To warrant zero-voltage turn on of the primary full-bridge's MOSFETs, Condition (3.8) can be rewritten to

$$L_{eq}\, i_L^2(t_0) \geq C_{oss(prim)}\, V_1^2 \tag{3.11}$$

and (3.8) holds for the secondary full-bridge:

$$L_{eq}\, n^2\, i_L^2(t_0 + gT_s) \geq C_{oss(sec)}\, V_2^2 \tag{3.12}$$

To guarantee sufficient inductive energy during the resonant transition, a minimum commutation current $I_{c,min}$ is needed and it holds for Condition II:

$$\begin{aligned} I_{c,min(prim)} &= \sqrt{\frac{C_{eq(prim)}}{L_{tot}}}\, V_1 \qquad \text{and} \\ I_{c,min(sec)} &= \sqrt{\frac{C_{eq(sec)}}{L_{tot}}}\, V_2 \end{aligned} \tag{3.13}$$

with

$$\begin{aligned} C_{eq(prim)} &= C_{oss(prim)} \qquad \text{and} \\ C_{eq(sec)} &= C_{oss(sec)} \end{aligned} \tag{3.14}$$

By inserting (3.13) into (2.22) and (2.23) the constraints that define the zero-voltage switching boundaries can be updated and it follows:

$$i_L(t_0) \leq -I_{c,min(prim)} \tag{3.15}$$

and

$$n\,i_L(t_0 + gT_s) \geq I_{c,min(sec)} \tag{3.16}$$

Violating the constraints leads to natural commutation and the loss of ZVS of the switched semiconductor device.

It is evident that although the MOSFET body-diodes conduct during each transition, they are not subject to hard switching. The diode current is softly commutated by the channel of the parent MOSFET. However, it should be noted that the reserve recovery of the diodes has to be considered. In the interval of Figure 3.10d, the body-diode of MOSFET T_1 needs to regain its ability to block the input voltage before it is turned off. This implies that the current through T_1 has to reverse its polarity for a time needed to recover its intrinsic body-diode. If the reverse recovery process of the diode is not completed by the time T_1 is turned off, the inability of the diode to block the input voltage results in a high current though T_3 and the body-diode of T_1. This effect is commonly known as "Shoot Through" and may destroy the MOSFETs over time. Therefore MOSFETs with a fast reverse recovery body-diode and high commutation ruggedness should be chosen for resonant topologies [55]. In Chapter 7 the switching behaviour of a silicon and a silicon carbide MOSFET is analysed.

One-Sided Clamped Modulation Scheme

An typical ZVS transition of the one-sided clamped modulation scheme of a DAB converter is depicted in Figures 3.13a to 3.13d. The switching operation shows the transition of v_{ac2} from $-V_2$ to zero. Analogue to the phase-shift modulated converter the primary side is assumed to be constant ($t_d << T_s/2$) during the depicted switching transition. The corresponding voltage and current waveforms are visible in Figure 3.12.

Prior to t_0 MOSFETs T_6 and T_7 are turned on and T_5 and T_8 are off (Figure 3.13a) applying a negative voltage v_{ac2} to the reactive network. The inductor current i_L flows in positive direction causing a positive current flow (with respect to the anti-parallel body-diode) through T_6 and T_7. The body-diodes of T_5 and T_8 are reverse biased and therefore the voltage across their output capacitance is equal to V_2.

At $t = t_0$ the switching transition starts when only MOSFET T_7 are turned off. MOSFET T_6 is still conducting and thus the inductor forces the current to commutate to the output capacitances C_{oss} of MOSFET T_5 and T_7 only. Consequently the voltage across T_7 to rises and the voltage across T_5 falls. The output capacitor is disconnected; consequently, no power is transferred.

When the output capacitance of T_5 is discharged below the threshold voltage of the body-diodes, the current forward biases the body-diode of T_5 it starts conducting

($t = t_c$). After the dead-time (t_d) passes T_5 is turned on with zero voltage across it at $t = t_1$. The switching transition is now completed.

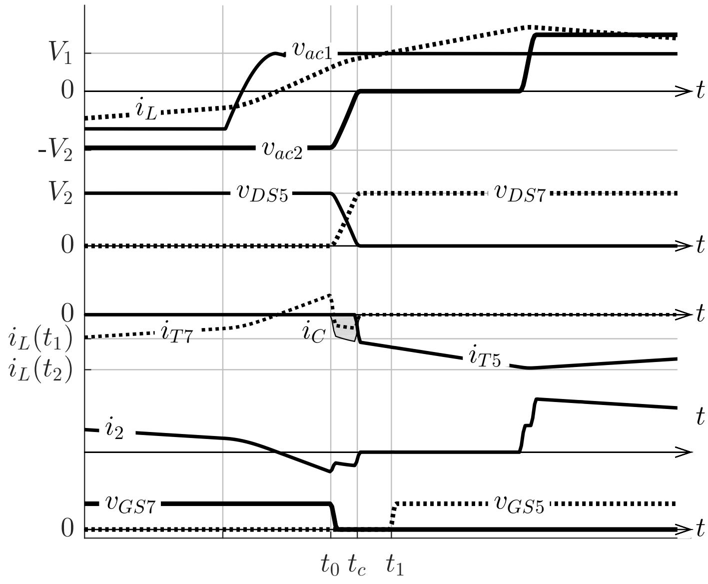


Fig. 3.12.: Current and voltage waveforms of ZVS operation sequence with the one sided-clamped modulation scheme

Figure 3.14 depicts the equivalent resonant LC circuit formed during $t_1 < t \leq t_c$. Since T_6 is not turned off during the ZVS transition only the output capacitance of T_5 and T_7 resonate with the total equivalent inductance. Therefore during the transition two output capacitances are driven in parallel which results in $2\,C_{oss}$ as the equivalent capacitance in the LC circuit.

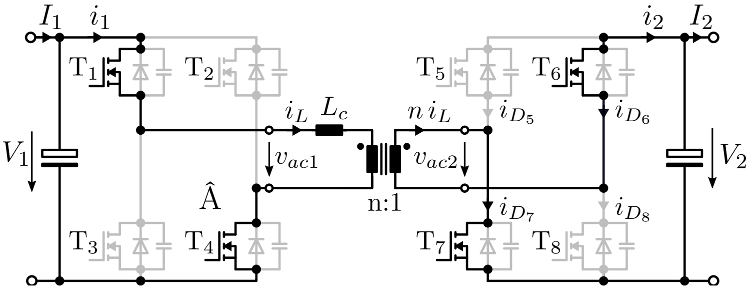
To fully warrant ZVS the minimum commutation current $I_{c,min}$ defined by Equation (3.13) can now be rewritten by inserting:

$$\begin{aligned} C_{eq(prim)} &= 2\,C_{oss(prim)} \qquad \text{and} \\ C_{eq(sec)} &= 2\,C_{oss(sec)} \end{aligned} \tag{3.17}$$

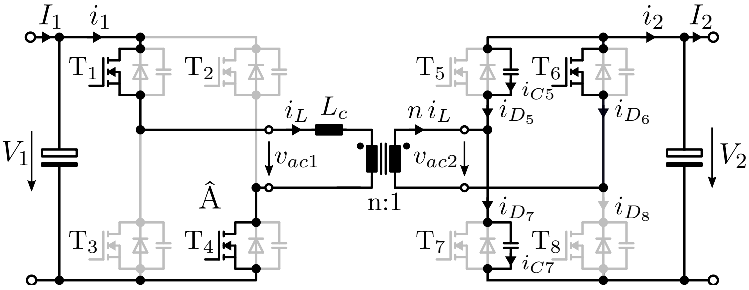
Comparing the switching transition from $v_{ac2} = -V_2$ to $v_{ac2} = +V_2$ to the transition from $v_{ac2} = -V_2$ to $v_{ac2} = 0V$ is apparent that the inductive energy needed to fully warrant the ZVS transition increases, because the equivalent resonant capacitance during resonance increases by the factor of two.

3.3. ZVS Constraints

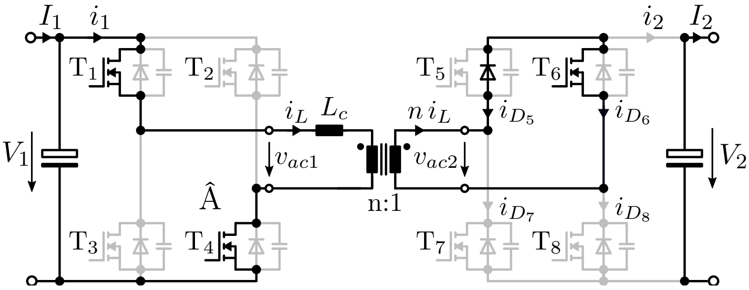
The ZVS constraints defined in Table 2.3 (cf. Section 2.3.1, assuming instantaneous voltage transitions) have to be updated. The resonant voltage transitions (caused by



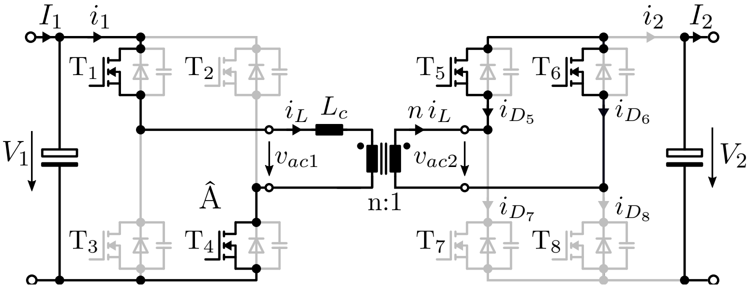
(a) During $t < t_0$ (Fig. 3.12) MOSFETs T_1 / T_4 and T_6 / T_7 conduct yielding $v_{ac1} > 0$, $v_{ac2} < 0$ and $i_L > 0$



(b) At $t = t_0$ (Fig. 3.12) MOSFET T_7 is turned OFF. The inductor forces the current to flow further discharging C_{oss} of T_5 and charging C_{oss} of T_7



(c) At $t = t_c$ (Fig. 3.12) the drain-source voltage of T_5 falls below the threshold voltage of its body-diode. The body-diode of T_5 becomes forward-biased and starts conducting.



(d) At $t = t_1$ (Fig. 3.12) T_5 is turned ON with ZVS applying the zero voltage to the resonant tank

Fig. 3.13.: ZVS transition of the one-sided clamped modulation scheme

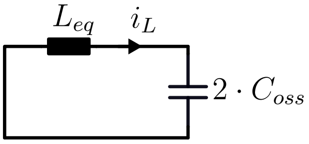


Fig. 3.14.: Resonant LC circuit formed during ZVS transition of the one-sided clamped modulation scheme

the real switching behaviour of a MOSFET) result in the updated ZVS constraints listed in Table 5.1:

Tab. 3.1.: ZVS constraints of the combined modulation scheme taking the transient voltage transitions into consideration. Regions I and II refer to the one-sided clamped modulation scheme with $g < 0$ and $g > 0$ respectively, whereas Region III the conventional phase-shift modulation denotes.

Region	ZVS Constraints		
I	$i_L(t_0) < -I_{c,min}$,	$i_L(t_1) > I_{c,min}$,	$i_L(t_2) < -I_{c,min}$
II	$i_L(t_0) < -I_{c,min}$,	$i_L(t_1) > I_{c,min}$,	$i_L(t_2) > \quad I_{c,min}$
III	$i_L(t_0) < -I_{c,min}$,	$i_L(t_1) > I_{c,min}$	

3.4. Conclusion

This Chapter describes the switching transient of a MOSFET and explains the reverse recovery effect of a diode. The additional switching loss and stress inflicted by the reverse recovery and the output capacitance of the MOSFET are mentioned. It is shown that the greater deal of the switching losses are caused by the parasitic elements of the device being turned off, rather than the switching semiconductor device itself. It furthermore is apparent that the parasitic elements limit the operating frequency of converters with half-bridge circuits when operated under hard commutation.

The advantages of resonant topologies are explained; being higher switching frequencies, lower losses and stress on the semiconductor devices. This results in higher possible power densities and higher operating efficiencies. The resonant transitions of a DAB converter modulated with the one-sided clamped modulation and the conventional phase-shift modulation are explained. The constraints for ZVS are derived for both modulation schemes and lastly, the ZVS constraints of the combined modulation scheme are updated to cater for the resonant voltage transitions.

4. AC-AC Dual Active Bridge Converter

The proposed one-stage AC-AC conversion system is based on the DC-DC DAB converter described in Chapter 2. To be able to block the voltage of both polarities and to conduct the current in both directions the transistors T_1 to T_8 (cf. Figure 2.19) are replaced by bidirectional switches to guarantee four-quadrant operation. Each transistor T_{xp} is extended by a second, anti-parallel connected transistor T_{xn} with $x \in [1; 8]$. The circuit diagram of the AC-AC DAB converter is shown in Figure 4.1. Furthermore, the electrolytic capacitors are replaced by film capacitors C_1 and C_2.

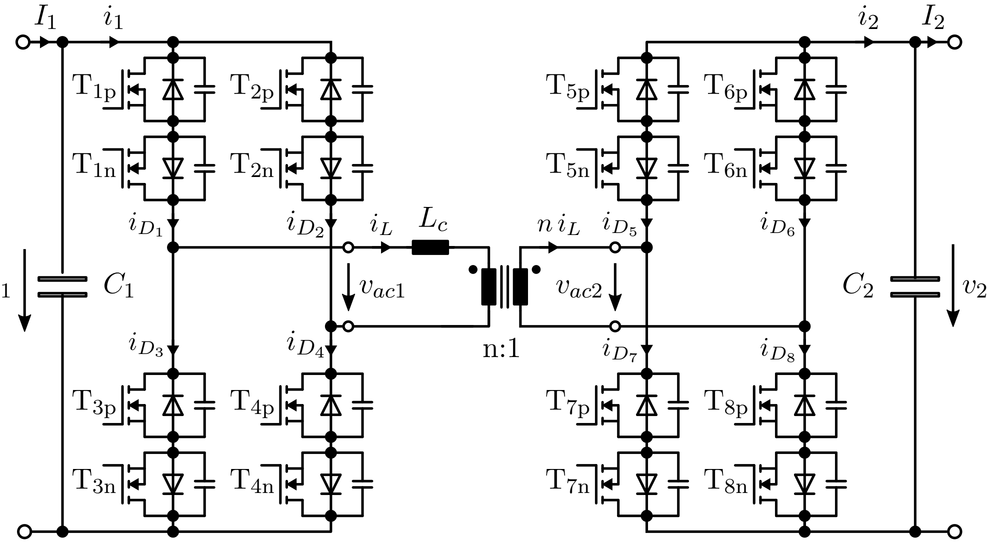


Fig. 4.1.: AC-AC Dual-Active-Bridge (DAB) converter. The DC-DC DAB converter (cf. Figure 2.19) is extended by bidirectional switches consisting of T_{xp} and T_{xn} to guarantee four-quadrant operation. T_{xp} with $x \in [1; 4]$ refers to positive input voltage v_1 and T_{xn} with $x \in [1; 4]$ to negative input voltage. T_{xp} and T_{xn} with $x \in [5; 8]$ applies for the secondary bridge accordingly.

4.1. Alternating sinusoidal voltage and current

The proposed AC-AC DAB converter is directly connected to the grid and produces an alternating voltage on the output without storing any energy along the path.

Therefore, the AC-AC DAB converter can be considered as a two-port network shown in Figure 4.2 with the time-varying input voltage $v_1(t)$, the input current $i_1(t)$, the output voltage $v_2(t)$ and the output current $i_2(t)$.

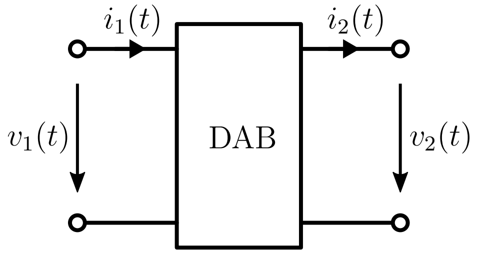


Fig. 4.2.: Two-port network

The sinusoidal voltages and currents are defined as:

$$v_1(t) = \hat{V}_1\, sin(\omega\, t + \varphi_{v1}) \tag{4.1}$$

$$i_1(t) = \hat{I}_1\, sin(\omega\, t + \varphi_{i1}) \tag{4.2}$$

$$v_2(t) = \hat{V}_2\, sin(\omega\, t + \varphi_{v2}) \tag{4.3}$$

$$i_2(t) = \hat{I}_2\, sin(\omega\, t + \varphi_{i2}) \tag{4.4}$$

The AC-AC DAB converter stores no energy during each switching cycle. Therefore, the instantaneous input and output power p_1 and p_2 are equal when the lossless DAB converter (Figure 4.5) is considered:

$$p_1(t) = p_2(t) = p(t) \tag{4.5}$$

The instantaneous power consumed by each port is given by

$$p(t) = v(t)\, i(t) \tag{4.6}$$

With Equations (A.6a) and (A.6b) the instantaneous power $p(t)$ can be rewritten to:

$$p(t) = P\,(1 + cos\, 2(\omega t + \varphi_v)) + Q\, sin\, 2(\omega t + \varphi_v) \tag{4.7}$$

The average power can furthermore be derived by averaging the instantaneous power over one cycle T and it follows:

$$\begin{aligned} \overline{p(t)} = P &= \frac{1}{T} \int_0^T p(t)\, \mathrm{d}t \\ &= V_{RMS}\, I_{RMS}\, cos(\varphi_v - \varphi_i) \end{aligned} \tag{4.8}$$

The instantaneous power oscillates with the amplitude of Q around its average value P. In the case of passive two-port networks the average value is ≥ 0. The instantaneous power $p(t)$ can however become negative during certain time intervals (cf. Figure 4.4). In these regions the passive two-port network delivers power to the source from its connected load with a capacitive or inductive storage.

Instantaneous Power

Figure 4.3 shows the two-port network with a connected load. Depending on the load the phase-shift φ_2 between the voltage and current alters and is defined by:

$$\varphi_2 = \varphi_{v2} - \varphi_{i2} \tag{4.9}$$

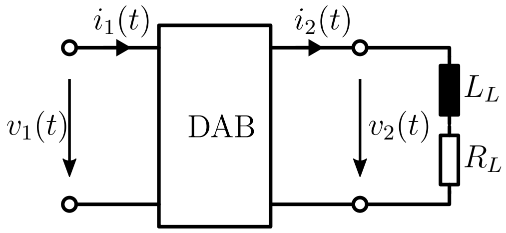


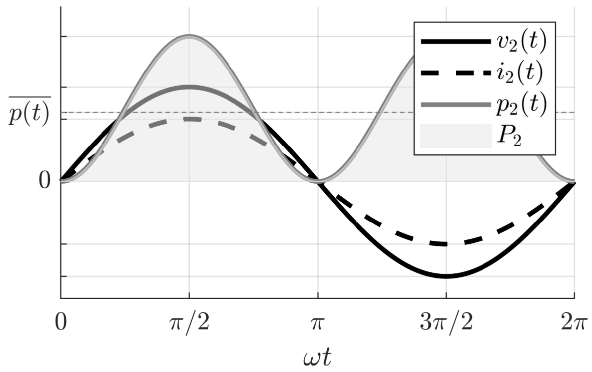
Fig. 4.3.: Two-port network with connected RL load

Active power only is transferred ($P > 0 \wedge Q = 0$) when $R_L > 0, L_L \to 0$. This results in $\varphi_2 = 0$ and thus the voltage and current are in phase. When $0 < \varphi_2 < \pi/2$ active power is transferred and reactive power is present ($P > 0 \wedge Q > 0$). With a phase-shift of $\varphi_2 = \pi/2$ ($R_L \to 0$) the average transferred power is zero and thus only reactive power is present ($P = 0 \wedge Q > 0$). Figure 4.4 shows the output voltage and current waveforms of a passive two-port network and the resulting instantaneous output power with $\varphi_2 = 0$ (Figure 4.4a), $\varphi_2 = \pi/4$ (Figure 4.4a) and $\varphi_2 = \pi/2$ (Figure 4.4a).

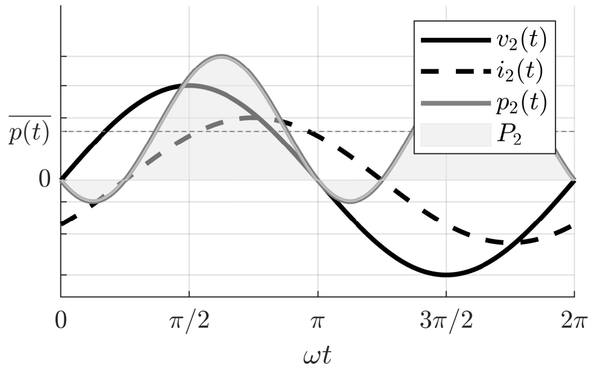
4.2. Principle of operation

The physical operation principle of the AC-AC DAB converter, depicted in Figure 4.1, is similar to the DC-DC DAB converter. The main difference is that the input and output voltages $v_1(t)$ and $v_2(t)$ are time-varying sinusoidal voltages, with

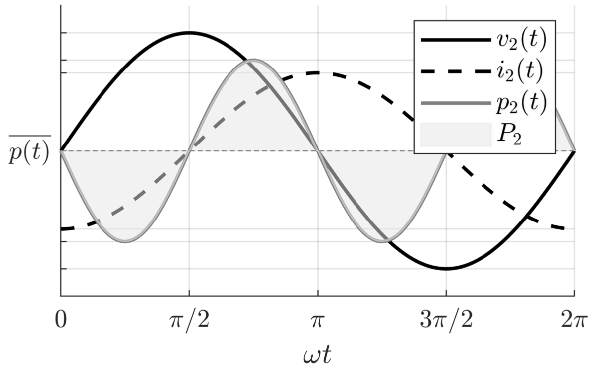
$$\begin{aligned} v_1(t) &= \hat{V}_1\, sin(\omega\, t + \varphi_{v1})) \\ v_2(t) &= \hat{V}_2\, sin(\omega\, t + \varphi_{v2}) \end{aligned} \tag{4.10}$$



(a) $\varphi_{v2} = \varphi_{i2}$



(b) $\varphi_{v2} - \varphi_{i2} = -\pi/4$



(c) $\varphi_{v2} - \varphi_{i2} = -\pi/2$

Fig. 4.4.: Current $i_2(t)$, voltage $v_2(t)$ and power $p_2(t)$ waveforms of a passive two-port network with $\varphi_{v2} = \varphi_{i2}$ (a), $\varphi_{v2} - \varphi_{i2} = \pi/4$ (b) and $\varphi_{v2} - \varphi_{i2} = \pi/2$ (c) depending on the connected load. Furthermore, the average power $\overline{p(t)}$ is depicted.

with the angular frequency ω

$$\omega = 2\,\pi\,f \qquad \text{with} \quad f = 50\,\mathrm{Hz} \tag{4.11}$$

The mains frequency f is assumed to be 50 Hz but the AC-AC DAB converter can be extended to 60 Hz operation by changes in software only.

The two full-bridge circuits generate square wave bridge voltages $v_{ac1}(t)$ and $v_{ac2}(t)$ where the amplitude is equal to the instantaneous amplitude of the alternating voltages $v_1(t)$ and $v_2(t)$ respectively. It is assumed that the bridge voltages $v_{ac1}(t)$ and $v_{ac2}(t)$ are constant during one switching period T_s as the switching frequency is much greater than the mains frequency ($f_s >> f$) and it holds:

$$\begin{aligned} v_{ac1}(t) &= v_1(t_0) = \text{const.} \\ v_{ac2}(t) &= v_2(t_0) = \text{const.} \end{aligned} \quad \text{with} \quad t \in [t_0; t_0 + T_s] \tag{4.12}$$

Hence, the AC-AC DAB converter can again be described by two voltage sources interfaced by an coupling inductor L_{eq} when all losses are neglected and assumed that the bidirectional power switches consisting of T_{xp} and T_{xn} are ideal. The resulting primary referred lossless equivalent circuit diagram of the AC-AC DAB converter is depicted in Figure 4.5. It is identical to the lossless model of the DC-DC DAB converter (cf. Figure 2.3). An inductor current is generated by changing the modulation parameters listed in Table 2.1 and thereby transferring power from the primary to the secondary side or vice versa.

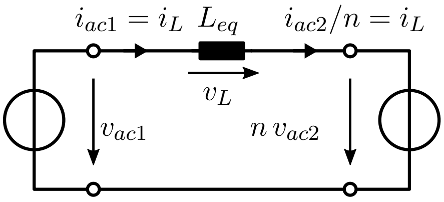


Fig. 4.5.: Primary-referred lossless equivalent circuit of a AC-AC DAB converter

4.2.1. Modulation schemes

The modulation schemes derived in Section 2.2 can be directly applied to the AC-AC operation of the DAB converter by replacing the the input and output voltages V_1 and V_2 with the time-varying sinusoidal voltages $v_1(t)$ and $v_2(t)$. It is shown in Section 4.3 that the modulation parameters are no longer constant under specific operating conditions, and thus the modulation parameters are considered to be time-dependent as well.

The time-dependent transferred power $p_{PS}(t)$ of a lossless AC-AC DAB converter modulated with the conventional phase-shift modulation can therefore be calculated by:

$$p_{PS}(t) = \frac{n\, v_1(t)\, v_2(t)\, g(t)\, (1 - 2\,|g(t)|)}{f_s\, L} \tag{4.13}$$

The transferred power of the one-sided clamped modulation scheme with $g(t) > 0$ is calculated by

$$p_{\Diamond}(t) = \frac{n\, v_1(t)\, v_2(t)\, (2\, g(t) - 4\, g(t)^2 + w(t) - 2\, w(t)^2 - 4\, g(t)\, w(t))}{2\, f_s\, L} \qquad \forall \quad g(t) > 0 \text{ and } w(t) > 0 \tag{4.14}$$

and finally the one-sided clamped modulation scheme with $g(t) \leq 0$ by:

$$p_{\Delta}(t) = \frac{n\, v_1(t)\, v_2(t)\, (2\, g(t) + w(t) - 2\, w(t)^2 - 4\, g(t)\, w(t))}{2\, f_s\, L} \qquad \forall \quad g(t) < 0 \text{ and } w(t) > 0 \tag{4.15}$$

The maximum transferable instantaneous power is given by (4.13) with $g = 0.25$ and is depicted in Figure 4.6.

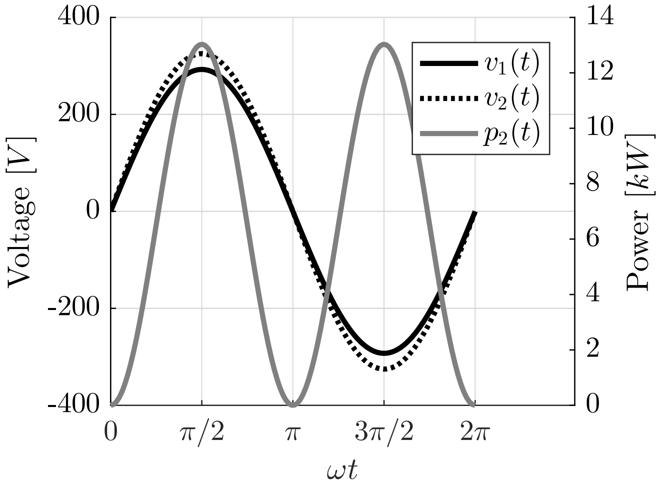


Fig. 4.6.: Transferred power of the AC-AC DAB converter with $V_{1,RMS} = 207V$, $V_{1,RMS} = 230\,\text{V}$, $L = 24\,\mu\text{H}$, $n = 1$, $f_s = 40\,\text{kHz}$, $g = 0.25$ and $\varphi_2 = 0$.

4.2.2. AC-AC DAB converter considering conduction losses

The DAB converter needs a path for the current to free-wheel during the dead-time t_d when both transistors of one bridge leg are turned off. Taking a closer look at the schematic of the AC-AC DAB converter shows that, if both switches of one bidirectional switch are modulated simultaneously, no free-wheeling path exists during t_d. Therefore the operation of AC-AC DAB converter distinguishes between the polarity of the input and output voltages $v_1(t)$ and $v_2(t)$. With a positive input voltage $v_1(t) > 0$ the transistors T_{xn} with $x \in [1;4]$ are turned on during the whole positive half-wave of the sinusoidal input voltage and the transistors T_{xp} are modulated according to the modulation schemes described in Section 2.2. The secondary Transistors are modulated accordingly depending on the polarity of the output voltage $v_2(t)$. Therefore, the AC-AC DAB converter can be described by two DC-DC converters with an additional resistance in series to each transistor. By only modulating one transistor of a bidirectional switch, the switching losses are not increased, and no additional stress is introduced on the gate drive circuitry, compared to the DC-DC operation described in Chapter 2. Figure 4.7 depicts the AC-AC operation with $v_1(t) > 0$ and $v_2(t) > 0$.

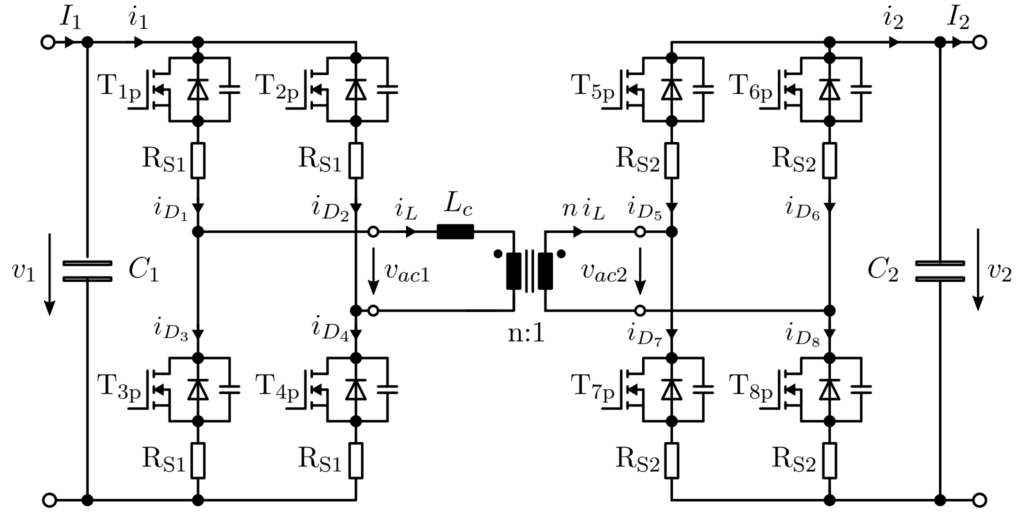


Fig. 4.7.: Operation of AC-AC DAB converter with $v_1(t) > 0$ and $v_2(t) > 0$. T_{xn} are turned on and are replaced by their on-state resistance R_S1 on the primary and R_S2 on the secondary side respectively. T_{xp} with $x \in [1;8]$ are modulated according the modulation schemes described in Section 2.2

The enhanced model considering conduction losses has to be updated to incorporate the additional MOSFETs' total on-resistance in the current path. The total resistance R of the relevant resistances of the equivalent circuit diagram shown in Figure 2.21 is hence changed to:

$$\begin{aligned} R &= R_{tot,1} + n^2 \cdot R_{tot,2} \\ &= 4 \cdot R_{S1} + R_1 + n^2 \cdot (4 \cdot R_{S2} + R_2) \end{aligned} \tag{4.16}$$

Impact on combined modulation scheme

Figure 4.8 shows the modulation parameters g, w_1 and w_2 in relation to the transferred output power P_2 with a total resistance of $R = 550\,\mathrm{m\Omega}$. It is assumed that $\varphi_2 = 0$ and thus the output voltage and output current are in phase. The corresponding inductor current at the switching times t_0, t_1 and t_2 is depicted in Figure 4.9. It is apparent that the increase in the total equivalent resistance (due to the added transistor of the bidirectional switches) decreases the maximum transferable output power. Figure 4.10 depicts the surface plot of the transferred output power P_2 in relation to the phase-shift g and the voltage ratio $1/d$ with an input voltage of $V_1 = 230\,\mathrm{V}$. It can be seen that the maximum transferable output power occurs before the maximum phase-shift of $g_{max} = 0.25$ of the lossless model. The maximum power transfer occurs at $g_{max}(R = 550\,\mathrm{m\Omega}) = 0.232$ and the phase-shift to transfer the maximum output power $P_{2,max}$ is independent on the voltage ratio $1/d$.

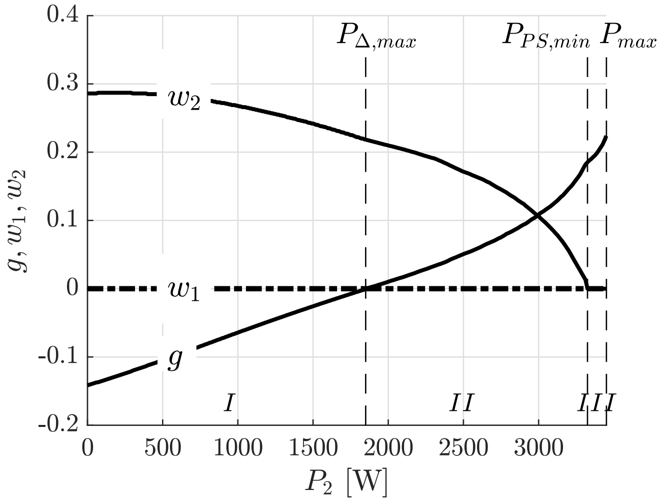


Fig. 4.8.: Modulation parameters g, w_1 and w_2 of an AC-AC operated DAB converter in relation to the transferred output power P_2 with $V_1 = 138\,\mathrm{V}, V_2 = 230\,\mathrm{V}, R = 550\,\mathrm{m\Omega}, L = 24\,\mathrm{\mu H}, n = 1$ and $f_s = 40\,\mathrm{kHz}$. Region I denotes $g < 0$ and Region II denotes $g > 0$ of the one-sided clamped modulation. Region III refers to the phase-shift modulation.

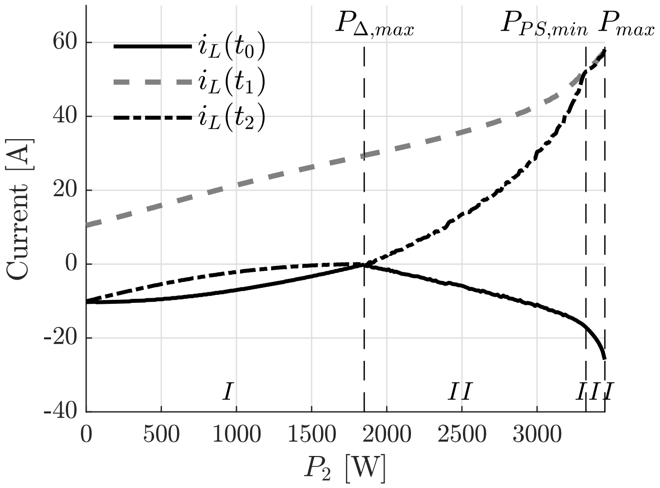


Fig. 4.9.: Inductor current of an AC-AC operated DAB converter at the switching times t_0, t_1 and t_2 in relation to the transferred output power P_2, $V_1 = 138\,\mathrm{V}, V_2 = 230\,\mathrm{V}, R = 550\,\mathrm{m\Omega}, L = 24\,\mathrm{\mu H}, n = 1$ and $f_s = 40\,\mathrm{kHz}$. Region I denotes $g < 0$ and Region II denotes $g > 0$ of the one-sided clamped modulation. Region III refers to the phase-shift modulation.

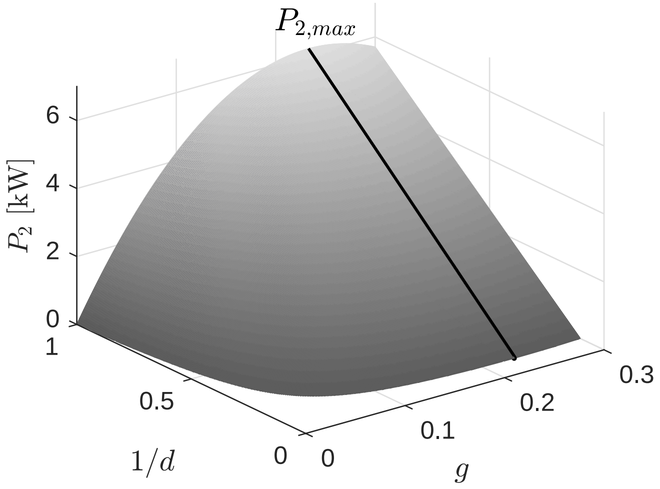


Fig. 4.10.: Transferable output power P_2 in relation to the phase-shift g and the voltage ratio $1/d$, $V_1 = 138\,\mathrm{V}, R = 550\,\mathrm{m\Omega}, L = 24\,\mathrm{\mu H}, n = 1$ and $f_s = 40\,\mathrm{kHz}$. The maximum power transfer is plotted and occurs at $g_{max}(R = 550\,m\Omega) = 0.232$ and is independent of the voltage ratio $1/d$.

4.3. AC-AC DAB Converter Operation

The AC-AC DAB converter is meant as a direct replacement for a conventional 50 Hz transformer. Therefore the operation of the AC-AC DAB converter with a power factor $\neq 1$ ($cos(\varphi_2) \neq 1$) has to be ensured.

The converter is modulated in such way that the output voltage is in phase with the input voltage and it holds:

$$\varphi_{v1} = \varphi_{v2} = 0 \tag{4.17}$$

The phase angle of the input and output current result are simplified with (4.17) to:

$$\begin{aligned} \varphi_{i1} &= \varphi_1 \\ \varphi_{i2} &= \varphi_2 \end{aligned} \tag{4.18}$$

Thus the expressions of $v_1(t)$ and $v_2(t)$ in 4.10 can be rewritten to:

$$\begin{aligned} v_1(t) &= \hat{V_1}\, sin(\omega\, t) \\ v_2(t) &= \hat{V_2}\, sin(\omega\, t) \end{aligned} \tag{4.19}$$

The operation of the converter will distinguish between two different operation modes. Firstly the real power operation ($cos(\varphi_2) = 1$) and secondly the reactive power operation. The two operating modes will be explained in detail the following Section.

4.3.1. Real Power Operation

Figure 4.11 shows the calculated waveforms of a AC-AC DAB converter under real power operation with an ohmic load connected ($R_L > 0 \wedge L = 0$) only. This results in $\varphi_2 = 0$ and thus the output voltage v_2 and output current i_2 are in phase. It is apparent that the phase-shift $g(t)$ does not change with time and it follows:

$$\begin{aligned} g(t) &= g = const. \\ w(t) &= w = const. \end{aligned} \tag{4.20}$$

The power transfer of the AC-AC DAB converter under real power operation for the conventional phase-shift modulation (4.13) and for the advanced modulation scheme with $g > 0$ (4.14) and $g < 0$ (4.15) can thus be simplified with (4.20). It is assumed that the load is constant and does not change during one sine period and thus with (4.17) the voltage ratio $d = n\, v_2(t)/v_1(t)$ is constant. With $d = const.$ the calculation of the optimal modulation parameters do not increase in complexity compared to the DC-DC DAB converter (cf. Chaper 2) and the operation can be considered equivalent to the DC-DC operation. The optimal parameters of the combined modulation scheme derived in Section 2.4.1 do not change with each switching cycle and thus are only calculated and updated periodically with the sine period $2\pi f$.

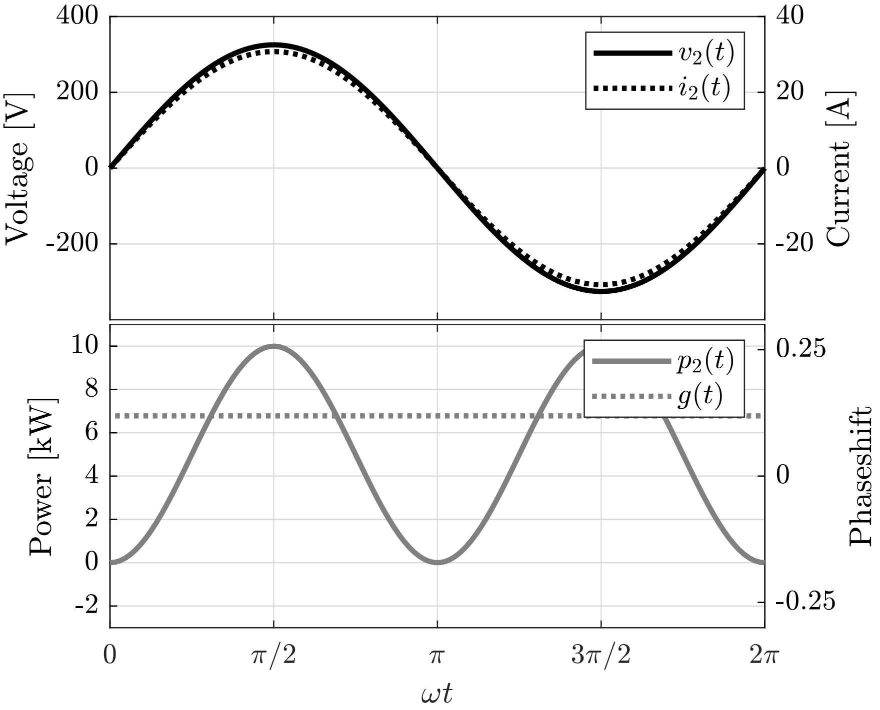


Fig. 4.11.: Calculated time dependant phase-shift $g(t)$ with $\varphi_2 = 0$, $V_2 = 230\,\mathrm{V}$, $P_2 = 5000\,\mathrm{W}$ and $w = 0$

4.3.2. Reactive Power Operation

The calculated waveforms of a AC-AC DAB converter under reactive power operation with $\varphi_2 = -\pi/4$ are depicted in Figure 4.12 and it follows with Equation 4.9

$$i_2(t) = \hat{I}_2\, sin(\omega\, t + \varphi_2) \qquad \text{with} \qquad -\pi/2 \le \varphi_2 < 0 \tag{4.21}$$

It is visible, that due to $v_2(t)$ and $i_2(t)$ being out of phase the phase-shift $g(t)$ is no longer constant but is time dependant and varies from -0.25 to $+0.25$ in one half sine period. The control parameter furthermore shows a discontinuity which occurs periodically with $n\,\pi$, $n \in \mathbb{R}$ and it is visible, that a region of maximum modulation occurs.

From the phase-shift parameter $g(t)$ (cf. Figure 4.12) several drawbacks of the reactive power operation are revealed. The input and output voltages are in phase. As the input voltage approaches zero, the converter has to transfer instantaneous power which is greater than the maximum transferable power of the converter, which is depicted in Figure 4.13. It is visible that regions exist, where the instantaneous calculated power exceeds the maximum transferable power of the converter. In theory, the control parameter would tend to infinity to be able to transfer the needed power to obtain a sinusoidal output voltage. In reality, the control parameter is limited and therefore, the reactive power operation of an AC-AC DAB converter results in regions, where the converter is no longer controllable [56]. This behaviour, furthermore, puts additional stress on the control circuit as the control scheme has to be very dynamic to keep track of the highly nonlinear control parameter with a discontinuity.

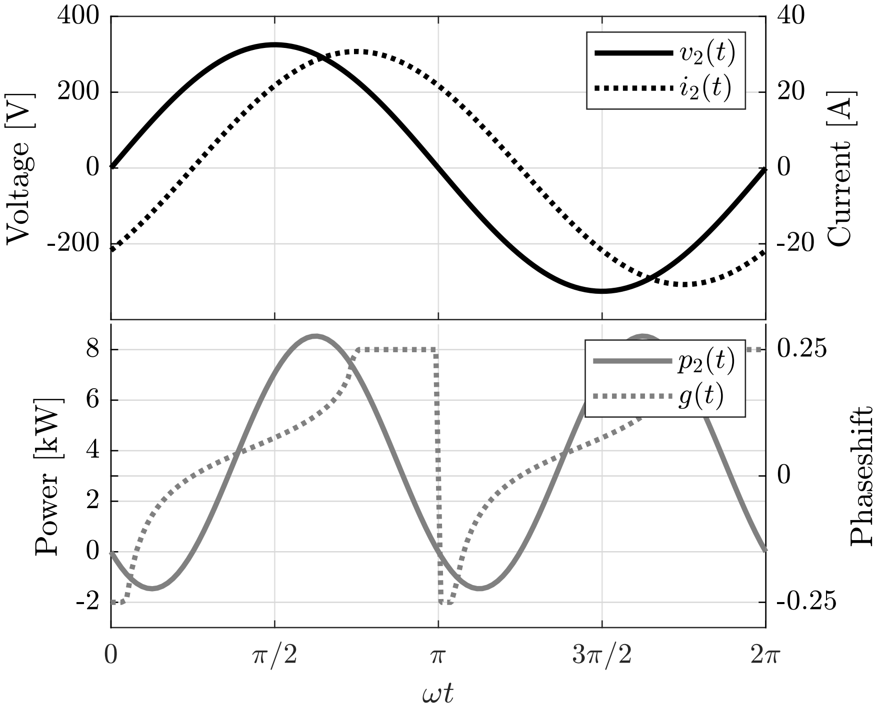


Fig. 4.12.: Calculated time dependant phase-shift $g(t)$ with $\varphi_2 = -\pi/4$, $V_2 = 230\,\mathrm{V}$ and $S_2 = 5000\,\mathrm{VA}$

It is apparent that due to the control parameters being no longer constant, the calculation of the optimal parameters of the combined modulation scheme increases significantly in complexity, as it becomes a time-dependent problem. This results in the necessity to calculate and update the control parameters dynamically, which has to be accomplished with each switching time interval $T_s = 1/f_s$.

Output voltage phase-shift

The main drawback of the AC-AC DAB under reactive power operation is the inability to transfer the required instantaneous output power (cf. Figure 4.13) leading to regions of maximum modulation. As no energy is stored during each switching cycle, the instantaneous input power is equal to the instantaneous output power, when the lossless model is considered (cf. Equation 4.5). With an inductive load connected, the output current cannot change instantly, and thus the output voltage varies from its

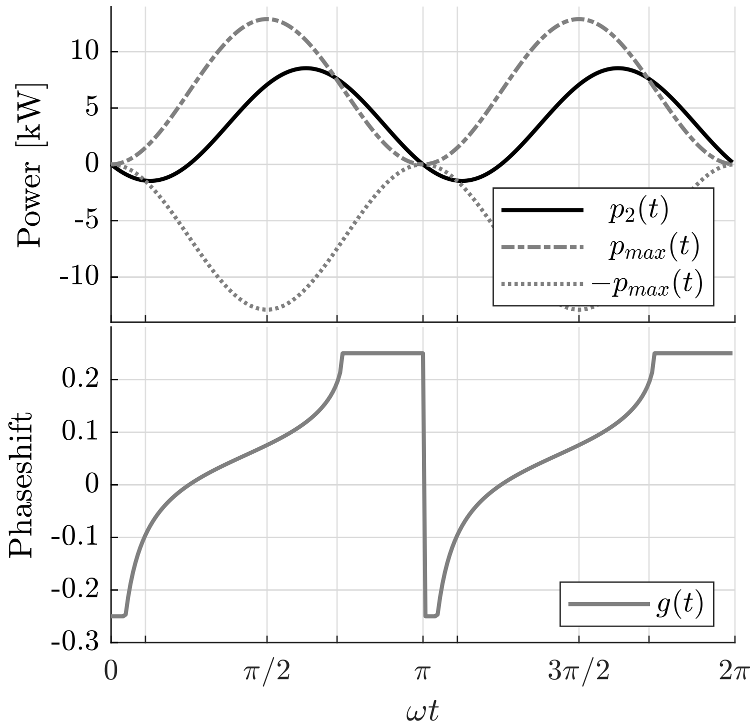


Fig. 4.13.: Calculated instantaneous output power $p_2(t)$ with $\varphi_2 = -\pi/4$. The maximum instantaneous transferable positive power $p_{max}(t)$ and negative power $-p_{max}(t)$ with $w = 0$ and $g = 0.25$ and $g = -0.25$ respectively are shown. The time dependent phase-shift $g(t)$ is depicted resulting from $p_2(t)$

sinusoidal reference value during the uncontrollable regions. This leads to undesired third harmonics in the input current, described in detail in Chapter 5.

From Equation 2.21 with

$$p(t) = v_2(t)\, i_2(t) \tag{4.22}$$

the phase-shift $g(t)$ can be rewritten to

$$g(t) = \frac{1}{4}\left(1 \pm \sqrt{1 - \frac{8\, f_s\, L\, |i_2(t)|}{n\, v_1(t)}}\right) \tag{4.23}$$

To obtain a constant phase-shift the following equality has to be true:

$$\frac{i_2(t)}{v_1(t)} = const. \tag{4.24}$$

The above Equality (4.24) is true if the input current $i_1(t)$ and output voltage $v_2(t)$ are in phase ($\varphi_{v1} = \varphi_{i2}$) and it holds:

$$\varphi_{v1} = \varphi_{i2} = 0 \tag{4.25}$$

Thus the expressions of v_1, v_2 and i_2 result to:

$$\begin{aligned} v_1(t) &= \hat{V}_1\, sin(\omega\, t) \\ v_2(t) &= \hat{V}_2\, sin(\omega\, t - \varphi_2) \\ i_2(t) &= \hat{I}_2\, sin(\omega\, t) \end{aligned} \tag{4.26}$$

Figure 4.14 depicts the calculated phase-shift $g(t)$ under reactive power operation with $\varphi_2 = -\pi/4$ and with the output voltage $v_2(t)$ and input current $i_1(t)$ in phase. It is visible that compared to the reactive power operation with $\varphi_{v1} = \varphi_{v2}$ (cf. Section 4.3.2 the phase-shift $g(t)$ is constant and thus the drawback of the control parameter's discontinuity and the non-linearity has been solved.

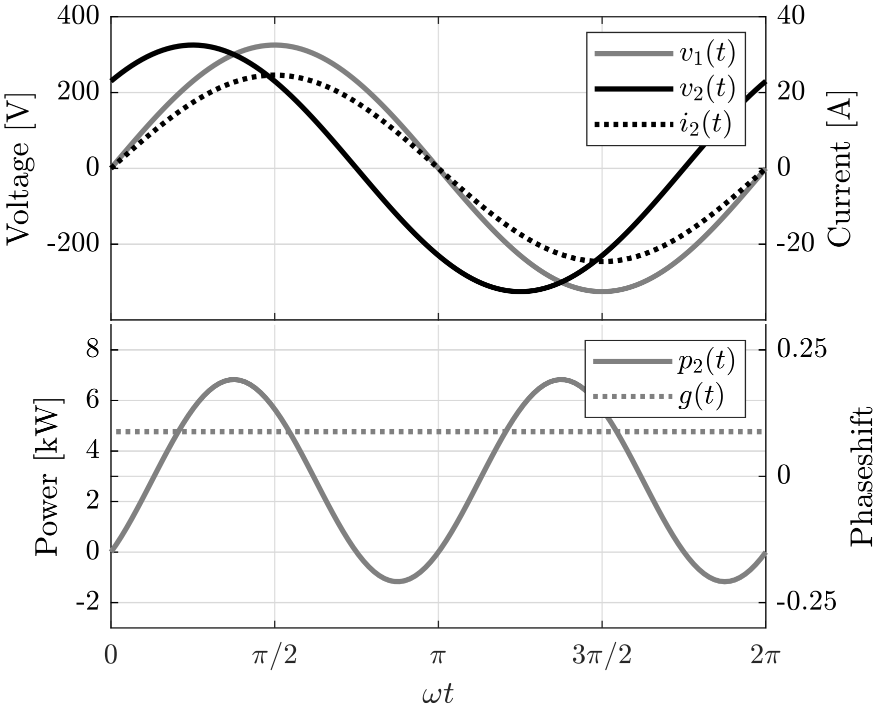


Fig. 4.14.: Calculated phase-shift $g(t)$ with $\varphi_2 = -\pi/4$, $\varphi_{v1} = \varphi_{i2}$, $V_1 = V_2 = 230\,\text{V}$ and $S_2 = 4000\,\text{VA}$

As the input and output voltages are no longer in phase, the voltage ratio d is not constant but changes with each switching cycle. From Chapter 2.2 it is known that the highest efficiency under phase-shift modulation is present when $d = 1$. With d being time-dependent the advanced modulation schemes have to be implemented to guarantee minimum RMS current in the transformer and to ensure ZVS over the whole operating range to maximize the converter efficiency. As mentioned in

Section 4.3.2 the optimal parameters still have to be calculated and updated with each switching cycle T_s. The difference is that control parameters are no longer highly nonlinear and show no discontinuity. This reduces the stress on the control circuitry. Furthermore, the converter is controllable over the whole operating range and thus removes the undesired third harmonic content from the input current.

4.4. Conclusion

This Chapter describes the working principle DAB converter operated with alternating sinusoidal voltage and current. The necessity of four-quadrant switches is detailed, and the effect on the modulation schemes by the alternating units and the four-quadrant switches is described. As the AC-AC DAB converter is meant as a direct replacement of a conventional transformer, the real power and the reactive power operation of the converter are described. It is shown that under real power operation, the voltage ratio d is constant and that the operation of the converter is thus equivalent to the DC-DC converter's. Furthermore, the calculation of the optimal modulation parameters does not increase in complexity.

The difficulties of the reactive power operation with the input and output voltages being in phase is detailed. It is shown that regions exist, where the instantaneous output power greater than the maximum instantaneous transferable power of the converter is. This leads to uncontrollable regions which cause an undesired third harmonic content in the input current. Furthermore, the control parameter shows a discontinuity and is highly nonlinear. It is described that by shifting the output voltage in such way, that the input voltage and the output current are in phase, the control parameter is no longer time dependant and becomes constant over one sinusoidal period. By this, the converter is controllable over the whole operating range, and the third harmonic content in the input current is eliminated. Due to the time-dependent voltage ratio d, the importance of the combined modulation scheme is detailed to guarantee maximum converter efficiency.

5. Steady-State Simulation of a DAB Converter

To verify and validate of the optimal modulation parameters g, w_1 and w_2 of the combined modulation scheme, proposed and detailed in Chapter 2, a transient simulation with LTspice is conducted. This Chapter firstly presents the simulated results of the DAB model considering conduction losses modulated with the combined modulation scheme. The above model only accounts for conduction losses; all other components are assumed to be ideal. The influence of real components (semiconductor devices and transformer) on the power transfer of a DAB converter are furthermore investigated, and the effect on the modulation parameters detailed.

A DC-DC converter with real components is simulated, and the efficiency of the converter modulated with the conventional phase-shift modulation is predicted. The simulation is then extended with the one-sided-clamped modulation scheme, and the efficiency gained by the combined modulation scheme is detailed.

Lastly, the AC-AC DAB converter is simulated. The active and reactive power operation is presented, and the drawbacks of the reactive power operation mentioned in Section 4.3.2 are shown in detail.

The ultimate design goal is the AC-AC DAB converter to replace a conventional power transformer. Therefore all the simulations conducted and described in the following Chapter are done in such way that the physical properties of the simulated converter represent them of an AC-AC DAB converter. The equivalent resistance in the DAB model considering conduction losses is thus chosen to be $R_{eq} = 550\,\mathrm{m\Omega}$. This represents all ohmic resistances in the power path of the prototype converter (cf. Chapter 6) and is described in detail below. Furthermore, the turns ratio is set to $n = 1$, as the prototype converter is meant as an replacement of a 1:1 isolation transformer.

5.1. DC-DC DAB Converter

A closed-loop stepped simulation of the DAB model considering conduction losses is conducted. The clamping interval w_2 is incremented and the control loop circuit controls the phase-shift g to transfer the output power, ranging from zero to P_{max}, at a fixed output voltage V_2. The inductor RMS current is calculated at each step, and the optimal clamping interval w_2 that minimizes the inductor RMS current at a given output power level is extracted. Furthermore the phase-shift g for the optimal clamping interval w_2 is extracted. The optimal parameters of the simulated results are then compared to the calculated modulation parameters of the proposed combined modulation scheme. The equivalent resistance of the simulated DAB model is chosen to be $R_{eq} = 550\,\text{m}\Omega$ and originates from the measured values of the prototype converter and is calculated with Equation (2.56).

Figure 5.1 depicts the calculated optimal modulation parameters (cf. Figure 4.8) with the simulated results overlaid. The clamping interval $w_2 \in [0, 0.5]$ is incremented in 0.01 steps and the output power in $100W$ steps. As the input voltage is smaller than the output voltage, w_1 is set to zero. The Figure shows that the deviation of the optimal parameters derived from combined modulation scheme is minimal.

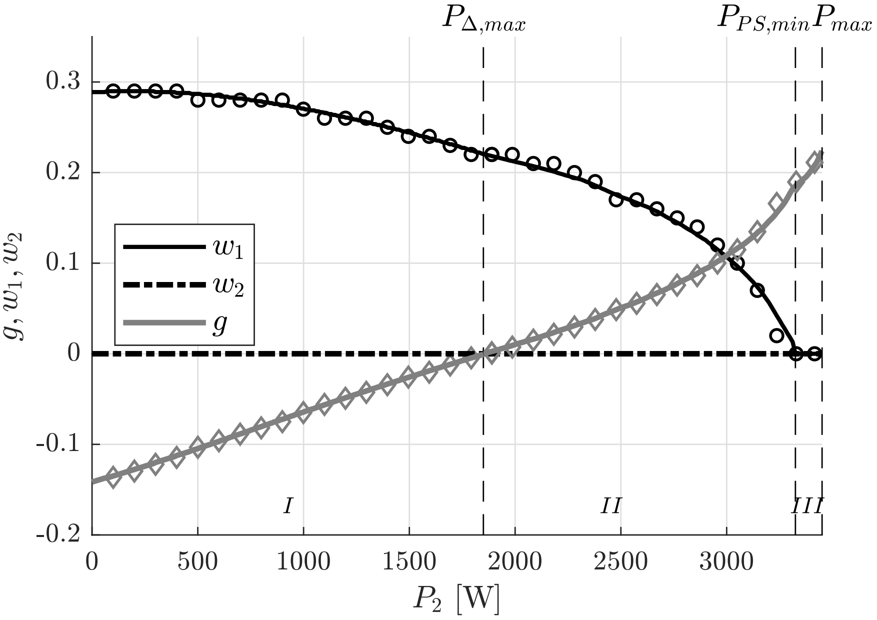


Fig. 5.1.: Optimal calculated clamping intervals w_1, w_2 of the combined modulation scheme with conduction losses in relation to the transferred output power P_2 with $V_1 = 138\,\text{V}$, $V_2 = 230\,\text{V}$ and $R = 550\,\text{m}\Omega$ of an DC-DC operated DAB converter. The phase-shift g results from the transferred output power at given clamping intervals w_1, w_2. The overlaid scatter plots denote the simulated results. Region I denotes $g < 0$ and Region II denotes $g > 0$ of the one-sided clamped modulation. Region III refers to the phase-shift modulation with $w_1 = w_2 = 0$.

The inductor RMS current and the converter efficiency of the DAB model considering only conduction losses are depicted in Figure 5.2 for the conventional phase-shift modulation (*ps*) and the combined modulation scheme (*opt*). It is noticeable that, due to the significantly reduced inductor RMS current in the low power region, the efficiency is significantly increased by the combined modulation scheme. The two efficiency curves approach each other with increasing power and reach each other when the converter reaches maximum modulation. The combined modulation scheme goes over into the phase-shift modulation.

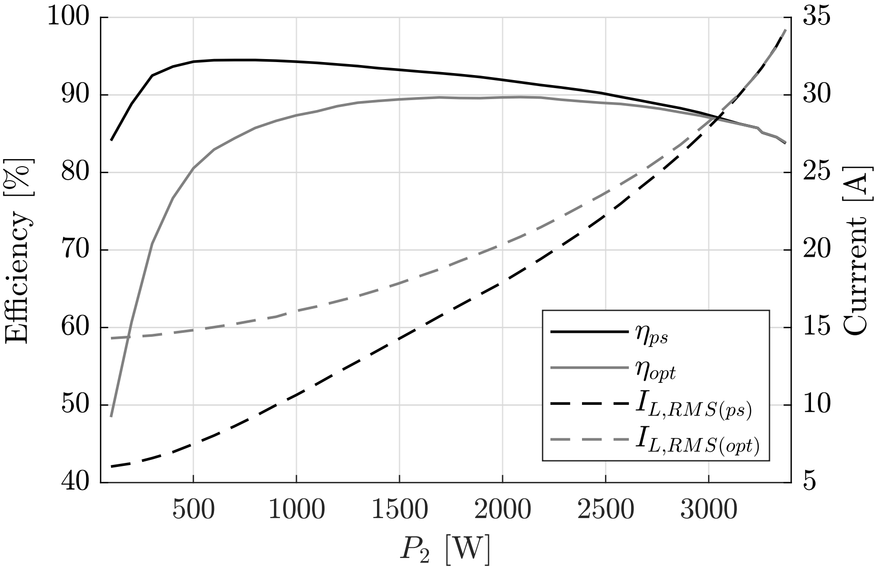


Fig. 5.2.: Converter efficiency and inductor RMS current of the DAB model considering conduction losses for the conventional phase-shift modulation (*ps*) and the combined modulation scheme (*opt*) in relation to the output power P_2 with $V_1 = 138\,\mathrm{V}$, $V_2 = 230\,\mathrm{V}$ and $R = 550\,\mathrm{m\Omega}$.

5.1.1. Real DAB Model

The before described DAB model that only considers conduction losses assumes that

- firstly, the magnetising inductance is much greater than the stray inductance ($L_M >> L_\sigma$) resulting in a much smaller primary inductance than magnetising inductance current ($i_M << i_L$), and
- secondly, the voltage transitions are instantaneous.

The implications of above simplifications on the inductor RMS current modulated with the calculated optimal modulation parameters are examined. The simulation is extended in two steps. Firstly the resonant MF tank is replaced with a T-model transformer depicted in Figure 5.3. After that, the ideal switches used in the previous simulation are replaced by real SPICE models of the IPW65R041CFD MOSFET.

The extended simulations are fed with the optimal clamping interval w_2 calculated and verified (cf. Section 5.1) for a given voltage ratio d and the output power ranging from from zero to P_{max}.

Transformer

The reactive MF network (previously simplified by only the equivalent inductance shown in Figure 2.3) is replaced by the network depicted in Figure 5.3. The real transformer is modelled by its T-model components $L_M, L_{\sigma 1}, L_{\sigma 2}, R_{cu1}$ and R_{cu2}. The transformation of the voltage is modelled by the ideal $n : 1$ transformer shown in Figure 5.3. As the turns ratio is 1 : 1, the coupling inductor L_c is not connected to the primary side of the DAB converter but is split evenly to the primary and secondary to guarantee full symmetry of the converter. It holds:

$$L_c = L_{c1} + L_{c2} \tag{5.1}$$

The components' values to feed the two-winding T-model transformer and the coupling inductances of the simulation are calculated from the measured values (cf. Appendix C) of the magnetic components designed for the 5 kVA prototype converter detailed in Chapter 6. The switch resistances R_{S1} and R_{S2} are chosen to $R_{S1} = R_{S2} = 50\,\mathrm{m\Omega}$ and represent the on resistance $R_{DS,on}$ of the Infineon IPW65R041CFD MOSFET at a junction temperature of $T_j = 50°C$ extracted from the data sheet [57].

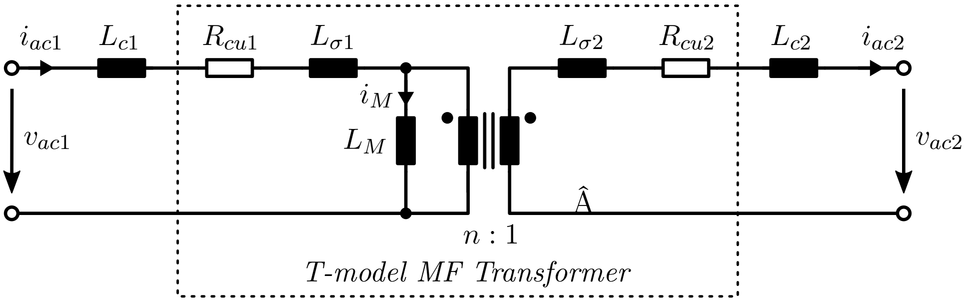


Fig. 5.3.: Equivalent circuit of the simulated reactive MF network with a T-model transformer and the coupling inductor is split to both the primary and the secondary L_{c1} and L_{c2}

The measured values of the prototype transformer are as follows:

$$\begin{aligned} L_{prim(open)} &= 420\mu H \\ L_{prim(short)} &= 2.4\mu H \\ R_{cu1} &= 60m\Omega \\ R_{cu2} &= 60m\Omega \end{aligned} \tag{5.2}$$

and for the coupling inductances L_{c1} and L_{c2}:

$$\begin{aligned} L_{c1} &= 11\mu H \\ L_{c2} &= 11\mu H \\ R_{lc1} &= 25m\Omega \\ R_{lc2} &= 25m\Omega \end{aligned} \tag{5.3}$$

It is often written that by shortening the secondary transformer winding the leakage inductance can be measured on the primary. This does not apply for the T-model as by shortening the secondary the reflected secondary leakage inductance $L_{\sigma2}$ is measured in parallel with the magnetizing inductance L_M, both again connected in series with the primary leakage inductance $L_{\sigma1}$ [58]. The accurate computation of the components' values to feed the simulation is described in [58] and it holds:

The coupling coefficient k is given by

$$k = \sqrt{1 - \frac{L_{prim(short)}}{L_{prim(open)}}} \tag{5.4}$$

the primary and secondary stray inductance ($L_{\sigma1}$ and $L_{\sigma2}$) are then computed by

$$L_{\sigma1} = (1-k)\, L_{prim(open)} \tag{5.5}$$

and

$$L_{\sigma2} = (1-k)\, L_{prim(open)}\, \frac{1}{n^2} \tag{5.6}$$

Finally the magnetizing inductance L_M is computed as follows:

$$L_M = k\, L_{prim(open)} \tag{5.7}$$

The resulting efficiency and inductor RMS current waveforms of the simulation with the two-winding T-model transformer and the split coupling inductances are shown in Figure 5.4. It is apparent that the primary and secondary inductor RMS currents $I_{prim,RMS}$ and $I_{sec,RMS}$ differ and that the secondary transformer current is slightly larger. This causes the efficiency to drop by 0.5% in the low power region, and the efficiency drops even further with increasing power. This originates from the increased inductor RMS currents at high power.

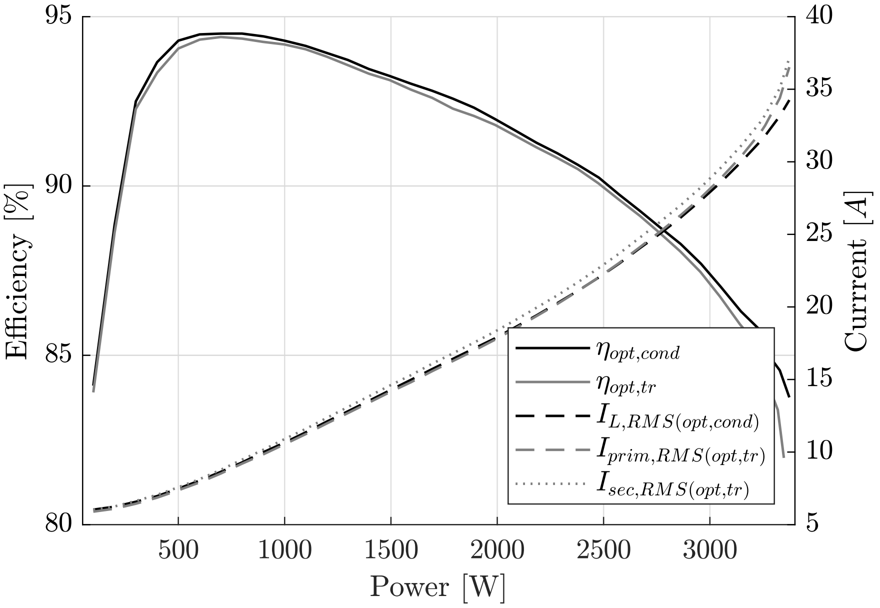


Fig. 5.4.: Converter efficiencies and inductor RMS currents of the DAB model considering conduction losses ($opt, cond$) and the DAB model with a T-model transformer and split coupling inductances (opt, tr) in relation to the output power P_2 with $V_1 = 138\,\mathrm{V}$, $V_2 = 230\,\mathrm{V}$ and $R_{S1} = R_{S2} = 100\,\mathrm{m}\Omega$. Both modulated with the combined modulation scheme.

MOSFET

As detailed in Section 3.2.2, the voltage transitions are of resonant nature (and not instantaneous as previously assumed), when real semiconductor switches are used. This makes it necessary to implement a dead-time t_d to avoid both transistors in one half-bridge conducting at the same time forming a bridge short circuit. Hence, a semiconductor device in a half-bridge circuit is only turned on once the complementary device has been turned off completely. The necessary dead-time of a IPW65R041CDF MOSFET ranges from 400 to 600 nanoseconds, depending on the size of the gate resistor chosen. Furthermore, losses are generated by overlapping voltage and current when a resonant switching transition occurs.

The ideal switches used in the previous simulation are replaced by real SPICE models of a IPW65R041CFD MOSFET. A dead-time of $t_d = 600ns$ and the gate-resistance $R_g = 15\Omega$ are chosen. The reactive MF network is modelled as described in Section 5.1.1 and depicted in Figure 5.3.

The minimum necessary primary and secondary commutation currents $I_{c,min(prim)}$ and $I_{c,min(sec)}$, defined in Equation (3.13) with the equivalent capacitances defined in Equations (3.14) and (3.17) for the phase-shift modulation and the one-sided clamped modulation respectively, are listed in Table 5.1 (showing the relevant switching times t_0, t_1 and t_2). Due to the presence of a magnetising current of the transformer, the table is updated and lists the minimum communication current to warrant ZVS for the primary and the secondary half-bridge circuits.

Tab. 5.1.: ZVS constraints of combined modulation scheme considering conduction losses and the magnetising current of the transformer

Region	ZVS Constraints		
I	$i_{L,prim}(t_0) < -I_{c,min(prim)}$,	$i_{L,sec}(t_1) > I_{c,min(sec)}$	$i_{L,sec}(t_2) < -I_{c,min(sec)}$
II	$i_{L,prim}(t_0) < -I_{c,min(prim)}$	$i_{L,sec}(t_1) > I_{c,min(sec)}$	$i_{L,sec}(t_2) > I_{c,min(sec)}$
III	$i_{L,prim}(t_0) < -I_{c,min(prim)}$	$i_{L,sec}(t_1) > I_{c,min(sec)}$	

Figure 5.5 depicts the simulated efficiency η and the inductor primary and secondary RMS currents $I_{L,prim,RMS}$ and $I_{L,sec,RMS}$. Furthermore, the power dissipated in the MOSFETS $P_{loss,Tx}$, where $x \in [1, 8]$ to the eight MOSFETs refers, and the phase-shift g and optimal clamping paramater w are visualized.

When studying the waveforms, it becomes apparent that an efficiency dip of the simulation with the real MOSFET model is present, when the phase-shift g approaches zero. Furthermore, a raised figure of the waveforms of the MOSFETs dissipated power is visible in this region. This increase in losses is explained as follows: The calculated model does not take the switching losses of the semiconductor devices into consideration. When g approaches zero, the transition from Case I to Case II of the one-sided modulation (Region I to II) occurs at $g = 0$. The calculated inductor currents at the switching times t_0, t_1 and t_2 (cf. Figure 4.9, Figure 2.27) show that the inductor current at t_0 and t_2 reach zero when $g = 0$. Although the current through the semiconductor device that is being switched is zero, the switching transition is defined as hard because switching losses are generated. The transition of a MOSFET (described in Chapter 3) is of resonant nature, and thus charges have to be moved during each switching transition. For this movement of charge, a certain energy in the resonant tank has to be present to warrant ZVS. With $i_L = 0$ the drain-source voltages v_{DS} remain constant during the dead-time, as no energy is available in the resonant tank to move the charges of the output capacitances and the body-diode during the dead-time. This energy is supplied by the switched device and is defined by the area under the current overshoot.

Furthermore, the inductor current curve in Region I ($g < 0$) at the switching time t_2 is concave. This leads to a relativity large output power interval where $i_{L,sec}(t_2) \approx 0$, before reaching zero at $g = 0$. The low current in this interval does not fulfil the

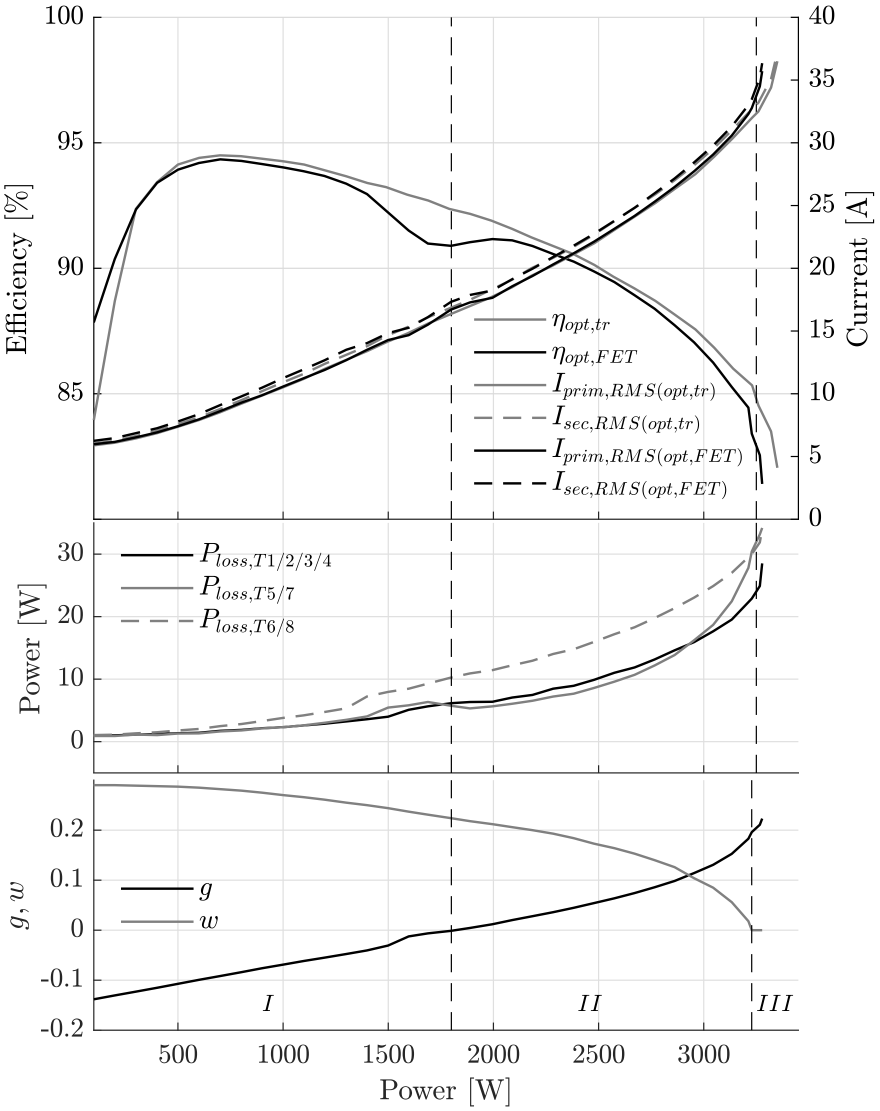


Fig. 5.5.: Simulated converter efficiencies and inductor RMS currents of the DAB model with a T-model transformer and split coupling inductances (opt, tr) and of the real model with bi-directional MOSFET switches (opt, FET) in relation to the output power P_2 with $V_1 = 138\,\mathrm{V}$ and $V_2 = 230\,\mathrm{V}$. Both modulated with the combined modulation scheme and both the phase-shift g and the clamping interval w are depicted. The resulting power loss dissipated in the semiconductor switches are shown and referred to by $P_{loss,Tx}$ with $x \in [1, 8]$

ZVS constraints listed in Table 5.1, and thus ZVS is not fully warranted. This is represented by an increased power loss during the above described interval (cf. Figure 5.5). It should, however, be mentioned that the increased power loss is minimal because the drain-current during the switching transition is close to zero and does not reverse its polarity.

Due to symmetry, the dissipated power of the semiconductor devices $P_{loss,Tx}$ of the primary full-bridge $x \in [1, 4]$ show an equal distribution over the plotted output power P_2 with the before described increase around $g = 0$. The dissipated power of the semiconductor devices T_5 and T_7 shows a strict monotonous increasing curve which correlates with the fact that the ZVS constraints for the half-bridge of T_5 and T_6 are always fulfilled. The dissipated power curve is, however, the greatest, which results from the switching transition occurring at the maximum instantaneous inductor current. Thus high turn-off losses are present. The dissipated power the semiconductor devices T_6 and T_8 reach the curve of T_5 and T_7 when the combined modulation scheme goes over into the phase-shift modulation. Consequently, all losses of the semiconductor devices of the secondary full-bridge are equal (due to symmetry).

A comparison of the efficiencies depicted in Figure 5.5, shows a slight decrease in efficiency when real MOSFET models are added to the simulation. The resonant transitions of the MOSFETs can explain this decrease. Although ZVS is warranted during the turn-on switching transitions (causing neglectable turn-on losses) the turn-off transitions of a MOSFET produce losses, caused by an overlap of drain-source voltage and drain-current during the switching transition.

Efficiency Enhancement of the Combined Modulation Scheme

Figure 5.6 depicts the efficiencies of the conventional phase-shift modulation and the combined modulation scheme, denoted *ps* and *opt* respectively of the simulated DAB model with the T-model transformer, split inductances and the real MOSFET SPICE models. Furthermore the primary and secondary inductor RMS currents I_{prim} and I_{sec} are plotted.

The efficiencies of the phase-shift and the combined modulation at different output power levels are listed in Table 5.2. It is apparent that the efficiency, due to the high RMS currents and the loss of ZVS of the phase-shift modulated converter, is remarkably enhanced by the combined modulation scheme. Especially in the low power region, the difference is significant, and an increase of nearly 50% is achieved. In the high power region, the efficiencies are equal, as the combined modulation scheme goes over into the conventional phase-shift modulation.

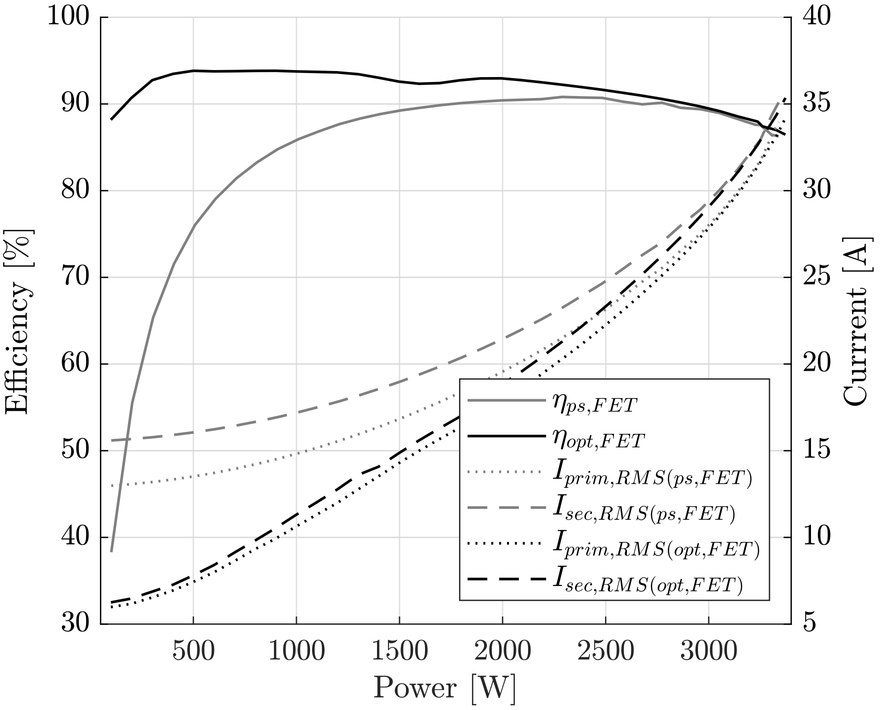


Fig. 5.6.: Converter efficiency and inductor RMS current comparison of the real DAB model of the conventional phase-shift modulation (ps) and the combined modulation scheme (opt) in relation to the output power P_2 with $V_1 = 138\,\mathrm{V}$, $V_2 = 230\,\mathrm{V}$ and $R = 550\,\mathrm{m\Omega}$.

Tab. 5.2.: Converter efficiency modulated with the conventional phase shift modulation and the combined modulation scheme

Output Power	**Converter Effeciency η**		
P_2	Phase-Shift	Combined	Enhancement
100W	38.3%	88.2%	49.9%
500W	76.0%	93.8%	17.8%
1000W	85.9%	93.7%	7.8%
1500W	89.2%	92.6%	3.4%
2000W	90.4%	93.0%	2.6%
2500W	90.7%	91.7%	1.0%
3000W	89.4%	89.7%	0.3%

5.2. AC-AC DAB Converter

The simulated results of a DAB AC-AC converter are presented. The real DAB simulation model described in Section 5.1.1 is extended with anti-series connected MOSFETs forming bi-directional switches to allow four-quadrant operation of the DAB converter. Firstly the active power operation is presented, and after that, the simulated results of a DAB AC-AC converter operated with reactive power are shown.

The output voltage is controlled to be in phase with the input voltage and therefore it holds:

$$\varphi_{v1} = \varphi_{v2} = 0 \tag{5.8}$$

which results to

$$\begin{aligned} v_1(t) &= \hat{V}_1\, sin(\omega\, t) \\ v_2(t) &= \hat{V}_2\, sin(\omega\, t) \\ i_2(t) &= \hat{I}_2\, sin(\omega\, t + \varphi_2) \end{aligned} \tag{5.9}$$

with

$$\begin{aligned} \hat{V}_1 &= \sqrt{2}\, V_1 \\ \hat{V}_2 &= \sqrt{2}\, V_2 \\ \hat{V}_2 &= \sqrt{2}\, I_2 \end{aligned} \tag{5.10}$$

where V_1, V_2 and I_2 to the RMS values of the respective unit refer.

5.2.1. Real Power Operation

Figure 5.7 depicts the simulated instantaneous input and output voltage ($v_1(t)$, $v_2(t)$) and current ($i_1(t)$, $i_2(t)$) under real power operation ($cos(\varphi_2) = 0$). The input RMS voltage V_1 ranges from 207 V to 253 V ($V_1 = 207\,\mathrm{V}(t \in [0, 20ms])$, $V_1 = 230\,\mathrm{V}(t \in [20, 40ms])$, $V_1 = 253\,\mathrm{V}(t \in [40, 60ms])$) and the output RMS voltage is fixed to $V_2 = 230\,\mathrm{V}$ transferring an output power of $P_2 = 5000\,\mathrm{W}$. The optimal clamping parameters for the input voltages $V_1 = 207\,\mathrm{V}$ and $V_1 = 253\,\mathrm{V}$ are depicted in Figure 5.8. For a input voltage of $V_1 = 230\,\mathrm{V}$ the clamping intervals result in $w_1 = 0 \wedge w_2 = 0$ due to $V_1 = n\; V_2$ (cf. Chapter 2). Form Figure 5.7 it is apparent that all waveforms are sinusoidal without any discontinuities. Therefore it can be concluded, that the active power operation is fully granted and the control of the converter is possible at every operating point.

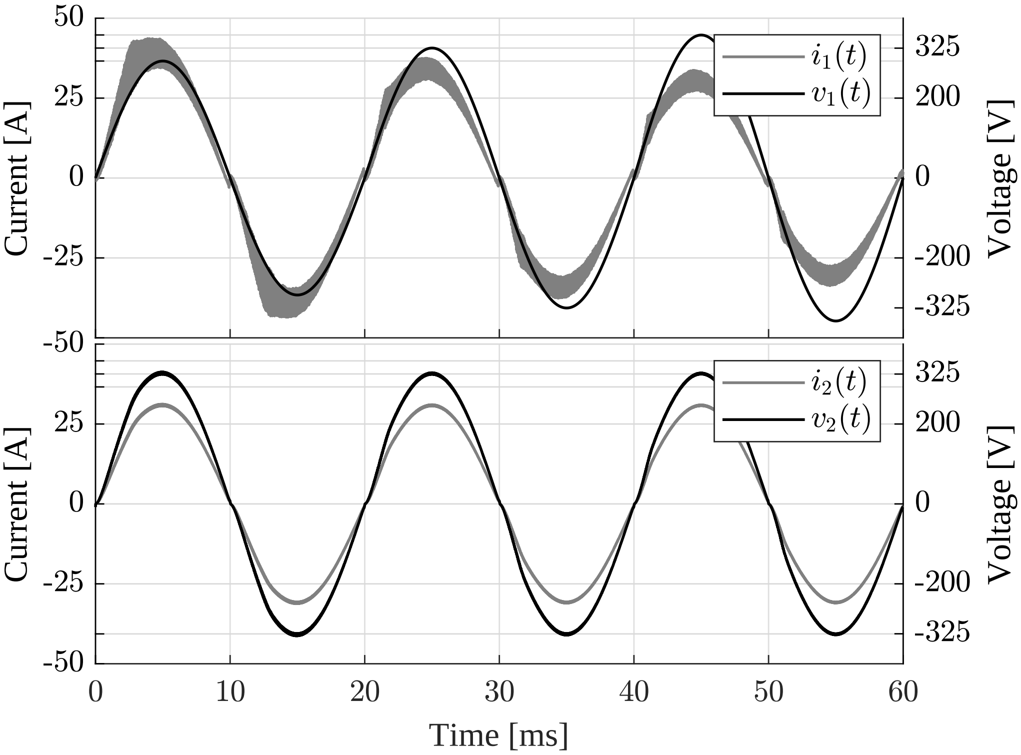


Fig. 5.7.: Simulated input and output current and voltage waveforms of a real AC-AC DAB converter model (cf. Section 5.1.1) with an output power of $P_2 = 5000\,\mathrm{W}$ and an output voltage of $V_2 = 230\,\mathrm{V}$. The input RMS voltage V_1 ranges from 207 V to 253 V ($V_1 = 207\,\mathrm{V}(t \in [0, 20ms])$, $V_1 = 230\,\mathrm{V}(t \in [20, 40ms])$, $V_1 = 253\,\mathrm{V}(t \in [40, 60ms])$). The switches of the primary and secondary full-bridges are replaced with bi-directional switches as described in Chaper 4.

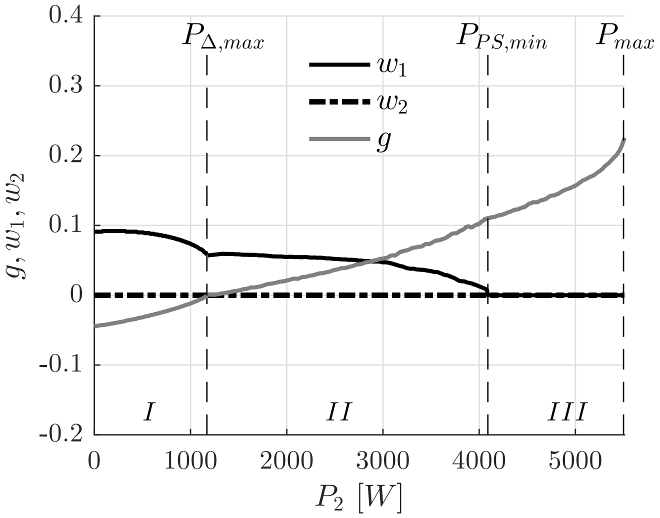


Fig. 5.8.: Optimal clamping interval w of the combined modulation scheme with conduction losses in relation to the transferred output power P_2 for the input voltages $V_1 = 207\,\mathrm{V}$ and $V_1 = 253\,\mathrm{V}$ with $V_2 = 230\,\mathrm{V}$ and $R = 550\,\mathrm{m\Omega}$ of an AC-AC operated DAB converter. For $V_1 = 207V$ the optimal clamping intervals hold $w_1 = 0 \wedge w_2 = w$ and for $V_1 = 253\,\mathrm{V}$ the optimal clamping intervals are swapped (due to symmetry) and hence result $w_1 = w \wedge w_2 = 0$. Region I denotes $g < 0$ and Region II denotes $g > 0$ of the one-sided clamped modulation. Region III refers to the phase-shift modulation with $w_1 = w_2 = 0$.

5.2.2. Reactive Power Operation

The instantaneous input and output voltage ($v_1(t)$, $v_2(t)$) and current ($i_1(t)$, $i_2(t)$) of the real DAB model operated as an AC-AC converter with reactive power transfer is shown in Figure 5.9. The depicted waveforms are simulated with an apparent output power of $S_2 = 5000\,\mathrm{VA}$ and a power factor of $cos(\varphi_2) = 0.8$ resulting in a real power transfer of $P_2 = 3400\,\mathrm{W}$. The drawbacks of the reactive power operation of the AC-AC DAB converter are apparent: Due to the theoretically needed instantaneous power being greater than the maximum transferable power at that timestamp, the converter has operating regions where it is not controllable. This can clearly be seen in Figure 5.9. When the output voltage reaches its maximum, the converter can no longer transfer the needed power, which results in the output voltage caving in and dropping to zero. As no power is stored in the power path of the converter, the input current falls to zero as the grid voltage cannot be influenced. After the zero-crossing of the output voltage, the converter can still not transfer the needed power. Due to the polarity reversal of the voltage, the voltage spikes and returns only to the voltage setpoint once the converters power transfer capability is greater than the needed transferable power. This again is directly transferred onto the input current. As mentioned in Chapter 4, this causes an undesired third harmonic content in the input current.

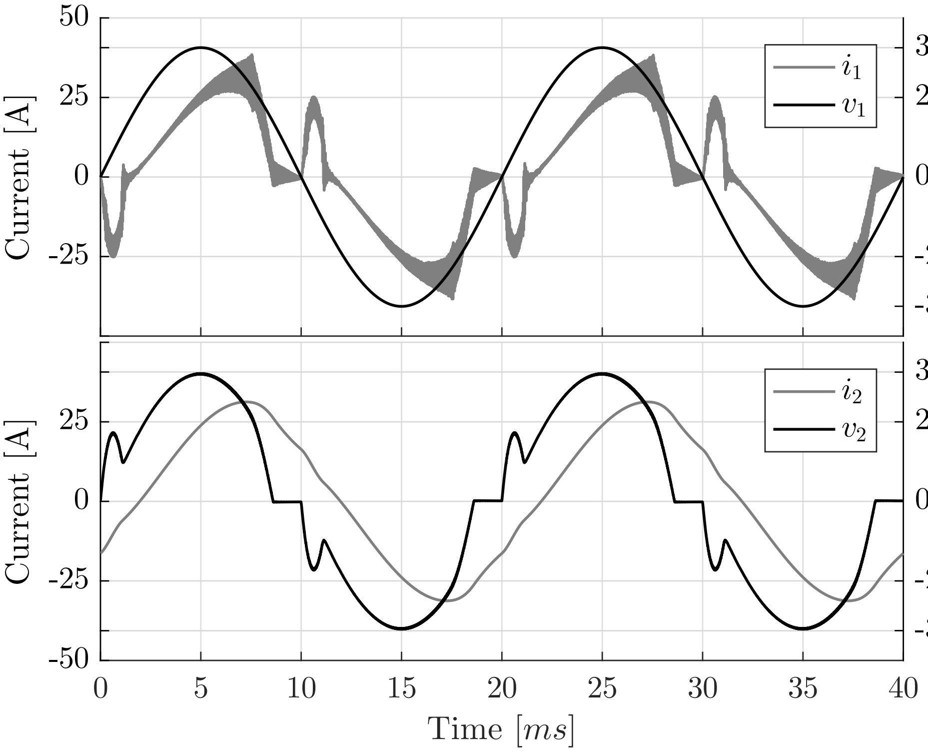


Fig. 5.9.: Simulated input and output current and voltage waveforms of a real AC-AC DAB converter model (cf. Section 5.1.1) with an apparent output power of $S_2 = 5000\,\mathrm{VA}$ and real output power of $P_2 = 3400\,\mathrm{W}$ ($cos(\varphi_2) = 0.8$) at an input and output voltage of $V_1 = V_2 = 230\,\mathrm{V}$.

5.3. Conclusion

The calculated optimal modulation parameters of the proposed combined modulation scheme are verified and validated by means of a SPICE simulation. The optimal clamping interval w of the model considering conduction losses, that minimizes the inductor RMS current, is extracted from a stepped simulation and plotted against the transferred output power. The comparison to the calculated optimal clamping interval w shows a good correlation.

The model that only considers conduction losses is extended by a T-model transformer and real MOSFET SPICE models, and the effect on the efficiency of the converter is investigated. It is shown that the calculated and verified optimal modulation parameters of the combined modulation scheme are valid for the real DAB model. The additional losses produced by the resonant switching transitions of a MOSFET are discussed, and the effect on the converter efficiency is presented.

Due to the parasitic elements of the MOSFET, the ZVS constraints are violated when the transition from the one-sided clamped modulation from $g < 0$ to $g > 0$ occurs. This results in a reduced efficiency in this region, caused by the higher dissipated loss power in the MOSFETs during the transition. As the current is close to zero and does not change its polarity, the switching losses inflicted by the violation of the ZVS constraints are minimal. The simulated results of the real DAB model modulated with the proposed combined modulation scheme show a significant increase in efficiency, compared to the conventional phase-shift modulation, especially in the low power region. It can, therefore, be concluded that the simulated results substantiate the added value of the proposed combined modulation scheme.

The simulated results of an AC-AC DAB converter are introduced, and the real power operation is described at first. It is shown that the operation is fully guaranteed with the combined modulation scheme. After that the reactive power operation is presented, and it is explained that due to uncontrollable regions of the converter, a third harmonic content in the input current is present. This is caused by a distorted output voltage, as the instantaneous transferable power is not sufficient in certain regions.

6. 5 kVA Prototype DAB Converter

This chapter presents the 5 kVA prototype AC-AC DAB converter shown in Figure 6.1. The design parameters are listed in Table 6.1. The block diagram of the prototype DAB converter is shown in Figure 6.2. The main components are shown. Furthermore, the power flow layer, the internal power supply layer, the control layer and the protection layer is visible.

Tab. 6.1.: Design parameters of the prototype DAB converter

Parameter	**Value**
Nominal input voltage	230 V
Nominal output voltage	230 V
Rated power (at 230 V, 50 Hz)	5000 VA
Grid frequency / range	50 Hz / 44 Hz to 55 Hz
Input voltage range	207 V to 253 V
Output voltage range	207 V to 253 V
Maximum power (30 s)	6200 VA
Efficiency (at 5000 W)	>92 %
Isolation (for 60 s)	5 kV
Power factor	0.7 leading, 0.7 lagging
Boxed volume	10 dm^3
Weight	9 kg

The control signals are the input voltage, the output voltage and the inductor current. For the implementation of voltage-mode control, only the output voltage is controlled, and the input voltage is needed for the calculation of the voltage ratio d for the computation of the optimal control parameters of the combined modulation scheme. In the case of average current-mode control, the outer voltage controller delivers the current setpoint to the inner current control loop with the average inductor current being the actual value.

Several protection measures are implemented such as overload, short-circuit, over-temperature protection and monitoring of the defined operating range of the converter (cf. Table 6.1). Thus the output current, the input frequency and the temperature of the magnetic components and the semiconductor switches are measured.

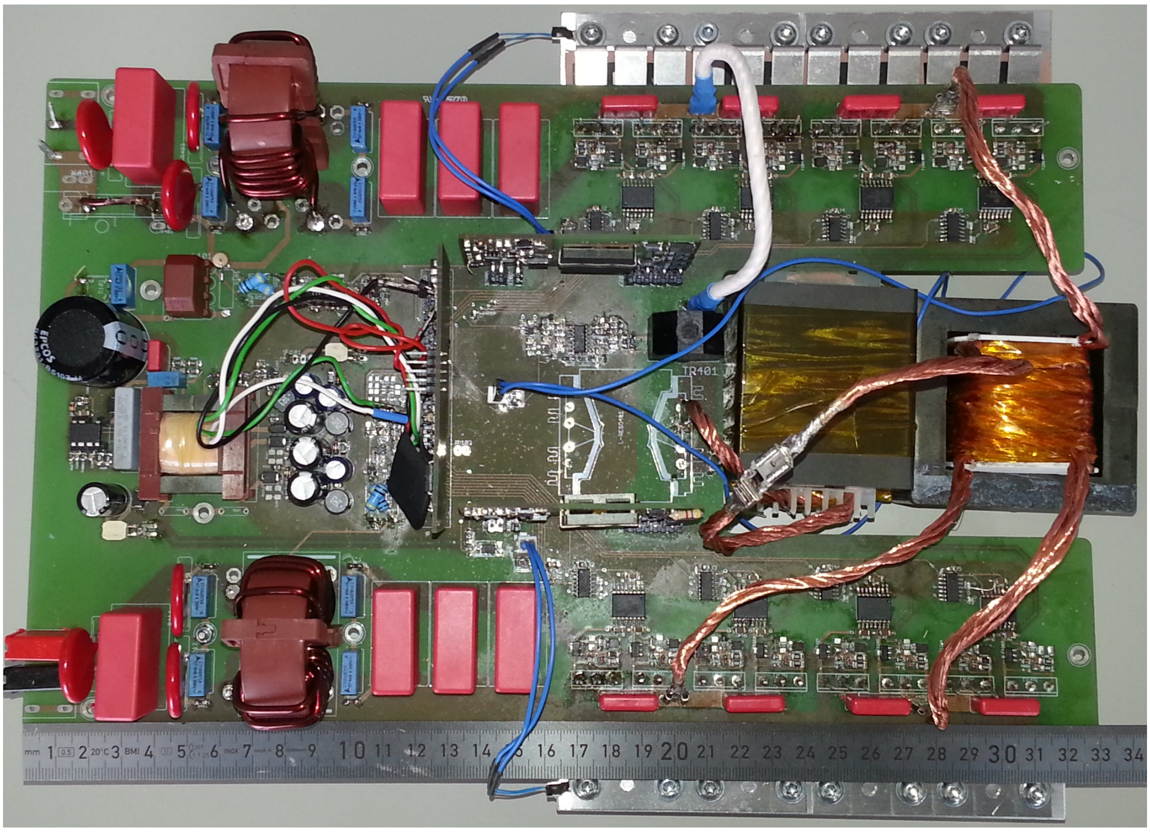


Fig. 6.1.: 5kVA AC-AC DAB prototype converter

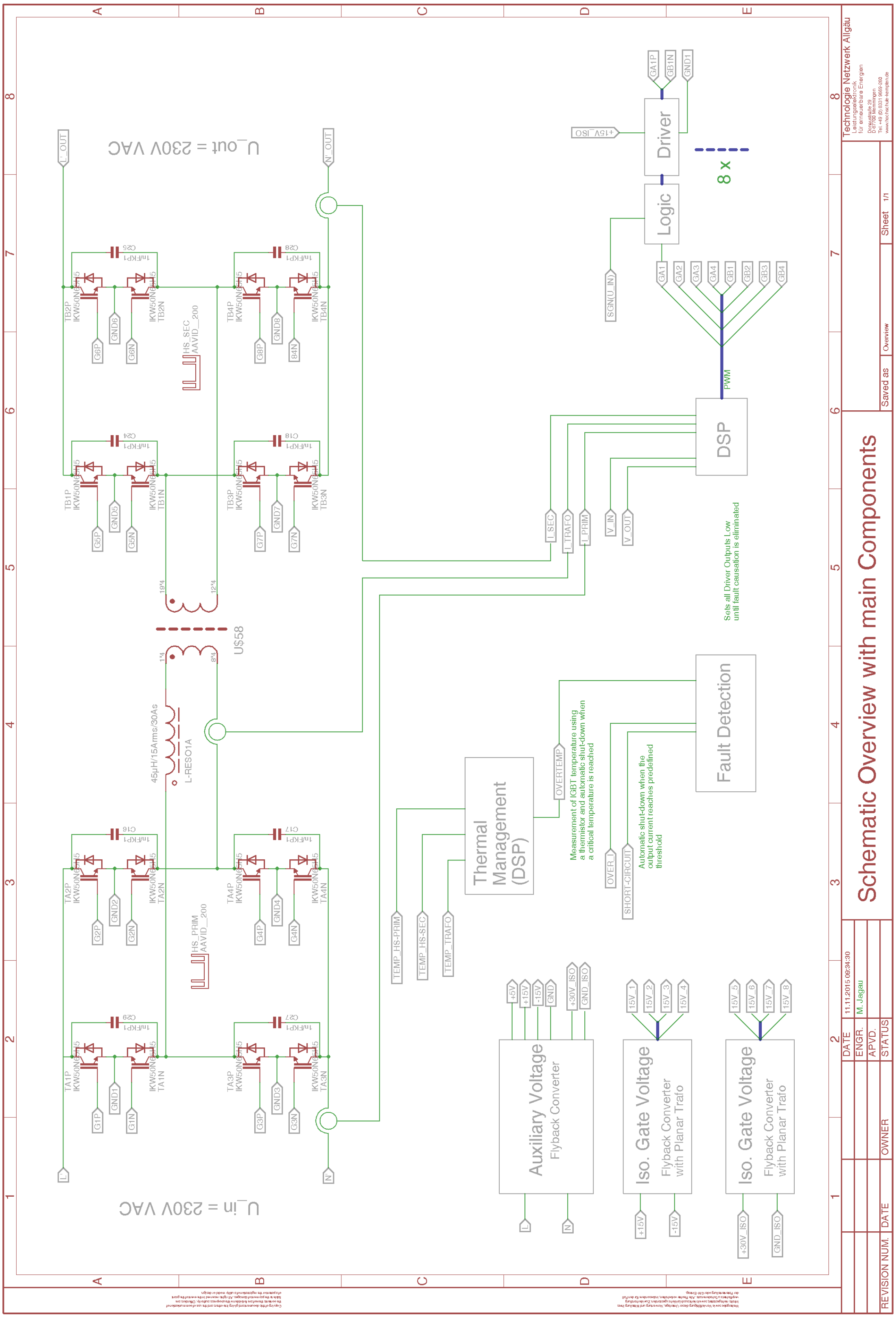


Fig. 6.2.: Schematic overview of the 5 kVA prototype converter

6.1. Calculation of Main Components

To be able to transfer the nominal design power P_{nom} (Chapter 2 (2.19)) the equivalent inductor has to be sized accordingly. As the maximum transferable power is inversely proportional to the equivalent inductor L_{eq}, a maximum value for the inductor exists and is defined by Equation (2.20). Equation (2.20) assumes a lossless model and due to the overall losses of the converter the transferred output power decreases. Furthermore a reserve should be considered to avail sufficient energy for a short overload time period. Equation (6.1) defines the maximum size of the equivalent inductance considering the converter losses (η_{pmax}) and catering for an overload capability by k_{ol}.

$$L_{eq,max} \leq \frac{n\,V_1\,V_2}{8\,f_s\,|P_{max}|}\,\frac{\eta_{pmax}}{k_{ol}} \qquad \text{with} \quad k_{ol} > 1 \tag{6.1}$$

It is shown in Chapter 2 that the maximum transferable power is achieved with the conventional phase-shift modulation. Therefore the calculations of the key components are based on the phase-shift modulation. Figure 6.3 shows the transistor RMS current, the inductor RMS current and the inductor current at the switching interval t_0 or t_1 as a function of the transferred output power and for the nominal, minimum and maximum input voltage and the nominal output voltage. The current at t_0 or t_1 presents the peak inductor current $\hat{I_L}$ depending on the voltage ratio and it holds:

$$\hat{I_L} = \begin{cases} i_L(t_1) & \text{for} \quad V_1 \leq n\,V_2 \\ i_L(t_2) & \text{for} \quad V_1 > n\,V_2 \end{cases} \tag{6.2}$$

It is apparent that the highest currents are present with an input voltage of $V_1 = 207V$. The design of the magnetic components and the semiconductor switches is therefore based on the values at rated output power and the minimum input voltage. The maximum calculated current values at rated power and minimum input voltage are listed in Table 6.2.

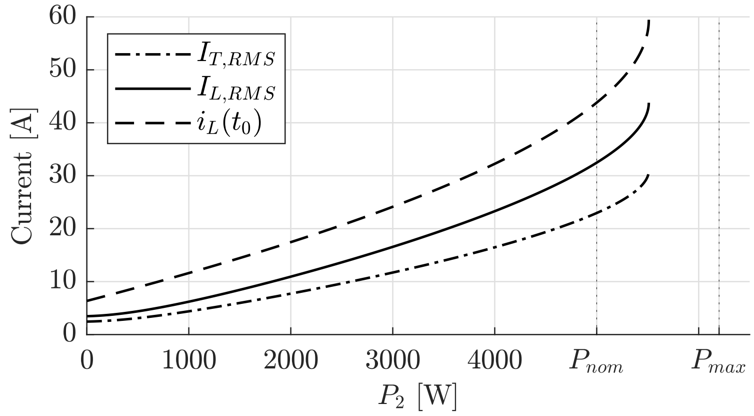
Tab. 6.2.: Maximum calculated current values at rated power and minimum input voltage

Parameter	**Value**
Transistor RMS current	$I_{T,RMS} = 23\,\text{A}$
Inductor RMS current	$I_{L,RMS} = 33\,\text{A}$
Peak inductor current	$I_{T,RMS} = 34\,\text{A}$

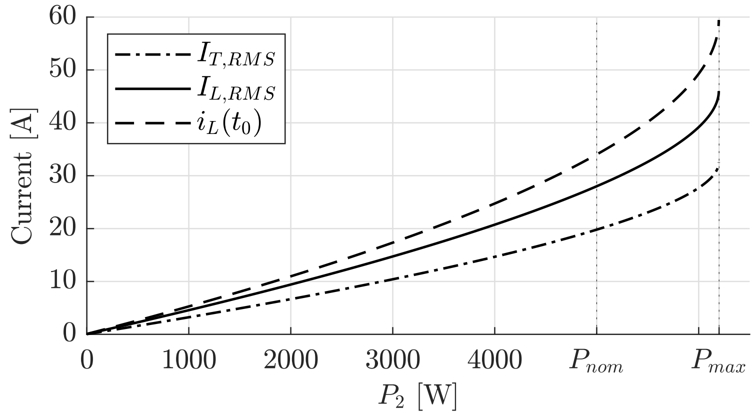
Equation (2.3) ($L_{eq} = L_c + L_{\sigma 1} + L_{\sigma 2}$) shows that the equivalent inductor is a sum of the discrete coupling inductance L_c and the transformer stray inductances $L_{\sigma 1}$ and

$L_{\sigma 2}$. The MF transformer is therefore designed first and the stray inductances are determined. Thereafter, the coupling inductor L_c is sized to satisfy Equation (2.3).

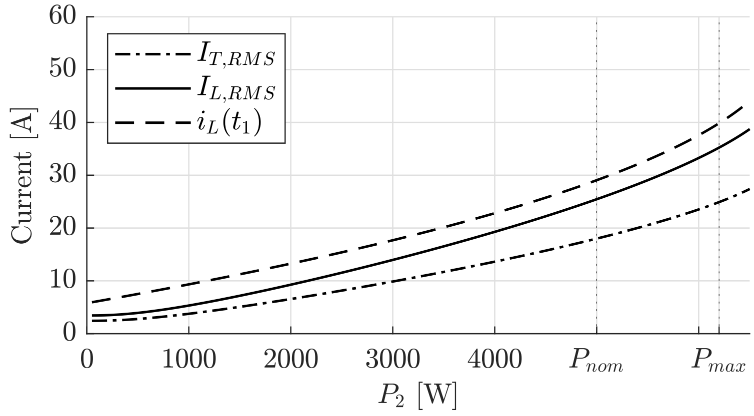
The switching frequency is chosen to be 40 kHz.



(a) $V_1 = 207\,\mathrm{V}$



(b) $V_1 = 230\,\mathrm{V}$



(c) $V_1 = 253\,\mathrm{V}$

Fig. 6.3.: Current values in relation to the transferred power for the design of the magnetic components and the semiconductor switches. The MOSFET RMS current $I_{FET,RMS}$, inductor RMS current $I_{L,RMS}$ and peak inductor current at $i_L(t_0)$ or $i_L(t_1)$ of the AC-AC DAB converter in relation to the transferred output power P_2 with the input voltages of $V_1 = 207\,\mathrm{V}$ (a), $V_1 = 230\,\mathrm{V}$ (b) and $V_1 = 253\,\mathrm{V}$ (c) are depicted.

6.1.1. Magnetic components

The design procedure of the magnetic components, namely the MF transformer and the coupling inductors are detailed in this Chapter. The magnetic components play a crucial part in achieving high power densities and ensuring high-efficiency operation of modern switched-mode power converters [59]. To guarantee high efficiency operation, the generated losses have to be minimised, and the individual components have to be designed accordingly. Many publications focus on the optimisation of the transformer [59], [27], [20]. [60] and [61] focus especially on optimising the transformer for a DAB converter. Most publications focus on the design and optimisation of the transformers, but the high-frequency effects are valid for the inductor as well. The main difference is that transformers transfer energy, whereas inductors store energy. Hence, the design procedure is different, but the below-described losses, be it the DC or AC part, are also valid and have to be considered in the design of the inductor as well.

The losses can be split into low-frequency (DC) and high-frequency (AC) losses, whereas the DC losses include the losses generated by the low-frequency ohmic resistance of the windings and the AC losses are caused by the core losses and the AC resistance of the winding losses. The AC resistance is made up by the skin and the proximity effect [62], [63].

The switching frequency is increased to maximise the power density of modern switched power electronic converters. With an increase in frequency eddy, currents in the transformer windings cause additional winding losses. The effect of the eddy currents on the transformer windings and the generated losses are described in [62] and [63]. These losses are generally categorised by losses, due to the skin and the proximity effect: The skin effect is due to eddy currents caused by the magnetic field of the current in the conductor itself, and the proximity effect is due to eddy currents that originate from external magnetic fields, e.g. from the neighbouring conductors' current or the magnetic field fringe caused by the presence of an air gap [64], [62], [63].

The core losses originate from the hysteresis losses and are thus dependent on the core material, the operating frequency and the peak flux density. These can be approximated either by the Steinmetz Equation [65], or by the data extracted from the material datasheet of the chosen core material [66].

The skin effect can be controlled by using Litz wire. Litz wire conductors are made up of multiple individually insulated strands twisted or woven together [64]. Thereby each strand is subject to the skin effect individually, and the optimal number and size of strands are presented in [64]. A simplified design approach is detailed in [67] where the single strand diameter is chosen with regard to acceptable losses. [68] presents the effect of twisting imperfections of Litz wire and the impact on the traditional approach on predicting the winding losses.

The proximity effect is influenced by the geometry and the winding pattern [63]. Generally, the better the coupling of the transformer, the lower the stray inductance and therefore, the lower the losses caused by the proximity effect [63], [68].

MF Transformer

The transformer is designed by a simplified approach, which is detailed in [69]. Firstly, a suitable core is chosen. In a second step, the maximum peak-to-peak flux density is defined, and from the datasheet, the core losses are estimated. After that, the minimum number of turns is calculated with Equation (6.7) to guarantee that the maximum flux density is not exceeded. The third step calculates the required diameter of the winding conductor to not exceed a previously defined current density. In a fourth step, the penetration depth at the chosen operating frequency is calculated and thereafter, the individual strand diameter of the Litz wire is selected from with Equality (6.10).

The core type chosen for the prototype converter is EPCOS E70/33/32 [70] with a effective cross-section Area of $A_{e,E70} = 676\,\mathrm{mm}^2$. The MF transformer is made up in an EE arrangement with two cores paralleled resulting in an effective cross-section area of $2\,A_{e,E70}$. The parameters of the designed transformer are listed in Table 6.3.

Tab. 6.3.: Parameters of the designed transformer for the prototype DAB converter

Variable	**Value**	**Description**
n	1	turns ratio
n_1	9	primary number of turns
n_2	9	secondary number of turns
k	0.997	coupling coefficient
$L_{\sigma,1}$	$1.2\,\mu\mathrm{H}$	primary-side leakage inductance
$L_{\sigma,2}$	$1.2\,\mu\mathrm{H}$	secondary-side leakage inductance
L_M	$420\,\mu\mathrm{H}$	magnetizing inductance
l_g	$200\,\mu\mathrm{m}$	air gap length
$n_{s,1}$	250	number of strands in a Litz bundle (primary-side winding)
$n_{s,2}$	250	number of strands in a Litz bundle (secondary-side winding)
$d_{s,1}$	$200\,\mu\mathrm{m}$	strand diameter (primary-side winding)
$d_{s,2}$	$200\,\mu\mathrm{m}$	strand diameter (secondary-side winding)
V_{trfm}	$320\,\mathrm{cm}^3$	boxed volume of the transformer

The volt-seconds of a periodic voltage v_{ac1}

$$\lambda_1 = \int_{t_0}^{t_1} v_{ac1}(t)dt \tag{6.3}$$

applied to the primary side to the transformer cause the flux density B to rise from its negative peak value to its positive if the voltage is positive and vice versa if the voltage is negative [71]. With Faraday's law of induction ($V = n\,{}^{\Delta\Phi}/_{\Delta t}$) the peak-to-peak flux density ($\Delta B = 2\,B_{max}$) equals to:

$$\Delta B = \frac{\lambda_1}{n_1\,A_e} \tag{6.4}$$

with the primary number of turns n_1 and the effective core cross-section area A_e.

The primary bridge voltage of a DAB converter modulated with the phase-shift modulation (clamping interval $w_1 = 0$) results in a square wave signal with the period $T = {}^1/_{f_s}$ and the voltage amplitude V_1. Therefore the volt-seconds from Equation (6.3) results in

$$\lambda_1 = \int_0^{T_s/2} V_1(t)dt = \frac{V_1\,T}{2} \tag{6.5}$$

and for the peak-to-peak flux density with (6.4) and (6.5) it holds:

$$\Delta B = \frac{V_1}{2\,f_s\,n_1\,A_e} \tag{6.6}$$

To reduce the maximum flux density, the number of turns can be increased or the effective cross-section area of the core can be increased. Hence the minimum number of turns, necessary to not exceed a defined maximum flux density deviation, is given by [69]:

$$n_{1,min} = (\frac{V_1}{2\,f_s\,\mathit{\Delta B}\,A_e}) \tag{6.7}$$

The size of the winding wire depends on the maximum RMS value of the current [69]. The maximum calculated RMS current (Equation (2.77)) occurs with the conventional phase-shift modulation. A current density of $S \in [2, 5]\mathrm{A\,mm^{-2}}$ is chosen, depending on the cooling and the thermal resistance of the core [69]. The wire diameter d_{wire} can then be calculated as follows:

$$d_{wire} = \sqrt{\frac{4\,I_{RMS}}{S\,\pi}} \tag{6.8}$$

Under high frequency operation the so called skin effect is present. This effect is caused by eddy currents which cause an uneven distribution of the current density inside the wire and thereby decreasing the effective cross-section of the wire. The greatest current distribution is present on the surface of the conductor with an exponentially decaying distribution towards the inside of the conductor [71]. Therefore the current flow is only present until a certain radial depth, defined as the penetration depth and is given, for a radial conductor, by [67]:

$$\delta = \sqrt{\frac{1}{\pi\, f_s\, \mu_0\, \sigma}} \tag{6.9}$$

with the natural permeability μ_0, the conductor conductivity σ and the switching frequency f_s.

It can be observed that the penetration depth is inversely proportional to $\sqrt{f_s\, \sigma}$, which indicates that the penetration depth decreases the better the conductor and the higher the switching frequency. Therefore Litz wire is used, which consists of multiple isolated strands. The diameter of the strands is chosen in such way that the diameter of the individual strands is smaller than the penetration depth defined above:

$$d_{strand} < \delta \tag{6.10}$$

MF Inductor

The determined stray inductance of the transformer, listed in Table 6.3, totals to $L_{\sigma,trfm} = 2.4\,\mu\text{H}$. The thereof resulting design parameter of the coupling inductors are listed in Table 6.4. It should be noted that the coupling inductor is split and connected to the primary and secondary side for reasons of symmetry.

Tab. 6.4.: Parameters of the designed inductors for the prototype DAB converter

Variable	Value	Description
n	5	number of turns
L	11 µH	magnetizing inductance
l_g	200 µm	air gap length
n_s	250	number of strands in a Litz bundle (primary-side winding)
d_s	200 µm	strand diameter (primary-side winding)
V_{ind}	320 cm^3	boxed volume of the transformer

Inductors, unlike transformers, store energy. The energy is stored in the core material and within the air gap as magnetic field energy. The energy stored in an inductor is defined as [72]

$$W_L = \frac{1}{2}\, L\, \hat{I}_L \tag{6.11}$$

with the inductance L and the peak inductor current $\hat{I}_L$.

The field energy is defined as [72]

$$W = \frac{1}{2} \int \vec{H}\, \vec{B}\, dV \tag{6.12}$$

where the integral is evaluated over the volume where a magnetic field is present [72]. With the assumption that of a constant magnetic flux density B and magnetic field H and that no fringing of the magnetic field is present, Equation (6.12) can be rewritten to

$$W = \frac{1}{2} \vec{H}_{core}\, \vec{B}_{core}\, V_{core} + \frac{1}{2} \vec{H}_{\delta}\, \vec{B}_{\delta}\, V_{\delta} \tag{6.13}$$

With Gauss's law for magnetism ($\nabla B = 0$) follows that the magnetic field density is continuous [72] and is hence equal in the core material and within the air gap:

$$\vec{B} \approx \vec{B}_{core} \approx \vec{B}_{\delta} \tag{6.14}$$

If the material of magnetic field presence is paramagnetic or diamagnetic a linear equation exists that links B to H and it holds [72]:

$$\vec{B} = \mu_0\, \mu_r\, \vec{H} \tag{6.15}$$

By substituting (6.14) and (6.15) into Equation (6.13) and defining $V_{core} = l_{core}\, A$ and $V_{\delta} = l_{\delta}\, A$ the magnetic field energy can be rewritten to

$$W = \frac{1}{2} \frac{B^2}{\mu_0} \left(\frac{l_{core}}{\mu_r} + \delta \right) A \tag{6.16}$$

with l_{core} being the effective magnetic path length of the core, A the core cross section area and δ the air gap length.

The relative permeability of the core material is significantly larger than the natural permeability ($\mu_r >> \mu_0$) [66] and Equation (6.16) can be thus simplified to [69]:

$$W \approx \frac{1}{2} \frac{B^2\, A\, \delta}{\mu_0} \tag{6.17}$$

It can therefore be noted that the energy is mainly stored in the air gap and not the core material. The inductor thus needs an air gap volume to store the required energy and with Equation (6.11) the minimum required air gap length is given as [69]:

$$\delta_{min} = \frac{L\, \hat{I}_L^{\,2}\, \mu_0}{B_{max}^2\, A} \tag{6.18}$$

The minimum number of turns is then calculated by [66]

$$n_{min} = \sqrt{\frac{L}{A_L(\delta)}} \tag{6.19}$$

with the magnetic conductance $A_L(\delta)$ specified in the data sheet [66].

Lastly the resulting magnetic flux density is calculated to verify that the maximum defined magnetic flux density is not exceeded [69].

$$B = \frac{n\,A_L\,\hat{I_L}^2}{A_{min}} \tag{6.20}$$

As the coupling inductor and the transformer are connected in series, the operating frequency f_s and the RMS current are identical. Therefore, the design procedure of the Litz wire is as described for the MF transformer.

Semiconductor Switches

The DAB converter has the ability to ensure ZVS on all semiconductor switches. It is shown in Chapter 7 that the overall losses of the semiconductor switches are mainly caused by the static losses, due to the reduced dynamic losses by the ZVS transitions (cf. Figure 7.11). Therefore the losses of the semiconductor switches are mainly caused by the on-resistance $R_{DS,on}$ of the MOSFET channel. The conduction losses of a MOSFET are defined as

$$P_{FET,cond} = I_{T,RMS}^2\,R_{DS,on} \tag{6.21}$$

Therefore a semiconductor switch is chosen that has a low on-resistance $R_{DS,on}$ and is suited for resonant topologies. The CFD2 Series MOSFETs from Infineon Technologies is specially designed for resonant topologies and has an improved body-diode characteristic [57]. As described in Section 3.2.2, MOSFETs with a fast reverse recovery body diode and high commutation ruggedness should be chosen for resonant topologies [55]. The DAB converter loses ZVS under certain operating conditions. This results in high peak drain currents during the switching transition and could destroy the semiconductor device over time if a poorly suited device is chosen [55].

Figure 6.4 depicts the junction temperature dependant on-resistance of the CFD2 Mosfet of the model IWP65R041CFD. The on-resistance of the silicon carbide MOSFET C3M0065090D is shown for reference. It can be observed that the silicon carbide MOSFET's on-resistance is more stable with a change in junction temperature, but the overall resistance is higher with the break-even point at approximately $T_j = 110\,°\mathrm{C}$.

The switching transitions and the therewith generated switching losses are detailed and analysed in-depth in Chapter 7.

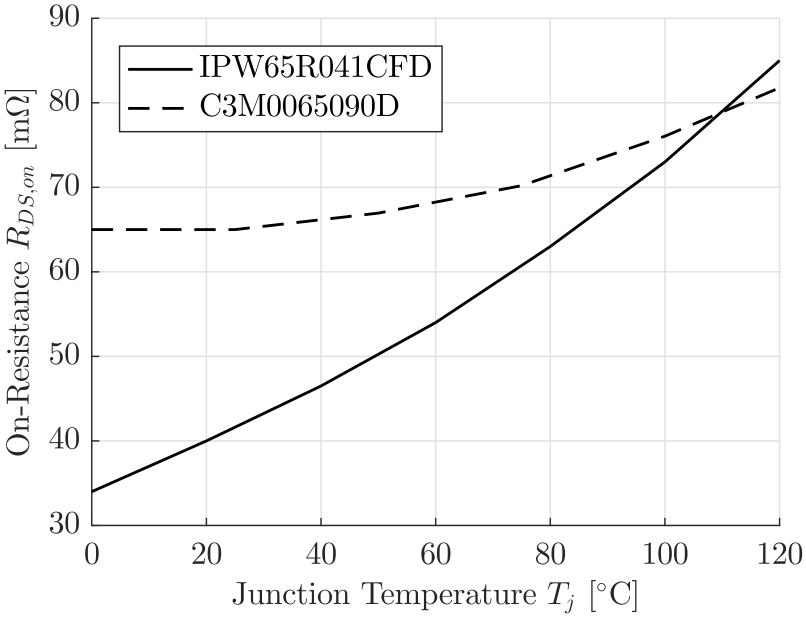


Fig. 6.4.: On resistance as a function of the junction temperature of the silicon MOSFET IPW65R041CFD and the silicon carbide MOSFET C3M0065090D.

6.2. Conclusion

The design parameters of the 5 kVA prototype converter are listed in this Chapter and the schematic hardware overview is presented. The main components are sized to allow the converter to operate within the given parameters. Lastly the magnetic components are designed and the semiconductor switches are chosen.

7. Experimental Verification

In the present Chapter the operation of a DAB converter modulated with the derived modulation schemes and the technical design is verified with the measurement results of the 5 kVA DAB prototype converter (cf. Chapter 6). The results of the converter operated as a DC-DC converter are presented first: In a first step, the operational functionality of the non-isolated (bypassing of MF transformer) DAB converter is described and thereafter the isolated DAB converter is detailed. Both versions are modulated with the combined modulation scheme, and hence the derived and calculated optimal modulation parameters are implemented. Lastly, the measured current and voltage waveforms of the non-isolated and isolated operation are compared to the calculated waveforms.

In a second step, the transient behaviour of the DAB converter is analysed. The switching losses of a hard and soft switching transition at different load currents are detailed. The reduced switching losses during a hard transition and the increased switching speed of the silicon carbide MOSFETs are shown.

Lastly, the experimental operation of a AC-AC DAB converter is presented: The experimental results of the two operating modes, namely the active and reactive power operation, are detailed and the drawback of the reactive power operation is visualised.

7.1. DC-DC DAB Converter

For the verification of the calculated optimal modulation parameters of the combined modulation scheme, an input voltage of $V_1 = 138\,\mathrm{V}$ and an output voltage of $V_2 = 230\,\mathrm{V}$ are chosen for the experimental measurements. This corresponds to the voltage ratio chosen for the presented calculations and simulations and thus makes a direct comparison possible.

7.1.1. Non-isolated DAB converter

The derived optimal parameters of the combined modulation scheme are calculated by means of the DAB converter model that only takes conduction losses into consideration and assumes all other components to be ideal. Thus also neglecting the magnetizing current of the transformer. To verify the calculated current and voltage waveforms, the resonant MF tank of the experimental converter is connected as depicted in Figure 7.1. The transformer is bypassed resulting in a series connection of the primary and secondary coupling inductors L_{c1} and L_{c2} and it holds:

$$i_L = i_{ac1} = i_{ac2} \tag{7.1}$$

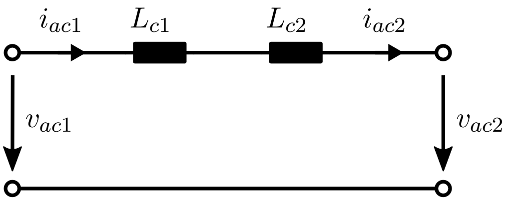
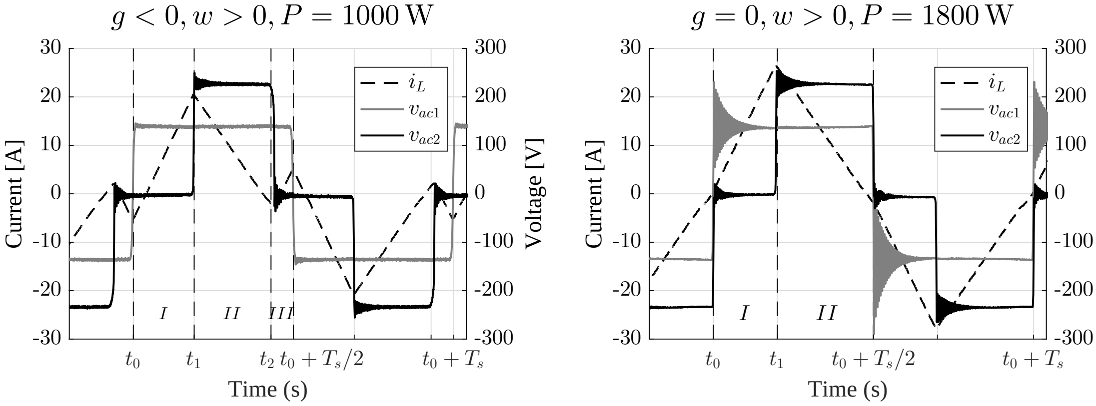


Fig. 7.1.: Reactive MF network of the non-isolated DAB converter. Transformer shorted resulting in a series connection of L_{c1} and L_{c2} with $i_{ac1} = i_{ac2} = i_L$

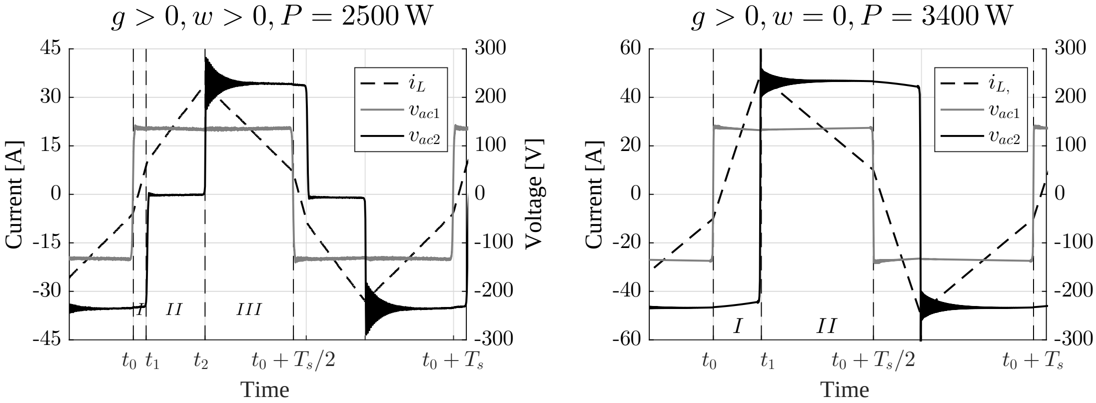
The measured voltage and current waveforms of the reactive MF circuit of the non-isolated DAB converter are shown in Figure 7.2. The Figure shows the four possible operating states of the combined modulation scheme with an input voltage of $V_1 = 138\,\mathrm{V}$ and an output voltage of $V_2 = 230\,\mathrm{V}$: Case I of the one-sided clamped modulation with $g < 0 \wedge w > 0$ (a), Case II with $g > 0 \wedge w > 0$ (c), the transition of Case I to II and vice versa of the one-sided clamped modulation with $g = 0 \wedge w > 0$ (b) and the conventional phase-shift modulation with $g > 0 \wedge w = 0$(d). It is apparent that ZVS on all power electronic switches is present in (a), (c) and (d) and resonant switching in (b).

The inductor RMS currents $I_{L,RMS}$ of the depicted waveforms of Figure 7.2 and the calculated values at the corresponding operating points are listed in Table 7.1. It can be seen that a good correlation of the measured to the simulated values is present.



(a) One-sided clamped modulation Case I ($g < 0$)

(b) Transition between Case I and Case II of the one-sided clamped modulation ($g = 0$)



(c) One-sided clamped modulation Case II ($g > 0$)

(d) Conventional phase-shift modulation with $w = 0$

Fig. 7.2.: Measured current and voltage waveforms of the possible operating states of the combined modulation scheme of the non-isolated DAB converter with $V_1 = 138\,\mathrm{V}$ and $V_2 = 230\,\mathrm{V}$: The one-sided clamped modulation with $g < 0$ (a) and $g > 0$ (c), the transition thereof with $g = 0$ (b) and the conventional phase-shift modulation (d). ZVS on all power electronic switches in (a), (c) and (d) and resonant switching in (b).

Tab. 7.1.: Calculated and measured inductor RMS current at power levels P_2 with $V_1 = 138\,\mathrm{V}$ and $V_2 = 230\,\mathrm{V}$

Operating Point	**Unit**	**Measurement**	**Calculation**
$P_2 = 1000\,\mathrm{W}$ $g < 0 \wedge w > 0$	$I_{L,RMS}$	10.3 A	10.4 AA
$P_2 = 1720\,\mathrm{W}$ $g = 0 \wedge w > 0$	$I_{L,RMS}$	15.2 A	15.6 A
$P_2 = 2500\,\mathrm{W}$ $g > 0 \wedge w > 0$	$I_{L,RMS}$	22.0 A	22.1 A
$P_2 = 3400\,\mathrm{W}$ $g > 0 \wedge w = 0$	$I_{L,RMS}$	32.9 A	32.6 A

7.1.2. Isolated DAB converter

The magnetizing inductance L_m of the transformer in the reactive network (cf. Figure 5.3) causes a magnetizing current i_{Lm} to flow. With the presence of a ferromagnetic core material (causing a magnetizing current) not only are additional losses introduced to the system but more importantly (for terms of calculation of the voltage and current waveforms of the reactive MF network) the equality $i_{ac1} = i_{ac2}/n$ (cf. Equation (2.2)) no longer finds validity and it follows:

$$i_{Lm} = i_{ac1} - i_{ac2}/n \tag{7.2}$$

The influence of the transformer is depicted in Figure 7.3. The Figure shows the voltage and current waveforms of a non-isolated and an isolated DAB converter at the same operating point with an input voltage and output voltage of $V_1 = V_2 = 230\,\mathrm{V}$ and a transferred output power of $P_2 = 3300\,\mathrm{W}$. i_L denotes the inductor current of the non-isolated version and $i_{L,prim}$ and $i_{L,sec}$ refer to the primary and secondary transformer current of the isolated version respectively. The calculated magnetizing current (cf. Equation (7.2)) of the prototype transformer is referred to as i_{Lm}.

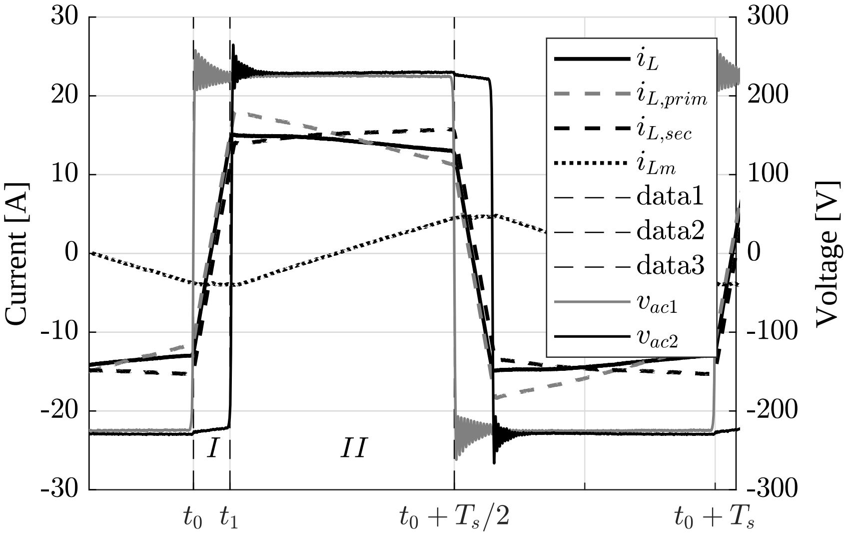


Fig. 7.3.: Measured results of a DC-DC DAB converter modulated with the combined modulation scheme with $g > 0.07 \wedge w = 0$, $V_1 = 230\,\mathrm{V}$, $V_2 = 200\,\mathrm{V}$, $P_2 = 3300\,\mathrm{W}$, $f_s = 40\,\mathrm{kHz}$ and $L = 24\,\mu\mathrm{H}$. i_L denotes the inductor current of the non-isolated DAB converter. $i_{L,prim}$ and $i_{L,prim}$ refer to the isolated DAB converter with the difference being the magnetizing current of the transformer i_{Lm}.

It is clearly visible that due to the presence of the transformer magnetizing current the current slopes the primary and secondary transformer currents in Region II differ, whereas no effect on the bridge voltages v_{ac1} and v_{ac2} can be recorded. It follows for the conventional phase-shift modulation:

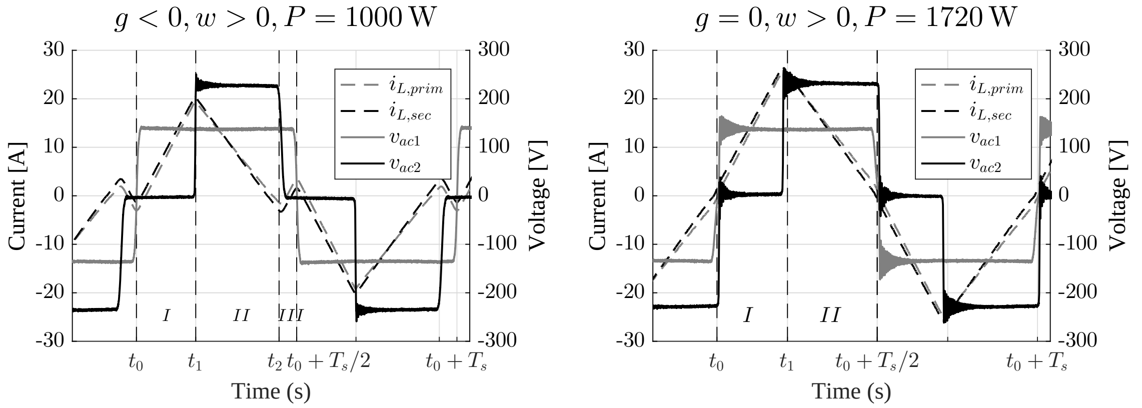
$$\begin{aligned} i_{L,prim}(t_0) &\neq i_{L,sec}(t_0) \\ i_{L,prim}(t_1) &\neq i_{L,sec}(t_1) \end{aligned} \tag{7.3}$$

and for the one-sided clamped modulation:

$$\begin{aligned} i_{L,prim}(t_0) &\neq i_{L,sec}(t_0) \\ i_{L,prim}(t_1) &\neq i_{L,sec}(t_1) \\ i_{L,prim}(t_2) &\neq i_{L,sec}(t_2) \end{aligned} \tag{7.4}$$

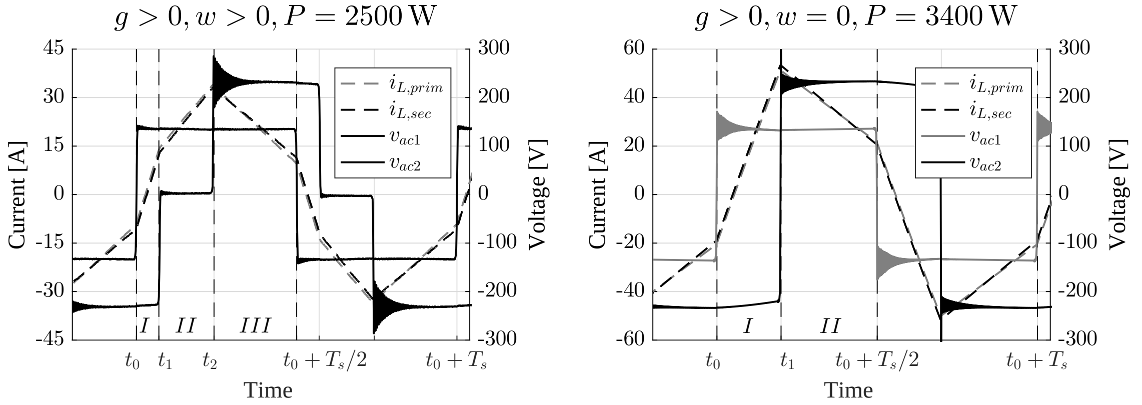
It should be noted that due to Equalities (7.3) and (7.4) the constraints for ZVS may not be fulfilled for both the primary and secondary half-bridge circuits in the low-power region, when the inductor currents at the switching times t_0, t_1 and t_2 are close to zero. This may lead to not sufficient energy being available in the resonant circuit during the switching transition. The measured voltage and current waveforms of the reactive MF circuit of the isolated DAB converter are shown in Figure 7.4. The four possible operating states of the combined modulation scheme are visualised. The primary and secondary inductor currents $i_{L,prim}$ and $i_{L,sec}$ are shown, and the effect of the magnetising current is apparent.

The measured efficiency of the DAB converter modulated with the conventional phase-shift modulation and combined modulation scheme are depicted in Figure 7.5, denoted as $ps, meas$ and $opt, meas$ respectively. The simulated efficiency curves are plotted for comparison purposes and are referred to as ps, sim and opt, sim for the phase-shift and combined modulated converter respectively. The measured efficiency points show a good match to the simulated efficiency curve. The distinct efficiency dip of the combined modulation scheme, caused by the change of polarity of the phase-shift g as described in Section 5.1.1, is confirmed by the measured results.



(a) One-sided clamped modulation Case I ($g < 0$)

(b) Transition between Case I and Case II of the one-sided clamped modulation ($g = 0$)



(c) One-sided clamped modulation Case II ($g > 0$)

(d) Conventional phase-shift modulation with $w = 0$

Fig. 7.4.: Measured current and voltage waveforms of the possible operating states of the combined modulation scheme of the isolated DAB converter with $V_1 = 138\,\mathrm{V}$ and $V_2 = 230\,\mathrm{V}$. The primary and secondary inducor currents $i_{L,prim}$ and $i_{L,sec}$ are shown. The one-sided clamped modulation with $g < 0$ (a) and $g > 0$ (c), the transition thereof with $g = 0$ (b) and the conventional phase-shift modulation (d). ZVS on all power electronic switches in (a), (c) and (d) and resonant switching in (b).

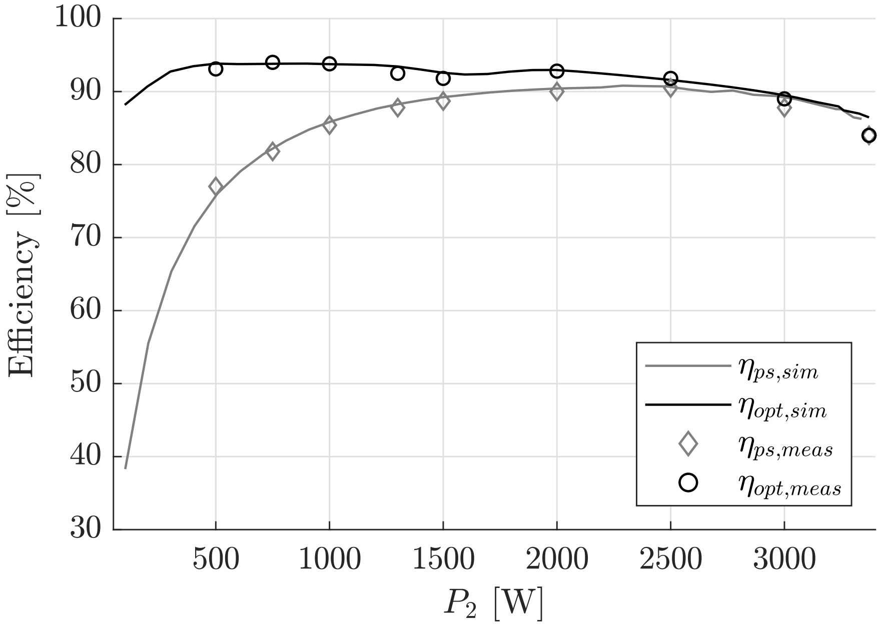


Fig. 7.5.: Measured efficiencies of a DC-DC DAB converter modulated with the conventional phase-shift modulation ($\eta_{ps,meas}$) and the combined modulation scheme ($\eta_{opt,meas}$) in relation to the transferred output power. The simulated efficiencies are shown for comparison purposes and are referred to as $\eta_{ps,sim}$ and $\eta_{opt,sim}$ for the phase-shift modulation and the combined modulation scheme respectively.

Optimum Efficiency

The measured voltage and current waveforms of a DC-DC DAB converter modulated with the conventional phase-shift modulation with $V_1 = V_2 = 230\,\mathrm{V}$ and the maximum achievable efficiency of the prototype converter is shown in Figure 7.6. The bridge voltages v_{ac1} and v_{ac2}, the primary and secondary inductor currents $i_{L,prim}$ and $i_{L,sec}$, the drain-source $v_{DS,x}$ and the gate-source $v_{GS,x}$ voltages are visualized, where $x \in [1, 8]$ the eight MOSFET switches of the two full-bridge circuits denotes. The maximum achievable experimental converter efficiency resulted in $\eta_{max} = 98.1\,\%$.

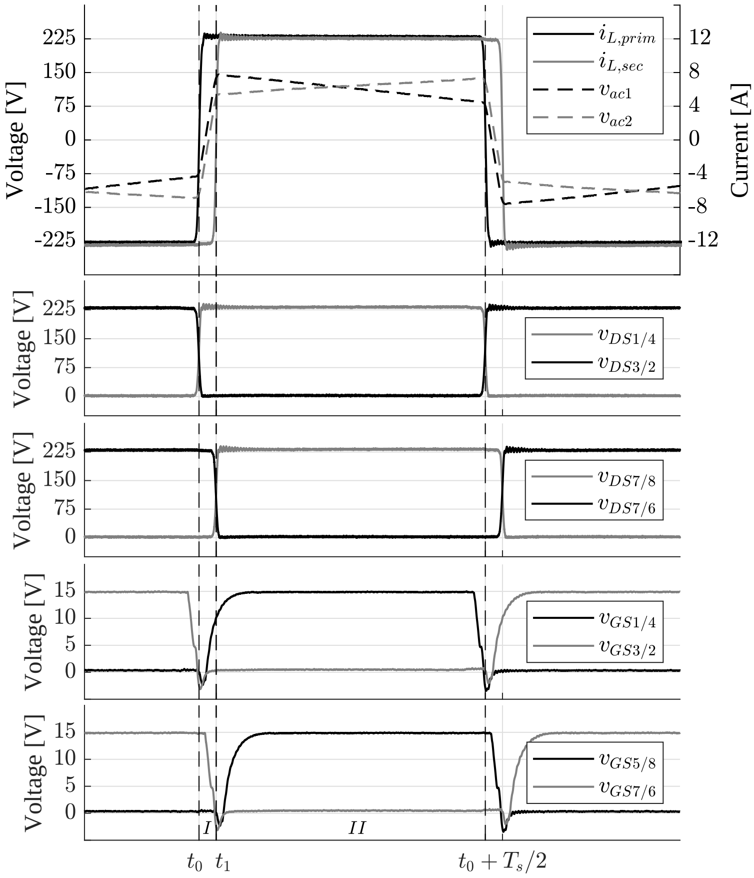


Fig. 7.6.: Measured voltage and current waveforms of the reactive MF circuit, the MOSFET drain-source $v_{DS,x}$ and the gate-source $v_{GS,x}$ voltages ($x \in [1, 8]$ denotes the eight MOSFET switches) of a DC-DC DAB converter modulated with the phase-shift modulation with $g = 0.03 \wedge w = 0$, $V_1 = 230\,\mathrm{V}$, $V_2 = 230\,\mathrm{V}$,$P_2 = 1300\,\mathrm{W}$, $f_s = 40\,\mathrm{kHz}$, $L = 24\,\mu\mathrm{Hz}$ and the maximum achievable experimental converter efficiency of $\eta_{max} = 98.1\,\%$

7.1.3. Comparison of experimental Results

Table 7.2 lists the calculated, simulated and measured inductor RMS currents $I_{L,RMS,prim}$ and $I_{L,RMS,sec}$ and the converter efficiency η at different output power levels P_2 and with an input voltage of $V_1 = 138\,\mathrm{V}$ and an output voltage $V_2 = 230\,\mathrm{V}$. Each power level refers to one operating point within the three regions (Region I with $g < 0 \wedge w > 0$, Region II with $g > 0 \wedge w > 0$ and Region III with $g > 0 \wedge w = 0$) and the transition from Region I to Region II with $g = 0 \wedge w > 0$ of the combined modulation scheme.

The corresponding relevant waveforms of the MF-tank of the operating points listed in Table 7.2 are shown in Figures 7.7, 7.8, 7.9 and 7.10 referring to Region I, the transition from Region I to Region II, Region II and Region III respectively.

A comparison of the RMS currents listed in Table 7.2 shows a good match of the calculated to the measured results. Due to the presence of the magnetising current of the transformer, the primary and secondary inductor RMS currents differ slightly, whereas the DAB model with conduction losses only one value provides. The measured results are well within the range of the calculated values. Therefore it can be concluded that the DAB model neglecting the magnetising current provides acceptable accuracy.

Tab. 7.2.: Comparison of measured, simulated and calculated results of a DC-DC DAB converter modulated with the combined modulation scheme at different power levels P_2 with $V_1 = 138\,\mathrm{V}$ and $V_2 = 230\,\mathrm{V}$

Operating Point	Unit	Measurement	Simulation	Calculation
$P_2 = 1000\,\mathrm{W}$ Region I $g < 0 \wedge w > 0$	$I_{L,RMS,prim}$	9.9 A	10.0 A	10.4 A
	$I_{L,RMS,sec}$	10.5 A	10.6 A	
	η	96.3 %	96.8 %	96.5 %
$P_2 = 1720\,\mathrm{W}$ Region I → II $g = 0 \wedge w > 0$	$I_{L,RMS,prim}$	14.9 A	14.9 A	15.2 A
	$I_{L,RMS,sec}$	15.2 A	15.5 A	
	η	95.2 %	94.5 %	95.6 %
$P_2 = 2500\,\mathrm{W}$ Region II $g > 0 \wedge w > 0$	$I_{L,RMS,prim}$	21.9 A	22.2 A	22.0 A
	$I_{L,RMS,sec}$	21.5 A	21.5 A	
	η	94.8 %	93.9 %	95.0 %%
3400 W Region III $g > 0 \wedge w = 0$	$I_{L,RMS,prim}$	33.2 A	33.0 A	32.9 A
	$I_{L,RMS,sec}$	33.9 A	33.8 A	
	η	88.4 %	88.7 %	89.1 %

From Figures 7.7, 7.8, 7.9 and 7.10 the resonant nature of the transitions during the dead-time can be seen. The model from which the calculated values are derived, assumes instantaneous voltage transitions, whereas the simulated and measured waveforms clearly show the distinct charging/discharging voltage curves of a capacitor (charging/discharging of the ouput capacitance of the MOSFETs). Especially in the low-power region (low current and less energy stored in the resonant tank during dead-time, cf. Figure 7.10) the resonant transitions are distinct and are clearly visible. With increasing power the voltage transitions become faster, due to faster charging/discharging of the output capacitances, as more energy becomes available during the dead-time (cf. Figure 7.10). Nevertheless it can be concluded that the DAB model with conduction losses delivers an accurate computation of the inductor currents.

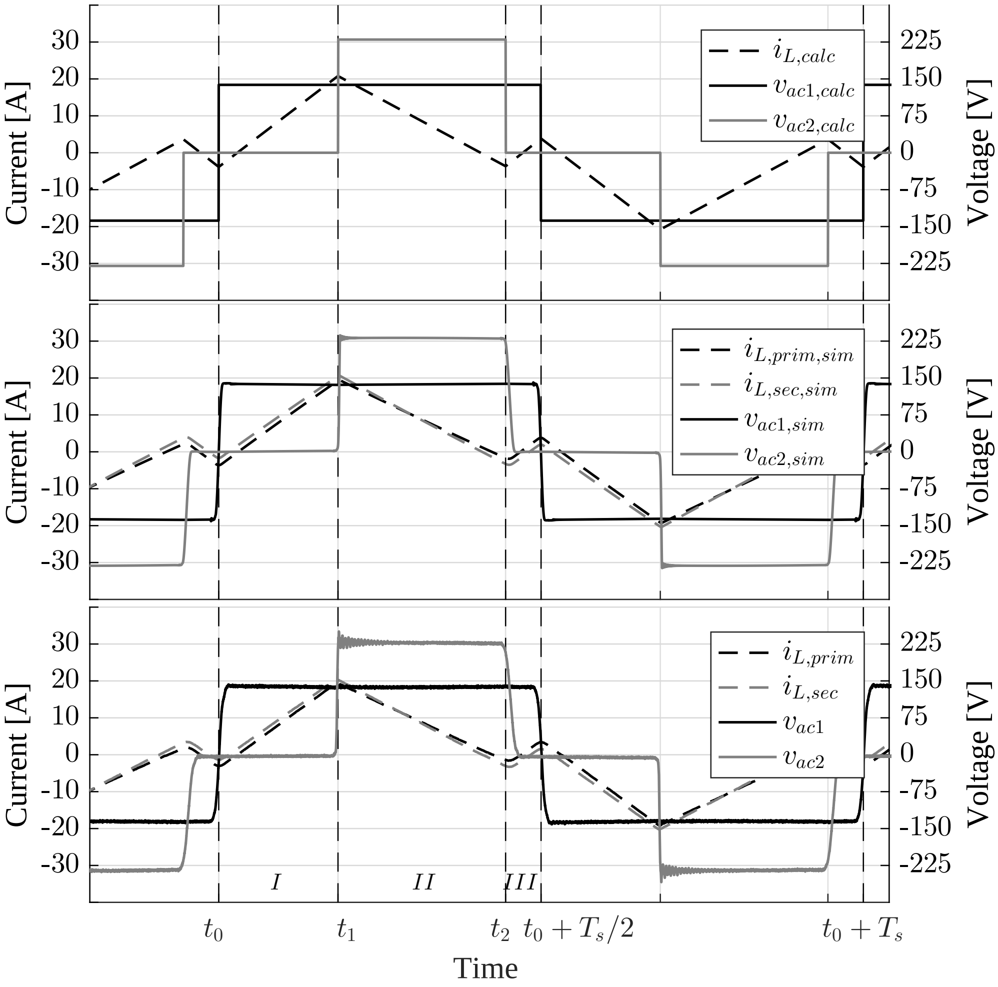


Fig. 7.7.: Calculated ($i_{L,calc}$, $v_{ac1,calc}$, $v_{ac2,calc}$), simulated ($i_{L,prim,sim}$, $i_{L,sec,sim}$, $v_{ac1,sim}$, $v_{ac2,sim}$) and measured ($i_{L,prim}$, $i_{L,sec}$, v_{ac1}, v_{ac2}) results of a DC-DC DAB converter modulated with the combined modulation scheme with $g < 0 \wedge w > 0$, $V_1 = 138\,\mathrm{V}$, $V_2 = 230\,\mathrm{V}$,$P_2 = 1000\,\mathrm{W}$, $f_s = 40\,\mathrm{kHz}$ and $L = 24\,\mu\mathrm{H}$. The converter efficiencies result to $\eta_{calc} = 96.5\,\%$, $\eta_{sim} = 96.8\,\%$ and $\eta_{meas} = 96.3\,\%$

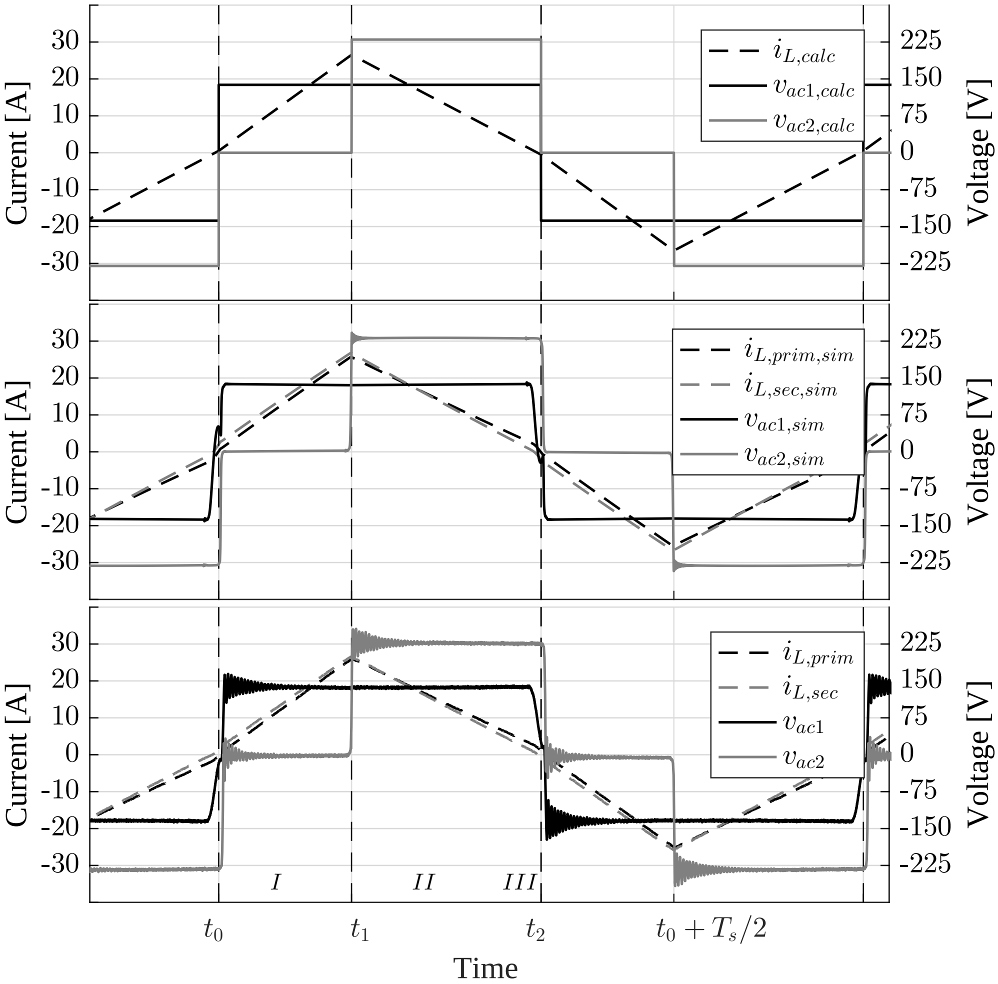


Fig. 7.8.: Calculated ($i_{L,calc}$, $v_{ac1,calc}$, $v_{ac2,calc}$), simulated ($i_{L,prim,sim}$, $i_{L,sec,sim}$, $v_{ac1,sim}$, $v_{ac2,sim}$) and measured ($i_{L,prim}$, $i_{L,sec}$, v_{ac1}, v_{ac2}) results of a DC-DC DAB converter modulated with the combined modulation scheme with $g = 0 \wedge w > 0$, $V_1 = 138\,\text{V}$, $V_2 = 230\,\text{V}$,$P_2 = 1720\,\text{W}$, $f_s = 40\,\text{kHz}$ and $L = 24\,\mu\text{H}$. The converter efficiencies result to $\eta_{calc} = 95.6\,\%$, $\eta_{sim} = 94.5\,\%$ and $\eta_{meas} = 95.2\,\%$

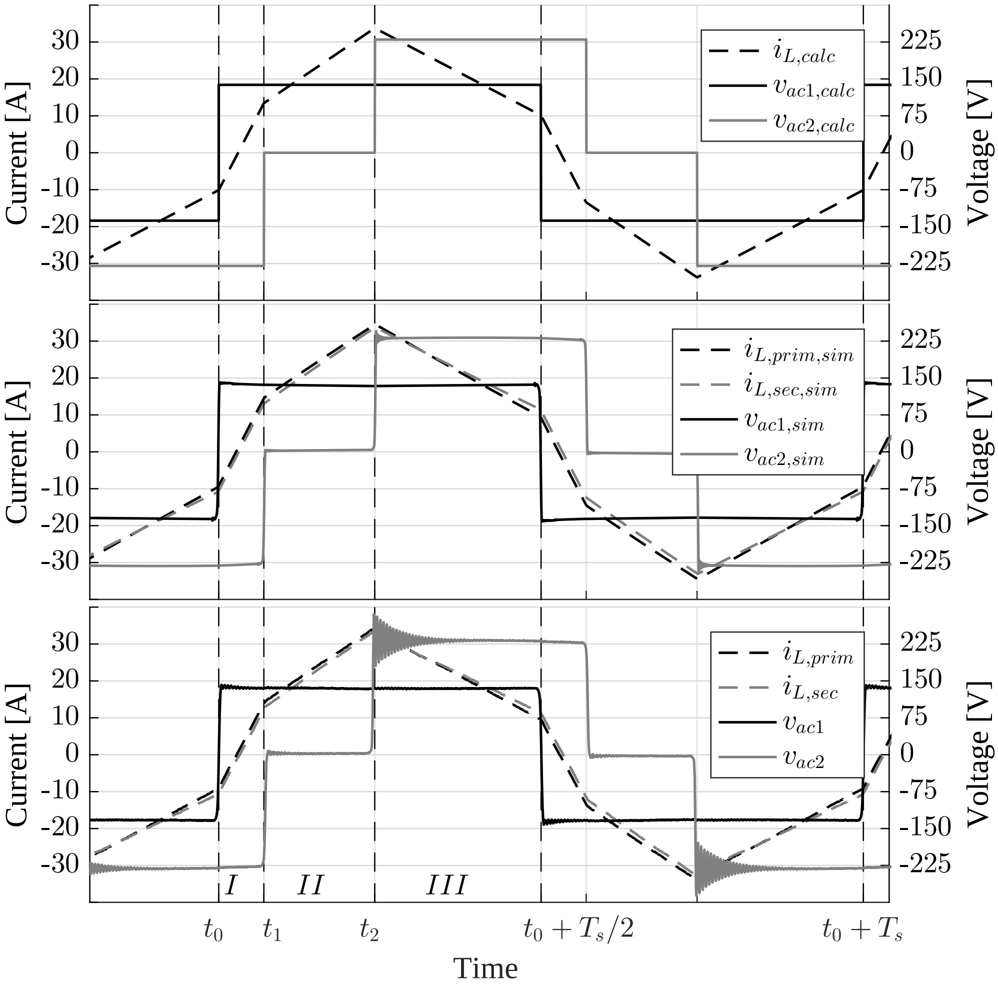


Fig. 7.9.: Calculated ($i_{L,calc}$, $v_{ac1,calc}$, $v_{ac2,calc}$), simulated ($i_{L,prim,sim}$, $i_{L,sec,sim}$, $v_{ac1,sim}$, $v_{ac2,sim}$) and measured ($i_{L,prim}$, $i_{L,sec}$, v_{ac1}, v_{ac2}) results of a DC-DC DAB converter modulated with the combined modulation scheme with $g > 0 \land w > 0$, $V_1 = 138\,\mathrm{V}$, $V_2 = 230\,\mathrm{V}$,$P_2 = 2500\,\mathrm{W}$, $f_s = 40\,\mathrm{kHz}$ and $L = 24\,\mathrm{\mu H}$. The converter efficiencies result to $\eta_{calc} = 95.0\,\%$, $\eta_{sim} = 93.9\,\%$ and $\eta_{meas} = 94.8\,\%$

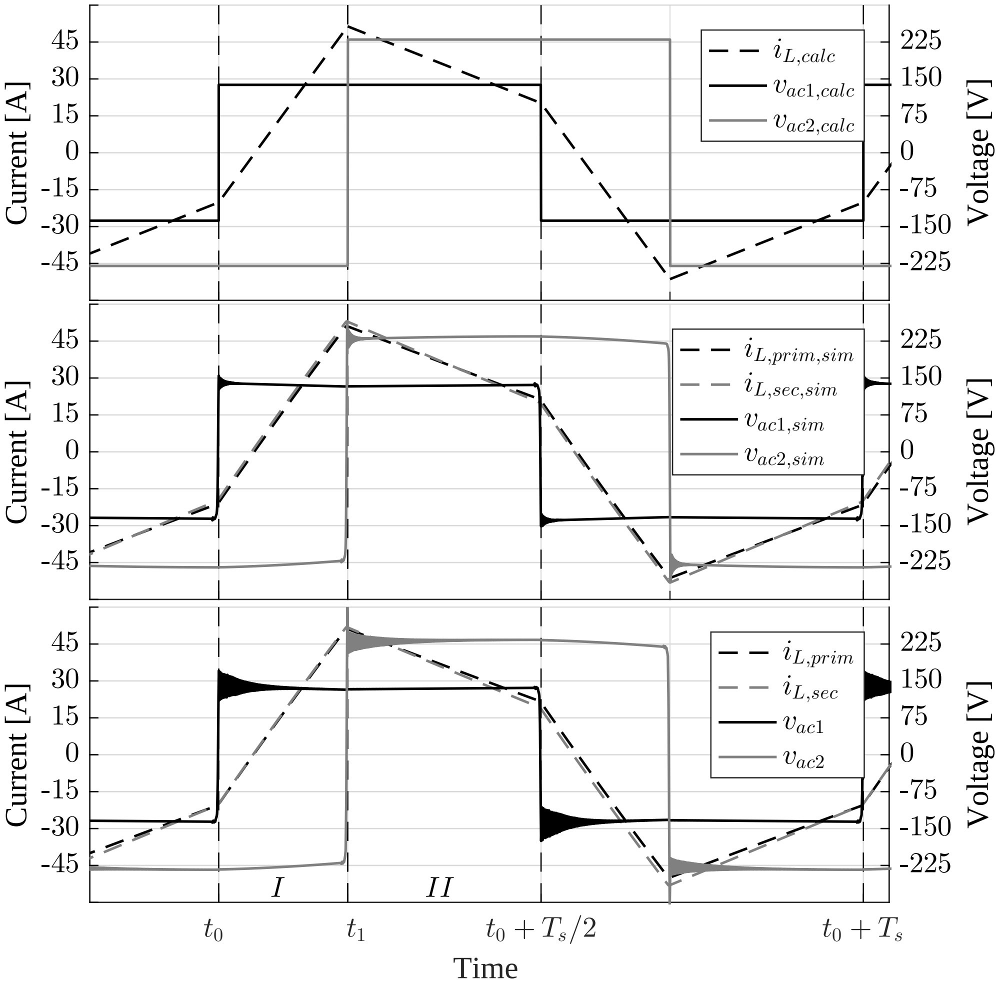


Fig. 7.10.: Calculated ($i_{L,calc}$, $v_{ac1,calc}$, $v_{ac2,calc}$), simulated ($i_{L,prim,sim}$, $i_{L,sec,sim}$, $v_{ac1,sim}$, $v_{ac2,sim}$) and measured ($i_{L,prim}$, $i_{L,sec}$, v_{ac1}, v_{ac2}) results of a DC-DC DAB converter modulated with the combined modulation scheme with $g > 0 \wedge w > 0$, $V_1 = 138\,\text{V}$, $V_2 = 230\,\text{V}$,$P_2 = 3400\,\text{W}$, $f_s = 40\,\text{kHz}$ and $L = 24\,\mu\text{H}$. The converter efficiencies result to $\eta_{calc} = 89.1\,\%$, $\eta_{sim} = 88.7\,\%$ and $\eta_{meas} = 88.4\,\%\%$

7.2. Transient Analyses of the DAB Converter

The transient behaviour of the DAB converter is analysed. The hard and soft switching transitions are described, and the losses caused thereby are shown and compared.

The silicon carbide (SiC) MOSFET is introduced, and the switching behaviour and losses are compared to the Si MOSFET.

7.2.1. Switching losses

The losses produced by a hard switching transition are described below. The turn-on and turn-off loss energy is calculated from the measured power dissipated during the relevant switching transition. Firstly the silicon MOSFET is analysed, and thereafter the losses of a silicon carbide MOSFET are detailed. Then the effect of the gate resistance on the turn-on behaviour and the switching losses for both the Si and the SiC MOSFET is analysed.

The chosen semiconductor devices, the Si MOSFET IPW65R041CFD from Infineon Technologies, and the SiC MOSFET C3M0065090D from CREE and their most important parameters are listed in Table 7.3.

Tab. 7.3.: Si and SiC MOSFET

Decive	**Technology**	V_{DS}	$R_{DS,on}$	C_{oss}	Q_g	Q_{rr}
IPW65R041CFD	Si	$700\,V$	$49\,\mathrm{m\Omega}$	$400\,\mathrm{pF}$	$300\,\mathrm{nC}$	$1900\,\mathrm{nC}$
C3M0065090D	SiC	$900\,V$	$65\,\mathrm{m\Omega}$	$60\,\mathrm{pF}$	$7.5\,\mathrm{nC}$	$150\,\mathrm{nC}$

The switching transitions of the two semiconductor devices are characterised by the double pulse test. The experimental set-up is made up from the prototype PCB with the half-bridge circuit consisting of T_1 and T_3 of the prototype PCB to determine the switching losses of the prototype converter accurately.

The experimental half-bridge set-up is discussed in detail in Appendix B.

In the double pulse test set-up the switching transitions of the low-side MOSFET T_3 (DUT) are analysed the generated instantaneous power p_x and the loss-energy E_x are computed, where x being either *on* for the turn-on transition or off referring to the turn-off transition. As only the DUT is of interest the drain-source voltage and the drain-current of the DUT are referred to by the simplified description as follows:

$$\begin{aligned} v_{DS,T3} &= v_{DS} \\ i_{D,T3} &= i_D \end{aligned} \tag{7.5}$$

The instantaneous switching loss power $p(t)$ is calculated by Equation (3.5) and the loss energy E is acquired by computing the integral over $p(t)$ from the start to the end of the switching transition and is given by (3.6). The average switching losses are obtained with (3.7) by multiplying the loss energy with the switching frequency of the converter (cf. Section 3.2).

Silicon MOSFET

Figure 7.12 presents the turn-on and turn-off switching transition of the Si MOSFET IPW65R041CFD at a supply voltage of $V_1 = 230V$ and at the load currents of $i_L = [10, 20, 30]\,A$. The drain-source voltage v_{DS}, the drain current i_D, the generated switching loss p_x and the loss energy E_x of the turn-on ($x = on$) and the turn-off ($x = off$) transition are visualized.

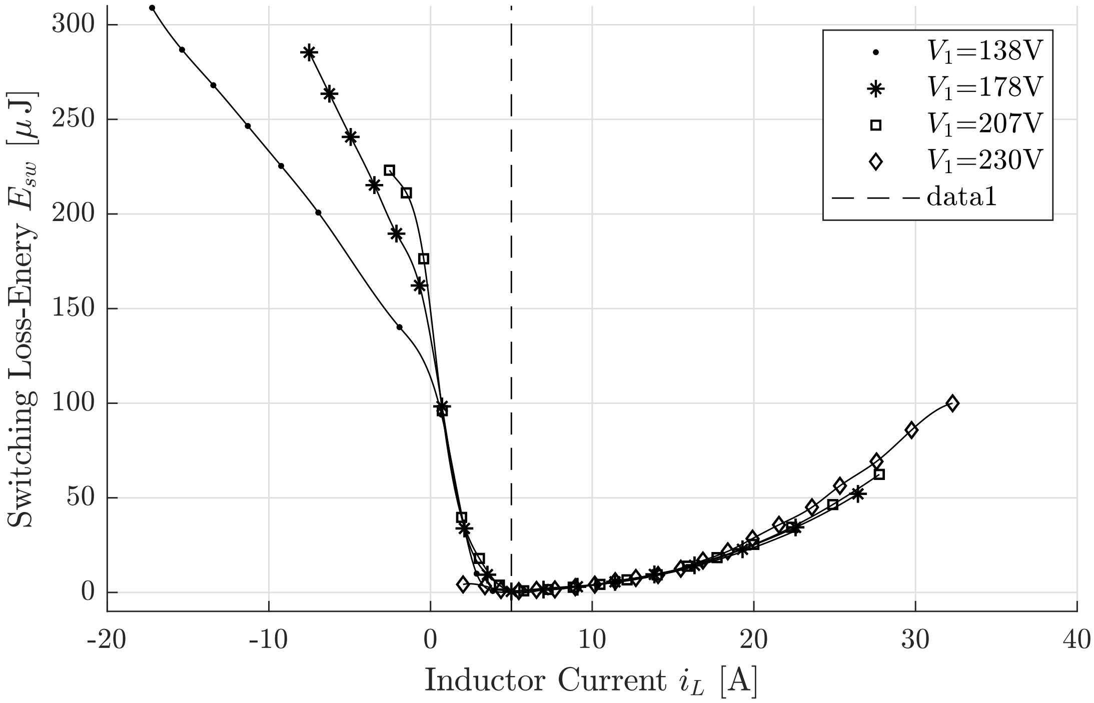


Fig. 7.11.: Total switching loss-energy $E_{sw} = E_{on} + E_{off}$ plotted against the inductor current with the input voltage V_1 as a parameter. In the region $0 \leq i_L < 5$ A partial charging/discharging of the output capacitance is achieved. At $i_L = 5$ A the ZVS constraint ($i_L(t_0) > I_{c,min}$) is satisfied and the loss-energy reaches its minimum. Thereafter the loss-energy increases again with an increase in inductor current. The turn-on losses dominate the hard-switching region ($i_L(t_0) < I_{c,min}$), whereas the turn-off losses are the main contributor to the ZVS region ($i_L(t_0) > I_{c,min}$).

The total switching loss energy $E_{sw} = E_{on} + E_{off}$ plotted against the inductor current i_L and with the input voltage as a parameter and with an output voltage of $V_2 = 230\,\mathrm{V}$ is shown in Figure 7.11. The losses are measured at T_3 from the prototype converter operated as a DC-DC converter and modulated with the conventional phase shift modulation. The output power is increased from zero to $P_{PS,max}$ and the drain-source voltage and the drain current are measured at the switching time t_0.

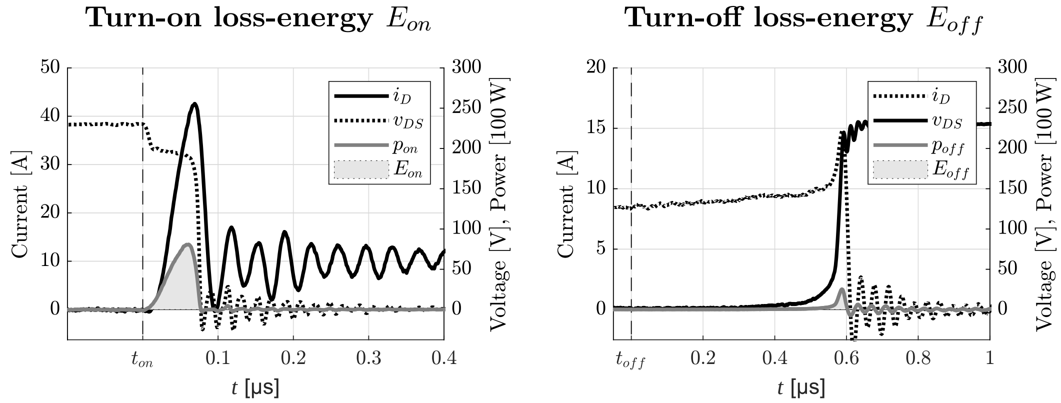
The greater the voltage ratio $d = n\,V_2/V_1$, the higher are the total switching losses with $i_L < 0$. As the inductor current changes polarity, energy becomes available in the resonant tank to move the charges during the dead-time. This results in a partial charging/discharging of the output capacitances of the MOSFETs $(0 < v_{DS}(t_0) < V_1)$ and with rising i_L more energy becomes available. Hence, the loss-energy decreases and reaches its minimum at $i_L = 5\,\mathrm{A}$, when the ZVS constraint for the primary half-bridges is satisfied ($i_L(t_0) > I_{c,min}$, cf. Table 5.1). Thereafter the loss-energy increases again, as the inductor current increases. The rate though, at which the losses increase in relation to the inductor current ($i_L > 5\,\mathrm{A}$) is less than compared to the rate with $i_L < 5\,\mathrm{A}$. This is explained thereby that the turn-on losses dominate the hard-switching region ($i_L(t_0) < I_{c,min}$), whereas the turn-off losses are the main contributor to the ZVS region ($i_L(t_0) > I_{c,min}$).

Silicon Carbide (SiC)

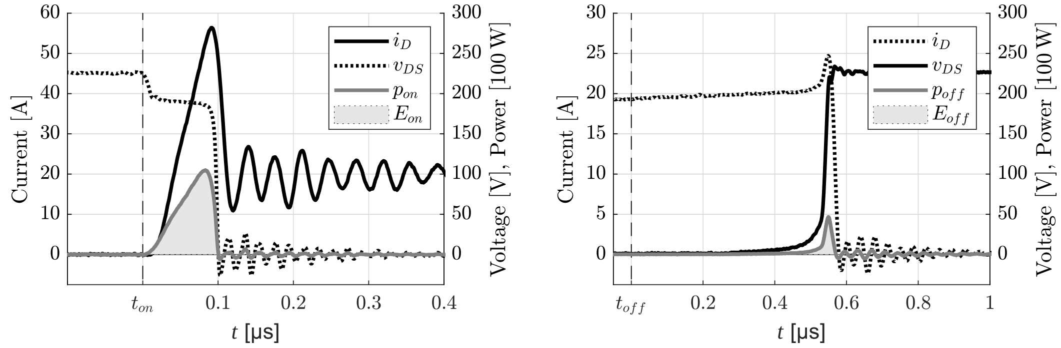
Silicon-based power devices are reaching their fundamental limit in the high voltage, low on-resistance application field, caused by the low critical breakdown field E_{crit} of the silicon. To achieve a higher voltage blocking capability, the weak doped drift region has to be increased, but the resistance increases greatly with the required breakdown voltage [74]. Significant improvements can only be achieved by using a new semiconductor material with more favourable material properties. Wide band-gap semiconductors, of which one contender is silicon carbide, have several advantages of their silicon counterpart [54]. Although more than 170 crystal structures of SiC are known, only two (4H-SiC and 6H-SiC) are commercially available [75]. 4H-SiC is preferred over 6H-SiC due to the higher electron mobility [75]. The material properties of Si and 4H-SiC, from now on, referred to as SiC, are compared in Table 7.4.

The advantages of SiC are:

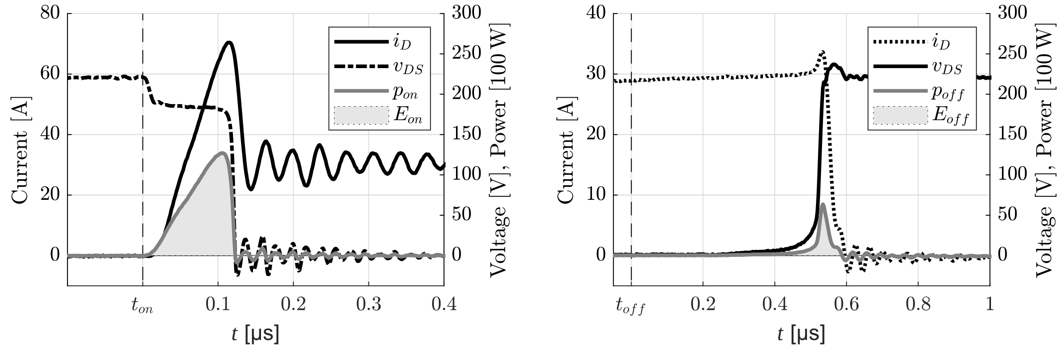
- The nearly 10 times higher electric breakdown field E_{crit} reduces the specific on-resistance significantly.
- The higher band-gap results in a much higher schottky metal-semiconductor barrier height, resulting in extremely low leakage currents at high junction temperatures [75]. Furthermore, the higher band-gap allows higher operating temperatures of the device.



(a) $i_L = 10\,\mathrm{A}$, $E_{on} = 275\,\mathrm{\mu W\,s}$ (b) $i_L = 10\,\mathrm{A}$, $E_{off} = 75\,\mathrm{\mu W\,s}$



(c) $i_L = 20\,\mathrm{A}$, $E_{on} = 539\,\mathrm{\mu W\,s}$ (d) $i_L = 20\,\mathrm{A}$, $E_{off} = 144\,\mathrm{\mu W\,s}$



(e) $i_L = 30\,\mathrm{A}$, $E_{on} = 814\,\mathrm{\mu W\,s}$ (f) $i_L = 30\,\mathrm{A}$, $E_{off} = 276\,\mathrm{\mu W\,s}$

Fig. 7.12.: Hard turn-on (a, c,e) and turn-off (b, d,f) switching transition of a silicon MOSFET IPW65R041CFD with a drain-source voltage iof $v_{DS} = 230\,\mathrm{V}$, load currents of 10 A, 20 A and 30 A and a gate resistance of $R_g = 15\,\Omega$. The waveforms of drain-source voltage v_{DS}, transistor drain current i_D and the turn-on loss-energy E_{on} and the turn-off loss-energy E_{off} respectively are depicted.

Tab. 7.4.: Si and SiC materiel properties

Property	**Si**	**4H-SiC**
Band-gap Energy E_g [eV]	1.12	3.26
Electron mobility μ_n [$\mathrm{cm^2/(V\,s)}$]	1400	800
Hole mobility μ_p [$\mathrm{cm^2/(V\,s)}$]	450	140
Intrinsic carrier concentration n_i [$10^{10}\,\mathrm{cm^{-3}}$]	1.5	5
Electron saturated velocity, v_{nsat} [$10^{7}\,\mathrm{cm^{-3}}$]	1.0	2.0
Critical electric breakdown field E_{crit} [$\mathrm{MV\,cm^{-1}}$]	0.25	2.2
Thermal conductivity Θ [$\mathrm{W/(cm\,K)}$]	1.5	3.0 - 3.8

- The higher thermal conductivity reduces the thermal resistance of the die, resulting in higher temperature operation and improved thermal management.
- the forward and reverse characteristic is barely temperature dependant, resulting in a more stable on-resistance with a positive temperature coefficient.
- the high electron saturated drift velocity v_{nsat} allows a faster movement of charge, resulting in higher possible switching frequencies.
- SiC-based semiconductor devices have an excellent reverse recovery behaviour improving the hard switching transitions. The metal-semiconductor junction capacitance, however, causes a transient negative current during the turn-off transition. [54]

In contrast to SiC diodes, it took much longer until SiC MOSFETs became commercially available in 2012 [76]. This was partially due to the insufficient performance of the SiC MOSFET and the trade-of between performance on the one side and robustness and manufacturing stability on the other hand, [76]. SiC power devices, however, bring a significant advantage in hard-switched, high voltage and fast switching power electronic converters such as solar converters, UPS, industrial drives or train propulsion, as the dynamic losses are greatly reduced [76].

In Figure 7.13 the turn-on and turn-off switching transition of the SiC MOSFET C3M0065090D at a supply voltage of $V_1 = 230\,\mathrm{V}$ and at the load currents of $i_L = 10\,\mathrm{A}$, $i_L = 20\,\mathrm{A}$ and $i_L = 30\,\mathrm{A}$ are shown. The operating points are thus identical to the measurements taken from the Si MOSFET allowing an accurate comparison. Compared to the switching transitions of a silicon based MOSFET (cf. 7.12) the turn-on and turn-off transitions of a silicon carbide MOSFET show two main enhancements:

- The switching transitions are faster
- The peak drain current overshoot is considerably lower; $\Delta i_{D,max,SiC}(i_L = 30\,\mathrm{A}) = 6\,\mathrm{A}$, whereas the same inductor current results in $\Delta i_{D,max,Si}(i_L = 30\,\mathrm{A}) = 40\,\mathrm{A}$.

The faster switching transitions are facilitated by a lower gate charge Q_g and output charge Q_{oss} of the SiC MOSFET. The decreased reverse recovery charge Q_{rr} reduces the reverse recovery current, which is needed to move these charges. This switching behaviour ultimately results in a great decrease of switching losses, listed in Table 7.5. Especially the turn-on transition shows a decreased loss dissipation of up to 80 % at an inductor current of $i_L = 30\,\mathrm{A}$.

Tab. 7.5.: Comparison of switching losses

	Turn-on loss energy E_{on}			**Turn-off loss energy E_{off}**		
i_L	10 A	20 A	30 A	10 A	20 A	30 A
Silicon	275 µW s	539 µW s	814 µW s	75 µW s	144 µW s	276 µW s
Silicon Carbide	38 µW s	83 µW s	156 µW s	38 µW s	125 µW s	257 µW s

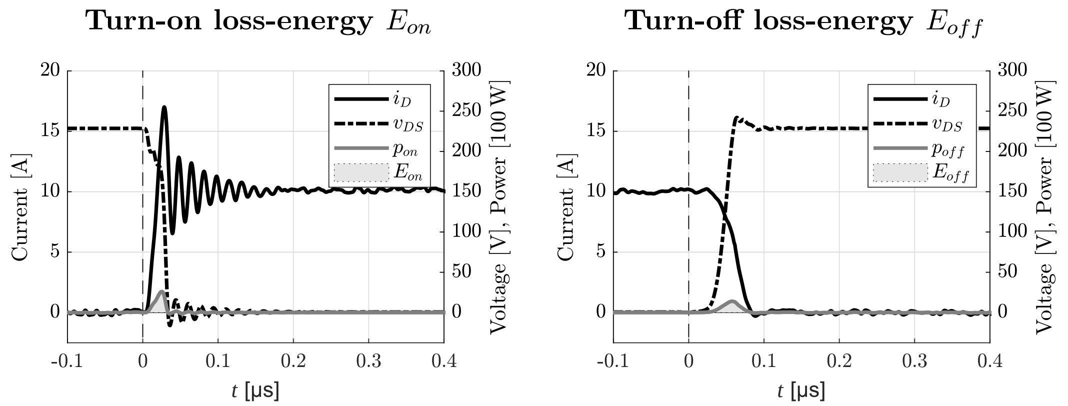
The lower switching losses and the faster switching times allow SiC semiconductor devices to be operated at increased switching frequencies. The dead-time can be decreased to below 200 ns, whereas the silicon-based MOSFET a dead-time of 600 ns requires. This reduces the switching delays and results in a more responsive circuit. This results in an enhanced transient response (more stable control loop), especially at high switching frequencies.

Gate Resistance

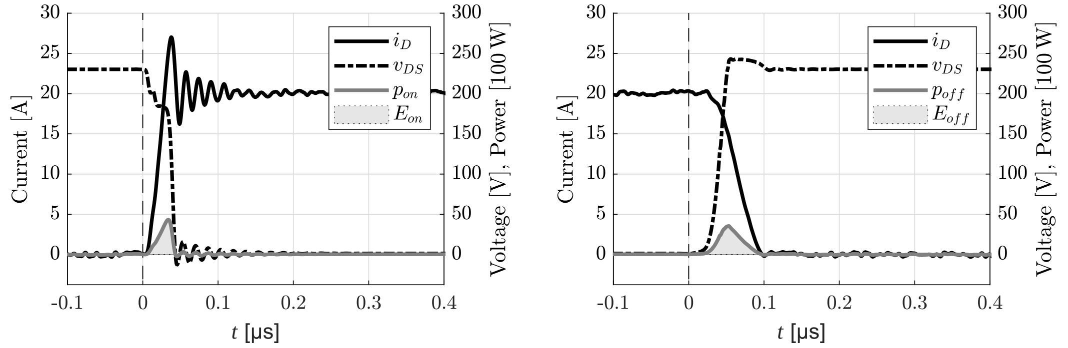
Figure 7.14 shows the effect of the size of the gate resistance on the turn-on switching transition of a silicon (a, c, e) and silicon carbide (b, d, f) MOSFET with a drain current of $I_D = 30\,\mathrm{A}$, a drain-source voltage of $V_{DS} = 230\,\mathrm{V}$ and with the gate resistances of $R_g = 15\,\Omega$ (a, b), $R_g = 47\,\Omega$ (c, d) and $R_g = 100\,\Omega$ (e, f). The resulting turn-on loss energies are listed in Table 7.6.

As described in Chapter 3, the speed of the switching transition is influenced by how fast the gate-charges of the MOSFET are moved. This is solely a function of the magnitude of the gate current. With an increase of the gate resistance, the gate current is decreased, resulting in a slower movement of charge. This lowers the current rise di/dt, which results in a decreased maximum overshoot of the drain current. As the current overshoot is mainly caused by the reverse recovery charge of the previously conducting diode and the reserve recovery charge does not change, the switching transition time has to increase. This is clearly visible in Figure 7.14. Due to the prolonged switching transition, the duration where the drain-source voltage and the drain current overlap increases. This results in an increase in the turn-on loss energy E_{on}. It can, therefore, be concluded that a higher value of the gate resistance

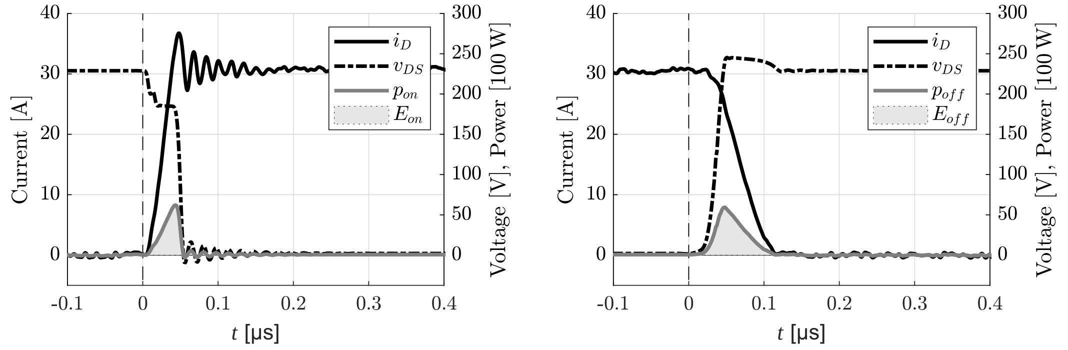
- decreases the overshoot of the drain current of the switched device, but



(a) $i_T = 10\,\mathrm{A}$, $E_{on} = 38\,\mathrm{\mu W\,s}$ (b) $i_T = 10\,\mathrm{A}$, $E_{off} = 38\,\mathrm{\mu W\,s}$



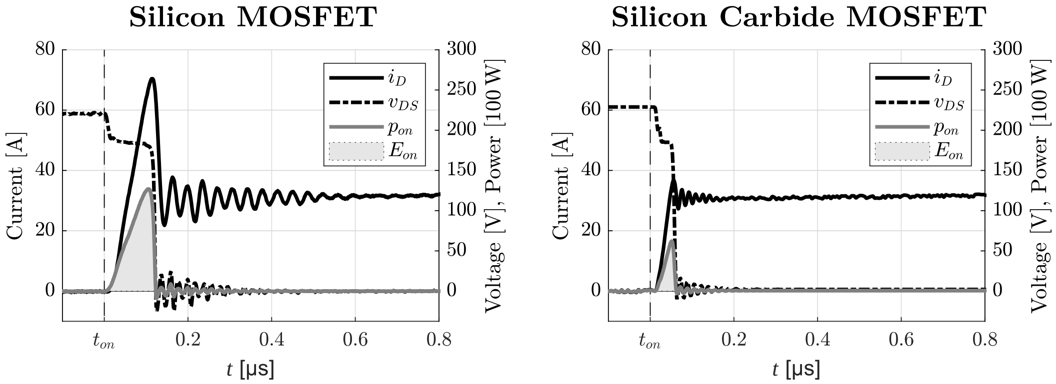
(c) $i_T = 20\,\mathrm{A}$, $E_{on} = 83\,\mathrm{\mu W\,s}$ (d) $i_T = 20\,\mathrm{A}$, $E_{off} = 125\,\mathrm{\mu W\,s}$



(e) $i_T = 30\,\mathrm{A}$, $E_{on} = 156\,\mathrm{\mu W\,s}$ (f) $i_T = 30\,\mathrm{A}$, $E_{off} = 257\,\mathrm{\mu W\,s}$

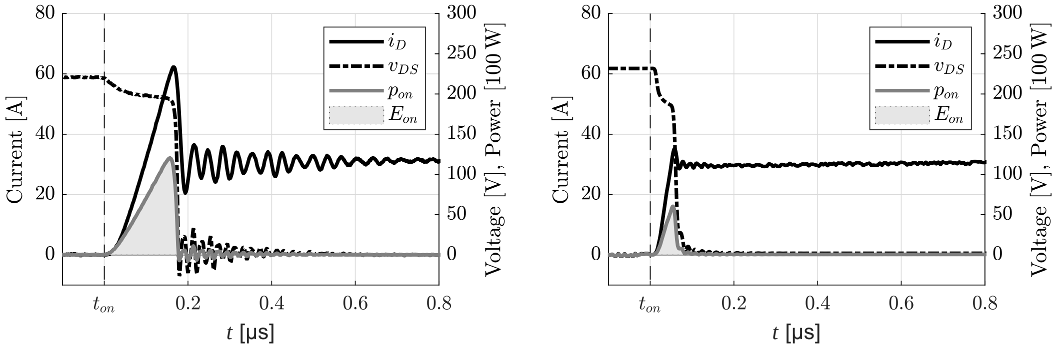
Fig. 7.13.: Hard turn-on (a, c,e) and turn-off (b, d,f) switching transition of a silicon carbide MOSFET C3M0065090D with the inductor currents of 10 A, 20 A and 30 A and a gate resistance of $R_g = 15\,\Omega$. The waveforms of drain-source voltage v_{DS}, transistor drain current i_T and the turn-on loss-energy E_{on} and the turn-off loss-energy E_{off} respectively are depicted.

- increases total switching losses of the same device.

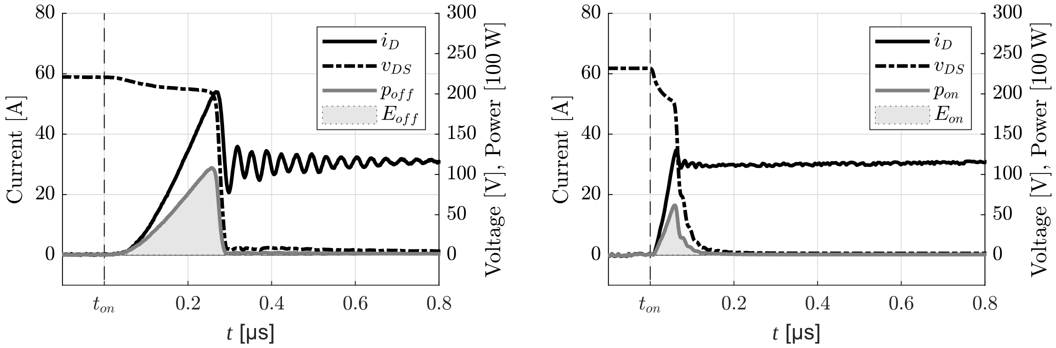

Silicon MOSFET

Silicon Carbide MOSFET

(a) $R_g = 15\,\Omega$, $E_{on} = 814\,\mu\mathrm{W\,s}$ (b) $R_g = 15\,\Omega$, $E_{on} = 156\,\mu\mathrm{W\,s}$



(c) $47\,\Omega$, $E_{on} = 1015\,\mu\mathrm{W\,s}$ (d) $R_g = 47\,\Omega$, $E_{on} = 177\,\mu\mathrm{W\,s}$



(e) $R_g = 100\,\Omega$, $E_{on} = 1255\,\mu\mathrm{W\,s}$ (f) $R_g = 100\,\Omega$, $E_{on} = 256\,\mu\mathrm{W\,s}$

Fig. 7.14.: Turn-on switching transition of a silicon MOSFET IPW65R041CFD (a, c, e) and a silicon carbide MOSFET C3M0065090J (b, d, f) with an inductor current of 30 A and with gate resistances of $R_g = 15\,\Omega$ (a, b), $R_g = 47\,\Omega$ (c, d) and $R_g = 100\,\Omega$ (e, f). The waveforms of drain-source voltage v_{DS}, transistor drain current i_D and the turn-on loss-energy E_{on} are depicted.

Tab. 7.6.: Comparison of turn-on switching losses in relation to the gate resistance R_g

	Turn-on loss energy E_{on}		
R_g	$15\,\Omega$	$47\,\Omega$	$100\,\Omega$
Silicon	$814\,\mu\mathrm{W\,s}$	$1015\,\mu\mathrm{W\,s}$	$1225\,\mu\mathrm{W\,s}$
Silicon Carbide	$156\,\mu\mathrm{W\,s}$	$177\,\mu\mathrm{W\,s}$	$256\,\mu\mathrm{W\,s}$

Efficiency

Figure 7.15 shows the converter efficiencies of a DAB converter with an input and output voltage of $V_1 = V_2 = 230\,\mathrm{V}$ and with the two discussed MOSFET technologies. Three prominent differences in the efficiency curve of the SiC MOSFET can be observed when compared to a Si MOSFET.

- Firstly, the efficiency of the DAB converter is boosted in the low power region.
- Secondly, the slope, at which the efficiency decreases (with an increase in power) is greater.
- Thirdly, the efficiency rolls off at an earlier power level.

The differences can be explained as follows: In the low power region the inductor current at the switching times t_0 and t_1 is lower than the required minimum commutation current necessary to ensure full ZVS, which results in a full or partial overlap of drain current and drain-source voltage. Hence, resulting in a hard switching transition. Therefore, due to the greatly reduced switching losses of a SiC MOSFET the efficiency is boosted in the low power region.

In the medium and high power region full ZVS is ensured reducing the switching losses significantly. Therefore the overall losses dissipated in the MOSFETs are dominated by the conduction losses of the channel. With the on-resistance of the SiC MOSFET being greater than the of a Si MOSFET ($R_{DS,on(SiC)} = 65\,\mathrm{m}\Omega > R_{DS,on(Si)} = 41\,\mathrm{m}\Omega$), the decrease of efficiency is greater of the DAB converter with SiC MOSFETs.

As the overall losses are dominated by the conduction losses, and these are defined by $P_{cond} = R_{DS,on}\, I_{RMS}^2$ the conduction losses do not increase linearly with increased power. This explains the roll-off of efficiency at high power levels. Furthermore, as the on-resistance of a MOSFET is temperature dependant and increases with temperature, the efficiency roll-off is intensified.

It can be concluded, that the usage of silicon carbide MOSFETs does not bring any added value in soft switched resonant topologies. The only enhancement can be observed in the low power region, where the efficiency is boosted. In the medium to high power regions, the semiconductor losses are dominated by the conduction losses, and therefore the strengths of a SiC MOSFET (high switching frequency and low switching losses) cannot be utilised.

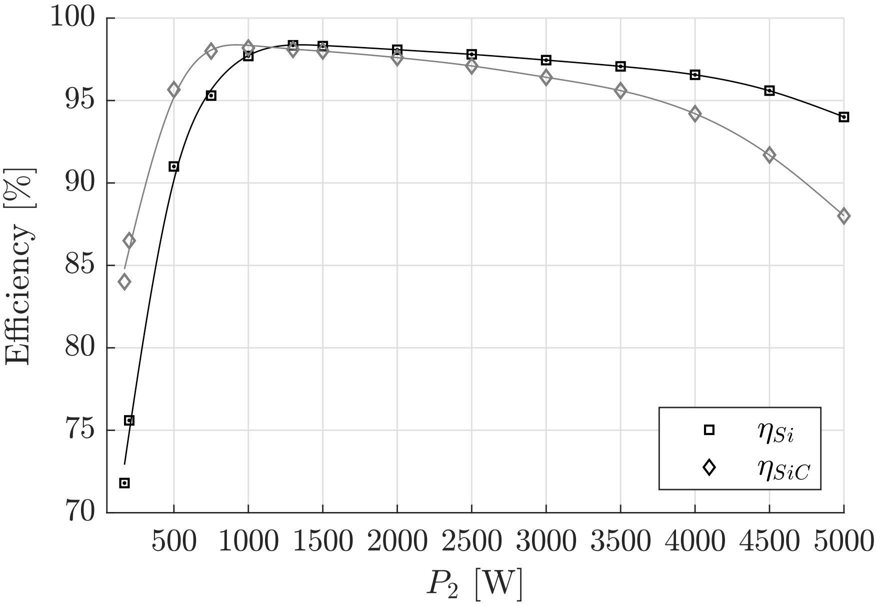


Fig. 7.15.: Measured efficiency of a DC-DC DAB converter in relation to the transferred output power P_2 with an input voltage of $V_1 = 230\,\text{V}$ and output voltage of $V_2 = 230\,\text{V}$. The efficiency curves of Si MOSFETs (IPW65R041CFD) and of SiC MOSFETs (C3M0065090D) are shown.

7.3. AC-AC DAB Converter

In this Section, the prototype operation of an AC-AC DAB converter is detailed. Firstly the measured results of the active power operation and thereafter, the reactive power operation are presented.

7.3.1. Active Power Operation

For the proof of concept of the proposed converter operated as an AC-AC converter, the active power operation with a pure resistive load of $R_L = 24\,\Omega$ is chosen. As the converter is meant to replace an isolation transformer with a voltage ratio $d = 1$ the output voltage is controlled to $V_2 = 230\,\mathrm{V}$. The input voltage range of the AC-AC converter is defined to $V_1 = 230\,\mathrm{V} \pm 10\,\%$.

Figure 7.16 depicts the voltage, current and power waveforms of the input and output with an input voltage of $V_1 = 230\,\mathrm{V}$. The converter is directly connected to the grid, and the grid voltage is thus equal to the input voltage $v_1(\omega t)$ depicted. The output voltage $v_2(\omega t)$ is sinusoidal, and when compared to the input voltage, the trapezoidal form is eliminated. As the connected load is purely resistive, the output current has no phase-shift and follows the shape of the output voltage. This results in only active output power $p_2(\omega t)$ being transferred. The input current $i_1(\omega t)$ though shows a slightly distorted waveform caused by the regulation of the output voltage. The AC-AC DAB converter does not store any energy along the power path. As the input voltage is fixed by the grid voltage and cannot be changed, the only unit that can change is the input current, when the output voltage varies from the input voltage. The distortion of the input current around the zero-crossing of the voltage is caused by the capacitors of the input and output EMI filters, that generate a small amount of reactive power.

As described before one of the advantages of an AC-AC DAB converter over a conventional transformer is the ability to regulate the output voltage. Figures 7.17 and 7.18 show the regulation of the output voltage to $V_2 = 230\,\mathrm{V}$, where the input voltage is decreased to $V_1 = 207\,\mathrm{V}$ and increased to $V_1 = 248\,\mathrm{V}$ respectively. It it apparent that the output waveforms remain stable with the change of input voltage.

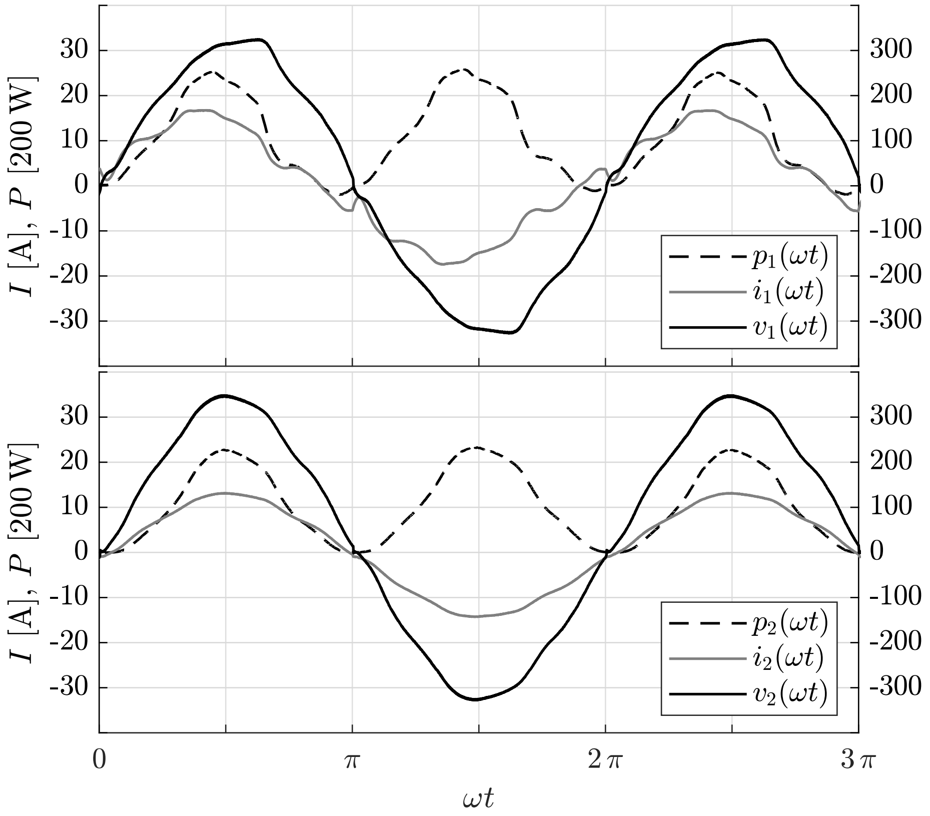


Fig. 7.16.: Measured input and output current and voltage waveforms of an AC-AC with an output power of $P_2 = 2150\,\mathrm{W}$ and an output RMS voltage of $V_2 = 230\,\mathrm{V}$ and an input RMS voltage $V_1 = 230\,\mathrm{V}$.

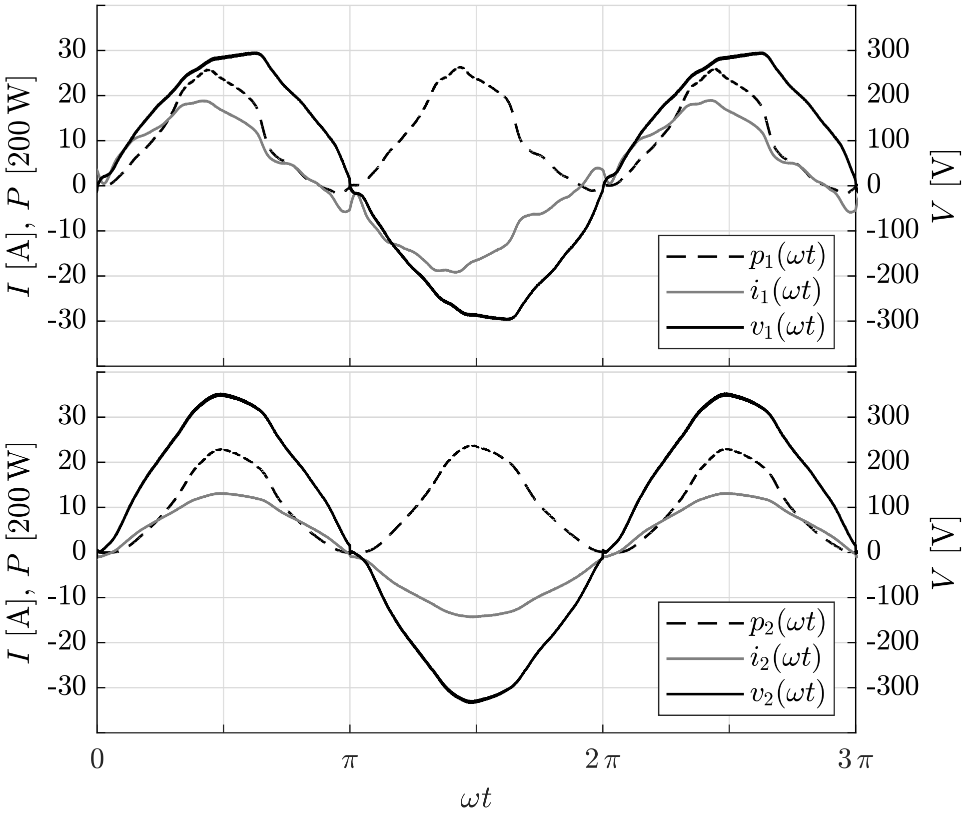


Fig. 7.17.: Measured input and output current and voltage waveforms of an AC-AC with an output power of $P_2 = 2150\,\mathrm{W}$ and an output RMS voltage of $V_2 = 230\,\mathrm{V}$ and an input RMS voltage $V_1 = 207\,\mathrm{V}$.

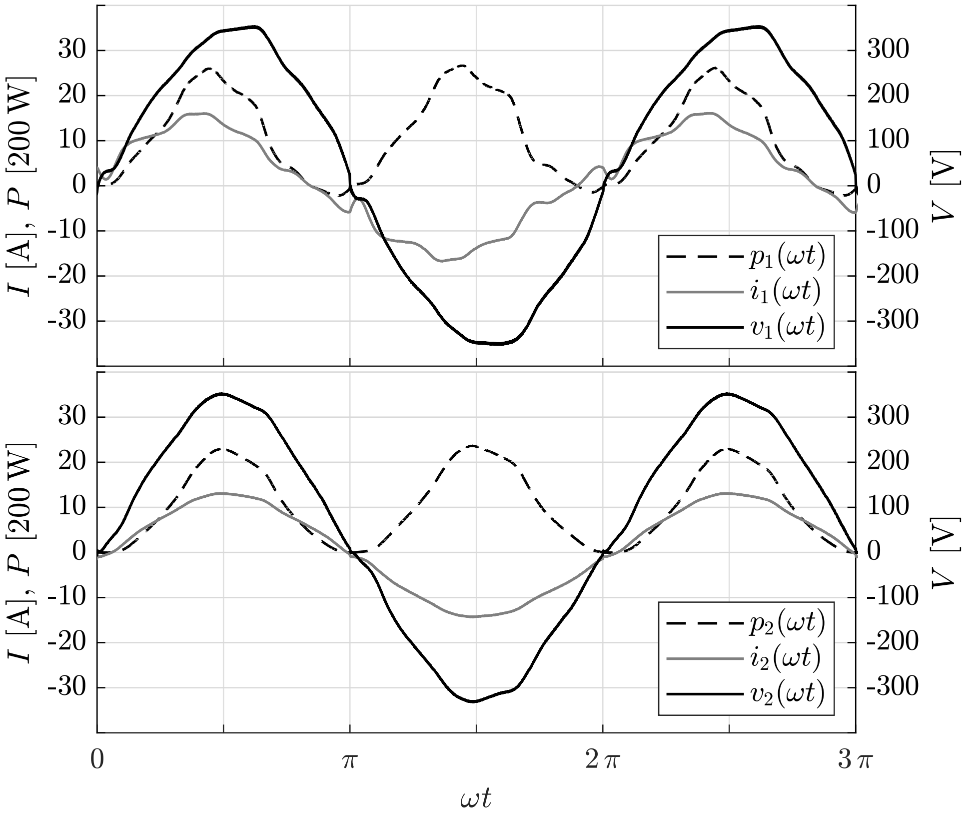


Fig. 7.18.: Measured input and output current and voltage waveforms of an AC-AC with an output power of $P_2 = 2150\,\mathrm{W}$ and an output RMS voltage of $V_2 = 230\,\mathrm{V}$ and an input RMS voltage $V_1 = 248\,\mathrm{V}$.

Efficiency

The measured efficiency of a AC-AC DAB converter with $V_1 = V_2 = 230\,\mathrm{V}$ is shown in Figure 7.19. Furthermore, the efficiency of a DC-DC DAB converter is plotted for comparison purposes.

As described in Section 7.2.1, the losses of the low power region are dominated by the switching losses and with increasing power ZVS is fully ensured. Thus the overall semiconductor losses are mainly caused by the on-resistance of the MOSFETs. The AC-AC converter has anti-series connected MOSFET switches to form bi-directional switches. Only one MOSFET is pulsed, whereas the other is turned-on during one sinusoidal half-wave. Therefore the switching losses do not increase with the bi-directional switches but the resistance doubles $R_{on,Tx} = R_{DS,on,Txp} + R_{DS,on,Txn} = 2\,R_{DS,on}$ (cf. Figure 4.1), where $x \in [0, 8]$ to the eight semiconductor switches of the two full-bridge circuits refers. The efficiency of an AC-AC DAB converter does not differ from the DC-DC converter in the low power region as the switching losses dominate this region. From of $P_2 = 1000\,\mathrm{W}$ the switching losses decrease rapidly until full ZVS is ensured at around$P_2 = 1300\,\mathrm{W}$. As the switching losses become less decisive and the losses are mainly caused by the conduction losses, the efficiency of the AC-AC converter starts to fall below the DC-DC converter's efficiency. The slope at which the efficiency decreases with power is greater, and at high power, the roll-off in efficiency increases. Again, this is caused by the higher resistance in the power path, which is also described in Section 7.2.1.

The impact of a different input voltage on the converter efficiency is shown in Figure 7.20, where the efficiency of and input voltage of $V_1 = 207\,\mathrm{V}$ is compared to the efficiency of an input voltage of $V_1 = 230\,\mathrm{V}$, both with an output voltage of $V_2 = 230\,\mathrm{V}$. It can be observed that at low lower the efficiency is slightly lower when the voltage ratio $d \neq 1$, as the ZVS constraints are violated of one full-bridge. From of $P_2 > 1300\,\mathrm{W}$ when full ZVS is warranted the efficiencies are approximately equal. At high power higher RMS currents are generated by the uneven magnitudes of the bridge voltages v_{ac1} and v_{ac2} when $d \neq 1$. This results in higher conduction losses which causes a decreased efficiency as depicted in Figure 7.20.

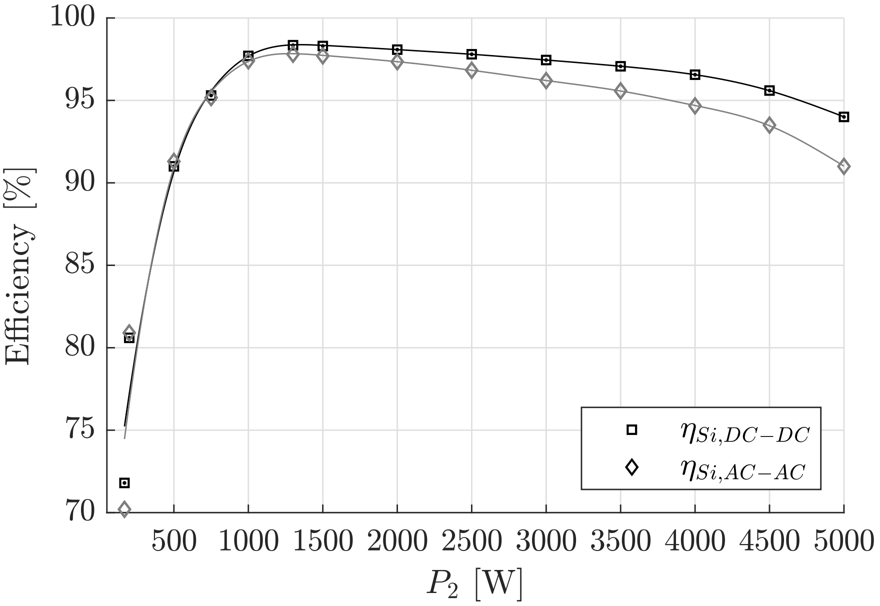


Fig. 7.19.: Measured efficiency of a AC-AC DAB converter in relation to the transferred output power P_2 with an input voltage of $V_1 = 230\,\mathrm{V}$ and output of $V_2 = 230\,\mathrm{V}$. The efficiency of a DC-DC DAB converter is shown for comparison purposes. The maximum achievable efficiency is $\eta_{si,AC-AC,max} = 97.8\,\%$ at $P_2 = 1300\,\mathrm{W}$

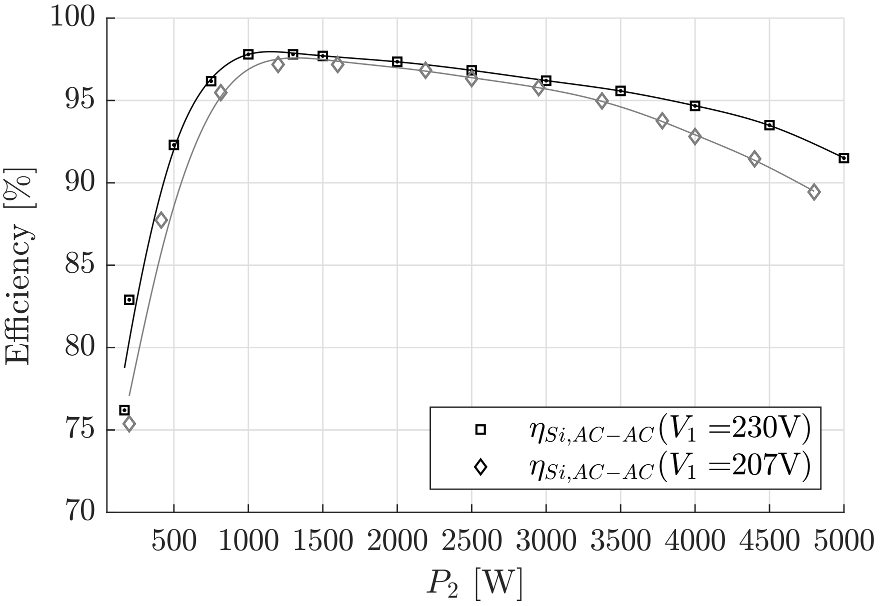


Fig. 7.20.: Measured efficiency of an AC-AC DAB converter in relation to the transferred output power P_2 with an output voltage of $V_2 = 230\,\mathrm{V}$ and the input voltage as a parameter.

7.3.2. Reactive Power Operation

Figures 7.21, 7.22 and 7.23 depict the voltage, current and power waveforms of the input and output of a AC-AC DAB converter under reactive power operation with different reactive loads connected.

The connected loads consist of a resistor R_L and inductor L_L connected in series and the resulting impedance is determined by the resistance R_L and the inductive reactance X_L and it follows:

$$\begin{aligned} Z &= R_L + jX_L \\ &= R_L + 2j\,\pi\,f_{grid}\,L_L \end{aligned} \tag{7.6}$$

The total impedance can be defined by the magnitude $|Z|$ and the angle φ_2 of the phasor sum of R and jX_L and it holds:

$$|Z| = \sqrt{R_L^2 + X_L^2} \tag{7.7}$$

and

$$\varphi_2 = tan^{-1}\left(\frac{X_L}{R_L}\right) \tag{7.8}$$

Figures 7.21 and 7.22 show the input and output waveforms with $V_1 = V_2 = 230\,\mathrm{V}$ at two different operating points with an connected impedance of $Z = 22.4\,\Omega$ and a phase-shift of $\varphi_2 = 0.245\,\pi$ (Figure 7.21) and $Z = 12.5\Omega$ and $\varphi_2 = 0.3\,\pi$ (Figure 7.22). The apparent output power results in $S_2 = 2150\,\mathrm{VA}$ and a transferred power of $P_2 = 1525\,\mathrm{W}$, and $S_2 = 3000\,\mathrm{VA}$ and $P_2 = 1720\,\mathrm{W}$ respectively.

As described in Section 5.2.2, the AC-AC DAB converter enters regions where the converter is no longer controllable, as the power needed to drive the output voltage is greater than the available instantaneous transferable power. In this regions, the control parameter g reaches maximum modulation, and the output voltage either falls to zero (before voltage zero-crossing) or rises above the sinusoidal reference value (after voltage zero-crossing). The input current is distorted, causing a third harmonic content as no energy is stored along the power path. The current spikes in the input current lead to ringing in the input voltage. The higher the phase-shift of the current φ_2 the longer the non-controllable regions become and the more distinct the distortion of the output voltage becomes.

Figure 7.23 shows the input and output waveforms with an input and output voltage of $V_1 = V_2 = 110\,\mathrm{V}$ and a phase shift of $\varphi_2 = 0.425\,\pi$. The increase in the non controllable regions and the thereby greater distortion of the waveforms are clearly visible. Furthermore an increase in power magnifies this behaviour as well, which becomes apparent by a comparison of 7.21 and 7.22.

From Figure 7.23 it becomes apparent that the reactive operating range of the AC-AC DAB converter has to be limited to ensure reliable operation of the converter. The maximum phase shift φ_2 has to be defined, which decreases as the power increases, as the uncontrollable regions increase with an increase in power. Failing to limit the operating range leads to high stress on the components, unstable operation and high EMI caused by the ringing and third harmonic content of the input current. The operating points depicted in Figures 7.21 and 7.22 lead to stable operation of the converter but nevertheless the third harmonic content in the input current is present and undesirable.

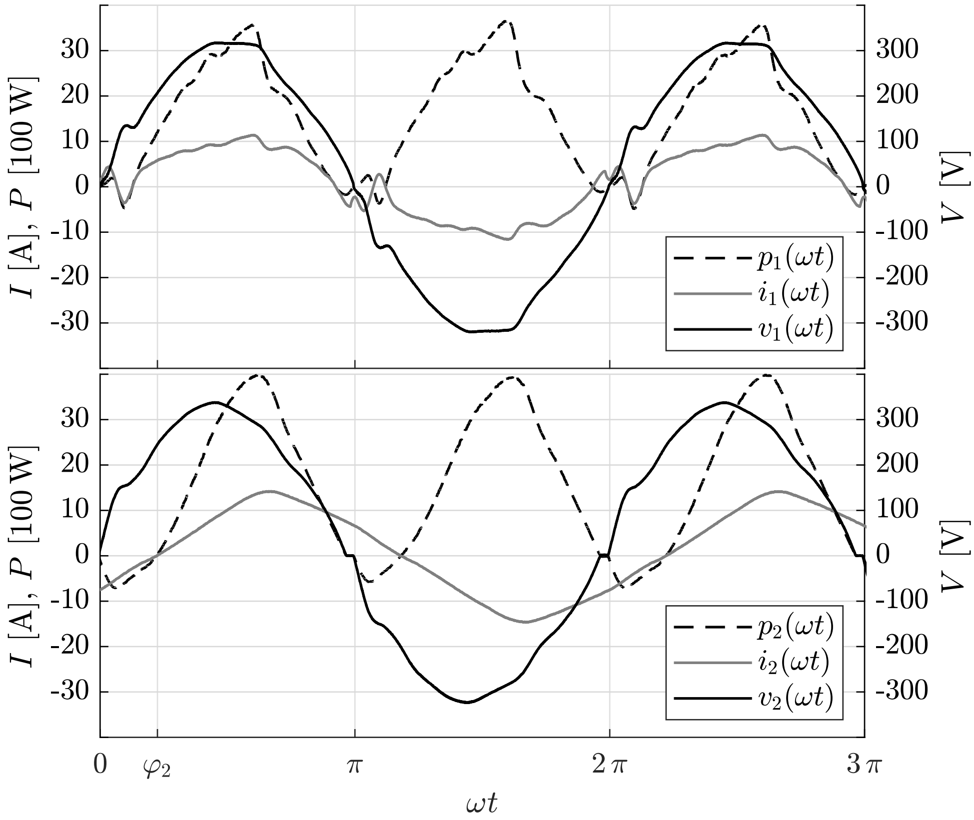


Fig. 7.21.: Measured input and output current, voltage and power waveforms of a AC-AC DAB converter with $V_1 = V_2 = 230\,\text{V}$ and an apparent output power of $S_2 = 2150\,\text{VA}$ and $\varphi_2 = 0.245\,\pi$ resulting in an active output power of $P_2 = 1565\,\text{W}$.

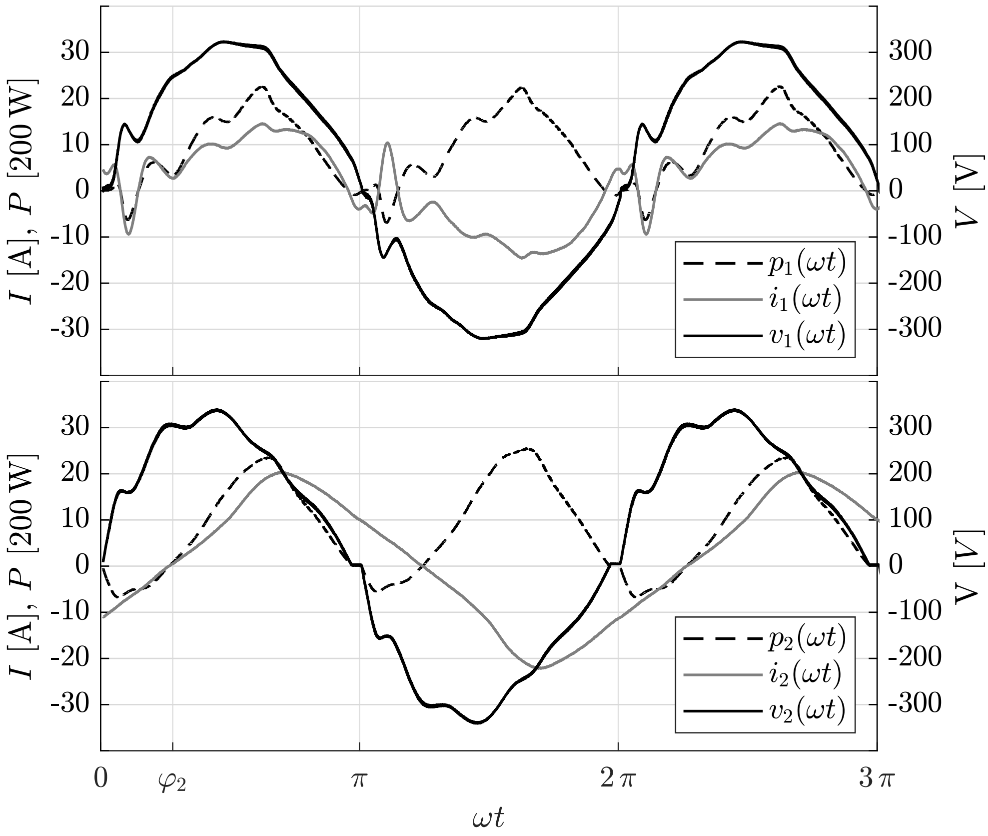


Fig. 7.22.: Measured input and output current, voltage and power waveforms of a AC-AC DAB converter with $V_1 = V_2 = 230\,\mathrm{V}$ and an apparent output power of $S_2 = 3000\,\mathrm{VA}$ and $\varphi_2 = 0.3\,\pi$ resulting in an active output power of $P_2 = 1720\,\mathrm{W}$.

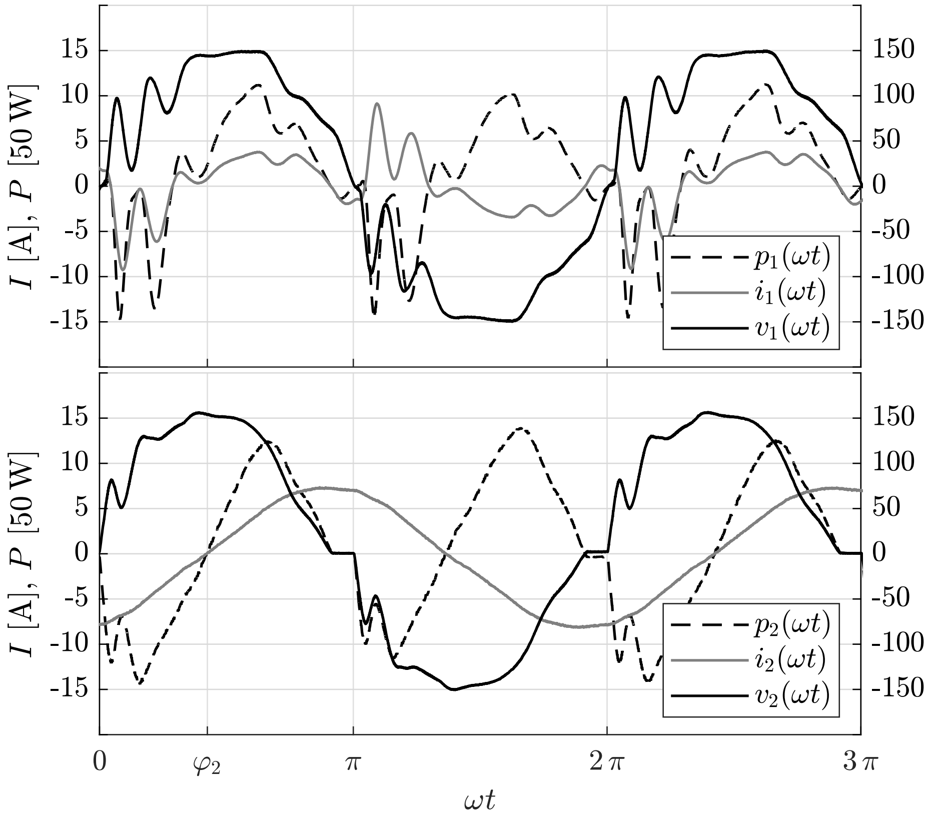


Fig. 7.23.: Measured input and output current, voltage and power waveforms of a AC-AC DAB converter with $V_1 = V_2 = 110\,\mathrm{V}$ and an apparent output power of $S_2 = 580\,\mathrm{VA}$ and $\varphi_2 = 0.425\,\pi$ resulting in an active output power of $P_2 = 48\,\mathrm{W}$. Due to the distorted waveforms the output power is lower than expected with $\varphi_2 = 0.425\,\pi$.

7.4. Conclusion

This Chapter presents the measurement results obtained from the 5 kVA prototype DAB converter. The theoretically derived modulation schemes and the technical design of the DAB converter are verified.

Firstly the DC-DC DAB converter is analysed, where in a first step the MF transformer is bypassed to form a non-isolated DAB converter. The measured inductor RMS current is compared to the calculated current, and a good match between the two values is achieved, which is shown in Table 7.1. In a second step, the measurement results of an isolated DAB converter are presented, and the influence of the MF transformer is described. The magnetising current of the transformer causes the slope of the primary and secondary inductor current to differ.

Thereafter the measured results are compared to the simulated and the calculated results in Table 7.2. The calculated values obtained with the DAB model considering conduction losses neglects the magnetizing current and therefore only one inductor current is listed. Nevertheless the model delivers acceptable RMS current results leading to a good match of the calculated to the measured values. From Figures 7.7, 7.8, 7.9 and 7.10 the resonant voltage transitions are visible.

In a second step, the transient behaviour of the prototype DAB converter is analysed, and the switching losses are presented. The loss-energy of a silicon MOSFET at different inductor currents is presented first. Thereafter silicon carbide as a semiconductor material is described, and the advantages of the new material are detailed. A silicon carbide MOSFET is introduced, and the switching behaviour is analysed. The switching loss-energy is compared to its silicon counterpart, and a significant reduction in switching losses is achieved under hard switching transitions. A comparison (cf. Figure 7.15) of the converter efficiency of a DC-DC DAB converter with silicon to silicon carbide MOSFETs shows that silicon carbide does not bring any added value to soft switched converter topologies. Although the efficiency is boosted in the lower power region, a high drop in efficiency is recorded at high power. This is due to the main contribution of the conduction losses to the overall converter losses. Hence the efficiency is mainly influenced by the on-resistance of the MOSFET.

The effect of the gate resistance is detailed, and it is shown, that a higher gate resistance decreases the current overshoot but prolongs the switching transition and thereby increases the switching losses.

In a third and last step, the prototype converter operated as an AC-AC converter is analysed, and the measurement results are presented. Firstly, the active power operation is detailed and secondly the reactive power operation is described. The active power operation shows stable input and output waveforms and the benefit of controlling the output voltage is shown. Therefore it can be concluded that the active power operation is fully guaranteed by the proposed AC-AC converter.

The drawbacks of the reactive power operation are presented and Figures 7.21, 7.22 and 7.23 clearly visualise the distorted waveforms caused by the non controllable regions of the converter. It is shown, that the higher the phase-shift φ_2 and the greater the apparent power the greater the non controllable regions become. Therefore to guarantee stable operation the phase-shift φ_2 has to be limited.

8. Conclusion and Outlook

8.1. Conclusion

In the course of this work, a smaller, lighter and resource friendlier alternative to a conventional low power low-frequency transformer is investigated. By increasing the operating frequency of the transformer, the build size can be drastically reduced. Furthermore, the introduction of power electronic switching networks enables smart features and smart protection previously not present in conventional LFTs. Three different energy conversion systems are presented, and the benefits and drawbacks of each are detailed and evaluated. The single-stage conversion system based on the DAB converter is considered to be most promising in reducing the size and weight without sacrificing the lifetime significantly. Hence a direct AC-AC DAB converter is studied in detail, and a prototype converter is developed.

In **Chapter 2**, the DAB converter is introduced, and the fundamental working principle and basic power transfer based on the lossless model is explained. The three possible modulation parameters influencing the power transfer are detailed. Firstly the conventional phase-shift modulation is analysed in detail, and the ZVS constraints are derived. It is shown that the ZVS constraints are violated with a voltage ratio $d \neq 1$ and low output power. This yields poor light-load converter efficiency. By utilising the advanced modulation schemes, which additionally exploit the modulation parameters w_1 and w_2, the inductor current can be manipulated. Thereby the inductor RMS current can be reduced, and the switching transition times of each half-bridge can be influenced to warrant ZVS. The evaluation of the advanced modulation schemes concluded that the two-sided modulation scheme (employing w_1 and w_2 simultaneously) only bears limited advantages with increased complexity. Consequently, the one-sided clamped modulation (only employing only w_1 or w_2 individually) is judged to be the most promising modulation scheme in the reduction of the inductor RMS current. The one-sided clamped modulation is studied in detail and the analytical current description is derived for Case I ($g < 0$) and Case II ($g > 0$).

A combined modulation scheme is proposed that utilises both the one-sided modulation and the conventional phase-shift modulation depending on the transferred output power. The optimal modulation parameters (g and w) are derived, and it is shown that a seamless transition from Case I over Case II of the one-sided clamped modulation to the phase-shift modulation is possible. This results in a continuity of the control parameters. The combined modulation scheme warrants ZVS over the whole operating range only with ZCS during the transition from Case I to Case II, when the lossless DAB model is considered.

Lastly, the lossless DAB model is enhanced to consider conduction losses. The analytical current description is derived, and the optimal parameters of the combined modulation scheme are updated.

The switching transient of a MOSFET is detailed in **Chapter 3**, starting with the ideal transient, over introducing the parasitic switching effects to the real switching transition. The hard and soft switching transitions are explained, and the resonant transitions of a DAB converter modulated with the phase-shift modulation and the one-sided clamped modulation are shown. Furthermore, the losses generated by each switching transition are characterised.

The proposed AC-AC DAB converter is presented in **Chapter 4**. The alternating sinusoidal voltage and current are described first, defining the phase-angles of input and output voltage and current. Due to the alternating units on the input and output, each half-bridge of the converter has to block voltage and current of both polarities. Hence the semiconductor switches are replaced by bi-directional switches to allow four-quadrant operation. After that, the principle of operation of the AC-AC DAB converter is detailed with emphasis on the modulation schemes introduced in Chapter 2. The impact on the optimal parameters of the combined modulation scheme by the added resistance of the bi-directional switches is investigated. It is shown that the total transferable power decreases and the power level at which the transition from Case I to Case II of the one-sided clamped modulation occurs changes.

As the proposed AC-AC converter is meant as a direct replacement of a conventional LFT, the real power and the reactive power operation of the converter are described in Section 4.3. It is shown that under real power operation, the voltage ratio d is constant and that the operation of the converter is thus equivalent to the DC-DC converter's. Furthermore, the calculation of the optimal modulation parameters does not increase in complexity.

The difficulty of the reactive power operation with the input and output voltages being in phase is detailed. It is shown that regions exist, where the instantaneous output power greater than the maximum instantaneous transferable power of the converter is. This leads to uncontrollable regions which cause an undesired third harmonic content in the input current. Furthermore, the control parameter shows a discontinuity and is highly non-linear. Shifting the output voltage in such way, that the input voltage and the output current are in phase results in the following; the control parameter is no longer time dependant and becomes constant over one sinusoidal period. By this, the converter becomes controllable over the whole operating range, and the third harmonic content in the input current is eliminated. Due to the time-dependent voltage ratio d the importance of the combined modulation scheme is detailed to guarantee maximum converter efficiency.

Chapter 5 presents the results obtained from a steady-state SPICE simulation. The optimal modulation parameters w (clamping interval) and g (phase-shift), extracted from a stepped SPICE simulation, show an accurate correlation with the analytically derived parameters. In Subsection 5.1.1, the real DAB model is introduced, and the influence of the previously neglected effects of the transformer and the dynamic losses of the semiconductor switches are investigated. It is shown that due to the parasitic elements of the MOSFET, the ZVS constraints are violated when the transition from the one-sided clamped modulation from $g < 0$ to $g > 0$ occurs. This is visualised by a drop of efficiency around the transition region. It is concluded that the derived optimal parameters of the combined modulation scheme are overall valid, and result in a significant efficiency enhancement of up to 50% under light-load operation.

The simulated results of the AC-AC DAB converter are introduced in Section 5.2 and the real power operation is described first. It is shown that the operation is fully guaranteed with the combined modulation scheme. After that, the reactive power operation is presented, and it is explained, that due to uncontrollable regions of the converter, a third harmonic content in the input current is present. This is caused by a distorted output voltage as the instantaneous transferable power is not sufficient in certain regions. The 5 kVA prototype converter is designed in **Chapter 6** and the design parameters are listed. The schematic hardware overview is presented, and the main components are sized. Lastly, the magnetic components are designed, and the semiconductor switches are chosen.

Chapter 7 finally presents the measurements results obtained from the 5 kVA prototype converter. The non-isolated DC-DC operation (transformer bypassed) shows a good match of the measured to the calculated inductor current. The results of the isolated DAB converter show the influence of the magnetising current of the transformer, which causes the slope of the primary and secondary inductor current to differ. These results are then compared to the calculated and simulated results. It is concluded that the DAB model considering conduction losses, delivers an acceptable approximation of the switching transition times of the semiconductors and the inductor RMS current.

After that, the transient behaviour of the prototype DAB converter is analysed, and the measured switching losses are presented. Firstly the silicon MOSFET is analysed and thereafter the silicon carbide as a semiconductor material is described and the advantages are detailed. A silicon carbide MOSFET is investigated, and the switching loss-energies under hard commutation are compared. The SiC MOSFET shows a significantly improved switching behaviour and the loss-energy is significantly reduced. The comparison of the converter efficiencies, however, shows that the benefits of the SiC MOSFET cannot be utilised by the DAB converter topology. Although the light-load operation efficiency is boosted, the efficiency drops with an increase of transferred power. This is due to the resonant nature of the DAB converter, where the converter losses are mainly contributed by the static losses, and the dynamic losses are negligible.

Section 7.3 finally presents the measurement results of the prototype converter operated as an electronic transformer. Firstly, the active power operation is detailed and secondly the reactive power operation is described. The active power operation shows stable input and output waveforms and the benefits of controlling the output voltage are shown. Therefore it can be concluded that the proposed AC-AC converter fully guarantees the active power operation. The drawbacks of the reactive power operation are presented, and the distorted waveforms caused by the non-controllable regions of the converter are depicted and described. It is shown, that the lower the power factor (the higher the phase-shift φ_2) and the greater the apparent power, the greater the non-controllable regions become. Consequently, a stable reactive power operation cannot be guaranteed over the whole operating range. To guarantee basic functionality the power factor (phase-shift φ_2) has to be limited.

8.2. Outlook and Future Research

The reactive power operation of the proposed AC-AC DAB converter, especially with high power and low power factor, bear challenges that have to be solved to guarantee the stable operation of the converter. The uncontrollable regions of the AC-AC DAB converter under reactive power operation caused by the inability to deliver sufficient energy cause distorted voltage and current waveforms. These have to be eliminated to guarantee the success of the proposed converter. This can be accomplished by shifting the output voltage in such a way that the output current and the input voltage are in phase. This results in a linear control parameter, and the non-controllable regions are omitted. Doing this the operating behaviour of the converter is similar to the operation with active power only. It has been proven that the operation with active power is fully guaranteed and high efficiencies and stable operation can be achieved.

Figure 8.1 shows the reactive power operation of the prototype AC-AC with the output voltage shifted in such way that the output current is in phase with the input voltage ($\varphi_{v1} \approx \varphi_{i2}$). It can be seen that the uncontrollable regions are removed and that the waveforms show a sinusoidal trend with no third harmonic content.

It is shown, that ZVS is warranted until low power when $d = 1$ (cf. Chapter 2) and modulated with the conventional phase-shift modulation. When $d \neq 1$ the proposed combined modulation scheme has to be implemented to minimize inductor RMS current and thereby enhance the converter efficiency. With the active power operation of the AC-AC converter the voltage ratio is constant over time ($d = const.$) as the input and output voltage are in phase ($\varphi_{v1} = \varphi_{v_2}$). When the output voltage is shifted as suggested, the voltage ratio is no longer constant, but changes with time and it holds

$$d(t) = \frac{n\, v_2(t)}{v_1(t)} \neq const \tag{8.1}$$

Therefore the optimal modulation parameters derived in Chapter 2 have to be continuously updated to ensure maximum converter efficiency.

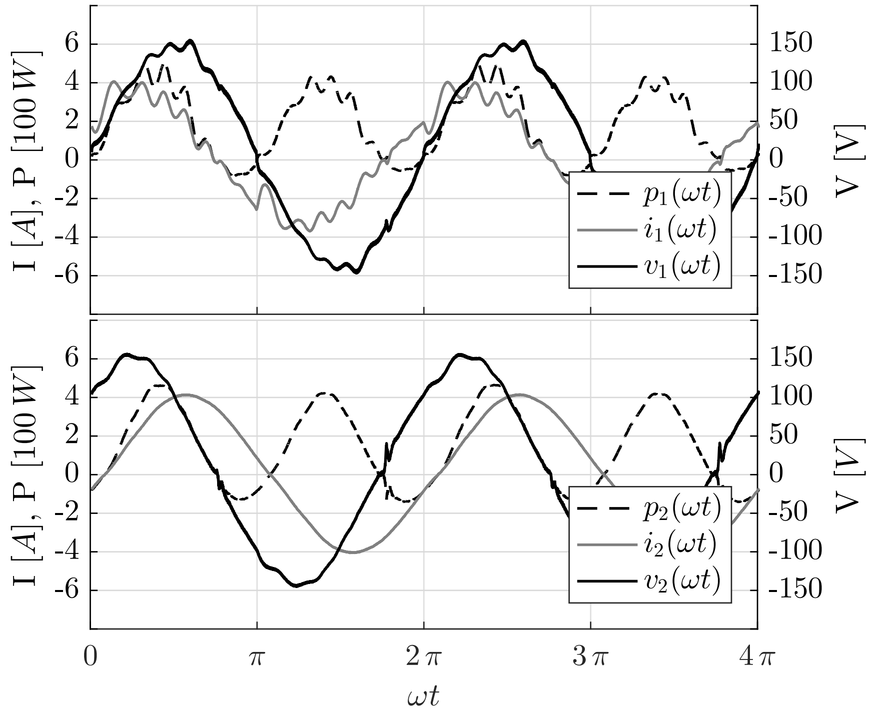


Fig. 8.1.: Measured waveforms with $V_1 = V_2 = 110\,\mathrm{V}$ and with the output voltage shifted to be in phase with the input voltage ($\varphi_{v2} = -0.3\pi$ and $\varphi_{v1} \approx \varphi_{i2}$). The apparent power equals to $S = 287\,\mathrm{VA}$ and a active power of $P = 138\,\mathrm{W}$ is transferred.

The groundwork has been done in the course of this thesis. The optimal parameters in relation to the voltage ratio d and the output power P_2 are derived, and it is shown that the combined modulation scheme boosts the efficiency up to 50% in the low power region. The active power operation is shown, and the functionality is fully granted, enabling high converter efficiencies. The uncontrollable regions can be omitted by shifting the output voltage in such a way that the output current is in phase with the input voltage. The different phase angles of the voltages result in a changing voltage ratio $d(t)$. Therefore, the optimal modulation parameters of the combined modulation scheme have to be continuously updated. The stable implementation of the control scheme with the varying modulation parameters has to be further investigated, but Figure 8.1 shows that the theoretical functionality is ensured.

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A. Alternating sinusoidal voltage and current

In direct current (DC) circuits the voltages and currents are generally constant and are not varying over time. In alternating current (AC) circuits however the instantaneous values of the voltages, currents and therefore the power are changing constantly over time.

The instantaneous power consumed by each port is given by

$$\begin{aligned} p(t) &= v(t)\, i(t) \\ &= \hat{V}\, \hat{I}\, sin(\omega\, t + \varphi_v)\, sin(\omega\, t + \varphi_i) \\ &= \frac{\hat{V}\, \hat{I}}{2}\, [cos(\varphi_v - \varphi_i) - cos(2\,\omega t + \varphi_v + \varphi_i)] \\ &= V_{RMS}\, I_{RMS}\, [cos(\varphi_v - \varphi_i) - cos(2\,\omega t + \varphi_v + \varphi_i)] \end{aligned} \tag{A.1}$$

with

$$\frac{\hat{V}\, \hat{I}}{2} = \frac{\hat{V}}{\sqrt{2}}\, \frac{\hat{I}}{\sqrt{2}} = V_{RMS}\, I_{RMS} \tag{A.2}$$

and the trigonometry identity:

$$2\, sin(\alpha)\, sin(\beta) = cos(\alpha - \beta) - cos(\alpha + \beta) \tag{A.3}$$

The term $cos(2\,\omega t + \varphi_v + \varphi_i)$ in Equation (A.1) can be rewritten in the form

$$\begin{aligned} cos(2\,\omega t + \varphi_v + \varphi_i) &= cos(2\,(\omega t + \varphi_v + \varphi_i) - (\varphi_v - \varphi_i)) \\ &= cos\, 2(\omega t + \varphi_v)\, cos(\varphi_v - \varphi_i) + sin\, 2(\omega t + \varphi_v)\, sin(\varphi_v - \varphi_i) \end{aligned} \tag{A.4}$$

and the instantaneous power $p(t)$ results in:

$$p(t) = V_{RMS}\, I_{RMS}\, [(1 + cos\, 2(\omega t + \varphi_v))\, cos(\varphi_v - \varphi_i) + sin\, 2(\omega t + \varphi_v)\, sin(\varphi_v - \varphi_i)] \tag{A.5}$$

It is apparent that the term $(1 + cos\, 2(\omega t + \varphi_v))$ an average value of 1 has, whereas the term $(sin\, 2(\omega t + \varphi_v))$ to a value of zero averages. The power that is consumed by each port of the two-port network is defined as active power P. The part of the instantaneous power that has an average value of zero is defined as reactive power Q and it holds:

$$P = \overline{p(t)} = V_{RMS}\, I_{RMS}\, cos(\varphi_v - \varphi_i) \tag{A.6a}$$

$$Q = V_{RMS}\, I_{RMS}\, sin(\varphi_v - \varphi_i) \tag{A.6b}$$

B. Double Pulse Test

The schematic of the experimental half-bridge set-up is depicted in Figure B.1. The generated waveforms by gating the device under test (DUT, T_3 in Figure B.1) with a double pulse are shown in Figure B.2. The double pulse test is characterized by the three shown time intervals denoted I to III:

- During time interval I ($t_0 \leq t < t_1$) MOSFET T_3 is turned on to generate the desired load current i_L.
- At t_1 MOSFET T_3 is turned OFF and the load current i_L free-wheels through the body diode of the complementary MOSFET T_1. The drain-source voltage $v_{DS,T3}$ and drain current $i_{D,T3}$ of the DUT (T_3) are recorded to compute the losses generated by the turn-off switching transition. During the time interval II ($t_1 \leq t < t_2$) the laod current is considered to be constant as $(t_2 - t_1) << (t_1 - t_0)$and therefore $i_L(t_1) = i_L(t_2)$.
- At t_2 MOSFET T_3 is turned ON and the current commutates off the conduction diode resulting in a hard switching transition. The drain-source voltage $v_{DS,T3}$ and drain current $i_{D,T3}$ of the DUT (T_3) are recorded to compute the losses generated by the hard turn-on switching transition. During III ($t_2 \leq t < t_3$) the load current rises again.
- At t_3 MOSFET T_3 is turned OFF and the double pulse test is concluded. The load current free-wheels though the body-diode of T_1 and decreases to zero.

The drain current $i_{D,T3}$ is measured with a wide bandwidth coaxial shunt (SDN-414-025 [73]) and the drain-source voltage $v_{DS,T3}$ with a 100:1 probe and the Tektronix MSO4054B 350 MHz model.

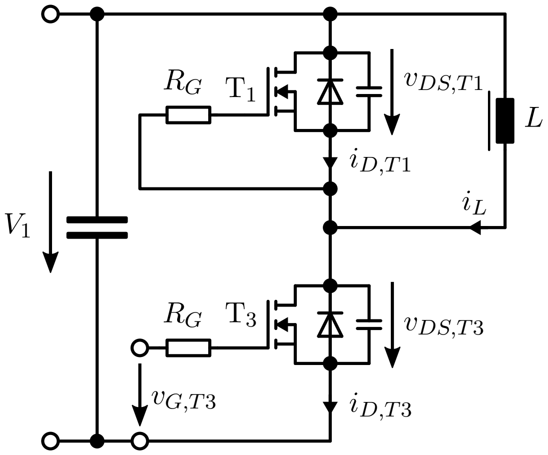

Fig. B.1.: Measuring set-up to determine switching losses

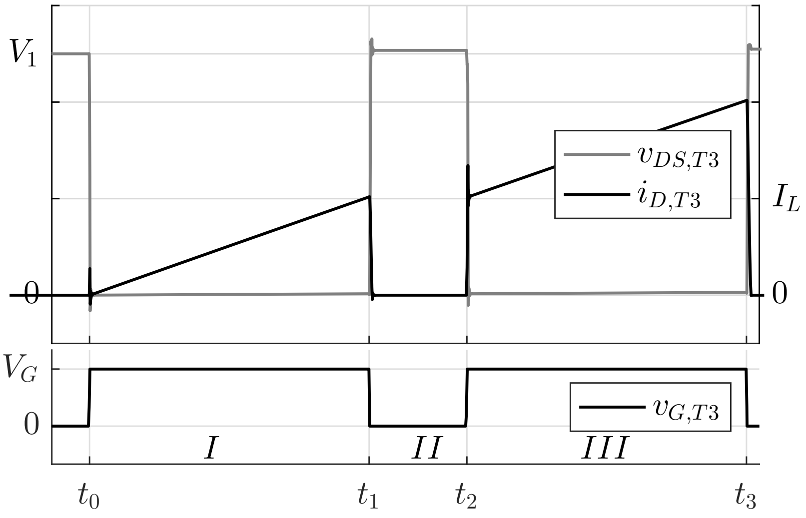

Fig. B.2.: Generated waveforms of the double pulse test to measure the drain-source voltage $v_{DS,T3}$ and drain current $i_{D,T3}$ of the DUT (T_3) to calculate the switching losses

C. Measurement of Magnetic Components

The bode plots gained from the frequency sweep measurement of the transformer (Figures C.1, C.2 and C.3) and the coupling inductor (Figures C.4 and C.5) are depicted below. The winding resistance (cf. Figure C.1 and C.4), the magnetizing inductance of the transformer (cf. Figure C.2), the inductance of the coupling inductor (cf. Figure C.2) and the stray inductance of the transformer (cf. Figure C.3) can be extracted.

C.1. Transformer

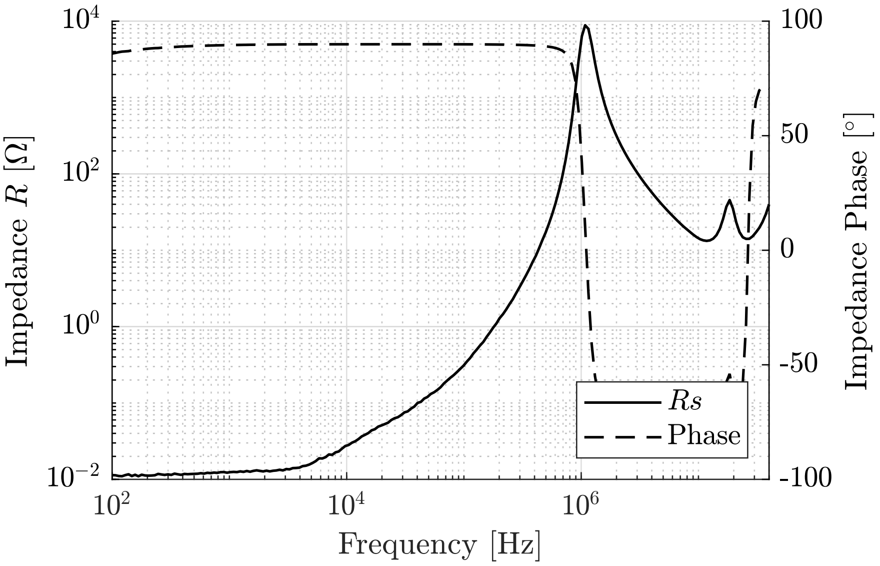

Fig. C.1.: Measured bode plot of transformer with secondary side open showing the winding resistance

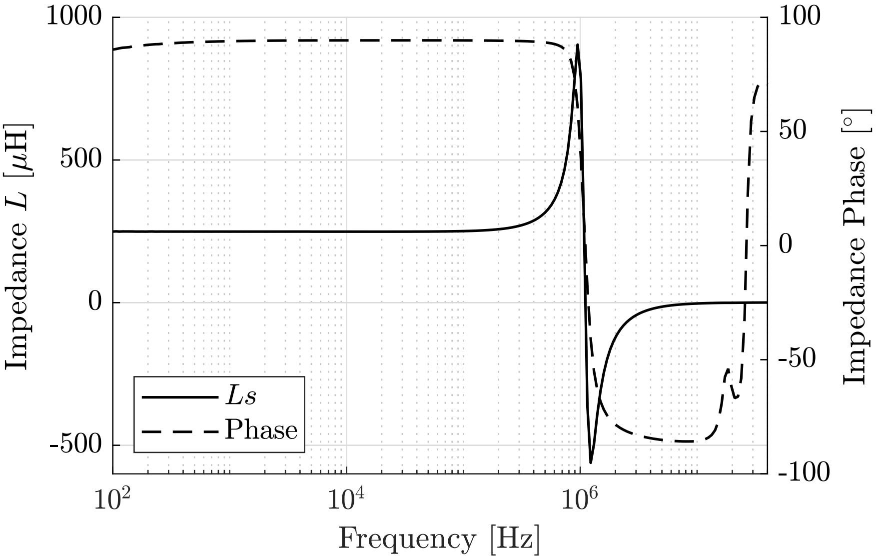

Fig. C.2.: Measured bode plot of transformer with secondary side open showing the inductance

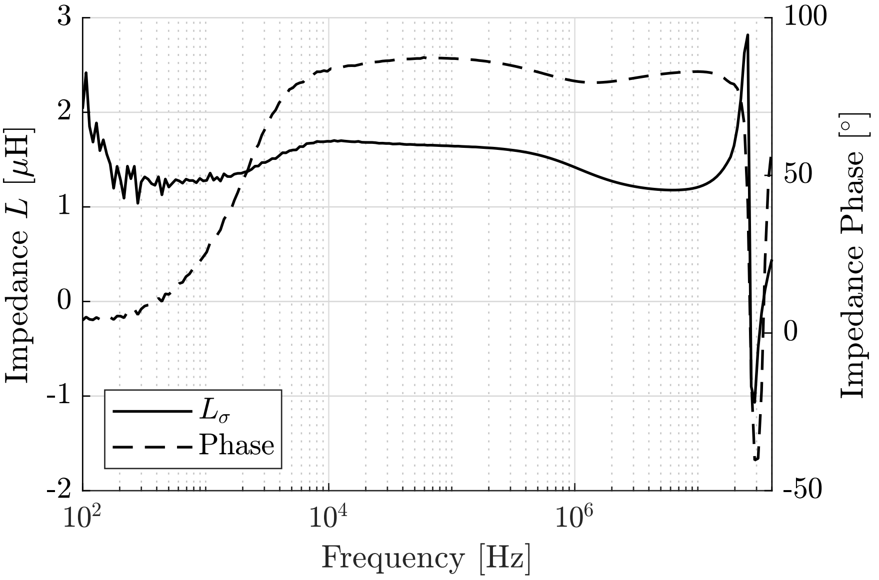

Fig. C.3.: Measured bode plot of transformer with secondary side shortened showing the stray inductance

C.2. Coupling Inductor

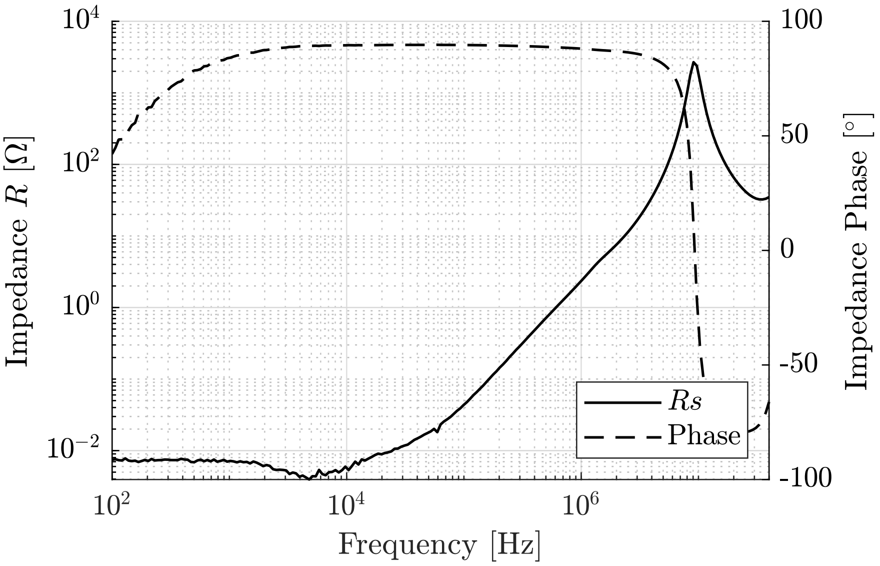

Fig. C.4.: Measured bode plot of the coupling inductor showing the winding resistance

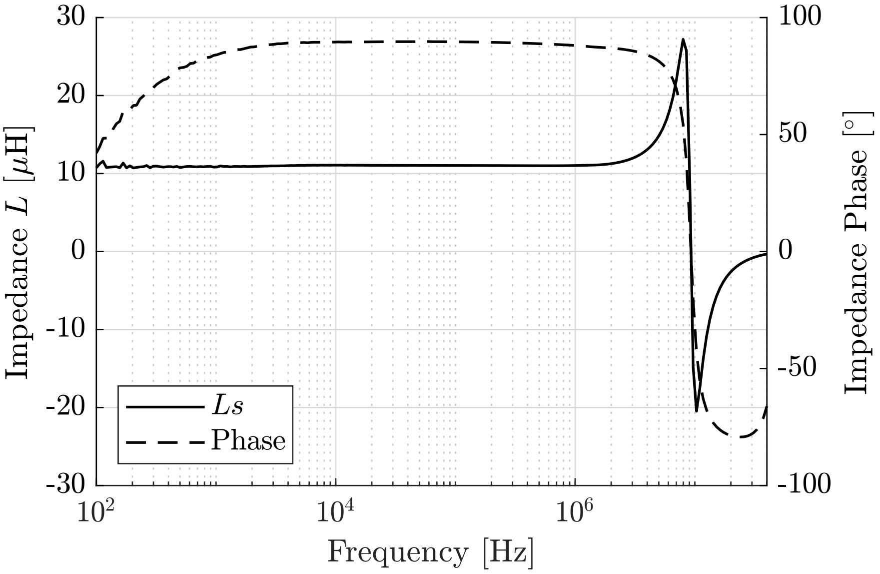

Fig. C.5.: Measured bode plot of the coupling inductor showing the inductance

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