Fakultät für Elektrotechnik und Informationstechnik
der Technischen Universität München

Behaviour of 4H-SiC Power Semiconductor Devices under Extreme Operating Conditions

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Abstract

Silicon Carbide (SiC) as material for power semiconductors allows applications at high temperatures, but the theoretical modeling of physical mechanisms inside the devices necessary to perform predictive TCAD-simulations relies mostly on Si-models, today. Therefore, 4H-SiC JBS-diodes and 4H-SiC PiN-diodes are investigated under extreme conditions in this PhD-thesis.
A high temperature measurement setup (300 K to 800 K) was implemented into a vacuum chamber and four different measurement configurations were established. The corresponding virtual experiments were implemented in the TCAD-simulator Sentaurus Device.
The measurements on JBS-diodes demonstrated the transition from unipolar to bipolar conduction in forward direction at high temperatures for low and high electric powers. The comparisons between diodes of two wafers evinced, that higher blocking capabilities causes higher knee-voltages in forward direction. A smaller gap between p-islands leads to a bipolar activation at lower electric powers but also, to an enhanced self-heating during surge-current pulses.
In reverse direction, closer arranged p-island result in lower leakage currents and less field emission, but also in less stable breakdown voltages.
The measurements on two different types of PiN-diodes were adjusted to TCAD-simulations of the corresponding virtual experiments in a temperature range from 300 K to 773 K. The diodes with higher blocking capability showed a decrease of SRH carrier lifetimes for temperatures above 600 K. This decrease was related to the electrical activation of carbon vacancies known as $EH_{6/7}$-centers within the intrinsic areas of the devices. An empirically deduced equation describing the temperature dependence of SRH carrier lifetimes by three parameters, that include the influences of carbon vacancies at different temperature ranges, was developed. The calibration of the equation allows estimations on the quality of the 4H-SiC epi-layer of a power device and gives feedback to a process engineer.
The measurements in blocking direction showed low leakage currents and a negative temperature coefficient of the breakdown voltage.
The results and knowledge gained throughout the investigations in this PhD-thesis help not only to improve our knowlegde of 4H-SiC power semiconductor device under extreme conditions but also our understanding of predictive TCAD-simulations at high temperatures.

Acknowledgment

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I would like to express my gratitude to my doctorate supervisor Prof. Dr. Gerhard Wachutka for the useful comments, remarks and engagement through the learning process of this PhD thesis. Furthermore, I would like to thank Prof. Dr. Gabriele Schrag and my mentor Dr. Franz Wittmann for supporting me with their scientific knowledge and for guiding me with their experience in the development an empirical PhD-thesis. Many thanks to Stefan Schaub for advising me with regard to all measurement circuits and for the development of a controllable pulsed current source. Moreover, my special thanks go to Dr. Adolf Schöner, Dr. Sergey Reshanov and Dr. Vlodek Kaplan from Ascatron AB (Sweden) as well as Andrei Mihaila from ABB Corporate Research Centre (Switzerland) for providing me with high temperature test-devices and the professional support with regard to process technology and device physics. Also, I would like to thank the participants of my survey, who willingly shared their precious time and knowledge during the elaboration of this PhD-thesis. At least, I would like to thank my family and in particular my partner Mihaela Hanea, who have supported me throughout the entire process.

Contents

Chapter 1

Introduction

The research on semiconductor devices and the fields of applications emerged within the last decades, completely changed the way we are living and communicating with each other, today. Precise process technologies allow the production of wafers including billions of devices that are used in large amounts for low power applications like memories and processing units. Another important task for semiconductor devices is the transportation and conversion of high electrical powers.
The requirements for power semiconductor devices are different compared to low power semiconductors. First, the device geometry has to be larger enabling higher electric fields in blocking direction and higher electric currents during forward conduction. High electric powers dissipate more heat inside the device, therefore an excellent heat conductivity of the semiconductor material is important to avoid thermal runaways. The specific application determines which feature has to be more distinct and thus a broad field of ideas and solutions to create power-semiconductors has been developed in the last decades [1].
Silicon (Si) is the most commonly used material for semiconductor devices. However, it exhibits disadvantages in the field of power semiconductors like it's comparatively small bandgap or it's lower thermal conductivity. It is possible to overcome some of these disadvantages by improving the internal designs of the devices' architectures, however, a more elegant way is to make usage of semiconductor materials that provide better physical properties for the field of power semiconductors.
One of the most promising indirect semiconductors for high-power applications is Silicon-Carbide (SiC). The bandgaps and thermal conductivities of certain polytypes are close to the factor of three larger in comparison to Si. That means e.g. that SiC-devices feature higher blocking voltages than Si-devices with the same layer thickness. The lower intrinsic densities provide lower leakage currents and the higher thermal conductivities stabilize the devices operating at high electric powers [1].

Power semiconductor devices fabricated with SiC have the potential to replace their Si-pendants, but this requires a deep understanding of the process technology and the physical processes inside the devices. The theoretical modeling of the internal design and the physical properties of Si-based devices is ongoing for almost 50 years. Precisely, well established process technologies and programs for 'Technology Computer-Aided Design' (TCAD) that allow for predictive simulations of devices are existing, today [1]. Similar research activities are ongoing for SiC as well, but yet several challenges are to be to overcome. On the one hand the processing of SiC-devices still creates various defects inside the crystal or at the interface to other materials as e.g. SiO_2 underneath the gate of a MOSFET. These defects and surface states cause various effects that reduce the charge carrier lifetime of SiC-device and their long-term reliability.
On the other hand, the theoretical modeling of the physical quantities, relevant to describe the operation of devices, is still incomplete for a lot of high power applications, today.
The purpose of this work is to provide deeper insight in the behaviour of power semiconductor devices under high temperatures and extreme operation conditions. For the empirical investigations a high temperature measurement setup inside a vacuum chamber was established. This setup enables the implementation of four different measurement configurations. So, extreme operation conditions like high blocking fields or large pulsed current densities can be created. A more detailed description of the measurement setup can be found in chapter 2. The devices measured are PiN-diodes and JBS (Junction Barrier Schottky) diodes fabricated of 4H-SiC. The first device type is an adoption from existing Si-devices, therefore a comparison to the Si-technology as well as an evaluation of advantages and disadvantages of the corresponding material can be performed. A JBS diode is a SiC-exclusive device type using the special properties of 4H-SiC to generate an improved device behaviour. The measurements cover many different operation modes of the devices and should give insight the special behaviour of the two types of SiC-Devices and relate them to process technology and material properties.
For the investigations of the physical properties describing the transport mechanisms inside the device corresponding virtual experiments are created with the TCAD simulator 'Sentaurus Device' (SDevice) for several measurement configurations [2]. A more detailed description of the simulation setup and the physical modeling of SiC-devices can be found in in appendix A.

Chapter 2

Measurement Setup for High Temperature Testing

A measurement setup appropriate for the characterization of 4H-SiC power semiconductor devices under extreme operating conditions requires good interconnections with respect to mechanical and thermal stability and a good shielding from external influences.
The measurement setup developed is capable of performing quasi-static measurements either in forward direction with a maximum electric current of 0.1 A and a maximum voltage of 42.0 V or in reverse direct with maximum voltage of 10.0 kV with a maximum electric current of 1.0 mA. In addition to that two different setups for pulsed measurements with maximum electric currents of 10.0 A and 80.0 A are built and characterized in detail enabling the investigation of device under higher electric powers. The operation temperatures for the investigations in this work range from room temperature (approx. 300 K) to 773 K. To ensure the stability of the measurements under extreme conditions (high temperatures, high reverse voltages, high pulsed currents) the setup is integrated in a vacuum chamber and all investigations were performed under high vacuum conditions.
In the following sections the measurement setup for high temperature testing used in this PhD-thesis, the temperature controlling of the vacuum chamber and it's electric connections are introduced. After that, the procedure of creating an electric connection that stays stable at high powers and high temperatures as well as the different measurement configurations and their digital representations are presented. Moreover, four different measurement configurations are shown and discussed based on representative measurement data.

2.1 Vacuum Chamber for High Temperature Measurements

The investigations in this PhD-thesis took place at the laboratory for high temperature measurements at the Chair for Physics of Electrotechnology at the Technical University of Munich. On account of earlier investigations under high temperature conditions [4], the laboratory features a vacuum chamber with pumping equipment and feed throughs for electrical connections. This chamber served as a firm basis for the development of different electric measurement configurations implemented inside it. Fig. 2.1 shows the closed vacuum chamber during a measurement from the outside. It consists of the inner measurement configuration enclosed by a cover made of stainless steel, that is placed on a platform with electric feed-throughs and a connection to the turbo-pump. The turbo pump is connected to a rotary vane pump that serves as backing pump. The entire pump configuration enables investigations under high vacuum conditions (measurement pressure $p_{vac} < 1 \times 10^{-4}$ Pa). This allows stable measurements at high temperature without disturbance of heat convection through air (hot air effects as e.g. oxidation of metal contacts) and also protects the setup from electrical punch-throughs at high voltage conditions (see Paschen's law investigated e.g. in [5]).
Each electrically isolated part of the chamber is connected separately to a common ground made from a copper block to avoid unintended current flows due to differences in the reference potentials throughout the chamber and the measurement devices.
The electric powers used for the majority of the performed measurements are harmful for human bodies. Therefore, the installation of a protective enclosure made of acrylic glass was necessary to avoid electrical contact with the vacuum chamber during measurements. This enclosure includes a front door with interlock switches that necessarily have to be closed before any measurement can be performed.
Fig. 2.2 shows the interior of the chamber that contains a platform for DUTs as well as precision manipulators for an exact placement of the interconnects. The manipulators and the platform are made of premium steel and have been developed and manufactured at the Chair for Physics of Electrotechnology. The inner measurement platform -where the DUT is mounted- is surrounded by a heat shield to keep the temperature stable and to protect the remaining parts of the vacuum chamber from high temperatures.

Fig. 2.3 shows the measurement platform with an exemplary DUT connected to spring-loaded contacts. The heating of the DUT is achieved by current flow through a heater-filament underneath the copper plate that is regulated by a temperature controller (see section 2.2).

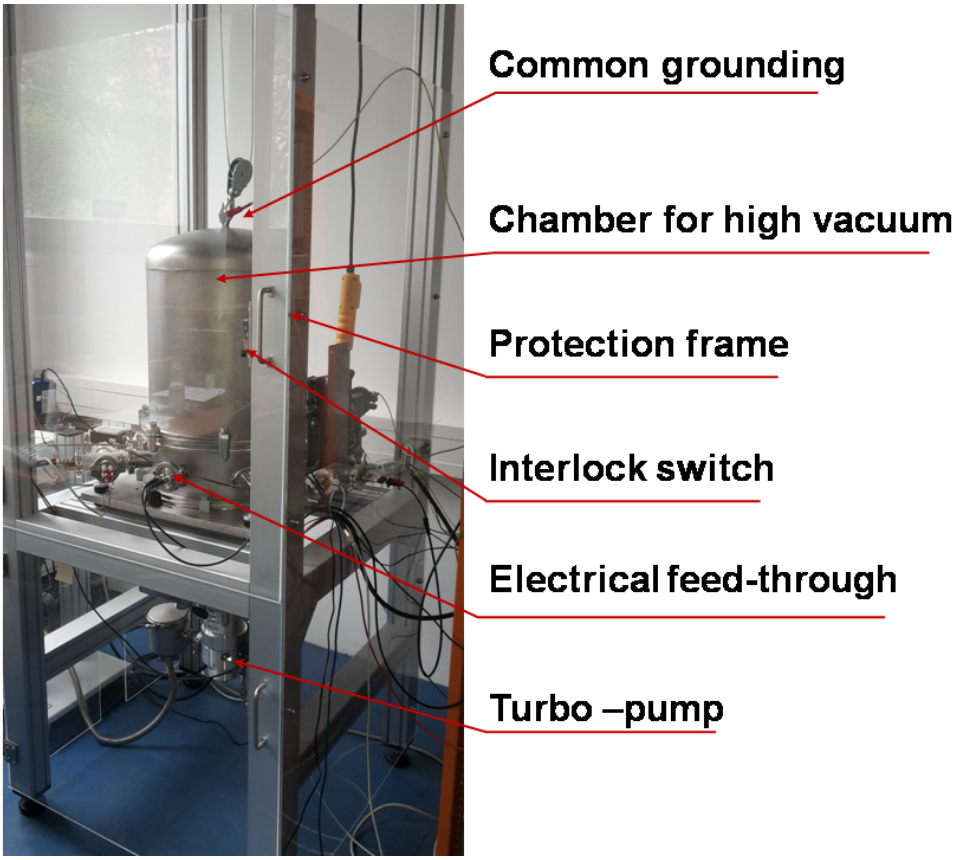

Figure 2.1: Vacuum chamber for ensuring a controlled environment for measurements at high temperatures.

The surrounding of the chamber is protected from high temperatures by a heat shield in close proximity to the heating stage.
A bare die (in this case a PiN-diode) with bottom and top contacts is connected by gold coated spring loaded contacts whereby the bottom contact is sintered with silver onto a gold coated AlN-substrate which leads to a very stable contact (see section 2.3). As additional electrical separation of DUT and heating stage a second AlN-Substrate is placed under the gold coated substrate. A thermal compound forms a joint for the two AlN-substrates and ensures a good heat transfer to the device.
In the next section the temperature controlling for the high temperature measurement setup is introduced.

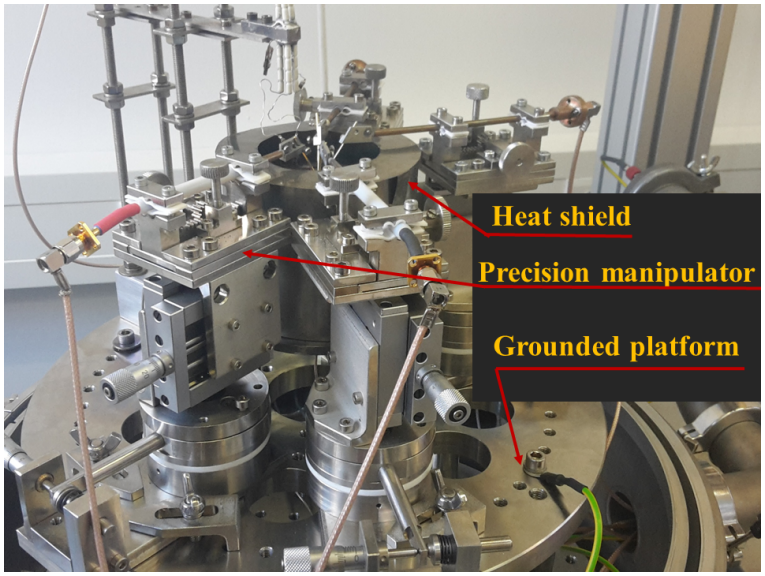

Figure 2.2: Interior of the measurement chamber, containing precision manipulators, a heat shield and a platform for the installation of measurement configurations

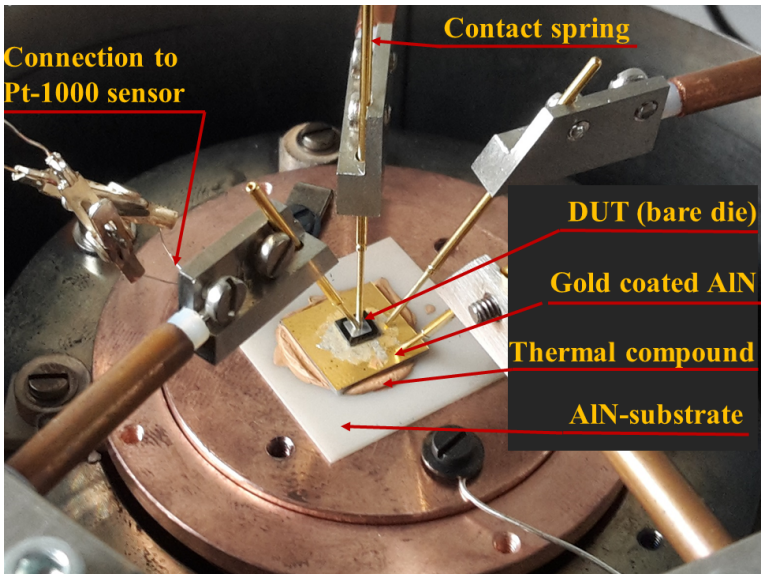

Figure 2.3: Measurement area with heating platform, the temperature sensor and the DUT connected by contact springs

2.2 Temperature Control of the Heating Platform

The contactless heating of the DUT is achieved via a heat filament made of constantan located below the copper-platform. Fig. 2.4 shows a schematic representation

of the electric connections for the temperature control of the sample stage.
A Pt-1000 sensor, located in close proximity to the DUT, is connected to the temperature control unit CN8Pt from OMEGA Engineering GmbH [6]. The CN8Pt provides an analog output signal with a maximum voltage of 10 V, that is used to control the power supply TDK Lambda 1.5 kW. The TDK Lambda 1.5 kW generates a current flow through a heat-filament made of constantan located below the copper chip. As the heating of the DUT is only performed under high vacuum conditions the heat is mainly transferred to the copper plate via heat radiation. The PID-controller of the CN8Pt adopts itself to the time-constants of the system and enables an accuracy in the temperature controlling of 0.1 K. The provided Platinum Series software allows the configuration of the PID-parameters as well as the remote access to the temperature controller.
The limit for the highest measurement temperature is defined by the maximum output-power of the Lambda 1.5 kW power supply from TDK Electronics AG. Depending on the Ohmic resistance of the heater-filament and the quality of the vacuum inside the chamber the maximum measurement temperature ranges between 1000 K and 1100 K. This is sufficient for all devices investigated within the framework of this PhD-thesis.

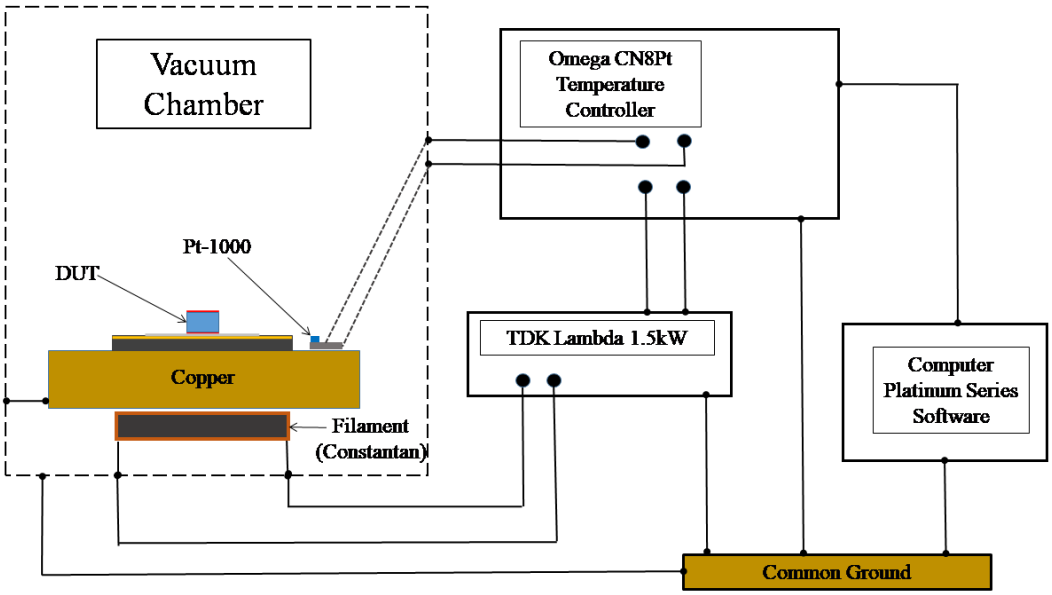

Figure 2.4: Heat control of the measurement chamber. The Omega CN8Pt temperature control unit reads the resistance of the Pt-1000 sensor and controls the TDK Lambda 1.5 kW power supply.

2.3 Bonding of the Test Devices

The electric interconnects of the DUT with the measurement setup are subject to higher requirements compared to conventional contacts (e.g. soldered contacts). While the melting point of tin solder is at around 505 K [8] and is therefore too low for measurements in the complete temperature range from 300 K to 773 K. The top contact of a vertical power device can be connected in a very stable and reliable way by gold coated, spring loaded contacts (see fig. 2.3).
The bottom contact however cannot be connected directly. It has to be bonded on a substrate, where the spring-loaded contacts can be placed. The substrates for all DUTs are made of AlN covered with a 50 nm thick layer of gold deposited via physical vapor deposition. To generate an electrical connection between the bottom contact of the DUT and the gold coated substrate, that remains stable at high temperature, a silver sintering procedure introduced by Schwarzbauer and Kuhnert in [7] is used.

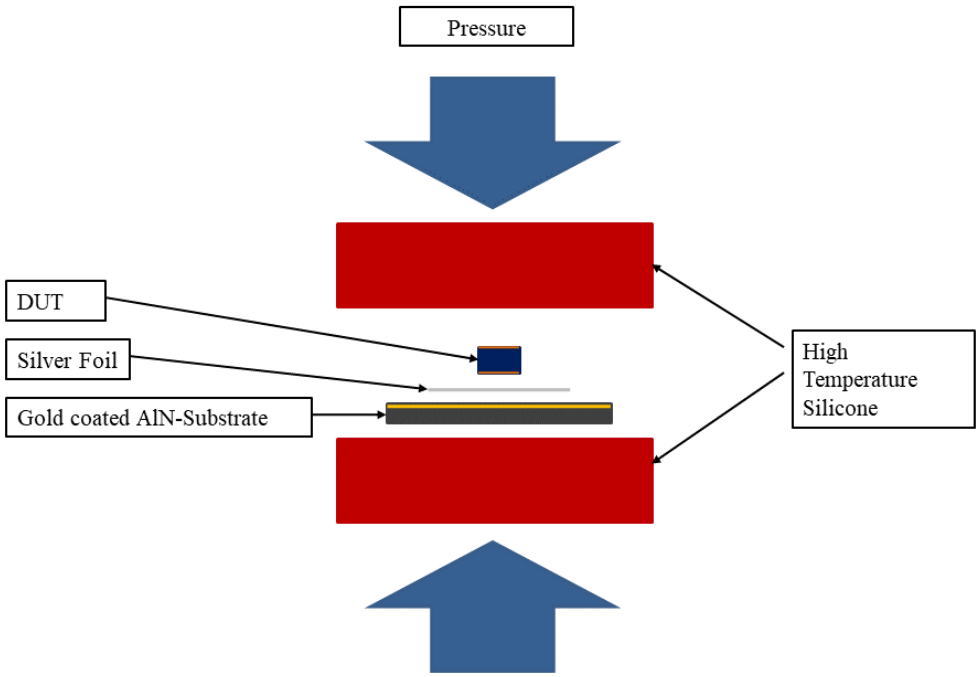

Figure 2.5: Schematic representation of the mechanical pressing during the low temperature joining technique.

For this low temperature joining technique the substrate and DUT are exposed to high pressure together with silver as intermediate layer (see figure 2.5). After reaching the maximum mechanical pressure of the compactor, the complete arrangement is heated up to 573 K (300 C) for 60 minutes. This results in a very stable electric connection sufficient for all measurements within the temperature used in the framework of this PhD-thesis. Fig. 2.5 shows the connection of the bottom contact via gold coated contact springs that are placed on the gold coated substrate whereby the sintered silver foil joins the DUT and the substrate.
This joining technique generates stable electric contacts for the measurements and also enables heat-flow from the bottom contact to the heat sink below. The following section presents a simple estimation of the thermal resistance of the layers underneath the devices rear contact.

2.4 Thermal Resistance of the Heat Sink

A semiconductor device transferring high electric powers generates heat (mainly due to Joule heat). For a commercial device the package serves as heat sink and enables the removal of the excess heat. For the DUT in the vacuum chamber of the high temperature measurement setup the bottom contact is connected to a heat sink consisting of several layers with different thermal resistances R_{th}. Figure 2.6 shows a schematic sketch of the layers consisting of a silver foil, a thin gold layer, the AlN-substrate and a round copper platform (copper-chip).

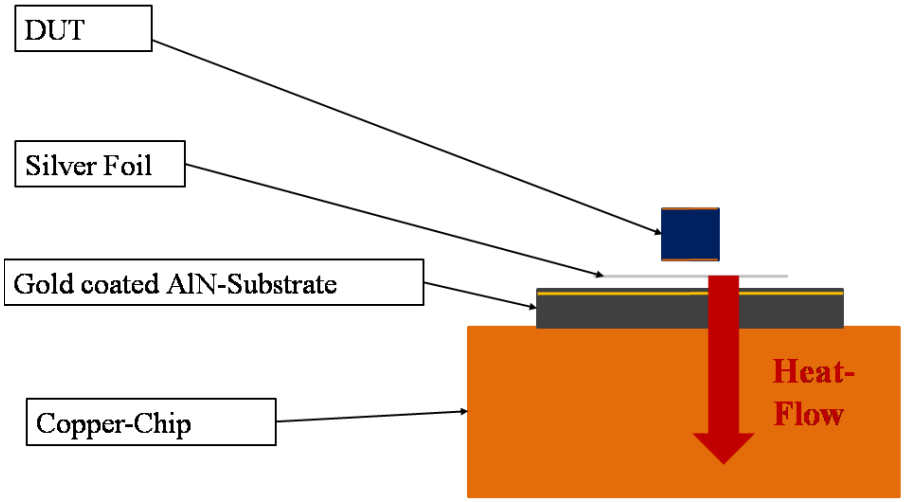

Figure 2.6: Heat sink below the bottom-contact of the DUT consisting of a silver-, a gold-, an AlN- and a copper layer.

A thermal network was used analog to an electric network to calculate the overall thermal resistance by assuming a connection of all thermal resistances in series. The dominant influence originates from the copper platform, that exhibits the largest volume of all layers in the thermal network. This calculation does not take into account the interfaces between the layers and their coupling which are not ideal and increase the thermal resistance, too. The estimation of these intermediate layers is not achievable with reasonable effort with the existing setup. Therefore, a 'best case' estimation was performed by only considering the thermal resistors of the layer connected in series, whereby the spreading of the heat-flow due to different lateral expansions of the layers was neglected. The resulting thermal

resistance is: $R_{th} = 0.041\,KW^{-1}$
The rear contact of the DUT is used as thermal contact with constant temperature (thermode) for all thermodynamic device simulations.
In the next section the average level of electric current caused by static noise inside the vacuum chamber is introduced.

2.5 Average Noise Level in the Vacuum Chamber

The investigation of low current levels (e. g. leakage currents of power-semiconductor devices during measurements in reverse direction) requires a strong discriminability between the average level of static noise in the measurement environment and the actual signals. The minimum level for electric currents inside the chamber was evaluated in different measurements. During the measurements, the gold coated, spring loaded contacts are placed either on a blank AlN-substrate or without connection to any material. Fig. 2.7 shows the results of two measurements at room temperature.

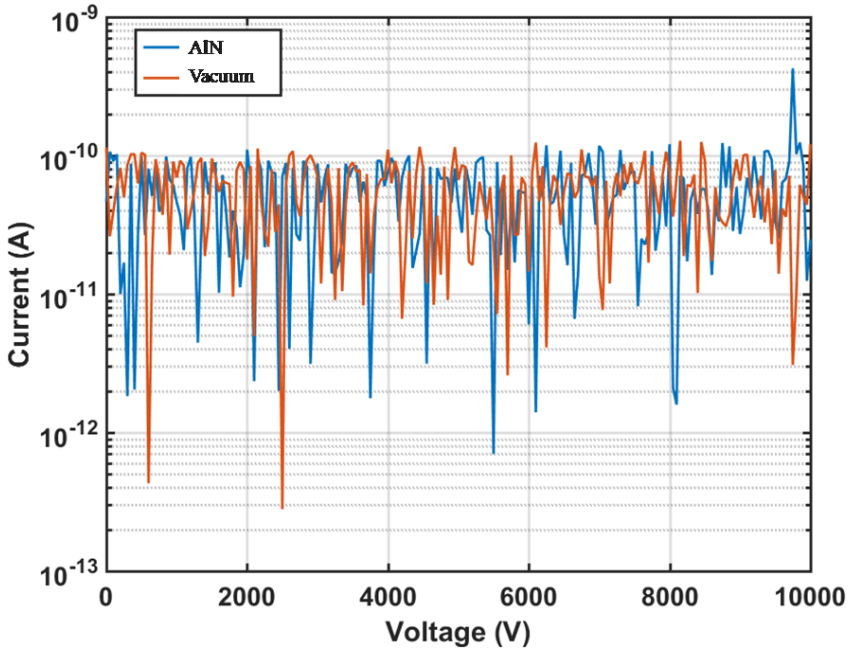

Figure 2.7: Average white noise level at room temperature. The spring-loaded contacts are either placed on an AlN-substrate or in vacuum.

The distance between the contact springs (with high and low electrostatic potential) was 1 cm for all measurements.
The average measured noise level is below 1×10^{-10} A and therefore allows a good measurement-resolution for electric currents in the nA range. This minimum current level is sufficient for all measurements performed within the framework of this PhD-thesis.
The next section introduces the four different measurement configurations implemented in the vacuum chamber.

2.6 Measurement Configurations

The interior of the measurement chamber provides spatial capacity for up to five precision manipulators carrying the electric contact-springs connected to electrical feed-throughs at the chamber's periphery connecting power supplies or measurement equipment outside of the vacuum-chamber. Due to the modular structure of the chamber's interior and the external measurement equipment, several different measurement configurations can be implemented, depending on the intended measurement scenario and the DUT.
Within the framework of this PhD-thesis four different measurement configurations are used and will be introduced in the following section.

2.6.1 Quasi-static Low-current (LC) Measurement

The measurement configuration for quasi-static low-current measurements utilizes the precision IV-tracer E5270B from Agilent as measurement device. It provides slots for 8 different source measurement units (SMUs) that perform quasi-static measurements with high accuracy [9].
Fig. 2.8 shows a schematic sketch of the measurement configuration for quasi-static low current measurements. The chamber as well as the Agilent E5270B and the -here not displayed- temperature control unit are connected to common ground to avoid current loops. The maximum current of all low-current measurements is 100 mA and the E5270B serves as power supply and, at the same time, as measurement device. The connectors force (F) and sense (S) of each SMU enable a four-terminal sensing with high accuracy.

From the triaxial connections of the Agilent E5270B adapters to coaxial-cables, that fit to coaxial feed-throughs of the vacuum chamber are used. BNC-cables (Bayonet Neill–Concelman cable) are used for the connections outside of the vacuum-chamber, the signals inside are transferred via SMC-cables (Sub-Miniature version C cable) to and from the DUT.
Fig. 2.9 exemplarily shows the IV-characteristic of a 4H-SiC PiN-Diode fabricated by ABB (Asea Brown Boveri, Zurich) in forward direction.

In all low current measurements SMU 2 forces 0 V and SMU 1 increases the forced voltage until an electric current of 0.1 A is reached. The best-case level at the lowest signal levels measurable of the forced voltage is 0.1 pV and the accuracy of the current measurements in this scenario is 0.1 pA [9]. The sub-threshold leakage currents of the diode are in the range of nA and can be recorded with high precision.

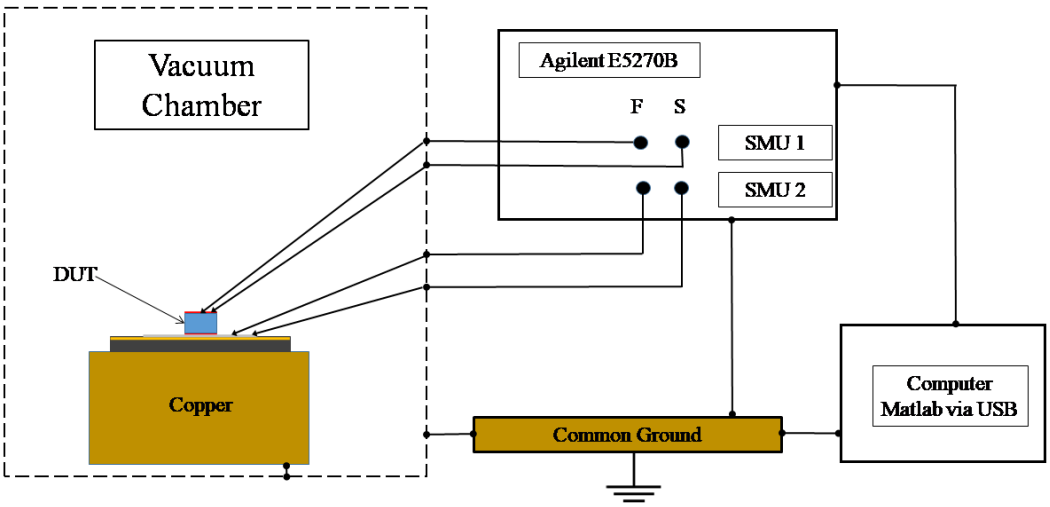

Figure 2.8: Measurement configuration for quasi-static low-current measurements.

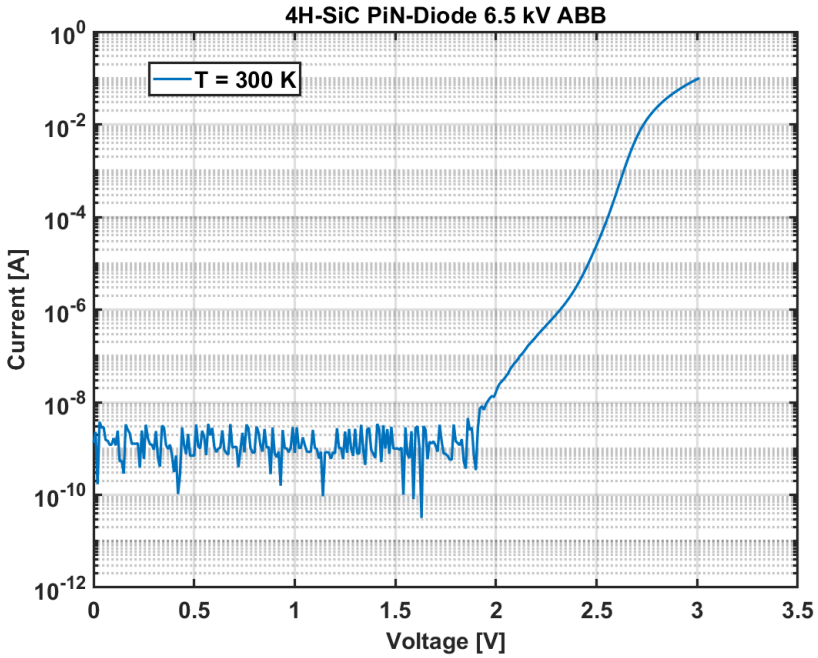

Figure 2.9: Forward characteristic of a 6.5 kV 4H-SiC PiN-Diode at room temperature.

2.6.2 Quasi-static High-voltage (HV) Measurements

Investigations on the blocking capabilities of power semiconductor devices require a source for high voltage and a security circuit to protect the measurement equipment against harmful electric powers. As source for high voltage the Keithley 2290-10 power supply (maximum voltage 10 kV, maximum current 1 mA) was chosen [10]. Stable measurements of very low leakage currents are achieved using the two SMUs of the Agilent E5270B connected to the Keithley 2290-10 PM protection module via two triaxial cables. The protection module ensures the safety of the Agilent E5270B in the case that high voltages are applied on the SMU (e. g. breakthrough of the DUT) [10]. Fig. 2.10 shows the measurement configuration for quasi-static high-voltage measurements. As the measurement voltages are very high and the measurement currents are very low, a two-point measurement outside of the chamber is sufficient for high accuracy. The accuracy of the current measurement is in the range of 0.1 pA as for other quasi-static measurements [9]. The accuracy of the voltage measurement as well as the accuracy of the force voltage is 1.0 V [10].

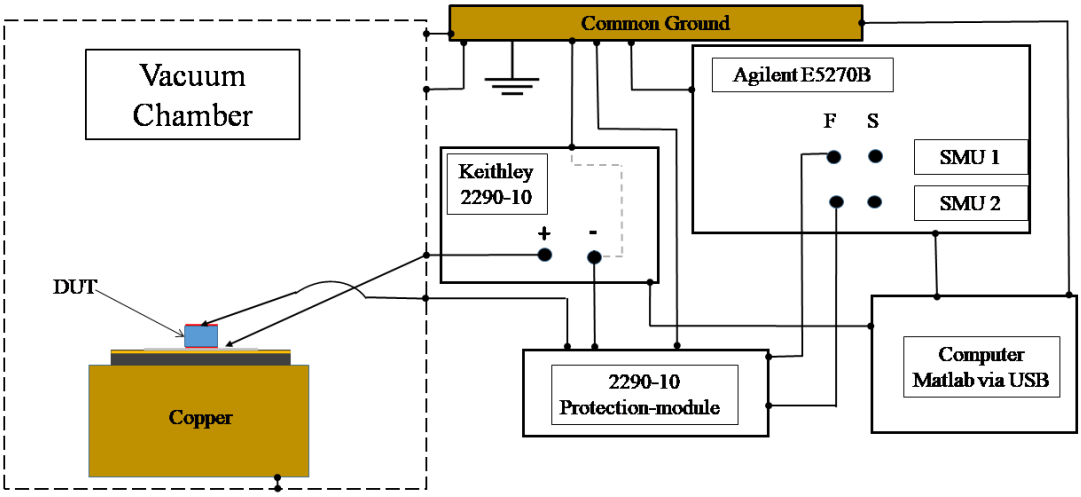

Figure 2.10: Measurement configuration for quasi-static high-voltage measurements.

The control of the Keythley 2290-10 power supply from the software-side via Matlab from The MathWorks Inc. allows fully automatic measurements and additional software-based protection for the user. Fig. 2.11 shows the graphical user

interface (GUI) for quasi-static high voltage measurements during the measurement of a 5.0 kV 4H-SiC PiN-diode fabricated by ABB (Zurich).

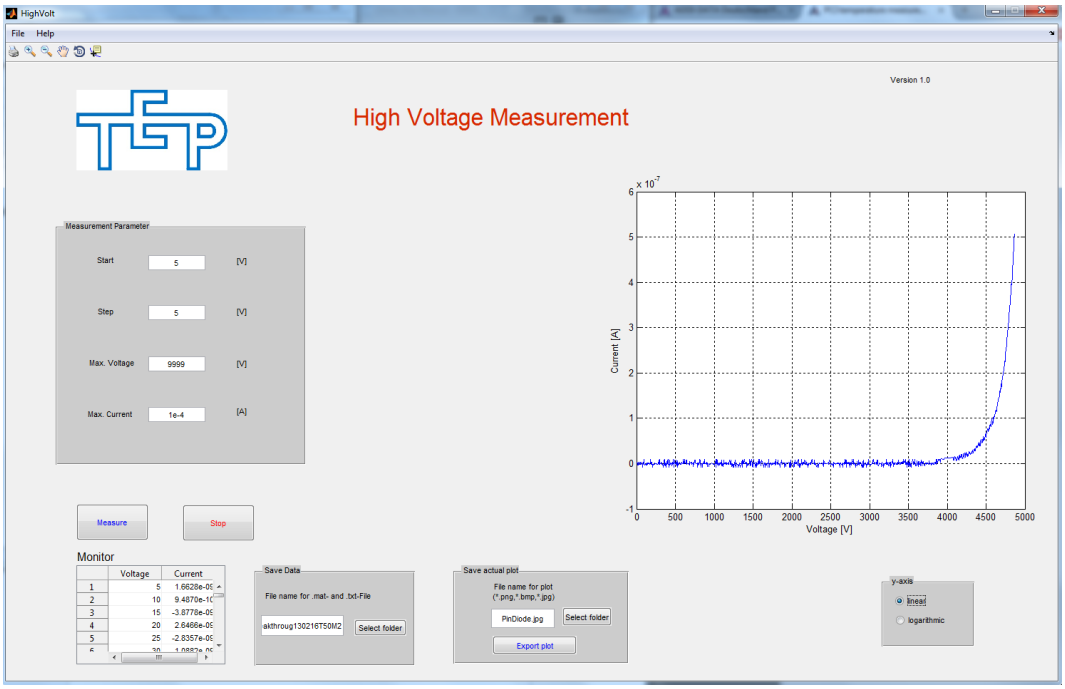

Figure 2.11: Graphical user interface for quasi-static high-voltage measurement. It features data display, break- and step-criteria and the connection to a self-organizing data-base.

2.6.3 Fast Dynamic Measurements

Power semiconductor devices as e. g. PiN-diodes are capable of conducting high electric currents (HC) in quasi-static applications and even higher electric currents during dynamic switching. To investigate the behaviour of 4H-SiC power devices during short pulses of up to 80 A, a pulsing unit was integrated into the measurement chamber. A schematic sketch of the measurement configuration is shown in fig. 2.12. The PicoLas LDP-V80 V3 is a commercial pulsing unit used for the characterization of laser-diodes. Due to its small size in combination with its maximum current of 80 A for a pulse length below 5 μs and its low rise-time of 6 ns the LPD-V80 V3 is sufficient to investigate forward conduction at high electric currents [11]. The LDP-V80 V3 is controlled via 10 digital pins that are connected to a NI-6001 data acquisition box (DAQ), which features -among others- 10 digital output channels and a driver software adopted for Matlab [12]. The rectangular trigger signal for the LDP-V80 V3 is generated by the Rohde and Schwarz AM300 arbitrary and function generator, which features pulsed signals (5 V) with a minimum length of 60 ns [13]. The dynamic current signal is measured by the current monitor (CM) of the LDP-V80 V3. The LDP-V80 V3 uses a shunt-resistor to sense the current and provides the signal at a 50 Ω SMC-output [11]. After passing the feedthrough, the current signal is monitored via a Tektronix TDS 3034B oscilloscope, which features 2.5 GS/s and a vertical resolution of 9 bit [14]. The dynamic voltage signal is sensed with an externally controlled, active voltage-probe (HP54701A), which provides the measured data in a decoupled 50 Ω output-signal [15].
After passing the electric feedthrough, the voltage signal is monitored by the PicoScope 5000, which provides a sample rate of 250 MS/s and a vertical resolution of 12 bit [16].
The integration of the LDP-V80 V3 into the chamber reduces the influences of parasitic elements in the measurement circuit due to its close proximity to the DUT.

Nevertheless, the electrical connections between LDP-V80 V3, precision manipulators and DUT as well as the signal transmission from the probes to the oscilloscopes outside of the chamber have non-negligible influences on the measurement results. Fig. 2.13 shows a lumped element circuit model for the fast dynamic measurements inside the chamber developed in [17]. As the LDP-V80 is a commercial device its exact circuit is not available and therefore it is modeled by a voltage source with the electric capacitance C_{Par} parallel to it and the Ohmic resistance R_{Ser} connected in series. The rise- and fall-times of the voltage source as well as the values of R_{Ser} and R_{Shunt} are taken from[11]. The DUT is symbolized by a diode and the connection to the pulsing unit causes the parasitic Ohmic resistance $R_{Connect}$ and the parasitic inductance $L_{Connect}$. The quantities of the parasitic elements are determined empirically, whereby, the parasitic capacitance of this

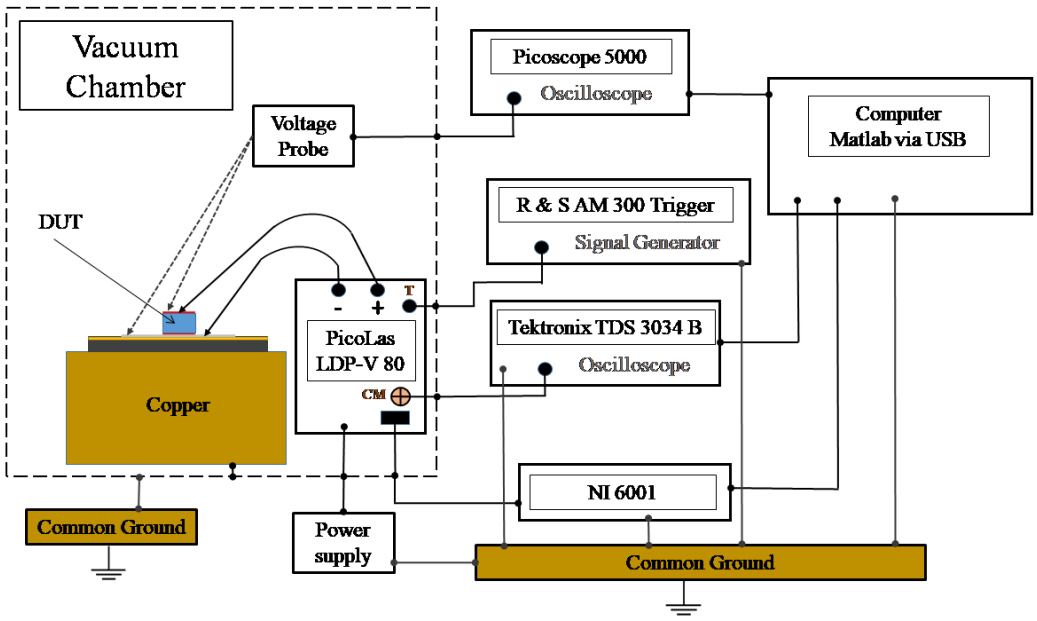

Figure 2.12: Measurement configuration for dynamic measurements with short pulse length (μs).

connection can be neglected [17]. The trigger signal turns on the internal MOSFET of the LDP-V80 V3 and a discharge current from the internal capacitance C_{Par} can flow through the DUT. As the MOSFET operates in its linear region during the pulse, it can be modeled by an Ohmic resistance (R_{MOS}) with the same value as the on-resistance of the MOSFET. The active voltage probe exhibits the internal Ohmic resistance R_{VProbe} and capacitance C_{VProbe} [15]. It's connection to the precision manipulator and the DUT causes the empirically determined parasitic elements $R_{VConnect}$ and $L_{VConnect}$.
As the HP54701A provides its output signal decoupled from the circuit in fig. 2.13, the data-transmission to the PicoScope 5000 does not need to be considered in the lumped element circuit model. For the measurement of dynamic current, the shunt resistance of the LDP-V80 V3 is connected via an SMC-cable to the electrical feed-through and via a BNC-cable connected to the Tektronix TDS 3034B oscilloscope. The values of R_{SMC}, L_{SMC}, C_{SMC}, R_{BNC} and L_{BNC} are investigated empirically in [17]. The values for R_{Tek} and C_{Tek} are taken from [14].
To estimate the influence of the measurement circuit on the measurement results the lumped element circuit model is simulated with LTSpice VII using an Ohmic resistance of 50 mΩ with low internal inductance and capacitance as DUT. This simulation also determines the minimum pulse-length necessary to get stabilized values. Fig.2.14 and 2.15 show the simulation results of both measurement paths.

The voltage signal of the DUT represented by an Ohmic resistor exhibits an inductive peak and is stable after 2.5 μs. The current through R_{Shunt} is also stable after 2.5 μs and can be calculated from the oscilloscope-signal by multiplying it with 40 A/V. The delay in the stabilization of the measurement signals is mainly caused by the inductance $L_{Connect}$. As the LDP-V80 V3 is already in close proximity to the DUT, $L_{Connect}$ cannot be reduced any further. Therefore, a minimum pulse length of 3.0 μs is required to identify stabilized values for the extraction of an IV-characteristic. The disturbance of the signal due to the measurement paths is not visible on fig. 2.14 and 2.15.

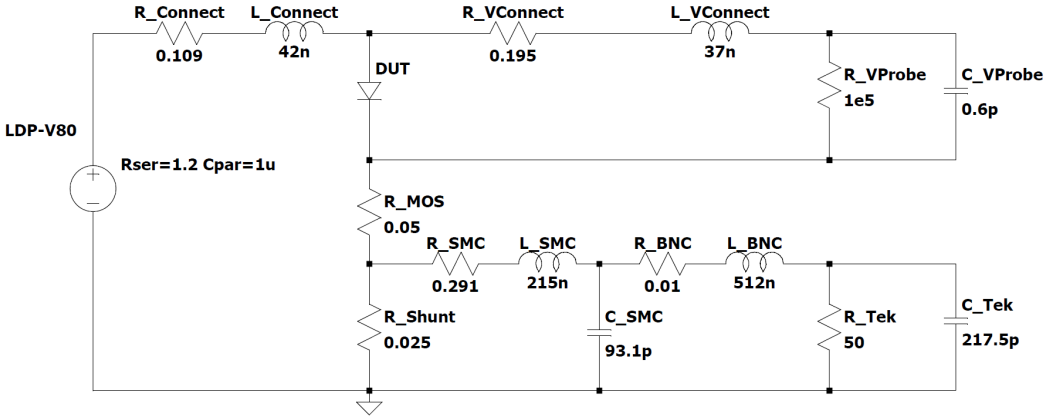

Figure 2.13: Lumped element circuit model for the fast dynamic measurement of a DUT (e.g. a PiN-diode) inside the measurement chamber. The values of the parasitic elements in the measurement paths for voltage and current were determined by empirical investigations in [17].

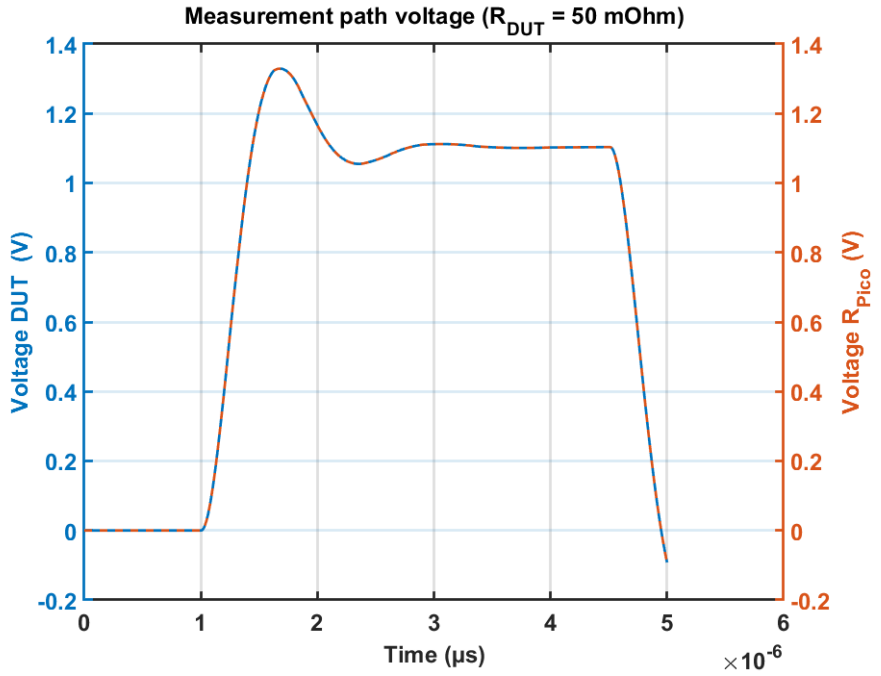

Figure 2.14: LT-Spice-Simulation of the measurement path for voltage. The voltage signals on the DUT (blue) and on the Picoscope 5000 (red) exhibit no visible difference for the Ohmic resistor simulated.

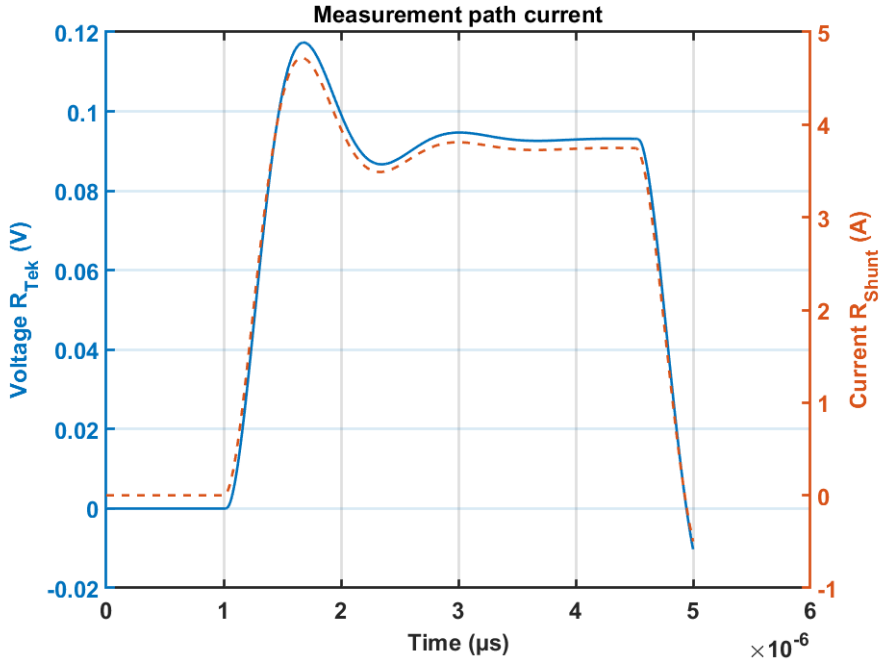

Figure 2.15: LT-Spice-Simulation of the measurement path for current.

Controlling the LDP-V80 V3 pulse generator as well as recording of dynamic signals of voltage and current are accomplished with Matlab. Fig. 2.16 shows the GUI for the extraction of quasi-static forward characteristics from dynamic measurements.

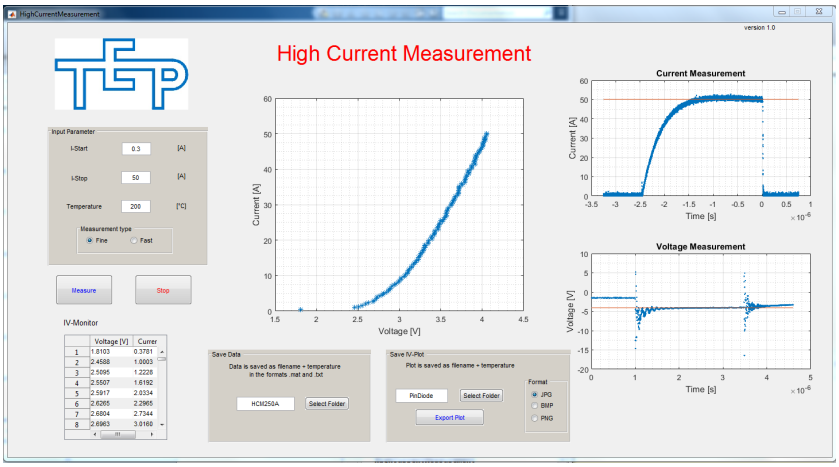

Figure 2.16: Graphical user interface for dynamic high-current measurements. The measured device is a 5.0 kV 4H-SiC PiN-diode fabricated by ABB (Zurich), the maximum current is 50 A and the temperature is 473 K.

The dynamic signals of voltage and current stabilize during a pulse and therefore every pulse generates one point on the quasi-static IV-characteristic. The GUI automatically controls the LDP-V80 V3 current pulsing unit, triggers the pulse, acquires the data from both oscilloscopes, evaluates the asymptotic steady-state values in the dynamic signals and compiles the static IV-characteristic from it. It is connected to a self-organizing database and stores the dynamic and static data of IV-characteristics as well as the calculated respective error in a single file.
The error calculation for the fast dynamic high-current setup considers the accuracies of controlling of the LDP-V80 V3, of the probes for the measurement of voltage and current and the oscilloscopes recording the signal. The vertical measurement error for any point of the quasi-static IV characteristic is strongly dependent on the vertical resolution of the Tektronix TDS 3034B oscilloscope, that is adopted to the measured signal by the GUI. Therefore, the errors of the pulse-measurements are maximal at the maximum current. At a current of 30 A the accuracy of the voltage measurement is 0.5% and the accuracy of the current measurement is 4.0%. For lower currents the accuracy of the current measurement improves to 1.2%. A detailed description of the error calculation can be found in [17].

2.6.4 Slow Dynamic Surge Current Measurements

In this section a setup for 'slow' dynamic measurements for the investigation of the surge current behavior of DUTs is introduced. Surge current is a phenomenon known from applications in the field of high-power semiconductors. It describes operation modes in which devices are exposed to high peak current under exceptional conditions that only last for a short interval of time (e. g. resulting from strong wind gusts at a wind power plant). Devices made of 4H-SiC that are robust enough to withstand strong surge currents mostly are integrated combinations of Schottky- and PiN-diodes. The most common devices are MPS- (Merged-PiN-Schottky) diodes and, as investigated in this study, JBS-diodes. To facilitate these conditions in a measurement chamber it is necessary to generate a current pulse with rising and falling edge and a pulse width between 1 ms to 10 ms, which correlates to the peak-current-length in real applications (see section 3.3).

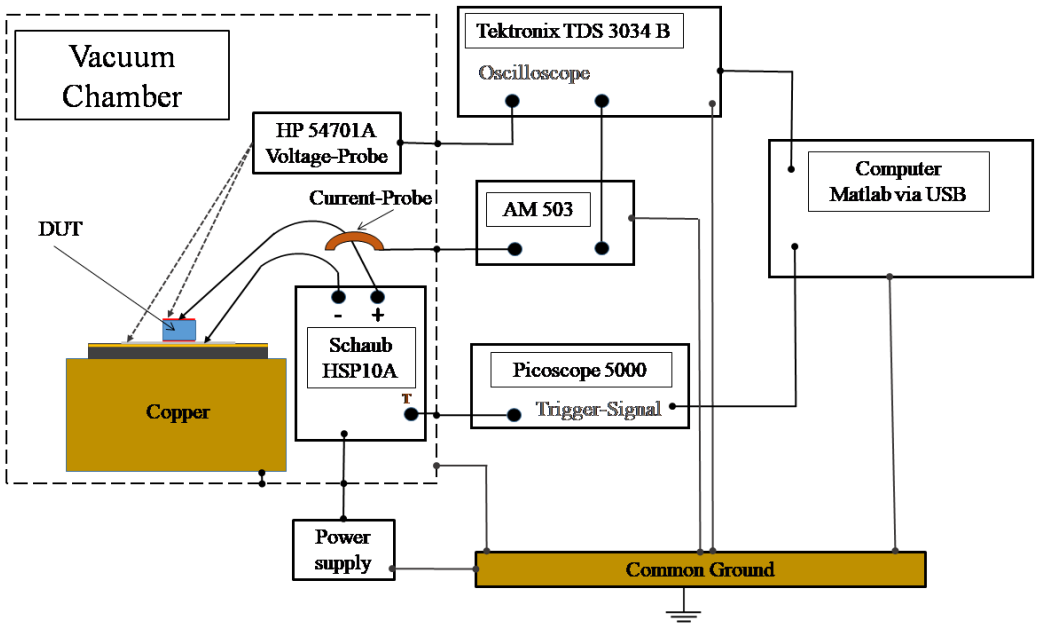

Figure 2.17: Measurement configuration for the investigation of surge current behavior.

To fulfill these requirements, a capacitive pulsing unit (Schaub HSP10A pulse generator) featuring half-sine wave pulses with a peak of 10 A was created [18] and characterized within the framework of [19]. Fig. 2.17 shows the measurement configuration for investigations under surge current conditions. The trigger signals as well as the shape of the pulse are generated by the Picoscope 5000 internal

signal generator, that is controlled via Matlab. The Schaub HSP10A pulse generator is integrated into the chamber to minimize the influence of parasitic elements on the measurement results. The voltage on the DUT is monitored with the HP 54701A voltage-probe and transferred to the Tektronix TDS 3034 B via a 50 Ω BNC-connected signal line. The current is sensed by an inductive current-probe connected to the Tektronix AM 503 Current Probe Amplifier and also transferred to the Tektronix TDS 3034 B via a 50 Ω BNC-connected signal line. The dynamic data is read out and processed via a Matlab-script that controls the measurement.
The connection to the DUT features the comparable parasitic elements as for the LDP-V80 V3, however the pulse width as well as its rise- and fall-time in case of the surge current measurements are by more than the factor of 1000 increased. Therefore, it can be concluded (with regard to section 2.6.3) that the influence of parasitic circuit elements on the measurement results can be neglected.
The accuracy of the dynamic measurements is determined by the resolutions of the HP 54701A Voltage-Probe [15] and the Tektronix AM 503 [20] and evaluated in [19]. The horizontal resolution of the Tektronix TDS 3034 B remains constant throughout a pulse and therefore the accuracy of the measurements remains constant, too. The accuracy of the voltage measurement is 30 mV and the accuracy of current measurement is 37.5 mA and therefore sufficient for a detailed investigation of the surge current behavior of power semiconductor devices.

2.7 Summary of the Measurement Configurations Used

Within the framework of this PhD-thesis four different measurement configurations have been developed and their possible applications were evaluated in terms of accuracy and the maximum electric powers. Table 2.1 summarizes the main features of the two quasi-static while table 2.2 summarizes that of the two dynamic measurement configurations.

Measurement	$\mathbf{V_{max}}$ **(V)**	$\mathbf{I_{max}}$ **(A)**	$\Delta\mathbf{I_{min}}$ **(A)**	$\Delta\mathbf{V_{min}}$ **(V)**
Low-Current	42	0.1	0.1p-1.0n	0.1p-1.0n
High-Voltage	10000	0.1	0.1p-1.0n	1.0

Table 2.1: Measurement configurations for the quasi-static characterization of 4H-SiC power semiconductor devices.

Measurement	$\tau_{\mathbf{pulse}}$ **(s)**	$\mathbf{I_{max}}$ **(A)**	$\Delta\mathbf{I_{min}}$ **(A)**	$\Delta\mathbf{V_{min}}$ **(V)**
Fast	3.5μ	80.0	$0.012\cdot\mathbf{I}-0.04\cdot\mathbf{I}$	$0.005\cdot\mathbf{V}$
Slow	5.0m	10.0	37.5m	30m

Table 2.2: Measurement configurations for the dynamic characterization of 4H-SiC power semiconductor devices. The accuracy of the fast measurement is depending on the pulse-current **I** and the respective device-voltage **V**.

In the next chapter the investigations on JBS-diodes are introduced and the results are discussed with regard to high temperature applications.

Chapter 3

Behaviour of 4H-SiC Junction Barrier Schottky (JBS)- Diodes Under Extreme Conditions

This chapter summarizes the investigations on two different kinds of Junction Barrier Schottky (JBS) diodes fabricated with different blocking capabilities and different geometrical structure.
At first, the concept of JBS-diodes is introduced and subsequently the investigated test-devices are presented. The experimental analysis covers quasi-static low current measurements (section 3.2), dynamic pulsed current measurements (section 3.3) and quasi-static high voltage measurements (section 3.4).

3.1 JBS-Diodes

Schottky-diodes were the first semiconductor devices manufactured on 4H-SiC introduced to the market. Possible reasons are the more stable and reproducible processing of SiC diodes exhibiting only metal-semiconductor-interfaces and no PN-junctions and the lower amount of degradation mechanisms of devices with only unipolar conduction. Therefore, the SiC-Schottky-diode is one of the few devices made of 4H-SiC that can be produced in industrial scale, today [1]. Schottky-diodes exhibit a faster switching speed compared to PiN-diodes, but are less stable at high surge current stress.
To overcome the potentially destructive surge current stress the Merge-PiN-Schottky (MPS) diode was developed. The idea is to integrate p-doped regions into the epilayer of a n-doped Schottky-diode that screen the regions with the unipolar current. During operation conditions with high current peaks (surge current) the Schottky current saturates and the PN-junctions start to inject holes into the epi-

layer. The now developed electron-hole plasma increases the electric conductivity of the device and lowers the overall voltage drop, resulting in an improved surge current stability for the device [21].
Another disadvantage of Schottky-diodes compared to PiN-diodes is their avalanche stability and their leakage currents under high reverse voltage, which is especially problematic for diodes made of SiC. The critical electric field for avalanche breakdown of charge carriers of a SiC Schottky-diode is significantly higher than that of a Si-Schottky-diode with comparable geometry. The disadvantage of this enhanced blocking capability is a high electric field underneath the Schottky-contact, that lowers and narrows the potential barrier (Schottky-barrier) resulting in high leakage currents [22].
The concept of a 'Junction-Barrier-Schottky' (JBS) diode was introduced to reduce the electric field underneath the Schottky-contact. Figure 3.1 shows a sketch of the anode region of a JBS-Diode with two p^+-islands.

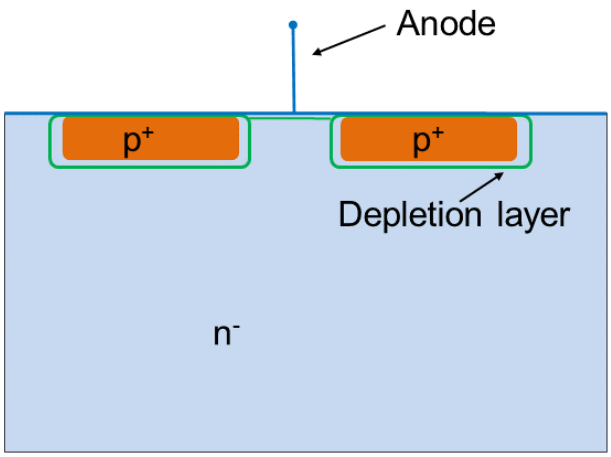

Figure 3.1: Structure of the anode region of a JBS-diode under forward bias. The p^+-islands are enclosed by small depletion regions.

The basic idea is to implant highly p-doped areas below the region of the Schottky contact. This p^+-islands are also connected to the top anode-electrode

and therefore the device contains a grid of small p^+n^--junctions. At voltages below the threshold voltages of the p^+n^--junctions, the device exhibits an unipolar conduction. At higher voltages, the p^+n^--junctions start to inject holes into the n^--drift-layer and therefore modulate the electric conductivity of the device. The impact of the p^+-islands on the electric behaviour of the device is related to the ratio of p^+n^-- and Schottky-areas in the active area of the anode-region. The larger the size of the overall area of p^+n^--junctions the more bipolar conduction will occur. Despite the possible influences on the forward conduction, for a JBS-diode, the purpose of the p^+-islands is to form depletion regions with the surrounding n-doped material in case the diode is under low forward bias (below the threshold voltage) or reverse biased. The depletion regions are able to incorporate electric fields due to the separation of charge carriers. If the depletion regions of adjacent p^+-islands are overlapping the Schottky contact above them is shielded from high electric fields.
In the next section the basic operation modes of a JBS-diode under a bias voltage as well as the concept of buried grid of p^+-islands are explained.

3.1.1 Geometrical Design of the JBS-Diodes

Figure 3.2 illustrates the anode-region of a JBS-diode in reverse direction during three different stages. It was created according to the work presented in [23]. Under a low reverse bias, only minor depletion regions enclose the p^+-islands (1) and an electron-current is flowing from the anode to the cathode (depicted in figure 3.2). Note, that also a negligible bipolar diffusion-current is flowing below the p^+-islands [23].
With increased reverse voltage, the depletion layers of the p^+-islands overlap, yet the shielding of the Schottky contact is not completely established (2). Beyond the pinch-off voltage, the overlapping depletion layers of the p^+n^--junctions accomplish a continuous depletion region, that pinches off the unipolar currents and shields the Schottky contact (3).
The pinch-off of the unipolar current enables a higher blocking capability, but increases the diode's power dissipation in forward direction. In forward direction the depletion layer has to recede to provide a low forward resistance. This results in a higher knee-voltage of JBS-diodes compared to Schottky-diodes. Narrowing the p^+-islands increases the overlapping of the depletion regions, while widening the gap increases the pinch-off voltage. Therefore, the threshold voltage of a JBS-diode is strongly depending on the geometrical design of the device [24] (see section 3.2). As a consequence, the shielding of the Schottky-contact is stronger for a smaller gap and the leakage current is suppressed more efficiently [24] (see section 3.4).

The p^+-islands located directly beneath the contact cause non-uniform potential distributions at the anode-contact due to the differences in the concentrations of

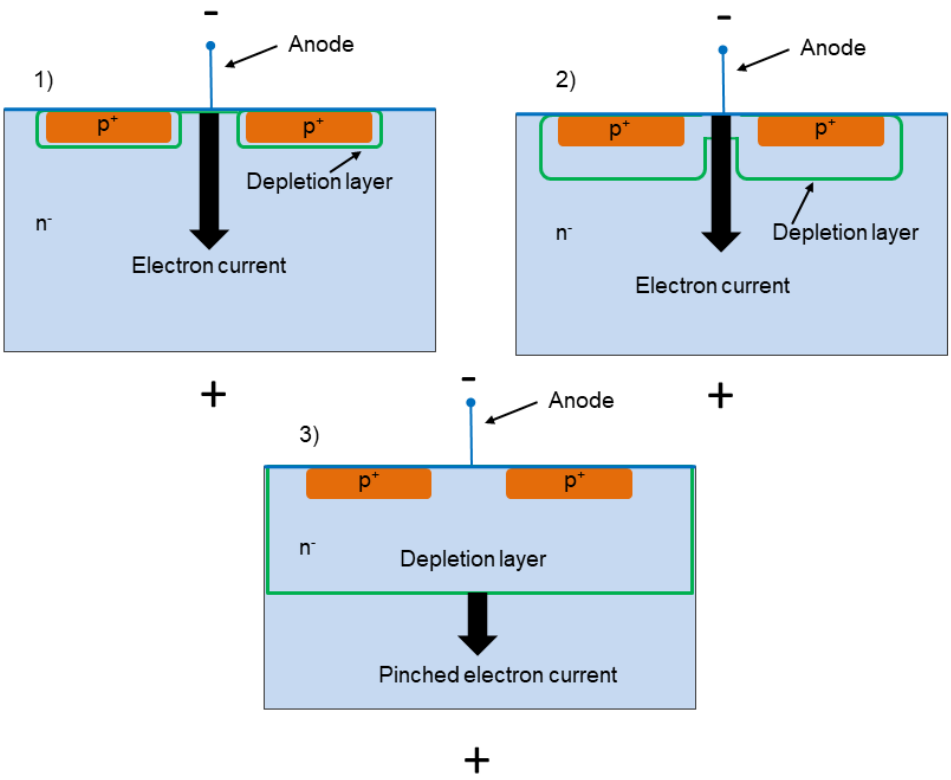

Figure 3.2: Structure of the anode region of a JBS-diode during different levels of reverse biasing (the electrostatic potential of the anode-contact is lower as for the cathode-contact). The black darts indicate the flow direction of the electrons forming the unipolar current.

charge carriers, that get enhanced with higher temperatures. Therefore, the device stability can be improved by burying the p^+-islands into the device structure. This enhances the blocking voltage due to the larger space for the depletion regions and the stability at high temperatures [25]. Figure 3.3 shows the geometry of the anode-region of a JBS-diode with a buried grid. In contrast to the structure shown in figure 3.1, the majority of the p^+-island has no connection to the anode-electrode (right part of figure 3.3). Nevertheless, a fraction of the p^+-island also exhibits an electrical connection to the anode-contact (left part of figure 3.3) [26].

A JBS-diode with buried grid exhibits p^+n^--junctions connected to the top-metallization as well as $n^-p^+n^-$-structures that from parasitic bipolar junction transistors (BJTs). In forward direction, the p^+n^--junctions can inject holes into the drift zone and change the device behaviour from unipolar to bipolar. Each

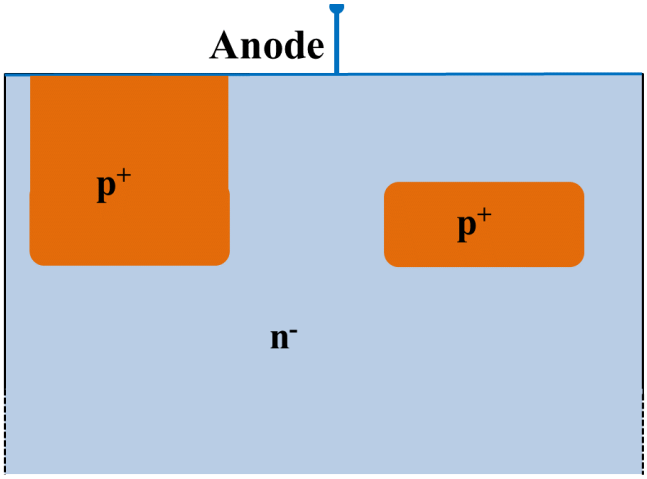

Figure 3.3: Geometry of the anode region of a JBS-diode with buried grid. The p^+-island on the left is connected to anode-contact, the buried p^+-island on the right has no electrical connection.

buried p^+-island serves as basis for a parasitic npn-transitor, the anode-contact acts as collector and the cathode-contact as emitter. If the unipolar electron current rises, the minoritiy carrier density inside a p^+-island increases, too and the parasitic bipolar transistor becomes conductive. Therefore, the electric conductivity of the device increases. Both processes described can enhance the bipolar activation of a JBS-diode with buried grid, but their degree of influence on the forward characteristics is strongly dependent on the ration of the p^+-areas on the total active area of the device. Figure 3.4 shows a section of the upper region of a JBS-diode with buried grid.

For simplicity only a single p^+-island of width W_{PiN} is depicted. The width of the gap between two islands (the "Schottky-area" of the device) is W_S.
In the next section the JBS-diodes investigated in this work are introduced. All of these JBS-diodes exhibit a buried grid and differ in their blocking capabilities as well as their ratios of W_S/W_{PiN}.

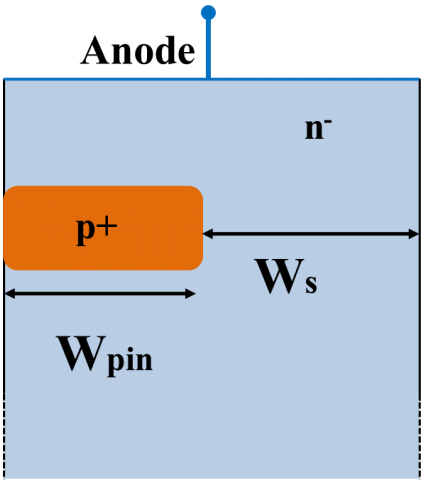

Figure 3.4: Geometry of the anode region of a JBS-diode with a single buried grid.

3.1.2 Test Devices

The test devices discussed in this chapter were designed and manufactured by the company Ascatron AB, Stockholm (Sweden). These diodes are test-devices with variations in geometry, doping concentration and blocking capability [26]. The two kinds of diodes are taken from two different wafers with a blocking capability of 6.5 kV (W1) and 10.0 kV (W2). Both wafers have been subjected to very similar processing, but the epi-layer of W2 is wider and slightly higher doped due to its higher blocking capability. The drift layer of all diodes from wafer 1 have a width of 64 μm with a base n-doping of 1.0×10^{15} cm^{-3}. For the diodes from wafer 2 the width is increase to 85 μm with a doping concentration of 5.3×10^{15} cm^{-3}. Two geometrically different diodes from each wafer, hence with identical doping profiles and metallization contacts, but different ratios of W_S/W_{PiN} were investigated [26]. Table 3.1 summarizes the differences of the diodes presented in this chapter.

Wafer	**Diode 1**	**Diode 2**
W1: 6.5 kV	$W_S/W_{PiN} = 3/1.5$	$W_S/W_{PiN} = 2/1.5$
W2: 10.0 kV	$W_S/W_{PiN} = 3/1.5$	$W_S/W_{PiN} = 2/1.5$

Table 3.1: Blocking voltages and ratios between PiN- and Schottky-areas for the JBS-diodes investigated.

All four diodes exhibit the same ratio of p$^+$-islands connected to the top metallization and buried into the drift-layer as well as a similar distribution of the electric contacts throughout the chip. The contacts were deposited in a stripe shape

with an injection pad in the center of the chip [26].
In the following sections the results of the LC-, HC- and HV-measurements on the JBS-diodes are discussed.

3.2 Analysis of the Low-Current Forward Conduction

In this section the behaviour of four different types of JBS diodes at low electric currents (< 0.1 A) is discussed for temperatures between 300 K and 773 K. As the diodes are supposed to have unipolar conduction, first, the temperature dependence of knee - voltage and the electric conductivity of a unipolar Schottky diode are discussed theoretically. Moreover, both wafers differ in doping concentration and thickness of the epi-layer. Therefore, the expected influence on the forward characteristics caused by these differences are discussed as well. Note, that for every type of diode presented in this section two different devices are measured and every measurement was repeated. As the characteristics of diodes from the same type were almost identical, only one exemplary characteristic per diode and/or temperature is shown in the figures below.
The analysis of the measurement results is introduced after the theoretical considerations and is separated in a low-temperature part (300 K - 473 K) and a high-temperature part (473 K - 773 K) due to different quasi-static behaviour.

3.2.1 Preliminary Theoretical Considerations

In this section the expected results for the knee-voltages and the electric conductivity as well as the temperature dependence of both are discussed.

Knee - Voltage of JBS-Diodes

In section 3.1.1 the pinch-off of the electron-current (majority carriers) due to overlapping depletion regions of p-island is explained. Based thereon, we conclude, that the voltage necessary to recede the depletion regions is higher if the p-island are arranged closer. Therefore, diodes with a larger ratio of W_S/W_{PiN} exhibit a lower knee-voltage for an identical doping profile (same wafer).
The main difference between the two wafers are the doping and the size of the intrinsic areas. The width of a depletion region at a PN-junction is determined by the applied voltage and the doping of p- and n-doped regions. At identical reverse bias, the diode with the lower epi-doping exhibits the wider depletion region in the intrinsic area [1]. Therefore, the diodes on wafer W2 should exhibit the lower knee-voltage due to their smaller depletion regions, that need less voltage to recede.

As the Schottky-barrier is lowered with higher temperatures and the higher thermal energy of the carriers also increases the tunneling probability of charge carriers, the knee-voltage has to decrease with increasing temperatures [1].

Electrical Conductivity of JBS-Diodes

For voltages exceeding the knee - voltage, a JBS-diode starts with a noticeable unipolar conduction of majority carriers. The electrical conductance of a JBS-diode is limited by the electrical resistance of the intrinsic area. Diodes fabricated on the same wafer possess the same doping profile and thickness of their epi-layers and processing. Therefore, they exhibit a very similar electrical IV-behaviour.
Comparing the two wafers, W2 features a thicker epi-layer as well as a higher background - doping. The thickness of the epi-layer reduces the electrical conductance compared to W1, the higher doping results in the reciprocal effect. Equation (3.1) allows to calculate the ohmic resistance R_Ω for the drift-layer of a unipolar device, whereby w_B specifies the width of the drift-layer and $A_{Schottky}$ the active area of the Schottky device [1].

$$R_\Omega = \frac{w_B}{q \cdot \mu_n \cdot N_D \cdot A_{Schottky}} \tag{3.1}$$

As the doping is only slightly higher, but the difference in w_B is more severe, the diodes of wafer W2 exhibit a lower electric conductance in comparison to the diodes of wafer W1.
The temperature dependence of the electric conductivity is mainly influenced by the temperature dependence of the mobility of the majority carriers, that exhibit a negative temperature dependence (see section A.3.1). The influence of rising carrier lifetimes is only relevant during bipolar conduction under low electric powers and therefore JBS-diodes exhibit a negative temperature-coefficient for the electric conductivity [24].

In the following sections the measurement results are evaluated based on the preliminary theoretical considerations.

3.2.2 Low Temperature Characteristics

As first step, the j-V-characteristics measured at room-temperature are compared and interpreted with regard to the previous sections. Figure 3.5 shows the j-V-characteristics for both diodes from W1 for one exemplary diode of each type.

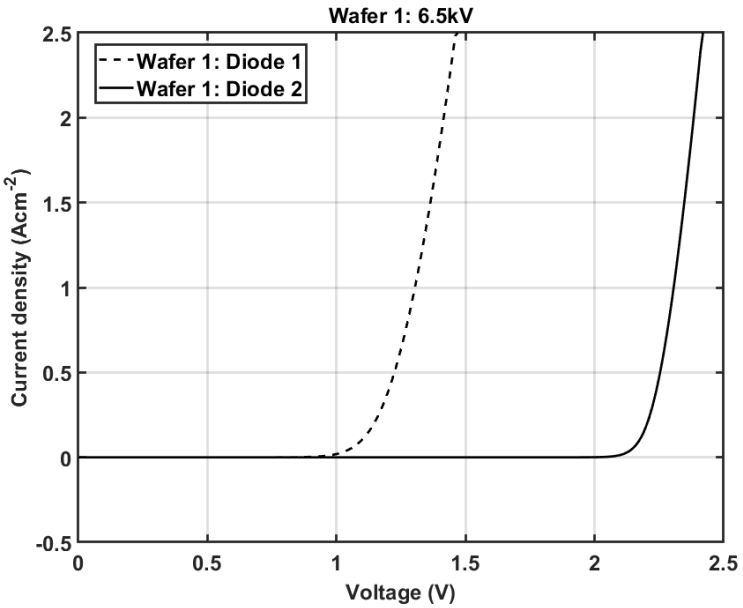

Figure 3.5: Quasi-static j-V characteristics of the two diodes from W1 (Diode 1: $W_S/W_{PiN} = 3/1.5$, Diode 2: $W_S/W_{PiN} = 2/1.5$)

As discussed in section 3.2.1, the larger ratio of W_S/W_{PiN} results in a lower knee-voltage. The knee-voltages of both diodes differ by almost 1 V. This difference is caused by the varying ratios W_S/W_{PiN}. The differential electrical conductance of both diodes is comparable, but from the respective data it is recognizable, that it is slightly higher for diode 1. This is caused by different widths of the depletion layers, that have a direct impact on the electric current as long as they are not fully receded.
The next step is the comparison between both wafers with regard to section 3.2.1. Figure 3.6 shows a comparison between two j-V-characteristics of diodes of type D1 for both wafers measured at 300 K.

The diodes from W2 feature a higher reverse blocking capability due to the larger extend and higher doping of the epi-layer (see section 3.1.2). The lower knee-voltage of the diodes from W2 is caused by the smaller depletion region due to the higher doping concentration. The higher electrical conductance of the diode from W1 shows that the resistance of the smaller epi-layer is lower.
Subsequently, the behaviour of both diodes at temperatures between 300 K and

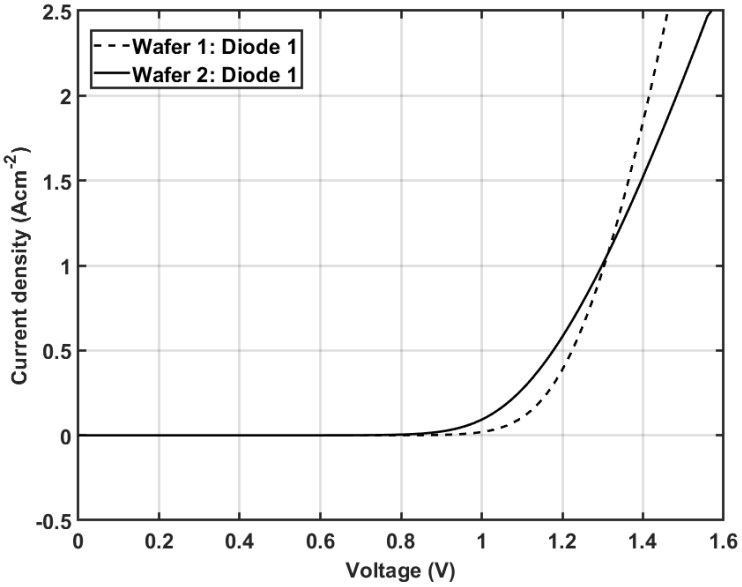

Figure 3.6: Quasi-static j-V characteristics of the two diodes of the same type from W1 and W2.

473 K are presented and discussed.
Measurements on both wafers showed very similar results regarding the differences between both types of diodes. Therefore, only the results for the two types of diodes from W2 are discussed below.
Figure 3.7 and 3.8 show the j-V-characteristics of both types from W2 in a low temperature regime.

Both diodes exhibit decreasing knee-voltages with increasing temperatures. Moreover, the electric conductivity features a negative temperature coefficient resulting in an almost identical point for the three characteristics of both diodes. This is a behaviour known from Schottky-diodes indicating that the forward current is unipolar for both diodes.
In the following section the comparison of the quasi-static forward characteristics is extended to temperatures between 573 K and 773 K.

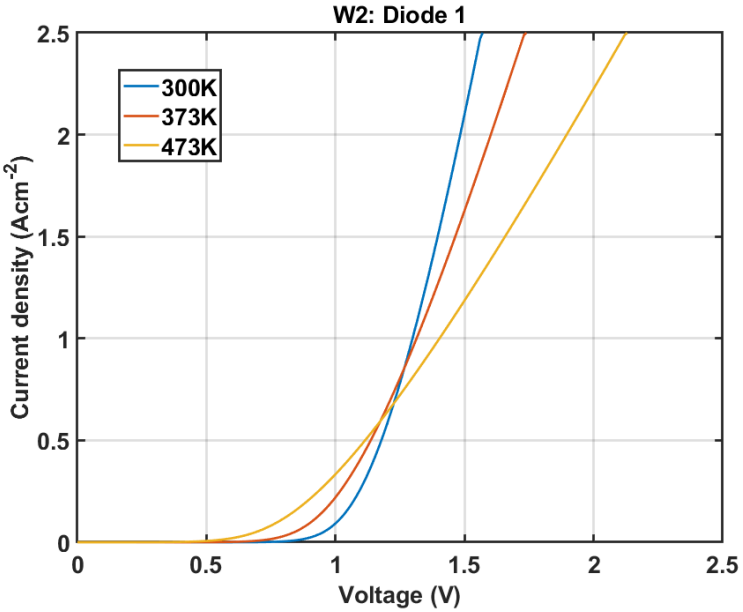

Figure 3.7: Quasi-static forward characteristics of diode 1 from W2 in a low temperature regime.

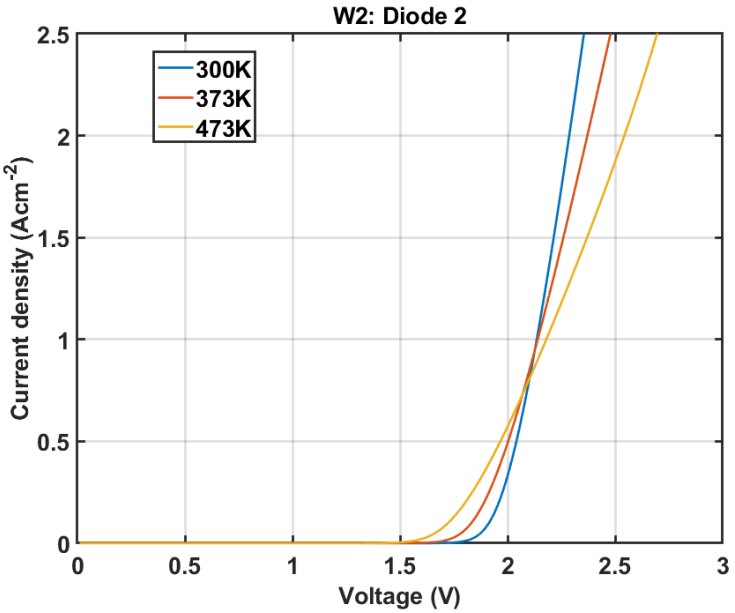

Figure 3.8: Quasi-static forward characteristics of diode 2 from W2 in a low temperature regime.

3.2.3 High Temperature Characteristics

The impact of high temperatures on the forward conduction of a JBS-diode can be estimated on the basis of the temperature dependence of the unipolar Schottky diodes. In the previous section this estimation allowed prediction of a negative temperature coefficient of the electrical conductance of the results at low temperatures (diodes unipolar conduction).
Figures 3.9 and 3.10 present the results of the quasi-static measurements in forward conduction in a temperature range between 573 K and 773 K.

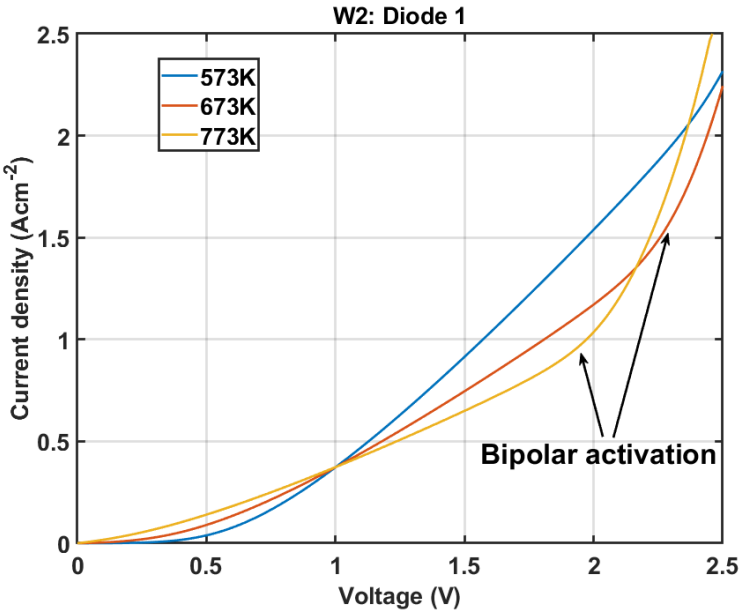

Figure 3.9: Quasi-static forward characteristics of diode 1 from W2 at high temperatures.

The characteristics at 673 K and above in fig. 3.9 as well as all characteristics in fig. 3.10 exhibit a clear non-linear increase in their electrical conductance above a certain level of electric power density. Above the knee-voltage, the increasing slopes of the high-temperature characteristics exceed the linear behaviour visible in figures 3.7 and 3.8. This is an indicator for a temperature-dependent bipolar activation of the devices at low electric powers. This behaviour is - to our best knowledge- so far not reported for JBS- or MPS-diodes. The scientific research on MPS-diodes suggests that bipolar activation is triggered at significantly higher electric current densities compared to the characteristics in figures 3.9 and 3.10 [21, 27]. The high operation temperatures enhance the injection of holes into the drift-zone by the p^+n^--junctions and the turn-on of the parasitic $n^-p^+n^-$- bipolar transistors. This leads to varying degrees of bipolar current depending on the

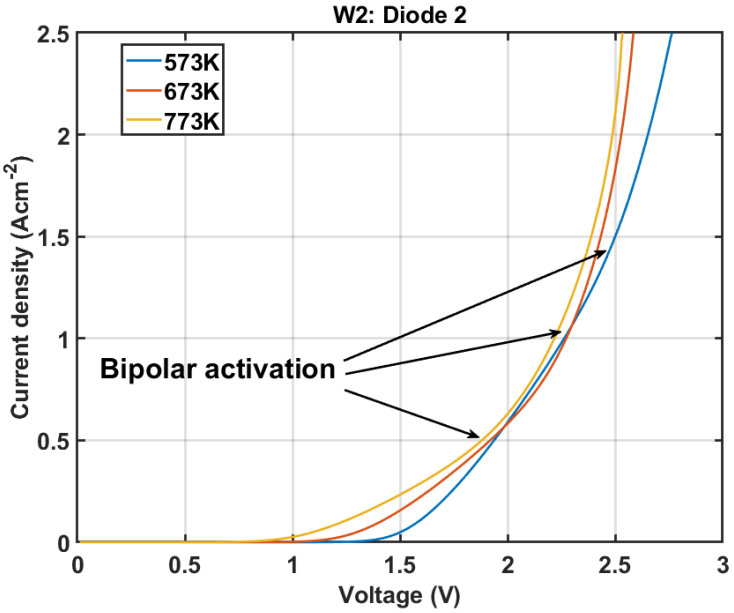

Figure 3.10: Quasi-static forward characteristics of diode 2 from W2 in a high temperature regime.

device temperature and geometry.
As the overall area of the buried and connected p^+-grids in Diode 2 is larger than that of Diode 1, the number of injected holes is higher and, therefore, the modulation of the electric conductivity is stronger (for equal active areas of both devices). Diode 1 exhibits a clearly visible temperature-stable point in the high temperature regime, but the sign of the temperature coefficient of the electrical conductance changes after the bipolar activation. This results in two intersections of the characteristic at 573 K and 673 K. Diode 2 shows a similar behavior, but the bipolar activation is triggered at lower power levels due to the higher number of holes in the drift-zone. The characteristic at 773 K exhibits the bipolar conduction at such a low electric power, that it does not share a temperature-stable point with the other characteristics, which is a behavior known from bipolar devices like PiN-diodes. In comparison, Diode 1 requires less electric power to reach the maximum electric current density of 2.5 Acm^{-2}, but the electrical conductance of Diode 2 is significantly higher at all characteristics exhibiting bipolar activation. Both devices switch to a temperature-enhanced bipolar activation at low electric power levels, but the higher amount of injected holes in the diode with lower ratio of W_S/W_{PiN} leads to an improved transition from unipolar to bipolar conduction.
In the next section the analysis is extended to dynamic measurements under even higher electric powers with a maximum electric current density up to 250 Acm^{-2}.

3.3 Analysis of the Surge-Current Capability

Surge current is a phenomenon encountered in several applications of high-power electronics, specifying conditions in which power devices are exposed to a high electric current density under exceptional conditions that only last for a short time period.
If a certain level of electric current is “squeezed” through a JBS-diode, the p^+-regions start to inject holes into the drift-zone and the electrical conduction changes from unipolar to bipolar charge carrier transport. The previous sections provide evidence that the amount of injected holes is strongly dependent on the ratio of W_S/W_{PiN} as well as the threshold voltage, at which the bipolar operational mode is activated (“turning voltage”). During the dynamic measurements presented subsequently the devices are subjected to half-sine-shaped current pulses with a maximum peak current density of $250\,\mathrm{Acm^{-2}}$ and a pulse width of 5 ms. Note, that for every type of diode presented in this section two different devices are measured and every measurement was repeated. As the characteristics of diodes from the same type were almost identical, only one exemplary characteristic per diode and/or temperature are shown in the figures below.
Figures 3.11 and 3.12 show the dynamic signals of voltage and current at a device temperature of 300 K whereby the fit-functions are contained for the extraction of a quasi-static characteristic. The decrease of the device voltage during rising electric current density (indicated in fig. 3.12 by "Bipolar Activation") is a clear sign of a conductivity modulation and therefore a bipolar activation. The dynamic characteristics of voltage and electric current density are traced by two different test probes and, therefore exhibit a slight time-shift between each other. To ensure that the extracted j-V-curves reflect the real device behavior, all extracted dynamic characteristics are shifted so that they coincide with the previously obtained low current forward characteristics (within the error margins of the measurement setup).

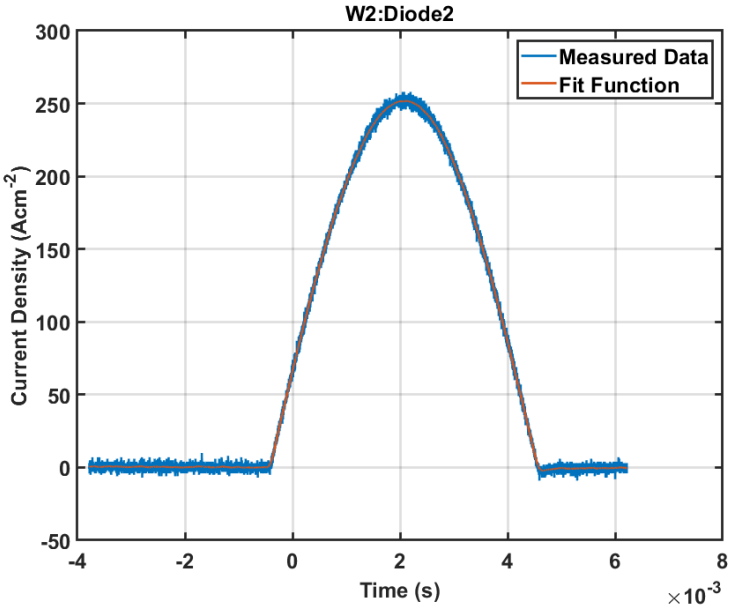

Figure 3.11: Dynamically measured electric current density for diode 2 from W2.

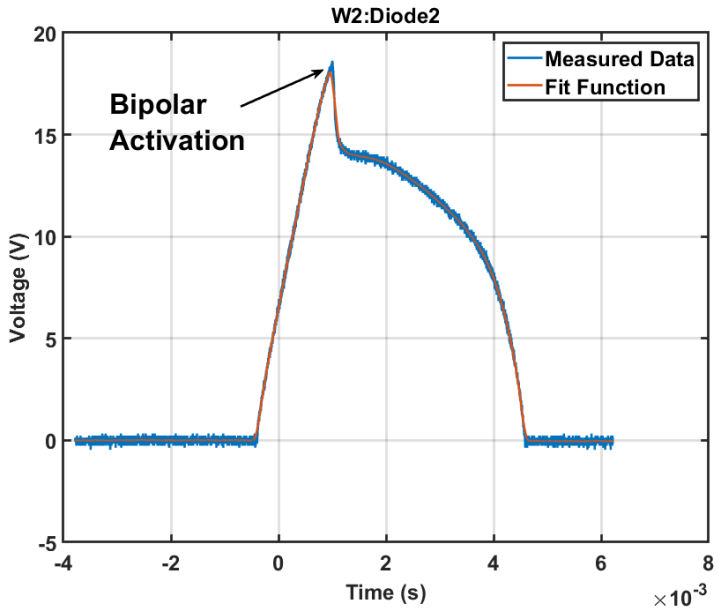

Figure 3.12: Dynamically measured voltage for diode 2 from W2.

Fig. 3.13 shows the respective quasi-static j-V-trajectory of the device extracted with by combining the fit-functions of the dynamic signal of voltage and electric

current density. The voltage level that marks the beginning of the transition from the unipolar branch (HC_{up}) to the bipolar branch (HC_{down}) is labeled as V_{turn}.

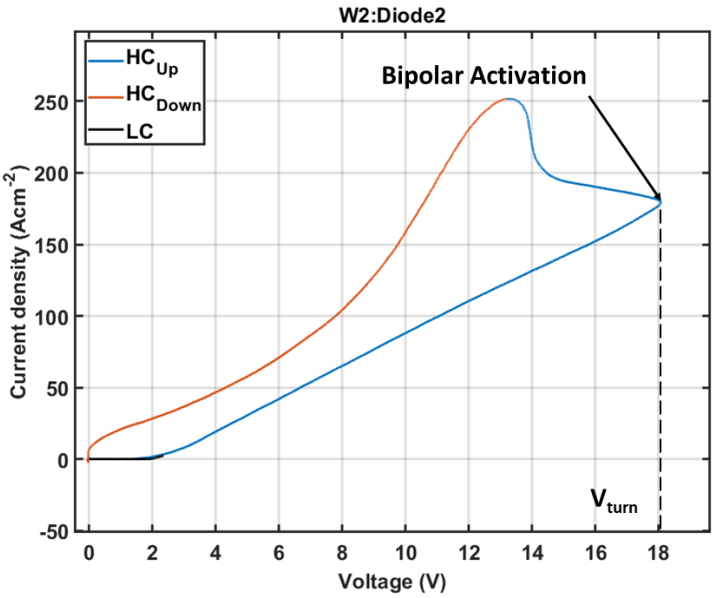

Figure 3.13: j-V-curve extracted from dynamic measurements. The low current measurement (LC) serves as a reference for the quasi-static j-V-characteristics. The difference between HC_{up} and HC_{down} is caused by the bipolar activation and the self-heating of the device.

From figure 3.13 we see a turning voltage V_{turn} of the device of 18.1 V that marks the starting of bipolar activation. In consequence of the formation of an electron-hole plasma inside the drift-zone, the device exhibits a negative differential resistance, until it has reached the bipolar branch of the j-V-curve (HC_{down}). To enable a high reverse blocking capability, the charge carriers inside the diodes must have a long carrier lifetime, which also implies a strong current flow in forward direction and thus a fast self-heating of the device. This self-heating can be recognized in the graph of HC_{down} in fig. 3.13. The rising device-temperature increases the intrinsic carrier density and the carrier lifetimes in the drift-zone and therefore, the self-heating increases, too. Moreover, as the intrinsic carrier density rapidly rises with increasing temperature in 4H-SiC the carrier mobilities are decreasing by the enhanced generation of heat through scattering of carriers with the 4H-SiC lattice. For the decreasing current during the second half of the pulse the time is not sufficient to remove all charge carriers and the device does not completely cool down to the ambient temperature.

Therefore, the device attains a different lattice temperature and a different level of carrier densities even at the end of the surge current pulse. To investigate this behavior several measurements with different pulse lengths varying between 1 ms and 10 ms were performed on a diode of type 2 from W2. Figure 3.14 shows the dependence of the turning voltage V_{turn} on the pulse length. The decrease of the turning voltage with increasing pulse-length in combination with decreasing electric current densities at the turning points is a clear indicator that the bipolar activation of the device is enhanced by thermal energy. As a pulse length of 5 ms is best suited for applications intended for these diodes [26], this length was taken for all further surge-current-measurements.

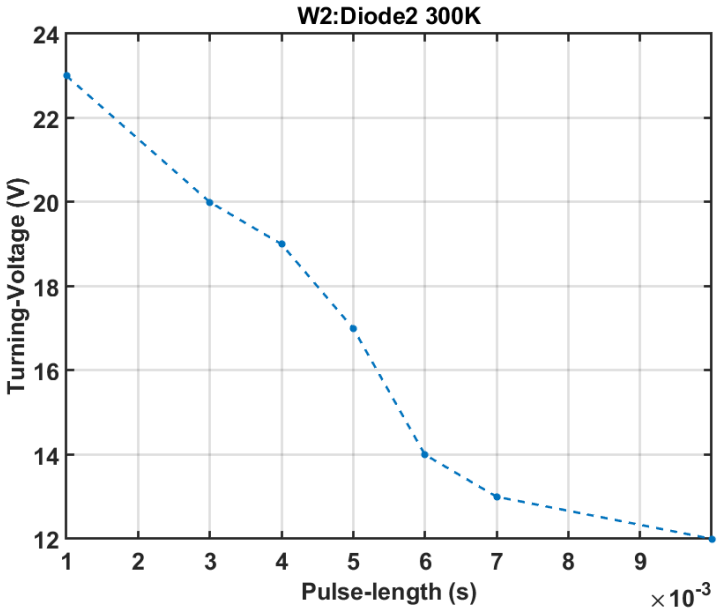

Figure 3.14: Dependence of the turning voltage V_{turn} on the pulse length for Diode 2 from Wafer W2 at 300 K.

Figures 3.15 and 3.16 exemplarily show a comparison of the surge current behaviours for both types of diodes from wafer 2 investigated at 373 K and at 523 K. Based on the low current measurements (section 3.2) we found that for temperatures below 573 K both diodes show unipolar conduction at relatively moderate electric power. Hence, the bipolar activation at temperatures below 573 K is investigated during a HC-pulse. All samples of Diode 2 showed a lower turning voltage at all temperatures between 300 K and 523 K in comparison to diodes of the type 1, which confirms well with enhanced capability of turning into the bipolar mode as examined in the previous sections.

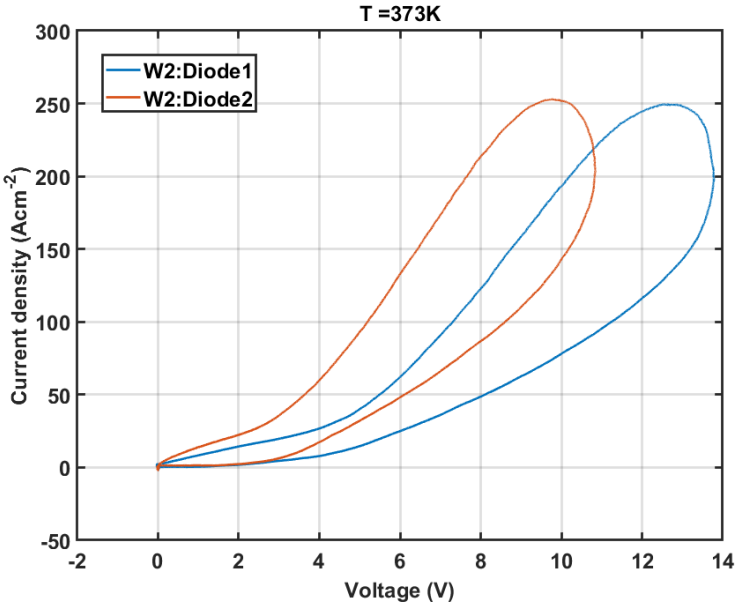

Figure 3.15: j-V-characteristics extracted from dynamic measurements at a temperature of 373 K.

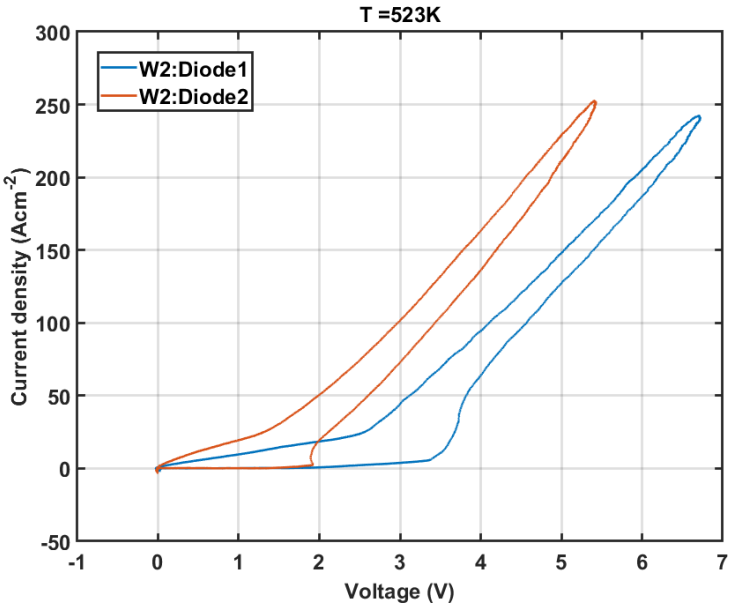

Figure 3.16: j-V-characteristics extracted from dynamic measurements at a temperature of 523 K.

The amount of self-heating can be qualitatively estimated by the difference between the characteristics of rising and falling electric current density. We conclude from the j-V-curves at 523 K that a larger spacing between the buried p^+-islands results in a smaller difference between the rising and the falling slope of the j-V-characteristics. This is an indication for a dependence of self-heating on the ratio of the Schottky-to-PiN current distribution as reported in [28].
Therefore, Diode 1 provides lower self-heating, remains more stable at high electric powers and requires more electric power to start bipolar conduction. During all surge-current measurements, Diode 2 shows the superior electric conductivity due to a higher level of injected holes. Diode 1 requires a higher electric power to reach the electric current density of 250 Acm^{-2}.
Supplementing the results discussed so far, fig. 3.17 displays the temperature-dependence of the turning voltage for both types of diodes under investigation for a pulse length of 5 ms. Diode 2 exhibits the lower turning voltage over the entire temperature range considered in consequence of its smaller ratio of W_S/W_{PiN}.
Nevertheless, the bipolar activation has caused self-heating inside the device, that can be destructive during a real application. Therefore, there is a trade-off between improved electric conductivity and self-heating that has to be considered.

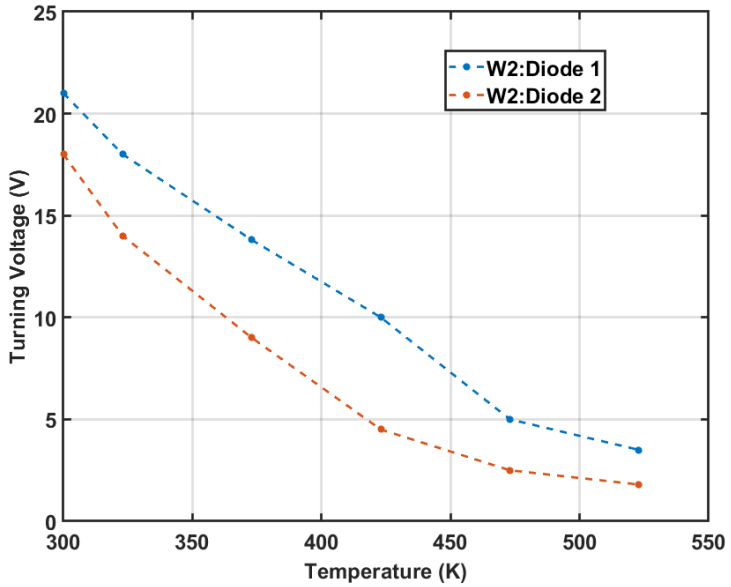

Figure 3.17: Temperature dependence of the turning voltage triggering the bipolar activation of W2:Diode1 and W2:Diode2 at a pulse length of 5 ms.

After the investigation of the bipolar activation of both types of diodes, the next section will discuss the reverse breakdown voltages as well as the leakage currents once again regarding the geometrical properties of the devices.

3.4 Analysis of the Blocking Capability

This section investigates the blocking capability of all four types of diodes introduced in section 3.1.2. The measurements performed are quasi-static, as presented and explained in section 2.6.2. Before discussing the measurement results, the theoretical modeling for leakage currents and the avalanche generation through impact ionization are summarized.

3.4.1 Preliminary Theoretical Considerations

In this section the two dominating leakage current mechanisms as well as the theoretical modeling of impact ionization are introduced, particularly in view of their high temperature dependence.

Mechanisms of Leakage Currents

The interface between the metallization of the anode contact of a JBS-diode and the n-doped semiconductor exhibits a potential barrier, the so called Schottky barrier. In forward direction, this energy barrier can be overcome by applying a positive voltage.
In reverse direction, the negative bias increases the height and the width of the potential barrier. Thus, the charge carriers will have less probability to pass the barrier. Nevertheless, a comparatively small electric current (leakage current) can be measured in the reverse direction. For JBS-diodes the leakage current is composed of mainly two different mechanisms [22].
At elevated temperatures, charge carriers acquire sufficient thermal energy to overcome the potential barrier. The contribution to the leakage current through this thermionic emission depends on the Schottky barrier height [22].
As the reverse voltage is increased the electric field intensity below the metal-semiconductor junction increases as well. The probability of charge carriers tunneling through the Schottky barrier depends on the electric field intensity and rises with increasing reverse voltage. This field emission of carriers through the barrier depends on the width of the Schottky barrier [22].
Moreover, with rising temperatures the intrinsic density (section A.2.2) as well as the degree of ionized dopants (section A.2.3) in the n-doped 4H-SiC will increase, enabling more charge carriers to overcome the potential barrier. Therefore, leakage

currents of JBS-diodes increase with elevated temperatures.
The p^+-islands and the n-doped 4H-SiC inside the JBS-diode form depletion regions, that overlap and shield the Schottky contact from high electric fields. As this shielding is not ideal, the electric field below the Schottky contact will rise with increasing reverse bias, too. An increase in the electric field reduces the width as well as the height of the Schottky barrier and therefore increases both mechanisms for leakage currents [22].
The JBS-diodes from one wafer defer in the ratio of Schottky- to PiN-area, which has direct influence on the leakage currents. A smaller distance between the p^+-islands results in a better shielding of the contact-region, hence a reduced electric field dependent leakage current. As consequence, the 'Diodes 2' from both wafers are expected to offer lower leakage currents.

Temperature and Field Dependence of Impact Ionization

If a power device is subjected to a high reverse voltage the charge mobile carriers inside may gain high kinetic energies due to acceleration in the electric field. Mobile free charge carriers may lose energy via interaction processes with lattice atoms and - after a critical electric field limit is exceeded - this can excite another electron from the valence into conduction band. This results in additional mobile electrons and holes which can even induce subsequent impact ionization processes, eventually causing an uncontrollable avalanche of charge carriers and most likely the destruction of the device [1]. The generation of charge carriers through impact ionization is related to the ionization coefficients of electrons (α_n) and holes (α_p). These parameters have a major influence on the blocking capability of a power device and their theoretical modeling for 4H-SiC is examined in several empirical investigations. The research covering - to this date - the widest range of electric fields and temperatures was published in [29].
Summing up, the field dependence of both ionization coefficients can be modeled by an adoption of Chinoweth's expression [30]. It shows an increase of both coefficients with rising electric field, whereby α_p is higher as α_n [29].
The temperature dependence of α_n and α_p is different which is influenced by the energy spectra in the valence and the conduction band. The energy spectrum in the valence band of a 4H-SiC crystal is continuous whereas it is discontinuous in the conduction band resulting in a less efficient impact ionization for electrons as described in [31]. Both coefficients are decreasing with rising temperatures due to a reduction of the free path inside the SiC-lattice, that leads to a lower average kinetic energy of charge carriers for the same applied electric field. Recent empirical studies show, that for temperatures between room temperature and 423 K the decrease of α_p as well as α_n is visible [29].
In summary, the ionization coefficients exhibit a negative temperature dependence.

As consequence, the ionization rate and therefore the generation of charge carriers decreases with rising temperatures. As the ignition of an avalanche of charge carriers is mainly dependent on the ionization coefficients and the electric field, the avalanche breakdown of a JBS-diode has to exhibit a positive temperature coefficient. It is important to note, that an increase of the breakdown voltage with rising temperatures is only guaranteed if the electric field peak igniting the avalanche is located at the PN-junctions shielding the contact. Here, the high electric field is directly related to the applied reverse voltage and the doping of the material. Another possibility for the development of a localized peak in the electric field can be a weakness of the inner structure induced during the processing of the device. A high curvature or a crystal defect e.g. at an edge termination may lead to an accumulation of carriers and therefore to a potentially high electric field, that can ignite an avalanche, too [31].
In the next section the results of the reverse characteristics of selected JBS-diodes are presented and analyzed with regard to the discussed mechanisms for leakage currents and the electrical breakdown of the device.

Blocking Characteristics at Room Temperature

In this section, results for diodes fabricated on different of wafers (6.5 kV and 10 kV), each with different geometric rating W_S/W_{PiN} (see table 3.1) are presented and explained based on the previous section 3.4.1. Figure 3.18 depicts the blocking characteristics of both types of diodes taken from wafer 1 at room temperature.

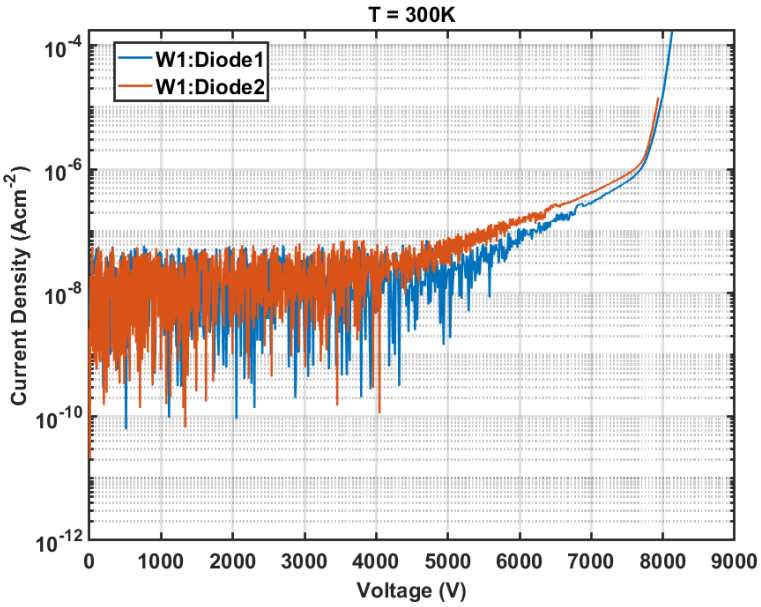

Figure 3.18: Leakage current and quasi-static electrical breakdown of Diode 1 (W_S/W_{PiN} = 3/1.5) and Diode 2 (W_S/W_{PiN} = 2/1.5) from Wafer 1 (6.5 kV) at room temperature.

The projected blocking capability of 6.5 kV could be verified for both diodes. The increase of the leakage currents starting at around 4.0 kV is a clear sign for rising electric fields below the Schottky contact supporting an increase in the field emission of charge carriers over the Schottky barrier. The steep increase of the electric current densities for blocking voltages larger than 7.5 kV indicates a charge carrier multiplication by impact ionization that finally ends in a static avalanche. The measurements were aborted before the electric power dissipation inside of the device has a destructive effect. Thus, all measurements could be verified reproducibly. Although both diodes exhibit different geometrical properties, their blocking characteristics are very similar, with Diode 1 showing a slightly lower level of leakage currents. Due to the larger PiN-area (see section 3.1.2) Diode 2 was expected have the lower leakage currents and the better blocking capability. Nevertheless, all measurements on diodes from wafer 1 at room temperature led to

similar or even higher leakage currents for diodes of the type 2. This behavior can be referred to the more complex process technology that can lead to weaknesses in the grid of p-island. The diodes of type 2 show wider variance in the leakage current level as compared to the diodes of type 1. This is an indication that the process technology is less reliable for the smaller ratio of W_S/W_{PiN}.
Figure 3.19 illustrates an equivalent comparison for two sample-diodes from wafer 2. The targeted blocking capability of 10.0 kV could be verified. The leakage current level of all diodes of type 2 was lower compared to all diodes of type 1 investigated. This result is expected with regard to the larger PiN-area of Diode 2 and shows that the processing of the p-grids is more reliable compared to wafer 1. The increasing leakage current level above 9.0 kV is only visible for Diode 1. Therefore, only Diode 1 exhibits a noticeable amount of field emission whereas the Schottky-contact of Diode 2 is shielded over the entire reverse voltage range. In the next section, this investigation is extended to higher temperatures.

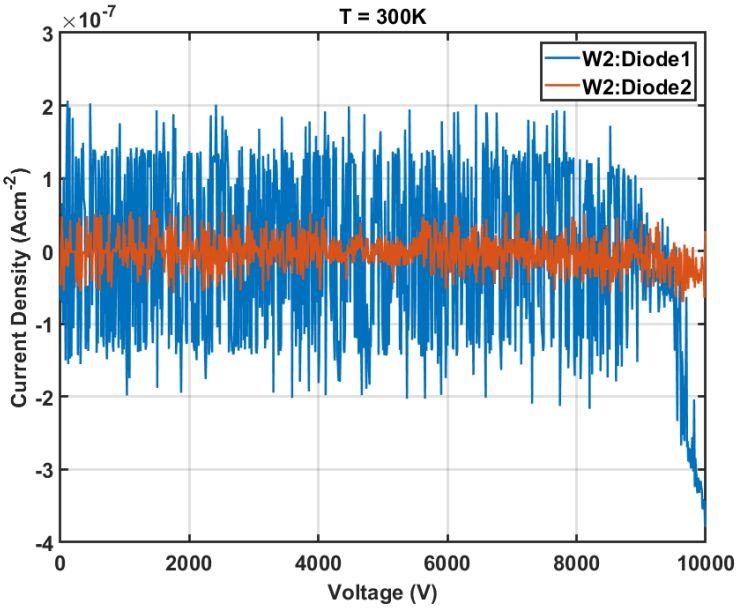

Figure 3.19: Leakage current and quasi-static breakdown of Diode 1 (W_S/W_{PiN} = 3/1.5) and Diode 2 (W_S/W_{PiN} = 2/1.5) from Wafer 2 (10.0 kV) at room temperature.

Blocking Characteristics at High Temperatures

This section covers a comparison of leakage currents and blocking capabilities of two geometrical different diodes from wafer 2 in a temperature range of 300 K to 773 K. Wafer 2 was chosen as it exhibits significantly less variation in the measured data of the blocking characteristics compared to wafer 1. Therefore, it is assumed that the implantation of p^+-islands is more reliable for epi-layers with higher doping levels (see section 3.1.2). Figures 3.20 and 3.21 show blocking characteristics as a function of temperature for both types of diodes.

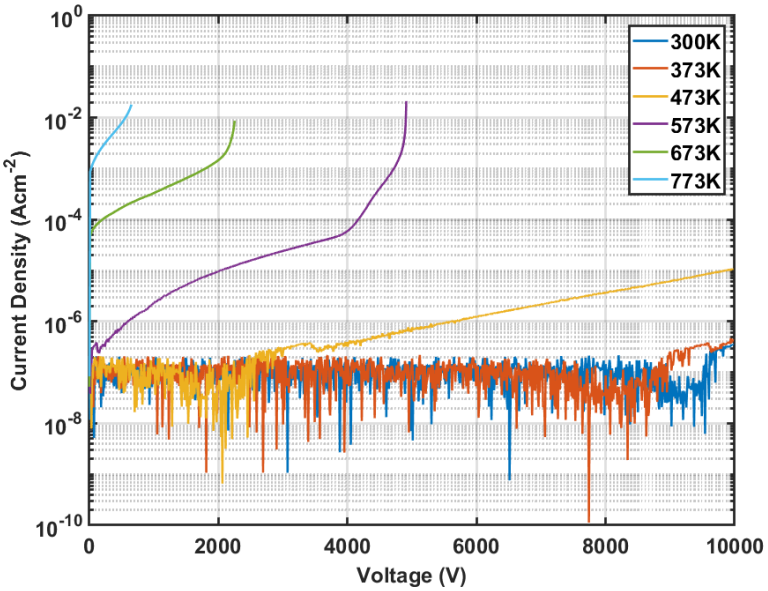

Figure 3.20: Leakage current and quasi-static breakdown of Diode 1 (W_S/W_{PiN} = 3/1.5) from Wafer 2 (10.0 kV) at high temperatures.

Both types can withstand revers voltages of 10.0 kV at 300 K and 373 K and Diode 1 also at 473 K, but with increased leakage current. In the characteristics at low temperatures the electric current densities are sufficiently low to exhibit small influences of the average noise level of the vacuum chamber described in section 2.5, that have less impact at higher leakage current levels. The increase of the leakage currents due to field emission of carriers is visible in all characteristics of Diode 1 and the reverse voltage necessary to enable the charge transport across the Schottky barrier is lowered with increasing temperatures. Diode 2 shows only a small contribution of field emission below 573 K. The blocking characteristic at 473 K features a static avalanche that led to an increase of the leakage currents of two orders of magnitude. From the low level of field emission it can be concluded, that the electric field below the Schottky contact is not the trigger for the static

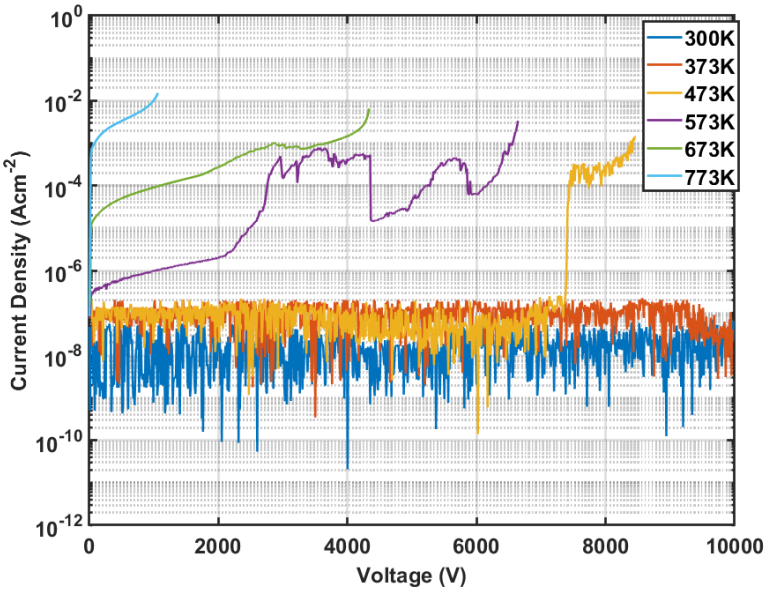

Figure 3.21: Leakage current and quasi-static breakdown of Diode 2 (W_S/W_{PiN} = 2/1.5) from Wafer 2 (10.0 kV) at high temperatures.

avalanche. Therefore, the carrier multiplication has to be activated at a defect in the internal structure of Diode 2, which may be created during the fabrication process. All characteristics that did not meet the blocking capability of 10 kV feature a steep increase in the leakage currents caused by impact ionization and the measurements were ultimately terminated due to the static avalanche in the device. Both diodes exhibit negative temperature coefficients for the breakdown voltages indicating either a positive temperature coefficient of the ionization coefficients or an ignition of the avalanche at a defect.
As the calculations in scientific literature, e.g. [1] and [3], as well as empirical studies as e.g. [29], do not suggest a positive temperature coefficient for ionization coefficients of electrons and holes, it is rather probable that the electrical breakdown is caused by a defect in the inner structure of the device (e.g. on a p-island close to the edge of the device).
The blocking capability at temperatures above 473 K is enhanced for Diode 2 compared to Diode 1 and the leakage currents are significantly lower. The characteristics for one diode of the type 2 at 573 K (purple characteristic in fig. 3.21) even shows the recovery from two static avalanches before the carrier multiplication final became too severe.
In summary, both diodes showed a good blocking capability and a low leakage current level. The leakage current as well as the field emission of charge carriers

over the Schottky-barrier are lower for Diode 2, but a weak spot inside the device is more likely. Therefore, both diodes show one side of a trade off between power loss in reverse direction and complexity in the process-technology.

3.5 Summary of the Behaviour of 4H-SiC JBS-Diodes

This chapter covers a comparison between JBS-diodes fabricated on two wafers with different blocking capability and doping of the epi-layers. The diodes of one wafer differ in the ratio of Schottky- to PiN-area (ratio of W_S/W_{PiN}), that influences the device behaviour. For each wafer and each type of measurement four test devices each from two different types of JBS-diodes were investigated and the conclusion described in this section are based on experiences gained throughout the measurements.
The different gaps between buried p^+-islands provide different additional bipolar conduction in forward direction and exhibit a strong influence on the knee-voltages of the diodes. A larger PiN-area causes a bipolar activation already at lower temperatures (473 K) and reduced electric power dissipation, but also results in a more pronounced pinch-off of the Schottky-contact. Measurements with surge current pulses emphasize the expected differences between larger and smaller PiN-areas. The diodes with an increased bipolar contribution to the total current dissipate less electric power before they reach the maximum pulse current and showed bipolar activation at lower turning-voltages. Nevertheless, the self-heating of the 'increasing bipolar' devices is intensified, thus the risk of thermal runaway during applications is increased, too.
Under reverse bias, the shielding of the Schottky contacts is improved for diodes with lower ratio of W_S/W_{PiN}, resulting in lower leakage currents. Both types of diodes fulfill the targeted blocking capability at low temperatures (<473 K) and the temperature coefficient of the breakdown voltage is negative. Although the larger PiN-area reduces the field emission, the more complex process technology causes more internal defects, which may serve as trigger points for an uncontrollable multiplication of charge carriers by impact ionization. The stability of the measurement results is better for wafer 2 indicating that a higher epi-doping is more reliable in the processing.
In summary, this chapter discussed the differences in the electrical behaviour of JBS-test-diodes with different blocking capabilities and geometrical structures. It is important to note, that all results gained are based on the measurements of a comparatively low number of devices available. The conclusions made in this chapter are adopted from the theoretical knowledge about JBS-, PiN- and Schottky-diodes, but their general validity still needs to be verified by a statistic generated with a higher number of investigated devices. Nevertheless, the investigations in this work showed that both geometric variations cause variations in the electric behavior of JBS-diodes (e.g. conductance, leakage currents or knee-voltages), that can be favored for certain applications. Therefore, both variations are good alternatives to the conventional Schottky and PiN-diodes and can be used in a wide field of applications.

Chapter 4

Behaviour of 4H-SiC PiN-diodes under extreme conditions

After the investigations on the quasi-bipolar JBS-diodes, the first devices using only bipolar conduction, that are on the edge of series-production readiness, are PiN-diodes. PiN-diodes made of 4H-SiC show very promising features such as high breakdown voltages and high operation temperatures, but still exhibit a lot of disadvantages, that are mostly related to insufficient process technologies [1].
In this chapter, first the properties of PiN-diodes as well as two different types from two different vendors are introduced. Subsequently, the results for quasi-static low forward-current, dynamic high forward-current and quasi-static high reverse-voltage measurements are presented. On the basis of the quasi-static measurements in forward direction an empirical equation describing the influences of different carbon-vacancies on the SRH-carrier lifetimes in n-type 4H-SiC is developed and tested on both types of diodes.

4.1 Structure and properties of PiN-diodes

The electrical properties of a PN-diode are determined mainly by the junction between p-doped and n-doped semiconductor materials. Under forward bias, the PN-junction enables bipolar conduction (electrons from the n-doped and holes from the p-doped area) which results in a high conductivity of the device. Under negative bias, the PN-junction forms a space charge region (depletion region) that expands with increasing voltage. The depletion region shields the anode-contact from high electric fields and prevents the flow of electric currents in blocking direction [1]. A PiN-diode is a special variant of a PN-diode that enables higher blocking fields by including a drift layer with intrinsic doping and large expansion. This intrinsic region (n^--area) of a PiN-diode exhibits only a low doping concentration

and is therefore capable of taking most of the electric field in blocking direction. Figure 4.1 shows a one-dimensional cut through an exemplary PiN-diode-structure that shows the netto-doping along the lateral extension.

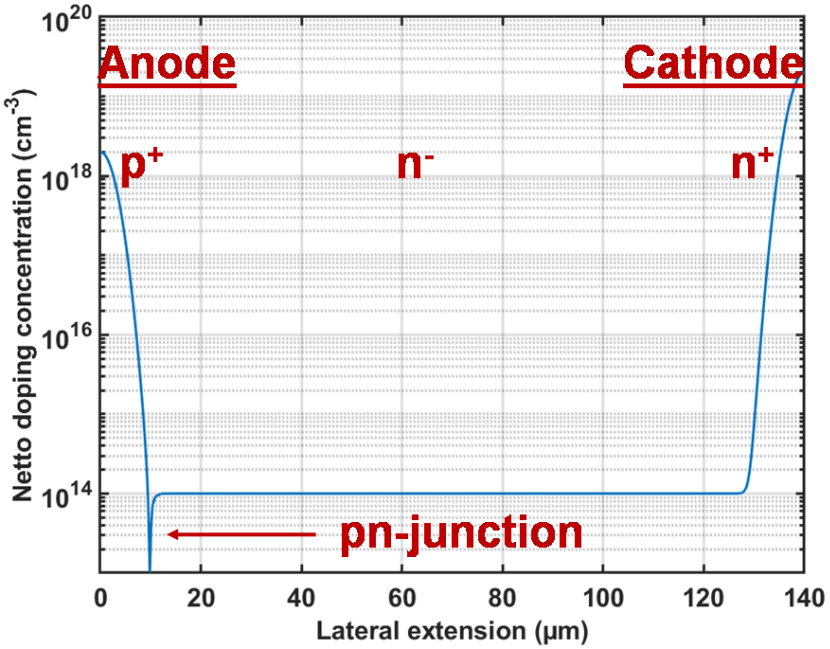

Figure 4.1: Doping-Profile and 2-D-strucutre of an exemplary n-Type PiN-diode. The anode-contact is located at the p^+-area and the cathode contact at the n^+-area.

If the PN-junction is under reverse bias, an electric field develops at the p^+n^--junction that blocks the electric current, whereby the peak of the field is situated directly at the junction [1]. The low doping concentration between the high doped areas results in a larger penetration depth of the electric field in the intrinsic area which significantly increases the breakdown voltage [3]. A larger expansion of the intrinsic area enables a higher blocking voltage, but also decreases the electric conductivity in forward conduction. A n-type PiN-diode exhibits a low n-doped intrinsic area and a p-type a low p-doped intrinsic area.
The PiN-diodes introduced in this chapter are all made of 4H-SiC and are n-type PiN-diodes. Due to the physical properties of 4H-SiC (e.g. the large band gap (see appendix A.1)) the blocking capabilities of these diodes are significantly higher compared to Si-pendants with comparable geometric features. Nevertheless, the properties that enhance the breakdown voltage and decrease the leakage currents in blocking direction, increase also the knee-voltage and decrease the electric conductivity in forward direction (see section 3.4.1).

The next section introduces the two different types of PiN-diodes investigated with special focus on the expected blocking capabilities and nominal currents.

4.2 Test devices

Within the framework of this PhD-thesis two different types of 4H-SiC PiN-Diodes were available from two different industrial partners. All devices were developed within the framework of the SPEED project funded by the European Commission. The SPEED project was a collaboration of several industrial and academic partners that took place from January 2014 to December 2018. Its goal was the improvement of process technology, packaging, characterization and real applications for SiC semiconductor devices [32]. This section introduces the different PiN-diodes and summarizes the information about the process-technology and the technical specifications available in advance to the measurements.

4.2.1 **Ascatron** 10.0 kV

The PiN-diodes from Ascatron AB Stockholm (Sweden) exhibit a blocking capability of 10.0 kV and a nominal current of 2 A. Figure 4.2 shows a schematic cross-section of the device taken from [33]. It consists of a highly n-doped substrate, a buffer-layer followed by a low n-doped epi-layer, two different p^+-doped areas and a highly p^+-doped on top, that was implanted to improve the transition between the semiconductor and the contact-metallization.

The diode exhibits three layers of passivation (LTO, ThO+LTO and Polyimide) and is separated in three different zones (a, b, c). The edge-terminations (zone-in and zone-out in figure 4.2) play a crucial role for achievement of a high blocking capability. As the nominal current of 2 A is comparatively low, the diodes are not suitable for measurements with high pulsed currents and are therefore only investigated during quasi-static measurements (LC and HV). In [33] only the doping profile and the geometric structure of zone a is explained in detail which limits the TCAD simulations to the forward direction (see section 4.3.4).

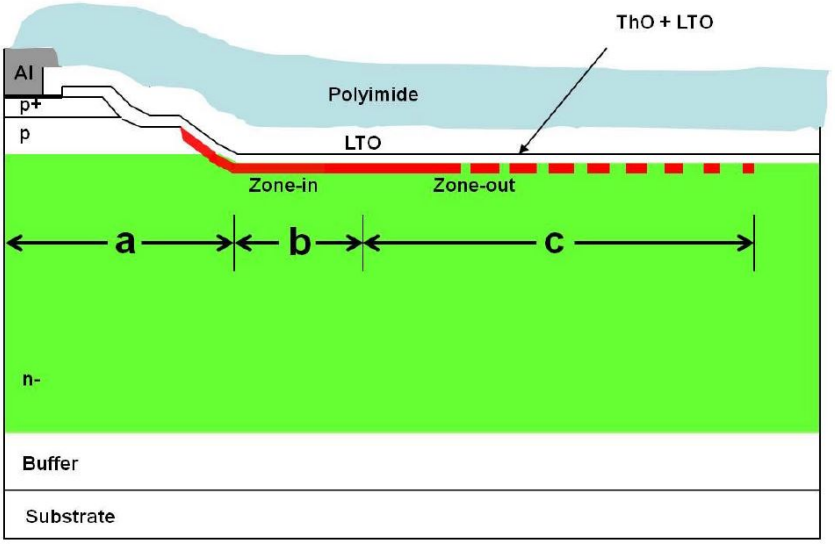

Figure 4.2: Schematic 2-D-structure of the 10.0 kV PiN diodes from Ascatron AB Stockholm [33].

4.2.2 **ABB** 5.0 kV

The 5.0 kV PiN-diodes from ABB Zurich (Swiss) exhibit an epitaxially grown drift-layer and a substrate. The p^+-area above the epi-layer shown in figure 4.3 is epitaxially grown, the layer above is formed via ion-implantation.

The nominal current of this diode is 15 A, which makes it suitable for pulsed high current measurement. As seen in figure 4.3 the complete doping profile of the central part of the diode is known but without detailed information on the edge-terminations. Therefore, the processing of the diode (without edge terminations) can be simulated and a good virtual representation for TCAD simulations in forward direction can be created with the tools of Sentaurus (see appendix A). Moreover, the ABB 5.0 kV PiN-diodes exhibit a similar structure of the epitaxially grown and implanted p^+-areas as the Ascatron 10.0 kV diodes, which enables the possibility of a qualitative comparison between both types of diodes.
In the next section the results of measurements and simulations in forward conduction are introduced and analyzed.

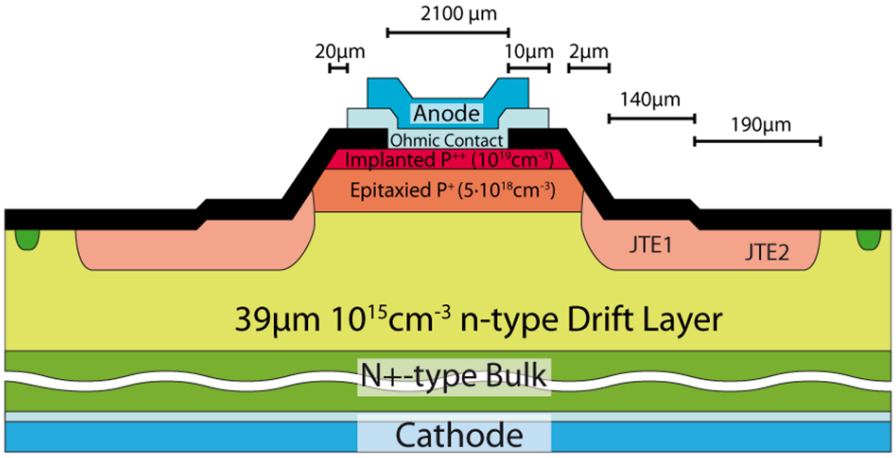

Figure 4.3: Schematic 2-D-structure of the 5.0 kV PiN diodes from ABB Zurich [34].

4.3 Low-current forward conduction

In this section the behaviour of the two different 4H-SiC PiN-diodes (Ascatron 10.0 kV and ABB 5.0 kV) under low forward currents (< 0.1 A) in a temperature range between 300 K and 773 K is analyzed. First, the temperature dependence of the electric conductivity on a conducting PN-junction as well as the electric field on a depleted PN-junction are discussed theoretically in section 4.3.1. Next, the measurement results at room-temperature are compared to each other with regard to the analysis of the differences between PiN-diodes with different voltage-classes and process technologies. This analysis is extended to higher temperatures in the next part. As last part of this section the diode introduced in section 4.2.1 is implemented into a virtual experiment and the adoptions of measurements and simulations for temperatures between 300 K and 773 K are presented.

4.3.1 Preliminary theoretical considerations

The forward conduction of a PiN-diode is composed of two states. First, the diode is only conducting a very low amount of current until the 'knee-voltage' is reached and second the bipolar conduction is triggered which leads to an exponential

increase of the device current. This section discusses the temperature dependence of the knee-voltage and the electric conductivity during bipolar conduction.

Temperature dependence of diffusion voltage

To understand the temperature dependence of the quasi-static forward conduction it is necessary to investigate the non-conducting state first.
A PN-junction without an external voltage source exhibits an electric field caused by the diffusion of electrons into the p-doped area and holes into n-doped area. This charge separation leads to an electric field that eventually stops the diffusion. In this steady state a diffusion voltage V_D can be calculated via integration over the lateral expansion of the electric field. The current flow through a PN-junction can only be achieved if the diffusion voltage is compensated by an externally applied voltage. The theoretical deduction of this physical quantity results in equation (4.1) and can be found in [1].

$$V_D(T) = \frac{k_B \cdot T}{q} \cdot \ln \frac{N_A \cdot N_D}{{n_i}^2} \tag{4.1}$$

The linear and positive temperature dependence in the first part of equation (4.1) has less influence on the temperature dependency of V_D than the temperature dependence of ${n_i}^2$. With the knowledge of the temperature dependencies from equations (A.3), (A.4) and (A.5) it can be concluded that the diffusion voltage V_D is decreasing with increasing temperatures. Therefore, the PiN-diodes start the electric conduction at lower external voltages (knee-voltages) if the temperature rises.

Temperature dependence of the electric conductivity

After the estimation of the temperature dependence of knee-voltages it is also important to understand the temperature-dependent influences on the electric conductivity of the devices during bipolar conduction. From equation (A.24) we know that the temperature dependence of the electric conductivity σ is depending on the temperature dependencies of the carrier concentrations n and p as well as the carrier mobilities μ_n and μ_p. Equation (A.11) shows that the carrier mobilities of electrons and holes are decreasing with rising temperatures, which causes a decrease of the electric conductivity.
On the other hand, the intrinsic carrier density n_i is increasing with increasing temperatures (see equation (A.3)) and the SRH-recombination rate R_{SRH} is decreasing due to increasing carrier lifetimes τ_n and τ_p. This together with the effect of the recombination rate on the two balance equations (equations (A.25) and (A.26)) leads to increasing carrier concentrations with rising temperatures.

The two effects described are contradictory to each other and their correct physical modeling is crucial to understand the behaviour of 4H-SiC PiN-diodes at high temperatures. In [1] an empirical research of the temperature dependence of the forward characteristics of Si PiN-diodes is presented. The results of a diode with implanted recombination centers (comparable to Ascatron 10.0 kV and ABB 5.0 kV) showed that for electric currents below 50 A the temperature dependence of the drift voltage is negative and the temperature dependence of the electric conductivity is positive. Above roughly 60 A an intersection of the characteristics measured at high temperatures (150 C) and low temperatures (−25 C) is visible. This indicates, that for PiN-diodes the increase of carrier concentrations is dominant over the reduction of carrier mobility until a certain electric current is reached [1]. In consequence of that, for the quasi-static measurement under low electric powers it can be assumed, that the electric conductivity of the PiN-diodes is increasing with increasing temperatures.

4.3.2 Forward characteristics at room-temperature

The diodes introduced in section 4.2 exhibit different blocking voltages, different current ratings and were processed in different fabrication environments. The lateral expansions of the epi-layers are -among others- a measure for the maximum electric field that can be taken by the diode in blocking direction. Therefore, the diode with the highest blocking capability (Ascatron 10.0 kV) features the larges epi-layer. Nevertheless, the diodes are designed with different technical specifications and therefore, exhibit differences in the doping profiles, electrically active chip areas and in the edge terminations. From [33], and [34] only limited information on the edge terminations of the respective diodes is available. Therefore, the influence of the edge-terminations on the electric resistance of the devices in forward conduction can only be estimated.
Figure 4.4 shows a comparison of the forward characteristics at room temperature. To compare the technical specifications of the diodes, the absolute electric current was chosen for this plot instead of the area-related electric current density. The knee-voltages of Ascatron 10.0 kV is comparable to ABB 5.0 kV but the electric conductivity is slightly lower which can be explained by the different lateral expansions of the epi-layers of both devices.

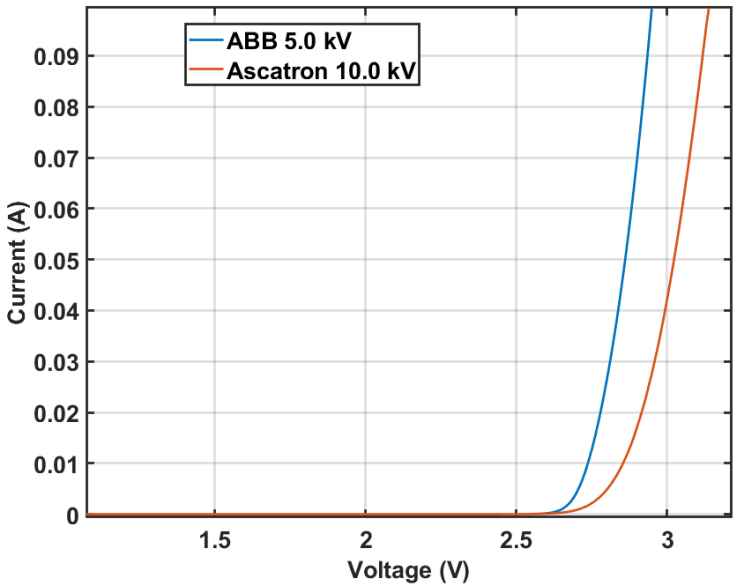

Figure 4.4: Quasi-static forward characteristics of the two PiN-diodes at 300 K.

In the next section the temperature dependencies of the forward characteristics of the diodes are analyzed. As a direct comparison is not reasonable due to the

various differences in topology and processing, the overall temperature dependent behaviour is compared qualitatively.

4.3.3 Temperature dependent forward characteristics

In this section the temperature dependencies of the quasi-static forward-characteristics of selected sample diodes from Ascatron 10.0 kV and ABB 5.0 kV are investigated. Both diodes were investigated in a temperature range between 300 K and 773 K.

ABB 5.0 kV

Figure 4.5 shows the forward characteristics of one sample-diode of the ABB 5.0 kV PiN-diodes and figure 4.6 the temperature dependence of the device voltage at an electric current density of 100 mAcm^{-2}. It is intended to compare the power consumption and therefore also the electric conductivity above the knee-voltage of the different devices.

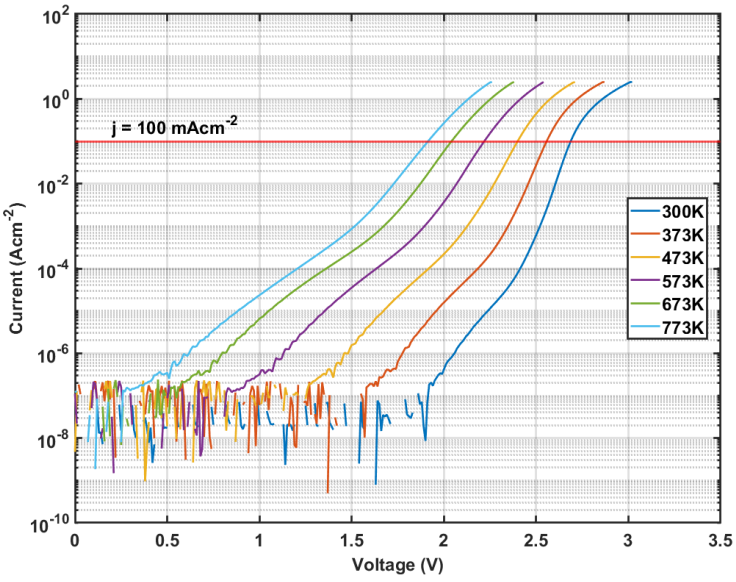

Figure 4.5: Quasi-static forward characteristics of an ABB 5.0 kV PiN-diode for temperatures between 300 K and 773 K. The red line marks an electric current density of 100 mAcm^{-2}.

All characteristics in figure 4.5 show very low sub-threshold currents and a strong non-linear increase of the electric current density after the applied voltage

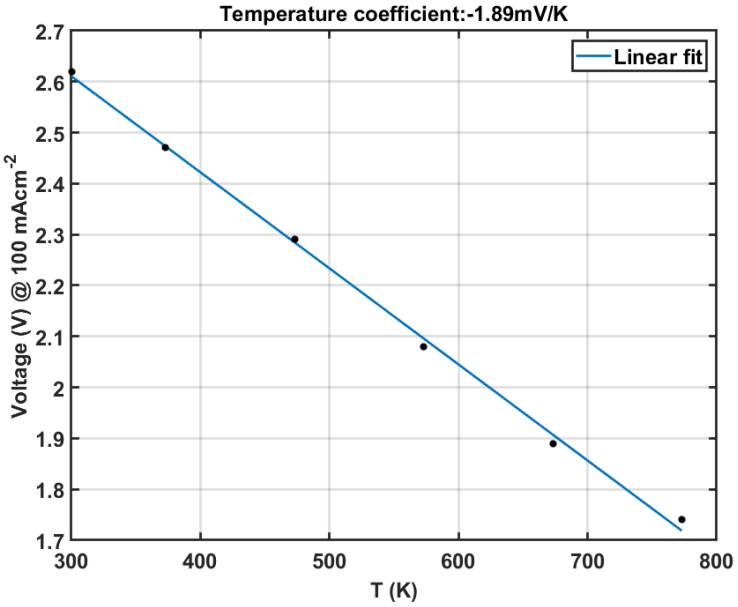

Figure 4.6: Temperature-coefficient β_{ABB} of the device voltage at an electric current density of 100 mAcm^{-2} of an ABB 5.0 kV PiN-diode for temperatures between 300 K and 773 K.

exceeds a certain level. The negative temperature dependence of the knee-voltages can be seen in figure 4.6. The increase of the electric conductivity with increasing temperatures can be analyzed from the measurement-data and is also clearly visible in the slopes of the graphs for electric current densities above 100 mAcm^{-2}. The temperature dependence of the forward conduction under low electric powers for ABB 5.0 kV PiN-diodes shows the same tendency throughout all temperatures and moreover, fit to the discussion on the temperature dependencies of knee-voltage and electric conductivity from section 4.3.1. The low current measurements were performed on two different devices, the mean value of the temperature coefficients of the knee-voltage was $\beta_{ABB} = -1.71$ mV/K with a standard deviation of 0.25 mV/K.

Ascatron 10.0 kV

Figures 4.7 and 4.8 show the forward characteristics of one exemplary Ascatron 10.0 kV PiN-diode as well as the temperature dependence of the device voltage at a low electric current density of 100 mAcm^{-2}.

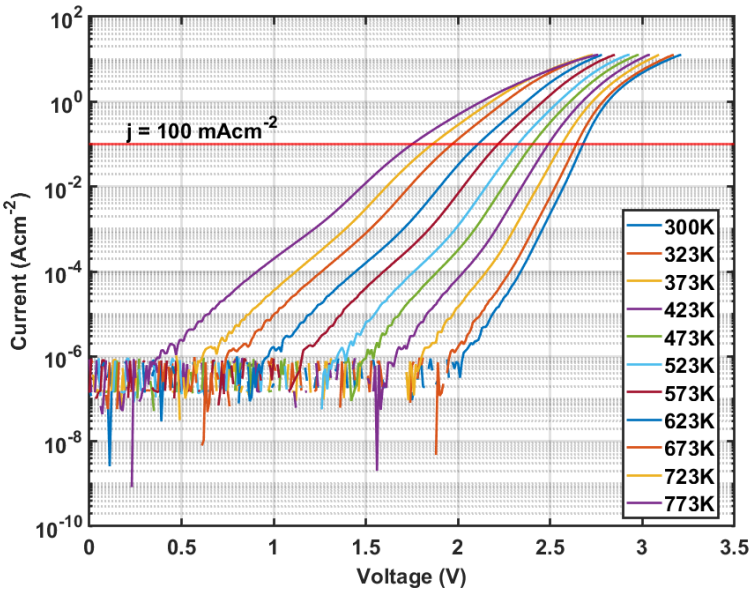

Figure 4.7: Quasi-static forward characteristics of an Ascatron 10.0 kV PiN-diode for temperatures between 300 K and 773 K. The red line marks an electric current density of 100 mAcm^{-2}.

The low current measurements were performed on five different devices, the mean value of the temperature coefficients of the knee-voltage at an electric current density of 100 mAcm^{-2} was $\beta_{Asc} = -1.94$ mV/K with a standard deviation of 0.18 mV/K. The Ascatron 10.0 kV PiN-diode also exhibits a negative temperature dependence of the knee-voltage, but the absolute value of the coefficient is slightly higher than for the ABB 5.0 kV PiN-diode. In figure 4.7 it is visible that the electric conductivity of the 10.0 kV PiN-diode is decreasing during bipolar conducting at high temperatures (above 600 K). This is contradictory to the results from the ABB 5.0 kV PiN-diode (see previous section) that did not exhibit a decreasing electric conductivity at in the investigated temperature range. Moreover, the simulated characteristics contained in 4.2 suggest a positive temperature coefficient of the electric conductivity for current densities below 200 Acm^{-2} due to the dominating influence of carrier lifetimes on the devices conductivity.
The main difference between the Ascatron 10.0 kV PiN-diode and the ABB 5.0 kV

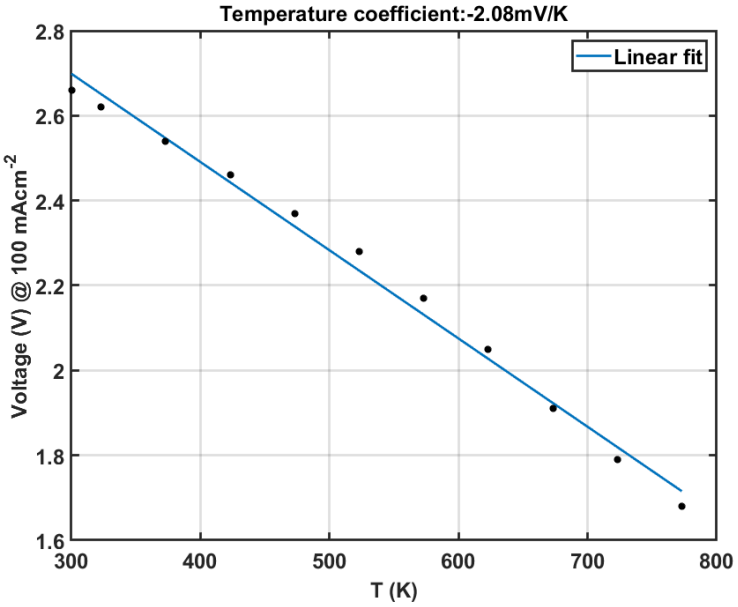

Figure 4.8: Temperature-coefficients β_{Asc} of the device voltage at an electric current density of 100 mAcm^{-2} of an Ascatron 10.0 kV PiN-diode for temperatures between 300 K and 773 K.

PiN-diode is the size of the epi-layer, but due to the fabrication in different laboratories the parameter of the process-technologies may vary, too. These differences in the processing can lead to different types of defects in the crystal and can therefore cause a different device behaviour.

In the last part of the analysis the measurement results of the quasi-static forward characteristics of the Ascatron 10.0 kV PiN-diodes are compared to TCAD simulations of the virtual device. As the ABB 5.0 kV PiN-diodes are capable of operating under a quasi-static conduction current of 15.0 A they are suited for dynamic measurements with high pulsed currents. Therefore, the comparison of measured data and TCAD simulations (see section 4.4.2) takes into account the low- and the high-power behaviour of the diodes.

4.3.4 Investigation on the quasi-static TCAD simulations of Ascatron 10.0 kV PiN-diodes

In this section the quasi-static forward characteristics simulated with the virtual representation of an Ascatron 10.0 kV PiN-diode are compared and adjusted to the measurement results of the real devices. The virtual device was designed on the basis of the process-information contained in [33]. The exact designs of the edge terminations are not available in [33]. Therefore, they have been approximated by a combination of a JTE and 60 floating field rings surrounding the anode contact. The influence of the edge terminations on the forward characteristic is an increase in the resistivity of the device due to the spreading of the bipolar current perpendicular to the direction of the flow. One major difference between virtual and real device are the ohmic contacts. In the simulation they are assumed to be ideal ohmic contacts with perfect conductivity and infinite recombination rates for charge carriers. This is necessary to assure a good numeric stability of the simulation, but the real contact may differ from the ideal one which has to be considered for further research.
The physical models for the TCAD-simulations are summarized in appendix A. The majority of the parameters for the model equations for 4H-SiC contained in [45] are still identical to the parameters for Si. For several models the parameter sets were updated for 4H-SiC if reasonable parameters based on recent, empirical investigations were available (see appendix A).
The adjustment of measurement and simulation was published in [35] and is introduced in the following.

Adjustment of quasi-static measurement to TCAD-simulations

As starting point for the investigations, the measured and simulated characteristics of the diodes at room temperature were adjusted by the adoption of the parameter $\tau_{i,max}$ for the SRH carrier lifetimes in the simulations (see appendix A.4.2). The parameter variations on $\tau_{i,max}$ enabled a good adjustment for all investigated 10.0 kV PiN-diodes at room temperature. It is important to note, that $\tau_{i,max}$ was chosen individually for the different parts of the device (e.g. substrate, drift-layer and p-doped areas). The highest value for $\tau_{i,max}$ is in the low-doped drift-layer and in the high p-doped layers below the anode contact the emitter recombination leads to a comparatively low $\tau_{i,max}$. As the dominating influence on the device characteristics is caused by the SRH carrier lifetimes in the large drift-layer, this approach was chosen to allow an investigation independent of the influence of the p- and n-emitter and without the need of the definition of one effective carrier lifetime for the whole device.
Figure 4.9 shows the comparison between the quasi-static measurement and the adjusted TCAD-simulation of one exemplary diode at 300 K. Due to the ideal

ohmic contacts and the perfect processing of the structure in the virtual experiment, the simulation is not able to reproduce the sub-threshold currents but exhibits a good agreement with the measurement results above the knee-voltage (high injection state).

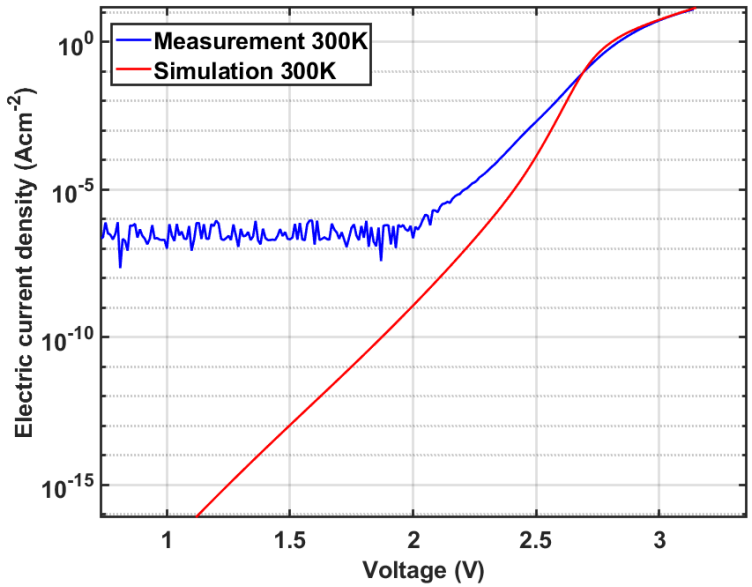

Figure 4.9: Comparison between quasi-static measurement and TCAD simulation of one exemplary 10.0 kV PiN-diode at 300 K.

After adjusting simulation and measurement by adopting the SRH-model parameter at room temperature this procedure was extended to higher temperatures. However, it is not possible to obtain a sufficient agreement of measured and simulated data at higher temperatures with the existing set of parameters of the physical models introduced in appendix A. In order to identify the weaknesses of the physical models used so far in our TCAD simulations, a high -performance computing cluster was employed to perform a systematic analysis of the problem. Based on these simulations (i.e. quasi-static forward characteristics) an investigation on the models of carrier mobilities (A.3), Auger lifetimes (A.4.1) and SRH lifetimes (A.4.2) was performed in a wide temperature range by making a sensitivity analysis w.r.t the relevant physical parameters. Similar to the adjustment at room temperature, the by far predominating influence on the threshold voltage and the electric conductivity of the diodes originates from the SRH lifetimes within the intrinsic region. There, the degradation of the carrier lifetimes due to high dopant concentrations is irrelevant and equation (A.22) has no significant influence. This allows the investigation of the temperature-dependent increase of the carrier life-

times by adjusting the temperature dependence of the SRH model in equation (A.23). As first step, the temperature dependence of equation (A.23) was switched off by setting the factor 2.55 in the exponent to 0. The next step was carried out by finding the best constant value for the carrier lifetimes of electrons and holes at the respective temperature condition with reference to the measured data. This led to the adjustment of the characteristics obtained by measurements and simulations for temperatures between 300 K and 773 K and an unexpected temperature dependence of SRH-carrier lifetimes, that will be discussed in the subsequent sections.
Fig. 4.10 shows the results of the "manual" adjustment for the selected example-diode at 573 K and 773 K. The simulations reproduce well the conductivity of the diode in the high injection state, but show discrepancies in the knee-voltages, which increase with temperature. Varying the parameters of the physical models in reasonable ranges could not diminish the discrepancies in the threshold voltages between measurement and simulation. After comparing this results to the research on ohmic contacts of 4H-SiC-devices published in e.g. [36], it can be concluded that the discrepancies in the knee-voltages are effected by the non-ideal ohmic contacts in the real device. The non-ideal ohmic contacts can cause an energetic barrier of uncertain magnitude that obstructs the injection of holes into the drift-zone [36]. Therefore, the TCAD-simulations exhibit differences in the development of the high injection state compared to the real device behaviour.

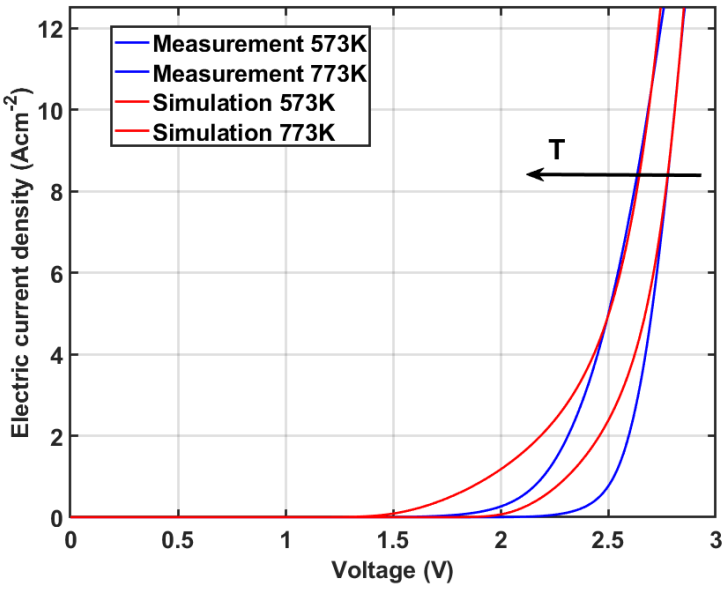

Figure 4.10: Comparison between quasi-static measurement and TCAD simulation of one exemplary 10.0 kV PiN-diode at 573 K and 773 K.

The adjustment of measurement and simulation described above was performed with 5 different Ascatron 10.0 kV PiN-diodes from two different wafers. The results show a good agreement of measurements and simulations -despite the ohmic contacts- from room temperature to 773 K during bipolar conduction.

Temperature dependence of SRH carrier lifetimes

The procedure of adjusting measurement results and simulated data described in section 4.3.4 was performed with 3 different diodes from one wafer (W1) and 2 diodes from a second wafer (W2), produced in another batch. The diodes of both wafers exhibit the same technical specifications, but were not processed simultaneously. Several process steps as e.g. annealing after implantation of Al-atoms and the additional implantation of C-atoms were performed differently by the manufacturer to investigate their influences on the device behaviour. The exact difference in the process technology are not contained in [33] but it can be expected that diodes from different wavers differ e.g. in the defect densities of their epi-layers. Moreover, the diodes investigated where taken from different locations on the wafer (e. g. center and rim), so that it is likely that the defects caused by the process-technology have a different manifestation on the diodes of one wafer.

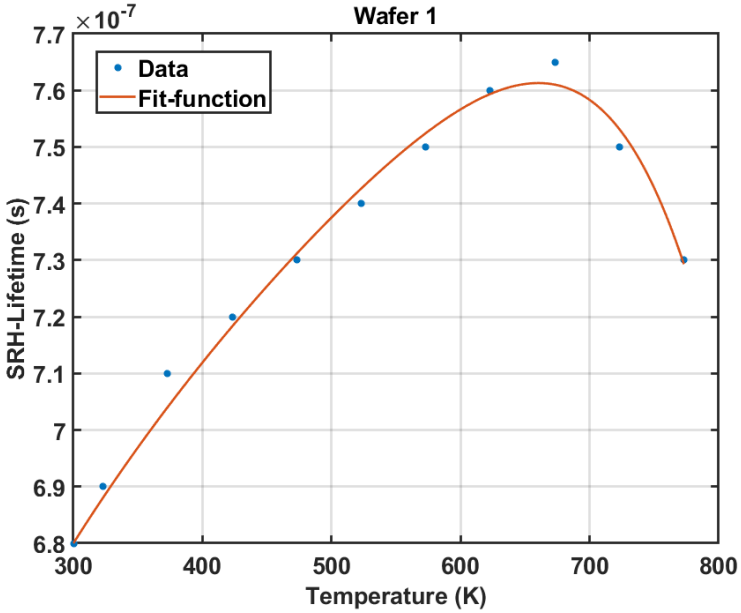

Figure 4.11: Temperature dependence of the SRH carrier-lifetimes of one exemplary diode from W1.

With this inherent difference it is not useful to compare the diodes quantitatively. Instead, the qualitative behavior of the temperature dependence of the SRH-carrier lifetimes was compared on the basis of the results from the adjustment of measured data to TCAD-simulations.
Figures 4.11 and 4.12 show the temperature dependence of the SRH-lifetimes for one example diode of each wafer. Both diodes show increasing carrier lifetimes

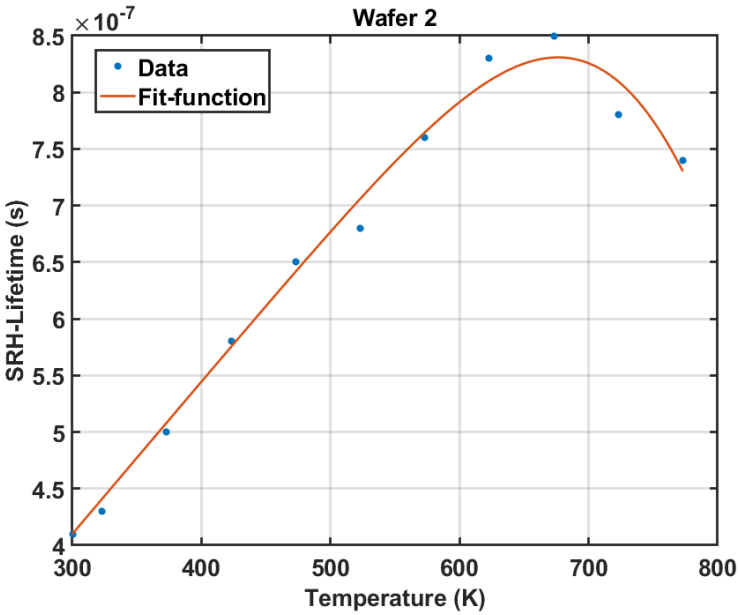

Figure 4.12: Temperature dependence of the SRH carrier-lifetimes of one exemplary diode from W2.

at rising temperature until a certain turning-temperature is reached and the carrier lifetime is decreasing again. All diodes investigated indicate a decrease of the carrier lifetimes above a certain temperature. The increase of the carrier lifetime with reference to its value at room temperature is stronger for diodes from W2. The mean value for the turning-temperatures of all diodes investigated was 651 K with a standard deviation of 28 K. In the next sections, first the physical interpretation of this behavior as well as its theoretical description are discussed and afterwards an empirically deduced fit-function and the interpretations of its parameters are introduced.

Influence of a single type of recombination-center on the SRH-recombination rate

In this section, the results shown above are discussed on the basis of the theoretical modeling of the SRH-recombination rate. Therefore, the theoretical description of the capturing and emitting of charge carriers by recombination-centers in a semiconductor crystal is introduced phenomenologically on the basis of the theoretical research of Karl Böer developed for Si-crystals in [37].
Recombination centers are either impurity atoms included in the semiconductor crystal, that originate from a different material than the crystal or vacancies in the lattice. The impurity atoms can either be implanted intentionally to change the

electrical properties of the semiconductor material (doping) or be created unintentionally during the process-steps. The carbon or silicon vacancies are part of every 4H-SiC epilayer and exhibit different concentrations depending on the process-technology [38]. An electrically active vacancy is also treated like an impurity atom with regard to the SRH-recombination and therefore all further explanations in this section are referred to impurity atoms for simplicity. In [37] the impact on the SRH-recombination caused by one species of impurity is described by its capture- and emission-rate of charge carriers. An electrically active impurity is a Coulomb-attractive center, that exhibits a capture coefficient defined over its capture cross-section and the average velocity of the charge carriers. Together with the emission rate of the impurity atom it can be estimated how a species of impurities impacts the recombination of charge carriers in the crystal. The temperature dependence of this behavior can be deduced from the temperature dependence of the capture cross-section. The capture cross-section of one type of impurity is shrinking with rising temperature and therefore, the recombination rate is decreasing and as consequence the carrier lifetimes are increasing (see equation (A.19)). An explanation of this behavior can be given by the increasing level of vibrations in the crystal with rising temperature [37]. In consequence, the SRH-carrier lifetimes of a Si-crystal should increase with temperature if only one type of impurity exists in the crystal. Since this theoretical model has a well-founded physical background, it is valid for a 4H-SiC crystal, too.
This means, that the decrease of the SRH carrier lifetimes visible at higher temperatures is not caused by one single type of impurities. As 4H-SiC crystals are not as perfect as Si crystals, so far, they tend to have a higher amount of impurities. Moreover, due to the large band gap of 4H-SiC the deep-level impurities exhibit a large energetic gap to the band-edges. Therefore, not every impurity is electrically active at room temperature. For deep-level defects the capturing and emitting of charge carriers only starts above a certain activation energy, which can e.g. be reached by heating up the crystal.
In summary, the temperature dependence of the SRH-lifetimes shown in figures 4.11 and 4.12 cannot be explained by only a single type of impurity. The decrease of the carrier-lifetimes at higher temperatures is a clear indicator for at least one additional recombination-center that gets electrically active at higher temperatures. In the next section a special type of carbon vacancy is discussed and identified as possible candidate for this lifetime-reduction.

Discussion on the influence of carbon vacancies on carrier lifetimes

The last section showed, that the 10.0 kV PiN-diodes investigated exhibit more than one type of recombination-center in their epi-layers. As the process-technology for 4H-SiC power semiconductor devices is not as advanced as for the Si-pendants, it is likely that these recombination centers are caused during a process-step.
From publications regarding the carrier lifetimes in 4H-SiC epi-layers as e.g. [38] and [39] it is known that the 4H-SiC crystal can exhibit vacancies. These vacancies can either be silicon- or carbon-vacancies that are also able to act as recombination-centers. If a type of vacancy gets electrically active, it can influence the recombination rates of charge carriers and therefore, the device behavior. Moreover, the known electrically active vacancies exhibit either a donor- or acceptor-nature and influence only the lifetimes of positively or negatively charged carriers [40, 41].
With regard to the 10.0 kV PiN-diodes investigated, TCAD-simulations showed that the major influence on the device behavior originates from the majority carriers in the epi-layer. This is reasonable as the decreasing electric conductivity is only visible in the state of high-injection. Therefore, if the decrease of the SRH-carrier-lifetimes is caused by a type of vacancy, it has to interact mainly with electrons and the conduction band.
With the measurements of the DLTS-spectra (deep level transient spectroscopy) of n-type 4H-SiC materials two lifetime-limiting deep level centers $Z_{1/2}$ (E_C-0.65 eV) and $EH_{6/7}$ (E_C-1.55 eV)) have been reported [40, 41]. Both are carbon-vacancies with different activation energies, that influence the SRH-lifetimes of electrons. Figure 4.13 shows the DLTS-signals of a 4H-SiC epi-layer [38]. The activation of the two carbon-vacancies is clearly visible and can be influenced by annealing and irradiation. The best candidates for the decreasing SRH carrier lifetime at higher temperatures are the $EH_{6/7}$ centers, because they exhibit a large capture cross-section and are activated at temperatures above 600 K [40, 41].

As the $EH_{6/7}$-centers are located deeper in the band, they exhibit a higher activation energy compared to the $Z_{1/2}$-centers. This means, that their influence on the lifetimes of electrons is increased with rising temperatures. This coincides well with the reduced slope of the τ-over-T plots (figures 4.11 and 4.12) for temperatures above 600 K due to the electrical activation of the $EH_{6/7}$-centers and the decrease of the SRH carrier lifetime for temperatures above 673 K due to the higher number of active $EH_{6/7}$ centers and their growing influence on the recombination rate in the crystal.
To investigate the deep-level impurities in the epi-layers, DLTS-measurements of the Ascatron 10.0 kV PiN-diodes could show the concentrations as well as the activation energies of the $EH_{6/7}$ carbon-vacancies. As DLTS-data was not available within the framework of this study, the relevant parameters for the $EH_{6/7}$-centers i.e. the concentrations, the capture cross-sections and the activation energies where

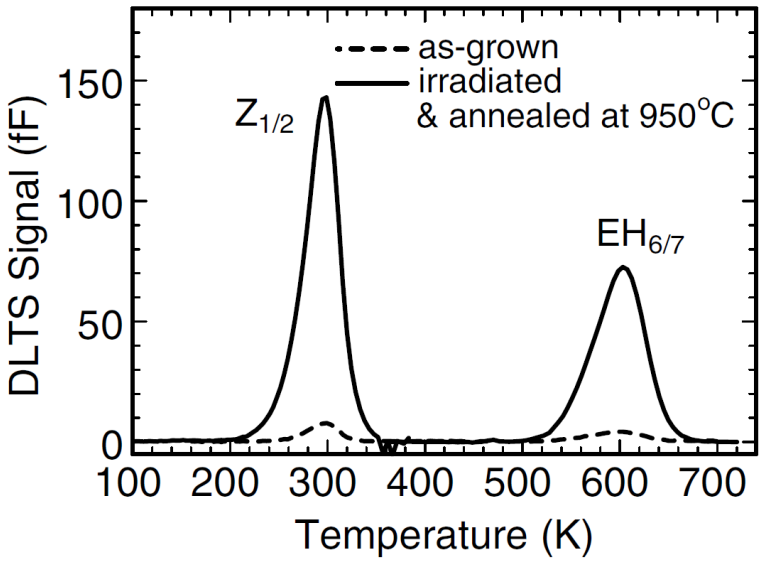

Figure 4.13: DLTS-signals of an n-type 4H-SiC epi-layer. The carbon vacancies $Z_{1/2}$ and $EH_{6/7}$ show strong signals at different activation temperatures that can be reduced by annealing and irradiation [38].

estimated on the basis of literature values taken from [38], [40] and [41]. This information under consideration of the model for incomplete ionization (see section A.2.3) allows an estimation of the density of active $EH_{6/7}$-centers $N_{tot}(T)$ under the assumption, that $EH_{6/7}$-centers act as donors. With the capture cross-section and the total number of active $EH_{6/7}$-centers it is possible to calculate the SRH-lifetimes for electrons with this impurity [1]. By using Mathiessen's rule the influences on the SRH-lifetimes originating from the doping materials and the $EH_{6/7}$-centers can be combined and therefore an analytical estimation of the temperature dependence of SRH-lifetimes could be made.
This was tested for three different concentrations and capture cross-sections for $EH_{6/7}$-centers, but the results deviate from the data obtained by the adjustment of TCAD-simulations and the measured characteristics. As consequence of this, the concentrations of impurities and carbon vacancies in the Ascatron 10.0 kV diodes are not comparable to the epi-layers investigated in [38], [40] and [41]. Therefore, this analytical approach - without DLTS-data - is not conducive to describe the temperature dependence of the SRH-lifetimes.
Nevertheless, to describe the recorded decrease of the SRH-lifetimes on the basis of a set of parameters, that give information on the overall quality of the epi-layer, an empirically deduced equation discussed in the following was developed. The

goal is not to give a theoretical description of the influence of carbon vacancies but to provide parameters that could give feedback to a process technology engineer.

Theoretical description of the influence of defects on the temperature dependence of SRH-lifetimes

In this section the fit-function contained in figures 4.11 and 4.12 is introduced and interpretations of its parameters are given. Note, that the model parameters of the fit-function are not related to a deduction based on field theory, rather than to an empirical description of process related influences on the carrier lifetimes. The concentrations of carbon vacancies in n-4H-SiC is strongly dependent on the annealing after the growth of the epi-layer and the irradiation with C-atomes [38]. Wafers 1 and 2 deviate in this crucial process steps and therefore a deviation of the concentrations of carbon vacancies is expected. As $Z_{1/2}$- and $EH_{6/7}$-centers are know to exhibit the dominant influences on carrier lifetimes they need to be addressed with different parameters in an empirical description. Nevertheless, it is necessary to also consider possible additional vacancies with activation temperatures between RT and 600 K.
Equation (4.2) shows the mathematical description developed to relate the decrease of SRH carrier-lifetimes with increasing temperatures to the concentrations of carbon vacancies and as consequence of the process technology. The equation uses the three parameters T_{coeff}, α_τ and β_τ, that are determined by a certain procedure that will be introduced in the following. Their interpretations will be discussed on the basis of possible vacancies of n-type 4H-SiC epi-layers.

$$\frac{\tau_n(T)}{\tau_n(300\,K)} = \left(\frac{T}{300\,K}\right)^{T_{coeff}} \cdot \exp\left[-\alpha_\tau\left(\frac{T}{300\,K} - 1\right)^{\beta_\tau}\right] \tag{4.2}$$

As first step, the SRH-lifetime at room temperature ($\tau_n(300\,K)$) influenced by defects like basal-plane dislocations (BPDs), stacking faults and vacancies active at low temperatures (dominated by $Z_{1/2}$) is determined. The diodes from both wafers differ in the SRH-lifetimes at room temperature. The values for $\tau_n(300\,K)$ range for W1 between 5.8×10^{-7} s and 7.4×10^{-7} s and for W2 between 3.3×10^{-7} s and 4.1×10^{-7} s. This means, that the concentration of active defects is higher for the diodes from W2 at room temperature. One possible explanation for these differences are the concentrations of active $Z_{1/2}$-centers in the epi-layers.

The first term on the right side of equation (4.2) describes the temperature dependence of the SRH-lifetimes at low temperatures. It is a measure for the amount of additional $Z_{1/2}$-centers activated with rising temperatures until they are fully activated at roughly 400 K. Figure 4.14 shows the influence of a variation of T_{coeff} on the temperature dependence of SRH-lifetimes of one exemplary

diode from W2. For diodes from W1 the values for T_{coeff} range only between 0.16 and 0.36 whereas all diodes from W2 exhibit parameter values larger than 1. This indicates, that the majority of $Z_{1/2}$-centers was already activated at RT in the epi-layers of the diodes from W2. In contrast, for the diodes from W1 the concentration of active $Z_{1/2}$-centers is still strongly increasing with rising temperatures.

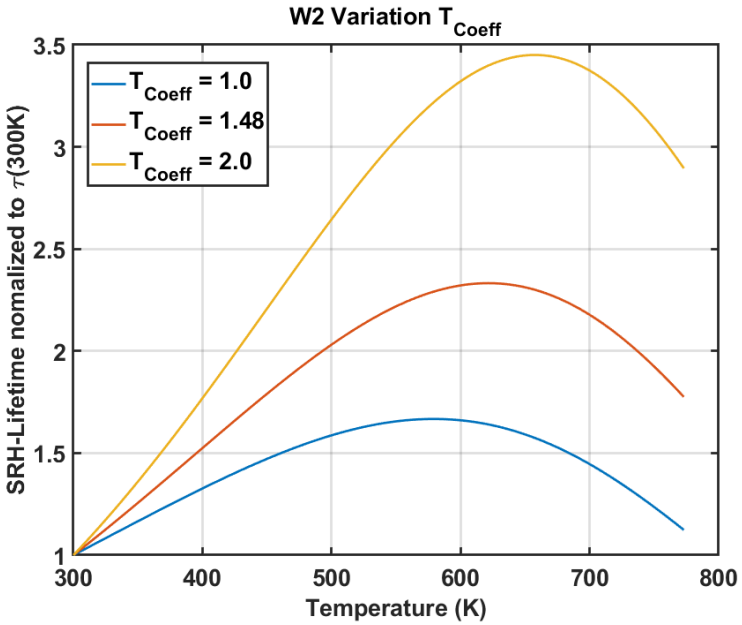

Figure 4.14: Variation of the parameter T_{coeff} in equation (4.2). A higher T_{coeff} leads to a stronger increase of the carrier lifetimes in the low temperature regime and is an indicator for the activation of additional $Z_{1/2}$-centers for temperatures below 400 K.

After T_{coeff} is determined the value of the next parameter α_τ can be approximated via the slope of the linear part of the τ-over-T plot. Figure 4.15 shows the influence of a variation of α_τ for the diode from W2. The SRH-lifetimes for diodes from W1 are higher at room-temperature, but increase to a lower amount with increasing temperatures. This is an indicator for additional defects as e.g. the X-centers described in [42], that get electrical active at temperatures below 600 K. These defects lead to a reduced increase of the SRH-lifetimes, but their influence is not strong enough to change the sign of the slope of the τ-over-T plot. The electrical activation of the $EH_{6/7}$-centers starting at roughly 600 K imposes the influence of the other centers and causes the decrease of the lifetimes. The values for α_τ are ranging from 1.33×10^{-3} to 1.61×10^{-2} for W1 and from 1.13×10^{-1} to 1.86×10^{-1} for W2. The parameter values for α_τ suggest that W1 exhibits a higher

concentration of defects as e.g. X-centers in the epi-layer that get electrically active at temperatures between 400 K and 600 K. For diodes from W1 the parameter values for α_τ exhibit a strong variation, that could be explained by the different positions of the diodes on the wafers. Devices close to the wafer edges tend to have a higher defect density and in consequence a lower value for α_τ.

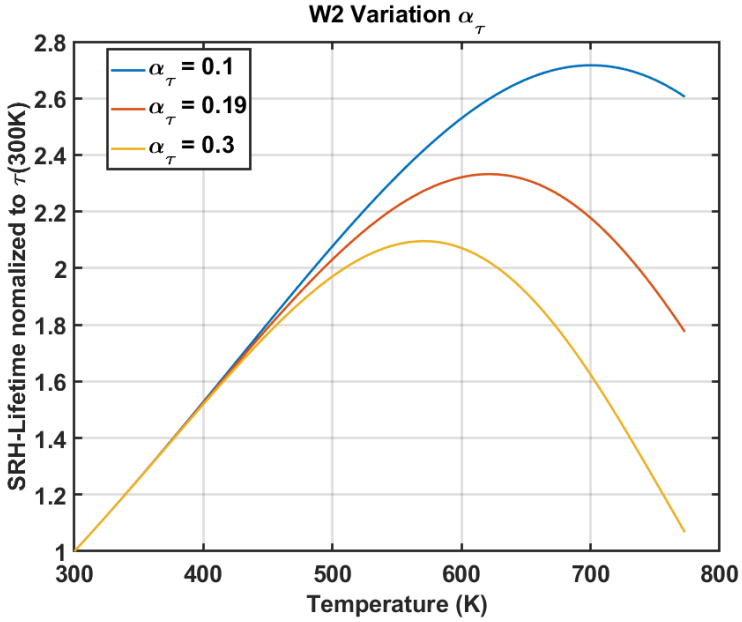

Figure 4.15: Variation of the parameter α_τ in equation (4.2). A higher value for α_τ lowers the turning-temperature and the maximum value for the SRH-lifetimes.

The differences in the parameters T_{coeff} and α_τ between the diodes from both wafers show, that the wafers exhibit different concentrations of the $Z_{1/2}$-centers and the defects in the temperature range between 300 K and 600 K. Despite these significant differences, the turning-temperatures as well as the turning-lifetimes are comparable. This indicates that this behavior is caused by the same type of defect, the $EH_{6/7}$ carbon vacancy, that gets active above a certain activation temperature. The slight differences between the turning-temperatures and the turning-lifetimes can be explained by different concentrations of the $EH_{6/7}$-centers. The parameter β_τ is an indicator for the concentration of the $EH_{6/7}$-centers electrically activated at temperatures above 600 K.
Figure 4.16 shows the influence of a variation of β_τ for the diode from W2.

The parameter β_τ defines the curvature of the turn in the τ-over-T plot. A high value leads to a more narrow curve and therefore to a stronger decrease of the SRH-lifetimes with rising temperatures. The diodes from W1 ($5.01 < \beta_\tau <$

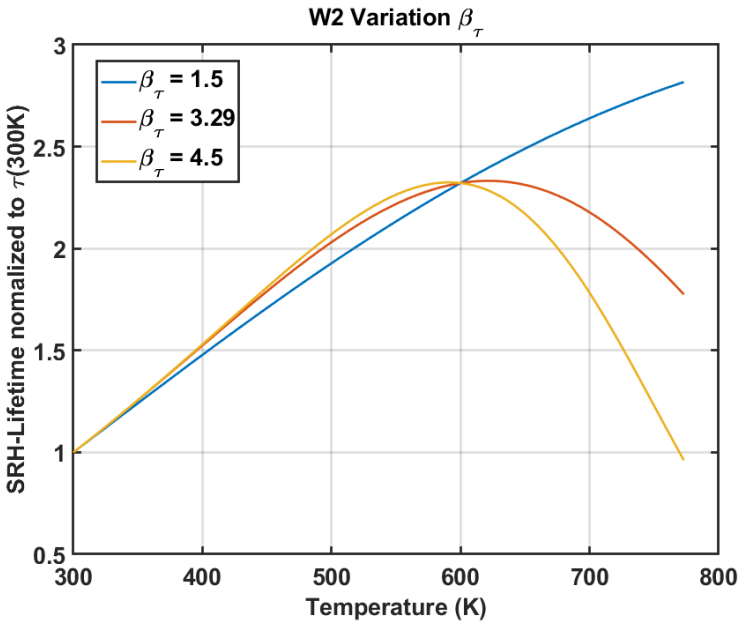

Figure 4.16: Variation of the parameter β_τ in equation (4.2). A higher value for β_τ indicates a higher concentration of $EH_{6/7}$-centers.

9.51) exhibit a higher curvature than their counterparts from W2 ($3.29 < \beta_\tau < 3.34$) and again a stronger variation in the parameter values. This suggests that the concentration of $EH_{6/7}$-centers is higher on diodes from W1 and varies at different positions on the wafer. The parameter values for diodes from W2 exhibit a very small spread and are overall lower. Nevertheless, they are also high enough to cause a decrease in the τ-over-T plot and so the diodes from both wavers show a negative temperature dependence os SRH-lifetimes.
Table 4.1 summarizes the parameter values for all diodes investigated.

-	T_{coeff}	α_τ	β_τ
W1:Diode 1	0.18	1.61×10^{-2}	5.01
W1:Diode 2	0.16	2.82×10^{-3}	7.43
W1:Diode 3	0.36	1.33×10^{-3}	9.51
W2:Diode 1	1.48	1.86×10^{-1}	3.29
W2:Diode 2	1.15	1.13×10^{-1}	3.34

Table 4.1: Parameter values for equation (4.2) for all diodes investigated from W1 and W2.

This section showed a procedure to model the behavior of 4H-SiC PiN-diodes at high temperatures. First, the parameter T_{coeff} can be estimated at low tempera-

tures after $\tau_n(300\,K)$ is found. Second, the parameter α_τ is determined by the slope of the linear part in the τ-over-T plot and third, the curvature of the graph is related to β_τ.
Equation (4.2) depicts a phenomenological description of the device behaviour at high temperatures without knowledge of the exact defect-levels from DLTS-measurements. A detailed analysis of all defects and physical description based on thermodynamics will give a more complete picture of the device, but the analysis is more complex and requires certain equipment.
Equation (4.2) was developed to allow estimations on the inner structure of the device and the parameters should give information on the pros and cons of certain process steps. If a diode should be mainly operated at RT the concentrations of $Z_{1/2}$-centers has to be monitored closely whereas at higher operating temperatures the activation of $EH_{6/7}$-centers needs to be considered.
For the Ascatron 10.0 kV PiN-diodes it can be concluded, that both wafers exhibit different concentrations and different activation energies of their defects. The differences between the wafers are most likely caused by different process-parameters and the difference between the diodes of one wafer are caused by the positions of the diodes on the wafer.
It is important to note, that the number of devices investigated in the framework of this thesis is not high enough to prove the general validity of equation (4.2). Especially the wide spread of the parameters α_τ for diodes from W1 needs to be investigated with a higher number of test devices. Nevertheless, the parameter sets generated can serve as starting point for further invetsigations and they allow for qualitative statements on the defect densities in the epi-layers of the Ascatron 10.0 kV PiN-diodes.

In the next section, the procedure is used for the investigation of the 5.0 kV PiN-diodes from ABB Zurich.

4.4 High-current forward conduction

For the dynamic investigations of PiN-diodes under high forward currents the pulsing unit PicoLas LDP-V80 V3 in combination with two oscilloscopes capturing the signals of voltage and electric current during a pulse was used (see section 2.6.3). From the two types of diodes available only the ABB 5.0 kV PiN-diodes exhibit the capability of surviving high pulsed currents due to their nominal current of 15.0 A. The Ascatron 10.0 kV PiN-diodes feature a nominal current of 2.0 A and therefore, did not survive pulsed currents above 10.0 A.
The investigations on the ABB 5.0 kV PiN-diodes were performed similarly as for the Ascatron 10.0 kV PiN-diodes. First, the quasi-static characteristics at low electric powers were measured with the configuration described in section 2.6.1 and the results are included in section 4.3.3. Second, the pulsed measurements were carried out with the measurement set-up for fast dynamic current pulses (see section 2.6.3). The evaluation of the dynamic data led to the extraction of quasi-static characteristics as shown in figure 2.16.
For the virtual experiment the ABB 5.0 kV PiN-diode shown in figure 4.3 was created with the process-simulator SProcess. The mesh of the processed device was optimized for the device simulator SDevice and the compact model shown in figure 2.13 was integrated as lumped element circuit into the mixed-mode simulation by using Spice-models.
In the following the measurement results are discussed and the adoption of measurement and simulation will be demonstrated at an exemplary temperature of 473 K.

4.4.1 IV-characteristic extracted from dynamic pulses

Figure 4.17 shows the extracted IV-characteristics for one diode at different temperatures.

Although the ABB 5.0 kV PiN-diode showed no decreasing electric conductance with rising temperatures in the LC-measurements (see figure 4.5), it is visible at higher current densities by comparing the characteristics at 573 K and 773 K in figure 4.17. This indicates that the temperature dependence of the carrier lifetimes is dominant at low electric powers and the temperature dependence of the carrier mobility is dominant at high electric powers as it is known for Si [1].

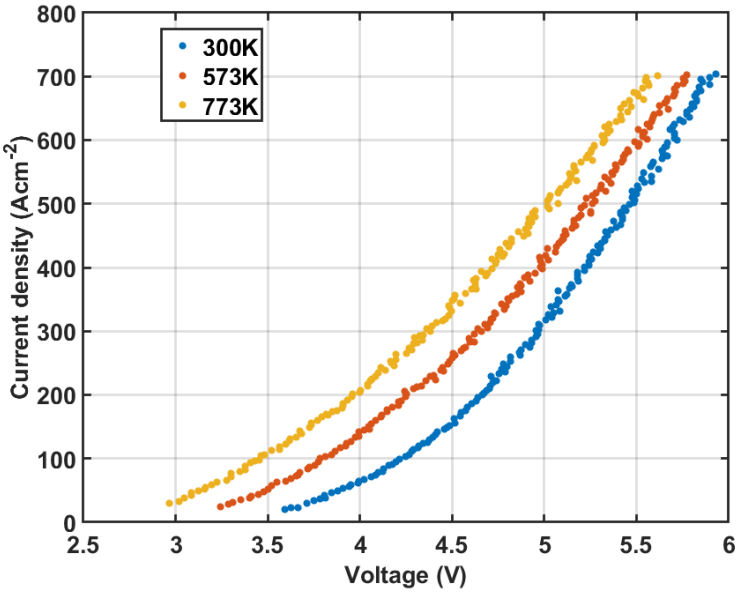

Figure 4.17: IV characteristics extracted from pulsed measurements for an ABB 5.0 kV PiN-diode at 300 K, 573 K and 773 K.

4.4.2 Results of device- and circuit simulation

The adjustment of quasi-static characteristics extracted from dynamic measurements with TCAD simulations of the virtual device was performed in two steps. First the characteristics obtained were compared to quasi-static simulations with isothermal conditions to identify the correct values for the crucial simulation parameters. As the pulse length in the dynamic measurements is short enough to avoid self-heating, the extracted IV-characteristics are comparable to an isothermal simulation. After adjusting the simulation results to the characteristic measured at room temperature by the adoption of SRH-lifetimes, another parameter study comparable to section 4.3.4 was performed. Similar to the Ascatron 10.0 kV PiN-diodes, the only way to achieve good agreement was the 'manual' adoption of the SRH-lifetimes for each temperature. Figure 4.18 shows the results for the adjustment at a temperature of 473 K.

The simulation reproduces well the conductivity of the diode during high injection, but is not possible to model the knee-voltage accurately. All simulated characteristics exhibit a slightly lower knee-voltage in comparison to the real devices. This behaviour is very similar to the one described in section 4.3.4 and therefore, it is assumed to be caused by non-ideal ohmic contacts, too.
As next step, the virtual device was integrated into the circuit of the compact model developed (see figure 2.13). To trigger the current pulse in the simulation the

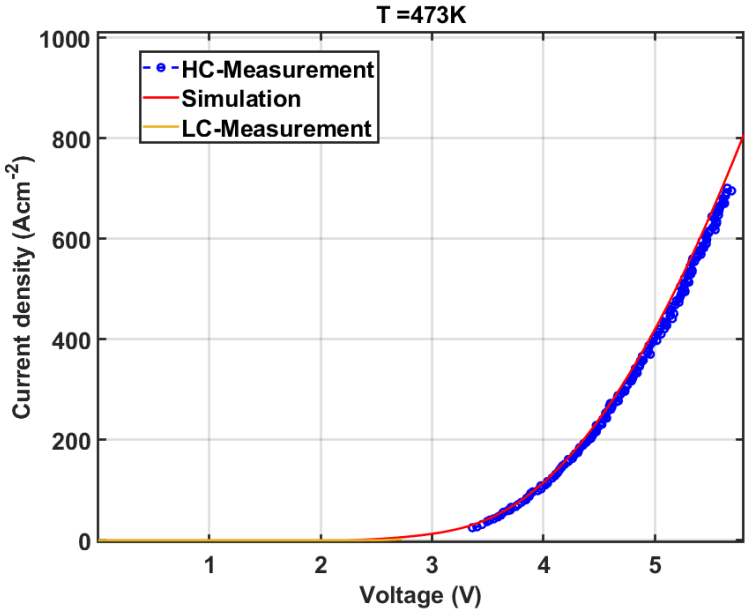

Figure 4.18: Comparison between the measured IV-characteristic (LC,HC) and a quasi-static device simulation at 473 K.

ohmic resistance of R_{MOS} is switched from 5.0 MΩ to 50.0 mΩ. In consequence, the electric capacitance C_{Par} discharges and the generated current flows through the circuit. The ABB 5.0 kV PiN-diode is simulated under thermodynamic conditions to monitor any heat generation in the device during a pulse. The parameter set for the TCAD-simulation was taken from the adoption of the quasi-static simulations to the measured data. To ensure a good comparability to the real measurements the dynamic signal of the device voltage was evaluated at C_{VProbe} and the current signal was calculated from the voltage drop on C_{Tek}.
Figures 4.19 and 4.20 show the results of dynamic measurement and the circuit simulation for one pulse at a temperature of 473 K. As mentioned in section 2.6.3 the PicoLas LDP-V80 V3 is commercial device and the parasitic elements of its circuit are unknown. As consequence, both measured dynamic signals exhibit more influence of parasitic elements than estimated in [17]. The high peak at the end of the measured signal in figure 4.19 as well as a comparatively slow rise of the measured current density in figure 4.20 are indicators for at least one additional inductance. The oscillations in figure 4.19 are caused by an additional parasitic capacitance that forms a resonant circuit with the parasitic inductance. A determination of these additional elements is not possible, but the simulation is still sufficient for the extraction of one point of a quasi-static characteristic.

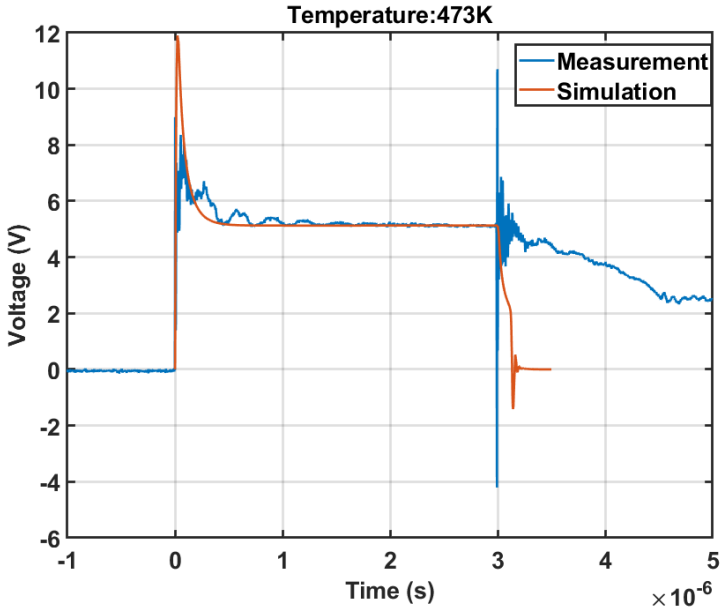

Figure 4.19: Comparison between a dynamic measurement and the simulation of the device voltage at 473 K.

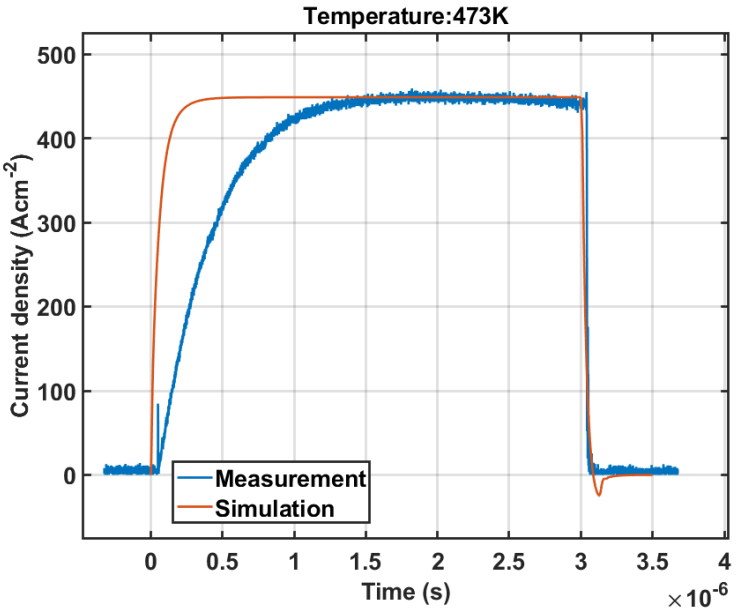

Figure 4.20: Comparison between the dynamic measurement and the simulation of the device current at 473 K.

The discrepancies in the rise times of the electric current densities of simulation and measurement as well as in the inductive peaks of the voltage signals are caused by the additional parasitic elements in the circuit of the pulsing unit, but eventually the real and the virtual device stabilize at the same levels. Figure 4.21 shows a comparison of the quasi-static IV-characteristics extracted from measured and simulated dynamic signals of voltage and electric current density. The quasi-static characteristic obtained from dynamic simulations shows a good agreement with the measured characteristic and also with the result from the quasi-static, isothermal simulation. This shows, that the self-heating during the pulsed measurements is negligible.

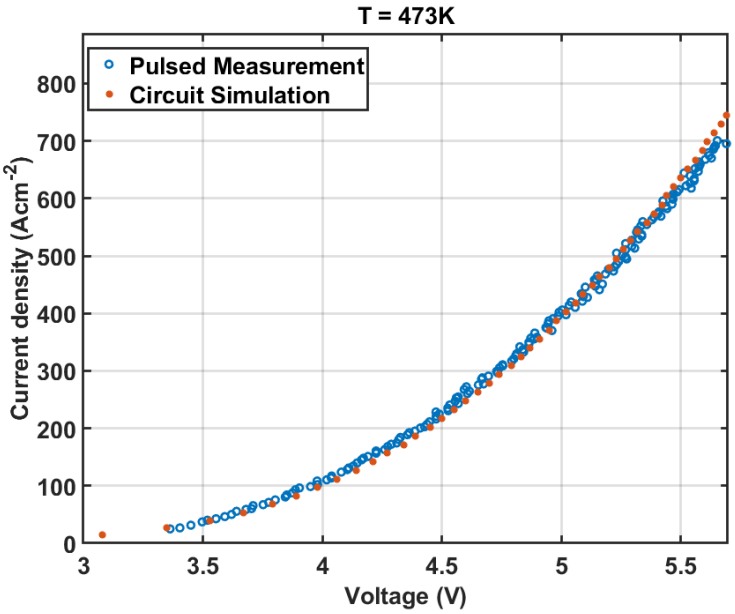

Figure 4.21: Comparison between the measured IV-characteristic (LC,HC) and a quasi-static device simulation at 473 K.

In the next section the model for the temperature dependence of the SRH carrier lifetimes introduced (equation (4.2)) in section 4.3.4 will be applied to the manually adjusted values obtained by the adoption of the quasi-static IV-characteristics of the selected ABB 5.0 kV PiN-diode.

4.4.3 Temperature dependence of SRH-lifetimes

After the 'manual' adjustment of the majority carrier lifetimes in the SRH-model, their temperature dependence can be visualized and equation (4.2) can be applied. Figure 4.22 shows the results for the SRH-lifetime of the diode investigated.

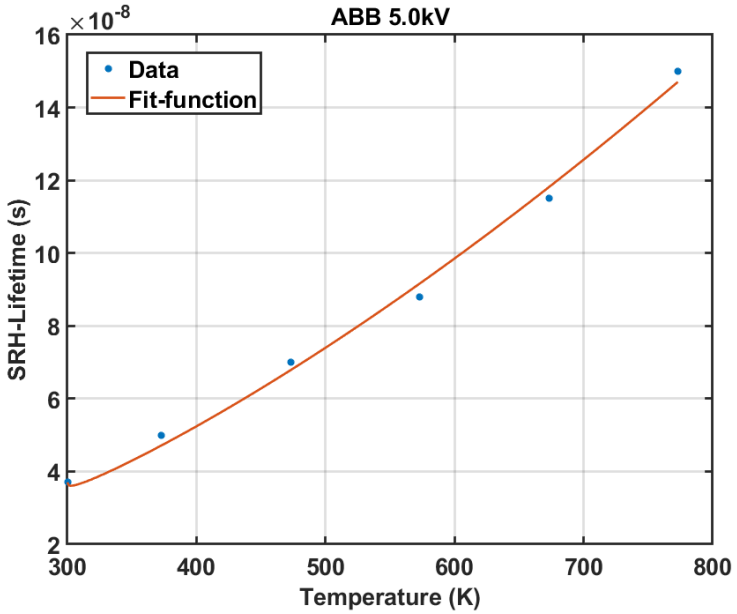

Figure 4.22: Temperature dependence of the SRH-lifetimes of majority carriers for an ABB 5.0 kV PiN-diode.

In contrast to the Ascatron 10.0 kV PiN-diodes the SRH-lifetimes of the ABB 5.0 kV PiN-diode exhibit no turning point at higher temperatures, but the SRH-lifetimes are in average one order of magnitude lower. This indicates, that the ABB 5.0 kV PiN-diode has an overall higher defect density and especially the $Z_{1/2}$-centers could have a strong influence on the carrier lifetimes. The influence of the activation of possible $EH_{6/7}$-centers is superimposed by the high concentration of $Z_{1/2}$-centers and therefore not visible in figure 4.22.
Equation (4.2) with the parameters $T_{coeff} = 1.74$, $\alpha_\tau = 0.23$ and $\beta_\tau = 0.36$ was used as the fit-function depicted in figure 4.22. The low value for β_τ shows that the concentration of $EH_{6/7}$-centers is low within the epi-layer of the diode. The values for T_{coeff} and α_τ are comparable to the parameter-values for W2 of the Ascatron 10.0 kV PiN-diodes (see table 4.1). Note, that these results are based on the measurements of the only device available for pulsed measurements in forward direction and therefore the parameter values for equation (4.2) are only indicators for the overall behaviour of the ABB 5.0 kV PiN-diodes.

The next section discusses the results of the quasi-static high-voltage measurements in blocking direction for an Ascatron 10.0 kV PiN-diode.

4.5 Blocking characteristics of a 10 kV PiN-diode

This section introduces the temperature dependent results of a selected device from the Ascatron 10.0 kV PiN-diodes (wafer 2). The measured characteristics are evaluated on the basis of the theoretical discussion in section 3.4.1.
Figure 4.23 shows the measurement results for the temperature dependent blocking characteristics of the diode selected.

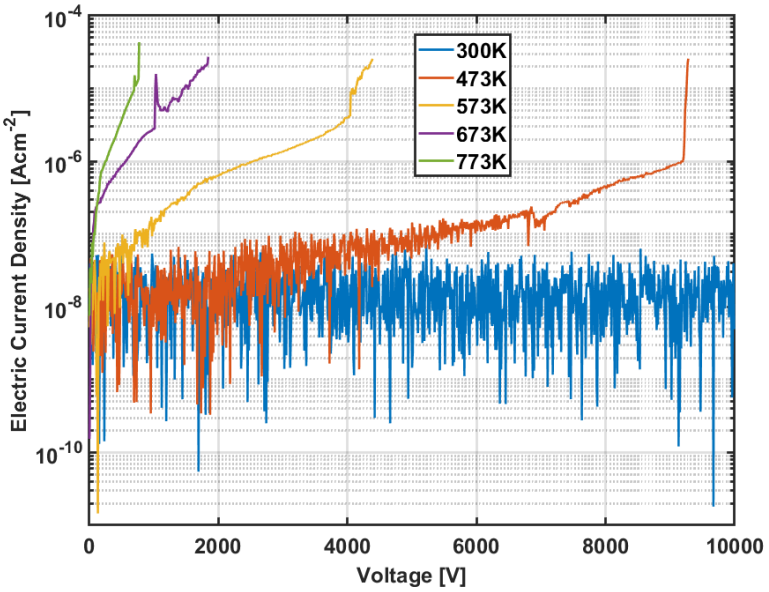

Figure 4.23: Blocking characteristics of an Ascatron 10.0 kV PiN-diode in a temperature range from RT to 773 K.

The blocking capability of 10 kV could be verified at RT and 373 K (not depicted in figure 4.23) and both characteristics showed no increase in the leakage currents. This means, that the shielding of the anode-contact by the depletion region formed by the PN-junction is sufficient to keep the leakage current constant. At temperatures of 473 K and above the leakage currents exhibit a higher level as more electrons can be lifted from the valence band to the conduction band via thermoionic emission.
In this temperature range the breakdown voltage exhibits a negative temperature coefficient. This indicates, that the static avalanches visible in figure 4.23 are ignited on weak spots in the edge terminations instead of the PN-junction as explained in section 3.4.1. It is possible that deep impurities as e.g. the aforementioned $EH_{6/7}$-centers act as centers for the generation for charge carriers.
Nevertheless, the diode stayed stable at low temperatures and exhibits low leakage

currents, which reduces the consumption of electric power in reverse direction. The combination of different edge-terminations introduced in [33] enables the high blocking capability, but the complex process technology can cause unintended geometrical weaknesses that favor field peaks.
The next section summarizes the results of the investigations on 4H-SiC PiN-diodes.

4.6 Summary of the behaviour of 4H-SiC PiN-diodes

This chapter showed that the temperature dependence of the forward conduction of a PiN-diode is strongly depending on the process-technology. High concentrations of defects like the $Z_{1/2}$-centers, that are electrically active at room-temperature can reduce the SRH-lifetimes. Defects that get electrically active between room-temperature and 600 K are harming the increase of the SRH-lifetimes with rising temperatures. Above 600 K the $EH_{6/7}$-centers get electrically active and if their concentration is high enough they can reduce the SRH-lifetime again.
To cover the different temperature dependencies of the SRH-lifetimes with an empirical description, equation (4.2) was developed and applied to the measurement results of both devices. The model parameters T_{coeff}, α_τ and β_τ are used to give a phenomenological description of the defect densities inside the epi-layer of the respective device and could help to improve the understanding of process-related defects. If a device exhibits e.g. a high concentration of $EH_{6/7}$-centers (high value of β_τ) a change in the annealing steps could lead to a reduction of these carbon vacancies.
The procedure of 'manual' adjustment of SRH-carrier lifetimes introduced to simulate the forward conduction of PiN-diodes can be applied to other 4H-SiC PiN-diodes and equation (4.2) can be used to investigate the defect densities in the intrinsic areas. With a higher number of test devices the general validity of the empirical equation could be tested and if necessary adoptions for a more detailed description of defect levels other than $Z_{1/2}$- and $EH_{6/7}$-centers could be included.
The differences between measured data and TCAD simulation were small in the state of high injection, but could not be reduced entirely due to non-ideal ohmic contacts.
The blocking capability of the diodes is enhanced by various edge terminations, that have advantages and disadvantages, that need to be considered for any specific application. The negative temperature coefficient of the breakdown voltage is an additional indicator for weak spots in the structure caused by the processing of the complex edge-terminations.
Overall, the experiences gained during the investigation of 4H-SiC PiN-diodes helped to expand the knowledge on the behavior of SiC-device at high temperatures and are one step forward into the improvement of the predictive simulation of 4H-SiC-devices under extreme conditions.

Chapter 5

Conclusions

This chapter summarizes the knowledge and experiences gained throughout all investigations in this PhD-thesis. The scientific impact of the dissertation will be presented on the basis of three main aspects: The experiences with a measurement setup for high power semiconductors, the -in part- unique measurement results at high temperatures and the development of an empirical equation to improve the understanding of the influences of certain steps during the processing of 4H-SiC devices.
Finally, several possibilities for future projects based on the research performed in this PhD-thesis are suggested.

5.1 Measurement Setup for Investigations Under Extreme Operating Conditions

The measurement setup introduced in chapter 2 exhibits several features, that are especially adopted to investigations under extreme conditions such as high temperatures and high electric power. The maximum temperature on the DUT is 1000 K as long as the recipient is under high vacuum conditions. Within the framework of this PhD-thesis the stability of measurements up to a temperature of 773 K under four different configurations has been demonstrated.
Moreover, the exact control of pressure and temperature at the location of the device sample allows reproducible measurements under high reverse voltages and high pulsed currents. The accuracy of all measurement configurations is well established and proven to be sufficient for the respective investigations.
The bonding of the test-devices and gold coated spring-loaded contacts enable very stable electrical connections to the DUT, that exhibit no degradation at high temperatures and high electric powers during all measurements.
The complete setup together with the graphical user interfaces for the controlling

the measurements and the analysis of data is unique in its properties. With the information contained in this PhD-thesis it is possible to reconstruct the setup and/or upgrade the existing measurement configurations.

5.2 Behaviour of 4H-SiC Power Devices Under Extreme Operating Conditions

This section summarizes the results obtained from the measurements on JBS- and PiN-diodes manufactured from 4H-SiC and draws conclusions and recommendations regarding advantages and disadvantages for industrial applications.

5.2.1 JBS-Diodes

The JBS-diodes investigated differ in the blocking capabilities of the devices and the ratio of Schottky- to PiN-area (W_S/W_{PiN}) (see section 3.1.2). The diodes exhibit implanted p+-areas, so that a grid of buried p+-islands is formed beneath the Schottky contact.
At low temperatures, the quasi-static forward characteristics exhibit only unipolar conduction of majority carriers and the diodes with larger PiN-areas showed higher knee-voltages due to the wider depletion regions that have to recede before the diode becomes conductive.
At temperatures of 473 K and above, the diodes possess bipolar activation with different manifestations. The diodes with the larger PiN-areas reveal the transition to bipolar conduction at lower electric powers.
The extension to dynamic surge current pulses again indicated that the smaller ratio of W_S/W_{PiN} enhances bipolar activation. The consumption of electric power is lower for a lower W_S/W_{PiN}. However, the self-heating of the device is increased. In consequence, the conductance in forward direction is enhanced for JBS-diodes with larger PiN-areas, yet the knee-voltage and the self-heating during dynamic switching both are higher, too. Therefore, the diodes with large W_S/W_{PiN} are more appropriate for dynamic applications with high stability demands, while the 'more bipolar' diodes have advantages in quasi-static applications under high temperatures.
The reverse characteristics showed, that all JBS-diodes investigated exhibit the designed blocking capability at room temperature, featuring low leakage currents. The breakdown voltage for all diodes have a negative temperature coefficient, indicating weak spots in the structure.
The wafer with a blocking capability of 6.5 kV demonstrates the enhanced blocking capability for diodes with smaller gaps between the p+-islands. The leakage

currents are lower and the probability of charge carriers tunneling through the Schottky barrier depending on the electric field intensity (field emission) is reduced. Moreover, the breakdown voltages at high temperatures are higher for the rather bipolar diodes with lower W_S/W_{PiN}.
The diodes with a blocking capability of 10.0 kV showed a similar behaviour. However, the weak spots (defects) in the device structure emerging during the processing of the more intricate edge terminations together with the higher doping of the epi-layer enhances the probability of static avalanches. The diodes with the lower ratio of W_S/W_{PiN} only exhibit lower leakage currents at temperatures above 473 K.
All diodes investigated fulfill the designated blocking capability at room temperature, but show different leakage currents and different blocking capabilities depending on their internal composition and their processing.
In summary, the higher voltage class provokes more process-related difficulties that may dominate the device behaviour. Depending on the application, a trade-off between technical specifications and the development status of the process-technology has to be made.

5.2.2 PiN-Diodes

The two different types of PiN-diodes investigated are differing in their blocking capabilities, the nominal forward currents (ABB: 15.0 A, 5.0 kV and Ascatron: 2.0 A, 10.0 kV) and the processing. The diodes are supplied from different vendors and exhibit different internal device structures (see section 4.2).
The quasi-static low current measurements support a negative temperature coefficient for the knee-voltages for both types of diodes. The temperature coefficients of both types of diodes remain constant throughout the entire investigated temperature range (300 K - 773 K). The conductance of the Ascatron 10 kV diodes is decreasing for temperatures above 600 K. This behaviour is not visible for any of the ABB 5 kV diodes and has different manifestations for all Ascatron 10 kV diodes. The temperature dependence of PiN-diodes under quasi-static low current measurements is dominated by the SRH-lifetimes of majority carriers in the intrinsic areas. In consequence, a decreasing electric conductance is an indicator for the thermal activation of unintentional impurities at elevated high temperatures.
Dynamic measurements with high pulsed currents only were possible for the ABB 5 kV diodes. The diodes are capable of carrying pulsed currents up to 35 A, yet the conductance is decreasing at higher temperatures. This indicates a significant influence of the mobilities of charge carrier, which exhibit a negative temperature coefficient at higher electric current density.
The complex edge terminations of the Ascatron diodes enables a blocking capability of 10 kV at room temperature, but causes a negative temperature coefficient

for the breakdown voltage, too. The combination of JTE and floating field rings published in [33] implies the development of weak spots in the internal structure that favor spikes in the electric field.

5.3 Temperature Dependence of SRH-lifetimes

The decreasing conductance of Ascatron 10 kV diodes at high temperatures was investigated via a sensitivity study performed with the TCAD-simulator SDevice. The evaluation of the results suggests that decreasing SRH-lifetimes of charge carriers reduce the conductance at high temperatures. The reconciliation with the basic concepts behind the SRH-model and the field theory behind it showed, that this behaviour cannot be explained with one type of impurity only. Besides, the base n-doping, an additional type of impurity has to be present in the epi-layer. Moreover, the energy for electrical activation has to be high enough, that these additional impurities only get activated at high temperatures. The best candidates for this unknown impurity are carbon vacancies known as $EH_{6/7}$-centers, that exhibit sufficient concentrations and capture cross-sections for a significant influence on the SRH recombination rates. Moreover, they become electrically active at temperatures close to 673 K and above.
To describe the influences of carbon vacancies by empirical parameters, equation (4.2) was developed and applied on the results for both types of diodes. The values of the empirical parameters should give a process engineer information on the influences of certain process steps on the concentrations of defects in the epi-layer of the device.
The procedure of manually adjusting the SRH-lifetimes led to a good agreement between measurements and simulations during the high injection state achieved in a temperature range between 300 K and 773 K. For one ABB 5 kV diode this adjustment was achieved for the dynamic measurements as well as by margin a compact model of the measurement circuit into the TCAD-simulations.
The empirical equation (4.2) could be utilized for all diodes investigated. It allows for the investigation of the influences of impurities in the epi-layer of power devices without the detailed knowledge of the DLTS-spectra of the respective layer. This investigation on the temperature dependence of SRH-lifetimes is another important step into a deeper understanding of 4H-SiC power-devices at high temperatures, but the general validity of equation (4.2) needs to be verified by a higher number of test devices.

5.4 Outlook for Future Projects

The investigations within this PhD-thesis reveal the potential of 4H-SiC power devices for applications under high temperatures. With these results, several properties as e.g. the negative temperature coefficients of breakdown voltages could be related to problems in the device processing. To investigate this in more detail, the systematic investigations of real and virtual test structures are necessary. To analyze the mechanism causing a negative temperature coefficient of breakdown voltages, test structures under reverse bias may be examined with infrared detectors to identify the trigger-points of the static avalanches by their elevated temperatures. This may help to distinguish different regions of the edge terminations, that favor electrical field peaks and to identify the critical process steps, which cause the additional impurities.
To investigate the temperature dependence of SRH-lifetimes and to examine the parameters in equation (4.2) it is necessary to manufacture several test structures with low doping concentrations. Differently processed epi-layers (e.g. with epitaxy and ion-implantation) can be used to determine the temperature dependence of SRH-lifetimes by calibrating equation (4.2). The parameter α_τ in equation (4.2) summarizes the influences of an unknown number of different impurities, that become electrically active at temperatures between roughly 400 K and 600 K. If the results obtained by the measurements and simulations of the test-structures are compared to DLTS-measurements of the respective epi-layers, the parameter α_τ may be separated into specific parameters for any type of these impurities, too.
The measurement setup introduced in this PhD-thesis can be modified and extended to continue the systematic research on the behaviour of 4H-SiC power devices under extreme operating conditions.

Appendices

Appendix A

Theoretical Basis for the TCAD Simulations of 4H-SiC Devices

The primary idea behind TCAD simulations of semiconductor devices is to model the physical properties within devices during fabrication-processes or different operation modes in applications as a function of position and time. Simulation-programs for the specification of either geometric structures or the necessary steps of the process-technology are creating a virtual representation of the device and discretize it into finite volumes.
The simulation of semiconductor devices behaviour in various applications is performed using a set of fundamental physical laws and physical models reproducing the material properties. The latter are mainly deduced from empirical results. As the computational effort for a simulation grows with the number of considered physical models, it is necessary to tailor the model set-up to the simulation-problem. This appendix summarizes the simulation tools used and explains the physical models considered for device simulations.
The TCAD tools used for all investigations within this PhD-work is 'Sentaurus' provided by Synopsys, Inc.. It contains several tools for the specification and simulation of semiconductor devices. Table A.1 summarizes all tools used for this work.

In the following subsections a theoretical framework for the simulation of 4H-SiC power-semiconductor devices during operation is introduced with a special view on the physical models used.

Program	Application
Sentaurus Process (SProcess)	Process simulation for the creation of 2 or 3 dimensional structures with electrical contacts.
Sentaurus Structure Editor (SDE)	Creation of 2 or 3 dimensional geometric structures with electrical contacts.
Sentaurus Mesh Generator (SMesh)	Specification of materials and their doping for a given boundary-file and meshing of the structure.
Sentaurus Device (SDevice)	Device simulator for quasistatic and dynamic applications. Accessibility of Hspice models for the integration of the device into a circuit.
Sentaurus Visual (SVisual)	Visualization and analysis of simulation results.

Table A.1: Simulation tools of Synopsys Inc. used in this thesis.

A.1 Differences Between Si and 4H-SiC

4H-SiC is a wide-bandgap-semiconductor and therefore, compared to Si, it exhibits quite different physical properties. Table A.2 shows a comparison of the most important physical properties of Si and 4H-SiC. The listed parameters are relevant for the device simulations in this work and the values are taken from [43].

Parameter	**Si**	**4H-SiC**
ε_r	11.7	9.66
$E_g(300\,K)$	1.12 eV	3.26 eV
$n_i(300\,K)$	$1.45 \times 10^{10}\,cm^{-3}$	$8.2 \times 10^{-9}\,cm^{-3}$
μ_n	$1400\,cm^2V^{-1}s^{-1}$	$1000\,cm^2V^{-1}s^{-1}$
μ_p	$471\,cm^2V^{-1}s^{-1}$	$115\,cm^2V^{-1}s^{-1}$
κ_L	$1.5\,Wcm^{-1}K^{-1}$	$4.5\,Wcm^{-1}K^{-1}$
E_{crit}	$0.3\,MVcm^{-1}$	$2.0\,MVcm^{-1}$

Table A.2: Comparison of physical parameters for Si and 4H-SiC relevant for the device simulation in this work [43].

The relative permittivity ε_r of both materials are comparable, but the bandgap E_g is almost three times larger for 4H-SiC compared to Si. This results in a lower intrinsic carrier density n_i (section A.2.2), lower leakage currents (section 3.4.1) and a higher critical electrical field strength E_{crit}(section 3.4.1). The mobilities of

electrons μ_n and holes μ_p are anisotropic for 4H-SiC (see section A.3) and lower as for Si which exhibits isotropic carrier mobilities. The last major difference - relevant for the device simulations in this PhD-thesis - is the thermal conductivity κ_L which is three times larger in 4H-SiC. This results in an increased thermal stability of 4H-SiC devices due to a superior heat transportation. A more detailed description of the physical parameters and their theoretical modeling will be given in the following subsections.

A.2 Charged Carrier Densities

4H-SiC possess a wider bandgap compared to Si, i.e. the energy gap between the valence-band-edge E_v and conduction-band-edge E_c is larger. Moreover, energetic levels of trap states E_t likewise may have larger energy differences with respect to the band-edges. The first property results in lower intrinsic carrier densities while the second provides an incomplete ionization of dopants in the SiC-crystal especially at room temperature. The following sections explain the empirical models for the bandgap, the intrinsic carrier densities and the incomplete ionization emphasizing their temperature dependencies.

A.2.1 Bandgap of 4H-SiC

The bandgap energy E_g is defined as the difference between the highest energy level in the valence band E_v and the lowest energy level in the conduction band E_c. It depends on the temperature as well as on the densities of dopants in the SiC-crystal. Equation (A.1) shows the empirical modeling of the temperature dependence of the bandgap as it was deduced for Si in [44]. The empirical model from [44] valid for Si, is used the simulator SDevice as well, offering a set of parameters for 4H-SiC [45], taken from [46].

$$E_g(T) = E_{g,0} + \delta E_{g,0} - \frac{\alpha_{Eg} \cdot T^2}{\beta_{Eg} + T} \tag{A.1}$$

Table A.3 summarizes the parameter values used for the TCAD-simulations.

Variable	**Value**	**Unit**
$E_{g,0}$	3.265	eV
α_{Eg}	0.010988	eVK^{-1}
β_{Eg}	32744.3	K

Table A.3: Parameter values for temperature dependent bandgap of 4H-SiC.

The parameter $\delta E_{g,0}$ refers to the physical modeling of the bandgap narrowing with increasing concentration of ionized impurities N_{tot}. The model selected from [45] was developed in [47] and is displayed in equation (A.2).

$$\Delta E_{bgn}(N_{tot}) = \delta E_{g,0} + E_1 \cdot \left[\ln(N_{tot}/N_{0,bgn}) + \sqrt{(\ln(N_{tot}/N_{0,bgn}))^2 + C_{bgn}} \right] \tag{A.2}$$

The parameters for 4H-SiC are also taken from [46] and summarized in table A.4.

Variable	**Value**	**Unit**
$\delta E_{g,0}$	0	eV
E_1	0.02	eV
$N_{0,bgn}$	1×10^{17}	cm^{-3}
C_{bgn}	0.5	1

Table A.4: Parameter values for modeling bandgap narrowing in 4H-SiC.

A.2.2 Intrinsic Densities

The intrinsic carrier density n_i specifies the concentration of free charge carriers intrinsic doped or only lightly doped semiconductor material. As shown in equation (A.3) it depends on the energy bandgap E_g, the effective density of states for electrons in the conduction band N_c, the effective density of states for holes in the valence band N_v, Boltzmann's constant k_B and the lattice temperature T [1]. Both effective densities of states are material parameters dependent on temperature. The modeling of the density of states for the respective type of charge carrier are expressed in equations (A.4) and (A.5) and are taken from [2].

$$n_i = \sqrt{N_c \cdot N_v} \cdot \exp\left(\frac{E_g}{2 \cdot k_B \cdot T}\right) \tag{A.3}$$

$$N_c(T) = 1.694\,93 \times 10^{19}\,\mathrm{cm}^{-3} \cdot \left(\frac{T}{300\,\mathrm{K}}\right)^{3/2} \tag{A.4}$$

$$N_v(T) = 6.474\,67 \times 10^{19}\,\mathrm{cm}^{-3} \cdot \left(\frac{T}{300\,\mathrm{K}}\right)^{3/2} \tag{A.5}$$

In an intrinsic semiconductor the concentrations of electrons n and holes p are equal to the intrinsic carrier density ($n = p = n_i$) to guarantee charge neutrality in the semiconductor. This leads to the law of mass action as in equation (A.6), which is as well valid for extrinsic (e. g. highly doped) semiconductors.

$$n \cdot p = {n_i}^2 \tag{A.6}$$

A.2.3 Incomplete Ionization

The bandgap of 4H-SiC is three times larger as for Si. The energy gap for a certain type of impurity (donor E_D, acceptor E_A) with reference to the center of the bandgap stays constant (with reference to T, N_A and N_D) for both materials. Therefore, the energy gap between a donor state and the conduction band edge ($\Delta E_D = E_c - E_D$) as well as the gap between an acceptor state and the valence band edge ($\Delta E_A = E_A - E_v$) are significantly larger in 4H-SiC compared to Si. The ionization of dopants in 4H-SiC require higher thermal energy compared to Si. Hence, the percentages of ionized dopants are different for both materials at a predefined temperature. The physical model describing the ratio between ionized dopants and their total number ($N_A/N_{A,0}$ or $N_D/N_{D,0}$) for SiC was introduced in [48] and is expressed in equation (A.7) for donors and equation (A.8) for acceptors.

$$N_D^+/N_{D,0} = \frac{1}{1 + g_D \cdot \frac{n}{N_c \cdot \exp\left(-\frac{\Delta E_D}{k_B \cdot T}\right)}} \text{ for } N_{D,0} < N_{D,crit} \tag{A.7}$$

$$N_A^-/N_{A,0} = \frac{1}{1 + g_A \cdot \frac{p}{N_v \cdot \exp\left(-\frac{\Delta E_A}{k_B \cdot T}\right)}} \text{ for } N_{A,0} < N_{A,crit} \tag{A.8}$$

Above critical concentrations of donors $N_{D,crit}$ and acceptors $N_{A,crit}$ respectively, the complete ionization of the dopants is assumed. Another factor, that has to be considered, is the reduction of the energy gaps ΔE_D and ΔE_A in dependence of the total concentration of electrical active dopants N_{tot}.

$$\Delta E_D = \Delta E_{D,0} - \alpha_D \cdot {N_{tot}}^{\frac{1}{3}} \tag{A.9}$$

$$\Delta E_A = \Delta E_{A,0} - \alpha_A \cdot {N_{tot}}^{\frac{1}{3}} \tag{A.10}$$

The parameter values for the dopants nitrogen (N), aluminum (Al) and boron (B) are taken from [2] and summarized in table A.5. whereby
$N_{D,crit} = N_{A,crit} = 1.0 \times 10^{22}\,cm^{-3}$ for all materials.

Variable	**N**	**Al**	**B**	**Unit**
$E_{A/D,0}0$	0.0525	0.230	0.345	eV
$\alpha_{A/D}$	3.38×10^{-8}	1.80×10^{-8}	3.10×10^{-8}	eVcm
$g_{A/D}$	2	4	4	1

Table A.5: Parameter values for modeling the incomplete ionization of dopants in 4H-SiC [2].

A.3 Mobility of Charged Carriers

The mobility of charged carriers is a measure for the electric conductivity in a material. It depends upon e.g. the lattice temperature, the concentration of electrical active dopants, the electric field and the concentrations of electrons and holes [1]. As 4H-SiC is an anisotropic crystal, the mobility along the c-axis is different in comparison to other directions. The flow of the electric current is aligned with the c-axis of the crystal for all devices investigated in this PhD-thesis. Therefore, the parameters reproduced in the following are only valid for a crystalline orientation of 4H-SiC close to the c-axis.

A.3.1 Phonon Scattering

The mobility of carriers is affected by the lattice vibrations of 4H-SiC which are described by quasi-particles called phonons. The phonon-oscillations, which depend on the lattice temperature, reduce the mobility of charge carriers. The theoretical model for the scattering of charge carriers by phonons is cited in equation (A.11) that was developed in [49].

$$\mu_{\mathrm{i}}^{\mathrm{L}} = \mu_{\mathrm{i,max}} \cdot \left(\frac{\mathrm{T}}{300K} \right)^{-\xi_{\mathrm{i,L}}} \tag{A.11}$$

The parameter set empirically deduced for 4H-SiC is summarized in table A.6 and is taken from [46].

Variable	**Electrons**	**Holes**	**Unit**
$\mu_{\mathrm{i,max}}$	1417	470.5	$\mathrm{cm^2V^{-1}s^{-1}}$
$\xi_{\mathrm{i,L}}$	2.5	2	1

Table A.6: Parameters for the modeling of $\mu_{\mathrm{i}}^{\mathrm{L}}$ for 4H-SiC [46].

A.3.2 Impurity Scattering

Besides lattice phonons, impurities (deposited intentionally as well as unintentionally) act as additional scattering centers for charge carriers. The reduction of the

carrier mobility due to high impurity concentrations was empirically investigated for Si in [50]. The model developed therein is valid for impurity concentrations N_{tot} of $1 \times 10^{14}\,cm^{-3}$ up to $1 \times 10^{19}\,cm^{-3}$. Above a concentration of $1 \times 10^{19}\,cm^{-3}$ the degradation of carrier mobility becomes a constant, asymptotic value, which was analyzed for Si in [51]. Equation (A.12) shows the empirically deduced formula for μ_i^{LI} covering the influence of low and high impurity concentrations. The index i indicates either for electrons (n) or holes (p).

$$\mu_i^{LI}(N_{tot}, T) = \mu_{i,min} \cdot \exp\left(-\frac{P_{i,c}}{N_{tot}}\right) + \frac{\mu_i^{L}(T) - \mu_{i,min2}}{1 + \left(\frac{N_{tot}}{N_{i,lowdop}}\right)^{\alpha_{i,lowdop}}} - \frac{\mu_{i,1}}{1 + \left(\frac{N_{i,highdop}}{N_{tot}}\right)^{\beta_{i,highdop}}} \quad (A.12)$$

The temperature dependent phonon scattering μ_i^L is included into the model. The last fraction of the equation (A.12) takes into account the saturation of the mobility degradation at high impurity concentrations. The parameter $P_{i,c}$ is a reference concentration for the doping material boron and is empirically deduced in [51].
The parameter for 4H-SiC are evaluated in [46] and are summarized in table A.7. They are not containing a modeling of the influence of high impurity concentrations ($\mu_{i,1} = 0$). As the p-doping in most 4H-SiC-devices is implanted aluminum, the boron-specific parameter $P_{i,c}$ is also set to 0.

Variable	**Electrons**	**Holes**	**Unit**
$\mu_{i,min}$	15.48	2.529	$cm^2V^{-1}s^{-1}$
$\mu_{i,min2}$	1.6	1.07393	$cm^2V^{-1}s^{-1}$
$\mu_{i,1}$	0	0	$cm^2V^{-1}s^{-1}$
$N_{i,lowdop}$	1.8037e17	1.27949e19	cm^{-3}
$N_{i,highdop}$	3.43e20	6.1e20	cm^{-3}
$\alpha_{i,lowdop}$	0.560723	0.332645	1
$\beta_{i,highdop}$	2.0	2.0	1
$P_{i,c}$	0	0	cm^{-3}

Table A.7: Parameter values for 4H-SiC to calculate doping dependent carrier mobilities [46].

The limitation in this empirical model is an impurity concentration of $1 \times 10^{19}\,cm^{-3}$ for 4H-SiC due to lack of parameters and has to be taken into account in device simulations.

A.3.3 High Field Saturation

The linear proportionality of the velocity $\vec{v_i}$ of a charge carriers as function of the electric field $\vec{E}$ is only valid until a material specific saturation velocity $v_{i,sat}$ is reached. The theoretical modeling for the calculation of the saturation velocities of electrons and holes was investigated for Si in [52] and is shown in equation (A.13). The index i indicates either for electrons (n) or holes (p).

$$v_{i,sat} = v_{i,sat,0} \cdot \left(\frac{300K}{T}\right)^{v_{i,sat,exp}} \tag{A.13}$$

The corresponding parameters for 4H-SiC are summarized in table A.8 and were deduced in [46].

Variable	**Electrons**	**Holes**	**Unit**
$v_{i,sat,0}$	2.2×10^7	2.2×10^7	cms^{-1}
$v_{i,sat,exp}$	0.44	0.44	1

Table A.8: Parameter values for velocity saturation in 4H-SiC [46].

The saturation of the carrier velocities leads to a reduced increase of the carrier mobility with higher electric fields. The reduction of the mobility μ_i^{LI} due to high electric fields is theoretically described in equations (A.14) and (A.15) that are both developed for Si in [52]. Equation (A.15) contains the temperature dependency of the high-field mobility. The index i indicates either for electrons (n) or holes (p).

$$\mu_{i,hsf}(\vec{E}) = \frac{\mu_i^{LI}}{\left[1 + \left(\frac{\mu_i^{LI} \cdot |\vec{E}|}{v_{i,sat}}\right)^{\beta_{i,hfs,temp}}\right]^{1/\beta_{i,hfs,temp}}} \tag{A.14}$$

$$\beta_{i,hfs,temp} = \beta_{0,i,hfs} \cdot \left(\frac{T}{300\,K}\right)^{\beta_{i,hfs,exp}} \tag{A.15}$$

The parameter values for 4H-SiC (see table A.9) are also taken from [46].

Variable	Electrons	Holes	Unit
$\beta_{0,i,hfs}$	1.2	1.2	1
$\beta_{i,hfs,exp}$	1.0	1.0	1

Table A.9: Parameter values for high-field-mobility in 4H-SiC [46].

A.3.4 Carrier-Carrier Scattering

Besides the scattering on phonons and impurities, the charge carrier densities (n and p) can also impact their mobility. This mobility reduction through carrier-carrier scattering can be considered independently from the other influences on the mobility. It is included calculating the total mobility via Matthiesen's rule (equation (A.16)).

$$\frac{1}{\mu_{\mathrm{i,tot}}} = \frac{1}{\mu_{i,hsf}} + \frac{1}{\mu_{\mathrm{i,ccs}}} \tag{A.16}$$

The empirical model describing the influence of carrier-carrier-scattering on the mobility ($\mu_{\mathrm{i,ccs}}$) was developed in [53] and is given in (A.17).

$$\mu_{\mathrm{i,ccs}} = \frac{\mathrm{D_{i,ccs}} \cdot \left(\frac{\mathrm{T}}{300\,\mathrm{K}}\right)^{3/2}}{\sqrt{\mathrm{np}}} \cdot \left[\ln\left(1 + \mathrm{F_{i,ccs}} \cdot \left(\frac{\mathrm{T}}{300\,\mathrm{K}}\right)^{2} \cdot (\mathrm{np})^{-1/3}\right)\right]^{-1} \tag{A.17}$$

The parameter $\mathrm{D_{i,ccs}}$ and $\mathrm{F_{i,ccs}}$ are fit-parameters (see table A.10) for the empirical investigations in [53] and have no additional adjustment for 4H-SiC.

Variable	**Electrons**	**Holes**	**Unit**
$\mathrm{D_{i,ccs}}$	1.04×10^{21}	1.04×10^{21}	$\mathrm{cm^{-1}V^{-1}s^{-1}}$
$\mathrm{F_{i,ccs}}$	7.452×10^{13}	7.452×10^{13}	$\mathrm{cm^{-2}}$

Table A.10: Parameter values for mobility reduction due to carrier-carrier-scattering in 4H-SiC [53].

A.4 Recombination of Charged Carriers

The recombination of carriers reduces the amount of free carriers in a semiconductor. Within the framework of this PhD-thesis two non-radiative recombination mechanisms are considered. First the recombination between two bands (Auger-recombination) and second the recombination via impurities (SRH-Recombination). Both have impact on the average lifetime of a charge carrier in the semiconductor.

A.4.1 Auger Recombination

Auger-recombination is a band-to-band recombination which means that e.g. an electron from the conduction band recombines with a hole in the valence band. As 4H-SiC is an indirect semiconductor the electron loses energy and impulse which is both transferred to another electron in the conduction band [1]. Auger-recombination is proportional to the concentrations of electrons and holes (n, p) and is modeled by equation (A.18) developed in [54].

$$R_A = (C_n \cdot n + C_p \cdot p) \cdot (n \cdot p - {n_i}^2) \tag{A.18}$$

For 4H-SiC there is no modeling of the temperature dependence of the capture coefficients for electrons C_n and holes C_p. Therefore, only constant values for C_n and C_p (see table A.11) are accessible in [46].

Variable	**Value**	**Unit**
C_n	3×10^{-29}	cm^6s^{-1}
C_p	3×10^{-29}	cm^6s^{-1}

Table A.11: Constant values for the Auger-coefficients of 4H-SiC [46].

A.4.2 Shockley-Read-Hall-Recombination

Shockley-Read-Hall (SRH)-recombination describes the recombination of charge carriers via electrically active impurities. The impurities are Coulomb attractive centers that capture and emit charge carriers. The recombination rate R_{SRH} is depending on the lifetimes of electrons τ_n and holes τ_p, that are dependent on the impurity concentration N_{tot} and the lattice temperature T [1]. Equations (A.19),

(A.20) and (A.21) describe the SRH-recombination under the assumption of only one type of impurity [55].

$$R_{SRH} = \frac{n \cdot p - {n_i}^2}{\tau_p \cdot (n + n_1) + \tau_n \cdot (p + p_1)} \tag{A.19}$$

$$n_1 = n_i \cdot \exp\left(\frac{E_t}{k_B \cdot T}\right) \tag{A.20}$$

$$p_1 = n_i \cdot \exp\left(\frac{-E_t}{k_B \cdot T}\right) \tag{A.21}$$

The reduction of the carrier lifetimes due high impurity concentrations is described by equation (A.22) that was developed for Si in [58].

$$\tau_{i,dop} = \tau_{i,min} + \frac{\tau_{i,max} - \tau_{i,min}}{1 + \left(\frac{N_{tot}}{N_{i,ref}^{SRH}}\right)^{\gamma_i^{SRH}}} \tag{A.22}$$

The parameter for 4H-SiC are summarized in table A.12 and are taken from [2].

Variable	**Electrons**	**Holes**	**Unit**
$\tau_{i,min}$	0	0	s
$\tau_{i,max}$	6×10^{-7}	1.2×10^{-7}	s
$N_{i,ref}^{SRH}$	7×10^{16}	7×10^{16}	cm^{-3}
γ_i^{SRH}	1	1	1

Table A.12: Values for the doping dependence of the SRH-recombination in 4H-SiC [2].

Besides the concentration of electrical active impurities N_{tot}, the lattice temperature T has a strong influence on the SRH carrier lifetimes. With increasing temperature the capture cross sections of the Coulomb-attractive centers (impurities) are diminished and as a consequence the recombination rate is decreasing significantly as well. This increase of the carrier lifetimes with increasing lattice temperature is modeled by equation (A.23), which is based on the research in [55].

$$\tau_i(T) = \tau_i(300K) \cdot \exp\left(2.55 \cdot \left(\frac{T}{300\,K} - 1\right)\right) \tag{A.23}$$

The parameters for 4H-SiC are taken from [56] and suggest a positive temperature coefficient for the carrier lifetimes, which is in contradiction to the behaviour described in [55]. Nevertheless, the final result in [55] is based on specific test devices and moreover the author explaines that the negative temperature coefficient for SRH carrier lifetimes may change with different process technologies for devices or varying semiconductor materials. Besides the parameters from [56] for TCAD simulations with SDevice the empirical data for hole lifetimes in high-voltage 4H-SiC rectifiers contained in [57] also shows a positive temperature coefficient. Due to this results in combinations with the theoretical explanations in section 4.3.4 we assume a positive temperature coefficient for SRH carrier lifetimes for the 4H-SiC rectifiers investigated in this work.

A.5 Basic semiconductor equations

The physical quantities presented in the previous sections have direct influence on the performance of power semiconductor devices. This section summarizes the equations necessary to calculate the electric current density of power semiconductor devices.
The theoretical description of quasi-static conduction in forward direction is based on the 'Drift-Diffusion-Model', which describes the electric current densities of electrons $\vec{j}_n$ and holes $\vec{j}_p$ driven by the gradient of the electrostatic potential (electrostatic field) and the gradients of the respective carrier concentrations. It is important to note, that a gradient in the device temperature can lead to an electric current of charge carriers, too. In this case the charge carriers transport the heat from hot to cold areas in the respective device. Among the measurements in this PhD-thesis only the surge-current pulses described in section 3.3 are long enough to rise the device temperature, which makes an accountable impact on the electric current density.
The amount of self-heating that occurs during measurements, that were also performed in TCAD-simulations, is negligible due to either low electric powers during quasi-static LC-measurements or very short pulse widths during fast dynamic HC-measurement. Therefore, it is convenient to assume isothermal measurement conditions and a homogeneous temperature distribution inside the devices, in these measurements.
The following equations link the previously discussed physical quantities to characteristic properties of power semiconductor devices. Equation (A.24) summarizes the influences of carrier concentrations and mobilities on the electric conductivity [1]. Moreover, it can be used for unipolar (only one type of carriers) and bipolar (two types of carriers) conduction and therefore also clarifies the difference in the electric conductivities of both types.

$$\sigma = q \cdot (n \cdot \mu_n + p \cdot \mu_p) \tag{A.24}$$

Equations (A.25) and (A.26) are the continuity equations for electrons and holes, that link together the concentration of the respective type of carrier, recombination rates and the ionization of dopants.

$$\frac{\partial n}{\partial t} = \frac{1}{q} \cdot \operatorname{div} \vec{j_n} - R + \frac{\partial N_D}{\partial t} \tag{A.25}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \cdot \operatorname{div} \vec{j_p} - R + \frac{\partial N_A}{\partial t} \tag{A.26}$$

Equations (A.27) and (A.28) describe the electric current densities of electrons and holes driven by an external electric field and the gradient in the respective carrier concentration [3]. The total electric current density of a device is calculated as the sum of both equations.

$$\vec{j_n} = q \cdot \mu_n \cdot n \cdot \vec{E} + \mu_n \cdot k_B \cdot T \cdot \nabla n \tag{A.27}$$

$$\vec{j_p} = q \cdot \mu_p \cdot p \cdot \vec{E} - \mu_p \cdot k_B \cdot T \cdot \nabla p \tag{A.28}$$

The equations introduced in this section serve as basis for later interpretations of measurement and simulation results. The effects on physical quantities caused by changing temperatures need to be linked from the respective physical parameter to the actual device behaviour. In the next section all physical quantities discussed in this chapter are summarized.

A.6 Theoretical setup for simulations in forward direction

All physical models introduced in the previous sections are used for the simulations of 4H-SiC diodes in forward direction. Table A.13 summarizes all physical models in combination with their dependencies on other physical quantities.

Physical Parameter	**Dependencies**
Bandgap	T
Intrinsic densities	T
Effective densities of states	T
Incomplete ionization	T
Carrier Mobility	T N_{tot} n, p $\vec{E}$
Auger-recombination	-
SRH-recombination	T N_{tot}

Table A.13: Summary of dependencies for physical parameter considered in the device-simulations with Sentaurus Device within the framework of this PhD-thesis [2].

By default, the parameter-sets introduced in this chapter are used, but for the adjustment of measurement and simulation certain parameters are varied (see chapter 4). Besides the modeling of physical processes in the devices, it is also necessary to define the boundary conditions to solve differential equations. By default, the top- and bottom-contact of all diodes in view are considered to be ideal Ohmic contacts with infinite recombination rates and electric conductivity. The alternative is a Schottky contact, but several test simulations with Schottky contacts exhibiting only small energetic barriers led to high very gradients in the electric currents that inhibited the convergence of the simulations. In consequenz of that, the idealization with Ohmic contacts was necessary to ensure numeric stability during the simulations. Following the implementation of the real measurement setup, the bottom-contacts of all devices simulated are defined as the heat sinks with fixed temperature and thermal resistance (see section 2.4). The definition of thermodes in the TCDA-simulation enables the simulation of a thermal network, too.

Glossary

α_{A}	Prefactor decribing the reduction of $\Delta E_{A,0}$ by N_{tot}
α_{D}	Prefactor decribing the reduction of $\Delta E_{D,0}$ by N_{tot}
α_{Eg}	Parameter for temperature dependence of the bandgap energy
$\alpha_{\mathrm{i,lowdop}}$	Exponent for the calculation of carrier mobility for low doping, i = [n,p]
α_{n}	Ionization coefficient for electrons.
α_{p}	Ionization coefficient for holes.
α_{τ}	Fit parameter for the temperature dependence of SRH-carrier lifetimes indicating the activation energy of defects
A_{Schottky}	Active area of a unipolar device.
β_{Eg}	Reference temperature for temperature dependence of the bandgap energy
$\beta_{0,i,hfs}$	Parameter for high field saturation mobility for SDevice (i stands either for n or p)
$\beta_{i,hfs,exp}$	Parameter for high field saturation mobility for SDevice, i = [n,p]
$\beta_{\mathrm{i,highdop}}$	Exponent for the calculation of carrier mobility for high doping, i = [n,p]
$\beta_{i,hfs,temp}$	Parameter for high field saturation mobility, i = [n,p]
β_{τ}	Fit parameter for the temperature dependence of SRH-carrier lifetimes indicating the the temperature dependence of the concentration of active defects
L_{BNC}	Inductance of the coaxial-cable connecting the electrical feedthrough and the Tektronix TDS 3034B oscilloscope (outside of the chamber)
C_{bgn}	Correction factor for bandgap narrowing
C_{n}	Auger-coefficient for electrons

C_{Par}	Capacitance of the voltage source connected in parallel
C_p	Auger-coefficient for holes
C_{SMC}	Capacitance of the coaxial-cable connecting the current monitor of the LDP-V80 V3 pulsed current driver and the electrical feedthrough (inside the chamber)
C_{Tek}	Internal capacitance of theTektronix TDS 3034B oscilloscope
C_{VProbe}	Internal capacitance of the voltage probe
$D_{i,ccs}$	Fit parameter for the calculation of carrier mobility taking into account the influence of carrier-carrier-scattering, i = [n,p]
$\delta E_{g,0}$	Bandgap energy correction
ΔE_A	Energy gap between the valence band edge and the acceptor level
$\Delta E_{A,0}$	Energy gap between the valence band edge and the acceptor level for low dopant concentrations
ΔE_D	Energy gap between the conduction band edge and the donor level
$\Delta E_{D,0}$	Energy gap between the conduction band edge and the donor level for low dopant concentrations
$\vec{E}$	Electric field intensity
E_1	Prefactor for bandgap narrowing
E_A	Energy level of an acceptor
ΔE_{bgn}	Narrowing of the bandgap energy
E_c	Energy level of the conduction band edge
E_{crit}	Critical electric field for charge carrier multiplication by avalanche generation
E_D	Energy level of donors
E_g	Bandgap energy
$E_{g,0}$	Bandgap energy at 0 K
ε_r	Relative permittivity
E_t	Energy level of a trap
E_v	Energy level of the valence band edge
$F_{i,ccs}$	Fit parameter for the calculation of carrier mobility taking into account the influence of carrier-carrier-scattering, i = [n,p]
g_A	Degeneracy factor for acceptor levels

γ_i^{SRH}	Exponent for doping dependence of SRH-lifetime, i = [n,p]
g_D	Degeneracy factor for donor levels
$\vec{j}_n$	Electric current density for electrons
$\vec{j}_p$	Electric current density for holes
k_B	Boltzmann constant
κ_L	Thermal conductivity of the semiconductor lattice
$L_{Connect}$	Inductance of the connection of LDP-V80 V3 pulsed current driver and the DUT
L_{SMC}	Inductance of the coaxial-cable connecting the current monitor of the LDP-V80 V3 pulsed current driver and the electrical feedthrough (inside the chamber)
$L_{VConnect}$	Inductance of the connection of the voltage probe and the DUT
$\mu_{i,1}$	Reference carrier mobility in the lattice for effects due to high impurity concentration, i = [n,p]
$\mu_{i,ccs}$	Carrier mobility taking into account the influence of carrier-carrier-scattering, i = [n,p]
$\mu_{i,hsf}$	High field saturation mobility taking into account the influences of phonon- and impurity scattering, i = [n,p])
$\mu_{i,max}$	Maximum carrier mobility in the lattice at 300 K, i = [n,p]
μ_i^{LI}	Carrier mobility under consideration of lattice temperature and impurity concentration, i = [n,p]
$\mu_{i,min}$	Minimum carrier mobility in the lattice, i = [n,p]
$\mu_{i,min2}$	Reference carrier mobility in the lattice, i = [n,p]
μ_i^L	Carrier mobility due to phonon scattering, i = [n,p]
$\mu_{i,tot}$	Carrier mobility taking into account all influences, i = [n,p]
μ_n	Electron mobility
μ_p	Hole mobility
n	Electron concentration
$N_{0,bgn}$	Reference impurity concentration for bandgap narrowing
n_1	Excess concentration of electrons for the calculation of the SRH-recombination rate
N_A	Concentration of electrical active acceptors

$N_{A,0}$	Concentration of acceptors
$N_{A,crit}$	Critical concentration of electrical active acceptors
N_A^-	Concentration of ionized acceptors
N_c	Effective density of states of the conduction band edge
N_D	Concentration of electrical active donors
$N_{D,0}$	Concentration of donors
$N_{D,crit}$	Critical concentration of electrical active donors
N_D^+	Concentration of ionized donors
n_i	Intrinsic carrier concentration
$N_{i,highdop}$	Reference impurity concentration for the calculation of carrier mobility for high doping, i = [n,p]
$N_{i,lowdop}$	Reference impurity concentration for the calculation of carrier mobility for low doping, i = [n,p]
$N_{i,ref}^{SRH}$	Reference doping concentration for SRH-lifetime, i = [n,p]
N_{tot}	Total concentration of electrical active impurities
N_v	Effective density of states of the valence band edge
p	Hole concentration
p_1	Excess concentration of holes for the calculation of the SRH-recombination rate
$P_{i,c}$	Reference impurity concentration, i = [n,p]
p_{vac}	Pressure in the vaccum chamber
q	Positive elementary charge
R	Total recombination rate
R_A	Auger-recombination rate
R_{BNC}	Ohmic resistance of the coaxial-cable connecting the electrical feedthrough and the Tektronix TDS 3034B oscilloscope (outside of the chamber)
$R_{Connect}$	Ohmic resistance of the connection of LDP-V80 V3 pulsed current driver and the DUT
R_{MOS}	Ohmic resistance of a MOS-FET in the on-state
R_Ω	Ohmic resistance of the drift-zone of a unipolar device.
R_{Ser}	Ohmic resistance of the voltage source connected in series
R_{Shunt}	Ohmic resistance of the current monitor

R_{SMC}	Ohmic resistance of the coaxial-cable connecting the current monitor of the LDP-V80 V3 pulsed current driver and the electrical feedthrough (inside the chamber)
R_{SRH}	SRH-recombination rate
R_{Tek}	Internal Ohmic resistance of the Tektronix TDS 3034B oscilloscope
R_{th}	Thermal resistance of the heat sink below the bottom contact of a DUT
$R_{VConnect}$	Ohmic resistance of the connection of the voltage probe and the DUT
R_{VProbe}	Internal Ohmic resistance of the voltage probe
σ	Electric conductivity
T	Lattice temperature
τ_i	SRH-lifetime, i = [n,p]
$\tau_{i,dop}$	Doping dependent SRH-lifetime, i = [n,p]
$\tau_{i,max}$	Maximum doping dependent SRH-lifetime, i = [n,p]
$\tau_{i,min}$	Minimum doping dependent SRH-lifetime, i = [n,p]
τ_n	SRH-lifetime for electrons
τ_p	SRH-lifetime holes
T_{coeff}	Temperature dependence of SRH-lifetimes without considering activated carbon vacancies
V_D	Voltage drop across a non-conducting pn-junction due to the electric field caused by the diffusion of majority carriers
$\vec{v}_i$	Velocity of a charge carrier, i = [n,p]
$v_{i,sat}$	Saturation velocity, i = [n,p]
$v_{i,sat,0}$	Saturation velocity at 300K, i = [n,p]
$v_{i,sat,exp}$	Parameter for saturation velocity, i = [n,p]
V_{turn}	Turning voltage for the bipolar activation of a JBS-Diode .
w_B	Width of the drift-zone of a device.
$\xi_{i,L}$	Exponent for temperature dependence of carrier mobility, i = [n,p]

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