Characteristics and optimisation
of vertical and planar tunnelling-FETs

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Abstract. Scaling MOSFETs becomes more and more difficult. The tunnelling-FET is a possible successor of today's MOSFET with better scaling possibilities. Two different device structures, a vertical and a planar version of a tunnelling-FET are presented and evaluated.

1. Introduction

The traditional MOSFET materials such as silicon, silicon dioxide, and polysilicon have been pushed to fundamental material limits and continued scaling of the classical MOSFET requires the introduction of new materials [1]. However, it is still very questionable if solutions, such as high-k materials can be used to overcome these limits [2].

A different approach for decreasing device size and therefore increasing device integration is the introduction of a transistor with a different working principle. One of the demands for such a transistor is compatibility to CMOS technology. Due to its small size, quantum mechanical effects like tunnelling, which are limiting the performance of MOSFETs, will influence the transistor's characteristics.

The tunnelling field effect transistor (TFET) is a promising candidate for enabling further scaling of device size without severe short channel effects (SCE) [3]. In this paper a vertical and a planar version of the TFET are investigated.

2. TFET working mechanism

The TFET is a tunnelling device. Its working principle is gate-controlled interband tunnelling in a reverse-biased *pin*-structure. The intrinsic region of this structure is covered by a MOS-gate. Fig. 1 shows the band diagram of the transistor's channel region close to the gate. In the off state, where the gate is grounded, the drain current I_d equals the extremely low reverse-blocking current of a *pin*-diode.

By applying a positive gate-source voltage an electron channel is formed underneath the gate oxide, which pulls the conduction and the valence band edges in the intrinsic region downwards. This leads to the formation of a shallow barrier at the interface of the p^+-doped region and the channel. Now, electrons can tunnel from the valence band to the conduction band and therefore induce a higher I_d. Because of the similar characteristics to a NMOS FET, this operation mode
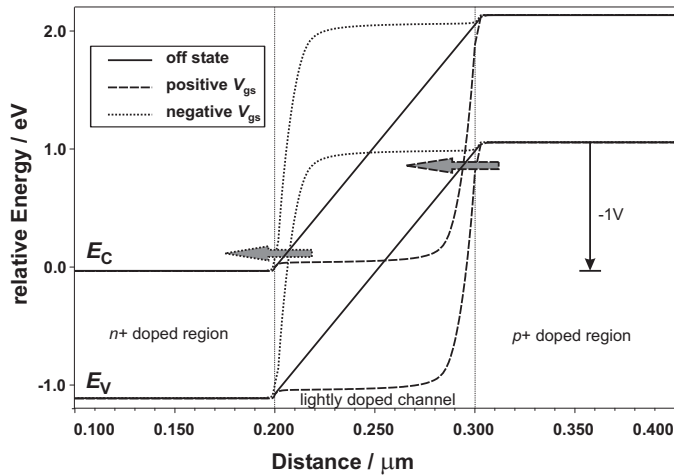
Figure 1. Simulated energy band diagram of a tunnelling FET for different gate voltages. The arrows indicate the tunnelling region and direction.

is also called NTFET. Note, that the source for both NTFET and PTFET is defined as the highly doped region, which is closest to the tunnel junction.

A negative gate-source voltage leads to the formation of a hole channel and the band edges become pulled up. Again, this leads to a shallow barrier, but this time at the interface of the n^+-doped region and the channel. Now, the transistor is in PTFET operation. The arrows in fig. 1 indicate the region, where tunnelling occurs.

Only the tunnelling region of the TFET is the active area of this device. Since this region is very small the channel can be scaled down to 20 nm and below without using other than standard MOSFET materials [4].

3. Device structures

Two different device structures have been investigated so far, the vertical and the planar TFET. Simulation results of previous work [5] show, that in general, the source doping, the oxide thickness of the MOS-gate and the doping profile at the source-channel interface are important parameters for optimising the device characteristics. The source doping should be as high as possible, a realistic value lies in the order of 1×10^{20} cm^{-3}. Thin oxides increase the impact of the gate potential on the channel and therefore improve the sub threshold slope as well as the maximum I_{d}. An abrupt doping profile would result the best characteristics, that is why doping smear out should be kept as small as possible.

3.1. Vertical TFET

A schematic of the device structure of a vertical TFET is shown in fig. 2. The doped silicon of the source, channel and drain region are deposited by molecular beam epitaxy (MBE). To realise the necessary abrupt, degenerately doped p^+-region a so called δ-layer is deposited above the intrinsic channel. Further, the wafers are mesa-etched for device patterning and isolation. On the vertical sidewalls the thermal gate oxide is fabricated and covered with n^+-poly-silicon. Experimental results of this device achieve a ratio $I_{\mathrm{d\,on}}/I_{\mathrm{d\,off}} = 10^5$ and a minimum leakage current of 4×10^{-10} A/μm [6].

Additional performance improvements in terms of $I_{\mathrm{d\,on}}/I_{\mathrm{d\,off}}$, S and V_{th} can be accomplished by replacing the highly doped silicon-δ-layer by a highly doped strained SiGe-δ-layer [7]. Due to the lower bandgap of this material, there is a higher tunnelling probability for electrons in this region and therefore higher $I_{\mathrm{d\,on}}$ can be realised. Fig. 3 shows the simulated transfer characteristics of a vertical TFET with a 1×10^{20} boron-doped SiGe-δ-layer. *IV*-curves for different fractions of Ge in the δ-layer are displayed. The 1×10^{16} doped channel is 100 nm long
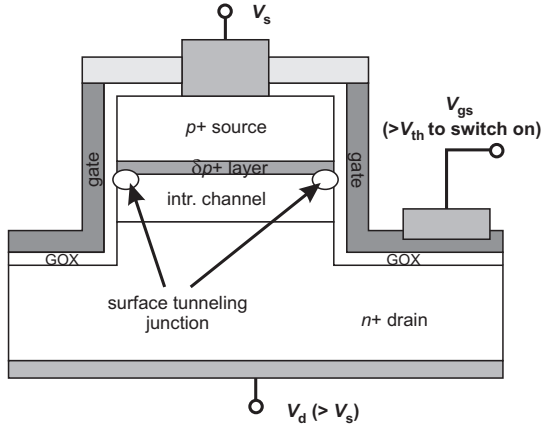
Figure 2. Schematic cross section through the structure of a vertical TFET, where the source is p-doped and the drain is n-doped (NTFET). For a high doping at the source-channel interface, a $p^+\delta$-layer is inserted.
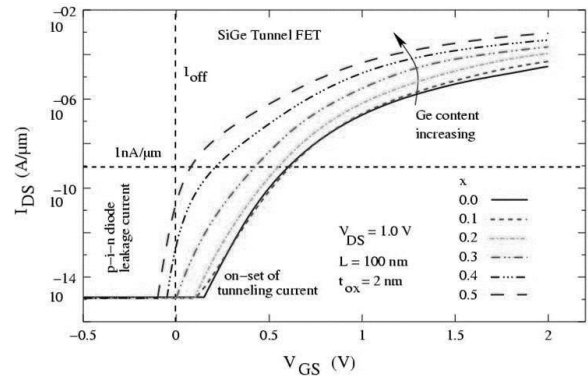

Figure 3. Simulated transfer characteristic of a vertical TFET with a SiGe δ-layer. x is the Germanium fraction.

and the sidewall is covered by a 2 nm thick gate oxide.

3.2. Planar TFET

Fig. 4 shows the schematic cross section of a planar TFET. This transistor is fabricated on a n^--doped substrate with a resistivity of 30-37 Ωcm. The heavily doped p- and n-regions are formed by diffusion of a spin-on-dopant (SOD) in a rapid thermal processing (RTP) chamber. Measurements carried out by a secondary ion mass spectrometer prove, that sharp doping profiles can be accomplished with this doping method. The maximum doping concentration at the surface is about 2.8×10^{20} cm^{-2}. The gate oxide thickness of this TFET is about 6 nm, formed by dry thermal oxidation at 900 °C.

The experimental transfer characteristic of the planar TFET at room temperature can be seen in fig. 5. Due to the reverse biased *pin*-structure, the minimum leakage current is very small. $I_{d\,on}/I_{d\,off}$ is larger than five orders of magnitude. The increase of the leakage current for negative gate bias, which indicates that the tunnel junction is now at the drain channel interface, can be suppressed by a lower drain doping.
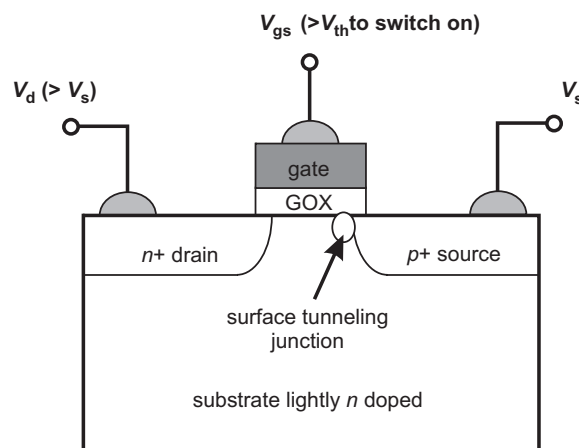

Figure 4. Schematic cross section through the structure of a planar TFET, where the source is p-doped, the drain is n-doped and the channel is lightly n-doped (NTFET). The tunnelling occurs at the surface of the device.
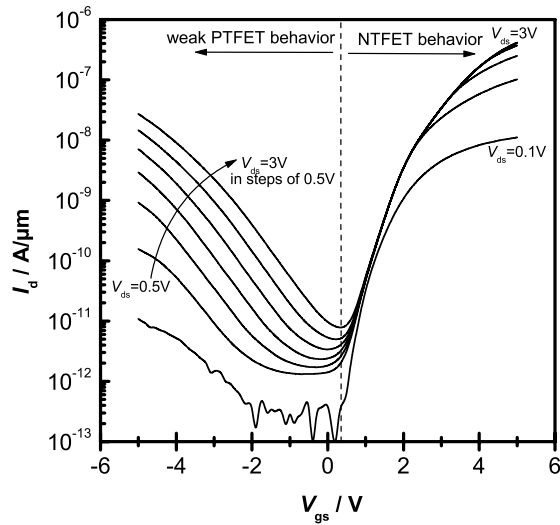
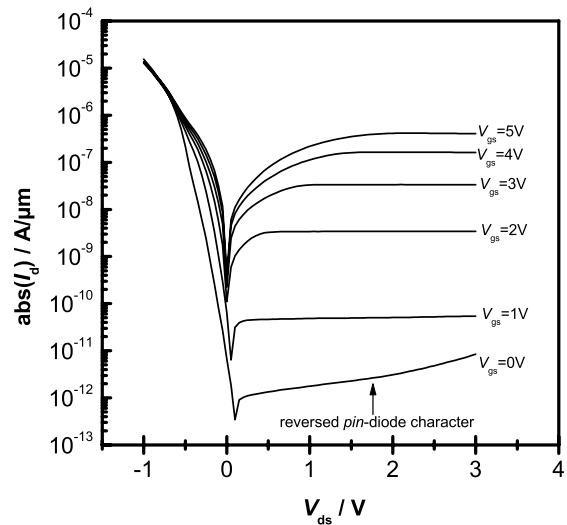**Figure 5.** Experimental transfer characteristic of a planar TFET.

Figure 6. Experimental output characteristic of a planar TFET.

Fig. 6 shows the experimental output characteristic of a planar TFET. At $V_{ds} = 1\,\text{V}$ a leakage current of $1 \times 10^{-12}\,\text{A}/\mu\text{m}$ is measured. Also, current saturation is achieved at very low voltages already. For $V_{gs} = 0\,\text{V}$ the behaviour of the *pin*-diode can be observed.

4. Conclusion and outlook

It is shown, that both the vertical and the planar TFET incorporate the potential for being used in integrated circuits. Further improvements of the device characteristics can be accomplished by integrating SiGe at the tunnel junction. Due to its extremely low leakage current and the large scalability the TFET is an attractive device for both ULSI and low power applications.

It is possible to fabricate a complementary device (PTFET) to the demonstrated NTFET on the same substrate by including *p*-wells in the design. Further investigation is needed to realise ICs with complementary TFET logic.

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