energies

MDPI

Article

AC–AC Modular Multilevel Converter—Hexverter

Cesar A. Arbugeri [1], Samir A. Mussa [1,*] and Marcelo L. Heldwein [2]

[1] Department of Electrical and Electronic Engineering, Federal University of Santa Catarina, Florianopolis 88040-900, Brazil
[2] School of Engineering and Design, Technical University of Munich, 80333 München, Germany
* Correspondence: samir@inep.ufsc.br

Abstract: This article proposes the study, control and analysis of the topology of an AC–AC modular multilevel converter, known in the literature as the Hexverter. The Hexverter is capable of converting the energy between two AC systems with a reduced number of elements, if compared with other modular multilevel topologies, which makes this topology attractive in AC–AC applications. However, there are few studies about the Hexverter in the literature, so this work presents its operation principle, conducts modeling, and proposes a control scheme for the converter's proper operation, validating the operation and control via hardware-in-the-loop emulation.

Keywords: AC–AC converter; Hexverter; modular multilevel converter

check for updates

Citation: Arbugeri, C.A.; Mussa, S.A.; Heldwein, M.L. AC–AC Modular Multilevel Converter—Hexverter. *Energies* **2022**, *15*, 8519. https://doi.org/10.3390/en15228519

Academic Editor: Nicu Bizon

Received: 6 October 2022
Accepted: 4 November 2022
Published: 14 November 2022

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Copyright: © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

One of the main industrial applications for static converters is the electrical drive for variable speed motor control. Typically in these applications, the conversion is performed in two stages. The energy from the electrical grid, considering the fixed voltage and frequency, is rectified to a regulated DC bus, and in the second stage, the DC bus voltage is converted to a three-phase system with variable voltage and frequency that controls the driven machine, regulating its torque and speed [1–5].

This AC–DC–AC conversion is widespread in the literature and is widely employed in industry, being generally employed for converters in the back-to-back configuration. This solution for AC–AC energy conversion is very robust; however, a DC bus with high voltage levels is required, employing electrolytic capacitors, which are bulky components with a high failure rate and a short service life [6].

The AC–AC conversion may also be achieved by a direct converter, i.e., without an intermediate energy storage stage. Among the direct converters, the matrix converters [7] stand out, which present high power density once capacitors are not employed in these topologies. However matrix converters can only be employed in applications where the output voltage is lower than the input voltage, and the lack of capacitors makes the converter control more complex. Once the converter dynamics are more susceptible to parametric variations, the switches actuation must be accurate to prevent short circuits or opening of an inductive circuit [8,9].

Another application for direct frequency converters that has become more popular in recent decades is the real-time emulation, PHIL (power hardware-in-the-loop) [10–12], whereby the converter can emulate loads, such as linear loads, non-linear loads, or electric motors. At the same time, it regenerates the energy to the electric grid, allowing these converters to be employed for the development and testing of electrical and electronic equipment such as electronic converters, motor drives, and protection systems, in addition to enabling tests on more complex systems that could not be tested in any other way, such as transmission lines, power systems, and micro-grids. Studies show that PHIL emulation presents better results than numerical simulations [12].

In recent decades, modular multilevel converters have been widely studied and are beginning to be employed in medium voltage applications, such as rectifiers, active filters,

and motor drives. More recently, different MMC topologies have been proposed, mainly in three-phase AC–AC conversion [13].

The main MMC AC–AC topologies are the indirect MMC converter (back-to-back topology), the direct matrix converter (M3C), and the Hexverter. Other topologies have also been proposed, such as in [14], where the Hex-Y topology is proposed, being a combination of different MMC, aiming to combine the different advantages of each converter.

A more recent work [15] proposes modeling and control in a unified two-frequency dq framework and develops a virtual V_C^2 to achieve converter power balance. At the same time, it evaluates two modulation strategies (nearest level control and phase-disposition), validating the results via simulation.

This paper presents the analysis and modeling of the Hexverted, an AC–AC modular multilevel converter, and proposes a control strategy that allows the conversion between two three-phase electrical systems with different levels of voltage, currents. and frequency.

Employing the synchronous and stationary reference frame, the converter current and voltage transfer function can be obtained, which allows classical control theory to be employed for the controller's design, resulting in simpler control for implementation and providing regulation with a proper transient response.

The control strategy is experimentally validated by employing hardware-in-the-loop emulation.

2. The Hexverter Modular Multilevel Converter

The Hexverter topology, as presented in Figure 1, consists of six arms connected to each other in the shape of a hexagon, hence the name Hexverter (hexagonal converter) [16].

Similar to other modular multilevel converters, the Hexverter's arms consist of an inductor, to limit the circulating current, and n sub-modules that impose the arm's voltage, controlling the power flow between the two AC systems.

It is important to note that the sub-modules of the Hexverter must operate in four quadrants (bidirectional in current and voltage) since it is an AC–AC converter. As depicted in Figure 1, the H-bridge converter is employed for the sub-modules.

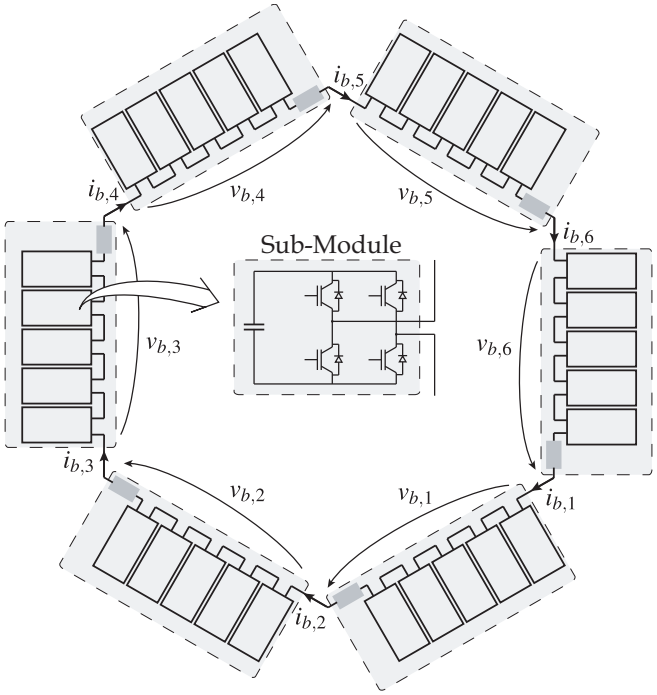

Figure 1. Hexverter topology depicting the connections between the six arms and the sub-module's H-bridge topology.

The AC systems are designated as port 1 (P1—relative to the phases A, B, and C) and port 2 (P2—relative to the phases R, S, and T), as the input port and output port, respectively. P1 and P2 can have different electrical characteristics of frequency, phase, reactive power, voltage, and current amplitude.

Hexverter Operation Principle

Assuming that the converter is operating properly, it can also be assumed that port P1 is composed of the phases A, B, and C, and port P2 is composed of the phases R, S, and T. The following equations describe the voltages and currents:

$$v_a = V_{P1} sin(\omega_1 t) \qquad i_a = I_{P1} sin(\omega_1 t + \phi_1) \tag{1}$$

$$v_b = V_{P1} sin(\omega_1 t - \frac{2\pi}{3}) \qquad i_b = I_{P1} sin(\omega_1 t - \frac{2\pi}{3} + \phi_1) \tag{2}$$

$$v_c = V_{P1} sin(\omega_1 t + \frac{2\pi}{3}) \qquad i_c = I_{P1} sin(\omega_1 t + \frac{2\pi}{3} + \phi_1) \tag{3}$$

$$v_r = V_{P2} sin(\omega_2 t) \qquad i_r = I_{P2} sin(\omega_2 t + \phi_2) \tag{4}$$

$$v_s = V_{P2} sin(\omega_2 t - \frac{2\pi}{3}) \qquad i_s = I_{P2} sin(\omega_2 t - \frac{2\pi}{3} + \phi_2) \tag{5}$$

$$v_t = V_{P2} sin(\omega_2 t + \frac{2\pi}{3}) \qquad i_t = I_{P2} sin(\omega_2 t + \frac{2\pi}{3} + \phi_2) \tag{6}$$

Considering the port voltages applied to the converter and the currents drained/injected into the ports and neglecting the voltage drop in the arm inductor, the voltages in the two adjacent arms are roughly equal to the line voltage applied by the respective port, while the current that circulates in each arm is equal to the phase current.

This results in the arm's voltages being given by:

$$v_1 = V_{P1} sin(\omega_1 t) - V_{P2} sin(\omega_2 t) \tag{7}$$

$$v_2 = V_{P2} sin(\omega_2 t) - V_{P1} sin(\omega_1 t - \frac{2\pi}{3}) \tag{8}$$

$$v_3 = V_{P1} sin(\omega_1 t - \frac{2\pi}{3}) - V_{P2} sin(\omega_2 t - \frac{2\pi}{3}) \tag{9}$$

$$v_4 = V_{P2} sin(\omega_2 t - \frac{2\pi}{3}) - V_{P1} sin((\omega_1 t + \frac{2\pi}{3}) \tag{10}$$

$$v_5 = V_{P1} sin((\omega_1 t + \frac{2\pi}{3}) - V_{P2} sin(\omega_2 t + \frac{2\pi}{3}) \tag{11}$$

$$v_6 = V_{P2} sin(\omega_2 t + \frac{2\pi}{3}) - V_{P1} sin((\omega_1 t) \tag{12}$$

Furthermore, the arm currents are given by:

$$i_1 = \frac{I_{P1}}{\sqrt{3}} sin(\omega_1 t + \frac{\pi}{6} - \phi_1) + \frac{I_{P2}}{\sqrt{3}} sin(\omega_2 t + \frac{5\pi}{6} - \phi_2) \tag{13}$$

$$i_2 = \frac{I_{P1}}{\sqrt{3}} sin(\omega_1 t + \frac{\pi}{6} - \phi_1) + \frac{I_{P2}}{\sqrt{3}} sin(\omega_2 t + \frac{\pi}{6} - \phi_2) \tag{14}$$

$$i_3 = \frac{I_{P1}}{\sqrt{3}} sin(\omega_1 t - \frac{\pi}{2} - \phi_1) + \frac{I_{P2}}{\sqrt{3}} sin(\omega_2 t + \frac{\pi}{6} - \phi_2) \tag{15}$$

$$i_4 = \frac{I_{P1}}{\sqrt{3}} sin(\omega_1 t - \frac{\pi}{2} - \phi_1) + \frac{I_{P2}}{\sqrt{3}} sin(\omega_2 t - \frac{\pi}{2} - \phi_2) \tag{16}$$

$$i_5 = \frac{I_{P1}}{\sqrt{3}} sin(\omega_1 t + \frac{5\pi}{6} - \phi_1) + \frac{I_{P2}}{\sqrt{3}} sin(\omega_2 t - \frac{\pi}{2} - \phi_2) \tag{17}$$

$$i_6 = \frac{I_{P1}}{\sqrt{3}} sin(\omega_1 t + \frac{5\pi}{6} - \phi_1) + \frac{I_{P2}}{\sqrt{3}} sin(\omega_2 t + \frac{5\pi}{6} - \phi_2) \tag{18}$$

It can be noted that each converter's arm has voltage and current components from both ports, given by the phase current and voltage, which implies an additional 30° lag between arm voltage and current components from the same port.

3. Hexverter Modeling

For modeling the Hexverter, the quasi-instantaneous average model of the converter will be considered, as presented in Figure 2, where the n sub-modules of the converter are substituted by their equivalent circuit.

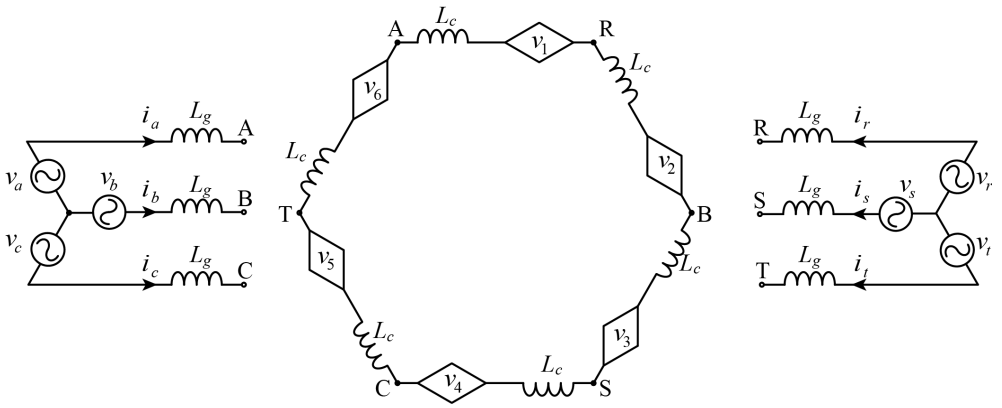

Figure 2. Equivalent circuit of the Hexverter, where the sub-modules are replaced by the equivalent model of a voltage source on the AC side and a current source on the DC side.

The converter model is obtained in a synchronous reference frame for the current control of the port and in stationary reference frame for the DC bus voltage control of the sub-module.

3.1. Synchronous and Stationary Reference Frame Transformation

Here, we present the transformations employed for converter modeling and control. The synchronous reference frame (dq0 transformation) and stationary reference frame ($\alpha\beta 0$ transformation) are considered.

The synchronous voltage transformation (dq0 reference frame) is given by

$$\begin{bmatrix} v_{dP1} \\ v_{qP1} \\ v_{dP2} \\ v_{qP2} \\ v_{0Y} \\ v_{0\Delta} \end{bmatrix} = \frac{\sqrt{2}}{3} \begin{bmatrix} \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & 0 & 0 & -\frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{1}{2} & \frac{1}{2} & \frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} \\ -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & 0 & 0 & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} & \frac{1}{2} & \frac{1}{2} & -\frac{1}{2} \\ \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} sin(\omega_1 t) & -cos(\omega_1 t) & 0 & 0 & 0 & 0 \\ cos(\omega_1 t) & sin(\omega_1 t) & 0 & 0 & 0 & 0 \\ 0 & 0 & sin(\omega_2 t) & -cos(\omega_2 t) & 0 & 0 \\ 0 & 0 & cos(\omega_2 t) & sin(\omega_2 t) & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \\ v_6 \end{bmatrix} \tag{19}$$

where it can be seen that the stationary reference frame transformation is multiplied by the rotation matrix. Similarly, the synchronous transformation for the converter currents can be given as follows:

$$\begin{bmatrix} i_{dP1} \\ i_{qP1} \\ i_{dP2} \\ i_{qP2} \\ i_{0Y} \\ i_{0\Delta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{1}{2} & -\frac{1}{2} & \frac{1}{2} & -\frac{1}{2} & -1 \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} & 0 \\ -1 & 1 & \frac{1}{2} & -\frac{1}{2} & \frac{1}{2} & -\frac{1}{2} \\ 0 & 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & -\frac{1}{2} & \frac{1}{2} & -\frac{1}{2} & \frac{1}{2} & -\frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} sin(\omega_1 t) & -cos(\omega_1 t) & 0 & 0 & 0 & 0 \\ cos(\omega_1 t) & sin(\omega_1 t) & 0 & 0 & 0 & 0 \\ 0 & 0 & sin(\omega_2 t) & -cos(\omega_2 t) & 0 & 0 \\ 0 & 0 & cos(\omega_2 t) & sin(\omega_2 t) & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \\ i_6 \end{bmatrix} \tag{20}$$

It can be seen that the voltage and the current are different. This is due to the converter geometry and the currents and voltages on each of the converter's arms.

Although both transformations are power-invariant, they are not orthonormal, which implies that the inverse transformation is not equal to the transpose. However, the inverse voltage transform is equivalent to the transpose of the current transformation. Similarly, the current inverse transformation is equal to the voltage transformation transpose.

Another important observation is that applying the power invariant dq0 transformation to the ports' voltages and currents results in the same direct and quadrature components as those calculated by Equations (19) and (20).

For the arms' DC buses, the following transformation can be considered:

$$\begin{bmatrix} v_{CC\alpha 1} \\ v_{CC\beta 1} \\ v_{CC\alpha 2} \\ v_{CC\beta 2} \\ v_{CC0Y} \\ v_{CC0\Delta} \end{bmatrix} = \begin{bmatrix} \frac{1}{2} & \frac{1}{4} & -\frac{1}{4} & \frac{1}{4} & -\frac{1}{4} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{4} & -\frac{\sqrt{3}}{4} & -\frac{\sqrt{3}}{4} & \frac{\sqrt{3}}{4} & 0 \\ -\frac{1}{2} & \frac{1}{2} & \frac{1}{4} & -\frac{1}{4} & \frac{1}{4} & -\frac{1}{4} \\ 0 & 0 & \frac{\sqrt{3}}{4} & -\frac{\sqrt{3}}{4} & -\frac{\sqrt{3}}{4} & \frac{\sqrt{3}}{4} \\ 1 & -1 & 1 & -1 & 1 & -1 \\ 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{CC1} \\ v_{CC2} \\ v_{CC3} \\ v_{CC4} \\ v_{CC5} \\ v_{CC6} \end{bmatrix} \tag{21}$$

The arms' DC bus transformation aims to decouple the influence of each arm's current and voltage from the bus voltage. This will become more apparent later, when the DC bus voltage equations are presented.

3.2. Input Current Model and Transfer Function

By equating the converter equivalent circuit depicted in Figure 2, it is possible to obtain the following matrix equation, which describes the current in the Hexverter's arms.

$$L\frac{\partial}{\partial t}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \\ i_6 \end{bmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & 0 & 0 & -1 & 0 & 0 \\ 0 & -1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 & -1 & 0 \\ 0 & 0 & -1 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 \\ -1 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \\ v_r \\ v_s \\ v_t \end{bmatrix} - \begin{bmatrix} d_1 \\ d_2 \\ d_3 \\ d_4 \\ d_5 \\ d_6 \end{bmatrix} nV_{CC} - \begin{bmatrix} -1 \\ 1 \\ -1 \\ 1 \\ -1 \\ 1 \end{bmatrix} v_{CM} \tag{22}$$

Applying the voltage and current dq transformation, it is possible to obtain the input current equations in dq coordinates for the converter, which are described by the matrix equation as

$$\frac{\partial}{\partial t}\begin{bmatrix} (L_{P1}+\frac{2}{3}L_c)i_{dP1} \\ (L_{P1}+\frac{2}{3}L_c)i_{q1} \\ (L_{P2}+\frac{2}{3}L_c)i_{dP2} \\ (L_{P2}+\frac{2}{3}L_c)i_{q2} \\ (L_{P1}+L_c+L_{P2})i_{0Y} \\ L_c i_{0\Delta} \end{bmatrix} = \begin{bmatrix} v_{dP1} \\ v_{qP1} \\ v_{dP2} \\ v_{qP2} \\ 0 \\ 0 \end{bmatrix} - \begin{bmatrix} d_{dP1} \\ d_{qP1} \\ d_{dP2} \\ d_{qP2} \\ d_{0Y} \\ d_{0\Delta} \end{bmatrix} nV_{CC} + \begin{bmatrix} 0 & -\omega_1 & 0 & 0 & 0 & 0 \\ \omega_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\omega_2 & 0 & 0 \\ 0 & 0 & \omega_2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{dP1} \\ i_{q1} \\ i_{dP2} \\ i_{q2} \\ i_{0Y} \\ i_{0\Delta} \end{bmatrix} - \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ v_{CM} \\ 0 \end{bmatrix} \tag{23}$$

From the input current equation, it is possible to obtain the equivalent circuit in dq coordinates, as shown in Figure 3.

It is possible to observe that, with the synchronous transformation, four equivalent circuits were obtained for the differential components of the currents, wherein the components from P1 are independent of the P2 components.

In addition, the model is similar to other three-phase AC converters, which allows the same control strategies to be employed for the input currents, which are already well-described in the literature.

The other two circuits control the common mode currents. The i_{0Y} will only circulate if the two ports' neutral points are connected, and the $i_{0\delta}$ is the converter circulating current.

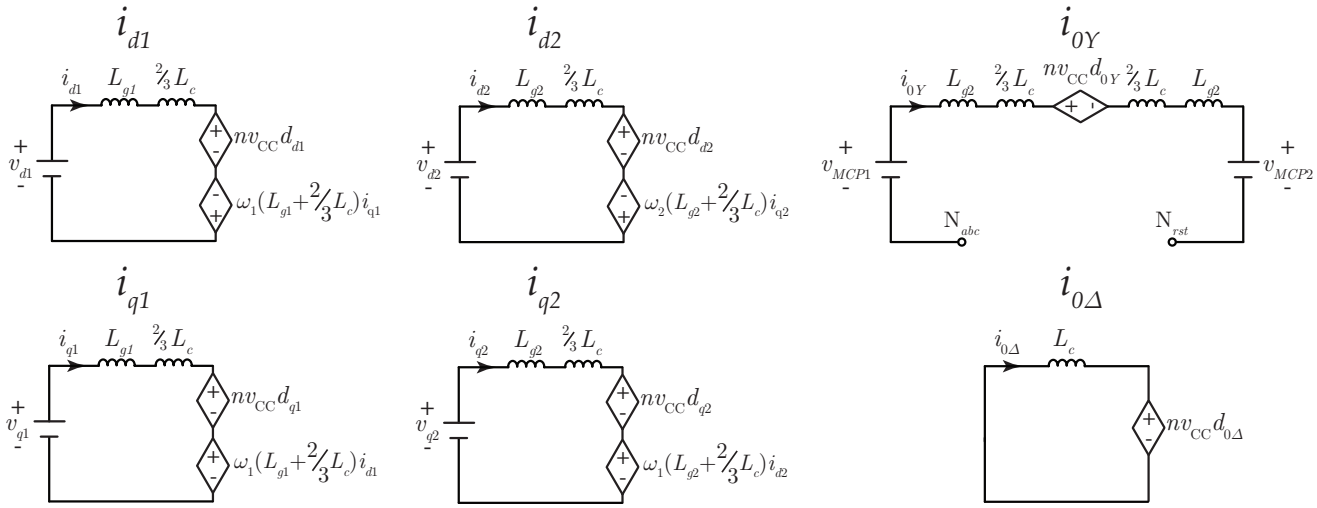

Figure 3. Equivalent circuit for the converter currents in dq coordinates.

3.3. DC Bus Voltage Model and Transfer Function

To obtain the stationary reference frame equivalent model and subsequently the transfer function for the DC bus voltage, the same procedure is adopted as the one for obtaining the input current model, being equated with the DC bus voltages as:

$$\frac{C}{n}\frac{\partial}{\partial t}\begin{bmatrix} v_{CC1} \\ v_{CC2} \\ v_{CC3} \\ v_{CC4} \\ v_{CC5} \\ v_{CC6} \end{bmatrix} = \begin{bmatrix} d_1 i_1 \\ d_2 i_2 \\ d_3 i_3 \\ d_4 i_4 \\ d_5 i_5 \\ d_6 i_6 \end{bmatrix} \tag{24}$$

By pre-multiplying the equation by the DC bus voltage transformation presented in Equation (24) and substituting the duty cycle and current values by the components in the $\alpha\beta$ stationary reference frame, it is possible to obtain the equation for the equivalent DC buses in the stationary reference frame.

Some of the DC bus current components are neglected because they do not influence the average bus voltage. This occurs with components that are the products of the current and duty cycle between port 1 and port 2 ($i_{\alpha1}d_{\alpha2}$, $i_{\alpha1}d_{\beta2}$, $i_{\beta1}d_{\alpha2}$, $i_{\beta1}d_{\beta2}$, $i_{\alpha2}d_{\alpha1}$, $i_{\alpha2}d_{\beta1}$, $i_{\beta2}d_{\alpha1}$, and $i_{\beta2}d_{\beta1}$) since they have different frequencies, the average value is equal to zero, and they only contribute to the DC oscillating voltage.

Furthermore, the i_{0Y} is null since there is no connection between the two systems' neutral point, so this component of the DC bus current may be neglected. Considering this simplification, it is possible to obtain the following equations for the DC bus voltages:

$$\frac{C}{n}\frac{\partial}{\partial t}v_{DC\alpha1} = i_{\alpha2}\left(\frac{d_{\alpha2}}{8} - \frac{d_{\beta2}}{8\sqrt{3}}\right) - i_{\beta2}\left(\frac{d_{\alpha2}}{8\sqrt{3}} + \frac{d_{\beta2}}{8}\right) + \frac{i_{\alpha1}d_{\beta1}}{4\sqrt{3}} - \frac{i_{\beta1}d_{\alpha2}}{4\sqrt{3}} + i_{0\Delta}\left(\frac{d_{\alpha2}}{8} - \frac{d_{\alpha1}}{2} + \frac{\sqrt{3}d_{\beta2}}{8}\right) \tag{25}$$

$$\frac{C}{n}\frac{\partial}{\partial t}v_{DC\beta1} = i_{\alpha2}\left(\frac{d_{\alpha2}}{8\sqrt{3}} + \frac{d_{\beta2}}{8}\right) + i_{\beta2}\left(\frac{d_{\alpha2}}{8} - \frac{d_{\beta2}}{8\sqrt{3}}\right) + \frac{i_{\alpha1}d_{\alpha1}}{4\sqrt{3}} - \frac{i_{\beta1}d_{\beta1}}{4\sqrt{3}} + i_{0\Delta}\left(\frac{d_{\beta2}}{8} - \frac{d_{\beta1}}{2} + \frac{\sqrt{3}d_{\alpha2}}{8}\right) \tag{26}$$

$$\frac{C}{n}\frac{\partial}{\partial t}v_{DC\alpha2} = -i_{\alpha1}\left(\frac{d_{\alpha1}}{8} - \frac{d_{\beta1}}{8\sqrt{3}}\right) + i_{\beta1}\left(\frac{d_{\beta1}}{8} - \frac{d_{\alpha1}}{8\sqrt{3}}\right) - \frac{i_{\alpha2}d_{\alpha2}}{4\sqrt{3}} - \frac{i_{\beta2}d_{\beta2}}{4\sqrt{3}} + i_{0\Delta}\left(\frac{d_{\alpha1}}{8} - \frac{d_{\alpha2}}{2} + \frac{\sqrt{3}d_{\beta1}}{8}\right) \tag{27}$$

$$\frac{C}{n}\frac{\partial}{\partial t}v_{DC\beta2} = i_{\alpha1}\left(\frac{d_{\alpha1}}{8\sqrt{3}} - \frac{d_{\beta1}}{8}\right) - i_{\beta1}\left(\frac{d_{\alpha1}}{8} + \frac{d_{\beta1}}{8\sqrt{3}}\right) + \frac{i_{\alpha2}d_{\alpha2}}{4\sqrt{3}} + \frac{i_{\beta2}d_{\beta2}}{4\sqrt{3}} + i_{0\Delta}\left(\frac{d_{\beta1}}{8} - \frac{d_{\beta2}}{2} + \frac{\sqrt{3}d_{\alpha1}}{8}\right) \tag{28}$$

$$\frac{C}{n}\frac{\partial}{\partial t}v_{DC0Y} = d_{0Y}i_{0\Delta} - \frac{d_{\alpha1}i_{\beta1}}{\sqrt{3}} + \frac{d_{\beta1}i_{\alpha1}}{\sqrt{3}} + \frac{d_{\alpha2}i_{\beta2}}{\sqrt{3}} - \frac{d_{\beta2}i_{\alpha2}}{\sqrt{3}} \tag{29}$$

$$\frac{C}{n}\frac{\partial}{\partial t}v_{DC0\Delta} = d_{\alpha1}i_{\alpha1} + d_{\beta1}i_{\beta1} + d_{\alpha2}i_{\alpha2} + d_{\beta2}i_{\beta2} + d_{0\Delta}i_{0\Delta} \tag{30}$$

Note that the currents in port 2 are imposed by the control, and the currents in port 1 must be regulated so the active power in both ports is equal, discounting the converter losses. By ensuring this, it is possible to regulate the total voltage ($v_{DC0\Delta}$).

Considering this, the only variables left to regulate the other five DC voltages components are the circulating current ($i_{0\Delta}$) and the common mode voltage imposed by the converter with the duty cycle d_{0Y}.

From the $\alpha\beta$ DC bus voltage equations, it is possible to define the following transfer functions for the control of the DC voltages:

$$\frac{v_{DC\alpha1}(s)}{i_{0\Delta}(s)} = \frac{nD_{\alpha1}}{Cs} \tag{31}$$

$$\frac{v_{DC\beta1}(s)}{i_{0\Delta}(s)} = \frac{nD_{\beta1}}{Cs} \tag{32}$$

$$\frac{v_{DC\alpha2}(s)}{i_{0\Delta}(s)} = \frac{nD_{\alpha2}}{Cs} \tag{33}$$

$$\frac{v_{DC\beta2}(s)}{i_{0\Delta}(s)} = \frac{nD_{\beta2}}{Cs} \tag{34}$$

$$\frac{v_{DC0Y}(s)}{i_{0\Delta}(s)} = \frac{nD_{0Y}}{Cs} \tag{35}$$

$$\frac{v_{DC0\Delta}(s)}{i_{d1}(s)} = \frac{nD_{d1}}{Cs} \tag{36}$$

It is important to note that the circulating current ($i_{0\Delta}$) is responsible for controlling all five differential DC voltage components ($v_{DC\alpha1}$, $v_{DC\beta1}$, $v_{DC\alpha2}$, $v_{DC\beta2}$, and $v_{DC0\Delta}$). To achieve this for each differential DC voltage component, the control must impose a circulating current in the same frequency and in phase with its relative voltage; for example, to control the $v_{DC\alpha1}$, the circulating current must have a component in phase with the voltage $v_{\alpha1}$.

In Equation (29), it can be seen that the v_{DC0Y} is dependent on the reactive power in both ports of the converter, which means that the reactive power being processed in each port will directly influence the balance of the DC buses. In other words, if the Hexverter operates with reactive power, it will cause an imbalance in the DC buses that will need to be compensated for.

4. Control

In this paper, the Hexverter is considered to be connected with two three-phase voltage sources, with different characteristics in terms of voltage and frequency. This occurs in applications such as the connection of two electrical grids or the connection of generators with mains, mostly in the field of wind generation.

It is essential to note that the converter can also operate by controlling the output port (P2) voltage if it is feeding a load, when the voltage is not imposed in the converter port by an external source.

The converter has two main control loops, a faster internal loop that controls the currents and an external slower loop that controls the DC bus sub-module voltages. Furthermore, a power loop that generates the current reference for one port must be considered,

for instance, an MPPT algorithm for a wind generator or a power-flow reference (active and reactive power) for the connection between two electrical grids.

4.1. Current Control Loop

The current control loop is responsible for imposing the currents in the ports and the circulating current in the converter ($i_{0\Delta}$). It can be observed that there is no connection between the two system neutrals, which implies that the current i_{0Y} is always null since there is no path to its flows.

For the ports, the control in dq coordinates is considered similar to any three-phase converter where the current error is applied to a controller—a PI controller in this case. Afterward, the decoupling is applied to the PI output, generating the reference for the converter modulator.

To control the circulation, a PI controller is employed, the input being the current reference subtracted from the $i_{0\Delta}$ measured, and the output being the duty cycle $d_{0\Delta}$. Figure 4 depicts the control block diagram.

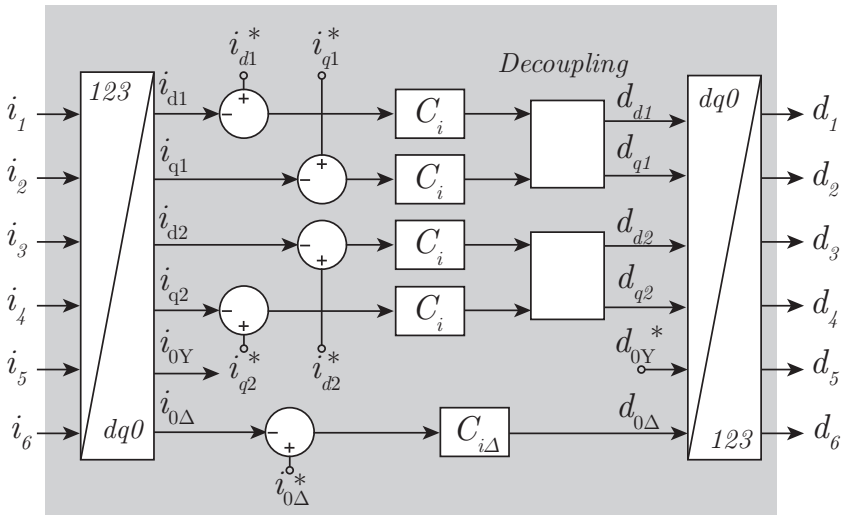

Figure 4. Current control scheme for the Hexverter.

4.2. Voltage Control Loop

The voltage control loop regulates the voltages in the sub-module's DC buses, generating the current reference for port 1 and the circulating current ($i_{0\Delta}$). In this work, the current reference for port 2, generated by the power flow reference algorithm, is already considered to be known, so these currents are regulated by considering an imposed reference.

As previously stated, the voltage $v_{DC0\Delta}$ is controlled by the P1 currents i_{dP1} and i_{qP1}, i_{dP1} being related to the active power and i_{qP1} being related to the reactive power.

The v_{DC0Y} is controlled by imposing a v_{0Y} value of voltage. In this work, the v_{0Y} imposed is equal to $\frac{V_{P1}}{6}sin(\omega 1t) + \frac{V_{P2}}{6}sin(\omega 2t)$; this reduces the peak amplitude of the voltage imposed by each converter arm allowing the DC bus voltage usage to be maximized. The effective control of the v_{DC0Y} is achieved by controlling the circulating current $i_{0\Delta}$.

The remaining differential components of the DC bus voltage are controlled by adding alternating components to the circulating current $i_{0\Delta}$. Ideally, the current's components should be in phase with the voltage imposed by the converter; however, considering that the phase shift between the converter and the load/feed is typically low, it is possible to synchronize it with the ports' voltage considering a small loss of performance.

The DC bus voltage control is presented in Figure 5, where it can be observed that this control loop generates the references for the i_{dP1} and $i_{0\Delta}$ currents.

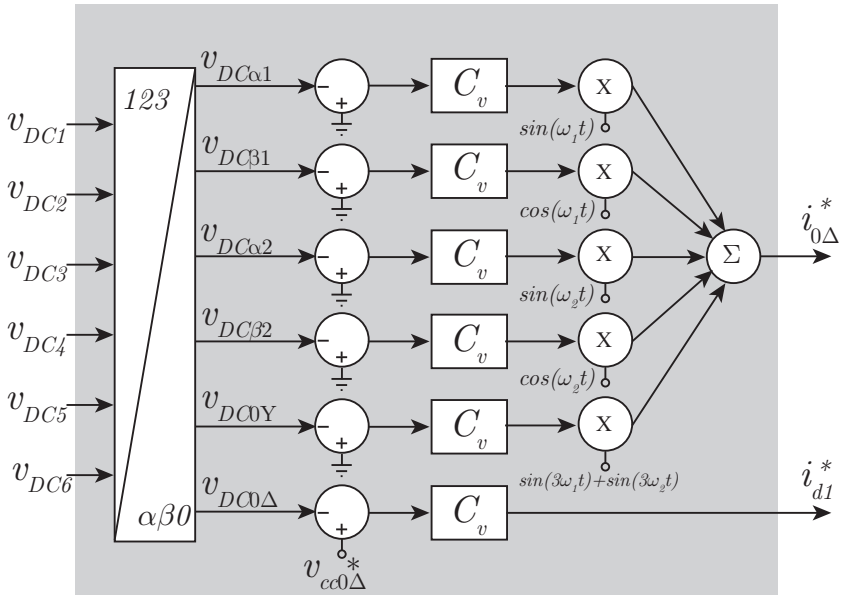

Figure 5. Voltage control scheme for the Hexverter.

4.3. Converter Parameters and Control Design

For the proper operation of the converter, a suitable design of the converter parameters (inductances and capacitances) and the controllers is required. Here, we present the design guidelines employed in this work.

To calculate an appropriate value of grid inductance, the power flow equation between two buses with a inductive transmission line is considered, which results in the following equation:

$$L_g = \frac{|V_{P1}^{grid}||V_{P1}^{conv}|}{2\pi f_{P1} P} sin(\delta) \tag{37}$$

Considering that the grid voltage (V_{P1}^{grid}) is approximately equal to the voltage imposed by the converter (V_{P1}^{conv}) and assuming a small value for the lag (smaller than 5°), it is possible to calculate the grid inductance with the converter power and the frequency of operation.

The adopted circulating inductance (L_c) is 10% of the grid inductance.

In order to calculate the sub-module's capacitance, the oscillating power in the arm is considered, which results in the following equation to calculate the sub-module capacitance with the desired voltage ripple:

$$C_{SM} = \frac{1}{4\pi n V_{DC} \Delta V} \left(\frac{I_{P1} V_{P1}}{f_{P1}} + \frac{I_{P2} V_{P2}}{f_{P2}} \right) \tag{38}$$

This equation considers the converter operating with the unit power factor in both ports; thus, only the ripple from the double frequency of each port is considered. However, when the converter operates with reactive power, an increase in the voltage ripple is observed, mainly in the frequency equal to the difference of the two ports' frequency ($\omega_1 - \omega_2$).

With the current and voltage transfer function, it is possible to design the current loop control and voltage loop control, employing classical control theory to design the controllers.

It is important to consider that the most internal control loops (current control loops) must have a faster response than the external control loops (voltage control loops).

In this paper, the phase-shift modulation is considered, and the duty cycle generated by the current control is directly applied to the modulators that generate the pulse for each respective arm sub-module, with each sub-module from the same arm being shifted by 360 degrees divided by the number of sub-modules per arm $\left(\frac{360^\circ}{n}\right)$.

5. Experimental Results

To obtain the experimental results for the Hexverter, the OPAL-RT OP-5700 was employed to emulate the converter. The HIL is responsible for emulating the Hexverter. The control was implemented in a Cyclone V FPGA, as seen in the control board. The control board samples the HIL's analogs output and generates the PWM pulses to control the Hexverter, which is being emulated in the HIL. The emulation system is shown in Figure 6.

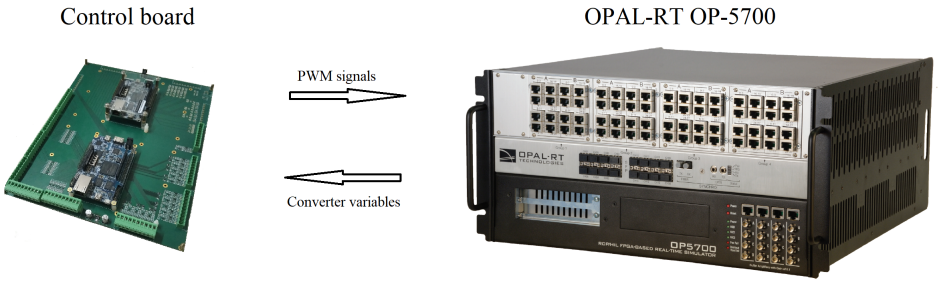

Figure 6. A picture of the control board where the control strategy is implemented, and the HIL OPAL-RT OP-5700, which is responsible for the real-time converter emulation.

The emulated converter is considered to be connected to two grids with different frequencies, and the power flow is considered to be from port 1 to port 2. The converter parameters are depicted in Table 1.

Table 1. Converter parameters specification.

Parameter	Value
Port 1 frequency	$f_g = 60$ Hz
Port 1 voltage	$V_{P1} = 13.8\ \text{kV}_{\text{RMS}}$
Port 2 frequency	$f_g = 50$ Hz
Port 2 voltage	$V_{P1} = 13.8\ \text{kV}_{\text{RMS}}$
Switching frequency	$f_s = 2000$ Hz
DC sub-module voltage	$V_{DC} = 4000$ V
Number of sub-modules	$n = 6$
Sub-module bus capacitance	$C_{SM} = 500\ \mu$F
Grid line inductances	$L_g = 1.0$ mH
Arm circulating inductances	$L_c = 100\ \mu$H

Here, we present the experimental results obtained with the FPGA-based control board and the OPAL hardware-in-the-loop. The results considering the steady-state operation of the converter are presented first, and the transient response performance is presented last.

5.1. Steady-State Operation

Figure 7 shows the voltages in the converter ports. It is possible to observe the three-phase voltages that are imposed in the Hexverter ports.

Figure 8 shows the currents in the converter ports. It is possible to observe the three-phase currents, which are regulated by the control, in the Hexverter ports.

The line currents in both ports can be observed, with a nominal value of 209 A and, consequently, a nominal power of 5 MW.

Figure 9 shows one voltage and one current value from each port of the converter, phase A from port 1 and phase R from port two. The active and apparent power per phase (calculated from the phase voltage and line current product) are shown.

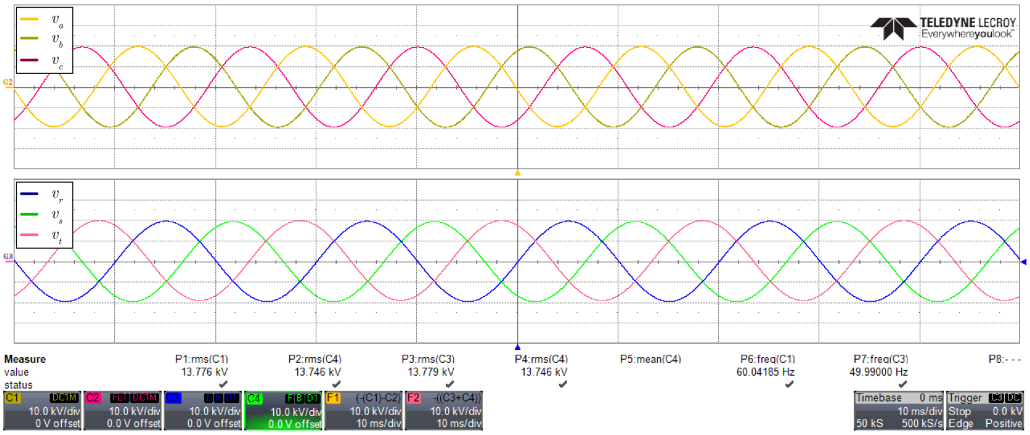

Figure 7. Hexverter line voltages in both ports, where the 13.8 kV rms value is measured in both ports, with a frequency of 60 Hz in port 1 and 50 Hz in port 2.

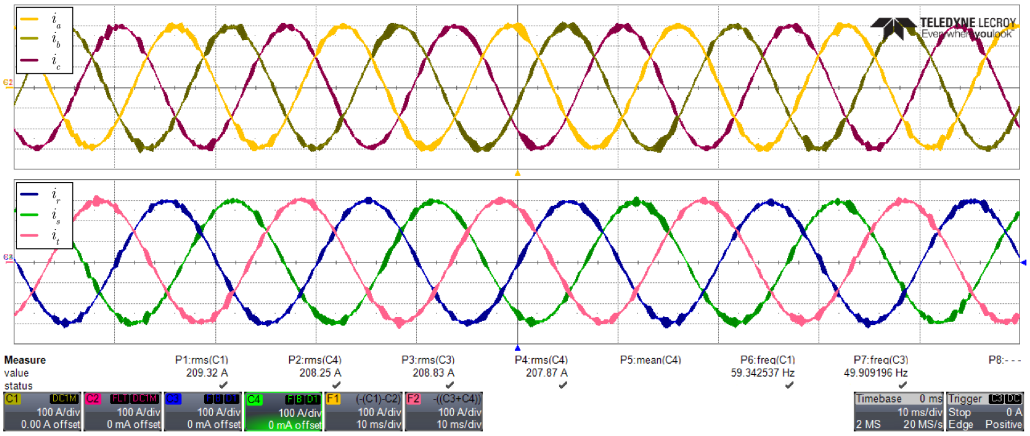

Figure 8. Hexverter line currents in both ports, where the 209 A rms value is measured in both ports, with a frequency of 60 Hz in port 1 and 50 Hz in port 2.

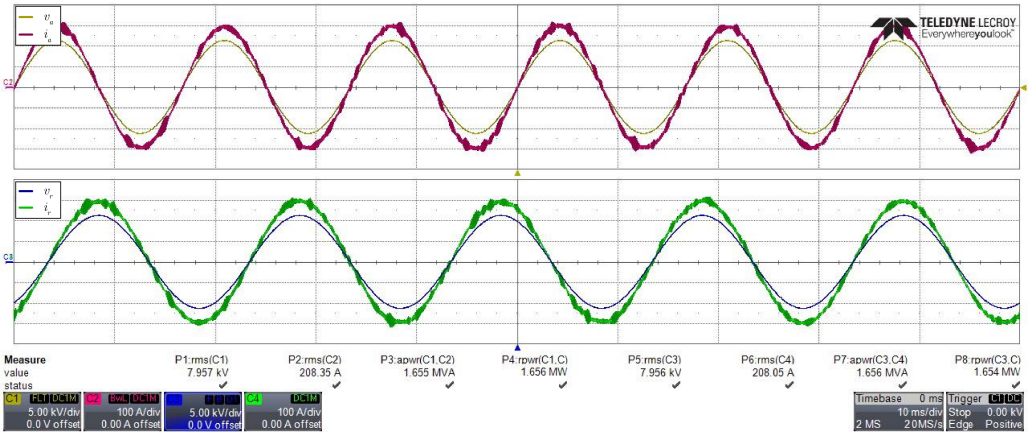

Figure 9. Converter operation with 5 MW power: phase voltage and line current in phase A port 1 and phase R port 2, showing the apparent and active power per phase in each port.

It can be seen that the converter operates with nominal power (5 MW or 1.66 MW per phase) and unit power factor in both ports, as evidenced by the apparent power being approximately equal to the active power.

Figure 10 presents the DC bus voltage from four sub-modules from distinct converter arms. It can be observed that all the sub-modules have approximately the same average voltage (4 kV) and reduced ripple, as shown in detail in Figure 11.

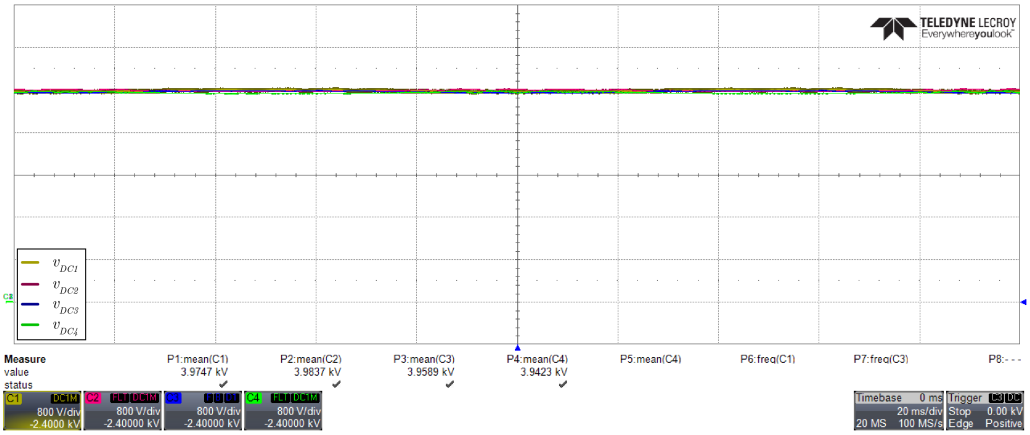

Figure 10. Sub-module DC voltage from four different converter arms.

The sub-module DC voltage ripple is relative to the single-phase power processed by the Hexverter's arms, being basically composed by the frequencies $\omega_1 - \omega_2$, $2\omega_2$, $2\omega_1$, and $\omega_1 + \omega_2$.

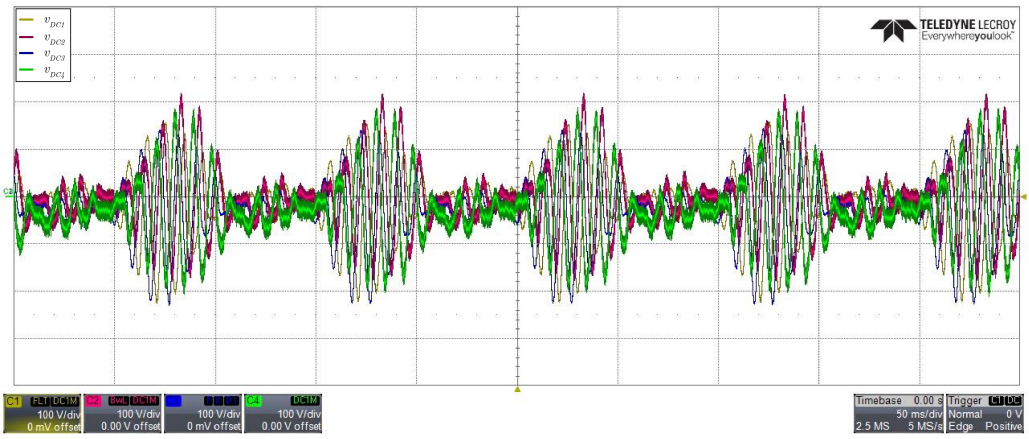

Figure 11. Sub-module DC voltage ripple from four different converter arms, showing only the voltage alternating components.

The synthesized arm voltages are presented in Figure 12, where the voltages of arm 1 and arm 2 are shown, as well as their sum, which is the V_{AB} line voltage.

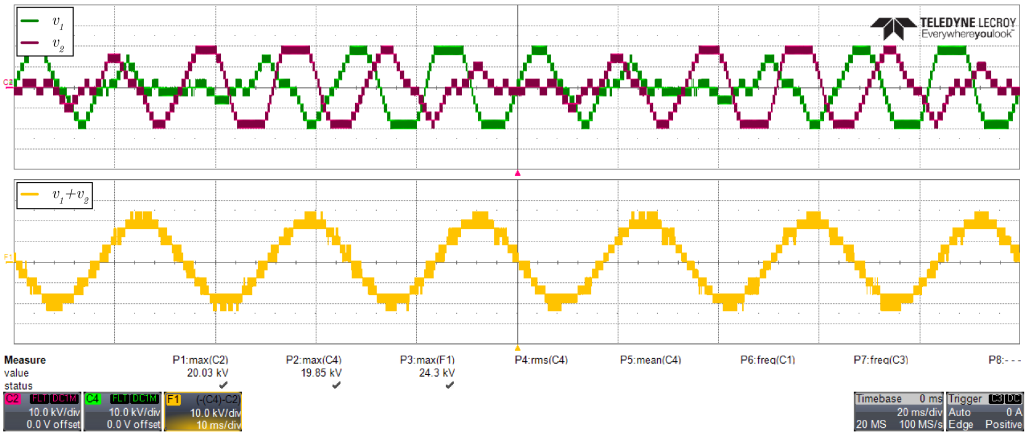

Figure 12. Voltages synthesized by two adjacent Hexverter arms. The sum of both results in the line voltage imposed by the converter.

It can be noted that the maximum voltage imposed by the converter arm is equal to $5V_{DC}$. This reduction of one level is achieved by the third harmonic injection in the

modulation. Without the third harmonic, it would be necessary to use all six levels to achieve the peak voltage demanded to control the port's currents.

Figure 13 shows the Hexverter circulating current for the converter, operating with unit power factor in both ports. In this particular case, the circulating current is relatively small since the imbalance comes from the grid imbalance and deviation of the converter parameters due to the tolerance of the components.

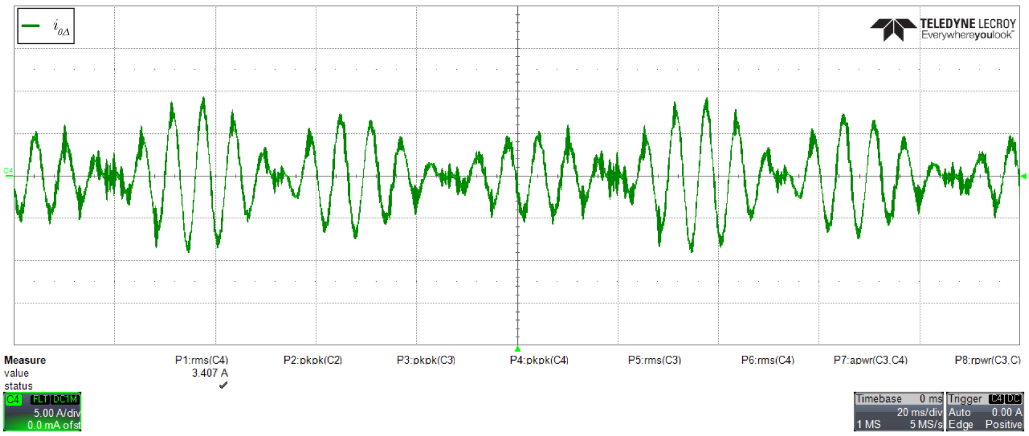

Figure 13. Circulating current in the Hexverter, with the unity power factor in both ports.

In an operating situation with reactive power in one port, the circulating current would increase significantly. In this case, the current circulation in the converter could be reduced by increasing the common mode voltage level (third harmonic). However, to increase the common mode voltage, it would be necessary to increase the total DC bus voltage and eventually have more sub-modules per arm, leading to an over-dimensioned DC bus.

The operation with reactive power is presented in the following figures. It is considered a power factor of 0.9 in port 2, while port 1 operates with a unit power factor.

Figure 14 presents the voltage and currents from phase A (port 1) and phase R (port 2).

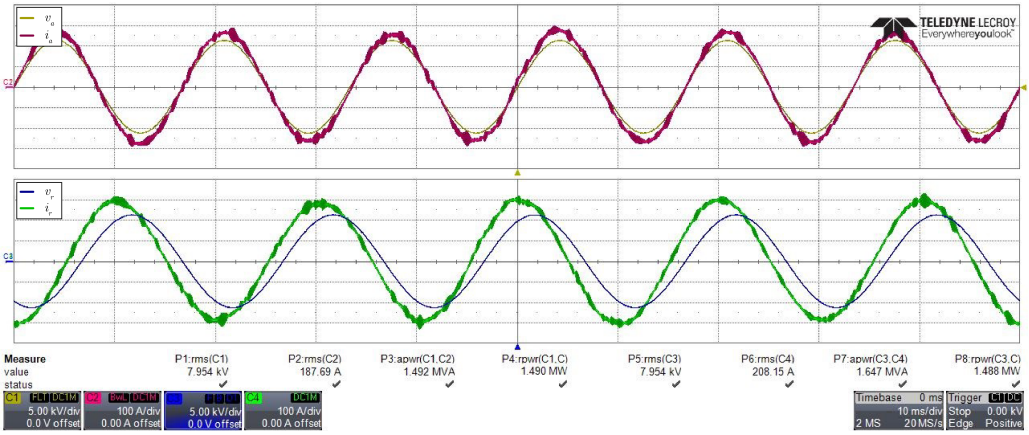

Figure 14. Converter operation with 5 MVA apparent power in port 2 with $\cos(\phi) = 0.9$, and port 1 with 4.5 MW and the unit power factor.

A leading current can be observed in phase R, while the current in phase A is in phase with the voltage.

In this case, as the converter processes reactive power, there is an imbalance in the common mode voltage (V_{0Y}), which is compensated for by increasing the converter circulating current, as depicted in Figure 15.

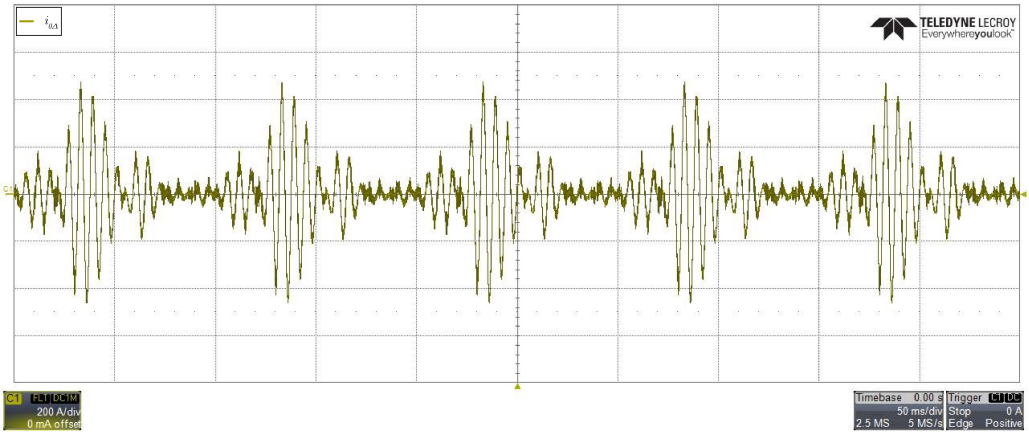

Figure 15. Circulating current for the converter while processing reactive power.

As the common mode voltage is fixed to achieve the minimum DC bus voltage necessary to synthesize the line voltage, a significant increase is implied in the circulating current ($i_{0\Delta}$) to provide balance for the DC buses.

The processing of reactive power also increases the interaction between current and voltage from different ports, which increases the sub-module's DC bus ripple, mainly in the frequency ($\omega_1 - \omega_2$), due to the increase in the oscillating power in this frequency in the arm, as shown in Figure 16.

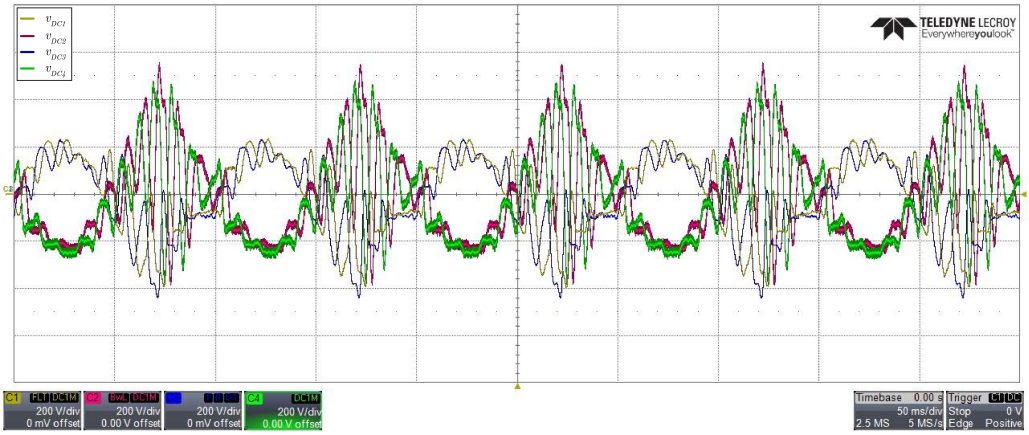

Figure 16. DC voltages from four different sub-modules, considering the operation with reactive power.

5.2. Transient Response

The transient response of the converter to a step in the current reference in port 2 is presented in Figure 17. It can be seen that the converter can achieve a fast current transient response. At the same time, the voltage loop has a slower response.

Figure 18 shows the DC voltages from the converter arms, without the average component.

It can be observed that the voltage is maintained after the transient response. It can also be observed that the ripple increases with the increase in power processed by the converter.

In addition, the control transient response was observed for the converter soft start with a ramp response for port 2. Figure 19 shows the transient response of the port 1 and port 2 currents for the ramp response range from 0% to 100% of power injected into port 2.

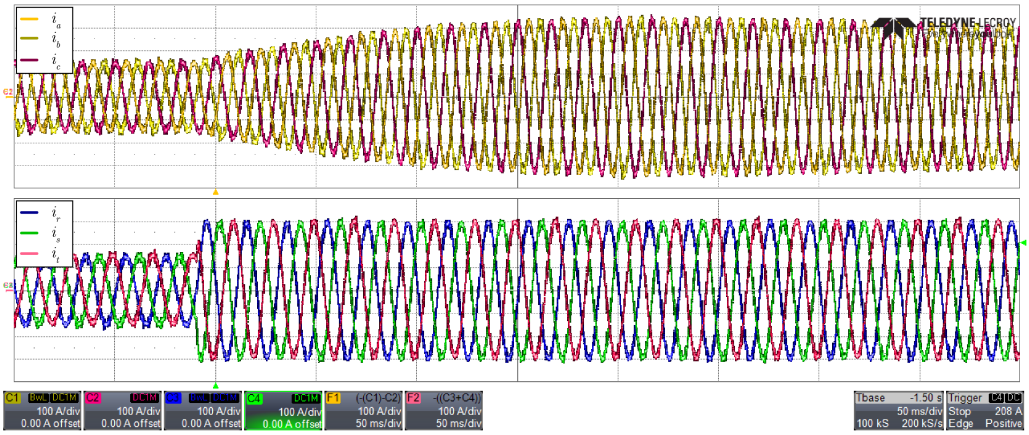

Figure 17. Transient response showing the port currents for a step from 50% to 100% in the power injected in port 2 of the converter.

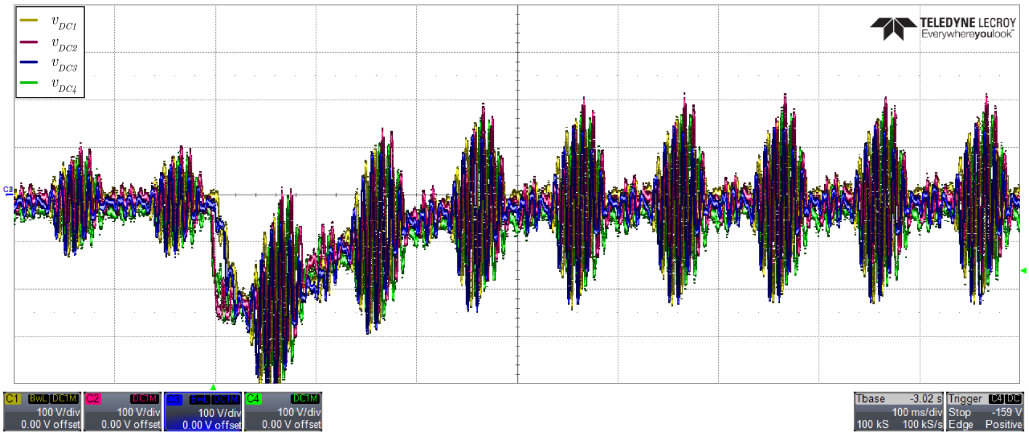

Figure 18. Transient response showing the DC bus voltages for a step from 50% to 100% in the power injected in the port 2 of the converter.

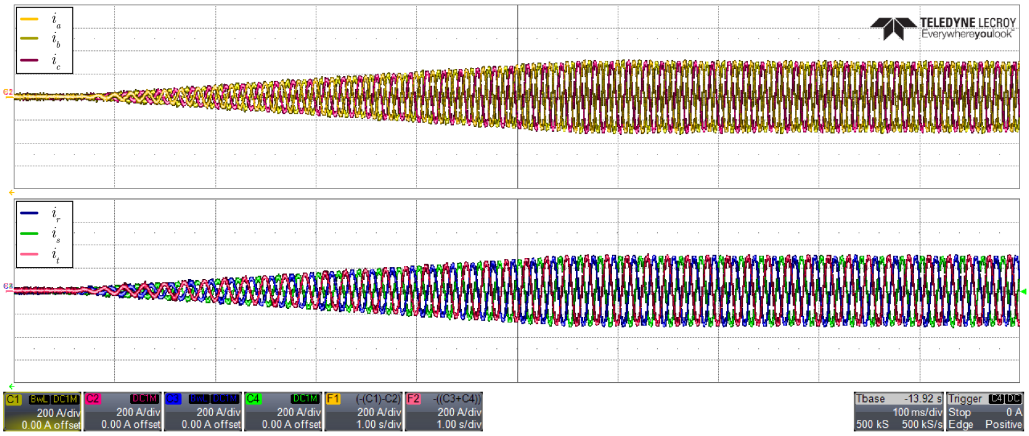

Figure 19. Transient response showing the port currents for a ramp from 0% to 100% of power injected into port 2 of the converter.

The DC bus voltages for the ramp transient response are presented in Figure 20.

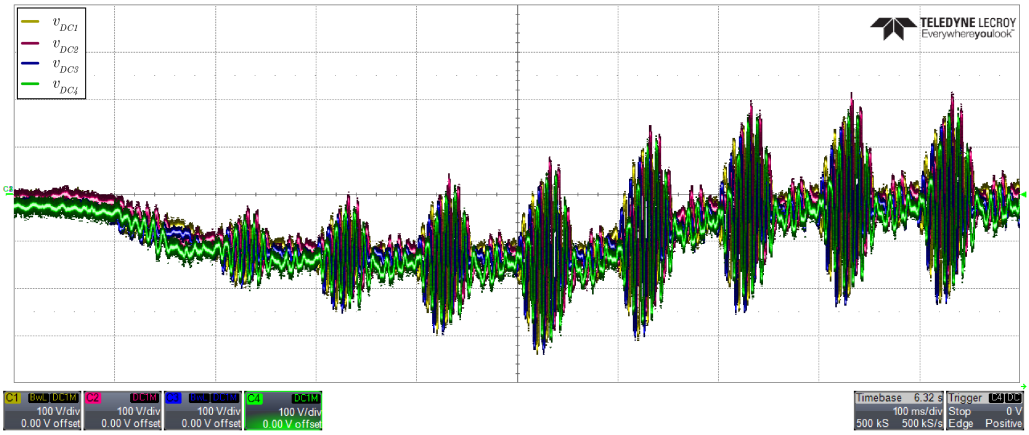

Figure 20. Transient response showing the arms DC voltages for a ramp from 0% to 100% of power injected into port 2 of the converter.

In this case, the sub-modules' DC voltages present a source of constant error during the transient response, achieving voltage regulation after the current in the port reaches its nominal value.

6. Conclusions

This paper presents a modular multilevel AC–AC converter modeled in a synchronous reference frame. The converter transfer functions were obtained, and a control scheme was proposed by employing classic control techniques.

A control strategy was proposed that regulates the currents in both converter ports as well as the circulating current and the DC sub-module bus. The control was validated by real-time emulation, employing the OP-5700 OPAL-RT real-time emulator, providing suitable results. The converter regulated the port currents with reduced harmonic distortion and also regulated the DC bus voltages.

As observed in the experimental results, the injection of the third harmonic allowed the DC bus usage to be maximized. This is an interesting aspect of the control, which allows the total DC bus voltage level to be reduced, or the converter redundancy to be increased, allowing the converter to operate with $n - 1$ sub-modules.

On the other hand, choosing the third harmonic injection to be 1/6 of the voltage amplitude implies the need for a high level of circulating current when the converter operates with different levels of reactive power between the two ports. This might be a limiting characteristic when using the converter in applications such as motor drives.

This could be observed when comparing the circulating currents of the converter operating with unit power factor in both powers (which presented a value of approximately 1% of the arm current). Meanwhile, when the converter operates by processing reactive power ($\cos(\phi) = 0.9$), the circulating current increases to the same level as that of the converter line voltage.

The proposed control strategy is suitable for the operation of a converter with unit power factor in both ports; however, some modifications will eventually be necessary if operation with reactive power processing is considered. Increasing the third harmonic injection would represent a trade-off between the necessary bus voltage and the circulating current amplitude, depending on the reactive power that is processed by the converter.

The main contribution of this paper is the proposal and modeling of a simple Hexverter control strategy with a control scheme for the converter's proper operation, allowing the design of controllers with classical control theory, which is widely known and is employed in various applications. The Hexverter is suitable in most high-power medium-voltage applications, such as wind power generation, medium-voltage motor drives, or connections between two electrical grids with different frequencies.

Author Contributions: Conceptualization, S.A.M. and M.L.H.; Formal analysis, C.A.A., S.A.M. and M.L.H.; Investigation, C.A.A. and M.L.H.; Methodology, C.A.A. and M.L.H.; Software, C.A.A.; Supervision, S.A.M. and M.L.H.; Writing—review & editing, S.A.M. and M.L.H. All authors have read and agreed to the published version of the manuscript.

Funding: The Graduate Program in Electrical Engineering (PPGEEL)—CAPES/PROEX: Code 41001010005P1.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Jung, J.J.; Lee, H.J.; Sul, S.K. Control of the Modular Multilevel Converter for variable-speed drives. In Proceedings of the 2012 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), Bengaluru, India, 16–19 December 2012.
2. Kucka, J.; Baruschka, L. A Hybrid Modular Multilevel DC/AC Converter. In Proceedings of the 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), Geneva, Switzerland, 8–10 September 2015.
3. Tai, B.; Gao, C.; Liu, X.; Chen, Z. A Novel Flexible Capacitor Voltage Control Strategy for Variable-Speed Drives with Modular Multilevel Converters. *IEEE Trans. Power Electron.* **2016**, *8993*, 128–141. [CrossRef]
4. Marquardt, R. Modular Multilevel Converter topologies with DC-Short circuit current limitation. In Proceedings of the 8th International Conference on Power Electronics—ECCE Asia, Jeju, Korea, 30 May–3 June 2011.
5. Alhasnawi, B.N.; Jasim, B.H.; Issa, W.; Esteban, M.D. A Novel Cooperative Controller for Inverters of Smart Hybrid AC/DC Microgrids. *Appl. Sci.* **2020**, *10*, 6120. [CrossRef]
6. He, L.; Zhang, K.; Xiong, J.; Fan, S.; Xue, Y. Modular multilevel converter with full-bridge submodules and improved low-frequency ripple suppression for medium-voltage drives. In Proceedings of the 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, USA, 15–19 March 2015.
7. Zhang, J.; Li, L.; Dorrell, D.G. Control and applications of direct matrix converters: A review. *Chin. J. Electr. Eng.* **2018**, *4*, 18–27.
8. Belhaouane, M.M.; Ayari, M.; Guillaud, X.; Braiek, N.B. Robust Control Design of MMC-HVDC Systems Using Multivariable Optimal Guaranteed Cost Approach. *IEEE Trans. Ind. Appl.* **2019**, *55*, 2952–2963. [CrossRef]
9. Baruschka, L.; Mertens, A. A new 3-phase direct modular multilevel converter. In Proceedings of the 2011 14th European Conference on Power Electronics and Applications, Birmingham, UK, 30 August–1 September 2011.
10. Kolb, J.; Kammerer, F.; Schmitt, A.; Gommeringer, M.; Braun, M. The Modular Multilevel Converter as Universal High-Precision 3AC Voltage Source for Power Hardware-in-the-Loop Systems. In Proceedings of the PCIM Europe 2014, Nuremberg, Germany, 20–22 May 2014.
11. Schmitt, A.; Gommeringer, M.; Rollb, C.; Pomnitz, P.; Braun, M. A Novel Modulation Scheme for a Modular Multiphase Multilevel Converter in a Power Hardware-in-the-Loop Emulation System. In Proceedings of the IECON 2015—41st Annual Conference of the IEEE Industrial Electronics Society, Yokohama, Japan, 9–12 November 2015.
12. Kotsampopoulos, P.C.; Lehfuss, F.; Lauss, G.F.; Bletterie, B.; Hatziargyriou, N.D. The Limitations of Digital Simulation and the Advantages of PHIL Testing in Studying Distributed Generation Provision of Ancillary Services. *IEEE Trans. Ind. Electron.* **2015**, *62*, 5502–5515. [CrossRef]
13. Karwatzki, D.; Baruschka, L.; Mertens, A. Survey on the Hexverter topology—A modular multilevel AC/AC converter. In Proceedings of the 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), Seoul, Korea, 1–5 June 2015.
14. Blaszczyk, P. Hex-Y—A New Modular Multilevel Converter Topology for a Direct AC–AC Power Conversion. In Proceedings of the 2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe), Riga, Latvia, 17–21 September 2018.
15. Robles-Campos, H.R.; Mancilla-David, F. Detailed Assessment of Modulation Strategies for Hexverter–Based Modular Multilevel Converters. *Energies* **2022**, *15*, 2132. [CrossRef]
16. Zhang, C.; Jiang, D.; Zhang, X.; Chen, J.; Ruan, C.; Liang, Y. The Study of a Battery Energy Storage System Based on the Hexagonal Modular Multilevel Direct AC/AC Converter (Hexverter). *IEEE Access* **2018**, *6*, 43343–43355. [CrossRef]