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Low-Frequency-Noise Reduction Technique for Linear Analog CMOS IC's

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KURZFASSUNG

Die Dissertation untersucht ein neues Verfahren zur Reduktion des niederfrequenten Rauschens in linearen analogen CMOS Schaltungen. MOSFETs, welche periodisch zwischen Akkumulation und Inversion geschaltet werden, zeigen ein gegenüber konstanten Arbeitspunkten reduziertes 1/f-Rauschen. Unter Ausnützung dieses physikalischen Effektes wird mit Hilfe im Rahmen der Dissertation entwickelter Schaltungstechnik eine Unterdrückung der Rauschleistung von bis zu 8dB erreicht. Die Auswirkungen der dazu notwendigen Eingriffe in eine typische lineare analoge Schaltung werden exemplarisch an einem Miller-Operationsverstärker untersucht. Dabei werden bei richtiger Dimensionierung der Schaltung keine wesentlichen Beeinträchtigungen in den Schaltungsparametern festgestellt. Die für das Verfahren wichtigen Schaltungsparameter werden im Rahmen der Arbeit diskutiert.

ABSTRACT

For AMS (analog-mixed signal) and RF (radio frequency) implementations CMOS (Complementary Metal Oxide Semiconductor) technology platforms are the mainstream today. These platforms provide great density and power savings on digital parts on the same chip and, in addition, a good mix of components for analog design. The analog performance of CMOS technology is worse compared to other technology options (e.g. bipolar technology), and its major advantage is the lower total cost of system. Several drawbacks have to overcome to build high performance analog integrated circuits using CMOS technology. One of those drawbacks is the poor 1/f noise property of CMOS technology.

Recently, but about ten years after this effect was first reported by Bloom and Nemirovsky of Technion-Israel Institute of Technology in Israel, the AMS/RF engineers began to pay an attention to a device-physics related effect: the periodical on-off switching of a MOSFET between strong inversion and accumulation leads to an anomalous reduction of the intrinsic 1/f noise of those devices. Especially, B. Nauta's group of Twente University in the Netherlands has been exploring its feasibility in a large signal circuits like VCO's. Although they seem to be the first to make use of the device-physics for the "real engineering world," they have not fully exploited the advantage of it. Direct use of the effect based on their evaluations is only feasible for a limited amount of circuits, where a bias current is needed only during certain time intervals or where signal processing is not taking place continuously.

The aim of this thesis is to present and to develop a principle for the 1/f noise reduction in linear analog CMOS IC's, using the known device physics-based effect which is aimed to be used in all kind of circuits including linear and time continuous circuits. This thesis describes the mathematical modeling, physical implementation and experimental demonstration of the principle in the fulfillment of this aim. In a first step, we propose the principle, "the complementary switched MOSFET architecture." Then, as an application example for the principle, we investigate an operational amplifier architecture which includes the principle. It is modified from a two-stage CMOS miller operational amplifier and later compared to a classical design of that class.

The principle is experimentally demonstrated in a standard 0.12 µm, 1.5 V digital CMOS technology and a threefold reduction (5dB) of the 1/f noise is achieved at 10 Hz compared to a reference circuit. The impact of the circuit performances is minor – e.g., a slight increase (6%) of the power-consumption, a slight degradation (1dB DC gain) of the open-loop ac characteristics and no significant change in the linearity (THD) of the architecture. The switching glitches, which originate from the principle, are easily suppressed by a first order low pass filter. In addition, the property of the 1/f noise reduction principle is investigated under various clock frequencies and off-voltages. Furthermore, the mathematical descriptions for the noise behavior and the signal transfer of the proposed operational amplifier architecture are derived. With the help of the derived equations, the distinct features of the principle are identified from the measurements and simulations: the noise aliasing due to the principle and the increase in the white noise plateau which attributes to thermal resistive noise increase of the switches with increasing clock frequency. Finally, it is noted that the clock mismatch parameter t_p should be optimized for best electrical performance.

The proposed principle is more area-effective compared to the most simple 1/f noise reduction method, the increase of an active area of noisy transistors. A twofold area increase of a transistor only leads to a factor of two in reduction of its 1/f noise, but the proposed circuit implementations yields a factor of three. This reduction factor is further enhanced to six with a proper noise-care design approach. Compared to the standard industry approach of chopper stabilization for 1/f noise reduction, less energetic glitches arise and thus less glitches have to be suppressed avoiding a higher order low pass filters which increases the complexity of circuits. Compared to the technique of correlated double sampling, the same increase in the white noise plateau is observed. This technique finds its main application in a discrete signal processing system like sampled-data or sample and hold circuits, so that the use of this technique to a continuous signal processing system is reluctant.

Results from this work should give a good guideline to AMS/RF circuit designers on how to best implement the noise reduction principle into their circuits.

TABLE OF CONTENTS

CHAPTER 1
INTRODUCTION

1.1 MOTIVATION

The evolution of VLSI (very large scale integration) technology has developed to the point where millions of transistors can be integrated on a single die or chip. Where integrated circuits once filled the role of subsystem components, partitioned at analog-digital boundaries, they now integrate complete systems on-a-chip by combining both analog and digital functions [1]. CMOS (Complementary Metal Oxide Semiconductor) technology platform is today's mainstream in AMS (analog-mixed signal) /RF (radio frequency) implementation. This platform provides great density and power savings on digital parts on a chip and, in addition, a good mix of components for analog design. Up to date the analog performances of CMOS technology platform has been regarded to be inferior to those of other cost-consuming technology platform like bipolar or GaAs process. But the remarkable enhancements of analog performance of CMOS technology are achieved today by the continuous down-scaling and increased process robustness. Furthermore it is still on-going and accelerating. Table 1.1 indicates that scaling-down of CMOS technology nodes today as well as in the foreseeable future will result in the enhancement of AMS/RF performances of devices [2]. Although the advantages of CMOS technology are well established and the analog performances are comparable to the other processes, there exists a major drawback for analog/RF applications: CMOS technology is extremely “noisy”: This is especially the case when the 1/f noise of CMOS technology is compared to that of bipolar technology. Although process optimization of this poor 1/f noise property has been made in terms of improvement of quality of SiO_2 - the 1/f noise of MOSFET relates its physical origin to random trapping and detrapping of a charge carrier by a trap between Si and SiO_2 [3]. - , even the so-called analog low noise CMOS technology shows much higher 1/f noise as shown in Figure 1.1.

This poor 1/f noise property of CMOS technology renders analog circuit designer reluctant to use this technology. When he gets decided to adopt such "noisy" CMOS technology platform, he faces a formidable challenge: how to design low noise AMS/RF functional blocks, taking advantages of the unique features of the technology and reducing the 1/f noise, or the so-called low frequency noise, by using appropriately the available design parameters. There exist several 1/f noise reduction techniques in CMOS circuits including a conventional method, enlarging of an active area of a MOSFET based on the 1/f noise property: inversely proportional to the active area. This method is quite simple to implement but loose a unique advantage of the technology down-scaling, a performance enhancement (e.g., cut-off frequency enhancement) in a short-gate-length device [4]. The most prominent examples of the 1/f noise reduction techniques for analog circuit design are correlated double sampling (CDS) and chopper stabilization (CHS) [5]. These techniques, nowadays, are industry standard and are known to be quite effective in reducing 1/f noise. But both techniques are restricted to low frequency circuits application and do not reduce the 1/f noise itself [6]. Recently, the AMS/RF circuit designers began to pay an attention to a device-physics related effect: the periodical on-off switching of a MOS transistor between strong inversion and accumulation leads to a anomalous reduction of the intrinsic 1/f noise of those devices [7].

Year	2001	2004	2007	2010	2013	2016
Technology node	130nm	90nm	65	45	32	22
Digital Supply Voltage (V)	0.9-1.3	0.7-1.0	0.5-0.7	0.4-0.6	0.3-0.5	0.3-0.4
Analog Supply Voltage (V)	3.3-1.8	2.5-1.8	2.5-1.8	1.8-1.0	1.8-1.0	1.5-1.0
NMOS Analog Speed Devices						
F_{max}(GHz)	160	175	190	200-230	230-260	260-290
g_m/g_{ds} at $10*L_{min\text{-}digital}$	100	100	100	100	100	100
Input 1/f noise (uV^2um^2/Hz)	500	300	200	150	100	75
3σ V_{th} matching (mVum)	15	12	9	3	2.5	2.0
NMOS Analog Precision Devices						
Analog V_{th} (V)	0.5-0.2	0.4-0.2	0.4-0.2	0.3-0.1	0.3-0.1	0.2-0.1
g_m/g_{ds} at $10*L_{min\text{-}digital}$	200	200	200	200	200	200
Input 1/f noise (uV^2um^2/Hz)	500	500	300	150	100	100
3σ V_{th} matching (mVum)	21	15	15	9	9	7.5

Table 1.1 Projected mixed-signal design parameters necessary for continuous design process [1]

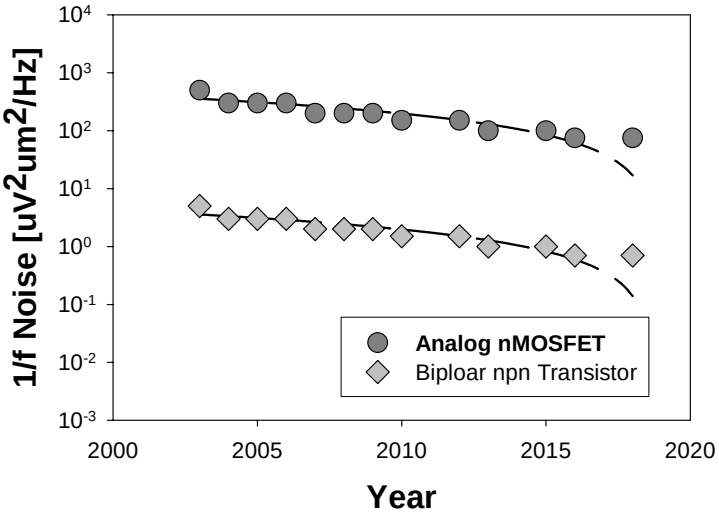

Figure 1.1 International Technology Roadmap for semiconductor 2004 for the 1/f noise [2]

This effect is first reported by Bloom and Nemirovsky of Technion-Israel Institute of Technology in Israel in 1991. Shortly after, their results were reconfirmed and related to RTS (Random Telegraph Signals), which plays a key role in generation of the 1/f noise [8]. In 1999 Klumperink of B. Nauta's group of Twente University in the Netherlands experimentally rediscovered the effect in ring oscillator phase noise measurements [9]. They seem to be the first to exploit its impact on CMOS circuits, achieving a twofold reduction of the $1/f^3$ contribution to the phase noise. And shortly after, they have proposed a 1/f noise reduction technique in large-signal circuits like VCO's, where a bias current is needed only during certain time intervals or where a signal processing is not taking place continuously. Although they seem to be the first to make use of the device-physics for the "real engineering world," they have not fully exploited the advantage of it. Direct use of the effect based on their evaluation is only feasible those limited amount of circuits. This gives the motivation of this work, to enhance the range of possible use of the effect to all kinds of circuits, especially including linear analog CMOS IC's for a continuous small signal processing. In linear continuous signal processing circuits, the active element most often used is the operational amplifier, whose main function in the circuit is to create a virtual ground, i.e., a node with a zero or constant voltage at its input terminal without sinking any current. Using op amps with MOSFET, the op amp input current at low frequencies can indeed be made extremely small. But a major drawback arises: the input voltage of a practical op amp is significantly large, typically in the order of 1 – 10 mV. This is because the CMOS op amp is easily affected by several non-ideal effects: 1/f noise and thermal noise and as well as the input referred dc offset voltage due to mismatch between input MOSFETs. Normally the thermal noise occupies a wide frequency band, whereas the 1/f noise and dc offset are narrowband low-frequency signals. Among the low-frequency narrowband imperfections, the 1/f noise is of the most significance, especially in linear analog CMOS IC's [10]

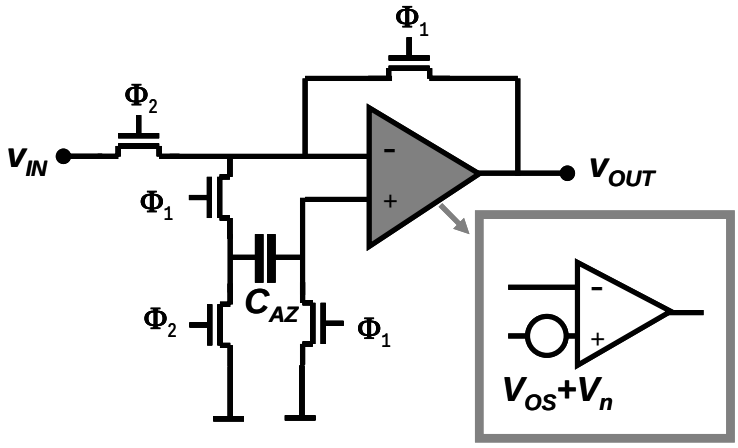

Figure 1.2 Example of the correlated–double sampling technique in an operational amplifier. The inlet indicates a simple model of an operational amplifier including the offset voltage V_{os} and the noise voltage V_n [11]

1.2 RELATED / PREVIOUS WORK

In this section, known and relevant circuit techniques for 1/f noise reduction in CMOS IC's will be reviewed briefly, in order to make a clear distinction between these techniques and the proposed technique for 1/f noise, which is presented in Chapter 3.

1.2.1 CDS & CHS TECHNIQUES

The most prominent examples of 1/f-noise reduction techniques in analog IC's are correlated double sampling (CDS) and chopper stabilization (CHS). While CDS technique is based on the sampled switched capacitor technique, the CHS technique depends on modulation rather than sampling, which has some major consequence on the performance [4].

The fundamental idea of the CDS technique is to sample the unwanted quantity (offset and 1/f noise) of the amplifier in an autozero phase (on the phase of Φ_1 in the Figure 1.2); while in the amplification phase (on the phase of Φ_2 in the Figure 1.2) it is held and subtracted form the input signal. If the noise is constant over time like a dc offset, it will be cancelled, as needed in a high-precision amplifier or high-resolution comparator. If the unwanted disturbance is 1/f noise, it will be high-pass filtered and thus strongly reduced at low frequencies but at the cost of an increased noise floor due to aliasing of the wideband noise inherent to the sampling process. This process requires at least two phases: a sampling phase Φ_1, during which the offset voltage V_{os} and the noise voltage V_n are sampled and stored, and a signal-processing phase Φ_2, during which the offset-free stage is available for operation. This technique takes advantage of the CMOS technology to memorize the existing defects like offset and 1/f noise on a storage capacitor.

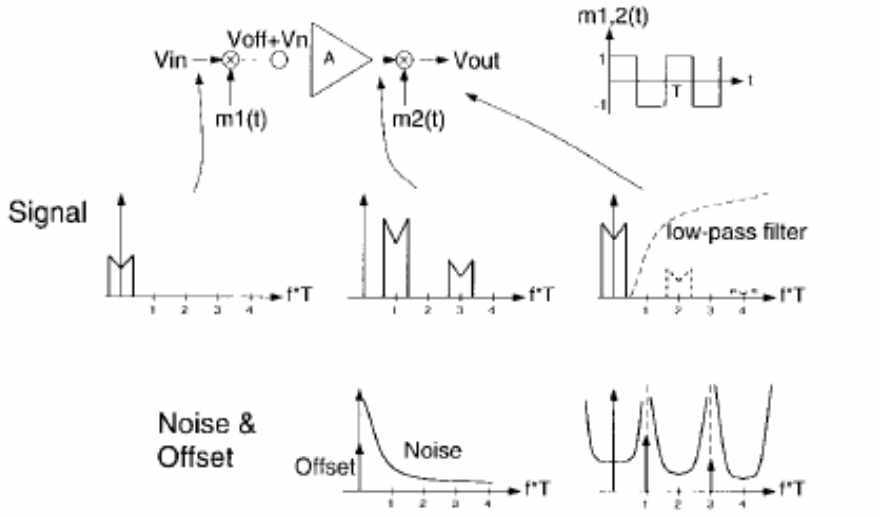

Figure 1.3 Principle of the Chopper technique. Picture is taken from [12]

This offset cancellation scheme is not only useful to reduce the offset of the amplifier, but is also capable of removing 1/f noise due to the strong correlation of two consecutive samples [12]. Although this CDS technique, first applied in the read-out circuitry to charge coupled devices [13], may substantially reduce the 1/f-noise, a dramatic increase of the thermal noise level must be taken into account, due to unavoidable under-sampling of broadband noise of the switches and the operational amplifier [14]. Furthermore, the offset reduction is limited by charge injection of the switches, which can be reduced to a certain extent by the use of some more elaborate circuit schemes [15]. CDS technique is more preferable in applications, which inherently use sampled-data circuits such as switched capacitor stages, so that the base-band noise behaviour is not made worse by noise aliasing [5].

Figure 1.3 describes the essential idea of the CHS technique, which combines the amplifier with two modulators at the input and output. The input signal is first frequency-shifted in the input modulator to higher frequencies, where the subsequent CMOS amplifier is free from 1/f noise, is then amplified and shifted back to its original frequency in the second modulator. In contrast to the signal, the offset and 1/f-noise of the amplifier between the modulators are only modulated once by the second modulator and translated to higher frequencies. Unlike the CDS technique, the chopper stabilization technique does not introduce any aliasing of broadband noise, which for CHS technique causes the power spectral density in the baseband to increase proportionally to the ratio of the noise bandwidth and sampling frequency. This large energy arising from chopping frequency, which is restricting the usable signal bandwidth, requires high order filter to be removed. This is a major drawback of CHS technique and the use of it in operational amplifiers is reluctant. Apart from these, CHS and CDS are limited to use in bandwidth. These techniques make only use of the non-diminishing auto-correlation function of non-white noise to predict its actual value based on the previous one. They do not help to reduce the 1/f noise “itself” [4].

1.2.2 SWITCHED BIAS TECHNIQUE

The impact of 1/f noise reduction phenomena on a CMOS circuit, using the periodically on-off switching of a MOSFET between an operational state (strong inversion) and a rest-state (accumulation) is first exploited by Klumperink of Twenete University in Netherlands in 1999. This is most relevant to the proposed principle in this thesis. His principle is named "the switched bias technique" and, is demonstrated on circuits for large signal application like VCO's (Voltage Controlled Oscillator) [16]. His principle is only feasible in a circuit, where a bias current is needed only during certain time intervals or signal processing is not taking place continuously. Oscillators are among these circuits and, in many types of an oscillator; the transistors contribute actively to the circuit's operation during only a fraction of the period of oscillation. The feasibility of the technique was demonstrated in an integrated CMOS 6-stage coupled saw tooth oscillator running at 120 kHz. Each ring stage subsequently produces a rising voltage ramp across a capacitor. The noise, which is present on the capacitor's charge current, now appears to be the dominant contributor to phase noise in the coupled saw tooth oscillator. At low frequencies, noise dominates the phase-noise performance.8 dB reduction of the 1/f noise induced phase noise is achieved, while the power consumption is reduced by more than 30%.

Implementing this technique is expected to be rather straightforward in "only" discrete-time circuits (e.g., PLL's, frequency dividers, mixers, sample-and-hold circuits, switched capacitor, switched op-amp, etc.). This technique is "not" suitable for a continuous signal processing circuits like an operational amplifier.

1.3 SCOPE

The aim of this thesis is to present a novel principle for the 1/f noise reduction technique in linear analog CMOS IC's, which is suitable for a continuous signal processing operation using the device physics-based effect. As well as the novel 1/f noise reduction technique, its impact on the performance of linear analog CMOS IC's should be exploited.

The contents of the thesis are organized in the following to fulfil these aims: Chapter 2 is concerned with noise phenomena, the intrinsic device noise in a MOSFET. First the mathematical properties of noise are briefly reviewed, which is statistically a random process. Based on the knowledge of noise properties, a physical origin of four main types of noise - shot noise, thermal noise, generation-recombination noise and 1/f nose- in a MOSFET is discussed. Subsequently a general noise macro model of a MOSFET and a circuit is introduced for a detailed noise analysis and simulation. At the end of this chapter, critical issues in measuring of 1/f noise are discussed and a relevant measurement setup for the proposed 1/f noise reduction principle in a linear analog CMOS ICs is presented. Chapter 3, which presents the central idea of this thesis, deals with the proposed principle for the 1/f noise reduction technique in linear analog CMOS IC's, which is suitable for a continuous signal processing operation by using the device physics-based effect : the periodically on-off

switching of a MOSFET. First the known 1/f reduction device physics-effect is detailed reviewed with introducing the recent explanations from literatures. And then, the 1/f noise reduction principle, “complementary switched MOSFET architecture” is proposed for a linear CMOS analog IC. To illustrate the noise behavior of the 1/f noise reduction principle, a mathematical description is presented. As an application of the principle to a linear CMOS analog IC, we propose a modified two stage CMOS miller operational amplifier which includes the proposed principle. Since the signal transfer is of a great concern in a linear CMOS analog IC, this is deeply discussed with a mathematical description. Chapter 4 deals with several issues in the design-consideration and physical implementation of the principle in the two stage CMOS miller operational amplifier. These design-examples are fabricated in a standard digital 0.12 um, 1.5V CMOS technology from Infineon Technologies AG. Subsequently, in Chapter 5, the principle is experimentally demonstrated. The impact of the principle on the performance of linear analog CMOS IC’s is investigated in terms of total harmonic distortion (THD) and power-supply rejection (PSR). Furthermore the thermal noise and related noise aliasing effects, which inherently arise from the proposed principle, on the noise performance of the IC is discussed. In Chapter 6 the work is concluded with a summary.

1.4 REFERENCES FOR CHAPTER 1

[1] R. Brederlow, W. Weber, S. Donnay, P. Wambacq, J. Sauerer, and M. Vetregt, "A Mixed-Signal Roadmap for the international Technology Roadmap for Semiconductor," IEEE Design and Test for Computers vol. 18, pp. 34-46, 2001

[2] International Technology Roadmap for Semiconductors 2004 Edition, ITRS, http://public.itrs.net/Files/2004ITRS/Home2004.htm, 2004

[3] R. Brederlow, W. Weber, R. Jurk, C. Dahl, S. Kessel, J. Holz, W. Sauert, P. Klein, B. Lemaitre, D. Schmitt-Landsiedel, and R. Thewes, "Influence of Fluorinated Gate Oxides on the Low Frequency Noise of MOS Transistors under Analog Operation," Proceedings of the 28th European Solid-State Device Research Conference, pp. 329-331, 1997

[4] K. Laker and W. Sansen, Design of Analog Integrated Circuits and Systems, Boston, McGrow-Hill, 1994

[5] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: auto zeroing, correlated double sampling and chopper stabilization," Proceedings of the IEEE, Vol. 4, pp.1584-1614, 1996

[6] A. P. van der Wel, E. A. M. Klumperink, S. L. J. Gierkink, R. F.Wassenaar, and H. Wallinga, "MOSFET 1/f noise measurement under switched bias conditions," IEEE Electron Device Letters, vol. 21, pp.43–46, 2000

[7] I. Bloom and Y. Nemirovsky, "1/f Noise Reduction of Metal-Oxide-Semiconductor Transistors by cycling from inversion to accumulation," Applied Physics Letters, vol. 58, pp.1664-1666, 1991

[8] B. Dierickx and E. Simoen, "The Decrease of Random Telegraph Signal Noise in Metal-Oxide-Semiconductor Field-Effect Transistors when cycled from inversion to accumulation," Journal of Applied Physics, vol. 71, pp. 2028-2029, 1992

[9] E. A. M. Klumperink, S. L. J. Gierink, A. P. Van der Wel and B. Nauta, "Reducing MOSFET 1/f noise and power consumption by switched biasing," IEEE Journal of Solid-State Circuits, Vol. 35, No. 7, pp. 994-1001, 2000

[10] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: auto zeroing, correlated double sampling and chopper stabilization," Proceedings of the IEEE, vol. 4, pp. 1584-1614, 1996

[11] P. E. Allen and D. R. Holberg, CMOS analog circuit design, New York, Oxford University Press, 1987

[12] K.-C. Hsieh, P. R. Gray, D. Senderowicz, and D. G. Messerschmitt, "A low-noise chopper-stabilized differential switched-capacitor filtering technique," IEEE Journal of Solid-State Circuits, vol.16, pp.708–715, 1981.

[13] C. C. Enz, E.A. Vittoz, and F. Krummenacher, "A CMOS chopper amplifier," IEEE Journal of Solid-State Circuits, vol. 22, pp.708–715, 1987.

[14] C. Menolfi and Q. Huang, "A low-noise CMOS instrumentation amplifier for thermoelectric infrared detectors," IEEE Journal of Solid-State Circuits, vol. 32, pp.968–976, 1997.

[15] I. Abe, J. Sugisaki, E. Nakazoe, and Z. Abe, "An ultra-low drift amplifier using a new type of series-shunt MOSFET chopper," IEEE Transaction on Instruments and Measurements, vol. 34, pp.54–58, 1985.

[16] S. L. J. Gierkink, E.A.M. Klumperink, A.P. van der Wel, G. Hoogzaad, A.J.M. van Tuijl, and B. Nauta, "Intrinsic 1/f device noise reduction and its effect on phase noise in CMOS ring oscillators," IEEE Journal of Solid-State Circuits, vol. 34, pp.1022–1025, 1999.

CHAPTER 2

FUNDAMENTALS OF NOISE

When we try to measure a weak signal, a lower limit is always set by the spontaneous fluctuations of the current, voltage, and other physical variables. And, when we are e.g. doing wireless communications, the information signal is always affected by other disturbances. These spontaneous or unexpected fluctuations are always unwanted and, of course, they are to be avoided. These are examples of noise and noise, in a broad sense, can be defined as any unwanted disturbance that interferes with a desired signal.

Noise is classified into two categories: artificial noise and intrinsic noise. Artificial noise is caused by numerous noise sources from environment. Examples are electrostatic and magnetic coupling between a circuit and ac power line, crosstalk between adjacent circuits, hum from dc power supplies and so forth. Intrinsic noise is generated in a device or circuit itself by the device-physics-related noise mechanism, the fluctuation of carrier number. Such for a MOSFET are shot, thermal, generation-recombination and 1/f noise. All electronic devices generate its own intrinsic noise and other devices operating on a same circuit also can induce noise. Artificial noise is, to some extent, eliminated by adequate shielding, filtering, or by changing the layout of circuit components. However, once a fabrication process of a chip is decided, intrinsic noise can be rarely reduced. The word “noise” in this thesis is limited to a use for representing the intrinsic noise which is randomly generated in a MOSFET.

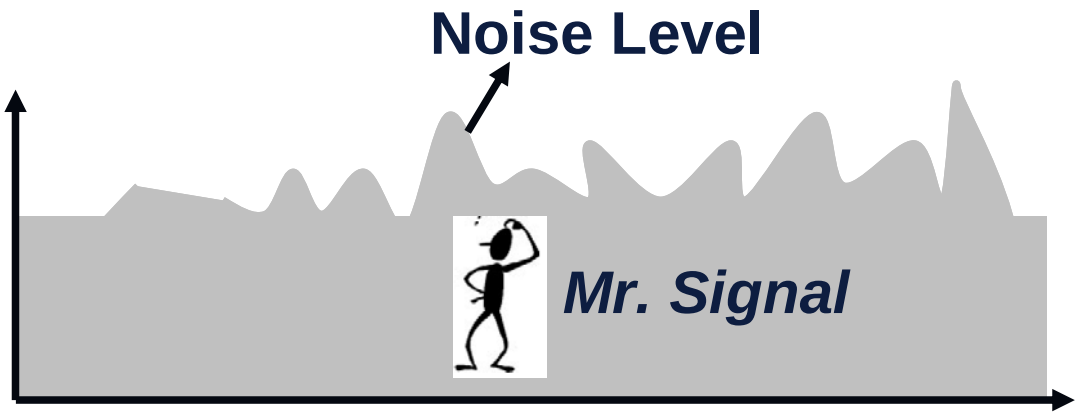

Figure 2.1 Noise limits the minimal signal level that a circuit can process with acceptable quantity.

2.1 STATISTICS OF NOISE

Noise is a totally stochastic process, which is a randomly varying function of time. The instantaneous amplitude of noise can not be predicted, but only the randomness of noise is predicted or estimated using statistical approaches. Most important of them are an average value of noise quantity and a related standard deviation. Noise is mathematically represented in a form of power spectral density and this is derived from autocorrelation functions, which are given by standard deviation of noise [1].

The average value represents a mean value of noise variables. Two ways of defining an average are popular used, which are a time average and an ensemble average. The time average of a variable *x(t)*, which is randomly varying in time *t*, for the averaging time *T* is defined as

$$\bar{x} = \frac{1}{T}\int_0^T x(t)dt \tag{2.1}$$

The time average is more directly related to real experiments. Sometimes an ensemble average is a convenient theoretical concept, since it is directly related to the probability density functions, which is more powerful and useful in dealing with countless number of noise events. If x_i is the output of the i_{th} source, the ensemble average of a random noise variable x at $t = t_1$ is defined by

$$\bar{x} = \frac{1}{N}\sum_{i=1}^{N} x_i \tag{2.2}$$

Averaging just gives a mean value of the variable and does not explain how large the fluctuation of the variable (noise) is. Variance gives this information, actually how far a quantity deviates from the mean value. Noise is mathematically expressed in the form of power spectral density. The power spectral density of a noise process is derived from the autocorrelation function, which describes the correlation strength between a random variable x at a certain time t and the same variable at a certain delay time of τ after t. Equation 2.3 describes the autocorrelation function.

$$\varphi_x(\tau) = \frac{1}{T} \int_{-T/2}^{T/2} x(t) \cdot x(t+\tau) dt \tag{2.3}$$

Now the power spectral density $S_o(f)$ is obtained thanks to Fourier Transformation of Equation 2.3 as

$$S_x(f) = 2 \int_{-\infty}^{\infty} \varphi_x(\tau) \cdot \exp(-j2\pi\tau) d\tau \tag{2.4}$$

The right hand side of Equation 2.4 is represented with the cosine function as

$$S_x(f) = 4 \cdot \int_{0}^{\infty} \varphi_x(\tau) \cdot \cos(2\pi\tau) d\tau \tag{2.5}$$

We interpret $S_x(f)df$ as being the amount of $x(t)^2$ that is contained in the frequency band from f to f +Δf. In this case, $S_x(f)$ is called the power spectral density of $x(t)$ and expressed in the unit of V^2/Hz.

In addition, the autocorrelation function gives information on how much noise reduction is possible. If there is no "correlation" between single events at different times, than noise reduction measures are not possible at all. Only if the autocorrelation is not diminishing, a circuit designer has a chance to reduce noise by techniques like correlated double sampling or chopper stabilization. This term of correlation is clearly explained in the following, as the total noise in a circuit is analyzed. This is indeed the case, since all active and passive devices used in the circuit can not be free of noise. A statistical summation of each device's noise contribution gives the total noise as

$$\overline{\sqrt{\sum_n x_n^2}} = \sqrt{\sum_n \overline{x_n^2} + \sum_{j,k} \overline{x_j \cdot x_k}} \tag{2.6}$$

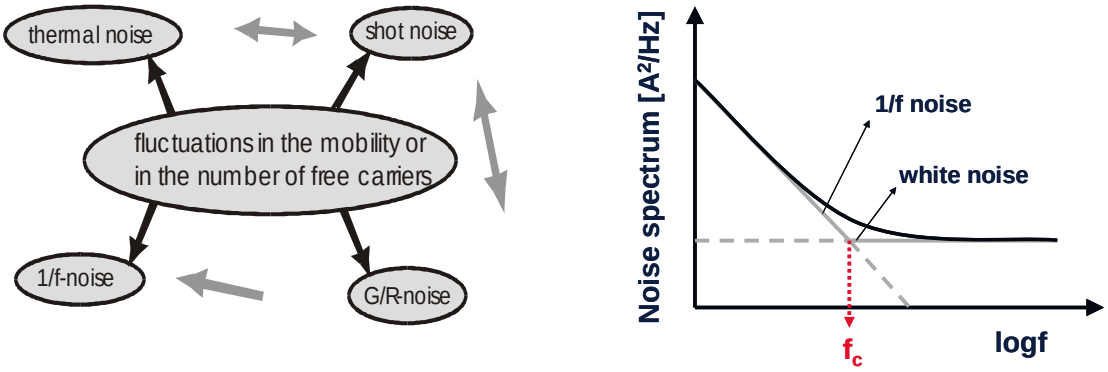

Figure 2.2 Left is a schematic representation of the four different types of noise mechanism in a MOSFET and their independencies [1]. Right is a typical noise spectrum in a MOSFET. The frequency f_c, where the 1/f noise meets the white noise (mainly thermal noise in a MOSFET) is noted.

Taking a close look at Equation 2.6 reveals that this is not a simple summation; there exists the second term in the root of the right-hand side. The second term shows correlation between two noise signal x_j and x_k. Equation 2.6 rewrites to Equation 2.7 using correlated factor C_{jk} which takes on the value in the range of -1 and 1. When the correlated factor C_{jk} is zero, the noise signals are uncorrelated and statistically independent.

$$\overline{\sum_n i_n^2} = \sum_n \overline{i_n^2} + c_{jk} \sum_{j,k} \sqrt{\overline{i_j^2} \cdot \overline{i_k^2}} \tag{2.7}$$

2.2 TYPES OF NOISE IN A MOSFET

Phenomenologically four main types of fundamental noise source are observed in a MOSFET. They are shot noise, thermal noise, generation-recombination noise and low-frequency noise which is often called flicker noise or 1/f noise. In this section, physics of these four types of noise are briefly discussed. Of course, an emphasis is laid on 1/f noise, which is of most importance and of great concern for the ongoing work in this thesis. Figure 2.2 illustrates the relation between these noise sources and the resultant noise spectrum of a MOSFET.

2.2.1 MOSFET NOISE MODEL

Figure 2.3 shows a small-signal MOSFET model which includes the noise sources. In Figure 2.3 the noise current i_g results from two noise sources: shot noise of the leakage current flowing through the gate and the gate-induced noise due to thermal fluctuations in the drain circuit that are coupled into the gate circuit. The noise current i_d is the result of thermal excitation of carriers in the channel of the device.

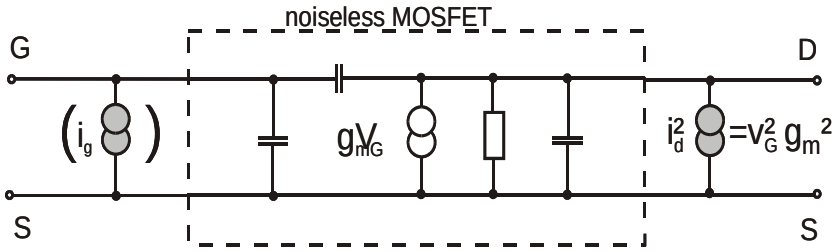

Figure 2.3 noise equivalent circuit for the common-source operation.

2.2.2 SHOT NOISE

Shot noise occurs when quantized carriers cross barriers with random spacing as in Schottky, pn-diodes or p-n junctions of a MOSFET biased in subthreshold. The arrival of one unit charge at a boundary is independent of when the previous unit arrived or when the succeeding unit will arrive. Two conditions are required for shot noise to occur: a flow of direct current and a potential barrier which the carriers cross over. This is graphically depicted in Figure 2.4. The shot noise generated in a nonlinear device (linear device does not create shot noise), which is first described by Schottky in 1918, is modelled by a parallel noise current pulse train with an amplitude of one electronic charge q ($1.602 \cdot 10^{-19}$ Coulombs) in a transition time of τ_t [2]. The corresponding autocorrelation function of this pulse train and related power spectral density are given in Equation 2.8 and Equation 2.9

$$A_{total,\tau}(\tau) = \frac{q \cdot I_{DC} \cdot (\tau_t - |\tau|)}{\tau_t} \quad \text{where} \quad I_{DC} = \frac{q}{\tau_t} \tag{2.8}$$

$$\frac{i_{shut}^2}{\Delta f} = \frac{2 \cdot I_{DC} \cdot q \cdot \sin^2(\pi f \cdot \tau_t)}{(\pi f \tau_t)^2} \tag{2.9}$$

When the transition time τ_t is small compared to the frequency f, Equation 2.9 simplifies to

$$\frac{i_{shut}^2}{\Delta f} = 2 \cdot I_{DC} \cdot q \quad \text{for} \quad f << 1/\tau_t \tag{2.10}$$

As seen in Equation 2.10, shot noise is white noise because the power spectral density is flat for small frequencies. On the contrast, from Equation 2.9, when the transition time τ_t is relative big compared to the frequency f, shot noise becomes to be negligible. In the case of MOSFETs, shot noise dominates the noise characteristics only when the device is in the sub-threshold region owing to the carrier transport in this region, which is very similar to conditions in bipolar transistors.

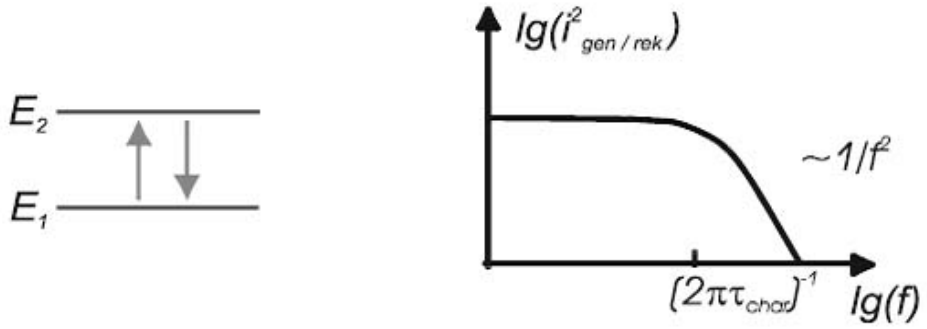

Figure 2.4 Generation-recombination noise is caused by the carrier density fluctuation due to generation and recombination process (the left picture) and the resulted noise power spectrum (the right picture)

2.2.3 GENERATION-RECOMBINATION NOISE

Carrier generation-recombination process between two energy states causes fluctuation in the number of carriers participating in current flow. This noise is called generation-recombination noise. The physical origin of this type of noise is reasonably well-understood and relies on the capture and release of charge carriers by a trap or generation-recombination centre [3].The operation of a single trap results in a discrete switching behaviour in the current flowing through the semiconductor. This discrete switching can be modelled in the time domain as a two-state signal with two separate transition probabilities between the two different energy states (the left of Figure 2.6). Such a signal is known as the Random Telegraph Signal (RTS).

The power spectral density of an RTS, given as Equation 2.11 and so-called Lorentzia spectrum can be found by Fourier Transformation of its autocorrelation function.

$$\frac{\overline{i_{GR}^{\,2}}}{\Delta f} = N \cdot P_{trap+}(E,x) \cdot (1 - P_{trap}(E,x)) \cdot \frac{4 \cdot \tau_0(E,x)}{1 + (2\pi f \tau_o(E,x))^2} \qquad (2.11)$$

The generation-recombination noise in a MOSFET mainly originates from bulk silicon/silicon dioxide interface defects [4]. The defects create traps that capture or release carriers. The generation-recombination noise is known to have a correlation with diffusion noise [5]. This will be detailed in the following chapter.

2.2.4 FLICKER NOISE (1/F NOISE)

The early days research of low frequency noise in a MOSFET has exhaustively demonstrated that this types of noise dominates at the lower part of the frequency spectrum, typically below of the frequency of a several hundred kHz [6, 7]. This type of noise is characterized by a power spectral density which varies proportional to a $1/f^{\lambda}$ law with λ close to 1 (typically, in the range of 0.7 to 1.3).

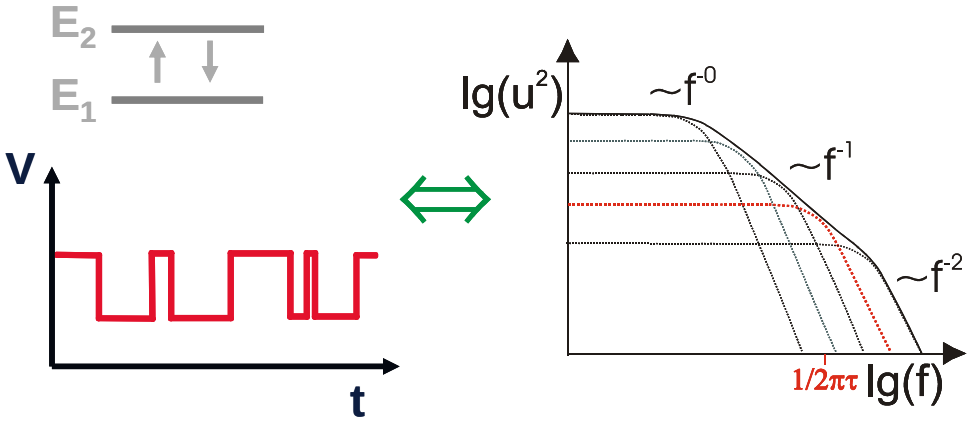

Figure 2.5 Left figure shows trapping and de-trapping process in energy band diagram and the resulting RTS signal. Right figure shows the corresponding GR noise and the resulting LF noise.

This is in contrast to a single generation-recombination noise, the Lorentzian-like spectrum, as shown in Figure 2.5. However, 1/f noise is understood by the superposition of a large number of Lorentzian-like spectra with an approximately exponential distribution of corner frequencies f_c over frequency. Equation 2.24 describes the power spectrum of the 1/f noise arising from a summation of such Lorentzian-like noise spectra.

$$S(f) = \iint N \cdot P_{trap+}(E,x) \cdot (1 - P_{trap+}(E,x)) \cdot \frac{4 \cdot \tau_{char}(E,x)}{1 + (2\pi f \tau_{char}(E,x))^2} dEdx \tag{2.12}$$

In spite of more than 30 years of research, there exists no unique model for 1/f noise in MOSFETs. Originally, it was thought that 1/f noise in semiconductor devices is a surface phenomenon and, therefore, is directly related to the quality of the Si/SiO_2 interface. Evidence has been advanced showing a good correlation with the density of interface (N_{it}) [8], or of near interface oxide traps (N_{ot}) [9]. The models, based on these observations, all fall roughly under what can be called the carrier number fluctuations or Δn theory, which find their roots in the McWhorter theory [10]. Opposite to the Δn model is the so-called the mobility fluctuation or $\Delta\mu$ theory, which considers mobility fluctuations for the origin of the 1/f noise and, for homogeneous semiconductors, assumes a volume and not a surface origin [11,12]. Different Δn-models use the superposition of Lorentzian spectra as the basis for modelling 1/f noise. These models mainly differ in the physical explanation for the specific exponential distribution of corner frequencies. The McWorther model assumes that the distances between electron traps in the oxide and the Si/SiO_2 interface are uniformly distributed. If the rate-limiting step for the trapping-detrapping process is simple quantum tunnelling, then it can be shown that an ensemble of uniformly distributed traps gives rise to the required exponential distribution of Lorentzian corner frequencies over frequency.

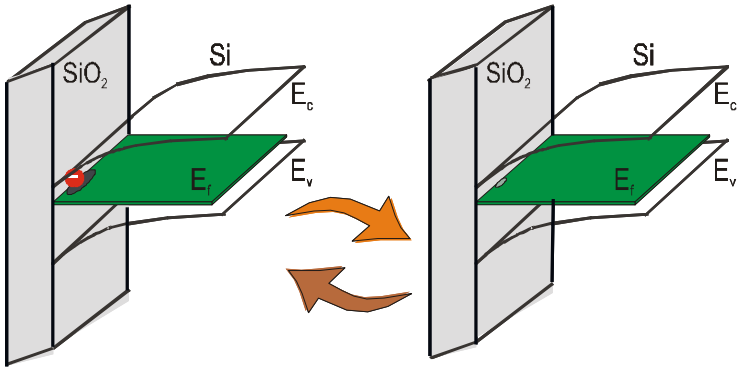

Figure 2.6 Energy band diagram in a MOSFET which shows the origin of 1/f noise: random trapping and detrapping process between Si/SiO_2 [1]

Differently shaped distributions result in smaller deviations from the pure f^{-1} frequency dependence. Other existing Δn-models relate the necessary exponential distribution of corner frequencies f_c to a certain distribution of some other physical parameter, like for example the activation energy of some processes. The treatment of these models is far beyond the scope of this thesis. An overview of the variety of models is given by Weissman [13]. Nevertheless, RTS-like signals involving single electron switching events have been observed in MOSFETs [14][15][16]. Especially as the active volume of devices is getting so small that it contains only a small number of charge carriers, the capture of a single electron into a localised state gives rise to a measurable change in device resistance.

The "mobility fluctuation" models ($\Delta\mu$-models) in a MOSFET is an empirical formula predicting input referred noise voltage increasing with gate bias voltage and proportional to oxide thickness. It is proposed by Hooge and has originally been formulated for metal films [20] [21]. These models assume that it is not the number of carriers that is fluctuating, but rather their mobility. This may be explained by lattice phenomena. Bulk mobility fluctuations play a significant role in homogenous semiconductors and metal films has been adequately demonstrated. Therefore some authors in the literature persist, that it seems unlikely that a MOSFET would be free of this sort of noise [22]. However, when looking at many low frequency noise spectra of modern small area devices can be reconstructed from measurements. This is very strong evidence for traps at the silicon/silicon-dioxide interface being the main source of 1/f noise in MOSFETs [17] and for the Hooge model not to be valid – at least for MOSFETs dominate low frequency noise contributions.

Irrespective of the kind of model which is followed, it is clear from this that the flicker noise of a MOSFET is a sensitive function of the technology and is either directly (ΔN) or indirectly through defect scattering ($\Delta\mu$) influenced by the material `quality' or the defectiveness at either side of the Si/SiO_2 interface. Hung proposed a unified model [18] - first introduction of the model is by Jayaraman and Sodini [19] - with a functional form resembling the number fluctuation model at low bias and the mobility fluctuation model at high bias. This model is often used as the basis for circuit simulations.

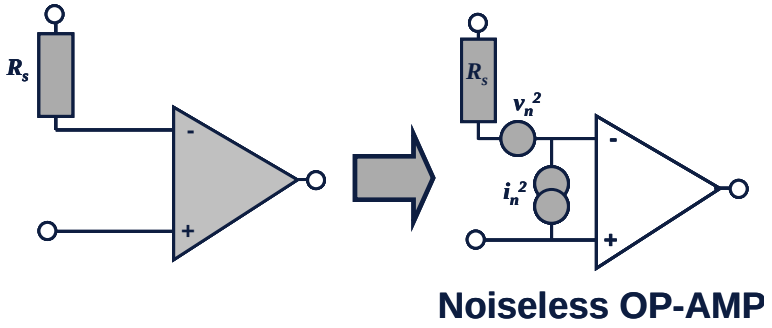

Figure 2.7 Op amp noise model

As an example, the gated-referred 1/f noise $S_{v_{gs}}^2$ is, given in Equation 2.24 according to [2].

$$S_{vg}{}^2 = 4 \cdot q^2 \cdot \frac{1}{C_{ox}{}^2 \cdot W \cdot L} \cdot \left(\frac{2V_{gs,eff} - V_{ds}}{2V_{ds}} \right) \int_0^{V_{ds}} \int_O^d N_{ot}(E,y) f_T (1 - f_T) \frac{\tau(y)}{1 + \omega^2 \tau^2(y)} \frac{1}{V_{gs,eff} - V_{ds}} dy dV \qquad (2.13)$$

In Equation 2.13 q is for electron charge, C_{ox} for oxide capacitance per area, W channel width, L channel width, $V_{gs,eff}$ for effective gate-source voltage, V_{ds} for drain source voltage, N_{ot} for oxide trapping density, f_T is quasi-Fermi level of trap, τ for time constant.

2.3 PRINCIPLE OF OP-AMP 1/F NOISE MEASUREMENTS

In general, it is extremely difficult to make a direct measurement of noise in an op amp. This is because noise voltage level is extremely small, typically in range of nano-volts, and because the noise sources are not physically confined to a point. In general, the noise sources are distributed through an op amp. It is impossible to place a sensitive noise meter at each point, where noise sources exist and which tells their magnitude. This section presents the principles of 1/f noise measurements of the op amp, which is detailed in Chapter 3 and discusses the relevant measurement setup of 1/f noise measurements of the proposed op amp.

2.3.1 1/F NOISE MODEL

It is much more practical in most cases to map the internal noise sources in an op amp to external noise sources. The general noise model puts a noise voltage source and a noise current source at each input to an op amp. Thus four noise sources are required, when the op amp has differential inputs. In general, the noise sources are correlated, but the correlation between the two sources on one input and the two sources on the other input is weak. If it is assumed that the op amp responds only to the differential input voltage, the two noise voltage

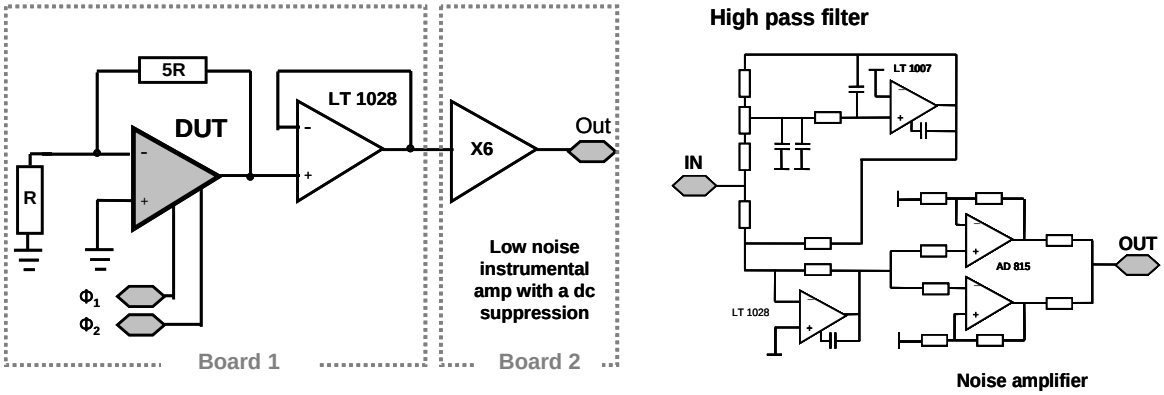

Figure 2.8 1/f noise of the operational amplifier measurements configuration. Right depicts The detailed schematic of the low-noise-instrumental amplifier with a high pass filter

sources in the general model can be replaced by a single noise voltage source at either input. In addition, the two noise current sources are replaced by a single differential noise current source under the assumption that the source impedance is the same for the op amp inputs. Figure 2.7 shows an op amp noise model according to the above statement, where v_n^2 represents the device voltage noise that exists when R_s equals zero, and i_n^2 represents the additional device current noise that exists when R_s does not equal zero.

Although the voltage noise v_n^2 and the current noise i_n^2 are normally correlated to some degree, it is common practice to assume the correlation coefficients are equal to zero [30]. Under these conditions, the total equivalent input noise voltage of an op amp is given as

$$v_{ni} = \sqrt{4kTR_s + v_n^2 + \left(i_n R_s\right)^2} \tag{2.14}$$

To measure i_n^2, a second measurement is made with a very large value of source resistance *Rs*. The source resistance R_s should be large enough so that the first two terms in Equation 2.25 are negligible. Under this condition the equivalent input referred noise current is obtained when the output noise voltage is divided by the product of the gain and the sources resistance. In the case of CMOS op amp, since the input current is enough small to be negligible, the current noise can be ignored to a good approximation.

2.3.2 1/F NOISE MEASUREMENTS SETUP

A noise measurement is usually made at the output of an operational amplifier. This is done for two reasons: the output noise level is higher and therefore easier to read on the meter, and it avoids the possibility of the noise meter up-setting the shielding, grounding or balancing of the input circuit of the device being measured. Since the measured output noise is the amplified sum of contribution from all noise sources in the amplifier, the input referred noise is preferred for intrinsic noise measurements. Then the measured output noise is referred to the input of the amplifier by dividing with the transfer voltage gain.

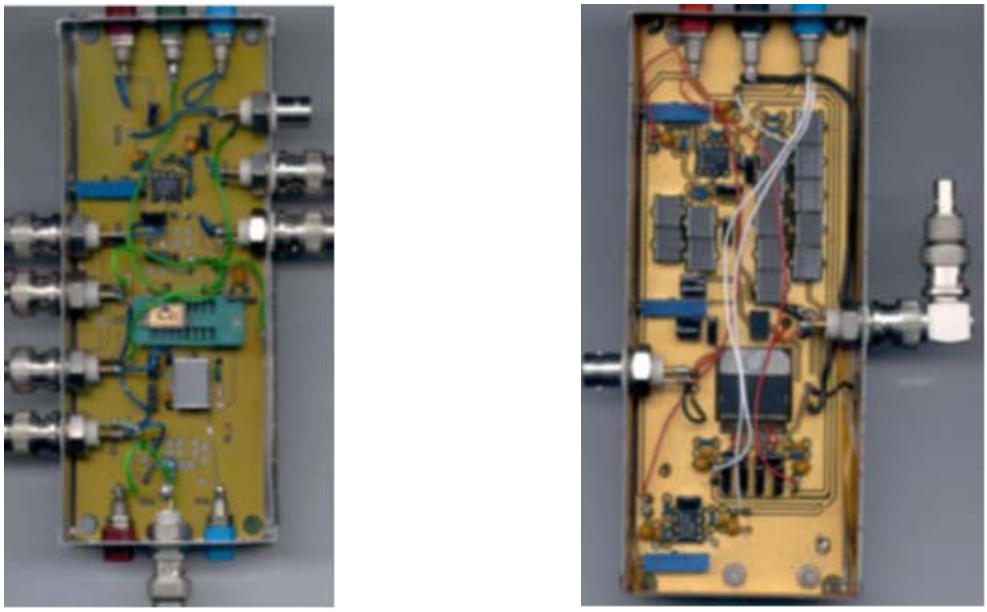

Figure 2.9 Left of the Figure shows Board 1 of Figure 2.8 which includes a DUT and the output buffer. Right of the Figure presents Board 2 of Figure 2.8, which is a low-noise-instrumental amplifier with a high pass filter

This is mathematically represented in Equation 2.15, where E_{ni} stands for the input-referred noise, E_{out} for the measured output noise and $G(f)$ for the transfer voltage gain. When the noise current i_n^2 can be ignored in Equation 2.14, the input-referred noise E_{ni} equals to the square root of the noise voltage v_n^2.

$$E_{ni} = \sqrt{\frac{E_{out}^2}{G(f)^2}} \tag{2.15}$$

When measuring this transfer voltage gain $G(f)$ of the amplifier, a special care should be taken : the signal level from the signal generator should be higher than the noise level and the amplifier should not get into saturation by doubling and halving the input signal. That is, the output signal should double and halve proportionately. Since this transfer voltage gain $G(f)$ is dependent on the source impedance and the amplifier's input impedance, the input noise is independent of the input impedance. Measuring of the output noise E_{out} is made with one input terminals of an op amp, which configures an amplification stage with a negative feedback, tied to the signal ground. In this configuration, the rms output noise voltage E_{out} reads on a spectrum analyser in a specified noise bandwidth Δf. A bandwidth span of DC to few hundred kilohertz range is used for measuring of the 1/f noise of an amplifier. When making spectrum analyzer readings of noise, three issues, which are the analyzer bandwidth, detection method and interfering signals, should be taken into account [20]. Figure 2.8 illustrates the 1/f noise of op amp measurements system that consists of a DUT, a buffer and a low-noise-instrumental amplifier with a high pass filter. As shown in Figure 2.8 the DUT (as

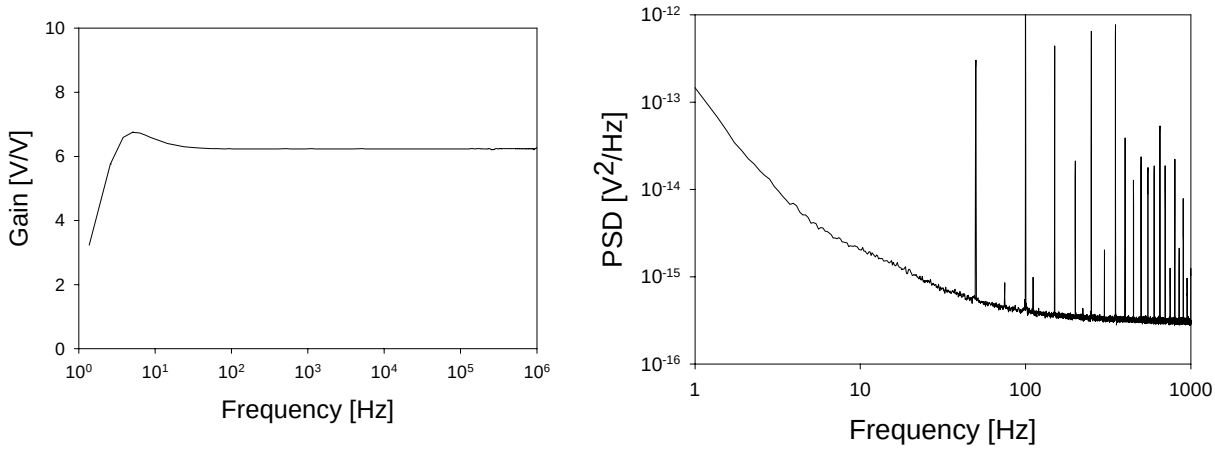

Figure 2.10 Left of the Figure shows the measured gain transfer function of the low noise instrumental amplifier and right shows its input referred noise power spectrum

it will be measured according to the principle described in the next chapters) requires a two complementary full-range swing (VSS to VDD) clocks for 1/f noise reduction. A commercial two-tone signal generator (Tektronix™ AWG 420) is used for this purpose. As Figure 2.10 depicts, the DUT is configured a gain stage of a factor of five using low noise and precision metal film resistors. The output buffer, which follows after the DUT, is configured with a commercially available low noise op-amp. In the next stage, an active high-pass-filter in the signal path suppresses the DC-offset output voltage of the DUT in order to extract the small dc noise signal.The active high-pass-filter is realized designing the filter to have a cut-off frequency of about 1 Hz. Finally the noise signal at the output is amplified by the instrumental amplifier and read by a commercial spectrum analyzer (Rohde & Schwarz™ UPD 320).

The measurement system is physically realized on two PCB (Printed Circuit Board): one contains DUT with an output driving buffer (the picture on the left of Figure 2.9 and the other is low-noise-instrumental amplifier with a high pass filter (the right-hand-side picture of Figure 2.9. Two PCBs are placed closet and connected together with a BNC cable for the measurement. As shown in Figure 2.9they are shielded. Since the noise signal is weak and easily affected by other external noise sources, all possible external noise reduction technique should be made. Shielding the measurements systems from other external environment is one of the examples: avoiding a ground loop, suppressing an external bias noise with a bypass filter or a battery are others. [21] .

The picture on the left of Figure 2.10 plots the measured transfer function of the low noise instrumental amplifier and demonstrates that the gain curve below 1 Hz is indeed strongly suppressed. In the noise amplification stage, a difference amplifier is used to suppress the common-mode signal of the noise. For optimal resolution to be achieved in the measurement, the noise instrument amplifier should have an optimal noise resistance: in this case its noise contribution to the total noise is as minimal as possible. In fact, its noise contribution is

negligible, as right-hand-side picture of Figure 2.10 shows: the measured input referred noise is much lower than that of the DUT (refer to Chapter 5): the instrumental amplifier is based on a bipolar operational amplifier while the DUT adopts CMOS technology.

2.4 REFERENCES FOR CHAPTER 2

[1] R. Müller, "Rauschen," Berlin, Heidelberg, New York, Springer-Verlag, 1990

[2] F. Schottky, "Über spontane Stromschwankungen in verschiedenen Electrizitatsleitern," Annalen der Physik, vol. 57, pp. 541–567, 1918.

[3] B. K. Jones, "Low-frequency noise spectroscopy," IEEE Transaction on Electron Devices, vol. 41, 2188-2197, 1994

[4] A. L. McWhorter, "Interfacial noise in semiconductors," Semiconductor Surface Physics, Philadelphia, University Press, pp. 169-196, 1957

[5] J.-P Nougier, "Fluctuations and noise of hot carriers in semiconductor materials and devices," IEEE Transactions on Electron Devices, vol. 41, pp.2034-2049, 1994

[6] S. Christensson, I. Lundström and C. Svensson, "Low frequency noise in MOS transistor – I theory," Solid-State Electronics, vol. 11, pp.791-812, 1968

[7] F. M. Klaassen, "Characterization of low 1/f noise in MOS transistors," IEEE Transactions on Electron Devices,vol.18, pp.887-897, 1971

[8] H. E. Maes, S. H. Usmani and G. Groeseneken, "Correlation between 1/f noise and interface state density at the Fermi level in field-effect transistors," Journal of Applied Physics, vol. 57, pp.4811-4813, 1985.

[9] L .K .J. Vandamme and R. G. M. Penning de Vries, "Correlation between 1/f noise and CCD transfer inefficiency," Solid-State Electronics, vol. 28, pp.1049-1056, 1985

[10] A. L. McWhorter, "Semiconductor surface physics," University of Philadelphia Press, Philadelphia, 1957

[11] F. N. Hooge, "1/f noise is no surface effect," Physics Letters A, vol. 29, pp.139-141,1969

[12] F. N. Hooge, T.G.M. Kleinpenning and L.K.J. Vandamme, "Experimental studies on 1/f noise," Reports on Progress in Physics, vol. 44, pp.497-532, 1981

[13] L. K. J. Vandamme, X. Li and D. Rigaud, "1/f Noise in MOS Devices, Mobility or Number Fluctuations? ," IEEE Transactions on Electron Devices, vol. 41, No. 11, pp.1936-1995, November 1994.

[14] K. S. Ralls, W. J. Skocpol, L. D. Jackel, R. E. Howard, L. A. Fetter, R. W. Epworth, and D. M. Tennant, "Discrete Resistance Switching in Submicrometer Silicon Inversion

Layers: Individual Interface Traps and Low-Frequency (1/f) Noise," Physical Review Letters, vol. 52, No. 3, pp.228-231, 16 January 1984.

[15] M. Schulz and H.H. Mueller, "Single-electron trapping at semiconductor interfaces," Advances in Solid State Physics, vol. 35, pp.229-241, 1964

[16] M. J. Kirton and M. J. Uren, "Capture and emission kinetics of individual Si:SiO_2 interface states," Applied Physics Letters, vol. 48 (19), pp.1270-1272, 1986.

[17] R. Brederlow, W. Weber, D. Schmitt-Landsiedel, and R. Thewes, "Fluctuations of the low frequency noise of MOS transistors and their modelling in analog and RF-circuits," Technical Digest of IEDM, pp. 159 – 162, 1999

[18] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A unified model for flicker noise in metal-oxide-semiconductor field-effect transistors," IEEE Transactions on Electron Devices, vol. 37, pp.654–665, 1990

[19] R Jazaraman, and C.G. Sodini, "A 1/f noise technique to extract the oxide trap density near the conduction band edge of silicon," IEEE Transactions on Electron Devices, vol.36, pp.1773-1782, 1989

[20] C. D. Motchenbacher, Low noise electronic system design, John Wiley and Sons, New York, 1993

[21] H.W. Ott, Noise reduction technique in electronic systems, Wiley-Interscience, New York, 1988

CHAPTER 3

PRINCIPLE FOR 1/F NOISE REDUCTION TECHNIQUE

The operational amplifier is an essential building block of electrical signal sensor system, switched capacitor filter, analog-to-digital converter etc [1]. Using op-amps with MOS input transistors, the op-amp input current at low frequencies can indeed be made extremely small; however, the input voltage of a practical op-amp is typically of the order of 1-10 mV, since it is affected by several non-ideal effects. These include 1/f and thermal noise, the input-referred DC offset voltage, as well as the signal voltage necessary to generate the desired output voltage of the op amp. Normally, the thermal noise occupies a wide frequency band, while the 1/f noise, offset and input signal are narrowband low-frequency signals. Among the low-frequency narrowband imperfections, the 1/f noise is of the most significance, especially in linear analog CMOS IC [2].

In this chapter a novel principle for the 1/f noise reduction technique in linear analog CMOS IC's is introduced. The principle is based on a known device physics-related mechanism which has been briefly introduced in Chapter 1 and more details of the effect will be given, at first. Based on these, we propose a new circuit configuration of a MOSFET for 1/f noise reduction which is suitable for a continuous signal processing operation. A discussion on the noise behavior of the new MOSFET architecture for 1/f noise reduction is given. The CMOS two stage miller operational amplifier is a type of a linear analog CMOS IC which today re-gains attentions from industry since it shows a good match with a modern low voltage/low power CMOS technology. The proposed circuit configuration of a MOSFET is applied to this type of circuits.

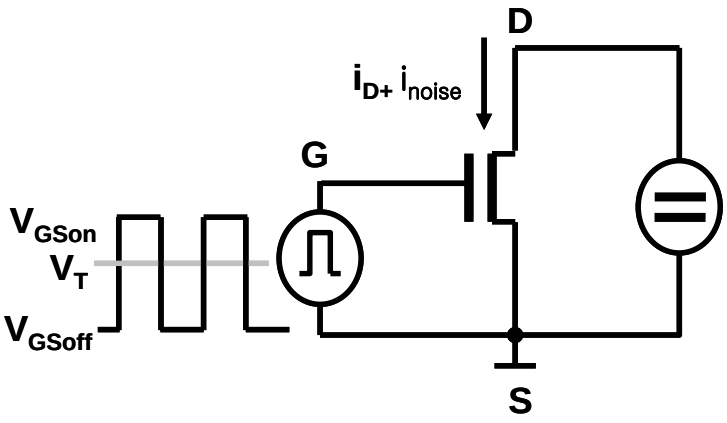

Figure 3.1 Picture shows the conceptual idea for the periodical on-off switching of a MOSFET between strong inversion and accumulation after [3].

3.1 MOSFET 1/F NOISE UNDER NON-EQUILIBRIUM STATE

A periodical on-off switching of a MOSFET between strong inversion and accumulation leads to an anomalous reduction of the intrinsic 1/f noise of those devices. Under this condition, the MOSFET is not in an equilibrium operating state.

3.1.1 GENERAL OVERVIEW

Figure 3.1 describes the operating conditions of a periodical on-off switching of an nMOSFET between strong inversion and accumulation. A square-wave voltage source with the high level V_{GSon} and the low level V_{GSoff} , switches the gate-to-source voltage V_{GS} of the nMOSFET between two bias states on a certain period. The high level V_{GSon} is greater than the threshold voltage V_T, so that the transistor is biased to a constant voltage in strong inversion on a half period, namely nMOSFET is “on.” The low level voltage V_{GSoff} determines a bias point of a MOSFET which corresponds to moderate inversion, weak inversion or accumulation (holes in the p-bulk accumulate under the gate-oxide) on the other half period. Especially when V_{GSoff} is equal or lower than the threshold voltage, the nMOSFET is “off.” In this configuration, the MOSFET experiences two bias states, the MOSFET is not in an equilibrium operating state. This periodical on-off switching of a MOSFET between strong inversion and accumulation leads to a reduction of the intrinsic 1/f noise of the device [3, 4]. Figure 3.2 shows the measured 1/f noise spectra of an nMOSFET, according to the schematic in Figure 3.1 [3]. The upper curve shows the measured 1/f noise spectrum of the nMOSFET which is constantly biased to a gate-source voltage of 2.5V.

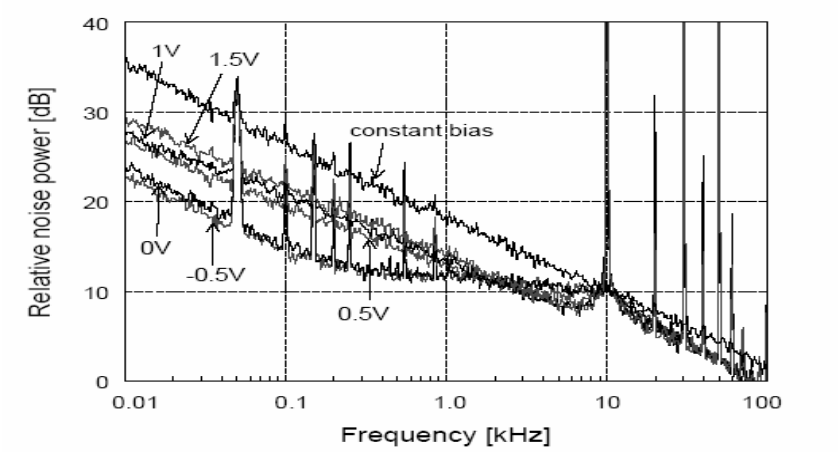

Figure 3.2 Measured 1/f noise for constant- and periodical on-off biasing conditions of an nMOSFET, which has a threshold voltage of 1.9V. The switching clock has a frequency f_{switch} of 10kHz and 50% duty cycle. V_{GSon} is 2.5V and various V_{GSoff} are as indicated. The picture is depicted from [**3**].

The remaining curves show the noise spectrum of the devices when it is periodically switched between the on-gate-to-source voltage V_{GSon} of 2.5V and various off-gate-to-source voltages V_{GSoff} with a square clock of 10 kHz and 50% duty cycle. The values of the off-gate-to-source voltage V_{GSoff} are indicated in the figure. A 6dB noise reduction is expected in the 1/f noise spectrum in this scheme, since the overall noise power is halved. This 6dB noise reduction is experimentally observed when the off-gate-to-source voltage V_{GSoff} is higher than the threshold voltage V_T. But the measurements show an additional anomalous reduction in the 1/f noise spectrum for the lower gate-to-source voltage V_{GSoff}. The amount of 1/f noise reduction is dependent on the off-gate-to-source voltage V_{GSoff}, even if it is well below the threshold voltage V_T. The additional reduction increases with decreasing V_{GSoff} and about 8 dB noise reduction is achieved at 1 KHz.

This effect was first reported by Bloom and Nemirovsky, in 1991, and they achieved 1/f noise reduction by a factor of three in a relatively long channel nMOSFETs at a switching frequency of 600 Hz [4]. They observed that the 1/f noise reduction is maximized when the MOSFET is cycled from strong inversion via weak inversion to accumulation. Their results were reconfirmed and related to RTS (Random Telegraph Signals) [5]. Although almost all literature relevant to this subject deals with nMOSFETs, pMOSFETs also show this anomalous 1/f noise reduction [6].

3.1.2 EXPLANATION OF THE NOISE-REDUCTION PHENOMENON

The 1/f noise reduction effect can be qualitatively explained using Figure 3.3. The 1/f noise current is caused by traps at the $Si/Si0_2$ interface. The carriers (electrons or holes) can fluctuate between trapped (no current contribution) and detrapped/free states (contribution to current), when both states have approximately equal free energy for the carriers.

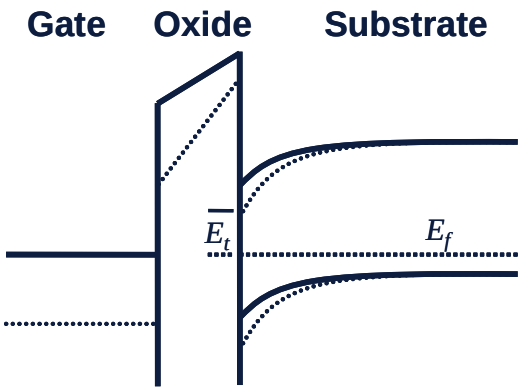

Figure 3.3 Energy band diagram for an n-MOSFET, with an active trap in the gate oxide. Solid lines show the transistors off-state (depletion), and dashed lines the transistor on-state (inversion) after [13]

In steady-state (under constant gate-to-source voltage and which is the case for a few traps), the trap-occupancy function follows the Fermi-Dirac statistics and is a function of the trap energy (E_t in Figure 3.3), and the Fermi-level of traps. Only the traps whose energy is nearly equal to the Fermi-level (E_f in Figure 3.3) of the free carriers in silicon contributes to the noise. Although the Fermi-level of the free carriers in silicon dose not change with the applied gate-to-source voltage V_{GS}, but the applied gate-to-source voltage V_{GS} is effective in changing the energy level difference from the Fermi-level to the conduction band. In fact, the number of free carriers in the channel depends on the band-bending in silicon and thus V_{GS} as shown in Figure 3.3.

Under periodical on-off switching - when the operating point of a MOSFET and respectively the gate-to-source voltage V_{GS} is changed strongly (e.g. from accumulation to inversion or strong inversion) and the Fermi level of the free carriers in silicon changes instantaneously with the changes in V_{GS} - the fluctuation probability between the two states (trapped/detrapped) is significantly reduced. This results in a smaller noise current contribution from the corresponding trap states. However, there is an almost equal amount of traps (at different trap energy levels) which contribute to 1/f noise at the other gate voltage. If the gate voltage is changed between the two gate voltages at a faster rate than the trapping / de-trapping time constant of the traps, the situation changes. Some occupied traps cannot be discharged as well as some non-occupied traps remain empty, thus this leads to a reduction in the 1/f noise current of the device.

This qualitative explanation is in line with Kohlhatkar's RTS noise models [7]. RTS signal is the limited case when a MOSFET has smaller active area and thus the available number of is "very" few (usually less than 10^4) [9]. Recalling the RTS noise and 1/f noise theory in Chapter 2, RTS noise can be regarded a type of 1/f noise when only few traps exist. During transients, especially when the device is switched "on," the trap-occupancy (which is given by $\tau_{e,on}/(\tau_{e,on}+\tau_{c,on})$ and shown in Figure 3.4) takes time to adapt to this new bias condition.

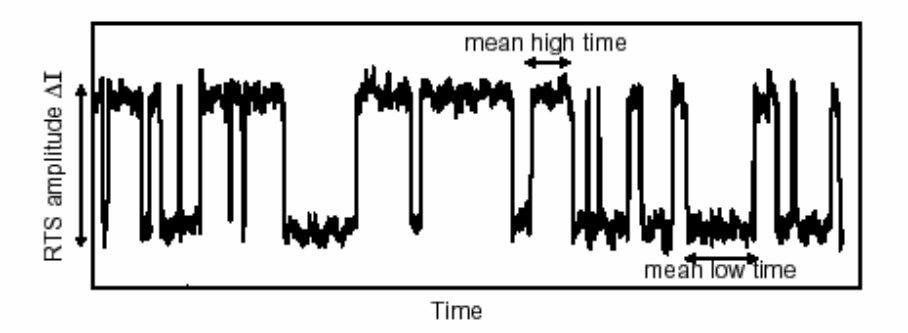

Figure 3.4 Time-domain trace of the drain current of a MOSFET showing a Random Telegraph Signal (RTS). Here τ_c is the mean high time and τ_e is the mean low time. The measurement is depicted from [9].

In fact, the instantaneous trap-occupancy does not follow the instantaneous step-voltage but increases exponentially from the steady-state off value to reach the steady-state on value as shown in Figure 3.5. When the frequency of the applied gate-bias is much higher than the corner frequency of the RTS, the averaged trap-occupancy is somewhere between the steady-state trap-occupancy in the on and off state as in Figure 3.6. Slow traps cannot adapt quick enough to fast change in the bias point and thus this leads to an RTS noise reduction. Historically, several authors made explanations for this effect. Zhang et al explained this effect using the amplitude modulation theory [8]. But an anomalous 1/f noise reduction of 8 dB cannot be explained from the amplitude modulation theory [3]. Tian et al proposes a non-stationary 1/f noise model [9]. But this model predicts complete disappearance of the 1/f noise below the switching frequency, which is not consistent with the recent experimental results. Van der Wel proposed a simulation model and method to account for RTS-related 1/f noise reduction, but his models lacks of a physical reason [10]. Recently, Kolhatkar et al has developed an RTS noise models in MOSFET under non-equilibrium state which is in line with the proposed qualitative explanations in this thesis, however no quantitative model exists up to now which is able to correctly describe the frequency behaviour of measured data under switched biasing conditions.

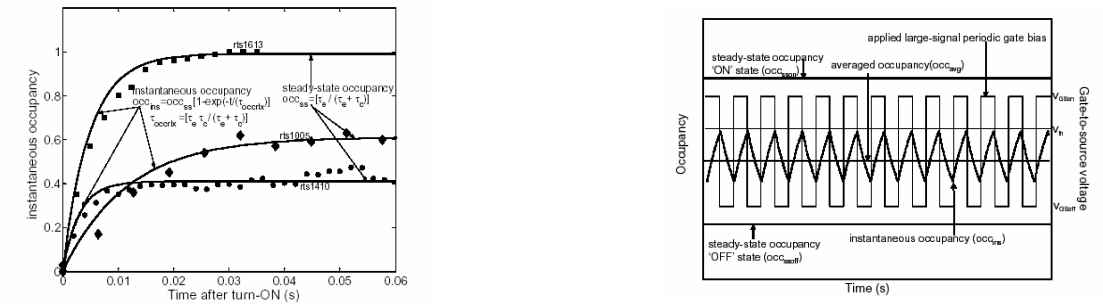

Figure 3.5 The left picture shows the measurement and simulated instantaneous occupancies for 3 different RTS on 3 different devices and the picture on the right shows the instantaneous trap-occupancy under periodic on-off switching of a MOSFET. The picture is depicted from [9].

3.2 COMPLEMENTARY SWITCHED MOSFET ARCHITECTURE

An application of the mentioned scheme for 1/f reduction (Figure 3.1) to discrete-time circuits is rather straightforward, because the discrete-time circuit like PLL, VCO needs a bias current only for a certain time or period [11]. However, from the point of view of a circuit designer, a direct use or adopt of the scheme to a continuous-signal-processing circuit is not a simple matter. We propose a new circuit configuration of a MOSFET in order to make use of the 1/f noise reduction effect (periodical on-off switching of a MOSFET) for a time-continuous signal processing like a linear analog CMOS IC's.

3.2.1 PRINCIPLE

The basis of the new circuit implementation of an nMOSFET and its counterpart, a pMOSFET are illustrated in Figure 3.6 and Figure 3.7 respectively. An nMOSFET (Left of Figure 3.6), whose noise contribution shall be reduced, is replaced by the circuit on the right side of Figure 3.6. This "replacement" nMOSFET (T1) consists of two complementary full swing range clocks (Φ1 and Φ2) and two switches (SW1 and SW2) and the two nMOSFETs T11 and T12. The nMOSFET T11 and T12 are identical to the nMOSFET T1 in geometry and device-physics. In this configuration, the two clocks (Φ1 and Φ2) and two switches (SW1 and SW2) connect a gate of the transistor T11 or T12 to the node G or GND alternatively during a half period of the clock. One of two nMOSFETs, connected to the node G (e.g., T11), is forced to operate in inversion state (on-state), when a potential greater than the threshold voltage of the transistor T11 is applied to the node G. The other is connected to the lowest potential node GND (e.g. T12) in accumulation (off-state) during the same period. Both transistors T12 and T12 will experience a switching transition between accumulation and inversion which is absolutely necessary for the intrinsic 1/f-noise reduction [11].

Thanks to this alternate switching of two MOSFETs, one is in operating mode (i.e. "process" a information signal of interest) and the other stays the noise-pre-charge state on the same period, namely a continuous operation of the transistor pair is assured [12][13]. The explanations are very similar for the pMOSFET (T2) in Figure 3.7. Unlike the nMOSFETs T11 and T12 in Figure 3.6, the gate of the pMOSFETs T21 and T22 are switched between the node G (on-state) and the highest potential node VDD (off-state). In real applications, this complementary switched MOSFET (e.g., T11 in Figure 3.6) architecture exhibits a "certain" time-discontinuous drain current of T1 as in the right of Figure 3.6 and 3.7. This discontinuity is mainly due to the mismatch in the duty cycle of the applied clocks Φ1 and Φ2, since all the clocks must, in reality, have a certain rising/falling time and thus they can not have perfect 50 % duty cycle. The discontinuous time is negligibly small, compared to the period T of the clocks. The detailed discussion is given in Chapter 4 with the simulated results).

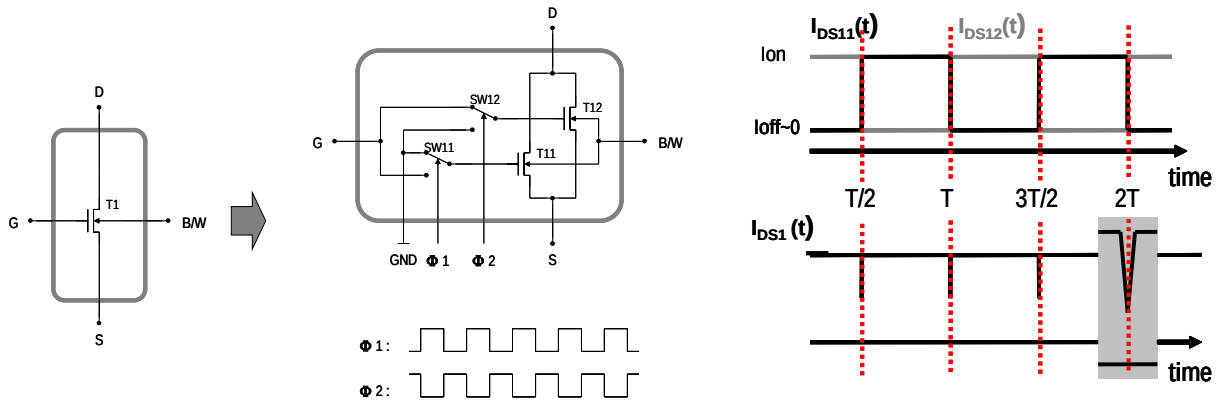

Figure 3.6 Picture on the left shows the replacement of an n-MOSFET with two transistors and two switches as proposed here for 1/f noise reduction. The right side shows the corresponding drain-to-source current of the transistors in the left figure. The enlarge view on the left side shows glitches during the switching of the applied clock signals Φ1 and Φ2.

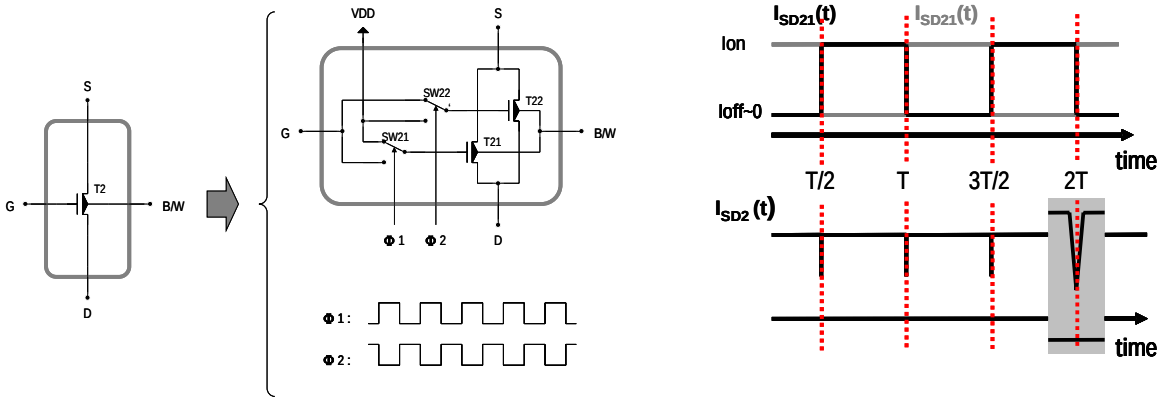

Figure 3.7 Picture on the left shows the replacement of a p-MOSFET with two transistors and two switches as proposed here for 1/f noise reduction. The right side shows the corresponding drain-to-source current of the transistors in the left figure. The enlarge view on the left side shows glitches during the switching of the applied clock signals Φ1 and Φ2.

This principle, the complementary switched MOSFET architecture is applicable to many time continuous analog circuits and topologies, especially where a strong 1/f-noise reduction is needed.

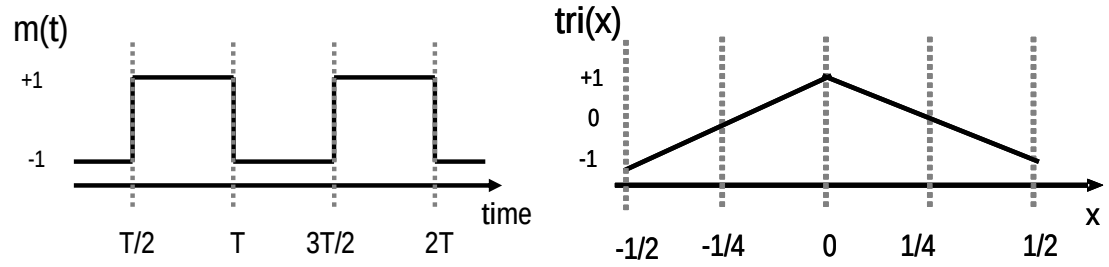

Figure 3.8 Plot of m(t) and tri(x)

3.2.2 NOISE BEHAVIOR

The complementary switched MOSFET architecture exhibits at least 3dB 1/f noise reduction, even though 1/f noise behavior under non-equilibrium effect is not taken into consideration. This is explained when a modulation theory is applied to the switched MOSFET architecture (e.g., Figure 3.6).

Mathematically the drain current I_{DS1} (t) of T1 can be given as the sum of the drain current I_{DS11} (t) of T11 and I_{DS12} (t) T12 as

$$I_{DS1}(t) = I_{DS11}(t) + I_{DS12}(t) = I_{ON} \cdot (\Phi_1(t)) + I_{ON} \cdot (\Phi_2(t)) \tag{3.1}$$

In Equation 3.1, the applied clocks Φ_1(t) and Φ_2(t) are represented with the periodic function m(t), which has a fixed switching frequency f_{clk} with an amplitude {-1,+1}.

$$\Phi_1(t) = \frac{1}{2} \cdot (1 + m(t)) \quad \text{and} \quad \Phi_2(t) = \frac{1}{2} \cdot (1 - m(t)) \tag{3.2}$$

In the time domain, the Fourier Series of the periodic function m(t) is represented as

$$m(t) = \sum_{-\infty}^{\infty} M_n \cdot \exp(j2\pi n f_s t) \tag{3.3}$$

or, in the frequency domain as

$$M(f) = \sum_{-\infty}^{\infty} M_n \cdot \delta(f - n f_s) \tag{3.4}$$

In Equation 3.4 δ(f) denotes the Dirac-delta function and the corresponding Fourier coefficient M_n which is given by :

$$M_n = \frac{1}{T} \int_{-T/2}^{T/2} m(t) \cdot \exp(-j2\pi n f_s t) \tag{3.5}$$

Equation 3.5 yields

$$M_n = \frac{2}{j\pi n} \quad \text{for} \quad n = odd \qquad M_n = 0 \quad \text{for} \quad n = even \tag{3.6}$$

In Equation 3.6, n denotes the integer number.

Using Equation 2.5, the autocorrelation function $\varphi_m(\tau)$ is obtained as [14]

$$\varphi_m(\tau) = \frac{1}{T}\int_{-T/2}^{T/2} m(t)\cdot m(t+\tau)dt = tri\left(\frac{\tau}{T}\right) \tag{3.7}$$

In Equation 3.7, $tri(\tau/T)$ is a periodic triangle function which is represented as

$$tri(x) = 1 - 4|x| \quad |x| \le 0.5 \qquad tri(x+n) = tri(x) \quad n \in N \tag{3.8}$$

and

Now the autocorrelation function $\varphi_{IDS11}(t)$ of $I_{IDS11}(t)$ is obtained as

$$\varphi_{IDS11}(\tau) = \frac{1}{T}\int_{-T/2}^{T/2} I_{DS11}(t)\cdot I_{DS11}(t+\tau)dt \tag{3.9}$$

$$= \frac{I_0^2}{4}\cdot\frac{1}{T}\int_{-T/2}^{T/2}(1+m(t))\cdot(1+m(t+\tau))dt = \frac{{I_0}^2}{4}\left(1+tri\left(\frac{\tau}{T}\right)\right)$$

Similarly, the autocorrelation function $\varphi_{IDS12}(t)$ of $I_{IDS12}(t)$ is obtained as[1)]

$$\varphi_{IDS12}(\tau) = \frac{1}{T}\int_{-T/2}^{T/2} I_{DS12}(t)\cdot I_{DS12}(t+\tau)dt \tag{3.10}$$

$$= \frac{I_0^2}{4}\cdot\frac{1}{T}\int_{-T/2}^{T/2}(1-m(t))\cdot(1-m(t+\tau))dt = \frac{{I_0}^2}{4}\left(1+tri\left(\frac{\tau}{T}\right)\right)$$

Reminding the autocorrelation function $\varphi_m(\tau)$ in Equation 3.9, the autocorrelation function $\varphi_{ID1}(t)$ is given as

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[1)] No correlation between $I_{IDS11}(t)$ and $I_{IDS12}(t)$ is assumed.

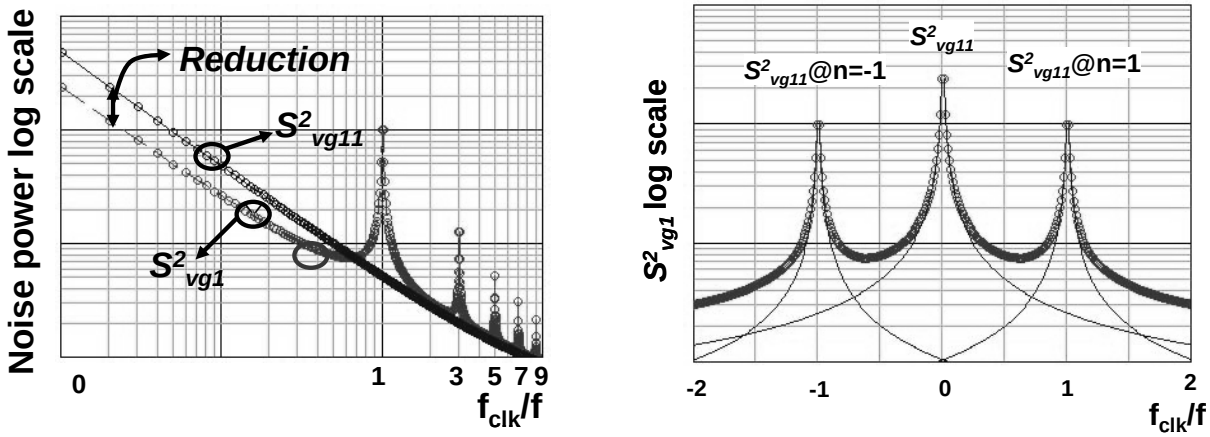


Figure 3.9 The left picture shows a calculation of the 1/f noise effect in a switched MOSFET, when the modulation is applied. A further reduction is expected in the architecture, when we take the 1/f noise behavior of MOSFET under non-equilibrium into account. The right picture shows the noise-aliasing into odd harmonics of f_{clk} due to the clocks.

$$\varphi_{ID1}(\tau) = \frac{I_0^{\,2}}{4}\left(1+tri\left(\frac{\tau}{T}\right)\right)+\frac{I_0^{\,2}}{4}\left(1+tri\left(\frac{\tau}{T}\right)\right)=\frac{I_0^{\,2}}{2}\left(1+tri\left(\frac{\tau}{T}\right)\right) \tag{3.11}$$

Recalling the Equation 2.5 to 2.8, Fourier-transformation of $\varphi_{ID1}(t)$ yields $S^2{}_{ID1}(f)$:

$$S^2_{ID1}(f) = S^2_{ID11}(f) * \left(\delta(f)+\sum_{-\infty,n=odd}^{\infty}\left|M_n\right|^2\cdot\delta(f-nf_{clk})\right) \tag{3.12}$$

In Equation 3.12, $S^2_{ID11}(f)$ (or $S^2_{ID12}(f)$) is the drain current noise power spectral density of the transistor T11 (or T12) when the steady-static bias is applied to. The symbol * denotes the convolution operation [14].

Now Equation 3.12 rewrites to:

$$S^2_{ID1}(f) = \left(S^2_{ID11}(f)+\sum_{-\infty,n=odd}^{\infty}\left(\frac{2}{\pi n}\right)^2\cdot S^2{}_{ID11}(f-nf_{clk})\right) \tag{3.13}$$

Equation 3.13 indicates that no reduction in the noise and that the principle accompanies with the aliasing of the fundamental noise $S^2_{ID11}(f)$ to the odd harmonics of the clock frequency.

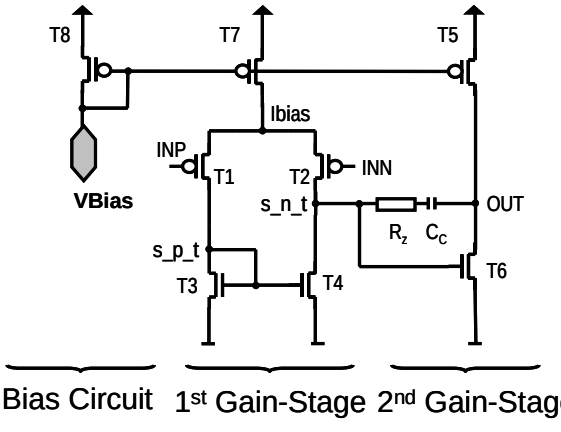


Figure 3.10 A CMOS two stage miller operational amplifier.

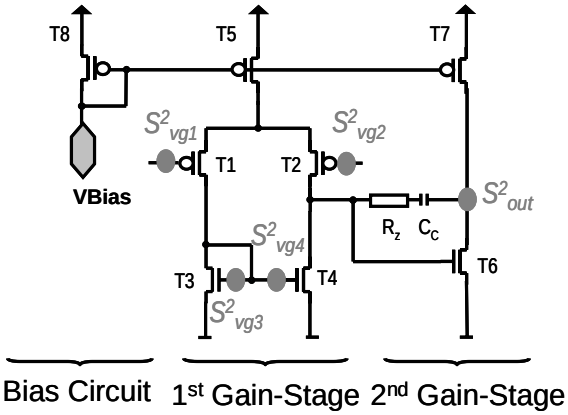


Figure 3.11 Main noise sources in the CMOS two-stage miller operational amplifier from the Table 3.1.

But the MOSFET 1/f noise behavior under non-equilibrium state expects an enhancement of the 1/f noise reduction: $S^2_{ID11}(f)$ of the principle is smaller than that of the "constant biased" MOSFET. Hence a further increase in the 1/f noise reduction is expected from the complementary switched MOSFET architecture. Now Equation 3.13 rewrites to

$$S^2_{vgs1}(f) = \left(S^2_{vgs11switched}(f) + \sum_{-\infty, n=odd}^{\infty} \left(\frac{2}{\pi n} \right)^2 \cdot S^2_{vgs11switched}(f - nf_{clk}) \right) \tag{3.14}$$

In Equation 3.14 $S^2_{vgs11}(f)$ is represented with $S^2_{vgs11_{switched}}(f)$ where $S^2_{ID11switched}(f)$ denotes the drain current noise power spectrum density of T11 (or respectively T12) under non-equilibrium state.

3.3 APPLICATION TO LINEAR ANALOG CMOS IC'S

As a demonstration example for a linear analog CMOS IC a CMOS Miller two stage op-amp (Figure 3.10) was chosen since this topology is frequently used in today's submicron and low-voltage CMOS technologies [15]. As the name indicates, a CMOS miller two stage op amp is composed of two stages: the first of which is a differential stage with transistors input devices (T1 and T2) and the current mirror (T3 and T4) acting as an active load (Figure 3.10). Here we chose pMOSFETs for the input devices. Of course, an nMOSFET is widely used for high speed application, as an nMOSFET has a superior mobility compared to a pMOSFET. But pMOSFETs are more attractive and area-effective in robust design because pMOSFETs have

a better matching constant and better 1/f noise properties [16]. The second stage is a simple CMOS source follower with T6 as a driver and T7 acting as an active load.

Its output is connected to its input, i.e., to the output of the differential stage by means of compensation capacitance Cc for stability reasons. Since the compensation capacitance actually acts as a Miller capacitance in that stage, the op amp is called a miller operational amplifier. [17].In this type of circuits, the 1/f noise is a main limiting factor of the minimal input signal resolution. Since this type of circuit is often used for low noise signal amplification like audio band applications (like a hearing-aid), there is a strong need to reduce or suppress this type of noise here. In the following the benefit of the principle for the 1/f noise reduction to the circuit will be discussed.

Transistor	A_{vni0}	$S^2_{vgi}\,(A_{vi0}/A_{v0})^2$
T1, T2	A_{vo}	$S^2_{vg1}\,S^2_{vg2}$
T3, T4	$(g_{m3}/g_{m1})\,A_{v0}$	$S^2_{vg3}\,(g_{m3}/g_{m1})^2$
T5	$(g_{m5}/g_{m6})\,A_{v20}$	$S^2_{vg5}\,(g_{m5}/(g_{m6}\,A_{v10}))^2$
T6	A_{v20}	$S^2_{vg6}\,(1/A_{v10}))^2$
T7	$(g_{m7}g_{o13}/(2g_{m3}g_{m1})\,A_{v20}$	$S^2_{vg7}\,(g_{m7}g_{o13}/(2g_{m3}g_{m1})\,A_{v10})^2$
T8	A_{v70}-A_{v50}	$S^2_{vg8}\,(A_{v70}-A_{v50})^2$

Table 3.1 Contribution of transistor noise sources to the total output noise $A_{v10}=g_{m1}/g_{O24}$, $A_{v0}=A_{v10}A_{v20}$ [17]

3.3.1 PROPOSED OPERATIONAL AMPLIFIER ARCHITECTURE

In the application of the 1/f noise principle - the complementary MOSFET architecture - the 1/f noise reduction is achieved at the cost of the chip-area. When, for example, we replace all the transistors in a circuit with the principle, the chip area increases roughly by a factor of two. But when we apply the principle to “only” the main noise contributors instead, we can reach to the trade-off between the 1/f noise-reduction and the area-cost saving. Hence, the main noise contributing devices in the CMOS two-stage miller operational amplifier is investigated before applying the principle. Using Equation 2.25, all the noise voltages in the transistors can be represented as one equivalent input noise voltage as

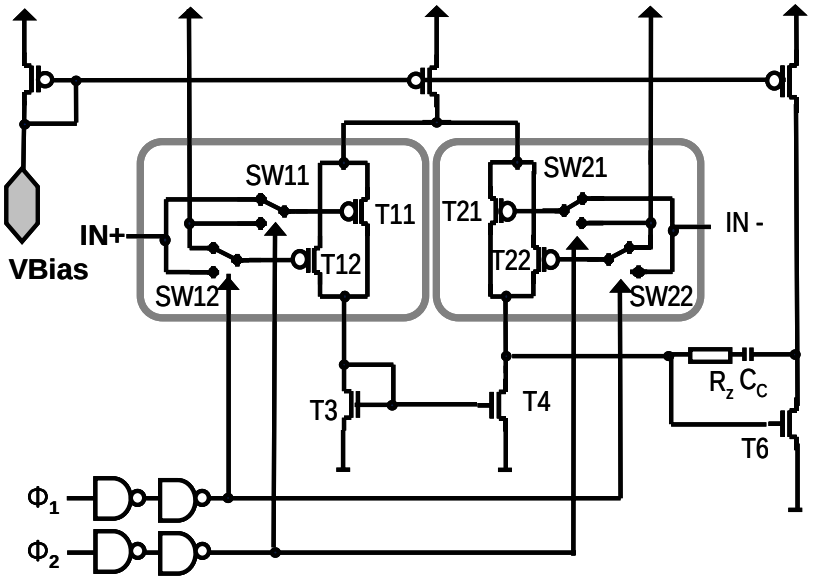


Figure 3.12 A modified operational amplifier for the 1/f noise reduction

$$S_{vin}^2 = \sum_{i=1}^{n} S_{vg_i}{}^2 \left(\frac{A_{vni}}{A_{v0}} \right)^2 \tag{3.15}$$

In Equation 3.15, $S_{vin}{}^2$ denotes the equivalent input noise voltage of the operational amplifier, and $S_{vg_i}{}^2$ is the equivalent noise voltage of transistor T_i. A_{vni} is the gain from the transitor T_i to the output. Table 3.1 collects the relevant expressions in Equation 3.14. It is apparent from Table 3.1 that the noise sources of transistor T5 to T8 are negligible when they are referred to the input as long as we assume a significant gain of the circuit. Thus, with the assumption that each transconductance of the input transistors (T1 and T2) and the load transistor (T3 and T4) are identical, and neglecting the noise contribution from the current sources the sum of the terms in the last column of Table 3.1 inserted into Equation 3.15 it approximates to:

$$S_{vin}^2 \approx 2S_{vg1}^2 + 2\left(g_{m3}^2 / g_{m1}^2\right) S_{vg3}^2 \tag{3.16}$$

Equation 3.16 indicates that only the two input transistors (T1 and T2) and the two load transistors (T3 and T4) among the transistors in the circuit have a significant contribution to the 1/f noise of the circuit. When assuming that the circuit has to be designed for low noise, especially the two input transistor (T1 and T2) have the strongest effect on the 1/f noise behavior. The ratio of the input and the load transistors transconductance (g_{m1}/g_{m3}) may be chosen by the designer in the best case that the 1/f-noise of the operational amplifier is determined by the input devices T1 and T2, i.e. g_{m1} is sufficiently greater than g_{m3}. This is mandatory in many cases since normally higher gain amplification is required in many applications.

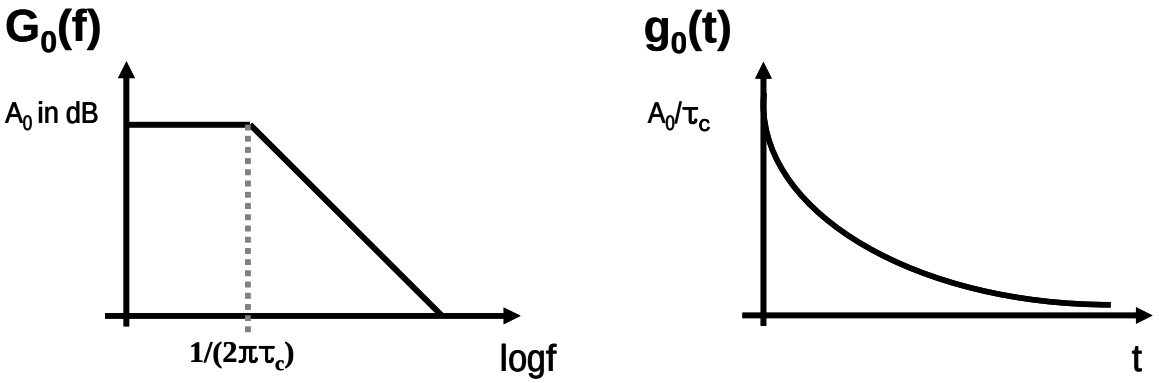


Figure 3.13 The left picture shows the transfer function $G_0(f)$ of the classic operational amplifier and the right picture shows the transfer function $g_0(t)$. Unlike $g_0(t)$, $G_0(f)$ is plotted on the log scale.

Now we present the "modified" operational amplifier architecture (Figure 3.12) after the principle is applied to the "classical" CMOS two-stage miller operational amplifier: the input transistors are replaced by the proposed transistors (T11, T12, T21 and T22) and switches (S11, S12, S21 and S22) from the Figure 3.5. For better rising/falling characteristic of the clocks in the chip, two matched pairs inverter are applied to the externally generated complementary clocks. During the Φ1 = VDD (Φ2 = VSS) phase the transistors T11 and T21 operate in inversion, while the transistors T12 and T22 are turned off (are operated in accumulation mode). Together with the next complementary clock phase, this enables a periodical switching of transistors T11 and T12, and T21 and T22 between inversion (operation mode for signal processing) and accumulation mode (relaxation mode for signal processing). This also enables a continuous operation of the operational amplifier. As stated in Chapter 3.2.2, the drain current of the input MOSFET exhibits a time-discontinuity at every half period of the clocks. The effect of this time-discontinuity on the signal transfer is detailed discussed in the next section.

3.3.2 SIGNAL TRANSFER FUNCTION

An amplified output signal y(t) of the operational amplifier due to an input signal x(t) is described using the transfer function g(t) as

$$y(t) = g(t) * x(t) \tag{3.17}$$

In the frequency domain, Equation 3.17 rewrites to

$$Y(f) = G(f) \cdot X(f) \tag{3.18}$$

In Equation 3.18, G(f) denotes the transfer function, X(f) and Y(f) are the input signal and the output signal in the frequency domain, respectively. In the case of the two-stage operational amplifier, the transfer function g(t) is of second order (two poles) and thus can be

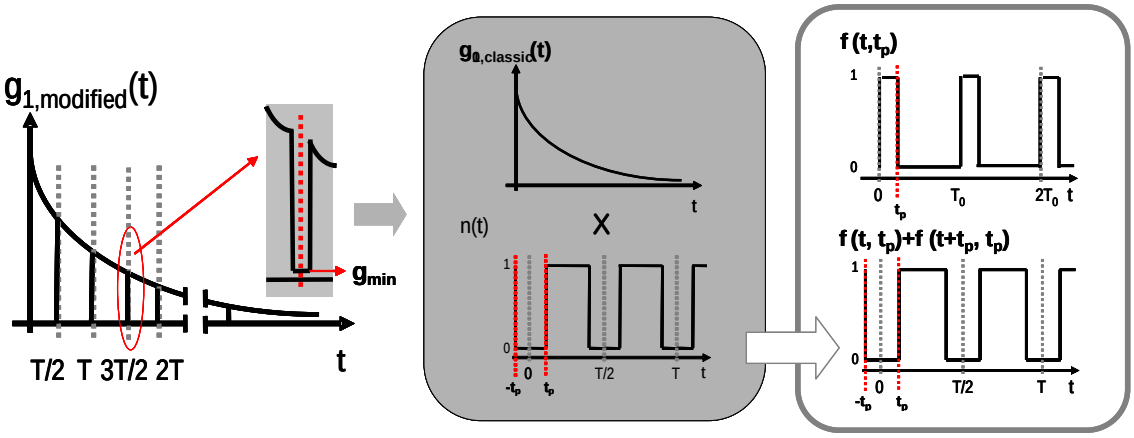


Figure 3.14 Transfer function of the 1st stage $g_{1,modified}(t)$ is explained by a product of $g_{1,classic}(t)$ and a periodic rectangular function n(t), where n(t) is mathematically obtained using $f(t,t_p)$

decomposed as

$$g(t) = g_2(t) * g_1(t) \quad \text{or} \quad G(f) = G_2(f) \cdot G_1(f) \tag{3.19}$$

Here $g_1(t)$ (or $G_1(f)$) and $g_2(t)$ (or $G_2(f)$) denotes the transfer function which correspond to the 1st gain stage and the 2nd gain stage of the operational amplifier. The transfer function of each stage has a form of a one-pole transfer function $g_0(t)$ (or $G_0(f)$) as

$$g_0(t) = \frac{A_0}{\tau_C}\exp(-\frac{t}{\tau_C}) \quad \text{or} \quad G_0(f) = \frac{A_0}{1 + j2\pi f\tau_C} \tag{3.20}$$

In Equation 3.20 A_0 denotes the small signal ac gain and τ_c is the 3dB bandwidth of the operational amplifier. Therefore the classic two stage CMOS mille operational amplifier in Chapter 3.2 has the transfer function:

$$g_{classic}(t) = \left(\frac{A_2}{\tau_{C2}}\exp(-\frac{t}{\tau_{C2}})\right) * \left(\frac{A_1}{\tau_{C1}}\exp(-\frac{t}{\tau_{C1}})\right) \quad \text{or} \quad G_{classic}(f) = \sum_i^2 \frac{A_i}{1 + j2\pi f\tau_{Ci}} \tag{3.21}$$

In the modified operational amplifier architecture using the proposed 1/f noise reduction technique, the "input complementary switched MOSFET architecture" causes a discontinuity in the drain current of the load transistors T3 (e.g.T4) at every half period of the applied complementary clocks. This discontinuous drain current also gives rise to a further periodic discontinuity in the gate-to-source voltage of T6 in the 2nd stage. This converts to the discontinuous voltage in the 2nd stage and finally a glitch voltage at every half period of the clocks is observed at the output node. Thus the transfer function in the time domain is also periodical discontinuous.

When we assume that only the transfer function of the 1st stage is "inherently" time-discontinuous, the transfer function of the 1st stage $g_{1,modified}(t)$ looks like as in Figure 3.14. Under this assumption, $g_{2,modified}$ is time-continuous and this assumption makes sense to some

degree. Although the discontinuous signal transfer is also expected in the 2nd stage, it does not occur inherently but indeed is induced. When we make the further assumption that the minimum of $g_{1,modified}(t)$ reaches zero, the transfer function $g_{1,modified}(t)$ is explained by a product of $g_{1,classic}(t)$ and a periodic rectangular function n(t) as in Figure 3.14. There, n(t) is defined as:

$$n(t)=1 \quad t\in[t_p, T/2-t_p] \qquad \text{and} \qquad n(t)=0 \quad t\notin[t_p, T/2-t_p] \tag{3.22}$$

and mathematically expressed as

$$n(t)=1-[f(t+t_p,t_p)+f(t,t_p)] \tag{3.23}$$

In Equation 3.23, a periodic rectangular function $f(t,t_p)$ varies between 0 and 1 with a duty cycle D, which is defined as $D=t_p/T_0$(Figure 3.13). Details on obtaining $f(t,t_p)$ are given in Appendix A.2.

Now the transfer function of the 1st stage $g_{1,modified}(t)$ is expressed as

$$g_{1,\mathrm{mod}ified}(t)=g_{1,classical}(t)\cdot n(t) \tag{3.24}$$

The whole transfer function $g_{modified}(t)$ is given as

$$g_{\mathrm{mod}ified}(t)=g_{2,classical}(t)*(g_{1,classical}(t)\cdot n(t)) \tag{3.25}$$

Equation 3.25 rewrites to

$$g_{\mathrm{mod}ified}(t)=\left(g_{2,classical}(t)*g_{1,classical}(t)\right)\cdot n(t)=g_{classical}(t)\cdot n(t) \tag{3.26}$$

From Equation 3.26, the transfer function $G_{modified}(f)$ in the frequency domain is obtained as

$$G_{\mathrm{mod}ified}(f)=G_{classical}(f)*N(f) \tag{3.27}$$

In Equation 3.27, N(f) is the Fourier transformed expression of n(t) and it is given as

$$N(f)=\left(1-2\cdot\frac{t_p}{T_0}\right)\delta(f)-\sum_{k=1}^{\infty}\frac{1}{k\cdot\pi}\sin(2\pi\cdot k\frac{t_p}{T_0})\cdot\left(\delta(f-k\cdot f_0)+\delta(f+k\cdot f_0)\right) \tag{3.28}$$

Taking it into account that the period T_0 is a half of the applied complementary clock period T_{clk}, Details in obtaining $M_0(f)$ are given in Appendix A.2. Now Equation 3.28 yields

$$N(f)=\left(1-\frac{4t_p}{T_{clk}}\right)\delta(f)-\sum_{k=1}^{\infty}\frac{1}{k\cdot\pi}\sin(4\pi\cdot k\frac{t_p}{T_{clk}})\cdot\left(\delta(f-2k\cdot f_{clk})+\delta(f+2k\cdot f_{clk})\right) \tag{3.29}$$

$$N(f)=\left(1-\frac{4t_p}{T_{clk}}\right)\delta(f)-\sum_{k=-\infty,k\neq 0}^{\infty}\frac{1}{k\cdot\pi}\sin(4\pi\cdot k\frac{t_p}{T_{clk}})\cdot\left(\delta(f-k\cdot f_{clk})\right) \tag{3.30}$$

When t_p is much smaller than T_{clk},

$$\sin(4\pi\cdot k\frac{t_p}{T_{clk}})\sim 4\pi\cdot k\frac{t_p}{T_{clk}} \tag{3.31}$$

Thus,

$$G_{modified}(f)\approx\left(1-\frac{4\cdot t_p}{T_{clk}}\right)G_{classical}(f)-\frac{4\cdot t_p}{T_{clk}}\sum_{k=1}^{\infty}\cdot\left(G_{classical}(f-2k\cdot f_{clk})+G_{classical}(f+2k\cdot f_{clk})\right) \tag{3.32}$$

Equation 3.32 can be represented as

$$G_{modified}(f)=\sum_{-\infty,n=even}^{\infty}H_n(f-n\cdot f_{clk})=G_{classical}(f)-\frac{4\cdot t_p}{T_{clk}}\sum_{-\infty,n=even}^{\infty}G_{classical}(f-n\cdot f_{clk}) \tag{3.33}$$

In the time domain, we get:

$$y(t)\approx g_{classic}(t)*x(t)-\frac{4\cdot t_p}{T_{clk}}\sum_{-\infty,n=even}^{\infty}g_{classic}(t)*x(t)\exp(j2\pi n\cdot f_{clks}t) \tag{3.34}$$

Equation 3.33 indicates several dinstinct features of the modified operational amplifier for the 1/f noise reduction.

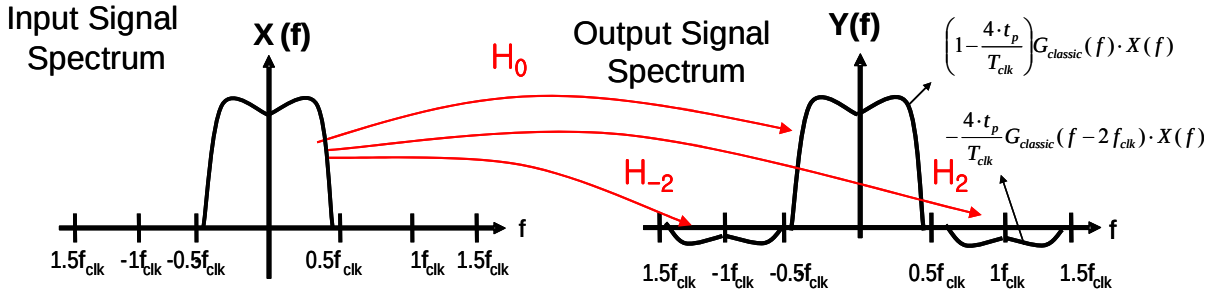


Figure 3.15 Baseband function $H_0(f)$ and transfer function H_2/H_{-2} when the signal bandwidth of the input signal X(f) is smaller than the f_{clk}.

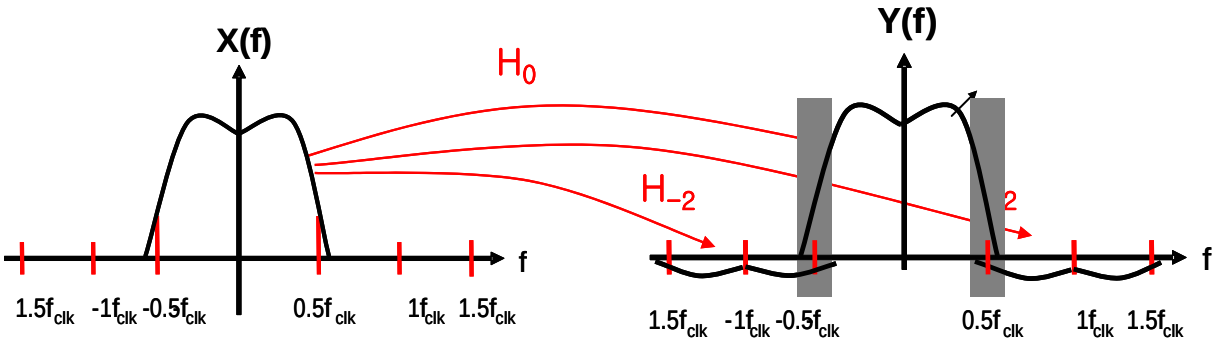


Figure 3.16 Baseband function $H_0(f)$ and transfer function H_2/H_{-2} when the signal bandwidth of the input signal X(f) is greater than the f_{clk}. Available output signal is reduced in the dark area in the right.

First, the replicas ($H_n(f-nf_{clk})$, when n≠0 in Equation 3.31) of the original signal exits at every "even" times f_{clk}. Interestingly, the replicas are out of phase of the original signal and the reduced amplitude by a factor of $4t_p/T_{clk}$. This is illustrated in Figure 3.15 in the case that the signal bandwidth of X(f) is less than the clock frequency. In Figure 3.15, the transfer function $H_0(f)$ is of a particular interest since it describes the linear (wanted) operation of the amplifier. Otherwise other transfer function $H_n(f)$, when n≠0, describe the nonlinear(unwanted) behavior of the amplifier. The effective DC gain of the proposed operational amplifier and the unity-gain bandwidth is less than that of the classical operational amplifier by a factor of $1-4t_p/T_{clk}$. This is apprent from Equation 3.35 where $H_0(f)$ is taken from Equation 3.33

$$H_0(f)=\left(1-\frac{4\cdot t_p}{T_{clk}}\right)\cdot G_{classical}(f)=\left(1-\frac{4\cdot t_p}{T_{clk}}\right)\cdot\left(\frac{A_0}{1+j2\pi f/2\pi f_C}\right) \tag{3.35}$$

In Equation 3.35 we assume that $G_{classical}(f)$ has a one-pole transfer function $G_0(f)$ in Equation 3.20.

Second, the clock frequency f_{clk} should be considerably greater than the maxmmal signal bandwidth of X(f), namely input signal should be a band-limited signal X(f< f_{clk}). In the case that the clock frequency f_{clk} is less than the signal bandwidth of X(f), X(f> f_{clk}), the available bandwidth of Y(f) will be limited (signal aliasing) as shown in Figure 3.16. For example, when X(f> f_{clk}), the base-band transfer function is given as

$$\left(1-\frac{4\cdot t_p}{T_{clk}}\right)\cdot G_{classical}(f)-\frac{4\cdot t_p}{T_{clk}}G_{classical}(f-2f_{clk}) \tag{3.36}$$

Equation 3.36 rewrites to

$$\left(1-\frac{4t_p}{T_{clk}}\right)\cdot\left(\frac{A_0}{1+j2\pi f/2\pi f_C}\right)-\frac{4t_p}{T_{clk}}\left(\frac{A_0}{1-j2\pi(f-2f_{clk})/2\pi f_C}\right) \tag{3.37}$$

Equation 3.35 and 3.36 indicates, the case of X(f> f_{clk}) limits the available bandwidth of Y(f). Especially, in this case, DC gain reduces by a factor of $4t_p/T_{clk}$, compared to the case that the clock frequency f_{clk} is no less than the signal bandwidth of X(f). This case results in a noise aliasing into the singal band when we recall the noise alnalysis of the complementary switched MOSFET architecture from Chapter 3.2.2. The noise alaisign will occur at odd harmonics of the clock frequency flck, and thus a serious noise aliaisng will reside in the signal band, when the clock frequency f_{clk} is less than the signal bandwidth of X(f).

Third, when $4t_p/T_{clk}$ goes to zero (or is negligibly small), $H_0(f)$ appoaches to that of the classical operational amplfiier and furthermore $H_n(f-nf_{clk})$, when $n\neq0$, will goes to zero. Under this condition,

$$G_{modified}(f) \approx G_{classical}(f) \tag{3.38}$$

Of course, this is an ideal case that we can not reach but only get close to. But, it should be noted that this condition implies the optimization of the clock mismatch parameter t_p is a need in terms of signal transferring. And detailed noise analysis in the proposed operational amplifier is given in Chapter 5 with experimental results.

3.4 REFERENCES FOR CHAPTER 3

[1] P. R. Gray and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, New York, John Wiley & Sons, 1993

[2] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: auto zeroing, correlated double sampling and chopper stabilization," Proceedings of the IEEE, vol. 4, pp.1584-1614, 1996

[3] A. P. van der Wel, E. A. M. Klumperink, S. L. J. Gierkink, R.F. Wassenaar, and H. Wallinga, "MOSFET 1/f noise measurement under switched bias conditions," IEEE Electron Device Letters, vol. 21,pp. 43 – 46, 2000.

[4] I. Bloom and Y. Nemirovsky, "1/f Noise Reduction of Metal-Oxide-Semiconductor Transistors by cycling from inversion to accumulation," Applied Physics Letters, vol. 58, pp. 1664-1666, 1991.

[5] B. Dierickx and E. Simoen, "The Decrease of Random Telegraph Signal Noise in Metal-Oxide-Semiconductor Field-Effect Transistors when cycled from inversion to accumulation," Journal of Applied Physics, vol. 71, pp. 2028-2029, 1992.

[6] J. S. Kolhatkar, C. Salm, M. J. Knitel, and H. Wallinga "Constant and Switched Bias Low Frequency Noise in p-MOSFETs with Varying Gate Oxide Thickness," The proceeding of the 29th European Solid State Device Research Conference 2002, 2002

[7] J. S. Kolhatkar, E. Hoekstra, C. Salm, A. P. van der Wel, E. A. M Klumperink, J. Schmitz and H. Wallinga, "Modeling of RTS noise in MOSFET under Steady-state and Large-signal Excitation," Digest of Technical Paper International Electronic Device Meeting, pp.140-143, 2004

[8] Z. Zhang and J. Lau, "Experimental on MOSFET's flicker noise under switching conditions and modelling in RF applications," The proceedings of Costumed Integrated Circuit Conference, pp.142-145, 2001

[9] H. Tian and A.E. Gamal, "Analysis of 1/f noise in switched MOSFET circuits, " IEEE Transactions on Circuits and Systems II, vol. 48, pp. 151-157, 2001.

[10] A. P. van der Wel, E. A. M. Klumperink, L. K. J Vandamme, and B. Nauta, "Modeling Random Telegraph Noise under Switched Bias Conditions Using Cyclostationary RTS Noise;" IEEE Transaction on Electron Devices, Vol. 50, No.5, pp.1378-1384, 2003

[11] S. L. J. Gierkink, E. A. M. Klumperink, A. P. van der Wel, G. Hoogzaad. J. M. van Tuijl, and B. Nauta, "Intrinsic 1/f device noise reduction and its effect on phase noise in CMOS ring oscillators, " IEEE Journal of Solid-State Circuits, vol. 34, pp.1022-1025, 1999

[12] R. Thewes, J. Koh and R. Brederlow, "Prinzip und dessen schaltungstechnische Umsetzung zur Verringerung des niederfrequenten Rauschens von MOS-Transistoren in Schaltungen", Deutsche Patentanmeldung DE.814758

[13] J. Koh, R. Thewes, D. Schmitt-Landsiedel and R. Brederlow, "A Circuit Design based Approach for 1/f-noise Reduction in Linear analog CMOS IC's," Digest. of Technical Paper VLSI Symposium on the Circuit, 2004, pp.222-225, 2004

[14] E. Kreyzig, Advanced Engineering mathematics, 7th edition, John Wiley & Sons, New York, 1993

[15] P. Tadeparthy, "An improvement frequency compensation technique for low power, low voltage CMOS amplifiers," Proceedings of the ISCAS, pp.497-500, 2004

[16] P. G. Drennan, C. C. McAndrew, "Understanding MOSFET Mismatch for Analog Design," IEEE Journal of Solid-State Circuits, vol. 38, pp.450-456, 2003

[17] K. Laker and W. Sansen, Design of Analog Integrated Circuits and Systems, Boston, McGraw-Hill, 1994

CHAPTER 4
CIRCUIT IMPLEMENTATIONS

This chapter is dedicated to the discussion of the design-considerations and the implementation-issues of the 1/f noise reduction demonstrating example: the operational amplifier which includes the 1/f noise reduction principle from Chapter 3 (Figure 3.8). First, a short brief of submicron CMOS technology is introduced since submicron CMOS linear analog IC design requires a solid understanding of the technology in use for the design. Subsequently two design examples are presented: a classic two stage CMOS miller operational amplifier and the proposed operational amplifier which includes the 1/f noise reduction principle. The classic operational amplifier serves itself as a reference for the performance comparison with the proposed one. The proposed operational amplifier is modified from the classic operational amplifier by replacing the input transistor with the proposed transistor architecture for the 1/f noise reduction. Both of the operational amplifiers are fabricated in a 120nm 1.5 V CMOS technology.

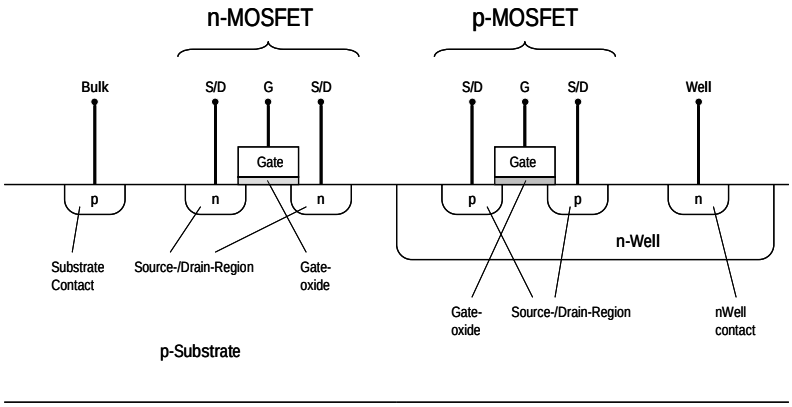


Figure 4.1 Schematic cross section of the CMOS twin well process used for the design and the implementation of the demonstrator circuit.

4.1 DESIGN OF A CMOS MILLER OP AMP

This section includes the design considerations of a classic CMOS two stage miller operational amplifier which will be modified later for the demonstration of the proposed principle for the 1/f noise reduction. This design will serve as a reference for the performance of the later discussed operational amplifier which includes the noise reduction principle.

4.1.1 PHYSICAL CONSIDERATIONS

The CMOS technology, which is used for the design and implementation, is based on the p-type substrate twin well process and has a list of active and passive devices. A technology cross-section is shown in Figure 4.1. Performances of the devices available in the technology are primarily optimized for digital application. This is because the digital functional blocks today consume most of the die area for a system-on-a-chip. The digital-application-optimized process renders the analog designer reluctant to use of it. However, today, it becomes a trend that the analog functional blocks are designed in the digital-application-optimized process for a system-on-a-chip application.

In the design of the linear analog circuit, the following consideration should be taken into account: Most linear analog circuits need the transistors in the circuit to operate in saturation region. That is, the drain-to-source voltage V_{DS} is high enough so that the inversion layer does not extend all over from drain to source. In this case, the channel charge stays constant and correspondingly the drain current I_D in saturation region is also almost constant even when the drain-to-source voltage V_{DS} is rising. The transistor works as a gate voltage controlled current source. In a simple long-channel device approximation, the drain current I_D of the MOS

transistor is given as

$$I_D = \mu_{n,p} C_{ox} \left(\frac{W}{L} \right) \left(V_{GS} - V_T \right)^2 \left(1 + \lambda V_{DS} \right) \tag{4.1}$$

In Equation 4.1 W is the device-width and L is the gate-length. μ denotes the mobility, where the subscript n and p stand for NMOS and PMOS transistor, respectively, and λ is the channel length modulation parameter. C_{ox} is the total gate oxide capacitance per unit area and given by

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{4.2}$$

In Equation 4.2 ε_{ox} and t_{ox} denote the dielectric constant and the thickness of the oxide.

In the saturation region, the drain-to-source voltage V_{DS} is specified by $V_{DS,SAT}$ which is defined as

$$V_{DS,SAT} = V_{GS} - V_T \tag{4.3}$$

Now the drain current in the saturation region is obtained using Equation 4.3 from Equation 4.1.

$$I_D = \mu_{n,p} C_{ox} \left(\frac{W}{L} \right) \left(V_{GS} - V_T \right)^2 \left(1 + \lambda V_{DS} \right) \tag{4.4}$$

Recalling from Equation 4.4, the drain current I_D in saturation has a square-law dependence on the gate-to-source voltage V_{GS} and is partially dependent of drain-to-source voltage V_{DS}. Figure 4.2 and Figure 4.3 presents the drain current I_D of the NMOS transistor (V_T = 0.273 V) and the pMOS transistor (V_T=0.256 V) with a drawn-gate-length L of 1 um and a drawn-device-width W of 24 um. This geometry is in use for the input transistors of the operational amplifier. Second, the transconductance g_m and the output transconductance g_{ds} of the MOS transistor are one of the most important design parameter in the linear analog circuit, since most linear analog circuit requires amplification of a signal, where amplification is usually given by the ratio of the transconductance gm and output conductance gds. The transconductance g_m of the device is defined as $\partial I_{DS} / \partial V_{GS}$.

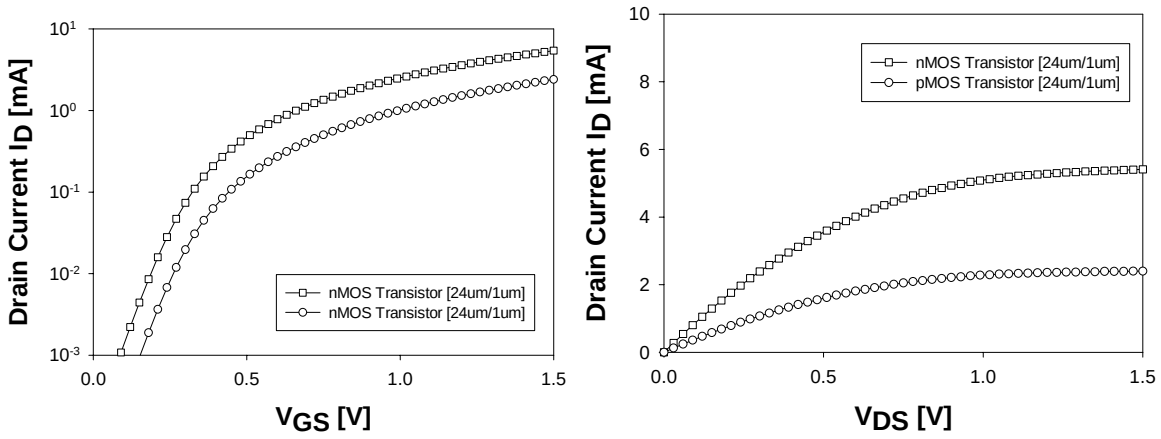


Figure 4.2 Left shows the drain current I_D versus the gate-to-source voltage V_{GS} when the-drain-to-source voltage V_{DS} is biased to 1.5V and right shows the drain current I_D versus the drain-to-source voltage V_{DS} when the gate-to-source voltage V_{GS} is biased to 1.5 V

In saturation region, it is easily found by differentiating the expression in Equation 4.4 for the drain current I_D as

$$g_m = \mu_{n,p} C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_T) \tag{4.5}$$

Equation 4.5 can also be expressed as

$$g_m = \sqrt{2\mu_{n,p} C_{ox} \left(\frac{W}{L} \right) I_D} \tag{4.6}$$

The output conductance g_{ds} of the device is defined as $\partial I_{DS} / \partial V_{DS}$. From Equation 4.4, the output conductance is obtained as

$$g_{ds} = \lambda \mu_{n,p} C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_T)^2 \equiv \lambda I_{DS0} \tag{4.7}$$

In Equation 4.6, I_{DS0} denotes the drain current when the channel length modulation effect is ignored. Figure 4.3 depicts the transconductance g_m of NMOS and PMOS transistors with a drawn-gate-length L of 1 um and a drawn-device-width W of 24 um.

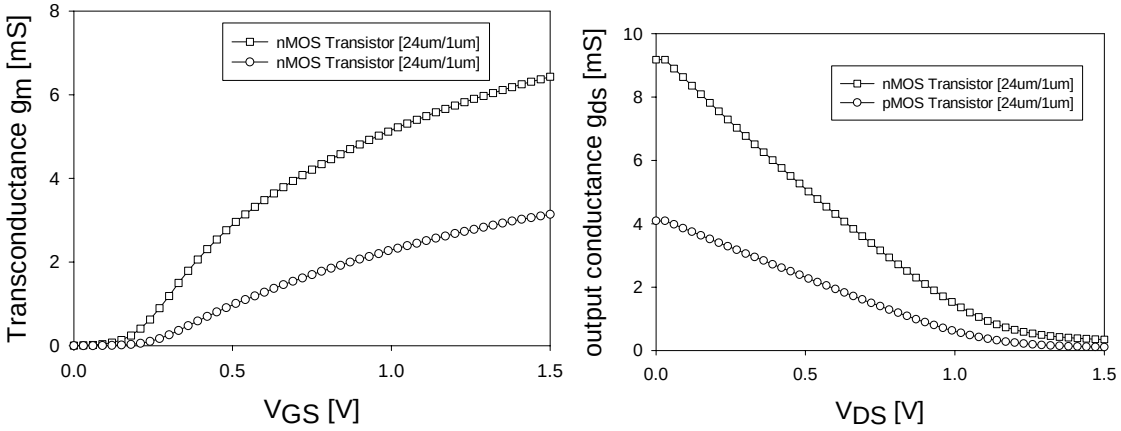


Figure 4.3 Left shows the transconductance g_m of NMOS and PMOS transistors when the drain-to-source voltage V_{DS} is biased to 1.5 V and right depicts the output conductance g_{ds} of NMOS and PMOS when the gate-to-source voltage V_{GS} is biased to 1.5 V

When we take a look at Equation 4.6, the greater mobility of the NMOS transistor also results in a higher transconductance. Normally the NMOS transistor is more preferred in high speed circuits, due to its higher speed compared to the PMOS transistor. This can be explained by the greater mobility of electrons μ_n compared to holes μ_p as

$$\mu_n \approx 2.5\mu_p \tag{4.8}$$

Irrespective of superiority in the speed and the transconductance g_m of the NMOS transistor, the use of it as an input transistor in the differential stage of an operational amplifier is sometimes reluctant. Especially in the low noise electronic design, the PMOS transistor is widely used in the differential stage of the operational amplifier, where the more robustness is of great concern compared to the high speed performance: the NMOS transistor normally shows worse 1/f noise behavior than the PMOS transistor [1]. In the application of the proposed 1/f noise reduction principle to a CMOS operational amplifier, the PMOS transistor as an input device is a better choice: two complementary full swing clocks switches the two identical transistors when the principle is in use. This switching may degrade the circuit performance by substrate switching noise (Figure 4.1), where it is impossible to make an individual well contact for an NMOS transistor. All NMOS transistors on the chip in a twin well process have to share the same substrate and thus the resulting switching noise may propagate through the common substrate. Otherwise a triple well CMOS platform can minimize this substrate switching problem with a deep n-well option [2]. In conclusion, in the noise reduction point of view, it is more attractive to configure a differential operational amplifier with a PMOS input transistor and replace the input PMOS transistors with the 1/f noise principle in a twin-well CMOS technology. Therefore the example is build with PMOS input transistors in the following.

4.1.2 PHYSICAL IMPLEMENTATION

Design specifications for operational amplifiers are determined by the application of the operational amplifier. The target application finds where operational amplifiers 1/f noise is of great concern. Examples are audio amplifiers, weak signal sensing systems like image sensor amplifiers and so on. A few MHz gain-bandwidth-products is enough for these applications.

A stable negative feedback operation of the op amp is of high importance in these applications. One of the most significant benefits of negative feedback is the stabilization of the gain of the amplifier against parameter changes in the active devices due to supply voltage variation, temperature changes, or device aging. Another significant benefit is the reduction in signal waveform distortion of negative feedback, and for this reason, almost all high-quality audio amplifier employs a negative feedback. However, the use of negative feedback increases the tendency for oscillations in the circuit, and careful attention is required to overcome this problem. Thus enough phase margin (of more than 60 degree) should be guaranteed. For the increase in signal range, an operational amplifier should have low nonlinearity and a good immunity to second order effects, e.g. the ability to suppress common mode signal gain or power supply fluctuations.

Apart from these, in the design of the core op amp, the following considerations are specially taken into account: despite of input devices being typically small for low input capacitance and therefore having significant contribution to the 1/f noise, the input-devices should dominate the total noise behaviour of the op amp for demonstration purposes here. The noise ratio of the input transistors to the total noise of the operational amplifier (Figure 3.7) is given in the following from Equations 3.1 and 3.2.

$$\frac{2S_{vg1}^2}{S_{vin}^2} = \left(1 + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \left(\frac{S_{vg3}}{S_{vg1}}\right)^2\right)^{-1} \tag{4.9}$$

Substituting the standard 1/f noise spice model (Equation 4.10)

$$S_{vgp}^2 = \frac{S_{IDn}^2}{g_{mn}^{\ 2}} = \frac{k_{fn} I_{dsn}}{C_{oxn} L_{effn}^{\ 2} g_{mn}^{\ 2}} \cdot \frac{1}{f} \text{ and } S_{vgp}^2 = \frac{S_{IDp}^2}{g_{mp}^{\ 2}} = \frac{k_{fp} I_{dsp}}{C_{oxp} L_{effp}^{\ 2} g_{mp}^{\ 2}} \cdot \frac{1}{f} \tag{4.10}$$

[3] [4] into Equation 4.9 refers to the 1/f noise of the operational amplifier as given in Equation 4.11. In Equation 4.10 subscript n and p denote for nMOSFET and pMOSFET, respectively.

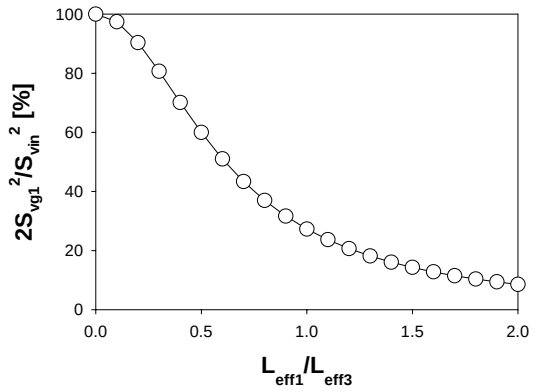


Figure 4.4: The contribution of the input devices to the total noise is a function of the gate length ratio of the input transistor L1 and the load transistor L3

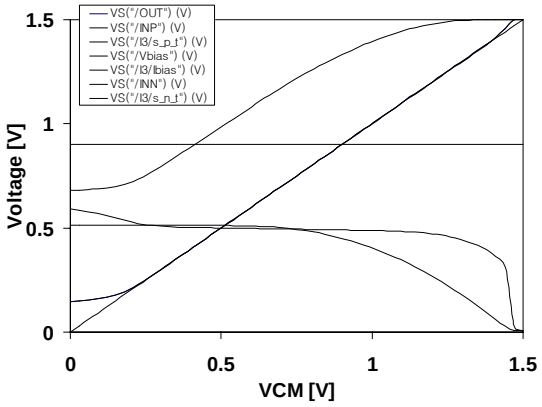


Figure 4.5 The internal DC bias point of the operational amplifier as the input common VCM varies from VSS to VDD. The node names are denoted in Figure 3.11

$$\frac{2 \cdot S_{vg1}^2}{S_{vin}^2} = \left(1 + \left(\frac{k_{f3}}{k_{f1}} \right) \left(\frac{L_{eff1}}{L_{eff3}} \right)^2 \right)^{-1} \tag{4.11}$$

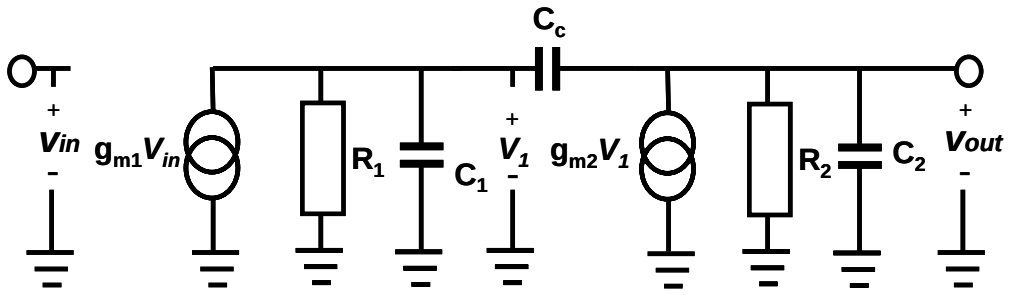
As depicted in Figure 4.4, the contribution of the input devices to the total noise is a function of the gate length ratio of the input transistor L_1 and the load transistor L_3. In the operational amplifier as designed here, the input device has about 75% contribution to the total noise which is related to a L_1/L_3 ratio of 0.3.

With this gate length ratio kept, the design procedure (device sizing) proceeds has to make sure that all transistors in the circuit operate in the saturation region or that the drain-to-source voltage V_{DS} of a transistor is kept greater than the effective gate-to-source voltage V_{GSeff}, which is given as the difference between the gate-to-source voltage V_{GS} and the threshold voltage V_T as in Equation 4.11.

$$V_{DS} \geq V_{GSeff} \approx V_{GS} - V_T \tag{4.12}$$

The effective gate-to-source voltage $V_{GSeff,}$ of the input transistors is written in Equation 4.7 with the process parameters, the drain current and the geometric parameter.

$$V_{GSeff} = V_{GS} - V_T = \sqrt{\frac{2I_D}{\mu \cdot C_{ox}(W/L)}} \tag{4.13}$$



`Figure 4.6 Small-signal equivalent circuit of the operational amplifier

A sufficient gate-to-source effect voltage V_{GS}- V_T should be guaranteed to ensure that the input transistors operate in the strong inversion regime. This is the most important requirement to make the 1/f noise reduction feasible. A sufficient gate-to-source effect voltage $V_{GS,}$ maximizes the 1/f noise reduction effect when a MOS transistor periodically-switched operates between strong inversion and accumulation state [5, 6, 7, 8]. The bias condition of the transistors in the operational amplifier is depicted in Figure 4.5 when the input common mode voltage V_{CM} varies from VSS to VDD. When the input common mode voltage V_{CM} is about the middle of VDD-VSS (750mV), the input PMOS transistor has the source-to-gate effective voltage V_{SG}- V_T of about 220mV (with V_T = 230mV) and operates in the saturation region. This guarantees the operation of the input transistors T1 and T2 in strong inversion regime [9].

Figure 4.6 represents the small-signal equivalent network of the two stage CMOS Miller operational amplifier, where each amplification stage is modelled as one voltage-controlled current source, output capacitor and output resistor. In two stage CMOS Miller operational amplifier, the first stage connects to the second stage through Miller capacitor C_C for the frequency compensation as shown in the figure.

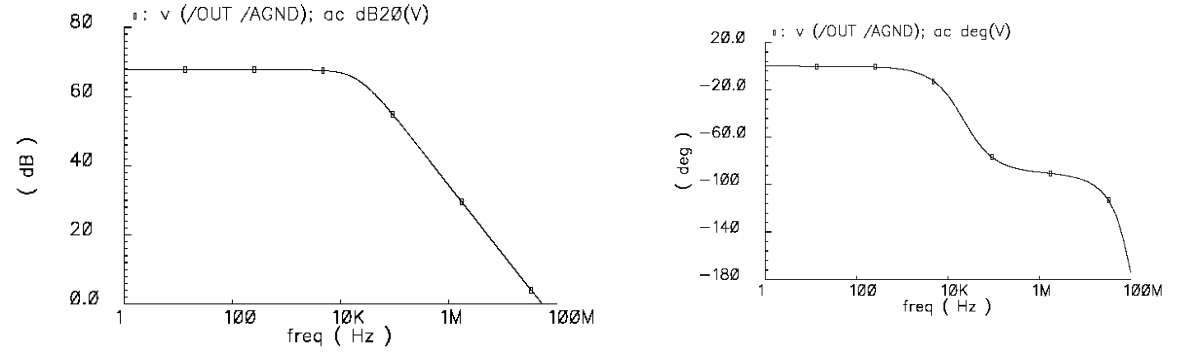


Figure 4.7 Left shows the simulated open loop small signal ac gain plot versus frequency and right shows the phase margin plot versus frequency

The corresponding small-signal transfer function is given as

$$\frac{V_O(s)}{V_{in}(s)} = \frac{g_{m1}g_{m2}R_1R_1(1-sC_C/g_{m2})}{1+s[R_1(C_1+C_C)+R_2(C_2+C_C)+g_{m2}R_1R_2C_C]+s^2R_1R_2[C_1C_2+C_CC_1+C_CC_2]} \quad (4.14)$$

Where $s = jw = j2\pi f$ and $j = \sqrt{-1}$. Equation 4.14 reduces to

$$\frac{V_O(s)}{V_{in}(s)} = \frac{A_v(1-s/z_1)}{(1+s/p_1)(1+s/p_2)} \quad (4.15)$$

As Equation 4.14 depicts the two stage CMOS Miller operational amplifier has a two dominant poles (p_1 and p_2) and one zeros (z_1) and they are represented as

$$p_1 \cong \frac{-1}{g_{m2}R_1R_2C_C}, \quad p_2 \cong \frac{-g_{m2}C_C}{C_1C_2+C_2C_C+C_1C_C} \approx \frac{-g_{m2}}{C_2} \quad \text{and} \quad z_1 \cong \frac{g_{m2}}{C_C} \quad (4.16)$$

Figure 4.6 depicts the open-loop small-signal gain and the corresponding phase margin of the operational amplifier. About 72 dB small-signal-amplification and 65 degree phase margin is achieved using a 1.2pF miller capacitor C_C in a capacitive load of 5pF. This enables the operational amplifier to operate stabile in a negative feedback configuration for the relevant 1/f noise measurement. In addition, several simulated performances of the operational amplifier are summarized in Table 4.1 Figure 4.8 shows the layout of the operational amplifier in 0.12 um 1.5 V CMOS standard logic process.

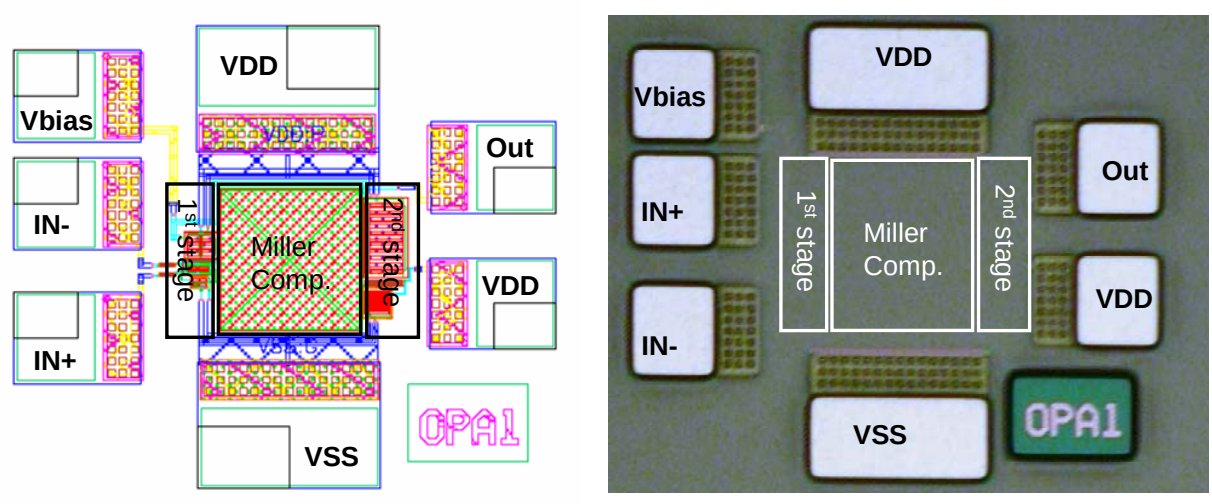


Figure 4.8 Layout (left)and chip photo (right) of the classic CMOS two stage miller operational amplifier

Simulated performance @ 5pF load	
Open loop Gain	68.3 dB
3dB Bandwidth	21.6 kHz
GBW	52.5 MHz
Phase Margin	60 °
Power Consumption	1.4mA@1.5V
Area	0.20mm x 0.21mm

Table 4.1 Simulated performances of the operational amplifier

4.2 DESIGN OF THE PROPOSED OPERATIONAL AMPLIFIER

In this section, the design-considerations on the 1/f noise reduction principle (the switched MOSFET architecture) and issues of applying it to the foregoing operational amplifier are discussed.

4.2.1 DESIGN CONSIDERATIONS

The switch finds many applications in integrated circuit design. In analog circuits, the switch is used to implement such useful functions as the switched capacitor realization of an analog resistor. In the 1/f noise reduction principle, in Figure 4.10 (a), the switch (e.g. SW11) acts as a multiplexer that connects the highest potential (VDD) and a potential at the node G (VG) to the gate of the input PMOS transistors (e.g. T11) on each half cycle, respectively. For this purpose, the switches SW11 and SW12 are composed of two switches, S1 and S2 as shown in the figure. For examples, in the switch SW11, the switch S1 conducts a certain potential at the node G (VG) to the gate (e.g. G11) of the PMOS transistor T11, where VG includes a DC bias and an ac signal source to be delivered. A CMOS transmission gate is used for the switch S1 since it has a larger dynamic control signal range than a single channel MOS switch when it is turned on [10]. A single channel MOS switch (e.g. NMOS switch) used instead would limit the control ac signal range because it needs a higher voltage than the threshold voltage at the (drain or) source node for the switch to operate properly [10]. This will limit the available input dynamic common mode range of the operational amplifier (Figure 3.8) in a feedback configuration (e.g. unity-gain configuration) when the common mode dc level is close to VDD or when the ac signal source is large enough to approach to VDD.

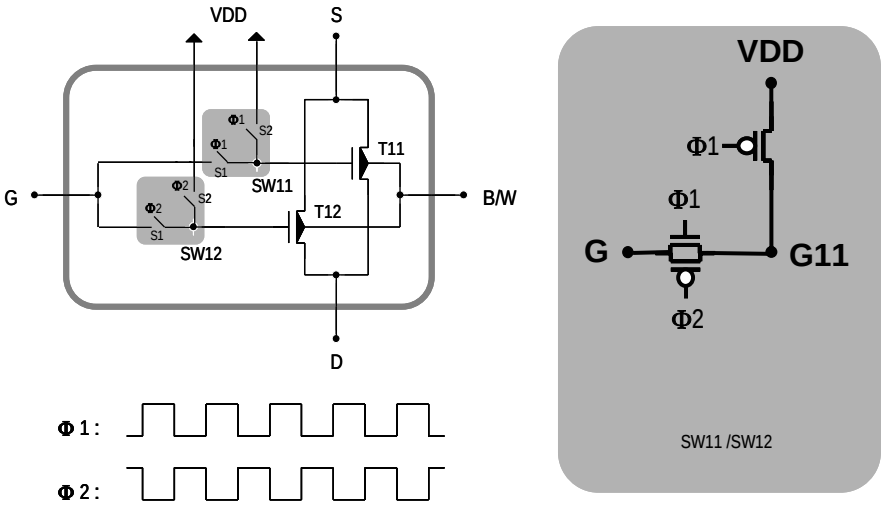


Figure 4.9 Implementation of the 1/f noise principle with a MOS switch

Otherwise, a single-channel PMOS transistor implements the switch S2. The switch S2 conducts a full range of VDD to the gate of the PMOS input transistor. For full switching behavior close to VDD at the source or drain of the switching transistor, a PMOS switch is more adequate than an NMOS one. An NMOS single-channel switch, however, is more suitable for good switching operation close to VSS or GND in the signal path.

Generally the on-state of a switch is characterized as a resistor, which is called the on-resistance R_{ON} and a load capacitor C_{load} as shown in Figure 4.10.

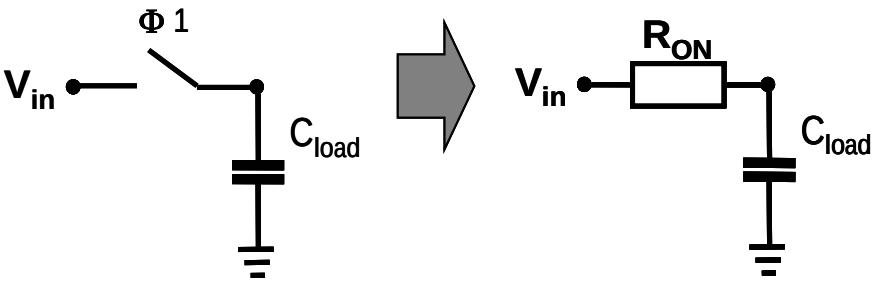


Figure 4.10 On-state of a MOS switch

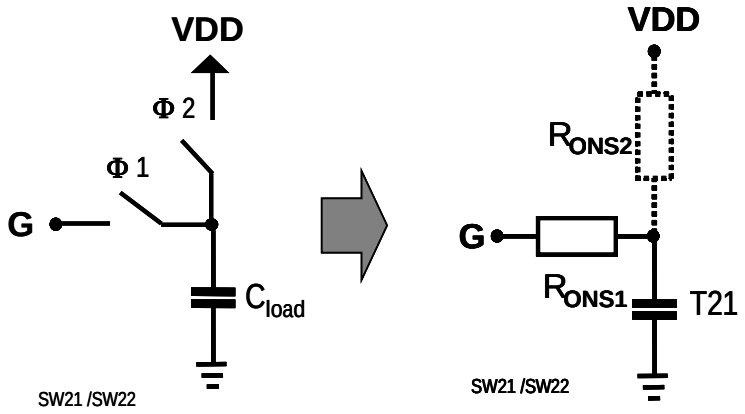


Figure 4.11 On-state of the switch SW11 and SW12

The on-state of the switch SW11 (or SW12) is shown in Figure 4.11, where two switches S1 and S2 have own on-resistance R_{ON} (e.g. for S_1, R_{ONS1} and for S_2, R_{ONS2}) and the input capacitance of the PMOS transistor T11 (or T12), additional load capacitance (Equation 4.17)

The size of the switch determines the on-resistance R_{ON} as follows

$$R_{ON} = \frac{1}{\partial I_D / \partial V_{DS}} = \frac{1}{\mu_p C_{ox}(W/L)(V_{GS} - V_T)} \tag{4.17}$$

$$C_{load} = C_{gs} + C_{gb} + C_{gd} \tag{4.18}$$

For distortion-free operation of the switch for signal transfer, $R_{on}C_{load} << T_{clk}$ is required where the clock period T_{clk} is the time when the clock Φ1 (or Φ2) is high. In Figure 4.12, the highest value for R_{on}, which varies greatly with the input voltage V_{in}, during the charging or discharging of C_{load} (when V_{DS}=0 and V_{GS}= Φ1-V_{in}) is used for sizing the transistors to achieve the desired charging or discharging time [10].

A care should be taken to the on-resistance and capacitance of the switches concerning switching noise; thermal noise integrated at the input capacitance. The dominant noise in the switch is the thermal noise (Equation 2.17) [11]. Where the on-resistor of the switch is in series with a load capacitor in Figure 4.10, the signal transfer function is given as

$$H(f) = \frac{1}{1 + j2\pi \cdot f \cdot R_{on}C_{load}} \tag{4.19}$$

The noise power is independent upon the on-resistance of the switch, but dependant upon the load capacitance.

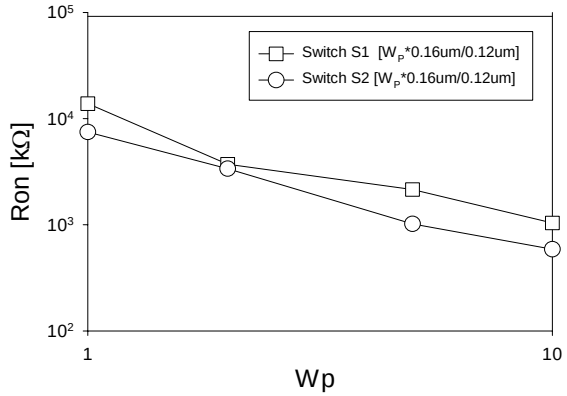


Figure 4.12. On-resistance of the switch S1 and S2 as the device-width increased, where Wp is the multiple of the minimum switch area

$$P_N = S_{v,thermal}\int_0^{\infty} H(f)^2\,df = \frac{4kT\cdot R}{2\pi\cdot R_{on}C_{load}}\arctan(2\pi\cdot f)\Big|_0^{\infty} = \frac{kT}{C_{load}} \tag{4.20}$$

4.2.2 PHYSICAL IMPLEMENTATION

When we apply the 1/f noise reduction principle to the operational amplifier in Chapter 4.1, two major cares should be taken into consideration. They are the periodic discontinuous source-to-drain current of the two identical MOS transistor in the 1/f noise reduction principle and the periodic impulse-like gate current of those. They occur at every half period of the applied full-swing clock (Φ1 and Φ2). The periodic discontinuous source-to-drain current of the two identical MOS transistor is an inherent phenomenon which attributes to two applied full swing complementary clocks. The periodic impulse-like gate current at every half period of the clocks is mainly explained by the charge injection effect in the MOS switches. The periodic impulse-like gate current will be detailed later and here the periodic discontinuous source-to-drain current is considered first. Although the two complementary clocks are assumed to have a 50 % duty cycle, in reality, all the clocks must have a certain rising/falling time and thus they can have no perfect 50 % duty cycle. As depicted in Figure 4.13, these full swing complementary clocks introduce a clock-like voltage VG11 & VG12 at the gate of the PMOS transistor T11 & T12 respectively. When the gate-voltage (e.g. VG11) of the transistor (e.g. T11) goes below VDD-$|V_{th}|$ (the times is denoted t_1 in Figure 4.13), the transistor (e.g. T11) turns on. Otherwise, at the same time, the other transistor (e.g. T12) still turns on and it gets into the off-state the time t_2 when VG12 goes higher than VDD-$|V_{th}|$. There must be a certain difference between these time t_1 and t_2, because the threshold voltage V_{th} of the two transistors T11 & T12 is not exactly the half of VDD-VG. This cause the discontinuity of the current (I11& I12) of the transistor T11 & T12 and thus the sum of the two current, which represents one "functional" transistor, shows also the discontinuous current at every half period of the clocks.

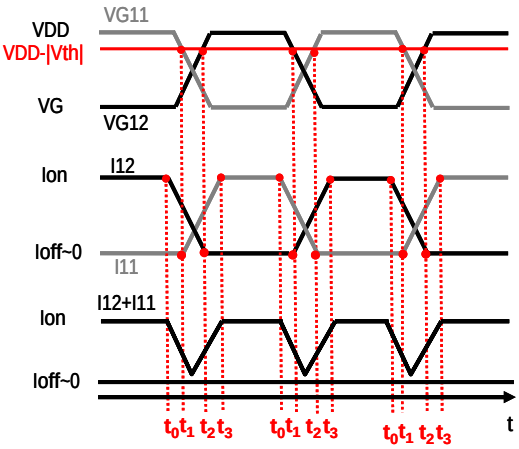


Figure 4.13 Gate voltage (VG11 & VG12), the source current (I11 & I12) of the transistors T11 and T12 versus time

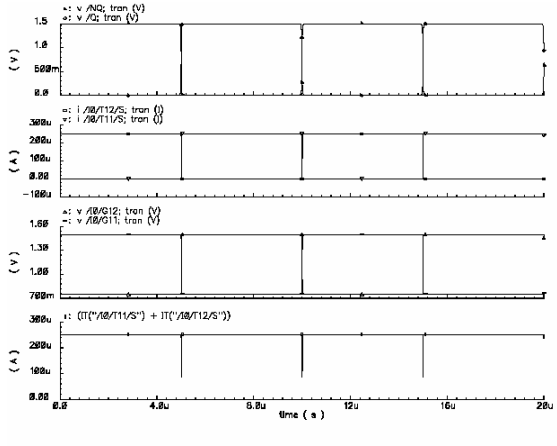


Figure 4.14 Simulated results of the principle MOSFET architecture, where the complementary clock of 100 KHz is applied.

Figure 4.14 shows the simulated currents - the source-to-drain current (i/I0/T11/S and i/I0/T12/S) of two identical input PMOS transistors (T11 &T12) and the sum current (i/I0/T11/S + i/I0/T12/S) of those, which corresponds to a functional transistor - in the 1/f noise reduction principle MOSFET architecture (Figure 4.9) when |VDS|=1.5 V and |VSG|=0.75 V. In Figure 4.14, the complementary clock (v/Q and v/NQ) of 100 KHz is applied and v/I0/G11 and v/I0/G12 are the gate-voltage of the transistors T11 and T12, respectively. Interestingly, the current of the transistor T11 and T12 swings between the on-current Ion ~ 251uA (the source-to-drain current of the transistor, e.g.T11, when it is on) and the off-current I_{off} ~ 0uA (the source-to-drain current of the transistor, e.g. T11, when it is off) but the sum current shows the minimum current I_{mim} (86.7uA) which is greater than I_{off} but smaller than I_{on}. Figure 4.15 shows the clock frequency dependency of the minimum source-to-drain current I_{min} of the 1/f noise reduction principle. As shown in Figure 4.15 the minimum source-to-drain current I_{min} increases as the clock frequency increased and thus the discontinuity in the sum current (i/I0/T11/G + i/I0/T12/G), which corresponds to the source-to-drain current of a functional transistor, decreases proportionally to the clock frequency. Thus in the application of the 1/f noise reduction principle to a continuous signal linear analog circuit, a switching clock with a higher frequency is better suited for the purpose. Next, the impulse-like gate current at every half period of the clocks is explained. When, e.g. an NMOS switch is on, that is, VDD is applied to the gate of an NMOS switch; a certain amount of charge is stored in the switch to form a conduction channel. By turning off the switch, e.g. by setting VSS to the gate of the NMOS switch, this charge is released from the channel and is distributed to the source and drain of the MOS transistor [11].

Figure 4.16 presents the conceptual considerations of the charge injection induced gate current in the switch. The charge injection effect can be cancelled in a CMOS transmission gate to some degree [10]. In the 1/f noise reduction principle, the switch S1 is a type of a CMOS transmission gate. The charge injection effect in the switch S1 is assumed to be ignored. Otherwise, in the case of the switch S2, this effect should be taken into account When the clock (e.g. Φ1) gets high, the PMOS switch S2 in SW1 turns off and connects VG to the gate of the PMOS transistor (e.g. T11). Thus the switch S2 releases the charge Q11 to the gate of the transistor T11 in the opposite direction of the arrow in Figure 4.16. Otherwise, at the same time, the other switch S2 in SW2 turns on and draws the charge Q12 (the same amount as the charge Q11) from the gate of the transistor T12 in the direction of the arrow. This induces the periodic Dirac impulse-like current at each gate of the transistors T11 & T12.

The periodic induced current at the gate of transistor T11 and T12 (i_{inj11} and i_{inj12}) can be mathematically represented as

$$\begin{aligned} i_{inj11}(t) &= \frac{1}{T_{clk}} \sum_{-\infty}^{\infty} \left[Q_{11} \cdot \delta(t - nT_{clk}) - Q_{11} \cdot \delta(t - nT_{clk} - \frac{T_{clk}}{2}) \right] \\ i_{inj12}(t) &= -\frac{1}{T_{clk}} \sum_{-\infty}^{\infty} \left[Q_{12} \cdot \delta(t - nT_{clk}) - Q_{12} \cdot \delta(t - nT_{clk} - \frac{T_{clk}}{2}) \right] \end{aligned} \tag{4.21}$$

In Equation 4.21, n is an integer number. When Q_{11} equals to the same amount as Q_{12}, the current i_G at the node G vanishes. Since the current i_G at the node G, in Figure 4.16, is given as

$$i_G(t) = i_{inj11}(t) + i_{inj12}(t) \tag{4.22}$$

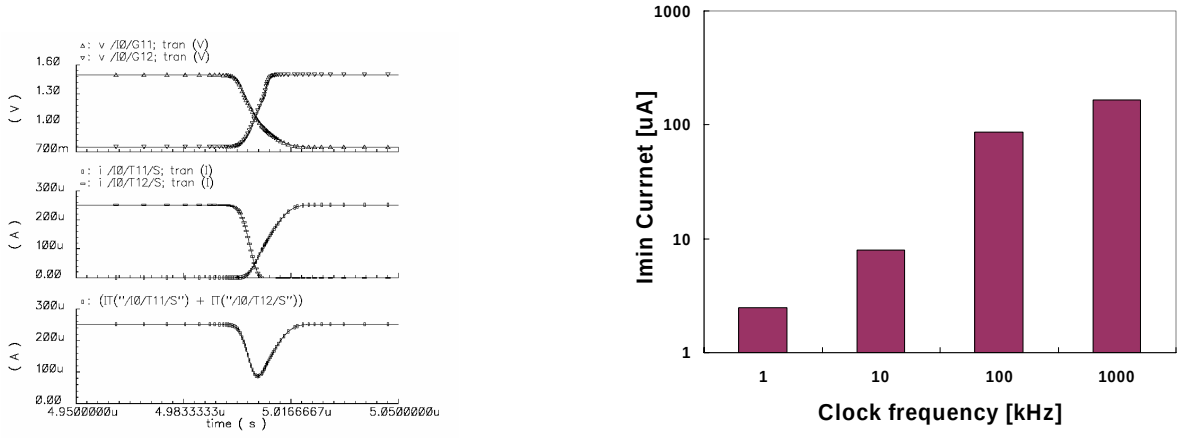


Figure 4.15: Left is the enlarged view of the Figure 4.14. Right is minimum source-to-drain current I_{min} versus clock frequency

Figure 4.17 shows the simulated results of Figure 4.16. Figure 4.18 shows the clock frequency dependency of the injected gate current I_{inj} of the 1/f noise reduction principle. Now, the operational amplifier, where the 1/f noise reduction principle is implemented, is discussed. Figure 4.18 shows the simulated currents of the transistors in the operational amplifier in the unity-gain configuration, when the two complementary clocks of 1 MHz are applied and no input signal is applied. The discontinuity, discussed in the above also appears in the source-to-drain current of the two input PMOS transistor (i/I14/T5/D and i/I14/T0/D).

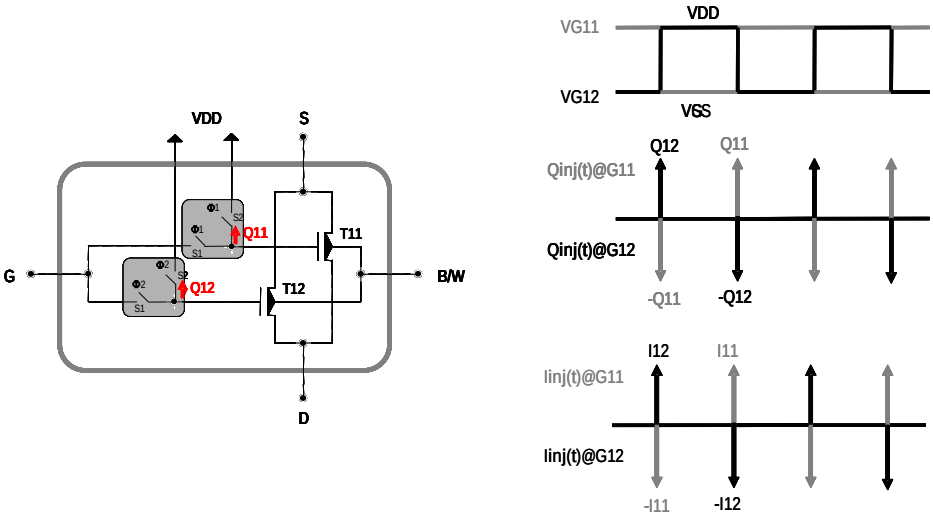


Figure 4.16 Dirac impulse-like gate current induced by the charge injection effect

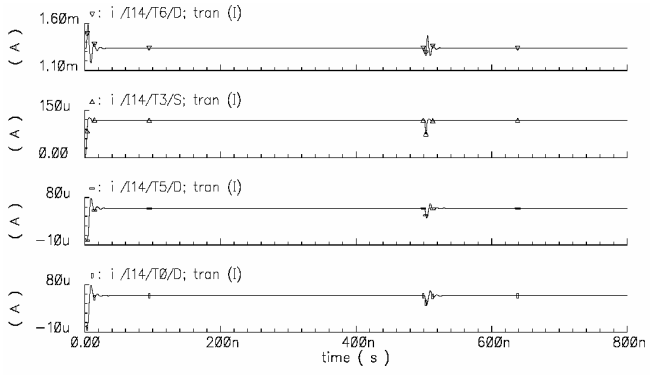


Figure 4.17 Simulated current of the transistors in the operational amplifier. i/I14/T5/D & i/I14/T0/D represent the two input transistors; i/I14/T3/S represents the tail-current source PMOS transistors. The other i/I14/T6/D is the current in the second stage.

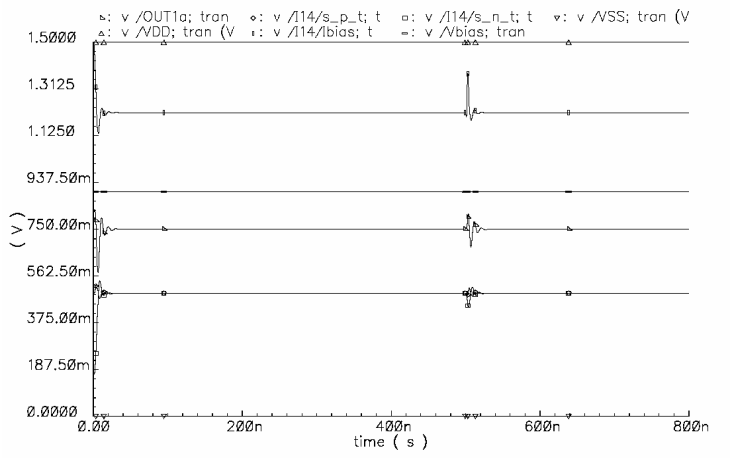


Figure 4.18 Simulated node voltages in the operational amplifier. The node names are denoted in Figure 3.11

This introduces further discontinuities in the current of the tail current source PMOS transistors (i/I14/T3/S) and as well as the second stage (i/I14/T6/D). The current discontinuity in each branch of the amplifier converts to the voltage "glitch." Figure 4.19 to 4.20 repeat the same simulated results, when a 100 mV input signal with a frequency of 100 kHz, is applied to an input of the operational amplifier in the unity-gain configuration.

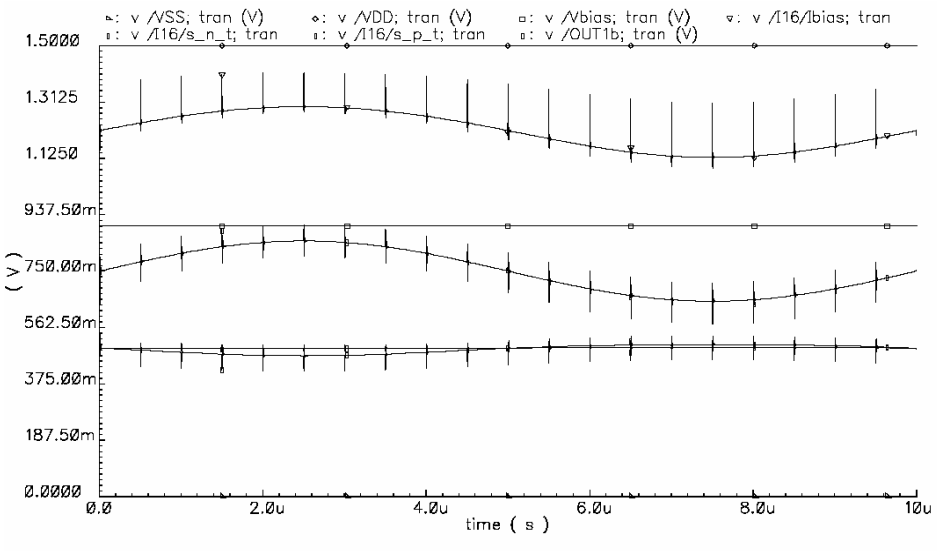


Figure 4.19: Simulated node voltage in the operational amplifier. The node names are denoted in Figure 3.11

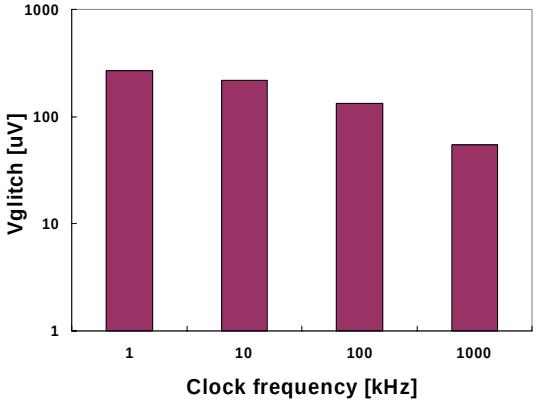


Figure 4.20 Glitch voltage versus the clock frequency

The glitches are also observed and they are expected to influence on the output voltage. The spectrums of the output voltage of the reference one from Chapter 4.1 and the proposed operational amplifier are compared in Figure 4.22. Apparently more harmonics of the output voltage with glitch (the proposed operational amplifier) are observed compared to those of the output voltage without glitch (the reference one). In general, the clock frequency should be greater than the input signal frequency. For example, in the sampled-and-hold systems, the sampling frequency should have at least two times signal bandwidth of interest in order to avoid the interference of the signal bandwidth. In the 1/f noise reduction principle, the clock frequency should be greater than the input signal frequency to minimize the voltage glitches. Figure 4.21 indicates the output voltage glitch decrease as the switching clock increases. The reason is the discontinuous current in each branch of the operational amplifier which decreases as the switching frequency increases. Thus a higher clock frequency is needed. But there is a limit for choosing an appropriate clock frequency: the higher clock frequency increase the switch noise as depicted in Equation 4.20. Thus, for low noise application, a special care should be taken.

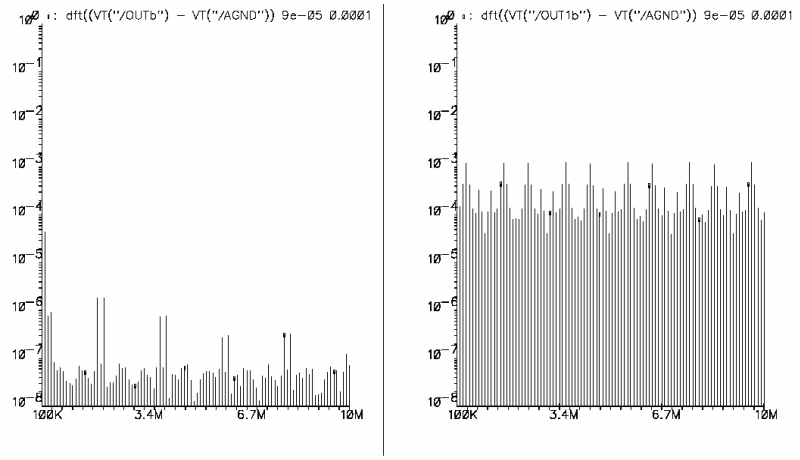


Figure 4.21 Left shows the Discrete Fourier Transformed output signal of the reference operational amplifier and right shows that of the proposed operational amplifier.

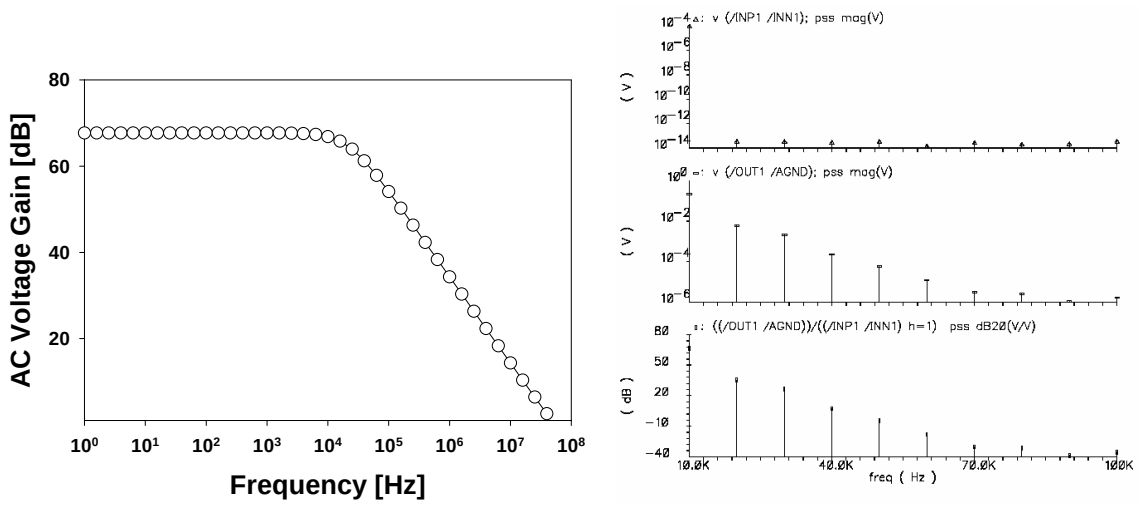


Figure 4.22 Left is the simulated open-loop small signal ac gain plot and right is the spectrum of input and output signal of 10kHz when the 100 kHz complementary clock signals Φ1 & Φ2 are applied.

The open-loop ac gain plot of the operational amplifier is shown in the left of Figure 4.22. Right of Figure 4.22 shows input & output signal spectrum, when the 100 kHz complementary clock signals Φ1 & Φ2 and input signal of 10 kHz are applied. When compared to the open loop gain plot of the reference one (Figure 4.7), no great degradation of DC gain is found in the proposed operational amplifier when the complementary clocks are applied. The proposed operational amplifier is implemented in a digital 0.12 μm 1.5V CMOS process. The layout is shown in Figure 4.23.

The additional area necessary for the transistors in the circuit to be replaced by the new circuit implementation is slightly more than twice the area of conventional transistor implementation. Since only the most noise sensitive transistors are replaced, the area increase is only 12.5% compared to a standard design. In addition, a variation of the proposed operational amplifier is designed as in Figure 4.24.

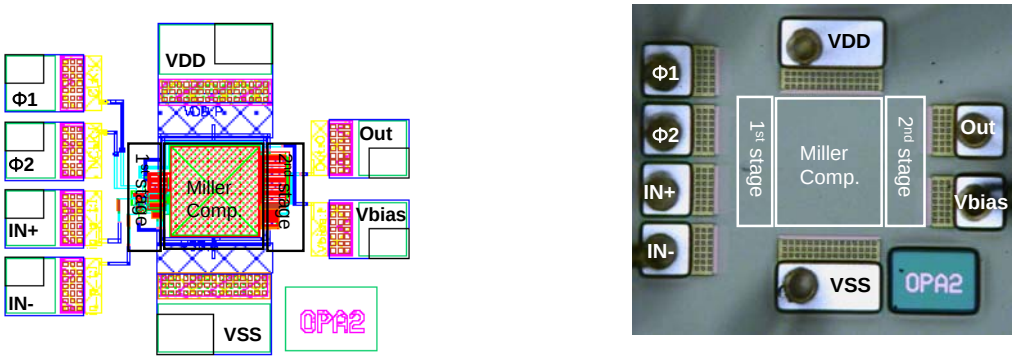


Figure 4.23 Layout (left) and chip-photo (right) of the proposed operational amplifier

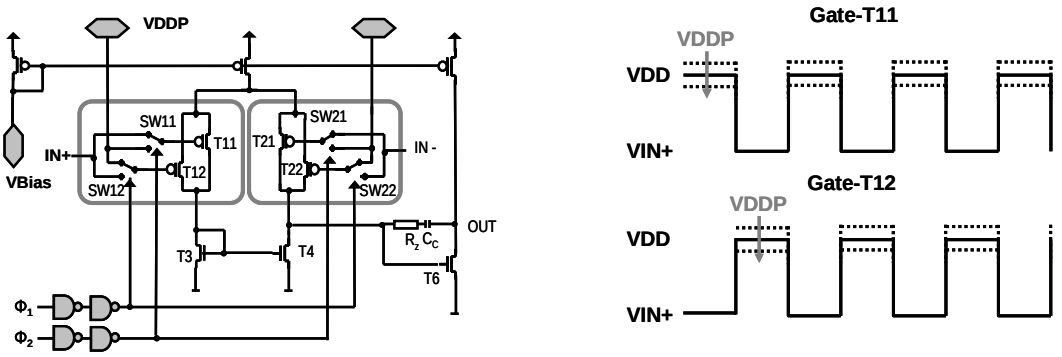


Figure 4.24 Left shows a variation of the proposed operational amplifier for varying the off-voltage (VDDP) for the input switched MOSFETs. Right illustrates the variation of the off-voltage given to the gate of an input transistor (e.g. T11) in the switched MOSFET architecture.

The operational amplifier in Figure 4.24 has an additional power supply VDDP for the input "switched" MOSFETs. In this configuration the off-voltage (VDDP) at the gate of a transistor (e.g. T11) in the switched MOSFET architecture can be varied without causing additional effect on the other transistors in the operational amplifier, as long as VDD is maintained. The layout and chip-photo are given in Figure 4.25.

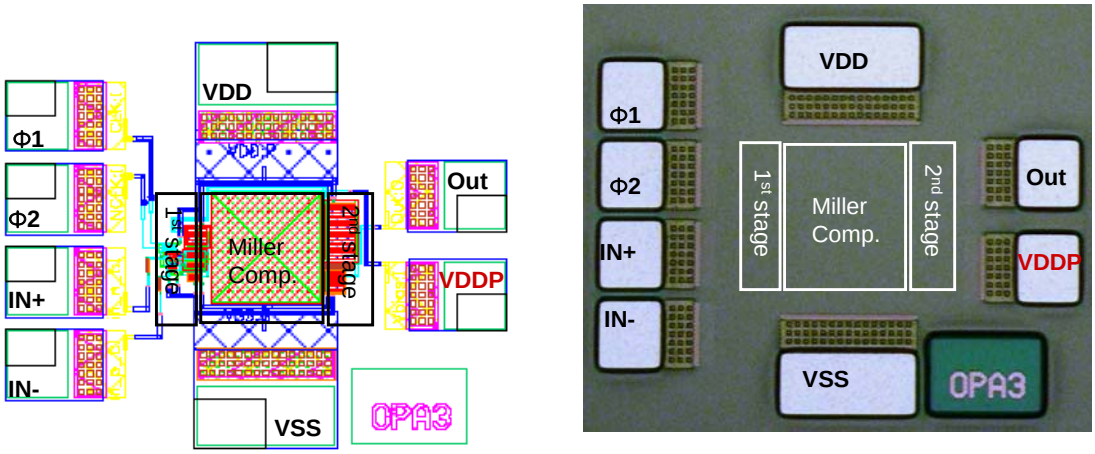


Figure 4.25 Layout (left) and chip-photo (right) of the proposed operational amplifier which has an additional power supply VDDP(Figure 4.28)

	Classic operational amplifier	Modified operational amplifier
Open loop Gain	68.3 dB	67.6 dB
Power Consumption@1.5V	1.4 mA	1.50 mA
Area	0.20mm x 0.21mm	0.24mm x 0.21mm

Table 4.2 Comparison of some data of the reference op-amp and the proposed new circuit implementation

4.3 REFERENCES FOR CHAPTER 4

[1] Ralf Brederlow, "Niederfrequentes Rauschen in Analogen CMOS-Schaltungen," Ph. D Dissertation, Technische Universität Berlin, 1999

[2] B. Razavi, "Design of Analog CMOS Integrated Circuits," New York, McGraw Hill, 2001

[3] Spice3f4 User Manual, ftp://ftp.pfnet.com/pub/spice3f4/ ,1998

[4] BSIM3v3 Manual, http://www-device.eecs.berkeley.edu/~bsim3/ ,1996

[5] A. P. van der Wel, E.A.M. Klumperink, S. L. J. Gierkink, R. F. Wassenaar, and H. Wallinga, "MOSFET 1/f noise measurement under switched bias conditions," IEEE Electron Device Letters., vol. 21,pp. 43 – 46, 2000

[6] I. Bloom and Y. Nemirovsky, "1/f Noise Reduction of Metal-Oxide-Semiconductor Transistors by cycling from inversion to accumulation," Applied Physics Letters, vol. 58, pp. 1664-1666, 1991.

[7] B. Dierickx and E. Simoen, "The Decrease of Random Telegraph Signal Noise in Metal-Oxide-Semiconductor Field-Effect Transistors when cycled from inversion to accumulation," Journal of Applied Physics, vol. 71, pp. 2028-2029, 1992.

[8] J. Koh, R. Thewes, D. Schmitt-Landsiedel and R. Brederlow "A Circuit Design based Approach for 1/f-noise Reduction in Linear analog CMOS IC's," Digest of Technical Paper VLSI Symposium on the Circuit, pp.222-225, 2004

[9] C.G. Linnenbank, W. Weber, U. Kollmer, B. Holzapfl, S. Sauter, U. Schaper, R. Brederlow, S. Crysian, S. Kessel, R. Heinrich, R. Hoefig and G. Knoblinger, A. Hesener and R. Thewes, "What do matching results of medium area MOSFETs reveal for large area device in typical analog application," Proceedings of the 28th European Solid-State Device Research Conference, pp.104-107, 1998

[10] K. Laker and W. Sansen, Design of Analog Integrated Circuits and Systems, Boston, McGraw-Hill, 1994

[11] G. Wagmann, E. Vittoz and R. Rahali, "Charge injection in analog MOS switches," IEEE Journal of Solid-state circuits, vol. 22, pp.1091-1097, 1987

CHAPTER 5

EXPERIMENTAL RESULTS

In Chapter 5, the 1/f noise reduction principle is experimentally demonstrated in a two stage CMOS miller operational amplifier. Compared to the reference operational amplifier in Chapter 4, a threefold reduction (5dB) at 10 Hz in the 1/f noise achieved for an operational amplifier designed in a standard 0.12 um, 1.5V CMOS technology. Subsequently the impact of the principle on the performance of linear analog CMOS IC's is investigated in terms of linearity, total harmonic distortion (THD) and power-supply rejection (PSR). Furthermore the thermal noise and the noise aliasing effects, which inherently arise from the proposed principle, on the noise performance of the operational amplifier are analysed.

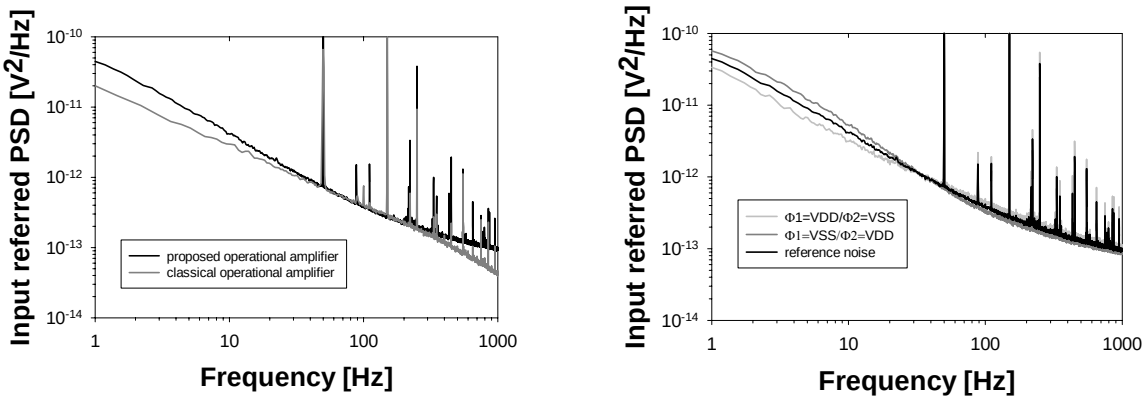


Figure 5.1 The left picture shows the "reference" input referred noise PSD of the proposed operational amplifier (Figure 3.12) and the measured one of the classical operational amplifier (Figure 3.10). Acquisition of the "reference" noise of the proposed operational amplifier is shown in the right of Figure 5.1

5.1 NOISE MEASUREMENTS

In this section, the 1/f noise reduction principle is experimentally demonstrated in the proposed operational amplifier architecture. Main noise experiments are made on the operational amplifier in Figure 3.12. In addition, the impact of the off-voltage of the principle is experimentally investigated.

5.1.1 REFERENCE NOISE

Left of Figure 5.1 plots the "reference" input referred noise power spectrum of the proposed operational amplifier (Figure 3.12) and that of the classical operational amplifier (Figure 3.10). The proposed operational amplifier exhibits the higher noise behavior than the classical one, because the proposed one has more active-noisy device (i.e., switches in the 1/f noise reduction principle in Figure 3.12) than the classical one. The "reference" noise of the proposed operational amplifier is taken from the average of the cases when static DC signals (i.e., Φ1 = VDD, Φ2 = VSS are applied and vice versa). This described in the right of Figure 5.1. Here a different noise behavior is observed in two cases, due to the internal mismatch in doping (V_{th}-fluctuations) and trap distribution (1/f-noise fluctuations) between the two input transistors T11 & T21 (T12 & T22) in Figure 3.12. In the measurements - and in the following measurements as well as - spectral peaks are observed due to the power-line (European standard 50Hz) related interference in the measurement set-up. This can be ignored for on-chip operational amplifier operation.

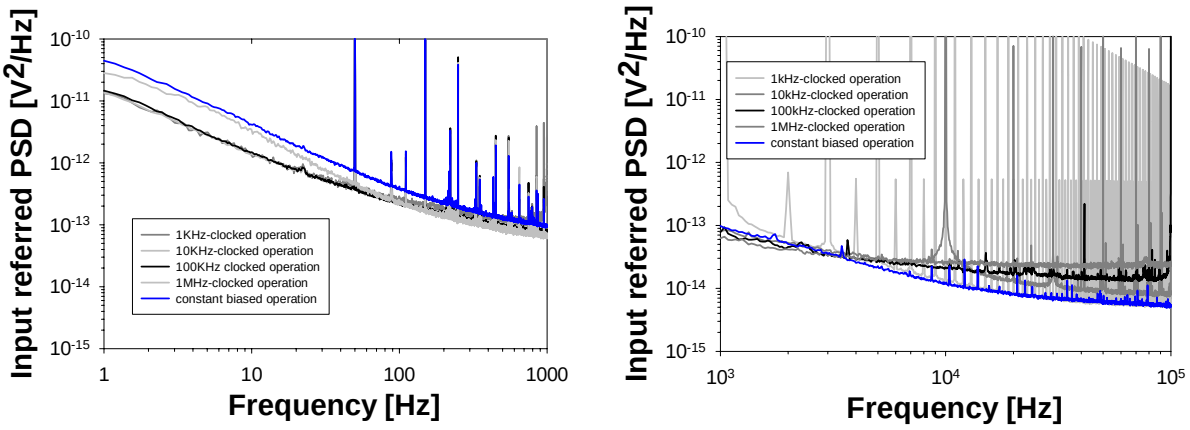


Figure 5.2 Input referred noise PSD of the proposed operational amplifier (Figure 3.12) under clocked bias condition and the constant bias condition. The different switching frequencies are indicated

5.1.2 NOISE REDUCTION

Figure 5.2 shows the input referred noise power spectral density of the proposed operational amplifier (Figure 3.12) in the frequency span of 1Hz to 10^3 Hz in the left and that of 10^3Hz to 10^5 Hz in the right[1)]. In the measurement the different clock frequencies are applied. The clock frequencies are indicated in the figures. In the low frequency region (e.g., 1 to 10^3 Hz), a distinct noise reduction is achieved. The noise reduction reaches to a factor of three (5 dB) at 1 Hz and 10 Hz when the clock frequency of 1 kHz to 100 kHz clock is applied (left of Figure 5.3). When 1MHz clocks are applied, the noise reduction (about 2dB @ 1Hz) is smaller for low frequencies. But, interestingly, the noise reduction reaches the same amount than other cases above 50Hz. In the high frequency region of 10^3 to 10^5 Hz, the peaks are observed at every integer times the clock frequency (remember the applied clocks are not less than 1kHz and thus the peaks in the left of Figure 5.2 are power-line related interferences). This is due to the noise aliasing effect, which inherently arises from the proposed principle (refer to Chapter 3.2.2 For the complementary switched MOFET architecture Equation 3.13 indicates that noise aliasing occurs at the odd harmonics of f_{clk}. However, noise aliasing also

[1)] Noise is measured in the frequency span of 1 to 10^3 Hz with higher accuracy than in between 10^3 and 10^5 Hz, since more precision in noise measurement is necessary in the lower frequency span of 1 to 10^3 Hz. The spectrum analyzer UP320 (Rohde & Schwarz™), which was used for the measurements, supports less measurement accuracy in the frequency region of 1 to 10^5 kHz. Hence the measured noise is separately plotted in Figure 5.2.

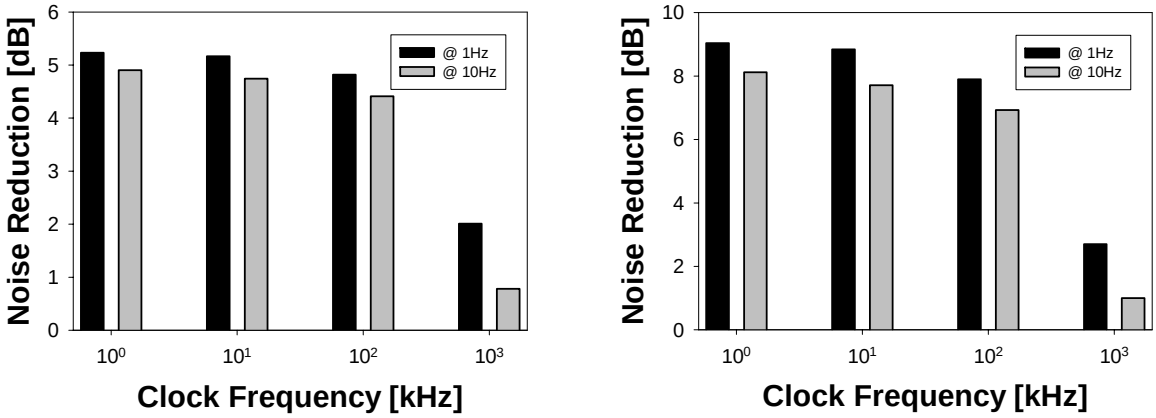


Figure 5.3 The left picture shows is the achieved 1/f noise reduction factor on dB-scale at low frequency region (@ 1Hz and 10Hz) in the proposed operational amplifier (Figure 3.12) and the right picture shows the calculated 1/f noise reduction in the input switched MOSFETs in the proposed operational amplifier.

occurs at the even harmonics of f_{clk} in the measurement for the proposed operational amplifier! The reason for this will be detailed in the following sub-chapter.

In addition to the noise aliasing effect, an increase of the noise plateau due to the thermal noise is observed when the clock frequency f_{clk} increases. In the reference noise spectrum[2)], a (white) noise plateau (ca.10^{-14} V^2/Hz @ 10^5Hz) appears starting at a few 10 kHz[3)]. This corner frequency gets smaller when the clock frequency f_{clk} goes higher. This is explained by a higher thermal noise component coming from the switch with increasing clock frequency f_{clk} (Equation 4.21). The effective noise reduction in the input switched MOSFET is depicted in right picture of Figure 5.3. In the operational amplifier in Figure 3.12, the input transistors T11 and T21 (T12 and T22) contribute 75 % to the total 1/f noise. Hence, the 1/f noise reduction of the complementary switched MOSFET architecture reaches to an about 8 dB @ 1Hz and 10Hz. Details on how to obtain the effective noise from the input switched MOSFET out of the operational amplifier noise measurements are illustrated in Appendix A.3. In a next step the noise reduction as a function of the noise-refresh potential VDDP is measured (see Fig. 4.28). The left picture of Figure 5.4 shows the input referred noise power spectrum of the operational amplifier (Figure 4.28) under the clocked bias condition with various frequencies

2) *"Reference" noise spectrum* is denoted as clocked bias operation in Figure 5.2

3) This frequency is called the noise corner frequency, where the white noise (e.g., thermal noise) gets predominant that the low-frequency noise (e.g., 1/f noise)

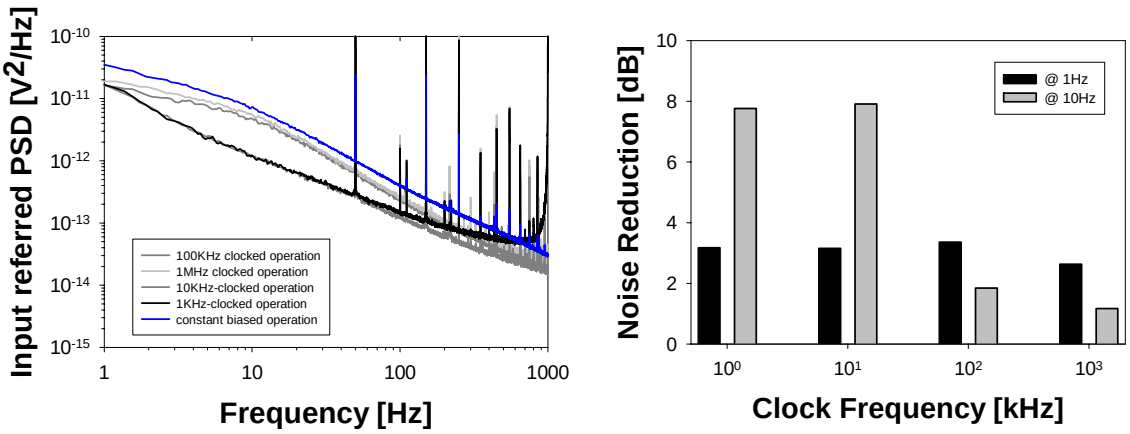


Figure 5.4 Left is the input referred noise PSD of the proposed operational amplifier (Figure 4.28) under clocked bias condition and the static bias condition. The switching frequencies are indicated Left is the achieved 1/f noise reduction factor on dB-scale at low frequency region (@10Hz).

compared to the static bias condition noise. The operational amplifier has a contribution from the input transistors of 90 % to the total 1/f noise.

The picture on the right side of Figure 5.4 depicts the achieved noise reduction of the operational amplifier. When compared to Figure 5.2, an enhancement of the noise reduction by a factor of a 3dB is achieved. This indicates that a proper “noise-care” circuit design (Equation 4.11) is a need for optimal exploitation of the 1/f noise reduction effect. Now the input referred noise spectrum of the operational amplifier is measured as a function of the VDDP. VDDP varies from 1.5V (VDD) to 1.65 V (VDD+10% of VDD). For those measurements the switching clock of 1 kHz is applied. The results are plotted in Figure 5.5. An enhancement of the noise reduction reaches to a factor of ca. 1.5 dB (the reduction factor increases from 7.9 dB to 9.4 dB as VDDP increases from 1.5 V to 1.55 V). But, no significant change is observed in the case that VDDP is greater than 1.55 V.

5.1.3 NOISE ALIASING

From the measured data in the previous sections, two drawbacks of the proposed operational amplifier architecture is discovered: (1) the fundamental noise aliases to “every” harmonics of the clock frequency f_{clk} and (2) the increase of the thermal noise level with increasing of the clock frequency. Those two effects and how to avoid or reduce them in practical analog circuit design is discussed here in more details. The noise aliasing inherently arises from the 1/f noise reduction principle, the complementary switched MOSFET architecture. According to Equation 3.14 it is apparent that the noise aliasing occurs at the odd harmonics in the proposed operational amplifier architecture. But, the aliasing is still observed at the even harmonics in this amplifier.

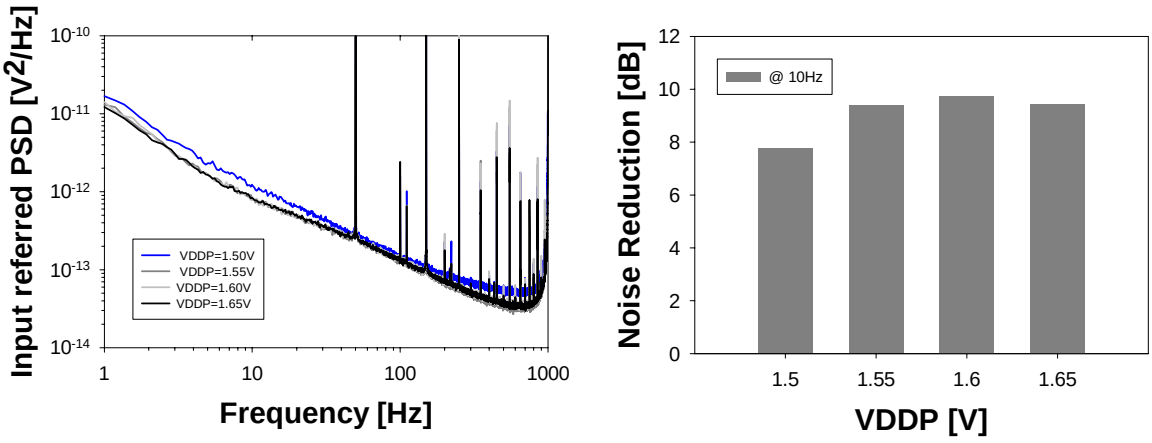


Figure 5.5 The left picture shows is the input referred noise PSD of the proposed operational amplifier (Figure 4.28) under clocked bias condition and the static bias condition. The switching frequencies are indicated. The right picture shows the achieved 1/f noise reduction factor on dB-scale at low frequency region (@10Hz).

This aliasing at the even harmonic originates from the fact that the replica of the signal transfer function shifts the extreme narrow-band signal (e.g., DC offset) into the even harmonics of f_{clk} [1]. This additional noise aliasing is explored in the following.

The output referred noise spectrum S^2_{vout} is expressed as

$$S^2_{vout} = S^2_{vin} \cdot \left|A_{vo}(f)\right|^2 = \sum_{i=1}^{n} S^2_{vg_i} \cdot \left|A_{vn_i}(f)\right|^2 \tag{5.1}$$

In Equation 5.1 $S_{vg_i}{}^2$ is the equivalent noise voltage of transistor T_i and A_{vni} is the gain from the noise source to the output (refer to Table 3.1). The contribution of input transistors in Equation 5.1 to the input referred noise spectrum S^2_{vin} and the output noise spectrum S^2_{vout} is most significant: the input transistors contribute 75% to the total 1/f noise of the operational amplifier as shown in Figure 3.12, and for the operational amplifier as shown in Fig. 4.26, the contribution of the input transistors reaches 90 %. Hence the noise contribution of the other transistors in Equation 5.1 can be ignored for simplification in a first approximation. Under this assumption, Equation 5.1 can be rewritten to

$$S^2_{vout} = S^2_{vin} \cdot \left|A_{vo}(f)\right|^2 \approx \sum_{i=1}^{2} S^2_{vg_i} \cdot \left|A_{vn_i}(f)\right|^2 \tag{5.2}$$

Hence, the input referred noise is simplified to

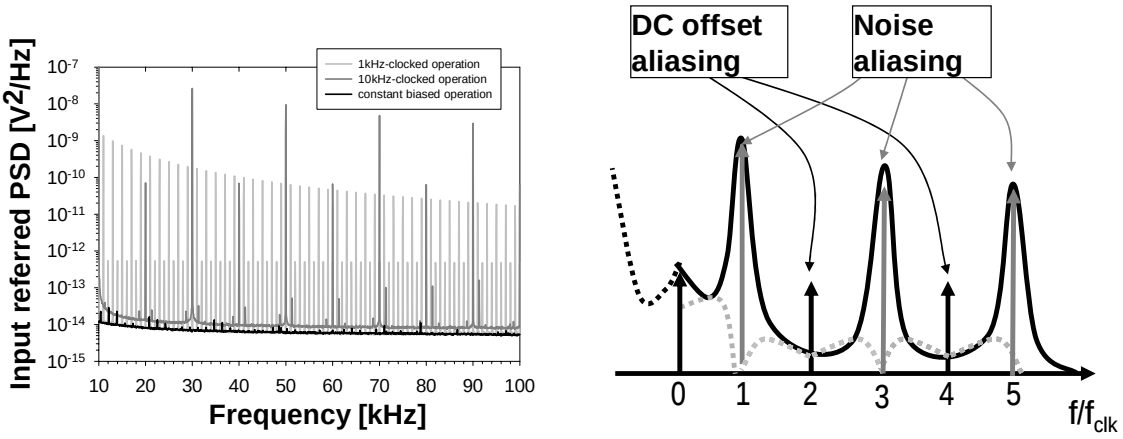


Figure 5.6 The left picture shows plots again the input referred noise PSD of the operational amplifier (Figure 3.12). In the right sided picture the graphical description for the noise aliasing occurring in the 1/f noise reduction operational amplifier architecture is shown

$$S_{vin}^2 \approx 2S_{vg1}^2 \tag{5.3}$$

Recalling Equation 3.13 and Equation 3.15, Equation 5.3 rewrites to

$$S_{vin}^2 \approx \left(S_{vgs11}^2(f) + \sum_{-\infty, n=odd}^{\infty} \left(\frac{2}{\pi n} \right)^2 \cdot S^2{}_{vgs11}(f - nf_{clk}) \right) \tag{5.4}$$

From Equation 5.4 it is apparent that the noise aliasing occurs at the odd harmonics of f_{clk}. Now, the aliasing at the even harmonics is mathematically described. When we denote X_{dc}(t) for the extreme narrow-band signal, X_{dc}(t) is represented in the frequency domain as

$$X_{dc}(f) = X_{dc}\delta(f) \tag{5.5}$$

When we use the mathematical expression of the signal transfer function *G(f)* from Equation 3.31, we obtain $X_{dc}(f)$ at the output, $X_{dc,out}(f)$ as

$$X_{dc,out}(f) = X_{dc}\delta(f) \cdot G(f) \tag{5.6}$$

where $G(f) = \sum_{-\infty, n=even}^{\infty} H_n(f - n \cdot f_{clk}) = G_{classical}(f) - \frac{4 \cdot t_p}{T_{clk}} \sum_{-\infty, n=even}^{\infty} G_{classical}(f - n \cdot f_{clk})$

Equation 5.6 expands to

$$X_{dc,out}(f) = X_{dc}\left(G_{classical}(0) - \frac{4 \cdot t_p}{T_{clk}} \sum_{-\infty, n=even}^{\infty} G_{classical}(-n \cdot f_{clk}) \right) \tag{5.7}$$

Since $G_{classical}(f)$ is the "even" function with regard to the frequency f, Equation 5.7 rewrites to

$$X_{dc,out}(f) = X_{dc}\left(G_{classical}(0) - \frac{4 \cdot t_p}{T_{clk}} \sum_{-\infty, n=even}^{\infty} G_{classical}(n \cdot f_{clk}) \right) \tag{5.8}$$

Now $X_{dc}(f)$ is obtained from Equation 5.8, when $X_{dc,out}(f)$ is referred to the input as

$$X_{dc}(f) = X_{dc}\left(\delta(0) - \frac{4 \cdot t_p}{T_{clk}} \sum_{-\infty, n=even}^{\infty} \delta(n \cdot f_{clk}) \right) \tag{5.9}$$

From Equation 5.9 $\left|X_{dc}(f)\right|^2$, which a spectrum analyzer reads, is given as

$$\left|X_{dc}(f)\right|^2 = X_{dc}{}^2 \left(\left(1 - \frac{4 \cdot t_p}{T_{clk}}\right)^2 \delta(0) + \frac{16 \cdot t_p{}^2}{T_{clk}{}^2} \sum_{-\infty, n=even, n\neq 0}^{\infty} \delta(n \cdot f_{clk}) \right) \tag{5.10}$$

Equation 5.9 and 5.10 indicates that the extreme narrow signal aliasing occurs at the even harmonics of the clock frequency $f_{clk.}$

Comparison between Equation 5.4 and 5.10 indicates that the amplitudes of the odd harmonics get smaller as the integer increases while that of the even harmonics remains constant. Taking a closer look at the input noise spectrum of the operational amplifier (Figure 5.6) makes conformation of the validity of the above two expression, Equation 5.4 and 5.10).. Left of Figure 5.6 exhibits two-decade difference between the even harmonics of the two cases when 1 kHz clock and 10 kHz is applied and a constant amplitude at the odd harmonics.

The increase of the thermal noise level is caused by the switching noise from the switches in the complementary MOSFET architecture. The thermal noise in the switch increase as the clock frequency f_{clk} increases. In Chapter 3.2.2, only 1/f noise and thermal noise are considered as the main noise sources of the complementary switched MOSFET architecture. However the switching noise of the switches should also be taken into consideration. This has been already expected in Chapter 4.2.2 and now becomes known from measured data, Figure 5.2. Under this consideration, Equation 5.4 should be represented as

$$S_{vin}^2 \approx \left(S_{vgs11}^2(f) + \sum_{-\infty, n=odd}^{\infty} \left(\frac{2}{\pi n}\right)^2 \cdot S^2{}_{vgs11}(f - nf_{clk}) \right) \tag{5.11}$$

$$\text{where } S_{vgs11}^2(f) \approx \frac{k_f I_{ds}}{C_{ox} L_{eff}{}^2 g_{m11}{}^2} \cdot \frac{1}{f} + \frac{8}{3} \frac{kT}{g_{m11}} + kTR_{ON,s1} \cdot f_{clk}$$

In order to reduce the thermal noise in the switch, a small on resistance should be chosen as already stated in Chapter 4.1.2. The small on resistance gives the lower switching noise due to the thermal noise in the switch but results in the clock mismatch parameter t_p due to the increase in the gate-area of the switch. This will increase the amplitude of the glitches in the 1/f noise principle, and thus a tight trade-off should be met in the design of the switch in the complementary switched MOSFET architecture.

5.2 ELECTRICAL PERFORMANCES

In this section, the impact of the 1/f noise principle on the performance of the two stage CMOS miller operational amplifier (OPA 2) is investigated in terms of signal transferring and linearity (e.g., total harmonic distortion (THD) and power-supply rejection (PSR))

5.2.1 SIGNAL RESPONSE

The left picture of Figure 5.7 shows the measured output signal of the OPA 2, with a 100 kHz complementary clock signals Φ1 and Φ2 are applied. In the measurement, a 5 mV input signal of 5 kHz is applied in a configuration as shown in the inset of the figure. Without low pass filtering (left plot of Figure 5.7), the glitches are observed, whose mechanism is already discussed in Chapter 4.2.2 (due to the complementary switched MOSFET architecture). These glitches can be strongly suppressed by an "easy" use of a simple "first order" passive low-pass filter at the operational amplifier output. This is shown on the right side of Figure 5.4 which plots the measured output signal of the operational amplifier with external filtering using a first order RC low pass filer with a cut-off frequency f_c of 8 kHz (the inset in right of Figure 5.7), This is one of the strength of the proposed 1/f noise principle, compared to the chopper stabilization technique for 1/f noise reduction (Chapter 1.2.1).

The chopper stabilization technique accompanies with a higher energetic glitch and thus, for the removal of it, the technique requires a higher order low pass filter: e.g., a 6^{th} order gm-C filter is used in [2]. A high order low pass filter enhances the system complexity and furthermore consumes more power and area. Whereas only a 1^{st} order filter is easily realized on the chip with an area and power efficiency.

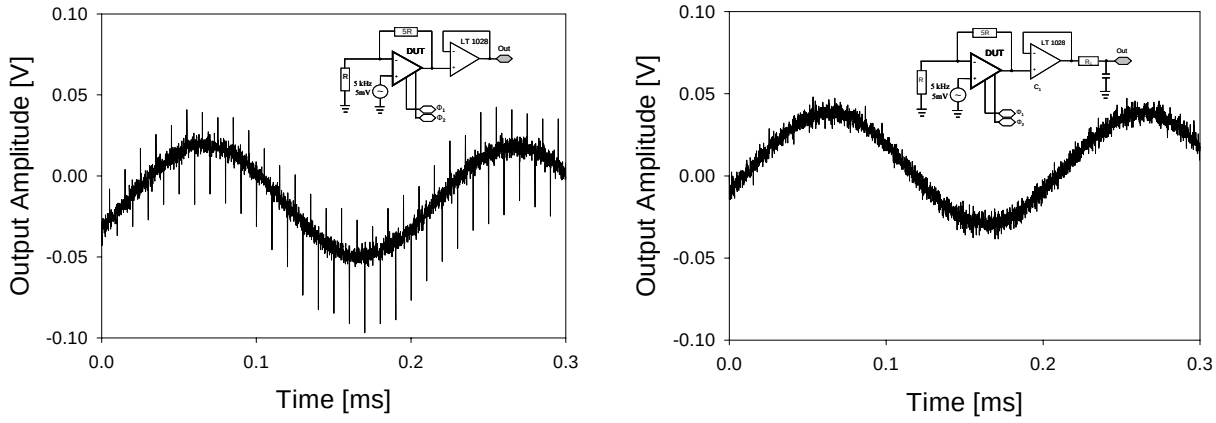


Figure 5.7 The left picture shows the measured output signal of the op-amp for 100 kHz complementary clock signals with 50 % duty cycle when no external low pass filtering is applied. The picture on the right side shows the measured output signal of the op-amp with a one-order low pass filter. Each inset depicts the measurement configuration.

5.2.2 GLITCH

Figure 5.8 (left) shows the measured glitch voltage of the operational amplifier for a 20 kHz complementary clocks are applied. In the measurement configuration depicts, no signal is applied. A glitch occurs at each half period of the applied clocks. It has a maximum height of 240mV (peak-to-peak) in the used measurement configuration (see right part of Figure 5.8). Division of 240mV by the gain of 6 of the measurement configuration results in a peak-to-peak glitch of 40mV referred t_p the input for a time window less than 2µs out of the 25µs clocking period. When we recall Figure 3.14 and Equation 3.32, this gives 1µs for t_p in Equation 3.32. Thus, the ratio t_p/T_{clk} equals about 8% in Equation 3.33 and only 8 % DC gain degradation is expected from Equation 3.33.

From these measurements it is obvious that the design of the switches and of an internal clock with high accuracy is advantageous for a good analog performance at higher frequencies. A low t_p/T_{clk} ratio is desirable in an optimized design of the switches: for example, a small size of the switches will result a low t_p but it can not avoid the increasing switching noise penalty.

5.2.3 DC GAIN AND GAIN BANDWIDTH (GBW)

Figure 5.9 (left) shows the measured signal gain of the operational amplifier when the complementary clock signals with 50 % duty cycle are applied. In the right of Figure 5.9, the measurement configuration is depicted. In the measurements, the input signal frequency is swept and the clock frequency is set to two times the input signal frequency.

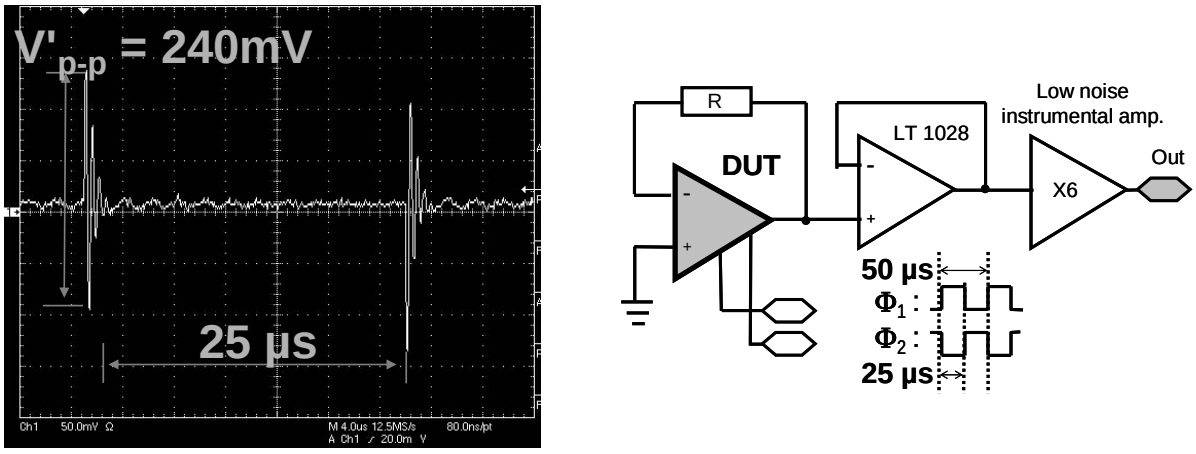


Figure 5.8 The left picture shows the measured output glitch of the op-amp for 20 kHz complementary clock signals with ca. 50 % duty cycle. The picture on the right side shows the corresponding measurement configuration.

In general, measuring of an open-loop gain versus frequency of an operational amplifier is not a simple matter, because of the inherent offset voltage. This offset voltage can easily force an operational amplifier to get into saturation and thus, in the result, prevents an operational amplifier from the no proper operation.

The measurement configuration, which is frequently called *unity-gain configuration* [3], is used here, to ensure the stable operation of the proposed operational amplifier architecture. Relevant parameters for the open-loop gain characteristic of the amplifier are easily obtained in this measurement configuration. An open-loop gain versus frequency measurement with a more accuracy is well described in [4]. In the followings are the details.

The signal transfer function $T(s)$ of the unity-gain configuration of an operational amplifier is given as

$$T(s) = \frac{1}{1+1/A(s)} \tag{5.12}$$

In Equation 5.12 $A(s)$ denotes a one-pole transfer function of an operational amplifier as depicted in Equation 3.13. Now Equation 5.12 rewrites to

$$T(s) = \frac{A_{DC}}{1+A_{DC}} \cdot \frac{1}{1+j\dfrac{\varpi}{\varpi_t}} \tag{5.13}$$

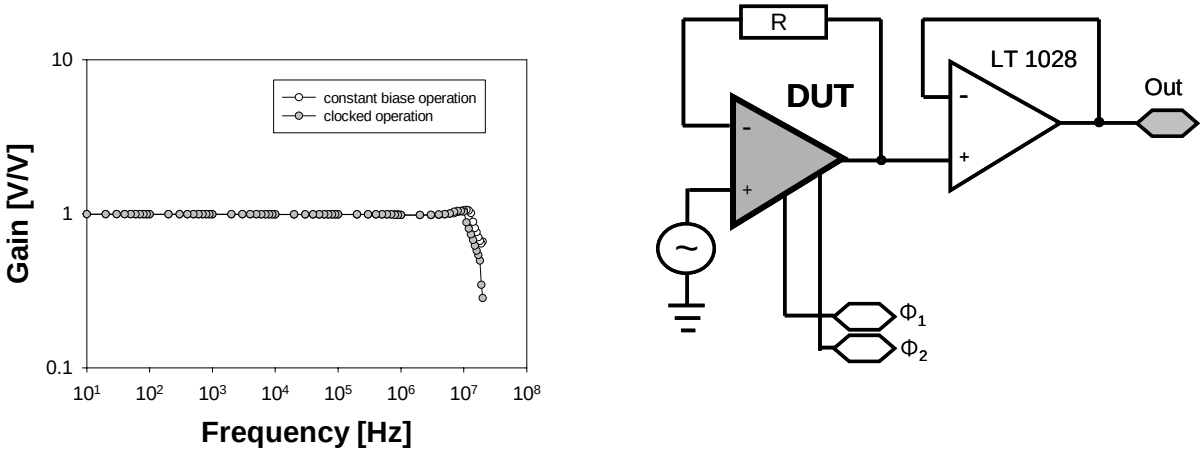


Figure 5.9 The left picture shows the measured signal gain vs. frequency of the operational amplifier when the complementary clock signals with 50 % duty cycle is applied according to the measurement configuration in right.

In Equation 5.13, A_{DC} denotes the DC gain and ϖ_t is the unity-gain bandwidth of an operational amplifier. Equation 5.13 depicts that the DC gain A_{DC} and the unity-gain bandwidth ϖ_t can be obtained from this measurement, and, in addition, that the one-pole transfer function $A(s)$ of an operational amplifier can be constructed from the measurement. From Figure 5.9 we get 14 MHz gain-bandwidth for the constant bias operated operational amplifier and 12 MHz for the clocked operated one: this indicates that the 1/f noise principle has no great influence on the unity-gain-bandwidth as predicted in Equation 3.35.

Figure 5.10 plots the "constructed" open loop small signal gain versus frequency of the operational amplifier. A degradation of ca. 12 % (about 1 dB) in the DC gain is observed in the operational amplifier (OPA 2) when the 1/f noise principle is applied, in comparison to the constant biased operation. This is reasonable: 8 % degradation in DC gain is expected from the glitch measurement in the previous section and the explanations in Chapter 3.2.2. The 1dB degradation in DC gain is not significant worse in real application of the operational amplifier, since almost all operational amplifiers operate in a feedback configuration which anyhow reduces DC gain.

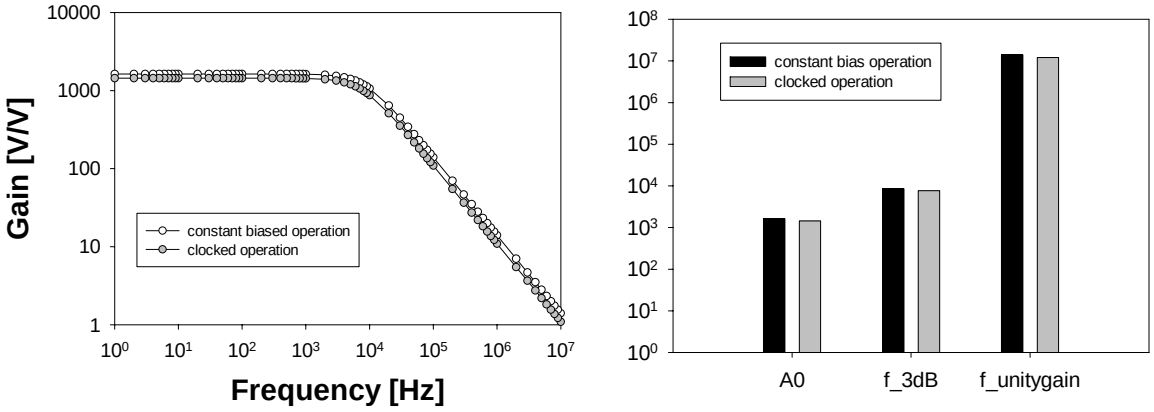


Figure 5.10 The left picture shows is the constructed small signal ac gain vs. frequency of the operational amplifier. The right picture shows the A0 (DC gain), f_3dB (3dB frequency) and f_unitygain (unity gain bandwidth) from the left of Figure 5.8.

5.2.4 TOTAL HARMONIC DISTORTION (THD)

In the left part of Figure 5.11, the total harmonic distortion (THD) for the two cases (constant bias operation and clocked operation of the proposed operational amplifier OPA 2) is plotted versus the applied input signal frequency. As in the DC gain and GBW measurement, the input signal frequency is swept (in this case, from 100 Hz to 100 kHz) and correspondingly the clock frequency is set to ten times the input signal frequency. The measurement configuration in the right of Figure 5.11 contains an output driver (LT 1028™). The output driver shows the THD below 0.0001 % in the closed loop gain of one [5]. Hence the THD of the output driver is ignored. In the constant biased operation case, a THD below 0.35 % is found. In the clocked operation (the input signal amplitude of $1mV_{peak\text{-}to\text{-}peak}$ is applied), a THD is smaller than that of the constant biased operation up to the input signal frequency of 10 kHz. Above 10 kHz, the THD in the clocked operation increases to 1.8 %.

The right part of Figure 5.11 shows the THD of the clocked operation case versus the applied switching clock frequency. In the measurement, the input signal frequency is set to 10 kHz and the switching clock is varied from one time to ten times the input signal frequency. The clock frequency which is far away from the input signal frequency results better THD in the proposed operational amplifier. This is why the clock frequency is set to ten times the input signal frequency in the above measurement.

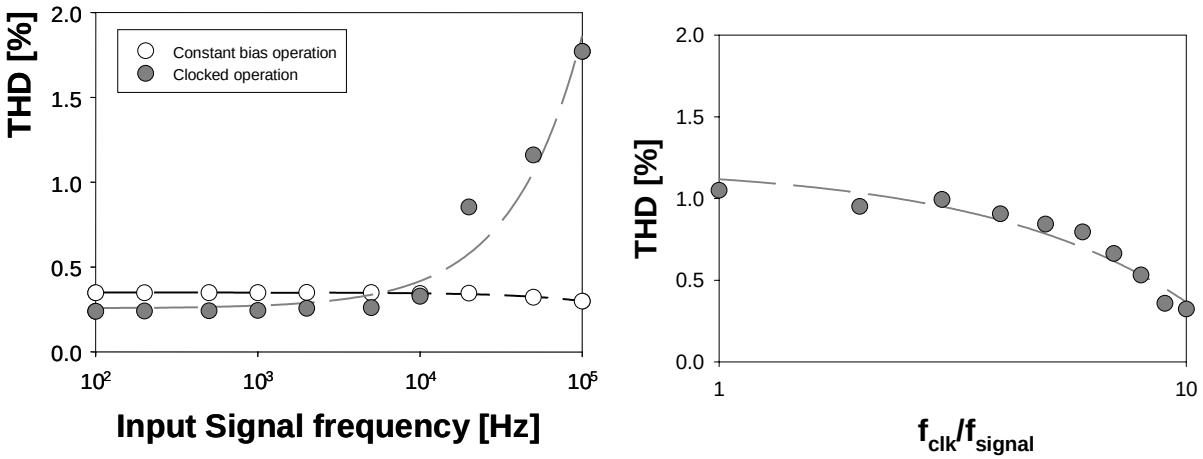


Figure 5.11 The left picture shows THD for the constant bias operation and the clocked operation of the proposed operational amplifier. The right picture shows the THD of the clocked operation case versus the applied switching clock frequency ($10*f_{signal}$), where the input signal frequency f_{signal} of 10 kHz is applied.

In the left part of Figure 5.12, the THD for the two cases (constant bias operation and clocked operation of the proposed operational amplifier) is plotted versus the applied peak-to-peak input signal amplitude. A signal frequency of 10 kHz and a clock frequency of 100 kHz are applied. Up to 500 mV_{pp}, the THD lower than 0.5 % is maintained for both of the cases. No significant difference is found between the cases.

From the results, it is proved that the 1/f noise reduction principle does not impose a significant worseness on the linearity of an operational amplifier.

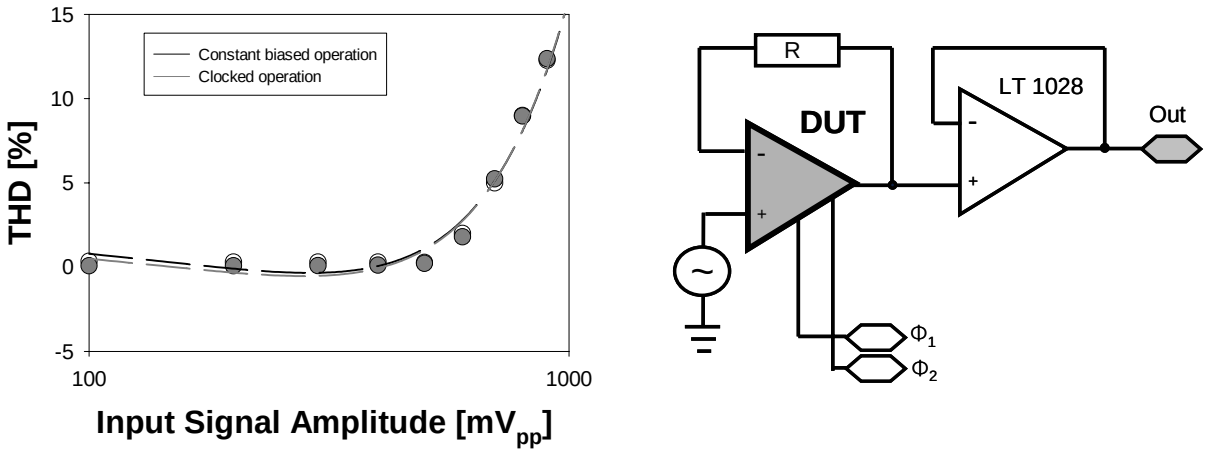


Figure 5.12 The left picture shows the THD for the constant bias operation and the clocked operation of the proposed operational amplifier. The right picture shows the corresponding measurement configuration.

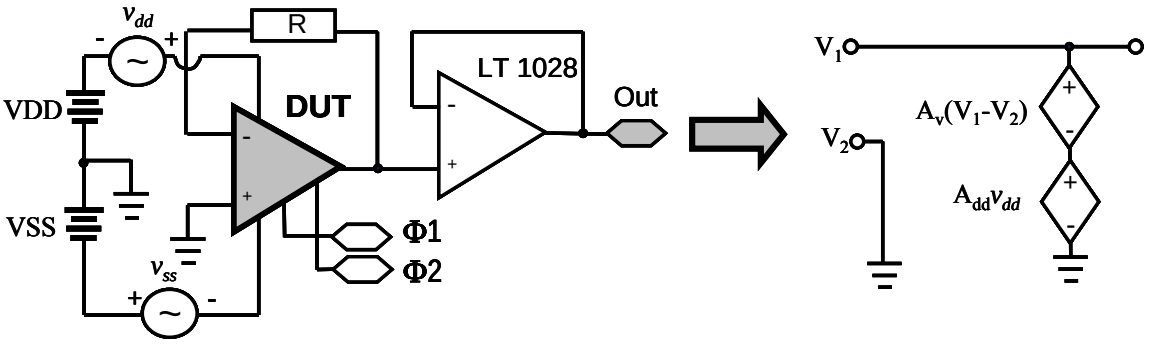


Figure 5.13 Method for the calculation of PSRR's in the unity-gain configuration. A small sinusoidal voltage is inserted in series with VDD (VSS) to measure PSRR+ (PSRR-).

5.2.5 POWER SUPPLY REJECTION RATIO (PSRR)

The Power Supply Rejection Ratio (PSRR) is defined as the ratio of the differential gain A_v of an operational amplifier to the gain from a voltage ripple in the power-supply referred to the output when the differential input is set to zero (e.g., A_{dd} for a V_{dd} ripple and A_{ss} for V_{ss} ripple). The positive power-supply rejection ratio PSRR+ and the negative power-supply rejection ratio PSRR- can be defined as

$$PSRR+ = \frac{A_v(v_{dd}=0)}{A_{dd}(v_{in}=0)} \qquad \text{and} \qquad PSRR- = \frac{A_v(v_{ss}=0)}{A_{ss}(v_{in}=0)} \tag{5.14}$$

The PSRR can be directly measured in a unity-gain configuration of the operational amplifier as shown in Figure 5.13 [6].Calculated from the equivalent circuit of this configuration PSRR+ is given as:

$$v_{out} = \frac{A_{dd}}{1+A_v}v_{dd} \cong \frac{A_{dd}}{A_v}v_{dd} = \frac{1}{PSSR+}v_{dd} \tag{5.15}$$

PSSR- is obtained a similar manner.

Figure 5.14 shows the PSRR- (left) and the PSRR+ (right) of the proposed operational amplifier under the constant bias and the clocked operation. In the measurements, the input signal frequency is swept- in this case, from 10 Hz to 100 kHz - while the clock frequency is set to ten times the input signal frequency for the clocked operation condition.

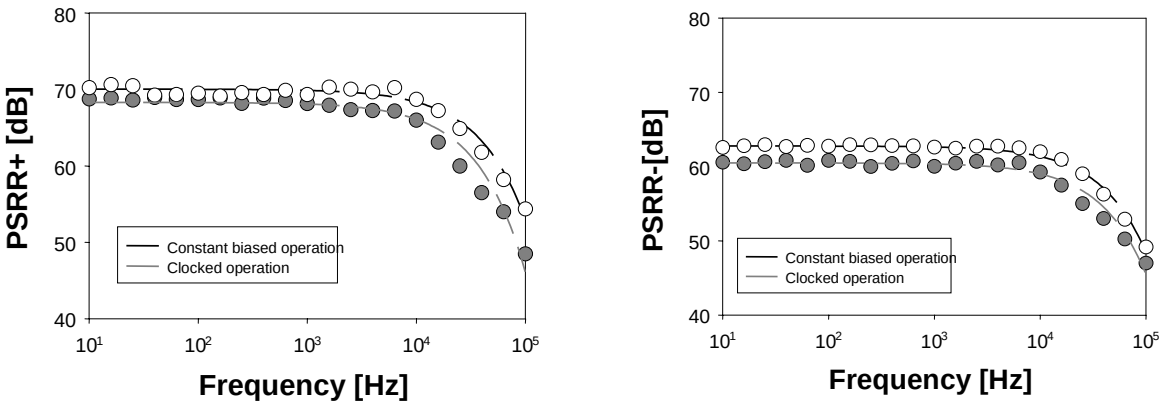


Figure 5.14 Left plots the THD for the constant bias operation and the clocked operation of the proposed operational amplifier. Right shows the corresponding measurement configuration.

A comparison between PSRR+ and PSRR, in both operation conditions, depicts a better PSSR is achieved for the positive power supply rejection ratio, namely the DC gain of PSRR+ is greater than that of PSRR The reason is because the DC gain of PSRR- is smaller by the amount of the second-stage gain. PSRR between constant biased operation and clocked one depicts that degradation of about 2dB is found in both of PSRR+ and PSRR- of the clocked operation case. This is due to the degradation of the DC gain A_v which originates from the 1/f noise reduction principle. The degradation of 2 dB is neglect small. From these measurements it is obvious that the design of the switches and of an internal clock with high accuracy is advantageous for a good analog performance at higher frequencies. The improvements of these values should be made for carefully optimized design of the switches

5.3 REFERENCES FOR CHAPTER 5

[1] Christian Ivo Menolfi, Low Noise CMOS Chopper Instrumentation Amplifiers for Thermoelectric Micro sensor, Ph. D thesis, ETH Zurich, Zurich, 2000

[2] C. Menolfi, and Q. Huang, "A chopper modulated instrumentation amplifier with first order low-pass filter and delayed modulation scheme," Proceedings of the 29th European Solid-State Circuit Conference, pp.54-57, 1999

[3] K. Laker and W. Sansen, Design of Analog Integrated Circuits and Systems, Boston, McGraw-Hill, 1994

[4] W. M. Sansen, M. Steyart, and P. J. Vandeloo, "Measurement of operational amplifier characteristics in the frequency domain," IEEE Transaction on Instruments and Measurements, vol. 34, No. 1, pp. 59-64, 1985

[5] Linear Technology Inc., Application Note, LT 1028, Ultra low Noise Precision High Speed Op Amps, 1995

[6] P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, 2nd edition, New York, Oxford press, 2002

CHAPTER 6
SUMMARY

In this thesis a novel principle for the 1/f noise reduction technique in linear analog CMOS IC's is demonstrated, which is suitable for a continuous signal processing operation. The principle makes use of a known device physics-based effect: a periodical on-off switching of a MOSFET between strong inversion and accumulation leads to an anomalous reduction of the intrinsic 1/f noise of those devices. The mathematical modeling, the physical implementation and the experimental demonstration of the principle, all are discussed in this thesis. In a first step, we have proposed a principle for the 1/f noise reduction in linear analog CMOS IC's using the "complementary switched MOSFET architecture." Making a use of the 1/f noise reduction from the effect that the 1/f noise of a MOSEFT under non-equilibrium reduces the total noise under the complimentary switched MOSFET architecture is smaller compared to a single device solution. The noise behavior of the principle has been mathematically described using a modulation theory. The description also gives an explanation for the fact that the principle accompanies with the alias of the fundamental noise at odd harmonics of the clock frequency.

Next, as an example application for the principle, we have presented an operational amplifier architecture which includes the principle. The architecture is modified from a two-stage CMOS miller operational amplifier. In the application of the principle, an area saving design approach has been presented: replacing only the main noise contributing transistors (e.g., the input transistors) with the complementary switched MOSFET instead of all transistors of the operational amplifier. In this way, a 1/f noise-reduction without a significant increasing area has been obtained. The signal propagation in the proposed operational amplifier

architecture has been mathematically modeled and studied. Several instinct features have been identified from this mathematical description: the replica of the original signal exits at every even harmonics of the clock frequency, the replicas are out of phase of the original signal and the amplitude of replicas is less than that of original signal in proportion to the ratio of the clock mismatch parameter t_p and the clock period T_{clk}. It has also been identified that the clock frequency should not be less than the signal bandwidth of the operational amplifier (or of interests) in order to avoid the signal or any kind of noise to alias into the signal-band. It has also been shown that the clock frequency can be arbitrary chosen, when the clock mismatch parameter t_p is minimized and thus the replica gets deeply suppressed. This implies that an optimization of the clock mismatch parameter t_p is a critical factor in the application of the 1/f noise reduction principle to any linear analog IC.

Implementation issues of the proposed operational amplifier architecture (OPA 2) have been discussed. For example, the sizing of the switches in the complementary switched MOSFET architecture has been discussed for the optimization of the switching noise and the clock mismatch parameter t_p: a small on-resistance lowers the switching noise but results in a clock mismatch parameter increase. Thus it has been shown that a trade-off has to be made in the design of the switches. In addition, it has been discussed that a matched inverter pair should be used for the complementary clocks close to the switches. A matched inverter enhances the slew rate of the clock and thus results in the steeper clock and finally optimizes the clock mismatch parameter t_p.

The principle has been experimentally demonstrated for two types of the proposed operational amplifier architecture (OPA 2 and OPA 3). OPA 2 and OPA 3 are based on the same architecture and are physically implemented in a standard 0.12 µm, 1.5 V digital CMOS technology. The main difference is an extra highest potential VDDP in the complementary input switched MOSFET architecture of OPA 3: the off-voltage of the complementary input switched MOSFET can be varied while it is fixed to VDD in OPA 2. The principle has experimentally demonstrated its superiority compared to conventional 1/f noise reduction methods. For example, OPA 2 features a 1/f noise reduction by a factor of three (5dB) at 1 Hz and 10 Hz in the input referred noise power spectrum when the 100 kHz complementary switching clocks are applied. In OPA 2, the input transistors contribute 75 % to the total 1/f noise. Hence, the 1/f noise reduction of the input transistors is ca. 8dB. A twofold area increase of a transistor only leads to a factor of two in reduction of its 1/f noise, the proposed circuit implementations is more area-efficient. Moreover, it has the additional benefit of more freedom in choosing device channel length. The enhancement of noise reduction using the "noise-care" circuit design and the refresh potential VDDP has been experimentally demonstrated in OPA 3. In OPA 3, where the input transistors contribute 90 % to the total 1/f noise, a 3dB higher noise reduction is archived at 1 Hz and 10 Hz compared to OPA 2. Here, the reduction factor can be enhanced when the noise pre-charge potential VDDP has a higher value than VDD: we got a further 1.5 dB increase in the 1/f noise reduction when increasing the value of VDDP from 1.5 V to 1.55 V. Apart from the remarkable noise reduction, as a drawback, it has been observed that the 1/f noise reduction principle accompanies with noise

aliasing due to the inherent switching phenomena in the complementary switched MOSFET architecture. The proposed operational amplifier architecture exhibits the aliasing at “every” harmonics of the clock. The presented noise behavior description demonstrates a good agreement when describing the odd harmonic aliasing but it does not explain the even harmonic aliasing. This has been explained by making use of the mathematical description for the signal transfer of the proposed operational amplifier architecture: the transfer function shifts the extreme narrow band signal (e.g. DC offset) into the even harmonics. A noise measurement in a wide-frequency-span for OPA 2 has shown good agreement with this explanation. Another shortcoming - the increase in the noise plateau due to the higher thermal noise component from the switch with increasing clock frequency – has been apparent in the wide-frequency-span noise measurements.

It has experimentally demonstrated that the 1/f noise reduction principle has a minor impact on the electrical performance of the proposed operational amplifier architecture, when compared to a similar but constant biased operational amplifier. The operational amplifier OPA 2 exhibits a degradation of 1dB in both of the open-loop DC gain and the unity-gain bandwidth. These degradations are negligible small especially since almost all operational amplifiers operate in a feedback configuration which anyhow reduces the DC gain. No significant degradation of the linearity has been observed in the proposed operational amplifier. The degradation of the power supply rejection (PSRR) has been measured to be 2dB. Furthermore, no significant difference in the total harmonic distortion (THD) was observed. Finally, good agreement between the derived mathematical description for the signal transfer function and the experimental results (e.g. open-loop DC gain) has been shown.

Glitches inherently arise from the complementary switched MOSFET architecture. They have been explained by the simulation results or the switching of the clocked transistors. The glitches can easily be suppressed using a simple first-order passive low-pass-filter. This is showing one of the strengths of the principle: when compared to the industry-standard chopper stabilization technique for the 1/f noise reduction: here higher energetic glitches arise which has to be suppressed by a higher order low pass filter. Furthermore, both principles may be used simultaneously for further low frequency noise reduction. Compared to the technique of correlated double sampling, the same increase in the white noise plateau is observed. This technique finds its main application in a discrete signal processing system like sampled-data or sample and hold circuits, so that the use of this technique to a continuous signal processing system is reluctant.

The presented principle is a novel circuit design-based approach for the 1/f noise reduction in a linear analog CMOS IC using a device-physics based effect, which recently regains an attention from the analog/RF circuit designers. This thesis is the first to present a MOSFET architecture which makes this kind of 1/f noise reduction exploitable for linear analog CMOS ICs and to demonstrate its abilities and limits for linear analog CMOS ICs. In addition, we have given guidelines for successfully applying the principle to a linear analog CMOS IC. The new implementation can be combined with low frequency noise reduction techniques like Correlated-Double-Sampling or Chopper-Stabilization to achieve additional low frequency

noise reduction. A complete application of the principle to a linear analog IC requires an integration with an on-chip clock generator (which should be available in any system-on-chip type design together with digital circuitry) for well-matched complementary clocks and with an on-chip low-pass-filter (e.g., g_m-c filter) for the suppression of the glitches due to the principle. This integration and related studies are not accomplished in the frame of this thesis. Those works are remained as future works.

Den 01.12.05 / München, Seoul

Jeongwook Koh

LIST OF FIGURES

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„For the Father loves the Son and shows him all he does. Yes, to amazement he will show him even greater things than these.“ John 5:13

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오늘도 못난 아들을 밤 새워 눈물로 기도하시는

사랑하는 나의 어머니 방위자집사님께

이 논문을 바칩니다.

December 2005 in München / Seoul

Jeongwook Koh

Ps. Special thanks for reading this humble Dissertation.

PUBLICATIONS

[1] R. Brederlow, **J. Koh** and R. Thewes, "LF noise properties of a 0.12 um CMOS technology," 3rd workshop for analog circuits, Technische Universität München, March 2002

[2] **J. Koh**, D. Schmitt-Landsiedel, R. Thewes, and R. Brederlow "A Circuit design-based approach for a 1/f noise reduction in a linear analog CMOS IC's," Digest of Technical Papers, VLSI Symposium on Circuits, Hawaii, June 2004

[3] **J. Koh**, D. Schmitt-Landsiedel, R. Thewes, and R. Brederlow "A 1/f noise reduction circuit technique for a linear analog CMOS IC's," 6th workshop for analog circuits, Technische Universität München, March 2005

[4] G. I. Wirth, **J. Koh**, R. da Silva, R. Thewes, and R. Brederlow, "Modeling of statistical LF-Noise of a deep submicron MOSFETs," IEEE Transaction on Electron Devices, Vol.7, 2005

[5] R. Brederlow, **J. Koh**, and R. Thewes, "A physics-based modeling of LF noise under large signal excitation," Proceedings of European Solid State Device Research Conference, Grenoble, September, 2005

[6] R. Brederlow, J. Koh, G. I. Wirth, R. da Silva, M. Tiebout, and R. Thewes, "Low Frequency Noise Considerations for CMOS Analog Circuit Design," Conference Proceedings American Institute of Physics, Vol.780, 2005, pp. 703-708

[7] **J. Koh**, D. Schmitt-Landsiedel, R. Thewes, and R. Brederlow "A complementary Switched MOSFET Architecture for a 1/f Noise Reduction in a Linear Analog CMOS IC's," IEEE Journal of Solid-State Circuit 2006, submitted.

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Koh Jeongwook was born in Seoul, Korea in 1975. He has begun a university-study at Sogang University, Seoul, Korea in 1993 and got earned B. Sc. and M. Sc. in Electronic Engineering from Sogang Univeristy in 1998 and 2001. During the study, he had a chance to work for Siemens AG, Munich, Germnay in 1999 as an intern (Praktikant) and completed the master thesis at power device division, Infineon Technologies AG in 2000 (Diplomand). After finished master study. in 2001, he joined a cooperative Dr.-Ing (Ph. D) program between Corporate Reserach der Infineon Technologies AG (Dr. Roland Thewes' Group CPR FEC) and Technische Universität München (Prof. Dr. Doris Schmitt-Landsiedel, Lehrstuhl für Technische Elektroniks), all in Munich, Germany. In 2004, he joined Samsung Advanced Institute of Technology, Samsung Electronics Co., Ltd. in Kiehung, Korea for a military exemption. In 2005 he got a Dr.-Ing. from Technische Universität München. He is expected to complete his military service June 2007.

CHAPTER A
APPENDIX

Several mathematical expressions used in a full context of the thesis are detailed analyzed in this Chapter . This Chapter will help the reader to have a solid understanding of the context.

A.1 PERIODIC FUNCTION $f(t,t_P)$

A Periodic rectangular function which varies between 0 and 1, with an arbitrary duty cycle D, defined as t_p/T, has a mathematical description as follows [1]:

$$f(t,t_p)=\sum_{-\infty}^{\infty}\frac{1}{k\cdot\pi}\sin(k\frac{\pi}{T_0}t_p)\exp(jk\omega_0(t-\frac{t_p}{2})) \tag{A.1}$$

A real form of Equation A.1, which is more practical in many applications, is given in Equation A.2.

$$f(t,t_p)=\sum_{k=1}^{\infty}\left(\frac{1}{k\cdot\pi}\left(\sin(k\omega_0(t_p-t))+\sin(k\omega_0 t)\right)\right)+1\cdot D \tag{A.2}$$

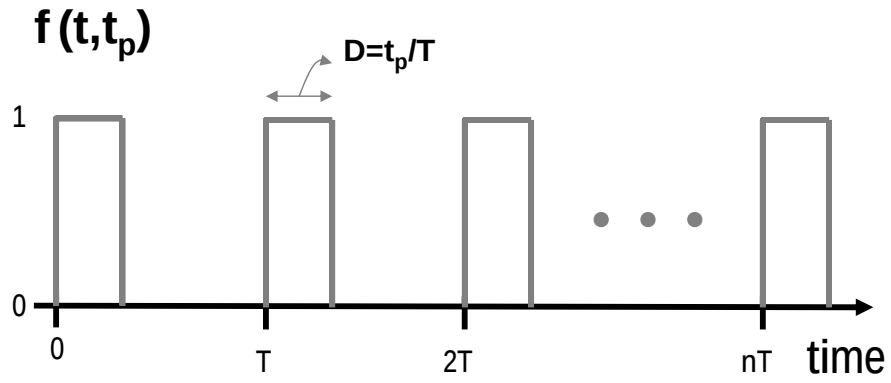

Figure A.1 A periodic rectangular function $f(t,t_p)$

In Equation A.2, $\lim_{k\to 0}\frac{1}{k\cdot\pi}\sin(k\frac{\pi}{T_0}t_p)\exp(jk\omega_0(t-\frac{t_p}{2}))=1\cdot D$. Equation A.2 expands to

$$f(t,t_p)=\sum_{k=1}^{\infty}\frac{1}{k\cdot\pi}\sin(k\frac{\pi}{T_0}t_p)\exp(jk\omega_0(t-\frac{t_p}{2}))+\sum_{k=-\infty}^{-1}\frac{1}{k\cdot\pi}\sin(k\frac{\pi}{T_0}t_p)\exp(jk\omega_0(t-\frac{t_p}{2}))+1\cdot D \qquad (A.3)$$

In a different form, Equation A.3 yields

$$f(t,t_p)=\sum_{k=1}^{\infty}\frac{1}{k\cdot\pi}\sin(k\frac{\pi}{T_0}t_p)\exp\left(jk\omega_0(t-\frac{t_p}{2})\right)+\sum_{k=1}^{\infty}\frac{1}{(-k)\cdot\pi}\sin((-k)\frac{\pi}{T_0}t_p)\exp\left(j(-k)\omega_0(t-\frac{t_p}{2})\right)+1\cdot D \qquad (A.4)$$

Equation A.4 is factorized as

$$f(t,t_p)=\sum_{k=1}^{\infty}\frac{1}{k\cdot\pi}\sin(k\frac{\pi}{T_0}t_p)\left(\exp\left(jk\omega_0(t-\frac{t_p}{2})\right)+\exp\left(j(-k)\omega_0(t-\frac{t_p}{2})\right)\right)+1\cdot D \qquad (A.5)$$

Equation A.5 yields

$$f(t,t_p)=\sum_{k=1}^{\infty}\frac{2}{k\cdot\pi}\sin(k\frac{\pi}{T_0}t_p)\cos(k\omega_0(t-\frac{t_p}{2}))+1\cdot D \qquad (A.6)$$

When the relationships between trigonometric functions are taken into consideration, finally Equation A.6 gives

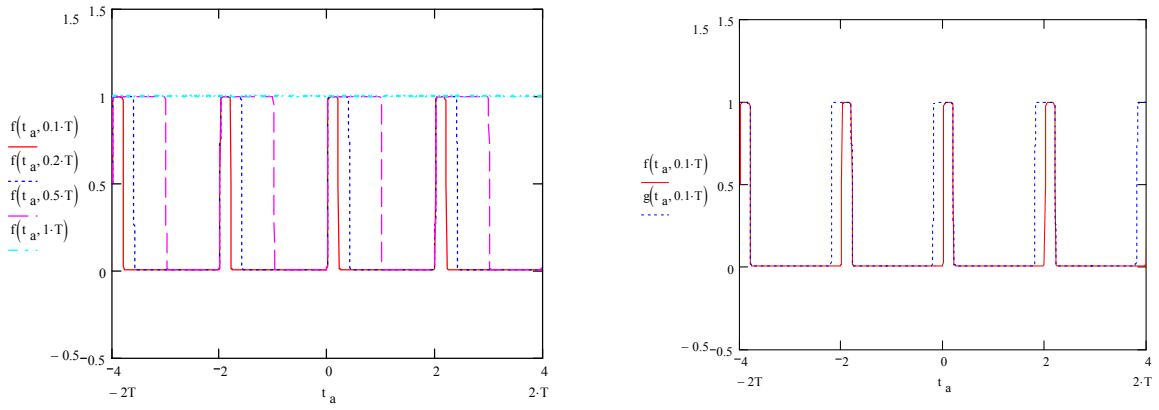

Figure A.2 The periodic rectangular function f(t,t_p).

$$f(t,t_p)=\sum_{k=1}^{\infty}\left(\frac{1}{k\cdot\pi}\left(\sin(k\omega_0 t_p-k\omega_0 t)+\sin(k\omega_0 t)\right)\right)+1\cdot D=\sum_{k=1}^{\infty}\left(\frac{1}{k\cdot\pi}\left(\sin(k\omega_0(t_p-t))+\sin(k\omega_0 t)\right)\right)+1\cdot D \tag{A.7}$$

For the verification of the Equation A.7, the periodic function f(t,t_p) is plotted with the help of MathCAD™[2] in Figure A.2. In the left of Figure A.2, the periodic functions have the different values of t_p.

The function g(t) in the right, which is used in Chapter 3.3.2, is given by

$$g(t)=(f(t,t_p)+f(t+t_p,t_p)) \tag{A.8}$$

Equation A.7 in a form of MathCAD™ is represented as

$$f(t,t_p):=\sum_{k=1}^{500}\left[\frac{1}{k\cdot\pi}\cdot\sin\left[k\cdot\omega_0\cdot(t_p-t)\right]+\frac{1}{(k\cdot\pi)}\cdot\sin(k\cdot\omega_0\cdot t)\right]+\frac{1\cdot t_p}{T} \tag{A.9}$$

A.2 PERIODIC FUNCTION $m_0(t)$

The periodic function $m_0(t)$ is mathematically expressed with the pre-described function $f(t,t_p)$ as

$$n(t) = 1 - [\, f(t + t_p, t_p) + f(t, t_p)] \tag{A.10}$$

Substituting the correspond terms from Equation A.7 into Equation A.10 yields

$$1 - \left(\sum_{k=1}^{\infty} \left(\frac{1}{k \cdot \pi} \left(\sin(k\omega_0(-t)) + \sin(k\omega_0(t + t_p)) \right) + 1 \cdot D \right) - \left(\sum_{k=1}^{\infty} \left(\frac{1}{k \cdot \pi} \left(\sin(k\omega_0(t_p - t)) + \sin(k\omega_0(t)) \right) + 1 \cdot D \right) \right. \right. \tag{A.11}$$

Equation A.11 expands to

$$1 - 2 \cdot D - \sum_{k=1}^{\infty} \left(\frac{1}{k \cdot \pi} \left(\sin(k\omega_0(-t)) + \sin(k\omega_0(t + t_p) + \sin(k\omega_0(t_p - t)) + \sin(k\omega_0(t)) \right) \right) \tag{A.12}$$

When the following trigonometric relationships are taken into consideration

$$\sin(A + B) + \sin(A - B) = 2 \sin A \cos B \tag{A.13}$$

Equation A.12 yields Equation A.14:

$$1 - 2 \cdot D - \sum_{k=1}^{\infty} \frac{2}{k \cdot \pi} \left(\sin(k\omega_0 t_p) \cdot \cos(k\omega_0 t) \right) \tag{A.14}$$

Since D is defined as t_p/T_0 and ω_0 is given by $2\pi/ T_0$, Equation A.14 rewrites to

$$\left(1 - 2 \cdot \frac{t_p}{T_0} \right) - \sum_{k=1}^{\infty} \frac{2}{k \cdot \pi} \left(\sin(2\pi \cdot k \frac{t_p}{T_0}) \cdot \cos(2\pi \cdot k \frac{t}{T_0}) \right) \tag{A.15}$$

The Fourier transform of cosine term in Equation A.15 [1] is given by

$$\frac{1}{2} \left(\delta(f - k \cdot f_0) + \delta(f + k \cdot f_0) \right) \tag{A.16}$$

Finally the Fourier transformed expression of $m_0(t)$, $M_0(f)$, is obtained as

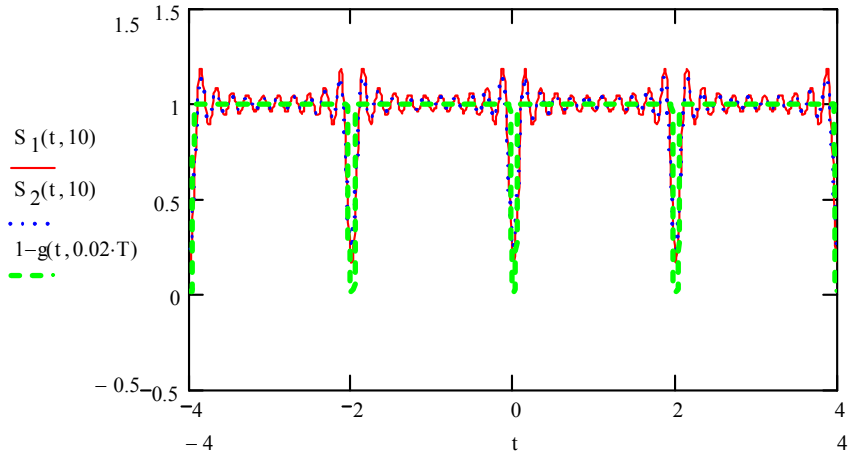

Figure A.3 S1 corresponds to Equation A.22 and S2 to Equation A.19, respectively.

$$N(f)=\left(1-2\cdot\frac{t_p}{T_0}\right)\delta(f)-\sum_{k=1}^{\infty}\frac{1}{k\cdot\pi}\sin(2\pi\cdot k\frac{t_p}{T_0})\cdot\left(\delta(f-k\cdot f_0)+\delta(f+k\cdot f_0)\right) \tag{A.17}$$

Interestingly, when t_p is much smaller than T_0,

$$\sin(2\pi\cdot k\frac{t_p}{T_0})\sim 2\pi\cdot k\frac{t_p}{T_0} \tag{A.18}$$

Thus Equation A.17 yields,

$$N(f)\approx\left(1-2\cdot\frac{t_p}{T_0}\right)\delta(f)-\sum_{k=1}^{\infty}2\frac{t_p}{T_0}\cdot\left(\delta(f-k\cdot f_0)+\delta(f+k\cdot f_0)\right)=\delta(f)-\sum_{k=-\infty}^{\infty}2\frac{t_p}{T_0}\cdot\left(\delta(f-k\cdot f_0)\right) \tag{A.19}$$

Under this assumption, we get

$$n(t)=1-2\frac{t_p}{T_0}\sum_{k=-\infty}^{\infty}\exp(j\cdot 2\pi\cdot k\cdot f_0\cdot t) \tag{A.20}$$

These expressions (Equation A.19 and A.22) are plotted with the help of MathCAD™ [2]

A.3 INPUT DEVICE NOISE EXTRACTION

Recalling Equation 3.14 and referring to Figure 3.11, we obtain the difference between the input referred noise of the operational amplifier ΔS_{vin}^2, when the 1/f noise reduction principle is applied and constant bias is applied[1)].

$$\Delta S_{vin}{}^2 = \Delta\left(\sum_{i=1}^{n} S_{vg\,i}{}^2\left(\frac{A_{vni}}{A_{v0}}\right)^2\right) = \sum_{i=1}^{2} \Delta S_{vg\,i}{}^2\left(\frac{A_{vni}}{A_{v0}}\right)^2 \tag{A.21}$$

In Equation A.18, $\Delta S_{vin}{}^2 = S_{vin}^{\#}{}^2 - S_{vin}{}^2$, and $S_{vin}^{\#}{}^2$ the input referred noise of the operational amplifier, where the 1/f noise reduction principle is applied. $S_{vin}{}^2$ is the noise of the operational amplifier, where a static constant bias is applied. Other terms are already depicted in Equation 3.14, 4.10 and Table 3.1.

Normalization of Equation A.18 with respect to $S_{vin}{}^2$ gives

$$\left(\frac{\Delta S_{vin}{}^2}{S_{vin}{}^2}\right) = \left(\sum_{i=1}^{2} \Delta S_{vg\,i}{}^2\left(\frac{A_{vni}}{A_{v0}}\right)^2\right) \Big/ \left(\sum_{i=1}^{n} S_{vg\,i}{}^2\left(\frac{A_{vni}}{A_{v0}}\right)^2\right) \tag{A.22}$$

When we use $S_{vg\,1+2}{}^2$ for the sum of input transistors T1 and T2, Equation A.19 rewrites to

$$\left(\frac{\Delta S_{vin}{}^2}{S_{vin}{}^2}\right) = \Delta S_{vg\,1+2}{}^2 \cdot \left(\sum_{i=1}^{2}\left(\frac{A_{vni}}{A_{v0}}\right)^2\right) \Big/ \left(\sum_{i=1}^{n} S_{vg\,i}{}^2\left(\frac{A_{vni}}{A_{v0}}\right)^2\right) \tag{A.23}$$

Equation A.20 can be expanded to:

$$\left(\frac{\Delta S_{vin}{}^2}{S_{vin}{}^2}\right) = \left(\frac{\Delta S_{vg\,1+2}{}^2}{S_{vg\,1+2}{}^2}\right) \cdot \left(\sum_{i=1}^{2} S_{vg\,i}{}^2\left(\frac{A_{vni}}{A_{v0}}\right)^2\right) \Big/ \left(\sum_{i=1}^{n} S_{vg\,i}{}^2\left(\frac{A_{vni}}{A_{v0}}\right)^2\right) \tag{A.24}$$

[1)] It should be noted here that only the input devices T1 and T2 are replaced with the switched MOSFET architecture.

And the rearrangement of Equation A.21 yields:

$$\left(\frac{\Delta S_{vg_{1+2}}{}^2}{S_{vg_{1+2}}{}^2}\right)=\left(\frac{\Delta S_{vin}{}^2}{S_{vin}{}^2}\right)\cdot\left(\left(\sum_{i=1}^{n} S_{vg_i}{}^2\left(\frac{A_{vni}}{A_{v0}}\right)^2\right)\right)/\left(\sum_{i=1}^{2} S_{vg_i}{}^2\left(\frac{A_{vni}}{A_{v0}}\right)^2\right) \tag{A.25}$$

The change in the input device noise can be extracted from the operational amplifier noise measurement when all terms in the right-hand-side of Equation A.22 are known.

A.4 REFERENCE FOR APPENDIX

[1] E. Kreyzig, Advanced Engineering mathematics, 7th edition, John Wiley & Sons, New York, 1993

[2] User Guide Book, MathCAD, MathSoft Inc. 2000