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Development and Electrical Characterization of Air Gap Structures for Advanced Metallization Schemes

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Abstract

The *RC*-delay and crosstalk noise of the interconnect system are major problems in modern and future high-performance semiconductor chips. For that reason, the coupling capacitance or the *k*-value of the insulator between the metal lines has to be reduced, which can be achieved by substituting SiO_2 by so-called low-*k* materials or by integration of cavities, called air gaps. In this work, air gaps fabricated by the selective O_3/TEOS deposition are considered for reduction of the line-to-line capacitance. Different integration schemes with air gaps were fabricated; air gaps requiring an additional lithography in a single and double layer Cu damascene metallization, self-aligned air gaps in Cu and in tungsten metallization, utilizing RIE (reactive ion etch) processing and air gaps fabricated by use of non-conformal deposition processes for the insulator in a 90nm Al RIE metallization scheme. For comparison of the properties of air gaps, structures were fabricated with and without air gaps.

The investigation shows that air gaps offer a substantial reduction of the line-to-line capacitance up to 50%, corresponding to an effective *k*-value of $k_{eff} = 2.3$ while using of standard SiO_2 and Si_3N_4 as materials of choice for the insulator. Measurements from the first to the second metal layer show, as expected, only a marginal reduction of the coupling capacitance of 10%. It could be shown that due to the hybrid structure of air gaps, the crosstalk can be reduced more efficiently than with a uniform low-*k* material. As a consequence of the high aspect ratio of the metal lines, the self-aligned air gaps in Al RIE metallization results in a very low effective *k*-value ($k_{eff} = 1.8$). All k_{eff}-values obtained by simulations are in good agreement with the measured capacitance values. The k_{eff}-value strongly depends on the geometry variations, which have been evaluated by additional simulations and can be optimized by extending the air gaps above and below the metal lines and increasing the aspect ratio of the metal lines. Vertical and horizontal air gap displacements are not critical. A $k_{eff} = 1.9$ was calculated for air gaps in SiO_2 material, a line aspect ratio of 2.0 and an air gap height of 1.4 times the line height. The breakdown field strength of air gap structures is lower (5-6MV/cm) than of full structures (8.4MV/cm). Compared to full structures, the leakage current of air gap structures is 30% higher at an electric field strength of 1MV/cm and 125°C. This can be explained by surface leakage currents and field enhancement inside the air gaps. The conduction mechanism between metal lines isolated by air gap structures can be described by the Frenkel-Poole mechanism at 20°C and Schottky emission at 140°C. A Frenkel-Poole behavior of full structures can be seen at all temperatures. Electromigration reliability tests showed an activation energy value of $E_a = 0.79 \pm 0.05$eV and current density exponent of $n = 1.1 \pm 0.2$ for air gaps and $E_a = 0.83 \pm 0.07$eV, $n = 1.1 \pm 0.2$ for full structures. Despite totally different failure mechanisms observed by SEM, the structures show comparable extracted lifetimes of 10.6a for air gap and 9.6a for full structures at 105°C, 5mA/μm^2 use conditions. Finally, the impact of air gaps on self-heating of the metal lines was measured and simulated, showing a 75% higher temperature increase compared to structures in dense SiO_2. In relation to the integration of porous low-*k* materials as intermetal and interlevel dielectric, the temperature increase of air gaps is only one quarter.

The results show that air gaps fabricated by the selective O_3/TEOS deposition can be integrated in a damascene or RIE metallization scheme. They display very promising electrical properties and exhibit an attractive alternative to low-*k* or ultra-low-*k* materials.

Contents

1 Introduction

The information technology revolution and enabling era of semiconductor integration have initiated an ever-increasing level of functional on-chip integration, driven by the need for higher circuit complexity, higher power density and higher operating frequencies. The larger number of transistors and bigger chip sizes lead to a more complex interconnect system. The number of wires increases with the square of the number of transistors and their average length increases linearly with the chip size. The functionality of an interconnect system is to distribute clock, data buses and other signals and to provide power/ground to and among the various circuits and systems on a chip. As gate lengths of the transistors approach 50nm and below, there is a demand for interconnect widths to decrease to similar dimensions. While traditional transistor scaling has thus far met this challenge, multilevel wiring is increasingly becoming a bottleneck in the fabrication of high-performance circuits. The growing influence of interconnect parasitics on crosstalk noise and RC-delay as well as electromigration and power dissipation concerns have stimulated the introduction of low-resistivity copper and low dielectric constant materials to provide performance and reliability enhancement [Hav01].

The industry is still in the process of a very difficult transition from silicon dioxide, silicon nitride and the dual damascene integration process to low-*k* and ultra-low-*k* materials. These dielectric materials exhibit some of the best combinations of mechanical, electrical, and chemical stability properties that integration engineers have had the luxury of working with. Although integrated circuits with copper-based metalization were introduced in 1998 with silicon dioxide as intermetal dielectric, the lowering of insulator dielectric constant predicted by the ITRS has been problematic. Instead of the revolutionary path contemplated in the ITRS 2001 document, the industry has chosen an overall evolutionary path. Fluorine doped silicon dioxide $k = 3.7$ was introduced at 180nm, however, insulating materials with $k = 2.7$ - 3.0 were not widely used until 90nm [ITR05]. Even at 60nm, the effective *k*-value will be still around 3.0 and only dense materials will be used. It is even believed that it will be very challenging to reduce the effective *k*-value far below 3.0 for future technology nodes.

The slower than projected pace of low-*k* dielectric introduction for microprocessors (MPUs) and application-specific ICs (ASICs) comes from the unexpected challenging reliability and yield issues associated with integration of these materials with dual damascene copper processing. The integration of porous low-*k* materials is expected to be even more challenging. Since the development and integration of these new low-*k* materials is rather time-invariant, the predicted acceleration of the MPU product cycle (two versus three years until 2009) will shift the achievable *k* to later technology generations. The introduction of these new low dielectric constant materials, along with the reduced thickness and higher conformity requirements for barriers and nucleation layers, pose a difficult integration challenge. Further challenges like resist poisoning, precise etching of porous materials, sidewall damage during etching, which increases the *k*-value, pore sealing to reduce diffusion, UV cure to repair the material, to name just some of them, have to be taken into consideration. Because of the foam-like structure of porous

materials, the contact with wet cleaning, etch solutions, water rinse or other liquid agents is problematic since the liquid penetrates into the film and especially water increases the *k*-value dramatically since it has a *k*-value of $k = 80$. Moreover, these new materials suffer from mechanical and thermal stability issues, reliability degradation, high metal diffusion, higher leakage currents and low dielectric breakdown field strength.

As of 2012, according to the ITRS, ultra-low-*k* dielectrics with $k < 2.0$ (ULK) will be required. Novel integration schemes may be necessary, such as air gap architecture – a hybrid dielectric stack utilizing air [ITR05]. The term "air gaps" describes cavities between adjacent metal lines filled with air or gas, or being under vacuum with a dielectric constant close to $k = 1.0$. Of course, the overall effective *k*-value is in practice larger than 1.0 since the metal lines have to be supported by some solid material. To obtain air gaps, several integration schemes are being pursued. The most straightforward approach is to remove the dielectric between the metal lines and then deposit another dielectric layer with a very non-conformal process [Arn01]. This will leave the gaps between the lines mainly unfilled. The air gaps extend above the top surface of the Cu lines and form dome-shaped voids. Despite its simplicity, this process has the drawback that for a wide spacing of the Cu lines the voids might become too high and be damaged by the subsequent metallization layer. The second approach uses a sacrificial material in which the Cu lines are embedded. The sacrificial material is capped by a porous dielectric. After the damascene process, the sacrificial material is then removed for example by a thermal process to vaporize the sacrificial material, leaving the air gaps [Daa05]. This way the air gaps fill only part of the space between the lines and moreover new porous materials need to be integrated.

The motivation of this work was to integrate and characterize air gap structures fabricated by the selective O_3/TEOS deposition as an alternative to porous ultra-low-*k* materials. The major advantage of the integration of such air gaps is that exclusively well-known conventional dielectric materials are used to achieve an effective *k*-value of as low as 2.4. The key process of our air gap fabrication is the selective O_3/TEOS deposition, which is an ozone activated deposition of SiO_2 with TEOS as precursor. This process can be treated such that the deposition only takes place on a "seed" material and is suppressed on a "base" material. The selective O_3/TEOS growth was performed on a variety of materials to investigate candidates as seed or base material. The basic principle of this selective process leads to a structure with base material on the sidewalls of the air gap trench and seed material at the top surface of the wafer. Since the selective O_3/TEOS only grows on the seed material, the air gaps are closed. The advantage over the non-conformal approach is the isotropic growth of the selective SiO_2 layer, which results in less high air gaps. Thus, the risk of opening the air gaps during CMP processing is reduced.

Various integration schemes were evaluated like air gaps in a two metal layer copper metallization scheme with an additional lithography, self-aligned air gaps in copper and tungsten RIE metallization, air gaps beneath metal lines and air gaps by non-conformal deposition in RIE aluminum metallization.

Another scope of this work was the overall characterization, like capacitance, leakage current, resistance, resistivity, breakdown voltage, thermal crosstalk, self-heating, mechanical properties and electromigration resistance of structures with air gaps compared to structures without air gaps. Further on, simulations of the line-to-line capacitance were performed to evaluate the effective *k*-value and simulations of thermal properties. The intention of this work is to highlight the advantages and risks of integrating air gaps by the

selective O_3/TEOS deposition and to compare their properties and characteristics to those of ultra-low-*k* materials. Besides integration and design, issues or potentials of air gaps within a modern metallization scheme will be discussed and assessed in detail.

2 Interconnect system in advanced semiconductor technology

The task of the interconnect system is to connect the active devices with each other and through bond pads, bond wires and pins with the outside of the chip. In recent times, the relative importance of the interconnect system called “Back End Of Line” has greatly increased, and will be likely to continue as integrated circuit technology progresses [Hav01]. The interconnect system itself consists of metal lines and via plugs, see Fig. 1. The metal lines are arranged in different levels and embedded in the intermetal dielectric (IMD). The interlayer dielectric (ILD) separates the different metal levels and comprises the via plugs, which connect the different metal levels. The interconnect system is hierarchically organized, divided in either global or local interconnects.

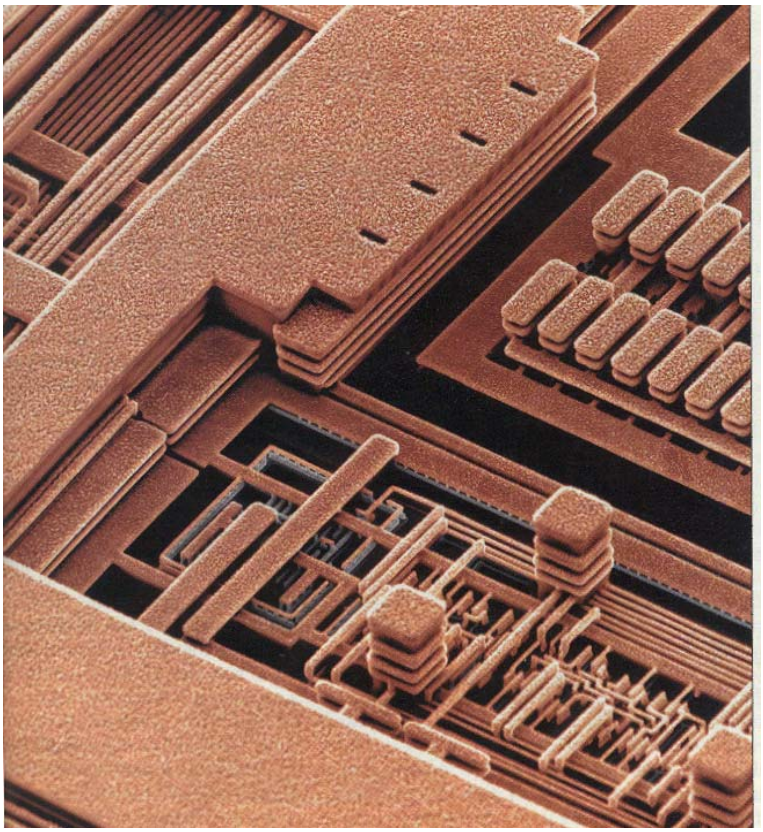


Fig. 1: Scanning electron microscope image of IBM’s six-level copper interconnect technology [IBM98]

In general, local interconnects are the lowest level of interconnects, located just above the active devices. They usually directly connect the active semiconductor regions and gates in MOS technology or bases in bipolar technology. Therefore, local interconnects can afford to have higher resistivity than global interconnects since they are rather short

[The00]. The rest of the interconnect system above the local interconnects consists of global interconnects, mostly made of Al or Cu. They are much longer than local interconnects and connect different devices and even different blocks of the circuitry. For this purpose, metals with low resistivity are used.

2.1 Requirements for advanced interconnects according to the ITRS

The international technology roadmap for semiconductors (ITRS), the essence out of Moore's law, predicts the properties of future chips. In Table 1, an excerpt of the ITRS is depicted, showing the requirements for future interconnect systems [ITR05].

Table 1: ITRS predictions for the interconnect system [ITR05]

	2005	2006	2007	2008	2010	2013	2016	2020
DRAM ½ pitch [nm]	80	70	65	57	45	32	22	14
Metal 1 A/R (for Cu)	1.7	1.7	1.7	1.8	1.8	1.9	2.0	2.0
Conductor eff. resistivity [μΩ·cm]	3.15	3.29	3.47	3.67	4.08	4.83	6.01	8.19
j_{max} [A/cm²] @ 105°C	8.9E+9	1.4E+6	2.1E+6	3.1E+6	5.1E+6	8.1E+6	1.5E+7	2.7E+7
Intermetal insulator k_{eff}	3.1-3.4	3.1-3.4	2.7-3.0	2.7-3.0	2.5-2.8	2.1-2.4	1.9-2.2	1.6-1.9
Intermetal insulator k_{bulk}	≤2.7	≤2.7	≤2.4	≤2.4	≤2.2	≤2.0	≤1.8	≤1.6

Manufacturable solutions exist and are being optimized
Manufacturable solutions are known
Manufacturable solutions are NOT known

According to the ITRS, the minimum metal line width for DRAMs will decrease from currently 70nm down to 22nm by 2016. In contrast, the aspect ratio of metal lines will further increase to lower the resistance increase with decreasing feature sizes. Unfortunately, this increase leads to a higher coupling capacitance of parallel lines [Hav01]. To reduce the coupling and *RC*-delays in interconnects, the *k*-value of the intermetal dielectric (IMD) k_{bulk} and the effective *k*-value k_{eff} between the metal lines is decreased. In former times, SiO_2 with $k = 3.9 - 4.2$ was the standard dielectric material, whereas at the moment, materials with *k*-values of about 3 are in use. The conductor effective resistivity is increasing with smaller feature sizes. This effect is described by the size-effect which originates in a scattering of the electrons at the side walls and grain boundaries which becomes more prominent as the feature size approaches the mean free path of the electrons (~ 45nm for Cu at room temperature) [Ste05]. The current density J_{max} will increase from about 1MA/cm² in 2005 up to 15MA/cm² by 2016. Extreme high current densities lead to severe reliability problems of the interconnect system due to

electromigration of metal. All in all, these requirements initiate a lot of numerous challenges for the future.

2.2 *RC*-delay in interconnects

In integrated circuits, the *RC*-delay slows down the overall performance and raises the power consumption. In Fig. 2, a simple model of one metal line connected to two MOSFETs is depicted to show the different terms contributing to the overall signal delay τ. The signal delay is the time a signal change at the input affects the output signal by 70.7% ($1/\sqrt{2}$) of its total signal level. The resistive elements are the on-resistance of the driving transistor R_{dr} (which is between 10 - 12kΩ for all considered nodes), and the wire resistance R_{wire}. The capacitive elements are the junction and gate capacitance C_{junc}, C_{gate} which originate from the active MOSFET device and the wire capacitance C_{wire} [Sch03]. These values are fixed because they are dependent of the dimensions of the MOSFET device. R_{dr} for example could only be reduced by a wider MOSFET, but increasing the width would be in total contrast to the feature size reduction.

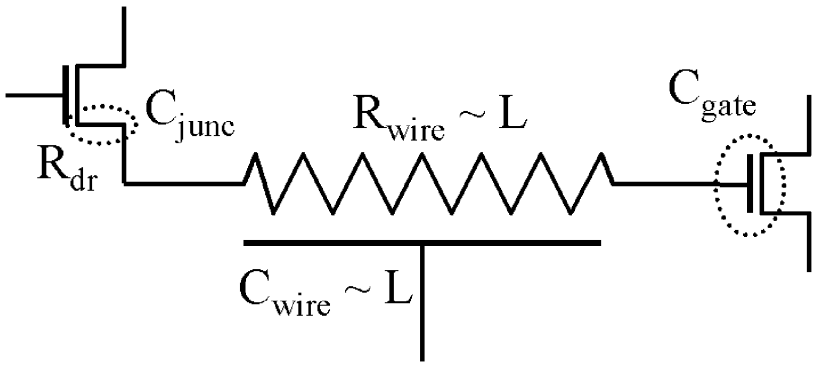


Fig. 2: Sketch of simple circuit with the parasitic elements considered

Out of this simple interconnect model, the total *RC*-delay τ of an interconnect wire can be derived, which conducts to the following formula:

$$\tau = \tau_{prop} + R_{dr}C_{junc} + (R_{wire} + R_{dr})C_{gate} + R_{dr}C_{wire} + \frac{1}{2}R_{wire}C_{wire} \qquad (1)$$

The resistance R_{wire} and the capacitance C_{wire} are dependent of the wire-length, whereas C_{junc}, R_{dr}, C_{gate} are dependent of the device design. This is particularly important for scaling, which is described by the scaling factor *f (f<1)*. The scaling factor *f* describes the shrinking of every dimension on a chip from one technology generation to another. For example, the length of an intermediate wire is shortened by the scaling factor and at the same time the cross section of the wire shrinks with f^2 because the height and the width of the wire are scaled by *f*, too. Consequently, the *RC*-delay of the short and intermediate interconnects remains more or less constant because the resistance R_{wire} is increased by the factor 1/*f*, but at the same time, the capacitance C_{wire} is decreased by the factor *f*.

In contrast to the feature scaling, the length of global wires will remain roughly constant because of the integration of increasing functionality, leading to a constant chip area [RHo01]. In this case, the capacitance remains constant, while the resistance increases

with the inverse square of the scaling factor f as described before. Therefore, $R_{wire}C_{wire}$ will also increase with $1/f^2$, indicating that the global wires will suffer most from the feature size reduction. This effect can only be lowered by the introduction of repeater circuits. In Fig. 3, the terms contributing to the overall signal delays are individually depicted.

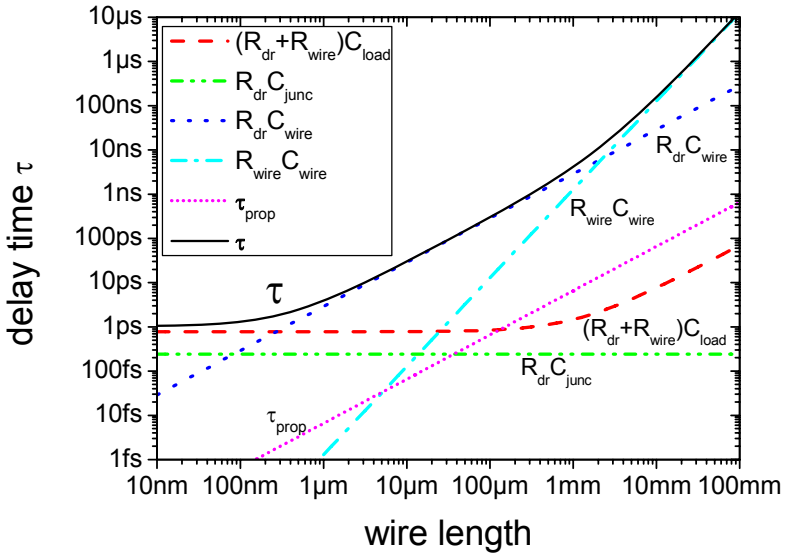


Fig. 3: Individual contributions to the delay time [Sch03]

As can be seen, the terms contribute very differently to the overall signal delay. For these calculations, minimum size transistors were assumed as driver and receiver. The propagation delay τ_{prop}, which is linear to the wire length, is negligible because it only accounts for 0.25% at the maximum of the signal delay. The so-called "device delay" $R_{dr}(C_{gate}+C_{junc})$ determines the delay for very short local connections and does not depend on the wire length. The dominant factor for short and intermediate wires is $R_{dr}C_{wire}$, which depends linearly on the wire length. The main contribution for long wires is $R_{wire}C_{wire}$, which depends only on wire parameters like cross section, length of wire and surrounding wires, dielectric. The contribution from $(R_{dr}+R_{wire})C_{gate}$ for long interconnects is negligible [Sch03].

This leaves two main delay contributions to be examined: $R_{dr}C_{wire}$ and $R_{wire}C_{wire}$. Assuming a minimum size transistor, the crossover between the two terms is usually in the range of hundreds of µm to a few mm, depending on the node size. However, for intermediate and long wires, usually larger transistors with smaller R_{dr} are used, therefore reducing the $R_{dr}C_{wire}$ contribution and shifting the crossover to smaller wire lengths. Consequently, even for intermediate wires, the $R_{wire}C_{wire}$ term cannot be neglected. The only way to improve the signal delay is to lower C_{wire} and R_{wire}. The resistivity term was already addressed by the introduction of copper replacing the higher resistivity aluminum. The capacitance can only be reduced by changing the dielectric material with a lower dielectric constant.

2.3 Crosstalk in interconnects

Crosstalk between two parallel RC lines is another important issue in the VLSI design. For instance, in combined circuits with bipolar and CMOS circuitry, the so-called BiCMOS, the CMOS large-swing logic signals and ECL small logic signals coexist on a chip. This combination may lead to malfunctions, if crosstalk induced by the high levels of the CMOS signal on the low level signals of ECL logic is so large that the noise on the ECL signal exceeds the logic threshold of ECL gates [Sak93]. As can be seen, these interactions may cause faulty functional and timing behaviors on the silicon chip [Sch03]. The timing behavior may vary extremely when two parallel lines are switched in push-pull mode. Push-pull mode means that the signal on the one metal line switches from high to low and vice versa on the other metal line. Especially bus systems can be affected dramatically, since there are long wires in parallel, and switching of the lines occurs with the system clock at the same time. In Fig. 4, a simple model of the parasitic capacitances of the interconnect system is shown.

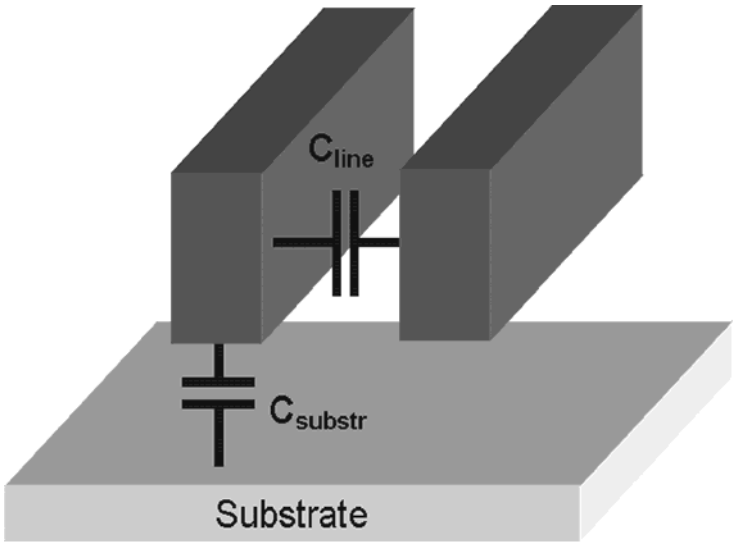


Fig. 4: Capacitive model of two parallel interconnect lines

Generally, only two parasitic capacitances affect the crosstalk behavior of interconnects; on one hand, the coupling intermetal capacitance C_{line} from line to line and on the other hand, the interlayer capacitance C_{substr}. The interlayer capacitance does not only designate the capacitance to the substrate but also to other metal lines. Practically, this capacitance is maximized when accounting lines directly above the substrate because metal lines in different levels are usually perpendicular to each other and, therefore, the face-to-face area is rather small, respectively C_{substr}. These two capacitances affect the disturb voltage induced by crosstalk $V_{x\text{-}talk}$, see following equation [Sak93].

$$V_{X-talk} \approx \frac{1}{1+\frac{C_{substr}}{C_{line}}} \tag{2}$$

The crosstalk signal $V_{X\text{-}talk}$ does not depend on the dielectric constant of the surrounding material, but on the ratio of line-to-line capacitance C_{line} and line to substrate capacitance

C_{substr}. As can be seen, it is appropriate to reduce only C_{line} to reduce crosstalk of adjacent lines. Especially in the future, crosstalk will become more important since the aspect ratio of the metal lines is increasing [ITR05], consequently C_{line} will increase.

2.4 Interconnect fabrication techniques

2.4.1 Interconnects by reactive ion etching (RIE)

The reactive ion etching RIE technique is a subtractive technique and has been used for more than 20 years for aluminum patterning. First, a silicon oxide layer is deposited on the wafer as interlayer dielectric (ILD). Then, a sandwich of a thin TiN layer serving as a barrier and adhesion layer, a thick aluminum layer, and a thin TiN anti-reflection layer is deposited. On top, a resist or double layer of hardmask and resist is deposited and patterned by a subsequent lithography step. The anti-reflection layer is necessary to prevent the aluminum from reflecting the light during lithography exposure which would lead to overexposure of the resist. This lithography resist exhibits the positive image of the metal lines (Fig. 5a). After the lithography step, the metal sandwich is dry-etched with reactive ion plasma etch (RIE) (Fig. 5b). For passivation of the metal lines, SiO_2 is deposited to close the gaps between the metal lines and to cover the metal lines. Chemical mechanical polishing of SiO_2 (CMP) may be used to planarize the wafer surface (Fig. 5c). This technique is also used for some types of tungsten metallization processing.

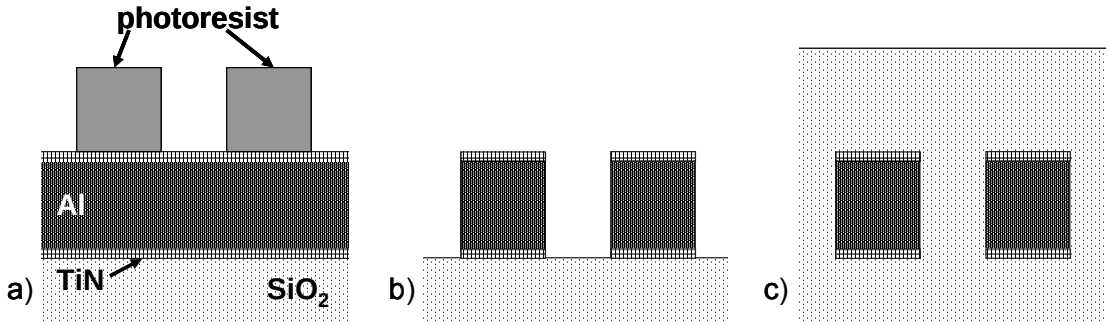


Fig. 5: RIE metallization scheme

The major advantages of aluminum metallization are that it can be easily dry-etched, it has a low resistivity and it does not contaminate Si because no diffusion of Al occurs in SiO_2 nor Si. Further on, it builds up ohmic contacts to Si and shows excellent adhesion to dielectrics [Sar03]. One severe disadvantage of aluminum is its low resistance against electromigration. For that reason, aluminum is doped with small incorporations of copper to strengthen the electromigration properties. Electromigration is the movement of atoms due to the impact of the electrons carrying the current through the wire. This effect can cause open circuits and is therefore a well-known reliability problem, see Chapter 2.9.1.

2.4.2 Interconnects by damascene technology

To reduce the line resistance and strengthen the electromigration resistance, copper was introduced as a new metallization material in 1997 [ITR05]. Unfortunately the subtractive

technique used in former aluminum technology is no more applicable due to difficult dry-etching of copper. The standard technology for the processing of copper interconnects is the damascene (in-laid) technique (Fig. 6). In contrast to the direct patterning of the reactive ion etch processing, the basis of the damascene technique is the deposition of copper into trenches of a patterned silicon oxide layer. First, a silicon oxide layer is deposited on the wafer. Then, a photoresist is deposited over the silicon oxide layer and subsequently patterned by lithography. This lithography exhibits the negative image of the metal lines (Fig. 6a). The following etching process leaves a patterned silicon oxide layer with trenches for the metal lines. Subsequently, a thin barrier layer is deposited to prevent diffusion of copper into the surrounding dielectrics and into silicon. Due to the bad adhesion of copper to dielectrics, the barrier also serves as an adhesion layer. Materials used as copper diffusion barriers are tantalum, tantalum nitride or titanium nitride. Often, both tantalum nitride and tantalum are deposited successively to obtain the better conducting alpha phase of tantalum [Tra02] (Fig. 6b). Finally, copper is deposited by electroplating on the whole wafer and polished back to the top of the patterned oxide by chemical mechanical polishing (CMP). After this step, only the trenches are filled with copper. To passivate the copper upper surface, a capping layer of Si_3N_4 or a-SiC is deposited (Fig. 6c). The damascene technique is also used for tungsten via processing. For the processing of tungsten wires both techniques - damascene or reactive ion etch - can be used.

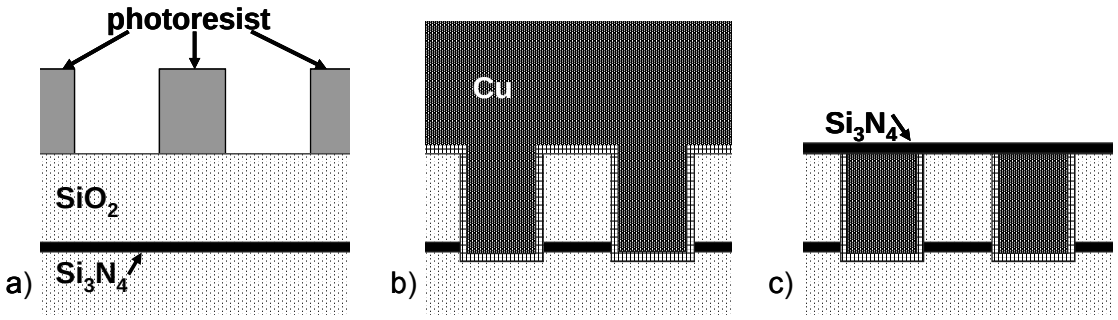


Fig. 6: Damascene metallization scheme

The major advantages of copper metallization is the lower resistivity of copper compared to aluminum and the serious increase in electromigration strength. Copper lines can carry about 3 - 6 times higher current density than aluminum lines without failure under the same stress conditions and the same dimension.

2.5 Requirements for the intermetal dielectric (IMD)

Properties required for an acceptable intermetal dielectric material are a low dielectric constant (ideally k = 1.0); mechanical, chemical and thermal stability; no moisture absorption or permeability to moisture; good thermal properties (high thermal conductivity and comparable coefficient of thermal expansion to the used metals and to silicon) and process compatibility. In Table 2, the requirements on the dielectric material are shown:

Table 2: Dielectric requirements [Vit04]

Key Performance Areas	General Requirements
Electrical	Low dielectric constant
	High breakdown strength
	Low loss factor
	High bulk resistance
	Low DC leakage current
Mechanical	Good Adhesion
	Low film stress
	High hardness
Chemical	Good patternability
	Low moisture uptake
Thermal	Good thermal conductivity
	High thermal stability

Besides the permittivity, further electric properties are of importance. The loss factor must be as low as 10^{-3} or lower over a wide range of frequencies. The breakdown voltage is another issue together with low leakage currents. Values of 2 - 3 MV/cm are needed if the material is supposed to replace SiO_2 or related compounds. Mechanical strength is important especially for bonding, packaging and for CMP. The thermal coefficient of expansion should not exceed 10ppm/°C otherwise cracks or delamination may occur. At last, environmental considerations must be taken into account. Generating large amounts of waste in processing must be avoided as well as use of poisonous precursors and byproducts. These requirements except the dielectric constant of 4.1 - 4.4 were achieved by CVD SiO_2, which was the material of choice up to now. The dielectric constant of CVD-SiO_2 is about 10% higher than of thermally grown SiO_2, because of impurities and a less stoichiometric SiO_2. As mentioned in Chapter 2.1, the International Technology Roadmap for Semiconductors calls for dielectrics with $k_{bulk} \leq 2.4$ by 2008 and $k_{bulk} \leq 2.0$ by 2012. If a reliable ultra-low-*k* dielectric system could be realized using conventional technological processes, a quantum step towards these goals would be achieved.

2.6 Low-*k* materials as IMD materials

The expression low-*k* dielectric in the semiconductor industry designates a material, which has a lower dielectric constant than SiO_2. These materials are meant as interlayer or intermetal dielectrics. They can be divided into two major groups, dense low-*k* materials and porous low-*k* materials. In general, there are three main physical ways to reduce the *k*-value of a material, first, reducing the polarity of the material, reducing the density or leaving out material. It has to be mentioned that the following *k*-values of the material are all bulk *k*-values which tend to be significantly lower than in an interconnect structure because etch stop layers, etch damage, moisture uptake or densification are neglected. Especially moisture uptake increases the *k*-value dramatically since water with its polar molecule has a *k*-value of 80. For example, for a typical comb structure, built in a

damascene scheme with a porous MSQ-based dielectric of relative permittivity k_{bulk} = 2.3, k_{eff} is 3.1 ±0.1. This structure includes a CVD SiCN etch stop (100 nm), hard mask (20 nm after CMP) and capping layer (50 nm), all of which have k = 4.3 [Kas04].

2.6.1 Dense low-*k* materials

Dense low-*k* dielectrics can roughly be divided in two groups: inorganic and organic materials. The purely inorganic materials are mostly successors of the incumbent silicon dioxide. This low-*k* materials are SiO_2 doped with fluorine (FSG) or with carbon (SiOC), the latter being an intermediate between organic and inorganic matter. The incorporation of such impurities leads to a less polar molecule and therefore reduces the *k*-value.

Silicon oxyfluoride (FSG) is a CVD-based deposited dielectric, which fulfills almost all of the requirements and is already used in production. But the problem is, that the dielectric constant can only be reduced to around 3.7. With higher fluorine content, the *k*-value could be further decreased, but the fluorine content must be limited to about 4% because otherwise fluorine evolution may cause degradation of the metal barrier or the metal lines. The stress and water absorption also increase with higher fluorine content.

Hydrogen silsesquisiloxane (HSQ) is another inorganic low-*k* material with a $k \sim 3.0$, which can be deposited by spin on [Dow05]. Furnace curing of the material at 400°C and higher results in an increase of the *k*-value accompanied by loss of hydrogen. The film stress is high and the resilience against O_2, which is usually used for resist strip is low [Cla01].

Amorphous fluorinated carbon (a-CF) films can be described as an inorganic material, because there is only carbon and fluorine present. The permittivity of 3.2 is rather high. Poor adhesion was observed on all substrates except for thermal oxide and silicon nitride and outgassing of fluorine occurs above 400°C with the *k*-value increasing.

Although organic dielectrics show an in situ low-*k* value, the thermal stability and sensivity towards oxygen at elevated temperatures or with plasma treatment are issues. Only some groups of polymers are candidates for integrated circuit processing: Fluorinated carbon (a-CF), polytetrafluorethylene (PTFE), fluorinated polyimide (FPI), polybenzoxazole (OxD), poly(arylene)-ether (PAE), parylenes, benzocyclobutene (BCB) and organo-silicon-based materials (alkyl-,aryl-siloxanes).

Si-based polymers (SiOC, MSQ) consist of a SiO_2-typical network with methyl-groups (CH_3-) attached to many of the silicon atoms. The SiOC can be deposited by spin on techniques or CVD [App05]. *K*-values reaching from 2.5 to 3.0 can be achieved. Because of the high content of organic material, SiOC-layers degrade very easily during resist stripping. Water uptake is also a problem, which degrades the *k*-value and leads to a high loss factor. Nevertheless, it was the first organo-spin-on-glass that reached integration at Sematech.

Fluorinated Polyimide (FPI) with (-CF_3) groups show good electrical (k = 2.6 - 2.9) and mechanical properties. The materials are tough, have a lower moisture uptake than normal polyimide and show high glass transition temperatures. Planarization and the reaction of excess fluorine with barrier materials seem to be problematic. Water uptake can still reach about 1wt%.

Poly(arylen)ether (PAE) is obtained by reaction of an bi-functional aromatic monomer with bisphenol giving a fully aromatic polyether chain. PAEs exhibit a $k \sim 2.6 - 2.8$. They better withstand temperature cycling than polymers. Excellent adhesion was observed on SiO_2 or Al. PAE material can be polished without a capping layer. A two-level Cu damascene structure was demonstrated by Fujitsu [LaP03].

Silicon containing benzocyclobutene (BCB) resins are spin on materials [Kaw03]. In contrast to the polymerization-reaction of polyimide, no water or other byproducts are formed and, hence, no corrosion or side reactions should occur. Because BCB contains silicon in the molecule plasma etching must be carried out with fluorine containing gas mixture. The fully cured BCB is a highly cross-linked material with excellent stability, resistant towards oxidation and very low water uptake. The loss factor over a wide range of frequency is low with a permittivity of 2.3 - 2.7 [Cla01]. The thermal stability of the BCB-film is limited to nearly 400°C. When the temperature reaches 375°C or higher, the adhesion on oxide or nitride layers deteriorates and blisters occur.

As can be seen, there is a wide spectra of dense low-*k* dielectric materials, every one with different integration issues or the necessity of additional process steps. With dense low-*k* dielectrics, the bulk *k*-value can be reduced down to 2.5. For further reduction, the density of the materials has to be decreased with the incorporation of pores filled with gas.

2.6.2 Porous low-*k* materials

The most effective way of reducing permittivity is the conversion of low-*k* materials, inorganic or organic, into nano- or mesoporous films formed by the evaporation of solvent or other sacrificial material leaving a layer with a foam-like structure. These advanced, porous dielectrics are also called ultra-low-*k* (ULK) materials. Because most of space occupied by the film is empty, the *k*-value can be as low as 1.3. The pore size in those films should be smaller than the pattern formed on their surface with a narrow distribution of pore diameters. In Fig. 7, the correlation of the porosity for two different materials versus the overall *k*-value is shown [Gol01].

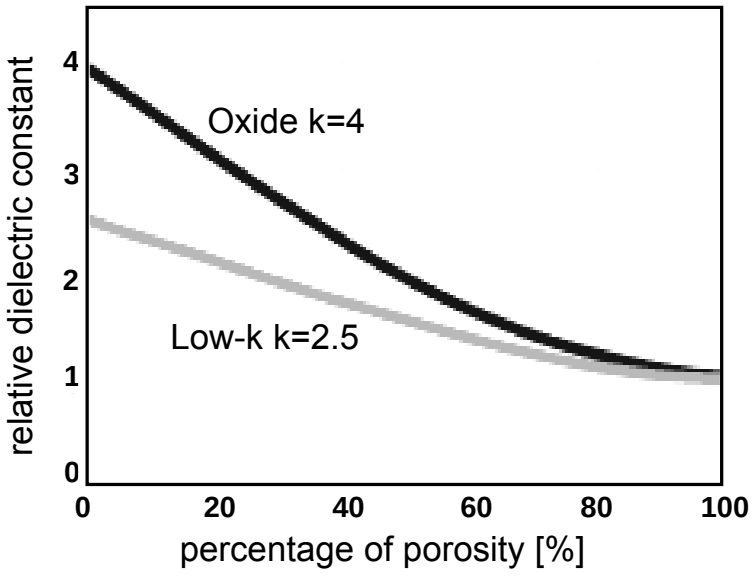


Fig. 7: Dielectric constant versus percentage of material porosity [Gol01]

As can be seen in the graph, the *k*-value can be reduced drastically by introducing pores into dielectrics. For example, when introducing 40% porosity in a material with a *k*-value of 4, the *k*-value would drop to as low as 2.3. When starting with a material with a *k*-value of 2.5, this value would drop to 1.8 with 40% porosity.
Nanoporous dielectrics are among the few materials options with ultra low-$k < 2.0$. Porous dielectrics called xerogels, nanogels, nanofoams or aerogels are commonly made by spin on deposition of dissolved organosilicates (e.g. TEOS) followed by partial hydrolysis (aging), a hydrophobic treatment and an outgassing and baking step leaving the silica species cross-linked with 30 - 80% porosity. Due to the low density of the material, the *k*-value can be as low as 1.3 - 2.5. The exact value is tunable by the process parameter changing the porosity of the product. This approach works for example with HSQ and two solvents with different boiling points [Iac02]. The pores are made by boiling out a solvent during a cure step, which lowers the dielectric constant of HSQ significantly to 2.0 - 2.5, depending on pore size. Afterwards, a hydrophobic treatment is necessary to prevent water absorption. Despite this treatment, i.e. conversion of hydrophilic surface silanole groups into hydrophobic trimethylsilyl groups ($-Si(CH_3)_3$), moisture uptake is still an issue.

Porous PAE materials have also been developed showing a $k = 1.9 - 2.2$ with good adhesion. A single layer Cu damascene integration was completed, but Young's modulus was reduced by 50% and there has been some decrease in thermal stability and plasma resistance due to the higher exposed surface area [Leu00].

Other nanoporous films can be formed via a two-phase controlled nanophase separation of a blend, hybrid or copolymer system. Porosity is controlled by selective removal of sacrificial components. IBM is characterizing porous organosilicates (nanofoams) with *k*-values of < 1.7 at $< 40\%$ porosity [Cla01]. These materials demonstrate high thermal stability and process simplicity. The nanoporous inorganic-organic hybrids are created through the vitrification of low molecular weight silsesquioxane (MSQ) in the presence of highly branched thermally labile aliphatic polyesters of controlled molecular weight and architecture. The thermally labile pore generator decomposes by heating to 350 - 400°C to leave behind pores in the inorganic oxide. The combined structure contains closed-cell pores in a hydrophobic matrix, minimizing moisture absorption.

Process integration of porous materials is very challenging because these dielectrics are mechanically weak and have large internal surface areas which can absorb moisture. They are brittle, generate particles and are easily attacked by etching, ashing, cleaning and CMP processes. Etching holes is a problem and migration of metals into the pores may occur. In Fig. 8, a metal line, etched via and line trenches in a porous low-*k* dielectric are shown, elucidating some of the integration issues associated with porous low-*k* materials:

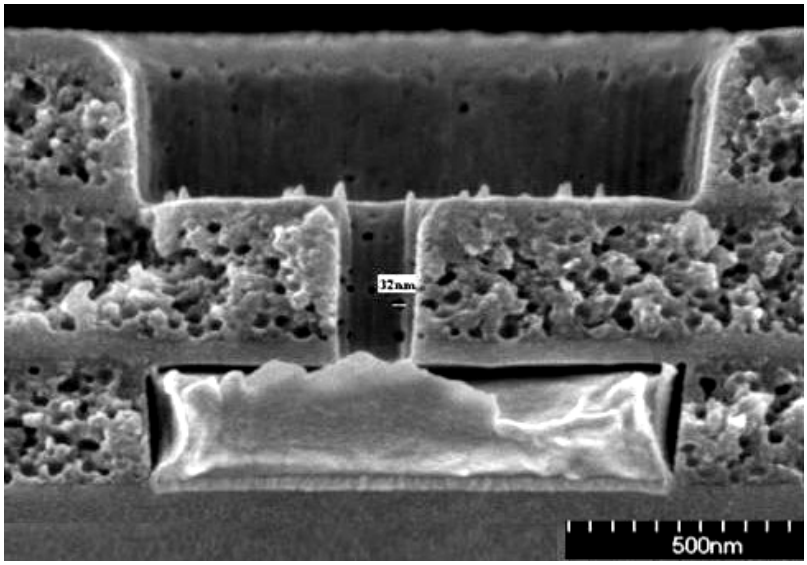


Fig. 8: SEM image of interconnects in a porous low-*k* dielectric [Pfe04]

A further issue associated with ULK materials is plasma damage, which leads to a less porous sidewall, see Fig. 8. The pore sealing itself is necessary because it prevents metal intrusions into the pores during metal deposition. Unfortunately, this effect leads directly to an increase of the material's *k*-value and therefore of k_{eff} of the insulation scheme. And even worse, the percentage of k_{eff} increase is higher with decreasing feature sizes as the thickness of the damaged surface layer does not decrease with scaling of the feature sizes. The pores also degrade dielectric breakdown voltage as well as increase the difficulty of depositing continuous films on these dielectric surfaces [Pfe04].

In the first integration experiments of low-*k,* films resist and via poisoning were a major problem. Via poisoning occurs when etched and stripped dielectric sidewalls absorb moisture prior to via filling, leading to metal corrosion respectively high via resistance. The moisture absorption takes place with the reaction of hydrogen bound to the low-*k* surface (during etching) and oxygen (during strip process). Resist poisoning can be avoided by plasma sources that convert nitrogen or ammonia gases to atomic nitrogen that quickly react with hydrogen and diffuse into the low-*k* films. Thereby, the hydrogen is bonded and cannot react with oxygen. Significant process work is required to eliminate such contamination [Cla01].

Further on, the Young´s modulus due to the porous structure of these soft ULK materials is much lower than of dense materials. Thermal coefficient of expansion is very high and may cause cracks in the film. Thermal conductivity is very low and may cause power dissipation problems. Some of these problems can be solved by depositing an oxide or nitride cap layer over the porous material, but this of course increases the effective *k*-value. In Fig. 9, an estimation of the thermal conductivity and the dielectric constant versus the future technology nodes is depicted [Chi02]. As can be seen, the effective *k*-value is directly correlated to the thermal conductivity, thus leading to very low thermal conductivity values for future technologies.

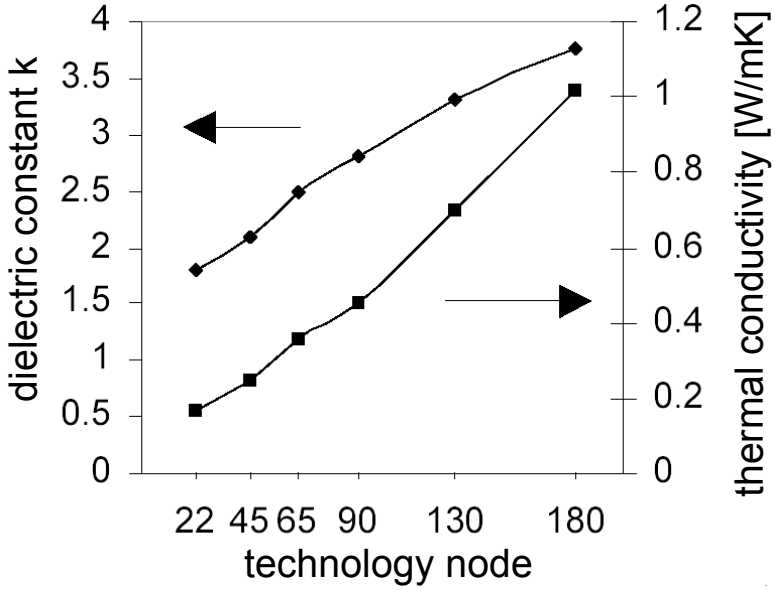


Fig. 9: Dielectric constant versus thermal conductivity of dielectrics [Chi02]

Despite the introduction of copper-containing chips in 1998 with silicon dioxide insulators, problems arose when reducing the insulator dielectric constant predicted by the ITRS. Although fluorine-doped silicon dioxide ($k_{bulk} = 3.7$) was introduced at 180nm, the use of insulating materials with $k_{bulk} \leq 2.7 - 3.0$ was not very common until 90nm. Contrary to the prediction, it soon was obvious that the reliability and yield issues associated with the integration of these materials with dual damascene copper processing would be a challenge, with the integration of porous low-*k* materials even being a higher challenge. The combination of introducing these new low dielectric constant materials and reducing the thickness and higher conformality requirements for barriers and nucleation layers turns out to be an integration difficulty [ITR05].

2.7 Air gaps as an alternative approach

Air gaps based on well-known conventional materials may be a viable alternative. The term air gap describes cavities between adjacent metal lines filled with air or gas. Since air/gas/vacuum has the lowest permittivity of $k \sim 1$ among all materials it looks very beneficial for electrical insulation purposes in interconnect schemes. In addition, air gaps can offer a scalable solution for multiple technology nodes. Of course, the overall effective *k*-value is in practice larger than 1 since the metal lines have to be supported by some solid material. As mentioned before, similar restrictions also apply to more conventional low-*k* or ultra-low-*k* approaches. There are various ways of producing air gaps, each with different advantages and disadvantages as functions of process maturity and targeted dielectric constant.

2.7.1 Gas dome concept as ultimate low-*k* solution

The gas dome concept is the most aggressive air gap approach. In the gas dome dielectric system (GDDS), SiO_2 forms a dome, in which a gas surrounds the metal conductors

underneath, see Fig. 10. The proposed concept can be summarized like this: Over dual damascene metal structures embedded in a polymer, a very thick and dense silicon dioxide layer is deposited forming the dome. Then vias through the thick SiO_2 capping layer of the dome are fabricated. Further on, vapor ports are etched through the capping of the dome. After pyrolization of the polymer through the vapor ports, the resulting gaps are filled with gas and finally the vapor ports are closed.

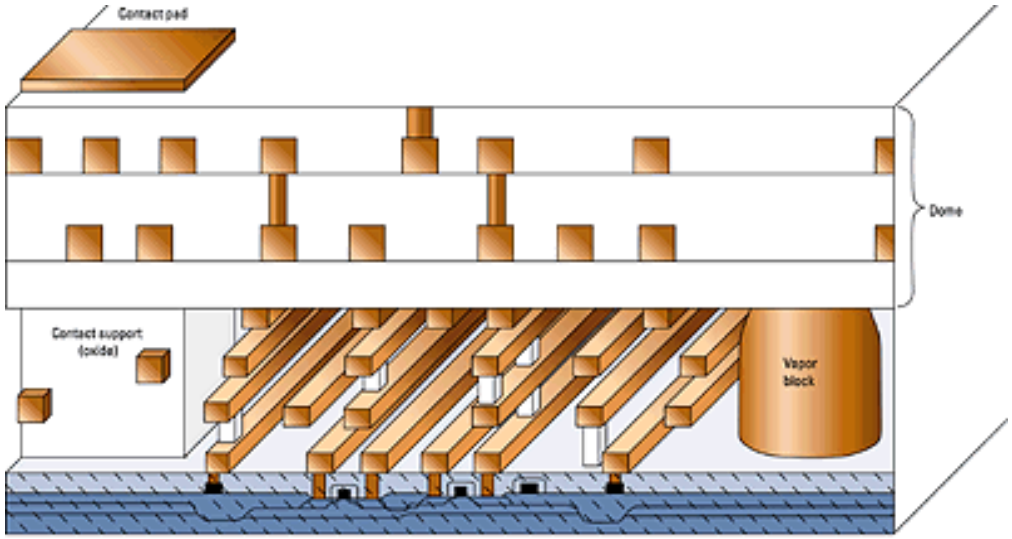
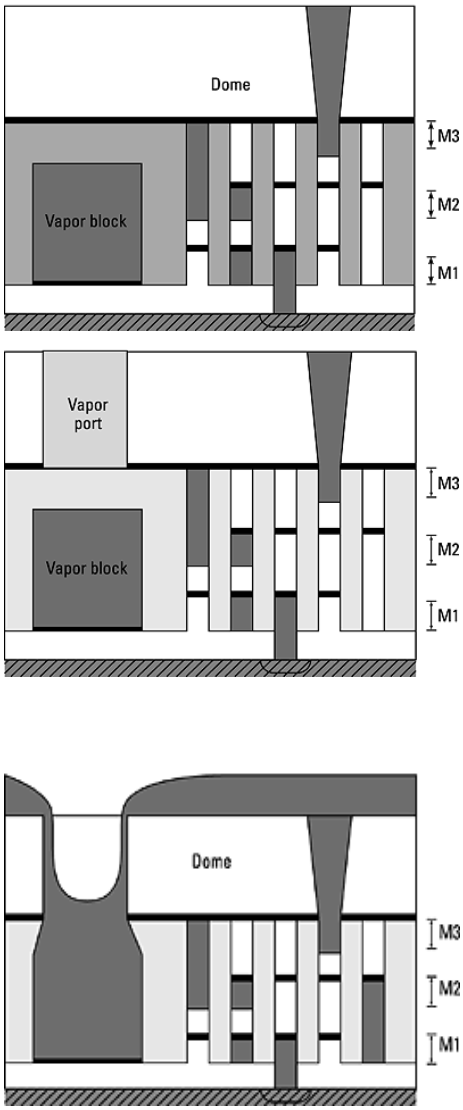


Fig. 10: The Gas Dome Dielectric System [Wad99]

As shown in Fig. 10, the dome may be a partial dome, covering only the lower level conductors or it can be a full dome where all metal levels are embedded in the gas dielectric. For purposes of process integration, reliability and thermal conductivity, the partial dome concept seems to be more practicable. If conductors are embedded in a gas, they must be supported to maintain structural integrity. The conductors can be held in place using inorganic insulating supports and braces (i.e., SiO_2) as illustrated in Fig. 10. Properly designed, these conductors can be structurally sound without the need of continuous underlying support. To add strength to long conductor lines, a thin stiffening material layer can be deposited on either the bottom or top side of the conductor [Wad99].

In the following, a possible process flow for the GDDS is depicted. Starting with a processed silicon wafer, a thick premetal dielectric (typically HDP-CVD SiO_2) is deposited and patterned to fabricate the metal support structures. Then, the SiO_2 is etched to a depth equal to the desired thickness of the first metal level and filled with a temperature degradable polymer. After curing the polymer and planarizing, a dual damascene etch is performed to define first metal level trenches and contact holes. Then, standard metallization takes place with metal deposition and CMP. The procedure for the following metal layers is alike. The next step is to deposit a thin etch-stop layer followed by a very thick and dense oxide layer, which will act as the dome for all underlying layers. In the following figure, the removal of the polymer and the closure of the vapor filled gas dome is described [Wad99]:



Damascene vias are etched through the dome, filled with metal and planarized to contact the metal lines. In the process of building up the various metal layers and vias, large metal vapor block structures are realized. These metal vapor blocks have multiple purposes, as will be shown. The next step is to etch large vapor ports in the dome layer directly above the metal vapor blocks all the way down to the low temperature degradable polymer material.

In the presence of a vacuum, this structure is then heated from the top side (RTP) to a temperature far exceeding the degradation temperature of the polymer. This causes the polymer to ash and vaporize through the vapor ports. Applying heat to the top side of the wafer causes the metal vapor block to heat up first, thus vaporizing the polymer around it. Since the dome layer heats faster than the silicon substrate, the top polymer layers will tend to vaporize before the lower layers, resulting in an orderly vaporization.

The final step is to fill the dome volume with the desired dielectric gas and close the vapor port. For better thermal conduction, light molecular gases like H_2 or He are most desirable. Backfilling could be conducted by depositing a thick metal layer under vacuum on top of the dome layer, the thickness has to be selected to almost completely fill the vapor port. The vacuum chamber is then filled with the dielectric gas and the metal around each vapor port is then spot welded, possibly with a laser, to cause the metal to flow into the port to close it.

Fig. 11: Process flow of polymer removal of the gas dome concept [Wad99]

This process guarantees the lowest achievable *k*-value, but for every metal layer, an additional lithography step plus one lithography step for the vapor port will be needed, which makes this process quite complex and expensive. Because of the complexity, no experimental results have been obtained up to now.

2.7.2 Air gap fabrication with the sacrificial layer approach

The principle of this air gap formation is the removal of a sacrificial layer after deposition of a capping layer. The metal lines are fabricated by the damascene technique in the sacrificial layer. Afterwards, a capping layer is deposited on top of the lines respectively the sacrificial layer. The final step is the removal of the sacrificial layer leaving air cavities

between the metal lines. In the following, three different techniques to produce such air gaps are shown.

2.7.2.1 Carbon layer as sacrificial material

One solution of air gaps by the removal of a sacrificial layer is the so-called NURA process which was developed at Toshiba [Ana96], as shown in Fig. 12.

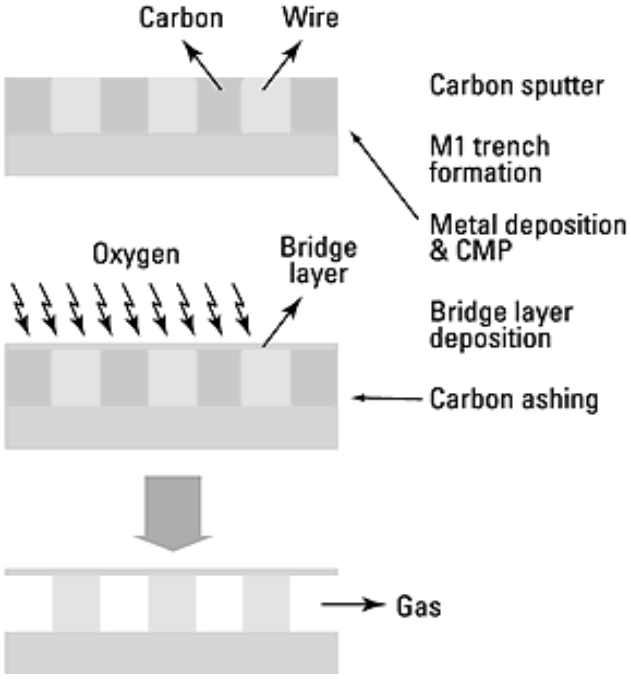


Fig. 12: Air gaps formed by sacrificial layer [Sin99]

The proposed process is a standard single damascene process with the only difference, that the trenches in which metals are filled are formed in a carbon layer instead of a dielectric film. The thickness of the carbon film is equal to the desired thickness of the interconnect lines as in the damascene process. Subsequently, metal is deposited to fill the trenches, followed by a CMP step to remove excessive metal. A thin SiO_2 dielectric capping layer (bridge layer), typically 50nm thick, is sputter deposited to cover the carbon film and the metal lines. A sputter process is chosen because this film is less dense than CVD SiO_2, which is needed to decompose the carbon through the capping layer. The final step is a thermal treatment in an oxygen atmosphere at 450°C. This causes oxygen to diffuse through the thin insulator film reacting with carbon to form carbon dioxide, which is outgassing through the thin capping layer and fills the remaining air gap [Sin99]. When using the carbon layer technique in the via level, too, the NURA process can be extended to the dual damascene processing scheme.

The wire-to-wire isolation characteristic of the NURA process is comparable to dense dielectrics up to an electric field of 1MV/cm. With that approach the delay per stage could be reduced by 56% compared to dense SiO_2 [Ana96]. Further, the overall mechanical stability of the structure is rather weak, which is explained in more detail in the following chapter.

2.7.2.2 Low-*k* material as sacrificial layer and porous capping layer

Philips Research Leuven improved the NURA process by replacing the carbon layer by a thermally degradable polymer (TDP) [Cha06]. What is even more important, they replaced the capping layer by a porous SiO_2-like material (HM2800), which ensures an easier decomposition of the sacrificial layer [Daa05]. This capping layer also serves as a hard mask for the damascene trench etch. Therefore the capping layer is deposited before the damascene processing of the metal lines, see Fig. 13. The Al and Pt contrast layers are just for TEM preparation purposes.

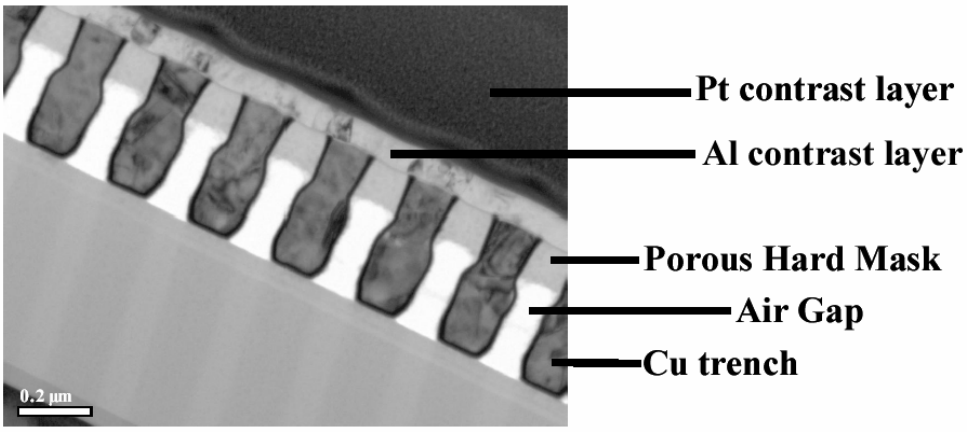


Fig. 13: 120 nm comb structure by decomposing a thermal-degradable polymer, leaving air cavities [Daa05]

This sequence is beneficial for via integration because the porous hard mask prevents metal deposition into the air gaps when filling misaligned vias (Fig. 14b). With the pure NURA process the air gaps are opened up during via trench etch when the via lithography is severly misaligned. During the subsequent metal deposition for filling the unlanded via trenches, the air gaps would be partially filled with metal, leading to high leakage currents or shorts to neighboring lines (Fig 14a).

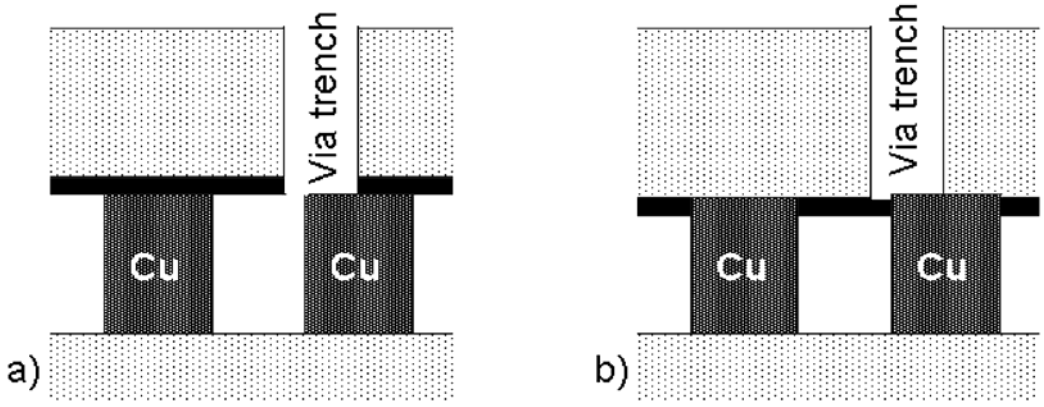


Fig. 14: Via integration with air gaps by removal of sacrificial material with the: a) NURA process b) Philips process

This air gap approach is problematic for wide dielectric spaces due to a collapse of the capping layer. However, this collapse is not an issue for the low-*k* properties because the

low effective *k*-value is only necessary in narrow spaced areas, but it is an issue for planarization (Fig. 15).

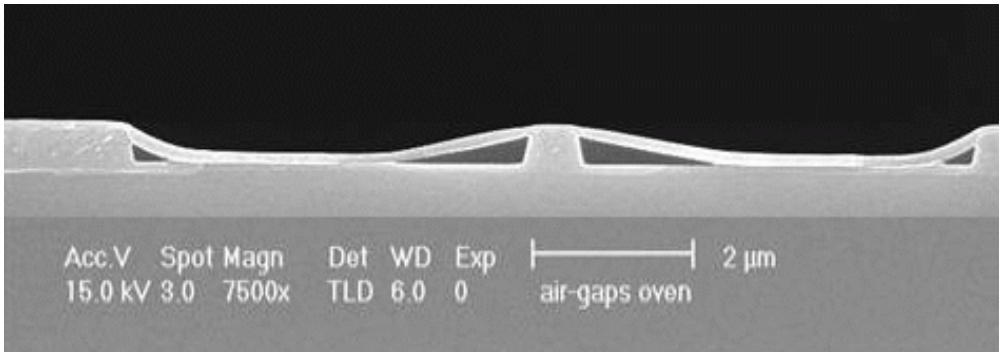


Fig. 15: Collapse of capping layer of wide dielectric spaces [Daa05]

To overcome this problem, either dummy metal structures in the design process can be introduced or a thick dielectric layer deposition and a subsequent polishing step have to be introduced for planarizing the wafer surface. Additionally, the whole structure is strengthened. According to simulations, k_{eff}-values below 2.0 could be achieved with this technique [Daa05].

2.7.2.3 Silicon oxide as sacrificial layer

The technical university Chemnitz [Sch05] works on another sacrificial layer approach in a copper damascene processing scheme with PECVD SiO_2 as sacrificial material and the use of an additional lithography step. The sacrificial SiO_2 dielectric is capped and removed by wet buffered HF etching solution through holes in the capping layer defined by lithography. This capping layer is further on called “wet etch mask”. In Fig. 16, the processing scheme of the key processes is depicted.

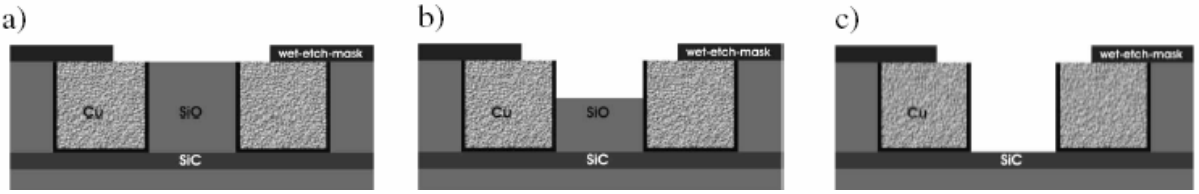


Fig. 16: Processing scheme of the air gaps by SiO_2 as sacrificial layer

As a starting point, copper damascene structures are embedded in PECVD SiO_2 with a standard etch stop layer at the bottom of the copper lines. Then, after CMP of the copper lines and the barrier, a capping layer, which also serves as “wet etch mask” is deposited to cover the top surface of the copper lines. Subsequently, the wet etch mask is patterned with an additional lithography mask such that orthogonal bands are etched to form small open spaces to the SiO_2 dielectric layer, see Fig. 16a. The distance of these bands defines the underetch of the buffered HF solution needed to remove the whole SiO_2 to form continuous air gaps. Then, the sacrificial SiO_2 dielectric between the copper lines is isotropically etched by buffered HF solution, see Fig. 16b. After proper etching time, the whole SiO_2 between the copper lines is removed, see Fig. 16c [Sch05].

In Fig. 17, an angular SEM cross-section is depicted with the formed air gaps.

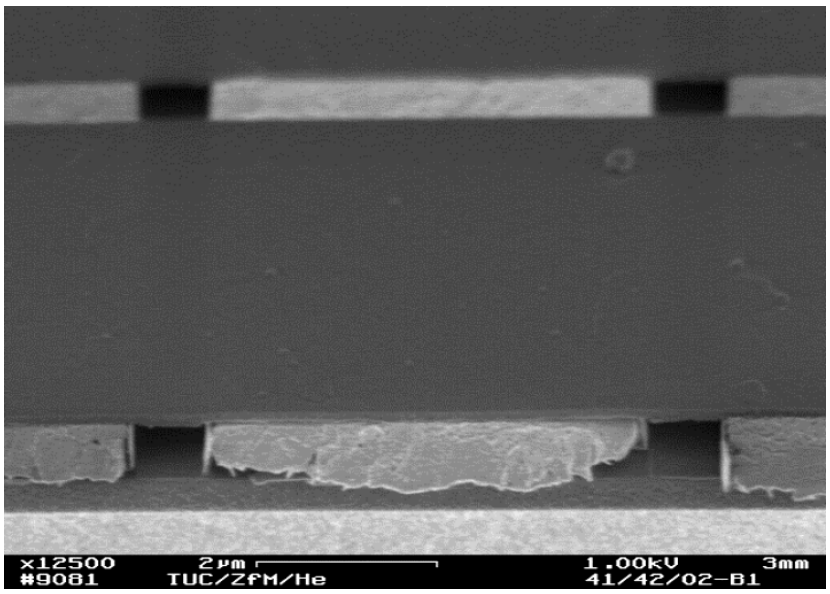


Fig. 17: Angular SEM image of air gaps by a sacrificial SiO_2 layer

The copper metal lines exhibit a line width of 5µm with adjacent air gaps of 1µm width. In the background of the image the etched orthogonal band in the wet etch mask can be seen. The light horizontal bar in the orthogonal band is the upper surface of the copper lines, divided by the air gaps (dark spots). After proper removal of the sacrificial SiO_2, the small remaining holes are closed by a non-conformal ILD CVD deposition [Sch06].

This approach can be modified with the integration of an additional capping layer of the air gaps and a spacer at the metal line sidewalls to scale down the holes for wet etch removal. Consequently, it is much easier to close the remaining holes the ILD dielectric. One big advantage for integration is that with the additional lithography the spots where air gaps are integrated can be controlled. Further on the alignment requirements for this lithography are low. The disadvantage of that approach is the need of an additional lithography and a long wet etch process, which implies the risk of underetching when etch stop layers are leaky.

2.7.3 Air gaps by non-conformal CVD deposition

2.7.3.1 Air gaps in a RIE metallization scheme

The easiest way of producing air gaps is by using a non-conformal CVD deposition in combination with an aluminum reactive ion etch RIE metallization scheme. Because of the patterning of the metal lines by etching, the spaces between the lines are already vacant, which is the perfect basis for air gaps. After the RIE process only a non-conformal CVD deposition has to be conducted to produce air gaps. In RIE metallization schemes, it is always difficult to fill the trenches between the metal lines completely. Therefore the CVD process is normally tuned to show good step coverage and conformality to suppress voids. For air gap fabrication, this CVD process is tuned to a very non-conformal deposition which generates huge voids, so-called air gaps, see Fig. 18.

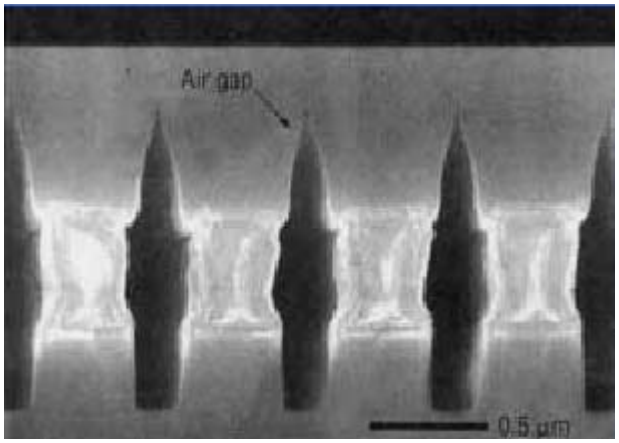


Fig. 18: SEM cross-section after SiO_2-air gap deposition [Shi98]

As can be seen, the CVD deposition is very non-conformal with almost no deposition at the sidewalls of the metal lines. The metal etch was also optimized to etch deep trenches beneath the metal lines to produce bigger air gaps. The non-conformal CVD deposition leads to very high pinnacles above the metal lines, which can be problematic during subsequent CMP processes. Critical requirements include air gap integrity because a misaligned via breaking through an air gap could lead to a decrease in insulation and contact yields. Another issue is that the height of the air gaps depends on the line space. Therefore, pertinent design rules have to be defined to control air cavity formation inside the interconnect structure [Arn01].

2.7.3.2 Air gaps in a damascene metallization scheme

With all these mandatory requirements in mind, an architecture compatible with air gap integration with non-conformal CVD deposition was developed by ST Microelectronics [Arn01]. ST extended this air gap approach to a copper damascene processing scheme and demonstrated a 5-metal-layer structure including 3 levels with adjacent air gaps, see Fig. 19.

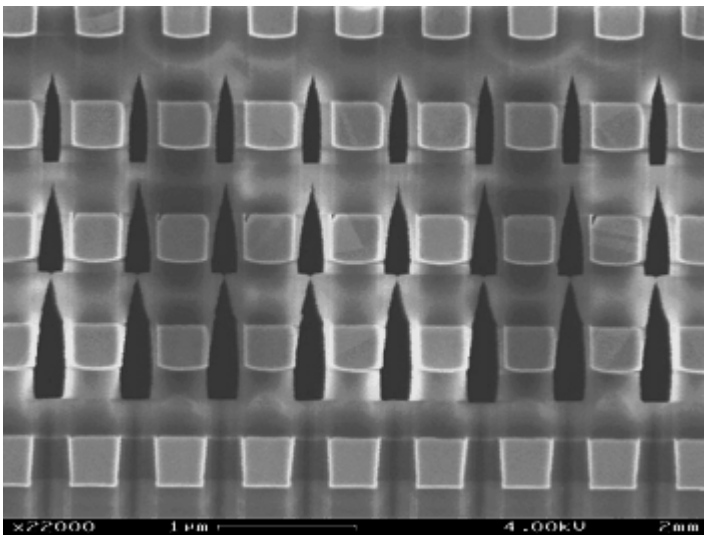


Fig. 19: SEM cross-section of 5 interconnect levels (metal space and width of 0.32µm) [Arn02]

The process steps to build these structures in a dual damascene architecture begin in a conventional way. After copper CMP at line level, an additional photo lithography and etch steps are performed to create trenches between lines for the air gaps. All trenches have the same width and are etched below the metal lines. This allows much better low-*k* performance and ensures a homogeneous formation of air gaps.

The first step is a deposition of a conformal liner. This liner serves as a spacer to center the air gaps in the middle of the trench. It is also used to form a landing zone for misaligned upper vias. The next step, the key process, is the non-conformal dielectric deposition. During this step, the air gaps are formed, the thickness of the layer is below that of the via level. The last step is a deposition of a gap fill dielectric. This step completes the stack deposition and ensures that all the air gaps formed at the lower metal level are closed well below the bottom of the interconnect lines etched in the upper dielectric level. This step was also found to planarize the surface without the need for an additional dielectric CMP process [Gos03].

The process with lithography allows to selectively integrate air gaps where a low-*k* value is necessary, for example around critical interconnect networks such as clock distributions or bus lines. Anywhere else, the dense dielectric material can be kept to reduce mechanical and thermal issues. With this approach, a reduction of the capacitance of 30 - 50% depending on material respectively geometry could be demonstrated [Arn02].

ST also demonstrated the integration of such air gaps with SiOC low-*k* material with a *k*-value of 2.9. A reduction of lateral capacitance of up to 58% compared to dense SiOC was observed. These values of coupling capacitances correspond to an effective permittivity of 1.7 [Gos03]. Also via and metal resistances, leakage currents and via chain yields were measured and compared with samples fabricated with standard SiO_2. Via yields show that contact between via and metal is as good as in the reference samples and that the issue related to via penetration into the air gap can be overcome. In terms of reliability resilience, times to failure were comparable for air gap and conventional SiO_2 and no new failure modes were detected. No extrusion of metal was observed, indicating that no significant mechanical weakness is introduced by the air gap.

According to ST, the advantages of low-*k* dielectrics based on air gaps is that the interconnect network is built in a bulk dielectric material with processes already employed or easily derived from those currently used with silicon dioxide. Design constraints and integration challenges exist, but air gaps may be easier to integrate than completely new low-*k* materials. Manufacturable processes can reduce interconnect capacitance by as much as 40 - 50% for tightly spaced metal lines [Gos03a].

Our air gap approach lacks the integration issues of CMP with the high elongated tip of ST's air gap approach because a selective O_3/TEOS process is used for closing the air gaps, leading to a flatter air gap tip. Details about the selective O_3/TEOS deposition will be shown in Chapter 3. The proposed process steps will be stated in Chapter 4.

2.8 Capacitance and k_{eff} of interconnects

2.8.1 Plate capacitor and fringe fields

With the dielectric constant *k* and the dimensions of a plate capacitor, the capacitance *C* can easily be calculated according to the following formula. This formula only applies to

plate capacitors with thin plates, a narrow space d between the plates and large side lengths of the area A compared to the space d and plate thickness. In this case, the capacitance due to fringe fields can be neglected.

$$C = \frac{A}{d}\varepsilon_0 k \tag{3}$$

As in practice, interconnect lines have an aspect ratio of 1.0 - 2.0, the fringe fields considerably contribute to the overall capacitance. Therefore the plate capacitor formula becomes inaccurate. In Fig. 20, the value calculated with the plate capacitor formula is compared to the values obtained when considering the fringe fields in dependence of the aspect ratio of the interconnect line.

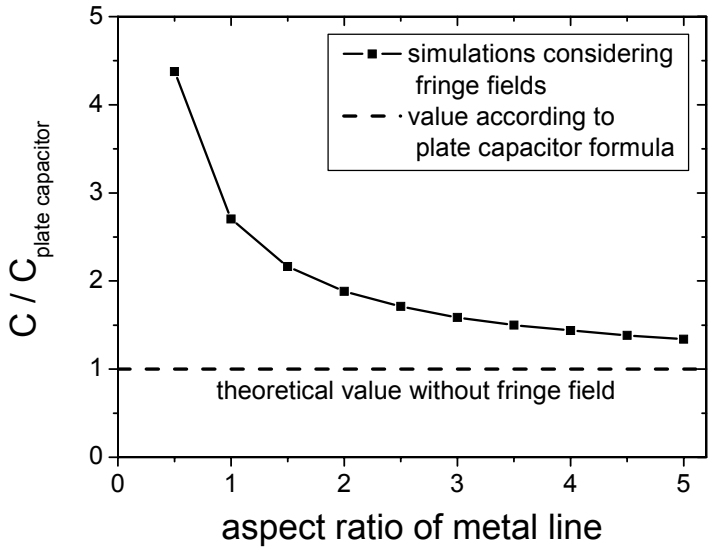


Fig. 20: Fringe field contribution to the overall capacitance [Sch03]

The calculation was carried out with parallel interconnect lines on Spicelink/Maxwell 2D, a simulation software of Ansoft. For low aspect ratios of the conductor line, the value according to equation (3) deviates massively, which is obvious since the metal lines have only a small face-to-face area but a large top area for fringe field formation. But even for very high aspect ratios of 4, the value according to equation (3) is still 44% smaller than the simulated value.

For that reason, the Maxwell equations have to be solved to exactly define the electromagnetic field between conductors. In our case, only the Poisson equation is used since we are only interested in electrostatic cases [Ans04].

$$\nabla \cdot \vec{E} = \frac{\rho}{\varepsilon_0 \cdot k} \qquad \rho \text{ charge density} \tag{4}$$

With the Poisson equation and the following expression, a direct correlation between the potential and the corresponding charge distribution can be affiliated.

$$\vec{E} = -grad\varphi \tag{5}$$

From the charge Q and the applied voltage V, the capacitance C can be calculated.

$$C = \frac{Q}{V} \tag{6}$$

Unfortunately, no closed form solution is known for the Maxwell equations. Consequently, it is not possible to calculate the capacitance of a complex structure by hand and, therefore, simulations were performed for approximation.

2.8.2 Capacitance simulations with Maxwell Spicelink

The simulations were performed with Maxwell Spicelink of Ansoft Corp, which provides quasi-static electromagnetic-field simulation for parasitic extraction of electronic components. Maxwell Spicelink is a suite of tools including a 2D field solver, a 3D field solver, a graphical interface based schematic capture tool and Maxwell SPICE [Ans04]. The Maxwell Spicelink tool suite allows a complete range of interconnects to be analyzed. RLC parasitics for arbitrary 3D structures such as wire bonds, package leads, connectors, vias, meanders, interdigitated capacitors and cross-overs can be modeled and simulated. In our case, only the 2D Extractor was used since long, uniform interconnect lines with varying surroundings were simulated.

In Fig. 21, the typical workflow of a simulation with Maxwell Spicelink is depicted. At the very beginning, the demanded parameters like capacitance, inductance, and resistance have to be defined. In our case, only the capacitance was of interest. Then, the interconnect lines with their vicinity were drawn with a CAD tool. The second step is to setup and correlate the drawn structures to material properties like their specific *k*-value or conductivity. Afterwards, the conductor type like source, floating or ground, and the boundary conditions are defined. In our case, usually periodic boundary conditions were assumed, since we simulated comb structures with a large number of long fingers in parallel. The unit cell repeated periodically consists of a central conductor line and two outer lines, the latter to be considered only in half in order to take care of the periodic boundary conditions (see Fig. 22 right). The central and the outer lines are assumed to be sources with opposite potentials. The last step is the setup of the simulation quality and the stopping criteria with the maximum number of iterations and the maximum error.

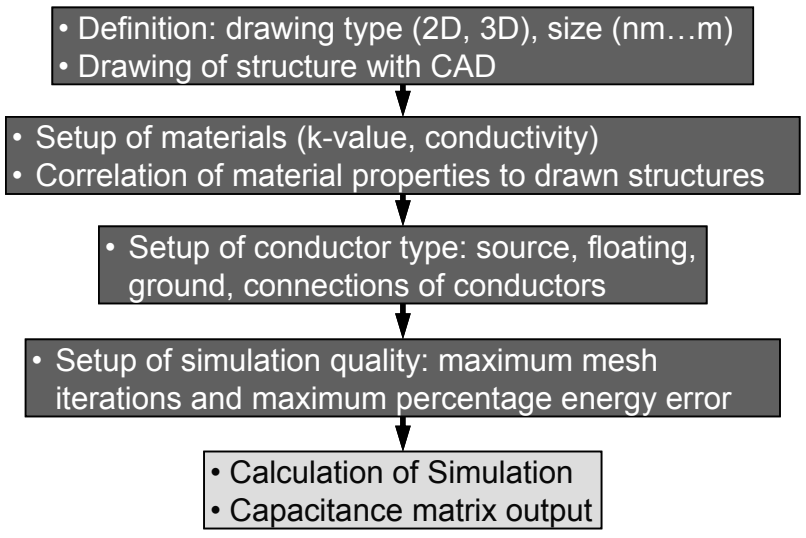


Fig. 21: Workflow of a simulation with Maxwell Spicelink

For the capacitance calculation itself, the Poisson equation has to be solved numerically for a given conductor line structure embedded in a stack of dielectric layers. For that purpose, the software uses adaptive finite element method (FEM) to generate a mesh, see Fig. 22. The idea of that method is to break up complicated shapes into simple pieces called finite elements. The mesh out of triangles is generated by the Delaunay tessellation method [Las96]. Of all possible triangulations for an arbitrary set of points, Delaunay triangles maximize the sum of the minimum angles, which reduces the number of calculations. In Fig. 22, a generated mesh and the corresponding drawn model is depicted.

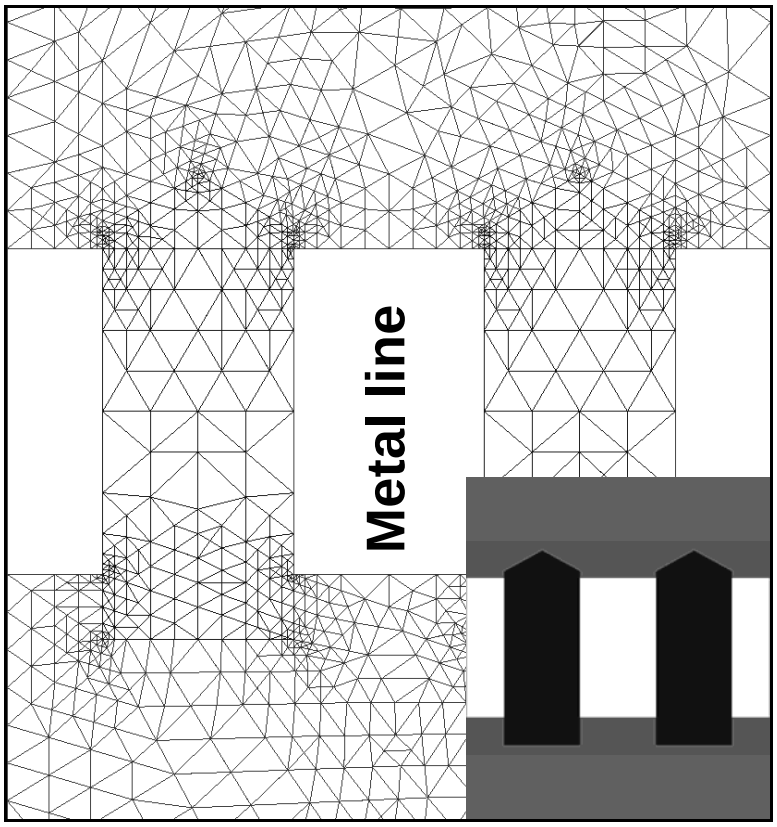


Fig. 22: Mesh of finite element calculator for capacitances

Fig. 23 shows the whole approximation process. After generating an initial mesh, the desired field in each element is approximated with a 2^{nd} order quadratic polynomial and calculated at six points of each triangle. Out of these values, a huge matrix of the Poisson equation is generated and solved. Then, the error is analyzed by comparing the findings of the current mesh with the findings of the refined mesh. When the error falls below the user specified error, the simulation is complete. Otherwise, the mesh is refined and the field is computed again. This loop is iterated until the stopping criterion is met … (or the computer crashes).

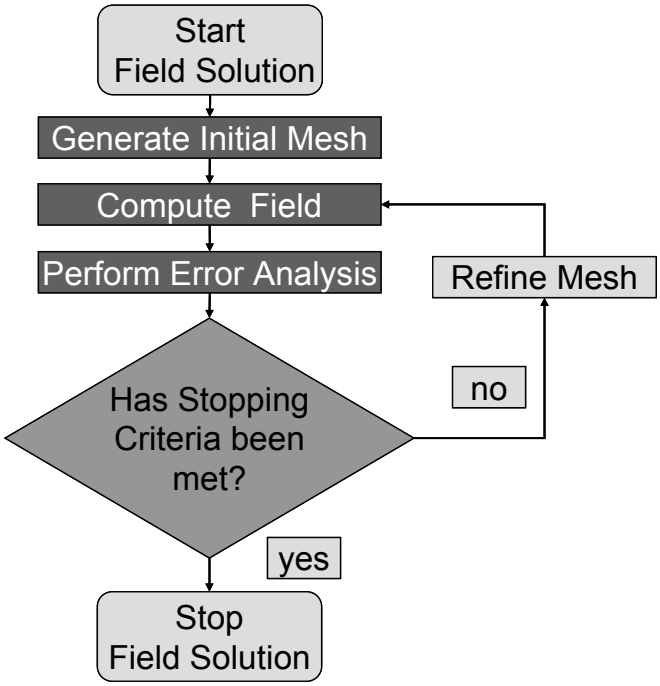


Fig. 23: Simulation process of Maxwell Spicelink

The solution itself is output in a capacitance, inductance, resistance matrix, which may then be used for generating spice models of the structure.

2.8.3 Effective *k*-value of interconnects

The relative permittivity ε_r or *k*-value is a material constant for common use conditions in semiconductor devices and describes the permeability of an electric field through matter. At high frequencies, the *k*-value degrades due to loss in the dielectric by ordering its molecules according to the external electric field. This effect is described by the loss tangent, which is small for materials used in semiconductor devices and therefore the effect can be neglected [Käm04].

Because the interconnect system consists of various different dielectrics an effective *k*-value is introduced. This is to be understood as the dielectric constant of a hypothetical, uniform material into which the metal lines with the same dimensions are embedded and which leads to the same line-to-line capacitance as the complex structure. It is not straightforward to specify the effective *k*-value of an interconnect system since it consists of a variety of materials, each with its own, known *k*-value. Therefore, theoretical calculations will have to be performed in order to determine k_{eff}. Effective *k*-values can be obtained from these calculations by relating the capacitances to those computed for a uniform dielectric matrix with known *k*:

$$k_{eff,\,complex\ structure} = k_{uniform\ structures} \frac{C_{complex\ structure}}{C_{uniform\ structure}} \tag{7}$$

It has to be emphasized that the effective *k*-value does not only depend on the materials used, but also on the geometry and the arrangement of the metal lines, as described in Chapter 5.1.4. The effective *k*-value is quite intuitive for capacitance evaluation, since it is

easy to compare different process technologies with each other independent of the used dielectrics and geometries.

2.8.4 Measurement of the capacitance

The capacitances are measured with an *LCR*-meter, which uses a four-point measurement technique and is capable of measuring capacitances or impedances at frequencies between 40Hz up to 40MHz. The *LCR*-meter itself, applies an a.c. voltage and measures the current and the phase shift of the current to the applied voltage. Out of these two values, the modulus of the impedance *Z* and the phase shift angle φ can be drawn, see example in Fig. 24.

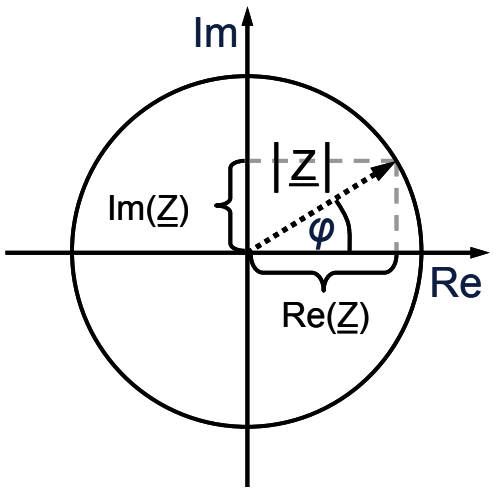


Fig. 24: Vector diagram of the impedance vector *Z* and the phase shift angle φ

Out of *Z* and φ, the real part and the imaginary part of the vector $\underline{Z}$ can be calculated.

$$R = \mathrm{Re}(\underline{Z}) = |\underline{Z}| \cdot \cos(\varphi) \tag{8}$$

$$X = \mathrm{Im}(\underline{Z}) = |\underline{Z}| \cdot \sin(\varphi) \tag{9}$$

$$\underline{Z} = R + jX \tag{10}$$

In Fig. 24, the geometrical correlation between *R*, *X* to the modulus of the vector $\underline{Z}$ is depicted; the mathematical correlation is as follows.

$$Z = |\underline{Z}| = \sqrt{R^2 + X^2} \tag{11}$$

With the real *R* and imaginary *X* impedance values, and the appropriate equivalent circuit, the capacitance/inductance and resistance can be calculated. As equivalent circuit for the measured units, capacitors, resistances and inductances can be arranged in parallel or in series.

In our case, it is required to measure capacitances with a high leakage resistance in parallel to the capacitance and a very low series resistance, which can be neglected. Consequently, the following equivalent circuit was chosen, see Fig. 25.

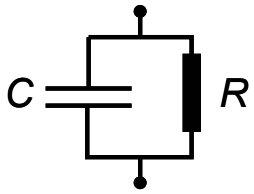


Fig. 25: Equivalent circuit for *LCR*-meter measurements

With that equivalent circuit, the parallel resistance is given by the real part of the impedance and the capacitance C can be calculated out of the imaginary part X and the measurement frequency f_m of the *LCR*-meter:

$$C = -\frac{1}{\omega_m \cdot X} \qquad \omega_m = 2\pi f_m \tag{12}$$

In practice, the equivalent circuit has to be setup in the *LCR*-meter and then these calculations are performed by the *LCR*-meter out of the measured values of Z and φ.

2.9 Reliability of the interconnect system

2.9.1 Electromigration of metal lines

Temperature stress and directed continuous current flow lead to a transport of metal atoms due to the momentum transfer from conduction electrons to lattice ions while drifting. This effect is called electromigration and leads to an increase of the line resistance until the metal line fails. The momentum originates in a superposition of an electrostatic force due to the electric field affecting the lattice ion and the opposing electron wind force. The driving force F for electromigration is given by [Hir96]:

$$F = Z_{eff} \cdot e \cdot E \tag{13}$$

Z_{eff} is the effective ion charge determined by the specific scattering mechanisms in momentum transfer, e is the elementary charge and E the electric field strength. The process of momentum transfer is dependent on the current density, which is very important for accelerated stress tests. The electromigration process is a material, current density and temperature dependent diffusion process, resulting in material removal (voids) on the one hand and material deposition (extrusions) on the other hand. This leads to an increasing resistance of lines or to lines shunted with neighboring lines. Electromigration initially takes place at grain boundaries, material interfaces and surfaces. Especially bottlenecks, like narrow wires, corners or vias, are prone to electromigration due to locally higher current density. Diffusion D and electron wind force F are obliged by the Einstein relation for drift phenomena [Heu73]:

$$v = \frac{D \cdot F}{k_B \cdot T} \tag{14}$$

Like most diffusion processes, it can be modeled by the Arrhenius law [Hir96]:

$$D_{lattice} = D_0 \cdot \exp\left(\frac{-E_a}{k_B \cdot T}\right) \tag{15}$$

$D_{lattice}$ is the diffusivity of the lattice ions, D_0 the material specific diffusion coefficient, E_a the activation energy of the process, k_B the Boltzmann constant and T the temperature. As can be seen, the diffusion process is temperature dependent which is very important for accelerated stress tests. From this model, the ion current J_{Ion} is given by [Hir96]:

$$J_{Ion} = \frac{N \cdot D_{lattice}}{k_B \cdot T} \cdot Z_{eff} \cdot e \cdot E \tag{16}$$

N is the ion density which is material dependent. For grain boundary diffusion, the equation has to be modified with the grain boundary diffusion constant and the effective grain boundary size. Volume diffusion takes place only at higher temperatures. Experiments showed that metallic materials with electron conduction have a negative Z_{eff}, which leads to an ion current and material transfer from the cathode to the anode side. This means that the electron wind force from the cathode to the anode dominates over the electric field which exerts a force on the ions in the other direction.

The electromigration process furthermore depends on the line geometry like cross-section, length and interfacial material [Pri05]. Material defects get critical since they can perform as nucleation sites for electromigration and void growth. Furthermore, the surrounding material can play an important role since it constrains the metal lines and can therefore suppress metal extrusions. The boundary materials such as the diffusion barrier and capping layer have an impact on the electromigration progress due to material stress. The material stress is dependent on the thickness, texture, and adhesion properties of the interfacial material [Tra02], [Zsc04].

The median time to failure (MTTF) of an interconnect line is inversely dependent to the ion current. Black proposed an empirical equation for the MTTF [Bla69]:

$$MTTF = C_m \cdot j^{-n} \exp\left(\frac{E_a}{k_b \cdot T}\right) \tag{17}$$

In Black's equation, C_m is a material constant, j the applied current density and n the current density exponent. This equation allows the extrapolation of electromigration lifetimes and conversion to different stress conditions. The two major parameters in electromigration testing are the activation energy E_a and the current density exponent n [Bla69]. Because of this dependency, it is easy to conduct accelerated electromigration tests by applying higher current densities and temperatures.

For copper, the activation energy was determined to vary from 0.3 - 1.2eV [Mur00] depending on the deposition and the interconnect line width. In addition, the deposition process parameters have a strong effect on the microstructure of the copper and therefore, also on the electromigration behavior. The current density exponent n was found to be between 1 and 2. Strong deviation from these values may indicate unusual behavior and certain failure mechanisms not related to pure electromigration [Fan98].

In practice, electromigration tests are performed with packaged samples with long metal lines at elevated temperatures and currents. During the test, the resistance over time is monitored. The standard failure criterion is determined by a resistance increase, due to

voiding of 20% from the initial value, see Fig. 26 The term DUT means “device under test”.

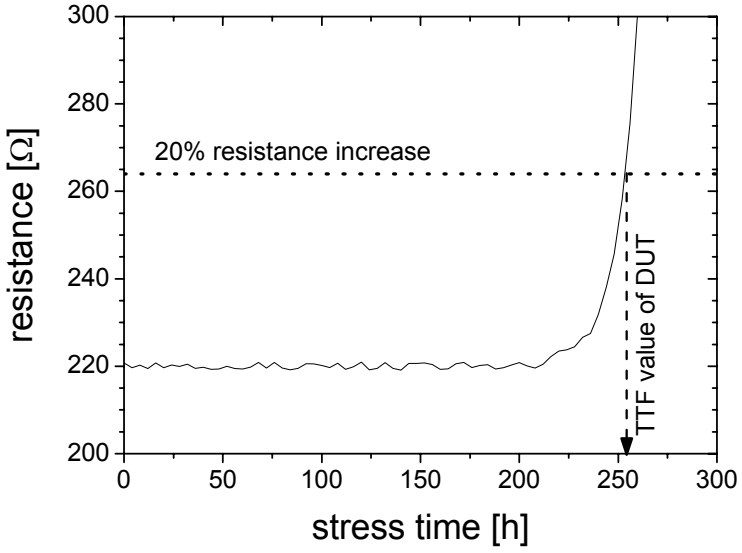


Fig. 26: Resistance shift during electromigration test

The median time to failure as a statistical value is determined by a log-normal distribution of the TTF of the devices under test according to equation [Hir96]:

$$MTTF = \exp\left(\frac{1}{n}\sum_{i=1}^{n}\ln\left(TTF(i)\right)\right) \tag{18}$$

The accordance of the model and the real TTF values can be evaluated best by drawing a failure distribution graph. In Fig. 27, three different test conditions with the linear fits are displayed. In this diagram, the cumulated percentage of failed samples is plotted as function of time to failure. Since the statistic is described by a log-normal law, the TTF is plotted logarithmically, and the percentage is plotted as the inverse (Z) of the cumulative error function. $Z = 0$ indicates the mean value of the distribution, $Z = +1$ or $Z = -1$ represent the value one standard deviation above or below the mean value, respectiveely. With that function, normal distributed distributions, which show S-type graphs in linear scale can be transformed into a linear appearance. There is a variety of distributions like Weibull, Laplace, Cauchy, exponential, or the logarithmic normal distribution. The standard normal distribution is applicable to processes which are influenced by a lot of parameters, where the influence of each parameter is not separable [Wik05]. In our case, the time to failure of metal lines was measured, which are influenced by all different fabrication processes therefore, the standard normal distribution is the best choice.

The activation energy is then determined by linear fitting of the logarithmic median time to failure (MTTF) values found for several testing temperatures at the same current densities, see Fig. 27. For extrapolation the linear fits have to be conducted such that the gradients of the linear fits of the different stress conditions are equal. It should be mentioned that for the determination of the activation energy, the line temperature deviates significantly from the storage stress temperature in some testing conditions due to self-heating of the lines, caused by the high stress current density.

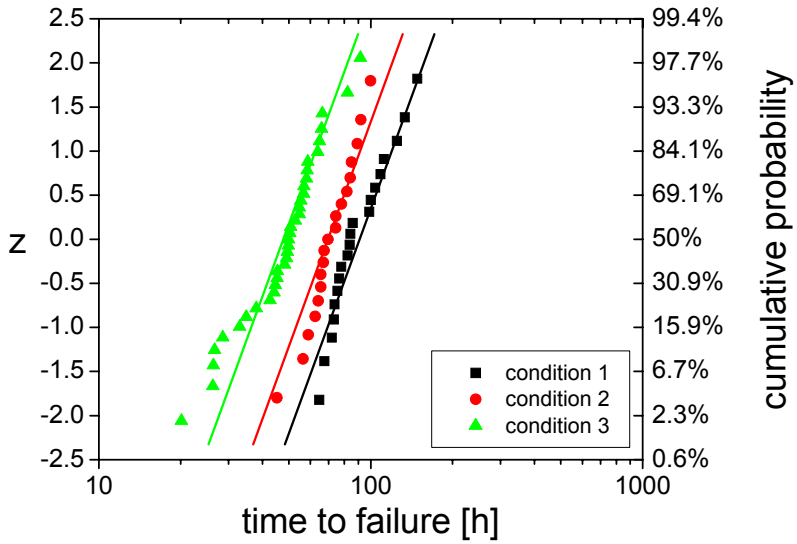


Fig. 27: Failure distribution of electromigration testing

The determination of the current density exponent is similar. Here, the stress tests are performed at different current densities at a fixed temperature and then the linear fitting of the MTTF values can be performed.

In practice, the TTF value not at high temperatures and current densities but at operating conditions is needed. Therefore, after the extraction of E_a and n out of the electromigration stress tests, the lifetime extraction at use conditions is performed. Estimates for the use conditions for different future technology nodes can be extracted from the ITRS [ITR05], see Chapter 2.1. With the following equation the found $MTTF_1$ value at temperature T_1 and with a current density j_1 can be transformed into use condition (index 2).

$$MTTF_1 = MTTF_2 \cdot \left(\frac{j_1}{j_2}\right)^{-n} \cdot e^{\left(\frac{E_A}{kT_1} - \frac{E_A}{kT_2}\right)} \tag{19}$$

This can also be graphically understood, see Fig. 28. As a last step failure probability has been taken into account since the MTTF value is the value when 50% of the samples already failed. Since in practice, the allowed failure rate has to be much lower, the practical TTF value is the intersection point of the straight line of the linear fit and the allowed failure rate, see Fig. 28. In our case, the allowed failure rate was set to Z = -5.3, which correlates to a failure probability of 5.8^{-8}. In productive stress tests, the set point for the failure probability is calculated out of the tested interconnect length compared to the product chip interconnect length and number, and of course to the requirements of the customers. For example, for automotive applications, a lower failure probability has to be reached than for cell phone chips.

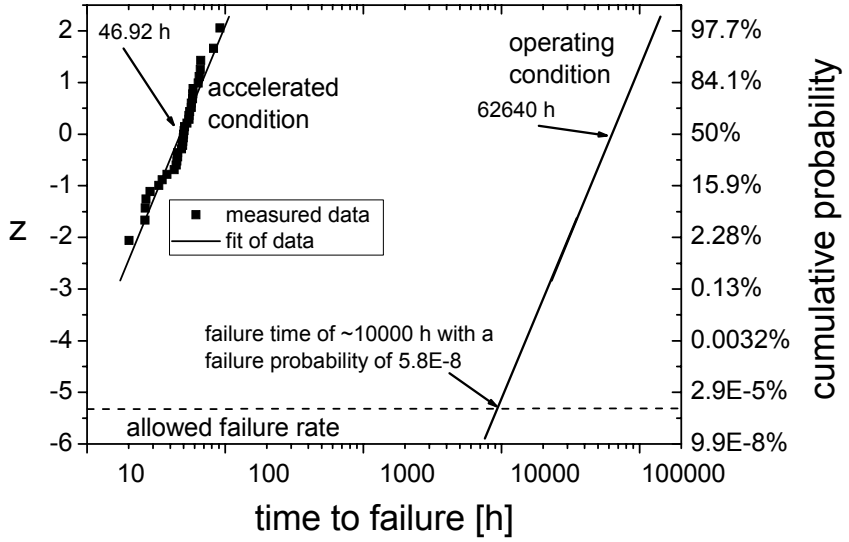


Fig. 28: TTF extraction from measured data

2.9.2 Leakage current and conduction mechanism through dielectrics

An ideal isolating dielectric would suppress any current through the material. In real dielectrics, current transport through the dielectric is possible depending on the material itself and the applied electric field. By means of the *IV*-characteristic, the conduction mechanism and the breakdown voltage can be examined.

Different mechanisms contribute to the leakage current like field emission or temperature dependent mechanisms like Schottky emission (Fig. 29a) and Frenkel-Poole mechanism (Fig. 29b) [Sze81]. Field emission and Schottky emission represent mechanisms that inject charges into the dielectric. They depend on the work function of the electrode material. In contrast to Schottky emission, the charge carrier transport of Frenkel-Poole mechanism is based on traps located in the dielectric. So, this mechanism describes properties of the dielectric itself. The trap density in the dielectric increases by the diffusion of Cu atoms into the dielectric, traps of etch damage or interfaces of dielectrics.

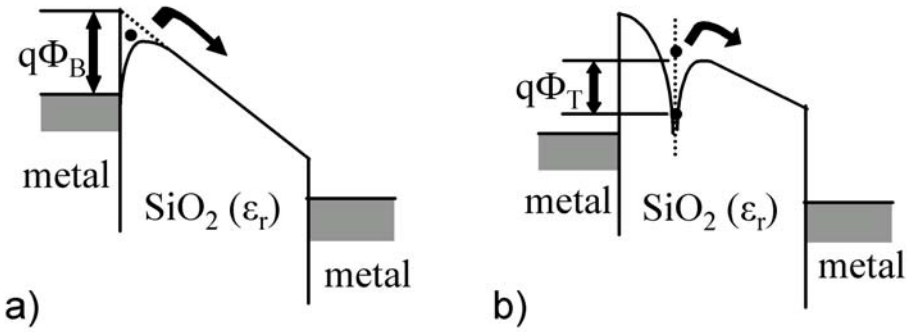


Fig. 29: Conduction mechanisms in dielectrics: a) Schottky emission (Φ_B – metal work function) and b) Frenkel-Poole mechanism (Φ_T – trap depth)

According to [Sze81], the conduction based on Schottky emission is given by:

$$J = A^* T^2 \exp\left[\frac{-q\left(\Phi_B - \sqrt{qE/4\pi\varepsilon_0\varepsilon_r}\right)}{k_B T}\right] \tag{20}$$

J denotes the current density, A^* the so-called effective Richardson constant, T the temperature, k_B the Boltzmann constant, Φ_B the work function of the metal, ε_0 the permittivity of vacuum and ε_r corresponds to the k-value of the dielectric. Transformation of the equation leads to a linear relationship of $\sqrt{E}$ as x-axis and $\ln\left(J/A^*T^2\right)$ as y-axis:

$$\ln\left(\frac{J}{A^*T^2}\right) = \frac{q\sqrt{\frac{q}{4\pi\varepsilon_o\varepsilon_r}}}{k_B T}\sqrt{E} - \frac{q\phi_B}{k_B T} \quad \Leftrightarrow \quad Y \approx A \cdot X + B \tag{21}$$

The effective k-value can then be calculated out of the gradient A of a linear fit of the IV-characteristic:

$$\varepsilon_r = \frac{1}{A} \cdot \frac{q}{4\pi\varepsilon_0 (k_B T)^2} \tag{22}$$

The corresponding relationship for Frenkel-Poole emission is:

$$J \propto E \exp\left[\frac{-q\left(\Phi_T - \sqrt{\frac{qE}{\pi\varepsilon_0\varepsilon_r}}\right)}{k_B T}\right] \tag{23}$$

The equation of the Frenkel-Poole mechanism can be transformed in a similar manner to a linear relationship of $\sqrt{E}$ as x-axis and $\ln(J/E)$ as y-axis, see Fig. 30. In this case Φ_T denotes the potential height of the traps in the dielectric.

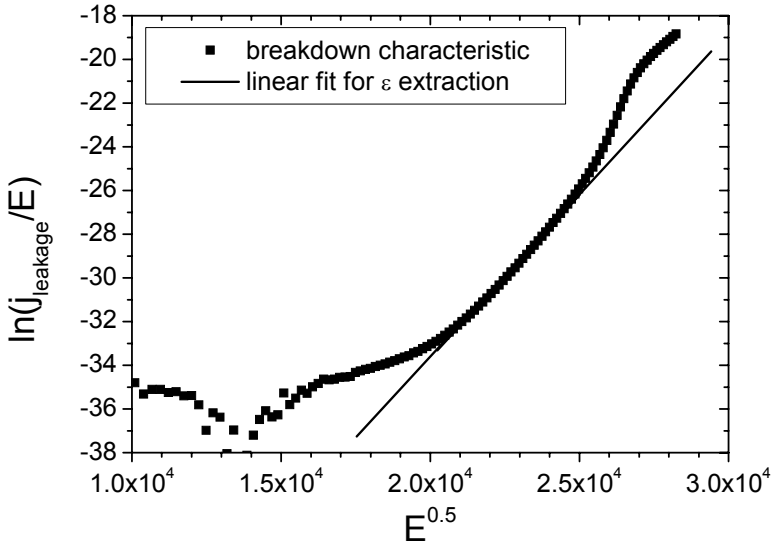


Fig. 30: Transformed JV-characteristic for Frenkel-Poole analysis

After the extraction of the *k*-value of Frenkel-Poole mechanism and Schottky emission, the conduction mechanism can be determined by comparing the obtained *k*-values with the real *k*-value of the structure. After Frenkel-Poole mechanism or Schottky emission have occurred, the leakage current at even higher fields is dominated by field emission before the dielectric breakdown (also called hard breakdown) occurs [Tra03].

Another conduction mechanism is surface conduction which occurs at dielectric surfaces or interfaces. This conduction mechanism is caused by surface states, dangling bonds, etch damage or foreign atoms. The mechanism increases the overall leakage current, has ohmic behavior and is strongly dependent on the surface area.

2.9.3 Dielectric breakdown of gases at micrometer spaces

Dielectric breakdown of gases means that a gas in a high electric field between two electrodes becomes a conductor. The theory of electrical breakdown is based on Townsend breakdown respectively avalanche discharge in gases. According to this well-known theory, an electric spark can occur only if free electrons accelerated by an electric field, gain enough energy between successive collisions with neutral gas atoms or molecules to ionize them. Ionization releases an additional electron which also accelerates, collides with atoms, and causes more ionization. The resulting avalanche leads to a spark. This behavior is represented by the familiar Paschen's law, which describes the dependency of the gas pressure *p* and the gap space on the breakdown voltage. In Fig. 31, Paschen curves for different gases are depicted. In the graph, the breakdown voltage versus the product of the pressure times the gap space is shown. It can be seen that the characteristic for all gases reaches a minimum for a specific *p·d* value. The minimum in this curve occurs at the condition where the electronic mean free path is just barely sufficient to allow electrons to gain the ionization energy [Hop02].

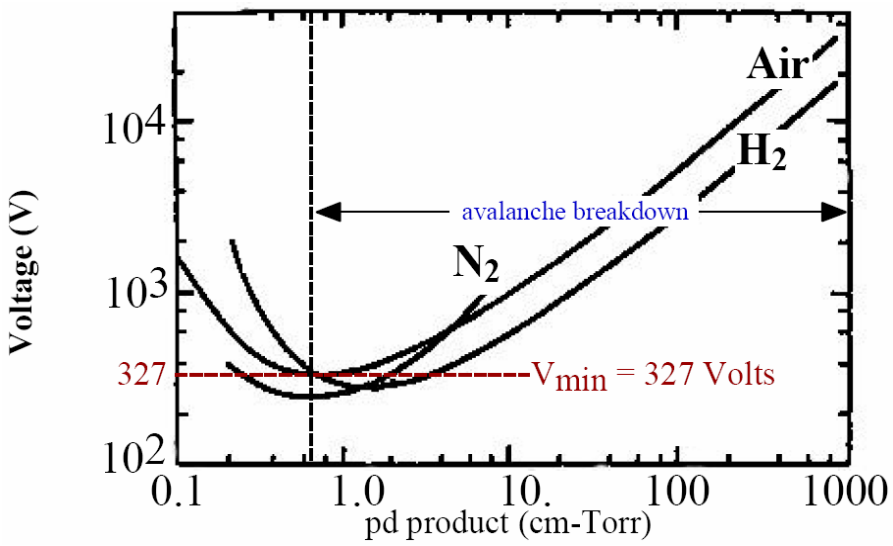


Fig. 31: Paschen curve of different gases [Jan92]

Paschen's law applies only to uniform field electrode gaps where the maximum electric field exists within the gap and is given by *V*/*d* and is uniform within the interelectrode space. The law essentially states that at higher pressures, the breakdown characteristics of

a gap are a function (generally not linear) of the product of the gas pressure p and the gap space d, usually written as $V = f(p \cdot d)$. This law is applicable to avalanche discharge, which holds true for a gap space between several 10µm to 10cm and pressures ranging from 10^{-3}mbar and 20bar [Oku97].

Unfortunately it was observed that Paschen's law is not applicable to narrow gap spaces [Boy55], [Dha00] like in the interconnect system. The major reason is that only Townsend discharge is taken into account in Paschen's law but at narrow spaces the mean free path of the atoms is in the range of the gap space and therefore no electron avalanche can be formed to generate a spark. For example for oxygen, the mean free path is 100nm at 550Torr [Wik04]. When sufficiently high electric fields at the surface of a conductor are applied, some of the conduction electrons in the metal lattice close to the surface are literally pulled out into the gap. This effect is called field emission. The electrons, now free, respond to the normal, applied field by accelerating rapidly toward the opposite, positive electrode. Even when the mean free path is in the range of the gap, so that the electrons can not gain sufficient kinetic energy to generate an avalanche electrostatic discharge (ESD) in the gas, other mechanisms such as localized heating can lead to a runaway process that results in a spark. At ambient pressure and normal temperature, in gaps less than a few microns, field emission coupled with other mechanisms is known to limit useable voltages to values well below those predicted by avalanche breakdown respectively Paschen's law. A modified Paschen curve for narrow gaps at room temperature and atmospheric pressure is depicted in Fig. 32 [Jop02].

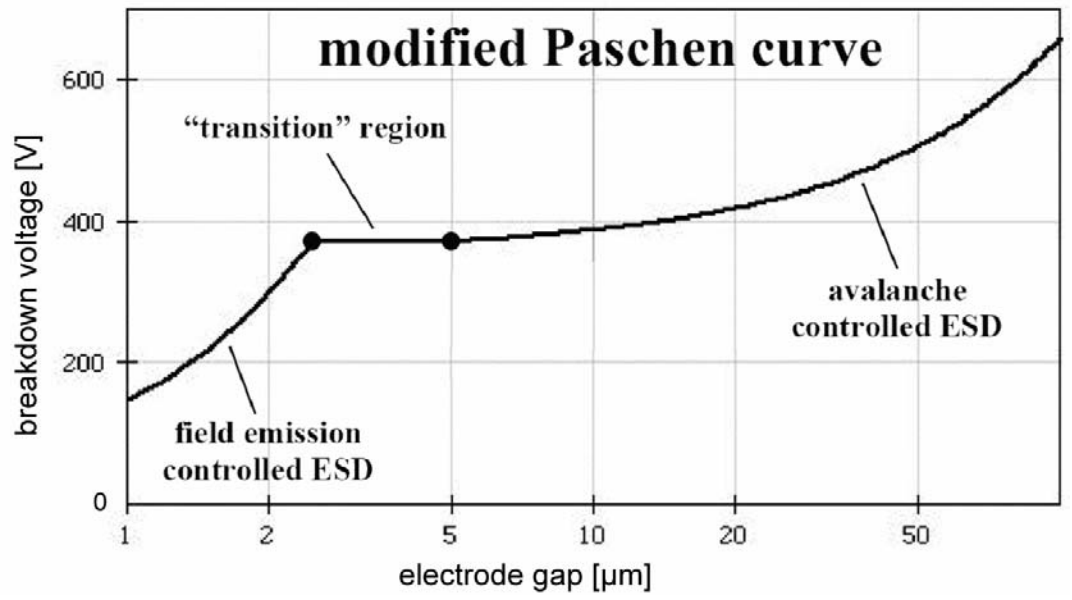


Fig. 32: Modified Paschen curve for narrow gaps [Jop02]

There are three different regions dependent on the electrostatic discharge mechanism. The first one is the avalanche controlled region, which can be described as mentioned by Paschen's law and is applicable to gap widths > 5µm. In the transition region, which is applicable to gap widths between 3 - 5µm, an insufficient number of electrons are generated for the avalanche phenomena [Dha00]. The region below 3µm gap width is the field emission controlled electrostatic discharge region, where the breakdown voltage depends on the work function of the electrode material. The work function is a material

constant and is the minimum energy needed to remove one electron from the Fermi level in a metal to a point at infinite distance away outside the surface. With the work function value of a metal the maximum breakdown field strength can be calculated [Dha00].

$$E_{\max} = \pi\ \varepsilon_0\ \frac{\Phi^2}{e} \qquad \Phi : \text{work function [eV]} \tag{24}$$

The maximum breakdown field strength E_{max} of 33.5MV/cm was calculated for copper, 30.5MV/cm for tantalum and 28.9MV/cm for aluminum [Wik04]. These high values can not be reached because local field enhancement due to electrode roughness and micro protrusions degrade the breakdown field strength to 1/10 down to 1/100 of the calculated values [Dha00]. For example for a gap width of 0.5µm breakdown voltages of 60V were measured, which correlates to a field strength of only 1.2MV/cm [Dha00]. When extrapolating the graph in Fig. 32 to 0.5µm, a breakdown voltage of ~120V can be seen.

2.10 Power dissipation and thermal crosstalk of interconnects

Another important aspect of the interconnect system is the power dissipation of the interconnect system. This power dissipation leads to higher power consumption and to increased heating of the chip. Both C_{wire} and R_{wire} contribute to the power dissipation P_{diss} as shown in the following formula:

$$P_{diss} = C_{wire} V_{dd}^{\ 2} 2\pi f + R_{wire} I^2 \tag{25}$$

Since R_{wire}, the operating voltage V_{dd} and the frequency f is more or less fixed due to the design, the only way to reduce the power dissipation technologically is by reducing the wire capacitance C_{wire}. The only way to reduce this capacitance is by lowering the k-value of the interconnect system, since the geometry is design-related. The second term of equation 25 describes simple Joule heating which is dependent on the wire resistance and the square of the current [Sar03]. This term is independent of C_{wire}. The resistance in modern chips was already minimized by introducing copper as interconnect material.

The power dissipation which leads to a higher temperature of the metal lines, called self-heating, is in particular important concerning electromigration reliability, since electromigration is strongly temperature dependent, see Chapter 2.9.1. The self-heating of the metal lines also depends on heat conduction of the line material and the surrounding material. To reduce self-heating it is important to conduct the heat effectively to the substrate of the chip and via the substrate to the package, respectively to the heat sink. The heat flux through matter is described by the following equation:

$$I = \lambda \cdot A \frac{\mathrm{d}T}{\mathrm{d}x} \tag{26}$$

I is the heat flux, λ is the thermal conductivity of the material, A is the heat conducting surface, dT is the temperature difference and dx is the distance. Since the geometry is fixed by the design, the heat flux strongly depends on λ. For example, the introduction of a low-k material as a gap fill material for metal 1 raises the DC thermal impedance by about 10%. The thermal impedance under short current pulse increases even more and the critical failure current density decreases by 10 up to 30% [Ban96]. This is undesirable

since the current density in modern chip design is increasing to extreme high values up to 15MA/cm² by 2016.

This effect of self-heating is becoming more severe with aggressive interconnect scaling by the increasing current density, more metal levels and the introduction of low-*k* materials. However, due to the poor thermal properties of interlayer dielectrics (ILD), Joule heating of the interconnect wires is fast emerging as an urgent issue [Cha02].

3 CVD O_3/TEOS process

3.1 Properties of the CVD O_3/TEOS deposition

SiO_2 chemical vapor deposition (CVD) from tetraethyloxysilane (TEOS) has usually been performed by plasma excitation or high temperatures. In the plasma activated process, the activation energy for decomposing the TEOS molecule is applied via the plasma. In the high temperature case, the TEOS molecule is decomposed at temperatures above 600°C which guarantees very good conformity but is not practicable for back end processing [Sha95], due to degradation of the metal at such high temperatures.

The CVD O_3/TEOS (so-called "O_3/TEOS" process) approach takes advantage of an ozone activated deposition: the high reactivity of ozone helps to reduce the deposition temperature to about 400°C which is compatible with BEOL requirements, and at the same time, the good gap fill properties of the high-temperature process are maintained. The chemical reaction is shown below:

$$8O_3 + Si(OC_2H_5)_4 \overset{400°C}{\Rightarrow} ...intermediates... \overset{400°C}{\Rightarrow} SiO_2 + 8CO_2 + 10H_2O \qquad (27)$$

The O_3/TEOS process is carried out on a P5000 CVD standard production tool of Applied Materials for 6" and the capability of 8" wafers. The tool is equipped with a non-standard more powerful ozone generator of Sorbios for ozone concentrations of up to 12wt% (200g/m³ at 20°C, 1bar) with high flow rates [Sor04]. The maximum possible ozone concentration is limited to around 14wt% because at this point, the ozone production and recombination is in equilibrium. Further, the wafer temperature, the gas flows of the process gases, the distance of the showerhead to the wafer can be set to change the process characteristic. In Fig. 33, you can see an overview of the used P5000 CVD tool.
The machine consists of two cassette handlers for 25 wafers each, a storage elevator with space for 8 wafers, which is inside the loadlock chamber together with the wafer handler and three process chambers. Chamber A is used for TEOS-based SiO_2 depositions with ozone or plasma activation and plasma pretreatments. Chamber B is used for silane-based depositions like Si_3N_4 or SiO_2 and chamber D is for hydrogen plasma treatments. The chuck of chamber A is heated constantly at 400°C with lamps mounted on the bottom side of the chuck. The chuck of chamber B and D can be heated as well, with a resistive heated chuck.

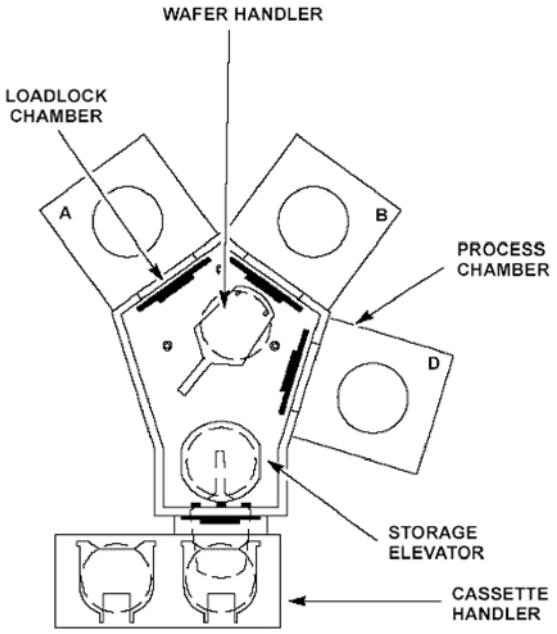


Fig. 33: P5000 CVD tool for O_3/TEOS deposition

The thermally and O_3 activated O_3/TEOS deposition can be tuned to be highly conformal or to occur selectively only on particular types of substrate materials. The conformal process can be used for trench filling [Sha95] in DRAM applications. This process can also be tuned to achieve a very unique deposition behavior: a selective deposition of SiO_2 from the gas phase.

3.2 Selective O_3/TEOS process

Selective O_3/TEOS deposition means that high-quality SiO_2-TEOS films grow only on certain types of underlayers such as silicon, aluminum, or silane-based PECVD oxide. These TEOS films are smooth and have a low wet etch rate indicating a dense morphology. On other substrate types, however, no film grows during the same deposition run, or the deposition has a low rate and results in very rough and porous films with high wet etch rates. Such underlayers are silicon nitride, thermal or PECVD TEOS oxide.

This particular behavior occurs when the pressure in the process chamber is raised to slightly below atmospheric pressure, typically 600Torr (SACVD). What is even more important is a high ratio of ozone gas flow to TEOS flow. There are several ways to achieve the latter condition [Pam01]. First, the TEOS flow can be decreased which leads to a decreased deposition rate and to a slower wafer throughput. Second, the O_3 concentration can be increased using a high power ozone generator as mentioned above. The third possibility is to reduce the O_2 flow through the ozonator which however may conflict with the requirement of high pressure. Fig. 34 shows two examples of the O_3/TEOS process with different process conditions.

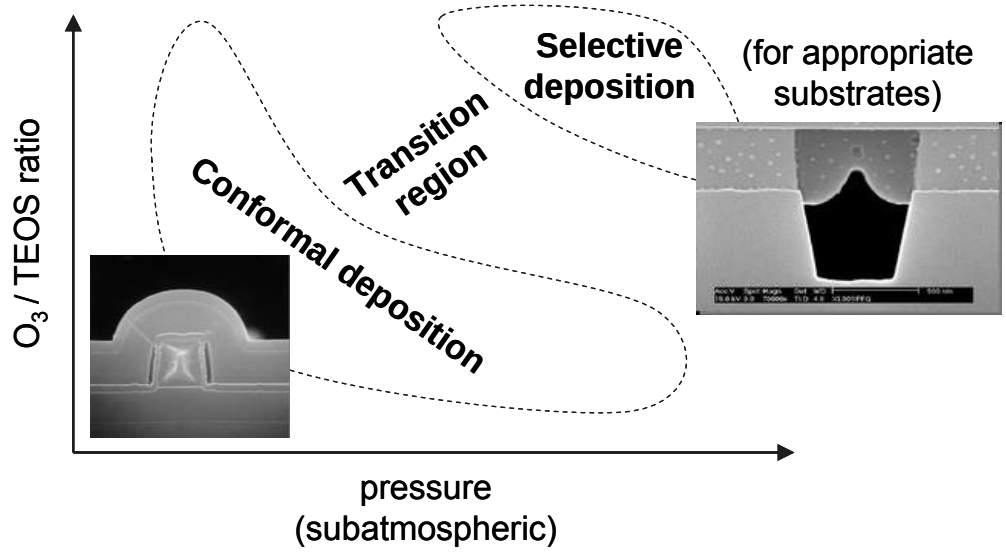


Fig. 34: Deposition properties versus pressure and O_3 to TEOS ratio [Pam01]

As can be seen on the left SEM image, the deposition at low pressure and low O_3 to TEOS ratio is very conformal across the etched aluminum metal line. When depositing O_3/TEOS at high pressure and high ozone concentrations and different materials at the surface, very high selectivity can be achieved, see right SEM image.

Table 3 describes the influence of all process parameters on the selectivity and the deposition rate [Gra98].

Table 3: Influence of process parameters on deposition rate and selectivity

Process parameter:		**Deposition rate:**	**Selectivity:**
Pressure	higher	lower	higher
TEOS flow	lower	lower	higher
Ozone flow	higher	lower	higher
Space wafer-showerhead	higher	lower	higher
Temperature	lower	lower	higher

The most important parameters as explained before are the ozone concentration at high flow rates and the pressure. The TEOS flow is set to the minimum controllable value of 230sccm while the O_2/O_3 flow is set to 7000sccm at 12.5wt% O_3 concentration, which is the maximum the ozone generator can produce. This very high flow of 7000sccm is necessary to deposit at high pressure without long dwell periods of the gases in the chamber. Long dwell periods would lead to a lower ozone cocentration due to increased recombination. Further on, this high flow leads to a high ratio of 30:1 of O_2/O_3:TEOS. The temperature is set constant to 400°C because this is the standard temperature for TEOS depositions and is not intended to be changed.

Another important aspect of a selective process is to make sure to start right at the beginning of the deposition with a high O_3 concentration. If the O_3 content is low at the beginning, this would destroy the selectivity due to a thin deposition of unselective O_3/TEOS layer at the beginning of the process. This unselective O_3/TEOS layer covers the whole wafer and consequently serves as a seed layer, leading to good O_3/TEOS growth independent of the substrate. For these reasons, the TEOS flow is settled first together with O_2 / He flow and then the deposition is started by switching off the O_2 / He and turning on the O_3 flow. The oxygen flow through the ozone generator is kept constant during the whole process to reach steady state conditions and it is switched via a three-way valve from an exhaust to the process chamber.

Further on, a cleaning process is performed after every deposition because the chamber walls and the showerhead itself are covered with deposited SiO_2. This reconditioning of the chamber is also necessary to always start with the same process conditions.

The O_3/TEOS layer is known for moisture uptake [Gra98]. For this reason and for electrical characterization of the *k*-value, wafers with plate capacitors were produced. The wafer was covered with a Ti/TiN layer, a 490nm thick O_3/TEOS SiO_2 layer and on top, aluminum pads were sputter deposited through a shadow mask. The capacitance was then measured and the *k*-value was calculated with the plate capacitor formula. The capacitance is very sensitive to moisture due to the very high $k = 80$ of water. The Ti/TiN layer is necessary to achieve a good bottom electrode for the capacitor, preventing a space charge region being formed in silicon during measurements. On both wafers, 20 structures were measured. Then, they were stored and measured every week to monitor changes due the moisture uptake. The results of these measurements can be seen in Fig. 35.

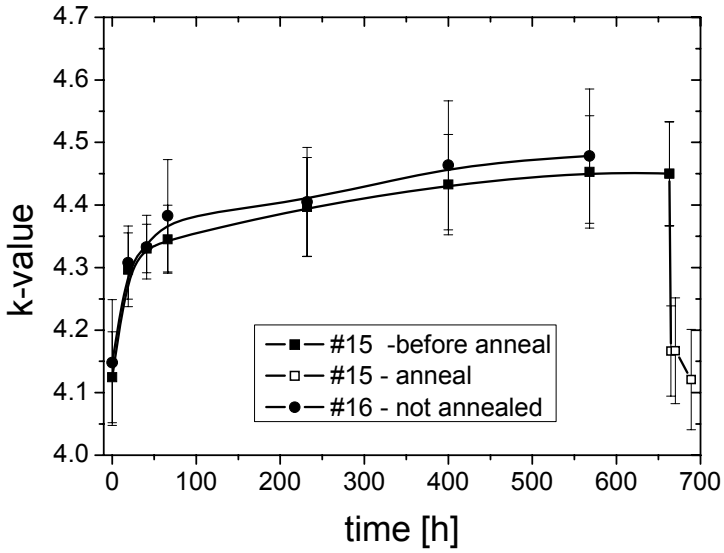


Fig. 35: *k*-value of O_3-TEOS versus storage time

The *k*-value of O_3/TEOS is 4.12 right after deposition which is relatively low compared to standard PECVD TEOS SiO_2 with $k = 4.28$ (measured with the same technique). After storing the wafers at room temperature for 19h after deposition, $k = 4.30$ was observed, and after approx. four weeks (663h), a *k*-value of 4.45 could be seen. After these 4 weeks, wafer #15 was annealed for 5min at 400°C in nitrogen atmosphere. As can be seen, the *k*-value decreases to 4.15 which is very close to the starting value. With a simple

proportional calculation, the increase of the *k*-value from 4.12 to 4.45 could be figured out to correlate to a moisture uptake of ~0.5wt%. Further experiments with PECVD TEOS capping layers on top of the O_3/TEOS layers were conducted which showed very stable *k*-values during 4 weeks storage time. To proove the moisture uptake physically, Fourier transform infrared spectroscopy (FT-IR) was carried out on a wafer with higher *k* and a reference wafer with the usual value. No difference of the spectra could be found. Obviously, the total amount of desorbed water is less than the detection limit.

For determining the stoichiometry of the O_3/TEOS film, Rutherford backscattering spectrometry (RBS) and elastic recoil detection (ERD) analysis were carried out on a blanket wafer. The ERD method is used to determine the hydrogen content, RBS is used for nitrogen and oxygen content. As a result, the stoichiometry is as follows: $Si_{1.00}O_{2.07}H_{0.15}$; the nitrogen content was below the detection limit of 0.1. As can be seen, the film is not perfectly stoichiometric due to hydrogen and too much oxygen content.

3.3 Theories about the selectivity of the O_3/TEOS deposition

3.3.1 Selectivity caused by hydrophilicity

There are various ideas to explain the behavior of selectivity. Fujino et al. suggested that the hydrophilicity of the surface of the substrate material causes the selectivity [Fuj91]. They performed experiments of O_3/TEOS deposition on thermal oxide and bare silicon with different ozone concentrations ranging from 0.5% to 5% and a constant process temperature of 400°C. No difference between the deposition on silicon and SiO_2 occurred for ozone concentrations below 2%. When increasing the ozone concentration to ~5%, the deposition rate on silicon is 27% higher than on thermal SiO_2 and moreover the wet etch rate of the film was 3.2 times lower (see Table 4). The wet etch rate of SiO_2 films is a measure of the film quality; the higher the wet etch rate, the lower the film quality [Fuj91]. On silicon, the deposition rate and the film quality increases with higher ozone concentrations because the decomposition of the TEOS molecule and the SiO_2 composition is improved. Further on, the surface roughness on thermal oxide is with 10 - 100nm very high and the film can even become porous (see Chapter 3.4).

Table 4: Relation between deposition rates, wet etch rates and contact angle

Base materials	**Silicon**	**Thermal SiO_2**
Water contact angle	50°	10°
Wet etch rate	85 nm/min	275 nm/min
Deposition rate	92 nm/min	126 nm/min

According to Fujino, the lower deposition rate on thermal oxide is attributed to hydrophilic property of thermal oxide and hydrophobic property of TEOS and silicon. Lower contact angles mean to be more hydrophilic, see Table 4. As water is a by-product during O_3/TEOS deposition, more water will be produced at higher ozone concentrations. Because of the hydrophilicity of the thermal oxide, more water will be adsorbed than on the hydrophobic silicon surface. The water adsorption at the surface of the thermal oxide

leads to a lower probability of adsorption of the hydrophobic TEOS molecule or TEOS reaction intermediates, resulting in a lower deposition rate and water incorporation in the growing film. On the other hand, a hydrophobic surface, such as bare silicon results in a high-quality deposition since the water is repelled from the surface [Fuj91].

3.3.2 Selectivity caused by electronegativity

The results obtained by Kwok et al. contradict this simple "hydro-affinity" model because there are discrepancies when expanding this model to other materials [Kwo94]. Kwok et al. suggest that the selectivity can be attributed to the presence of electronegative species such as fluorine on the surface of the PECVD oxide underlayer. Experiments were performed on three different substrates: Thermal SiO_2, silicon, TEOS-based PECVD SiO_2, silane-based PECVD SiO_2 and TEOS-based PECVD SiO_2 with N_2O as second precursor instead of standard used oxygen. Experiments with three different O_3 to TEOS ratios (O_3:TEOS: 12.6:1, 5.2:1, 3.7:1) were performed. Furthermore, three different plasma treatments with argon, nitrogen and helium were performed to investigate the effects of plasma treatments on the selectivity.

As a result, good, smooth films were found on silicon, silane-based PECVD SiO_2 and TEOS-based PECVD SiO_2 with N_2O independent of the O_3 to TEOS ratio. On TEOS-based PECVD SiO_2 and on thermal SiO_2 a very rough surface structure and high wet etch rates were found when depositing with the highest O_3 to TEOS ratio.

To find out more about the composition, which might chemically explain the selectivity of the different materials, SIMS, XPS, RBS and NRA analyses were performed. SIMS (secondary ion mass spectroscopy) analysis allows a very sensitive element composition analysis in the ppm range. RBS (Rutherford backscattering spectrometry) analysis is to determine the element concentration. With XPS (X-Ray photoelectron spectroscopy) analysis, the binding energy can be figured out, which is known for all element bindings and therefore the binding itself can be detected. The inspection depth is typically 10nm. The NRA (nuclear reaction analysis) method is a nuclear method in materials science to obtain concentration vs. depth distributions for certain target chemical elements in a solid thin film.

The results obtained by RBS, NRA and SIMS indicate that the bulk composition of the various oxides has no effect on the surface dependence. This phenomenon and the fact that all observed materials except for silicon are SiO_2-based materials lead to the conclusion that not the bulk material is important for the selectivity, but the surface plays the most important role [Kwo94]. In addition to carbon, oxygen and silicon, XPS revealed the presence of fluorine and nitrogen on selected oxide surfaces. These XPS results clearly suggest that the surface dependence effects observed on PECVD TEOS-based SiO_2 are caused by the presence of fluorine.

Out of these data, Kwok et al. propose the following model [Kwo94]: In the gas phase, O_3 thermally decomposes to oxygen radicals and O_2 which react with TEOS to form gas phase precursors adsorbing on the substrate surface and reacting to form SiO_2. Due to the abundance of free oxygen radicals the gas mixture is assumed to be electronegative. The higher the O_3-concentration, the higher the concentration of oxygen radicals and hence the more electronegative the gas mixture becomes. If the substrate surface is electronegative as well, the adsorption on the substrate will be suppressed to result in a decreased deposition rate. The presence of fluorine in this case makes the substrate more

electronegative, which then results in the suppression of oxide film growth and in higher selectivity. Silicon substrates covered with e.g. thermal oxide and nitride are very electronegative (Si-N-bond 4.94eV, Si-O_2-bond 5.34eV), thus explaining the decreased deposition rate on these layers.

Table 5: Effect of bonding type (XPS) on selectivity [Kwo94]

Substrate	Bonding type	Surface sensitivity
Si	C-C/C-H	No
Steam SiO_2	Si-O	Yes
PECVD SiO_2 TEOS-based	Si-F	Yes
PECVD SiO_2 Silane-based	C-N	No
PECVD SiO_2 TEOS/N2O	C-N	No
PECVD Si_3N_4	Si-N/C-F	Yes
PECVD SiO_2 TEOS + Ar plasma	C-C/C-H	No
PECVD SiO_2 TEOS + N2 plasma	C-N	No

It is postulated that an opposite polarity between the surface of the oxide underlayer and the O_3/TEOS precursors will lead to a favorable reaction and a high quality film, whereas a similar polarity will result in severe surface dependence effects and poor film quality. As a consequence, the substrate dependence seen with the PECVD TEOS-based SiO_2 underlayer at high ozone concentration is proposed to be due to repulsion between the fluorine species on the surface being very electronegative and the electronegative gas phase mixture of the O_3/TEOS reaction.

3.3.3 Selectivity caused by hydrogen saturation on surface

Graßl finally claimed that the surface sensitivity is caused by a hydrolysis reaction of the OH-groups of the TEOS precursors adsorbed on the surface with a hydrogen-terminated surface. Graßl performed a lot of experiments during his thesis with ozone activated SiO_2 deposition. He used a variety of different organic precursors deposited on patterned wafers with standard aluminum metal lines. The selectivity of the process was intended to be used for planarization of the metal lines by filling just the line spaces. The lines were fabricated on PECVD silane-based SiO_2 and capped by a thin TiN layer. He observed a good growth of the O_3/TEOS deposition on PECVD silane-based SiO_2 and only very slow growth on TiN.

Furthermore, Graßl mentioned that the electronegativity model is not suitable due to two orders of magnitude lower surface energies compared to the high free energy of ozone decomposition [Gra98].

$$2O_3 \Rightarrow 3O_2 + 2.87eV \tag{28}$$

His model of the O_3/TEOS deposition consists of four parts: gas phase reaction, adsorption, surface diffusion, and desorption or film growth. The maximum possible deposition rate is limited by the precursor flow rate and the chosen O_3:TEOS ratio. In the gas phase, the TEOS molecules will be transformed by the atomic oxygen of the ozone

decomposition into very reactive decomposition products, like silicic acid - $Si(OH)_4$. When the ozone concentration is high, more TEOS molecules will be transformed into silicic acid. These decomposition products will be transported to the substrate surface by convection transporting the energy for deposition to the substrate surface. The film growth itself is a bare oxidizing chemical reaction.

The selectivity of the process is explained by the density of hydroxyl groups on the substrate surface adsorbing the silicic acids which diffuse across the surface until they reach - according to their tetraedal structure - three bonds via hydrogen bonds. Then a hydrolysis and oxidizing reaction takes place to obtain SiO_2. If only a few or no hydrogen groups are present at the surface, no binding of the silicic acid is possible.

Especially silane-based PECVD oxides are rich in hydrogen and offer a lot of docking sites for the TEOS precursors, metals such as TiN offer none [Gra98]. Graßl also mentioned that the behavior of the O_3/TEOS deposition on patterned wafers can be different than on blanket wafers. For example, when depositing O_3/TEOS on a blanket TiN surface, a good-quality, smooth deposition can be observed, but when depositing on a structured wafer with TiN and silane-based SiO_2 areas, no or only little deposition can be observed on TiN. This behavior can be explained by the formation of a mutual network of the precursor decomposition products on the wafer.

3.4 Selectivity experiments on blanked wafers

In order to assess the usability of different underlayer materials for air gap fabrication with the selective O_3/TEOS process, experiments on unstructured, blanked wafers were carried out. Due to the fact that this work was carried out within the European NanoCMOS project, various project partners (ST Microelectronics, Philips Research Leuven) contributed basic planar layers with materials that are not available at Infineon Technologies in Perlach. All these 18 wafers were then coated with the selective O_3/TEOS layer. The wafers were cleaved after deposition and SEM inspection was performed to verify potential selectivity. In general for air gap fabrication we need two different materials on the wafer: One on which the O_3/TEOS film grows with high deposition rate called “seed layer” and another one with low deposition rate, called “base layer”. The exact process steps will be explained in detail in Chapter 4.

All SEM images were rendered on a LEO 1560 scanning electron microscope. The LEO 1560 SEM provides high resolution down to 3nm. For good SEM analysis, the wafers were cleaved by a diamond scribe, decorated with 1% HF solution and then sputtered with a thin metal layer. The decoration with HF is necessary to intensify the contrast due to topology generation because of the different HF wet etch rates of the different materials. Even different PECVD silicon oxides i.e. TEOS-based and silane-based, show different wet etch rates and can then be discerned in SEM inspection. The sputtered metal layer, usually 10nm Ti, is necessary to prevent charge effects due to the electron beam of the SEM.

3.4.1 Dense growth of selective O_3/TEOS

Materials, for which O_3/TEOS deposition shows no selectivity, usually exhibit a compact and dense structure of the deposited layer as can be seen in SEM analysis (Fig. 36). On the

other hand, on materials with a suppressed O_3/TEOS deposition, a very porous, coral- or Swiss cheese like structure can be found in SEM analysis (Fig. 38, 39).

As can be seen in Fig. 36, a very dense and smooth film of O_3/TEOS covers the 40nm thin Ti layer. Beneath the Ti, a thick SiO_2 layer is deposited to isolate the Ti layer from the substrate. Such a good film growth can also be seen on silane-based SiO_2, silicon, tantalum, TaN, TiN, O_3/TEOS, CoWP, NiMoP and tungsten. The CoWP, NiMoP films were deposited on a copper underlayer because they can only be selectively deposited on metallic layers (see Chapter 4.3.2). Additionally, the ability of such layers to protect copper from oxidation during ozone exposure could be proven.

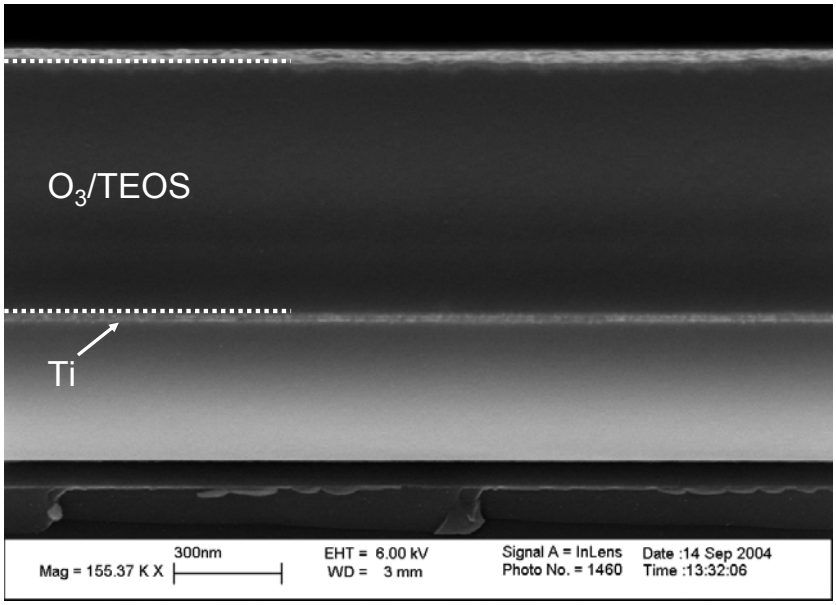


Fig. 36: O_3/TEOS SiO_2 on Ti (no Swiss cheese effect)

It is an important observation that unprotected Cu is not compatible with direct exposure to the O_3/TEOS environment because Cu is heavily oxidized during the deposition leading even to delamination of the Cu layers. Therefore, more experiments have been done with thin Ta/TaN or Ti/TiN layers on copper. Apparently, these materials are not sufficiently dense to prevent Cu oxidation during ozone exposure.

On the wafers with a SiCN or a standard TEOS-based SiO_2 underlayer, only a few voids are visible close to the interface of the two layers (Fig. 37). SiCN and standard TEOS-based SiO_2 films are both deposited by PECVD. The surface roughness of the O_3/TEOS film itself is only marginally higher, compared to Fig. 36.

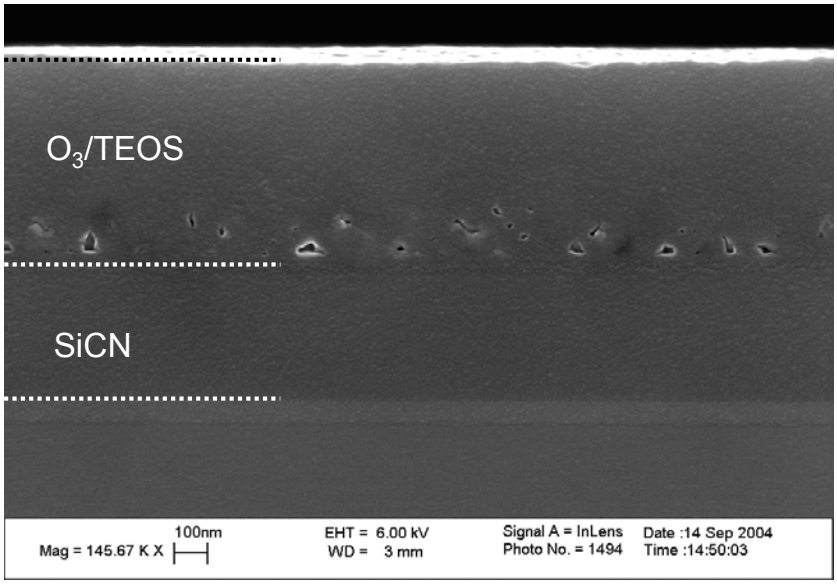


Fig. 37: O_3/TEOS SiO_2 on SiCN or standard TEOS-based SiO_2

3.4.2 Swiss cheese effect of selective O_3/TEOS growth

In Fig. 38, the deposition of O_3/TEOS on nitrogen doped TEOS-based SiO_2 can be seen. Nitrogen doped TEOS-based SiO_2 is especially developed for higher selective growth of O_3/TEOS. It is a SiO_2-based film with a slight incorporation of nitrogen. The process is based on the standard TEOS SiO_2 deposition with an addition of N_2. The composition of such a film was evaluated by RBS (Rutherford backscattering spectrometry), ERD (elastic recoil detection) and XPS (X-ray photoelectron spectroscopy). The oxygen content was measured by RBS, hydrogen by ERD and carbon, nitrogen by XPS analysis. The composition based on silicon is: $Si_{1.00}O_{1.90}H_{0.27}C_{0.045}N_{0.06}$. On the account of only a small amount of nitrogen, the *k*-value is 4.26, which is almost the same as of standard TEOS-based SiO_2 ($k = 4.28$).

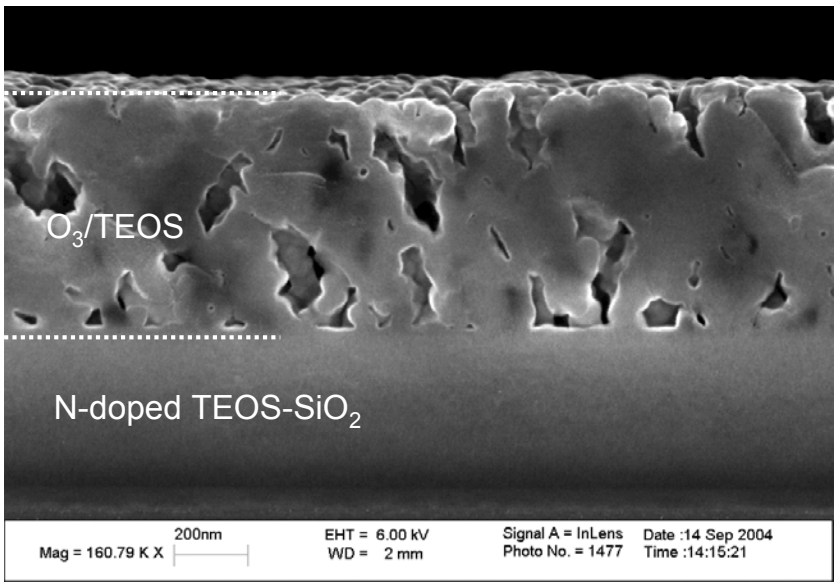


Fig. 38: O_3/TEOS SiO_2 on nitrogen doped TEOS-based SiO_2

In Fig. 38, it is visible that a porous film deposition, called Swiss cheese effect, occurs causing an increased surface roughness. This kind of behavior is comparable when depositing on a-SiC (amorphous SiC).

The strongest Swiss cheese effect can be obtained when depositing O_3/TEOS on Si_3N_4, SiOC or fluorine doped TEOS-based SiO_2, see Fig. 39. The surface becomes very rough with thickness variations of more than ±20% of the nominal deposited film thickness for the same deposition time. The nominal film thickness on such underlayers is comparable to those with good film growth, but the density due to the strong Swiss cheese effect is very low. The density according to SEM analysis is about half to a quarter compared to a dense film. This strong Swiss cheese effect explains the very high wet etch rate of O_3/TEOS on thermal oxide mentioned in Chapter 3.3.1. Due to the porous structure of this SiO_2, the surface for wet etching is extremely high in contrast to dense films.

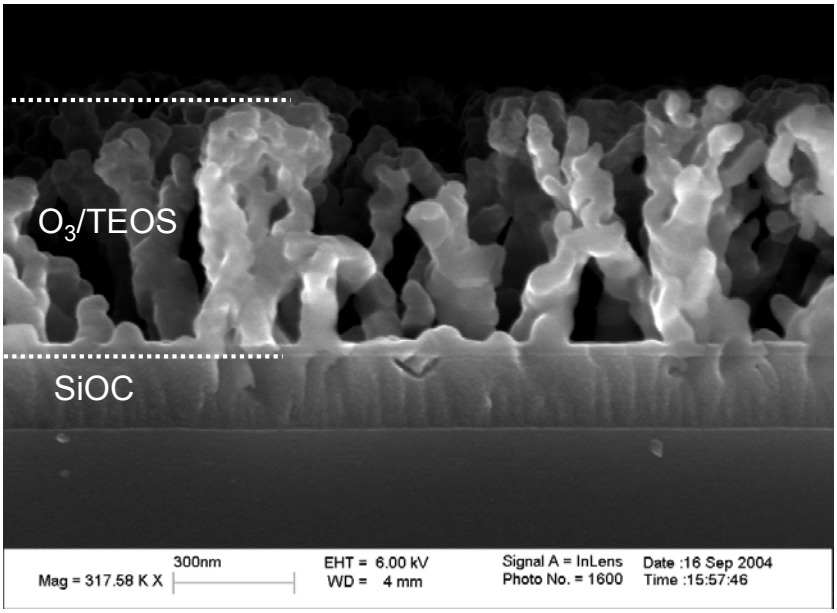


Fig. 39: O_3/TEOS SiO_2 on silicon oxy carbide (strong Swiss cheese effect)

The Swiss cheese effect was already observed before, by Fujino [Fuj91] and by Z. Gabric [private discussion]. Fujino wrote of films with very rough surfaces, which may be due to the Swiss cheese effect. Z. Gabric optimized the O_3/TEOS process for very selective growth and has seen this kind of behavior especially on Si_3N_4 surfaces. Obviously, only a few nucleation spots on the wafer surface allow O_3/TEOS, to grow and therefore lead to the Swiss cheese effect. These nucleation spots can be more than 200nm apart from each other and lead to 50 - 100nm thick SiO_2 pillars, see Fig. 39.

Further on, it is important to mention that all these experiments were only conducted on blanket wafers and that the selectivity effects may be different on patterned wafers. Especially the selectivity will be affected by the affinity of O_3/TEOS to the different materials on the wafer.

3.4.3 Summary of selective O_3/TEOS deposition

Table 6 gives an overview of all tested materials with electronegativities [Uni99] and contact angles. The contact angle was measured manually with a contact angle measurement tool. The measurement is conducted by putting a droplet of water with a pipette on the inspection surface. Then, the droplet is inspected from the side via an eyepiece and, finally, the contact angle is measured via a scale in the eyepiece.

Table 6: Overview of Swiss cheese effect on different materials

Material	**Magnitude of Swiss cheese effect after O_3-TEOS**	**Contact angle**	**Electronegativity (Pauling) [Uni99]**
SiO_2 – TEOS-based	medium	25°	2.82
SiO_2 – Silane-based	none	27°	2.82
SiO_2 – O_3/TEOS-based	none		2.82
SiO_2 – TEOS-based, N doped	strong		2.82
SiO_2:F – TEOS-based, F doped	strong		2.82
Si_3N_4	strong	28°	2.49
NiMoP	none		~1.9
CoWP	none	72°	~1.9
Cu	none	86°	1.90
Si	none	70°	1.90
a-SiC	strong	67°	2.20
SiCN	medium	71°	
SiOC	strong	40°	
Ta	none		1.50
TaN	none		2.14
Ti	none	58°	1.54
TiN	none	48° - 60°	2.16
W	none		2.36

For some material combinations like CoWP and silicon nitride, the selectivity theory of Fujino et al. [Fuj91] that the selectivity is dependent on the contact angle seems correct. On the other hand, only a marginal difference in the contact angle of silicon nitride and silane-based SiO_2 results in a severe selectivity difference, see Chapter 3.3.1. When examining a-SiC and silane-based SiO_2, the practical results are even contrary to the theory.

We did not experimentally verify the theory of Kwok et al. about the electronegativity [Kwo94], since we did not investigate the existing chemical surface bonding types. The numbers stated in Table 6 are calculated values for bulk electronegativity and are therefore most probably not valid for proof of the theory as different bonding types may be available on the surface with different electronegativities. For example, for the different

SiO_2s in Table 6, the surface electronegativity would be very important since the bulk value is equal and therefore cannot be a measure for different selectivity.

The theory of the hydrogen content on the surface of Graßl [Gra98] was tested by exposing Si_3N_4 and a-SiC layers to hydrogen plasma to influence the amount of hydrogen groups on the surface. After 2min of hydrogen plasma exposure of Si_3N_4 the growth of O_3/TEOS with strong Swiss cheese effect changed to a dense growth behavior. In contrast no behavioral change is observed when performing the same experiments on a-SiC.

As a conclusion, all theories about the selectivity of O_3/TEOS obviously do not explain the behavior in general; they can only explain the phenomenon for special material selections. In addition, it has to be mentioned that it was not the intention of this work to evaluate or discover a new theory of the selectivity of the O_3/TEOS deposition.

4 Fabricated air gap structures

4.1 Test chip structures

The used test chip for fabrication of air gaps with the selective O_3/TEOS process is a BEOL (Back End Of Line) test chip for copper metallization with aluminum pads. The test chip size is equal to the die size with 17.3mm times 18.2mm. A 6" wafer comprises a number of 34 dies, see appendix A. The test chip is without active devices and comprises additional lithography layers for air gap fabrication with additional lithography. For comparison purposes, versions of all structures with air gaps and without (the so-called "full" structures) are available on the test chip. This design allows direct correlation of all electrical and physical data to the presence or absence of air gaps all fabricated with the same processes on the same wafer. The test chip is designed for two metal layers with air gaps and comprises eight lithography masks, for details see Appendix A.

4.1.1 Mask set of the test chip

The first mask (MB) is for the first damascene copper lines M1, see Table 7. The damascene masks for the first and second metal layer are designed with respect to CMP and therefore include dummy fill structures.

Table 7: Lithography masks of test test chip G0826

Lithography mask	Abbreviation	Alignment
Metal 1 (M1)	MB	-
Air gap 1	CI	MB
Via (M1 to M2)	RA	MB
Metal 2 (M2)	PB	RA
Air gap 2	HA	PB
Pad window	PV	MB
Substrate contact	TV	MB
Aluminum pad	TD	PV

The mask CI defines the air gaps between the metal lines M1 and is therefore aligned on MB. This alignment is very critical, as a misalignment would lead to a damage of the metal lines during air gap trench etch. The dual damascene vias between M1 and M2 are defined by the RA mask and aligned to the MB layer. The PB mask is aligned to the via level and determines the second metal layer M2. The air gaps between the second metal level are defined by the HA mask, which is aligned to PB (M2). The CI and HA masks are only used for the air gap approach with lithography, see Chapter 4.2. The last three masks are uncritical and define the pad window (PV), substrate contact (TV) and the aluminum

pads (TD). The pad windows are a type of large via to contact the 2nd metal level with a footprint of 80µm by 80µm. The substrate contact is also a type of via with the same size as the pad window, but it contacts the substrate. The last mask, the TD mask defines the 100µm by 100µm aluminum pads for electrical contact.

4.1.2 Comb structures

One of the most important test structures are the comb structures. The comb or finger structures have a footprint of 4mm² to achieve sufficiently high capacitances for measurements with a *LCR*-meter. These comb structures serve for capacitance measurements in the 100kHz range and not for high frequencies due to the 2mm long combs which are afflicted with a significant series resistance. The combs are available with different distances between the Cu lines ranging from 0.45µm to 1.1µm. The serpentine length ranges from 4.208m for the 0.45µm structure to 2.496m for the 1.1µm structure. In Fig. 40, a microscope image of a two-metal layer comb structure with adjacent air gaps, 1µm line space and M2 perpendicular to M1, is depicted. To ensure a uniform shape of all air gaps and consequently the same air gap height, the air gap width is fixed in the design to 0.50µm. The air gaps are visible in the microscope as dark lines between the light-colored reflecting metal lines.

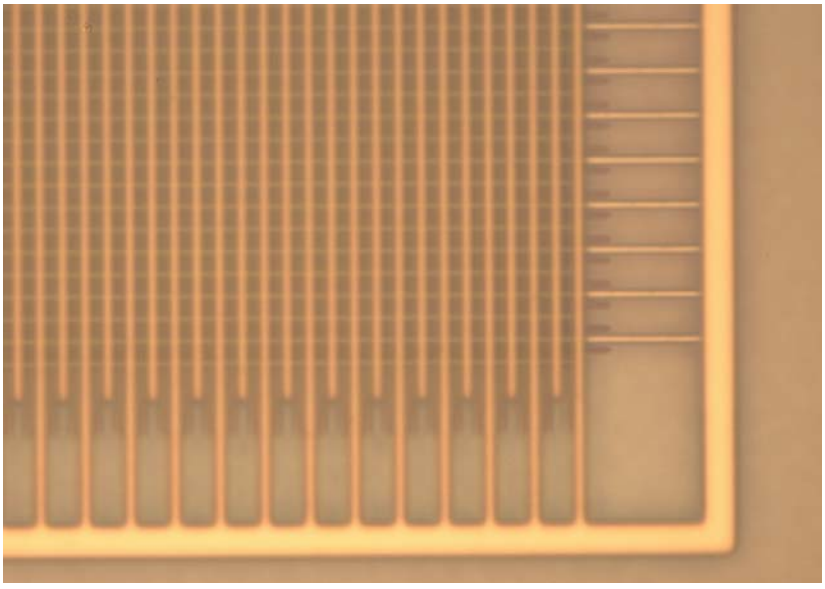


Fig. 40: Comb structures of two metal layers with adjacent air gaps

The comb structures are available with the second metal layer (M2) perpendicular or parallel to the first metal layer (M1). Further on, the air gaps are continuous over the whole comb length or segmented with a 0.5µm wide SiO_2 pillar every 10µm distance. Around the comb structures is a guard ring for shielding. Additionally, a contact to the substrate is located close to the comb structure to ensure a defined potential of the substrate during measurements. As explained later in detail, the substrate is coated with a metallic layer to avoid a space charge region inside the semiconducting substrate. For further details, like the serpentine length and the variety of comb structures, see Appendix B.

4.1.3 Structure for SEM analysis

For process control, a structure for easy SEM analysis, called SEM bar, is included on the lower left corner of the test chip, see Appendix A. The SEM bar includes an array of 20 lines of all different line and space dimensions and space types like full, air gaps, segmented air gaps or double air gaps (Fig. 41). The line length and width of the SEM bar is 2 mm. This long dimension makes it easier to cleave the wafer at the right spot. Since every variant is only repeated 20 times, this structure makes it very comfortable to analyze all structures with only one SEM preparation. Additionally, all lines are connected on each end to reduce charging effects during SEM analysis. On the right side of each structure variant, a label is placed for identification when microscope inspection is performed.

Fig. 41: Microscope image of SEM bar

4.1.4 Reliability structures

Reliability structures are intended for resistance, resistivity measurements and for reliability testing. These structures are available with and without air gaps and different line spaces ranging from 0.45µm to 1.1µm, for details see Appendix B. With these structures, the effect of air gaps can directly be correlated to reliability stability and effects on the resistance can be investigated. The structure itself is a 1mm-long line embedded in an array of lines consisting of 40 parallel metal lines (Fig. 42). The adjacent lines are necessary to avoid lithography effects like proximity effects and over development during the photoresist development, see Chapter 4.2.3.

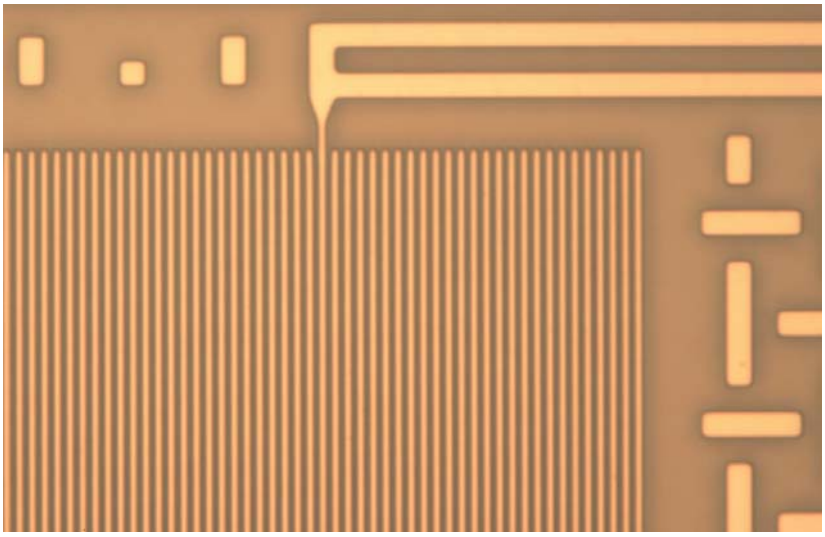


Fig. 42: 1mm long structures for reliability analysis

The 1mm-long line is connected to two pads on each end to allow four point measurements. One pad on each side is used as a force pad for test current application and the other two pads are used as sense pads for voltage sensing. This measurement method allows error-free resistance measurements of the 1mm long line, as the contact resistances and the voltage drop in the feed lines are excluded. Further, the line is smoothly tapered in the transition region between the wide and narrow part of the test structure. This design minimizes current crowding effects and sharp temperature gradients due to higher self-heating of the narrow line in contrast to the wide line. Without the tapered line, the lines would fail at the transition region during electromigration testing and therefore this spot would falsify the electromigration results [Ull00].

4.1.5 Crosstalk structures

With the so-called crosstalk structure, the capacitive or thermal coupling between two parallel metal lines can be measured. The crosstalk structures are available with different line spaces and as full or air gap structures. The structure consists of two 3.62mm-long parallel metal lines which are connected to four pads each, see Fig. 43. The active line is called aggressor and the sense line is called victim.

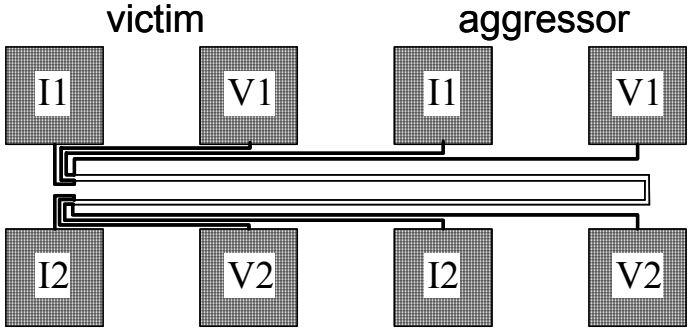


Fig. 43: Crosstalk structures on the test chip

Both lines are connected to two pads on every side for current feed (I1, I2) and voltage sense (V1, V2). Thermal coupling measurements are done by driving very high currents through the aggressor line and sensing the resistance increase of the victim and aggressor line. By means of the resistance increase, the temperature of the line can be calculated [Tip94]. For electrical crosstalk measurements, a high frequency is applied to the aggressor line and sensed for example by an oscilloscope at the sense line.

4.1.6 Additional test structures

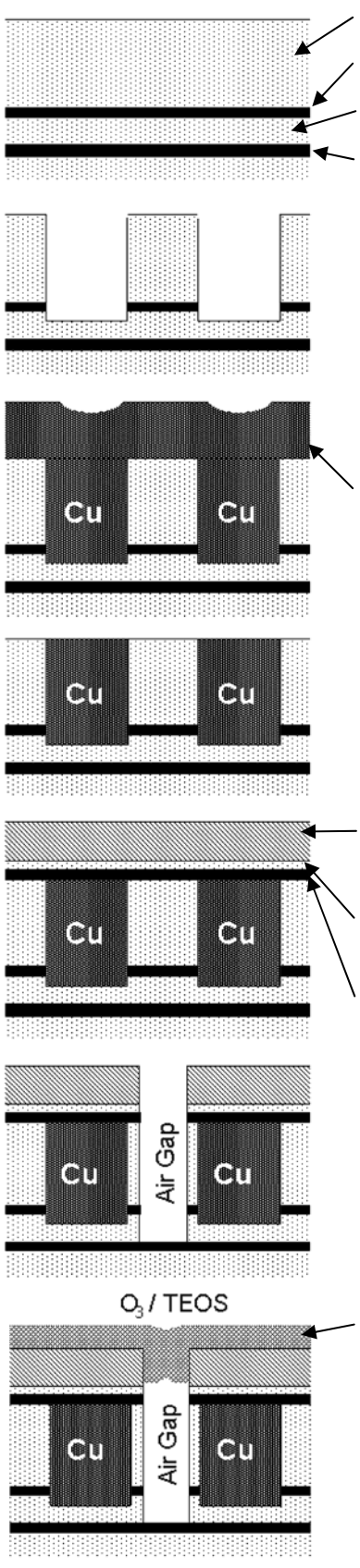
Moreover, there are additional structures like Kelvin crosses, via chains with different contact numbers, alignment marks, plate capacitors from the first metal layer to the substrate, long meander structures and Van-der-Pauw structures on the test chip.

Other structures used in this work are the via chains und the long meander test structures. Via chains consist of many short metal lines in the first and second metal level which are connected by vias. The via chains are available with different contact numbers ranging from 20 to 20000 contacts and different spaces between the air gaps to the metal lines. The long meander structures with a footprint of 1mm² are like the reliability structures for resistance and resistivity measurements and are available with different line spaces and as full or air gap design. Both structures can be measured by the four point method.

4.2 Air gaps by additional lithography

4.2.1 Processing scheme of air gaps by lithography

The key process is the selective deposition of O_3/TEOS [Gab03] as described in Chapter 3. First of all, a dielectric stack for the copper damascene lines was deposited and the trenches for the metal lines were fabricated (Fig. 44-1, 2). Then, the copper for the damascene lines of 0.5µm width was deposited in a matrix of modified TEOS and chemically mechanically polished (Fig. 44-2, 3). Si_3N_4 was inserted as etch stop and capping layer (Fig. 44-5). Si_3N_4 and modified TEOS prevent the deposition of O_3/TEOS. Modified TEOS is a TEOS-based SiO_2 with a slight incorporation of nitrogen featuring a *k*-value of 4.2. A stack of modified TEOS for air gap extension above the metal lines and silane-based oxide seed layer was deposited on top, providing a basis for excellent growth of O_3/TEOS (Fig. 44-5). The air gaps were then defined by lithography and the air gap trenches were etched between the Cu lines (Fig. 44-6). The depth of the air gap was either defined by an optional buried Si_3N_4 etch stop layer or by a timed etch. The design and the exposure parameters of this lithography step were optimized to leave a thin layer of at least 40nm on the sidewalls of the metal lines after etching. Although this results in a less efficient capacitance reduction, the spacer is necessary to prevent copper oxidation during the O_3/TEOS deposition and to maintain the selectivity of the O_3/TEOS process. After proper cleaning of the air gap trenches from etch residuals with EKC265, a production cleaning solution for removing polymers [EKC06] and a HF-dip in a 0.5% HF DI-water solution, the air gap trenches were finally closed off by the selective O_3/TEOS deposition (Fig. 44-7). To obtain selective growth, the O_3/TEOS deposition was performed at high pressure and ozone concentration [Gab03]. In order to ensure a uniform shape of all air gaps, the air gap width is fixed to 380nm for all line spaces.



1. Modified TEOS SiO_2 - (no O_3/TEOS growth)
   Si_3N_4 etch stop layer for Line trench etch (50nm)
   Modified TEOS SiO_2 for air gap extension beneath
   Si_3N_4 etch stop layer for the Air gap trench etch (50nm)

2. Lithography to define the Cu line structures
   Metal line trench etch, 500nm wide
   Wet post etch cleaning

3. Standard Cu damascene technology:
   PVD deposition of TaN/Ta barrier (not depicted) and Cu seed layer – thickening of the copper with electro chemical deposition (ECD) to fill the line trenches

4. Chemical mechanical polishing (CMP) to remove excessive Cu
   2nd CMP to remove the TaN/Ta barrier

5. Silane-based SiO_2 as seed layer (good O_3/TEOS growth)
   Modified TEOS SiO_2 for air gap extension above metal lines (no O_3/TEOS growth)
   Capping layer of Si_3N_4 (50nm)

6. Lithography to define the location of the air gaps
   Air gap trench etch, 380nm wide
   Proper post etch cleaning with EKC265 and 1% HF DI-water solution

7. Closure of the air gap trench by selective deposition of O_3/TEOS SiO_2
   Deposition of 300nm silane-based SiO_2
   Finally dielectric CMP for planarization

Fig. 44: Schematic process flow for fabrication of air gaps using selective O_3/TEOS deposition

The extension of the air gaps above and beneath the metal lines is not mandatory, but leads to an additional capacitance reduction. Three additional layers are necessary for the air gap extension: the Si_3N_4 etch stop layer for the air gaps and the modified TEOS SiO_2 layers beneath and above the metal lines.

The air gaps were fabricated with a standard 0.35µm technology. The stack for the fabrication started with a 44/200nm Ti/TiN layer on top of silicon. This layer is necessary to prevent space charge effects in the semiconductor during capacitance measurements. Then, a 700nm standard TEOS SiO_2 is deposited followed by the actual air gap stack as described above: 50nm Si_3N_4 as air gap etch stop layer, 250nm modified TEOS SiO_2, 50 nm Si_3N_4 etch stop layer for the copper lines, 500nm modified TEOS SiO_2, 50nm Si_3N_4 capping layer, 200nm modified TEOS SiO_2, 200nm silane-based SiO_2 and 500nm O_3/TEOS SiO_2. On top of that, another 300nm silane-based SiO_2 is deposited either before dielectric CMP or after dielectric CMP. The advantage of deposition before CMP is a reduced risk of opening up air gaps.

4.2.2 Preparation and SEM inspection of air gaps by lithography

Hundreds of SEM images were taken for detailed visual inspection of the process and the fabricated structures. A big advantage was that SEM analysis was directly available, which allowed a very fast and detailed feedback. This was especially valuable for process variations influencing the selectivity of the selective O_3/TEOS deposition. Further on, our SEM was equipped with an EDX detector, which allows measurements of the local chemical composition.

A detailed SEM cross-sectional image is depicted in Fig. 45 showing fabricated air gaps embedded in damascene copper metal lines. To enhance the image contrast, the sample was decorated with an HF-dip. Thus the interfaces of the different layers could be visualized. For illustration, the used dielectric materials, like Si_3N_4 (nitride), seed layer, base layer and O_3/TEOS layer, were colorized in the SEM image.

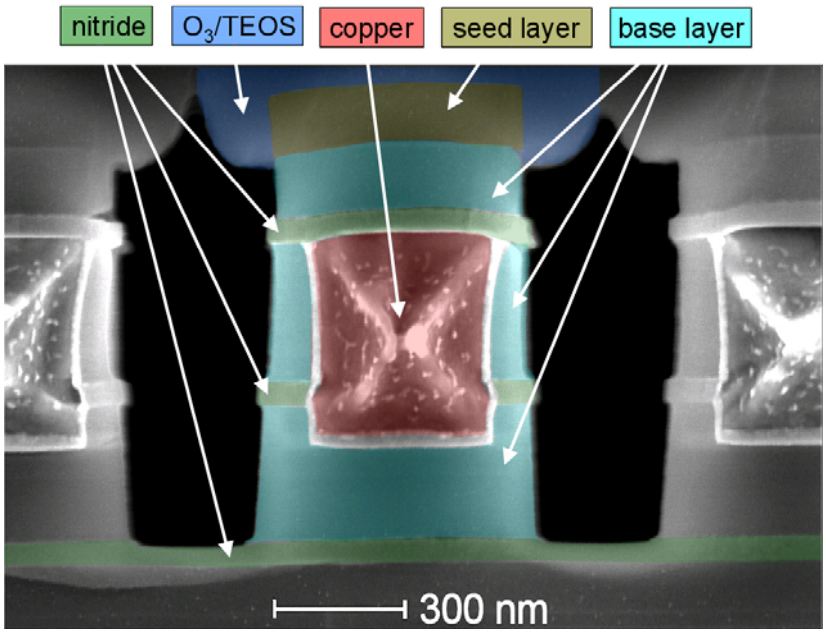


Fig. 45: SEM micrograph of an air gap formed between Cu lines

As can be seen, the selectivity of the O_3/TEOS process is very high; no film growth can be seen on the sidewalls of the air gap trenches. Further on, the tip of the air gap is relatively flat, which improves chemical mechanical polishing.

For 3D visualization of the perpendicular comb structures with air gaps, a sample edge was cleaved out of a wafer. Because the cleaved edge did not look smooth and a lot of particles were visible, the edge was milled by a focused ion beam. The ion milling was performed with argon ions in a FIB tool. An overview of the sample is depicted in Fig. 46.

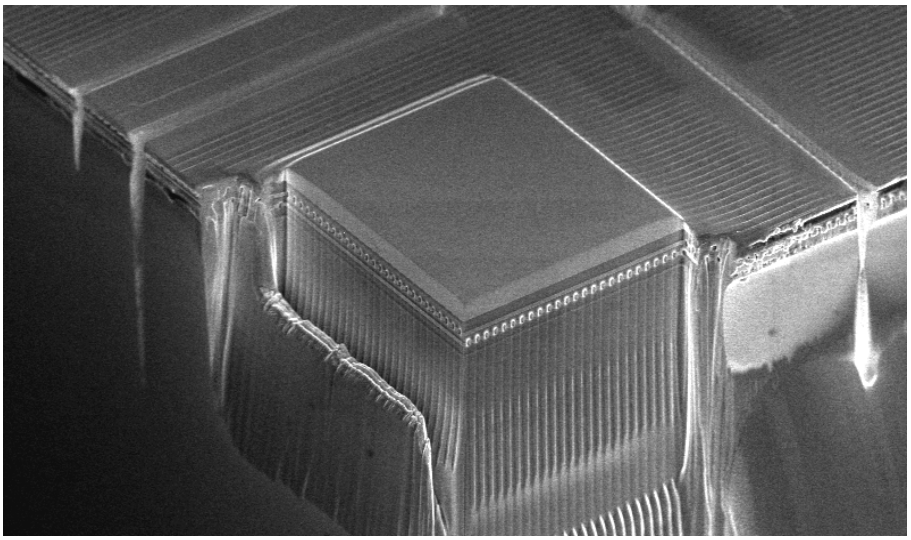


Fig. 46: Overview of cleaved sample after FIB milling

This technique was given preference to polishing to prevent the air gaps from filling with residuals. The disadvantage of ion milling is that it leads to a curtaining effect of the dense copper and the weak air gaps. The curtaining effect can be explained by the higher mechanical resistance of copper compared to air gaps for the argon ions and can be reduced by depositing a thick tungsten layer on top. Another effect of the FIB preparation observed while preparing the first sample was a massive charge up of the metal lines resulting in dielectric breakdown and decay of the structure. Therefore, deep trenches were milled at a distance from the edge and filled with tungsten to shunt the metal lines to the substrate, see right side of Fig. 46. The deposition of tungsten can also be conducted by our FIB machine.

The SEM cross-sectional images in Fig. 47 and 48 show two perpendicular layers of line comb structures with air gaps.

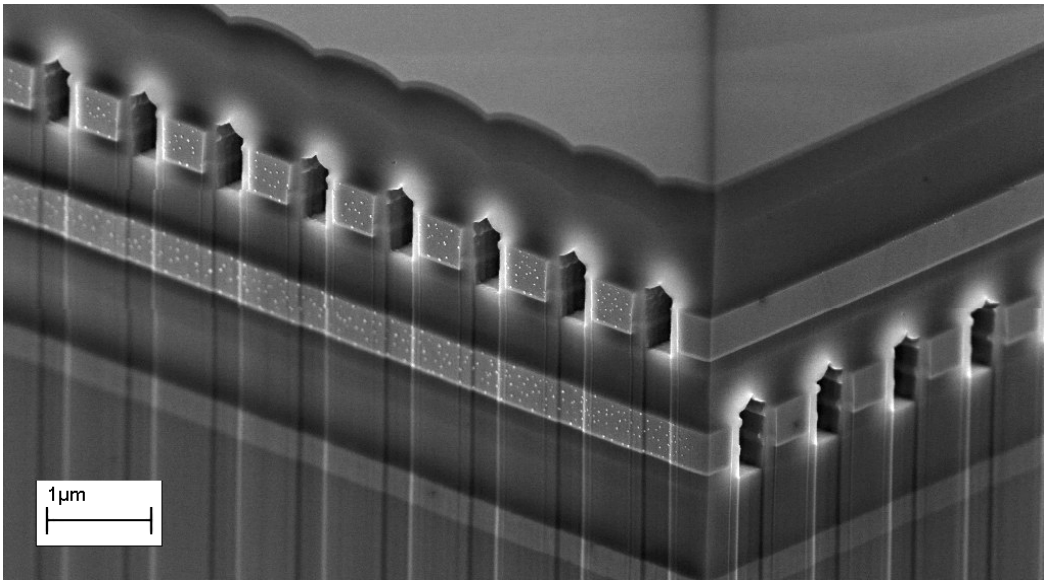


Fig. 47: SEM cross-sectional micrograph of two metal layers with air gaps

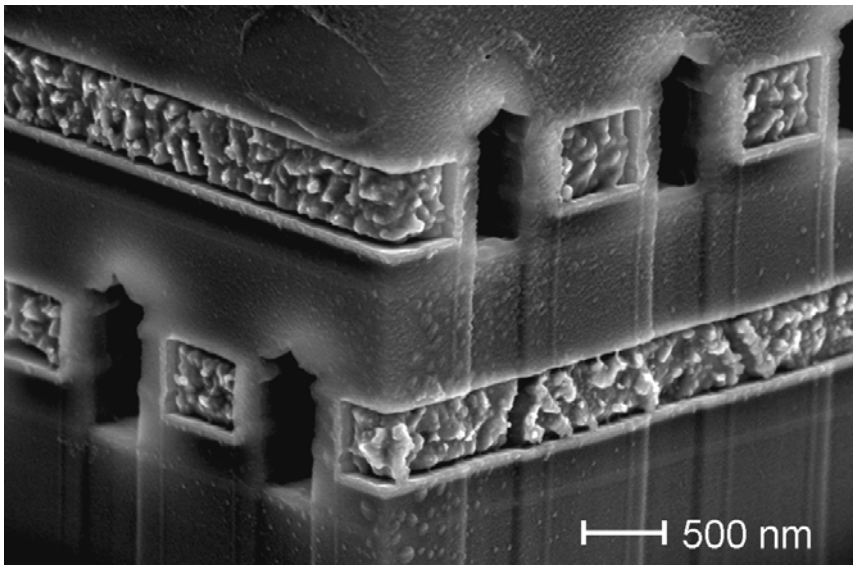


Fig. 48: Detailed SEM image of two metal layers with air gaps

All samples were deposited with 10nm Ti after FIB preparation to avoid charge up effects during SEM inspection. The particular appearance of the copper in the sample of Fig. 48 comes from the decoration with 1% diluted HF solution. The sample shown in Fig. 47 was not decorated with HF solution. The FIB milling of copper leads to a damage of the copper structure and is therefore etched by the HF solution. The argon ion intrusion depends strongly on the crystal direction of the copper grains. The stronger intruded and more damaged copper grains, are then easily etched by the HF solution and thus decorated the copper grains. This theory is supported by the fact that this effect is only visible after argon FIB milling and not during standard SEM inspection.

4.2.3 Process challenges

There are some critical processes implied in this processing scheme. The first one is the possibility of opening up the air gap tips during chemical mechanical polishing. This problem can be overcome by reducing the air gap extension above the copper lines. The O_3/TEOS deposition for air gap closure is generally clearly better than the non-conformal PECVD (Chapter 2.7.3) deposition for air gap closure, which leads to extremely long elongated tips. Unfortunately, CMP processing may still be problematic. In Fig. 49, it can be seen that a 100nm thin SiO_2 bridge separates the air gaps from the ambience which provides a sufficient safety margin for further processing.

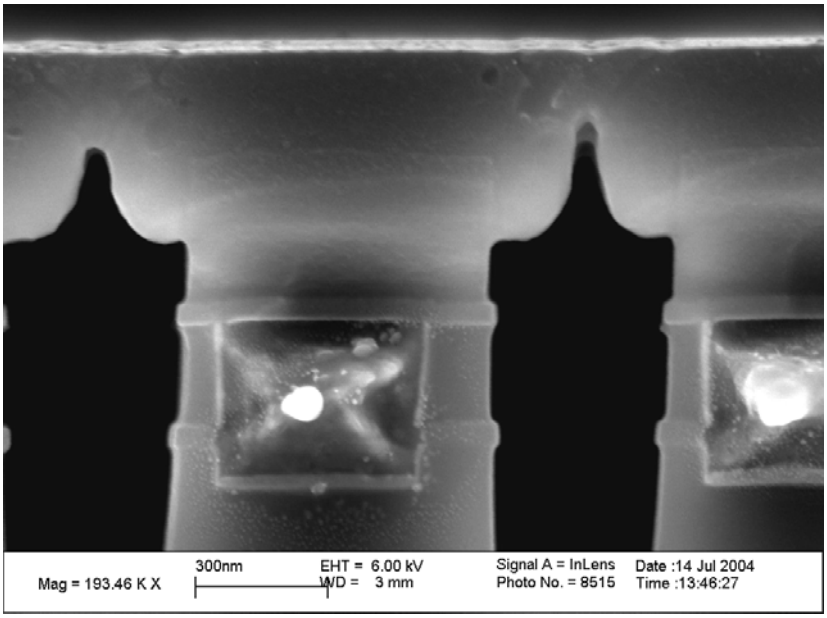


Fig. 49: SEM cross-section after CMP

Further on, the O_3/TEOS layer above the air gaps is quite weak and shows small voids. For improvement, the O_3/TEOS deposition can be reduced and a silane-based SiO_2 layer above the O_3/TEOS layer can be deposited before CMP.

Another very challenging process is the selectivity of the O_3/TEOS deposition. In production, only very few selective processes like silicidation or metal capping layers have been used so far because of complicated chemistry influencing selectivity. The selectivity is very critical against etch residuals like polymers or metallic residuals. These residuals can be removed by the EKC265 wet cleaning solution and then the surface is reconditioned by a 10 - 30s HF-dip in 1% HF DI-water solution. Unfortunately, the EKC265 cleaning solution is very aggressive to copper, too. For this reason one has to exercise care, to cover all copper surfaces, especially due to the very high etch rate of EKC265 against copper. Additionally, three other cleaning solutions were tested, which are compatible with copper, but unfortunately did not show good selectivity results. In Fig. 50, an image with improper residual removal is depicted, leading to O_3/TEOS deposition on the side walls.

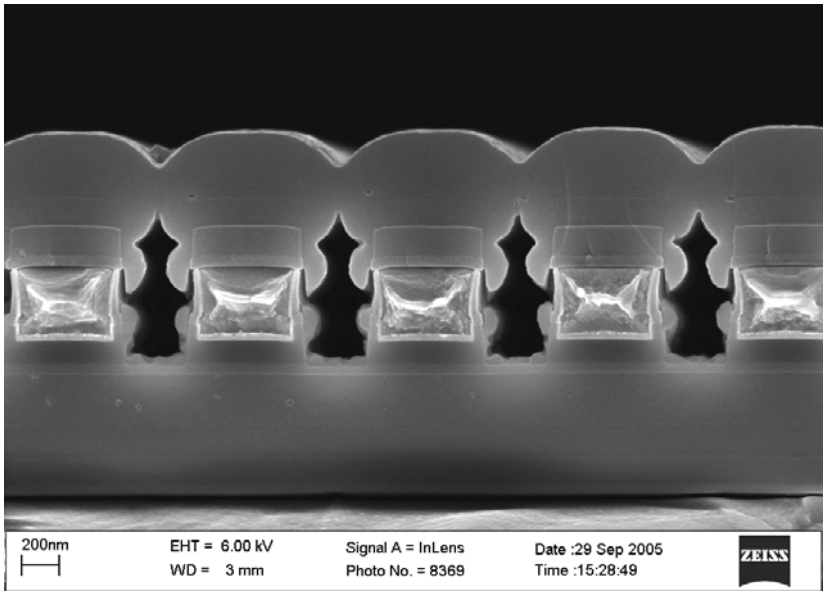


Fig. 50: SEM image with improper cleaning leading to sidewall deposition

The aggressive cleaning solution and the fact that copper rapidly oxidizes in ozone atmosphere leads to the most critical process: the air gap lithography. When the air gap lithography is not aligned properly between the metal lines, no dielectric spacer remains after the air gap trench etch or even the metallic barrier is damaged, see Fig. 51.

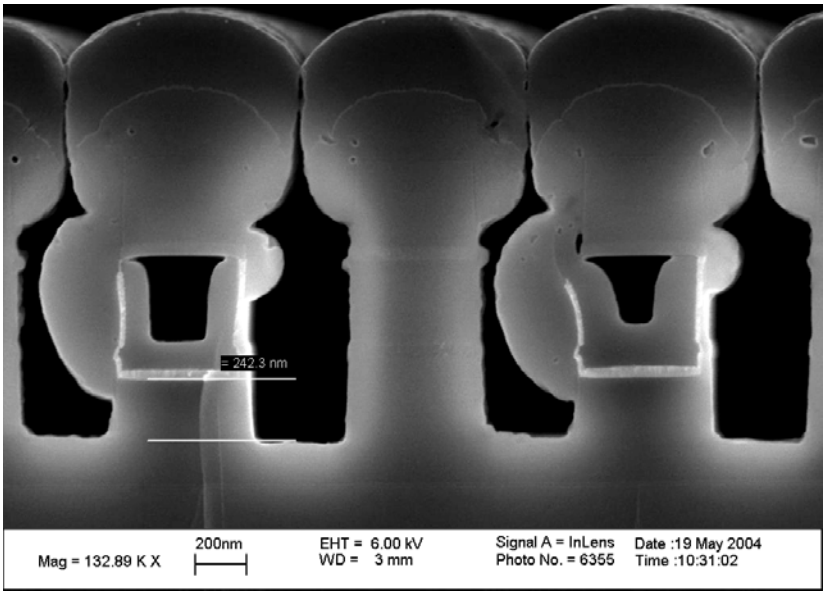


Fig. 51: SEM image of misaligned air gap lithography

Then, the copper surface is oxidized during O_3/TEOS deposition and the copper may incidentally be removed during EKC265 cleaning. Only the thin barrier metal of the lines remains and the O_3/TEOS can grow on the inside of the former Cu line, see Fig. 51.

Another lithography effect is the proximity effect, which leads to narrower lines at the edges of structures close to wide unstructured regions. In contrast to that effect, wider air

gaps were detected at the borders of comb structures, leading to damaged copper lines. This effect can be explained by an overdevelopment of the photoresist at the structure borders. Because of the long distance to neighboring structures, a fresher, unused developer is present and therefore the resist development is further progressed. In Fig. 52, the resist structure at the right side shows a V-shaped side wall. During air gap trench etch, this shape is then transformed into the SiO_2, leading to damage on the left side wall of the right copper line.

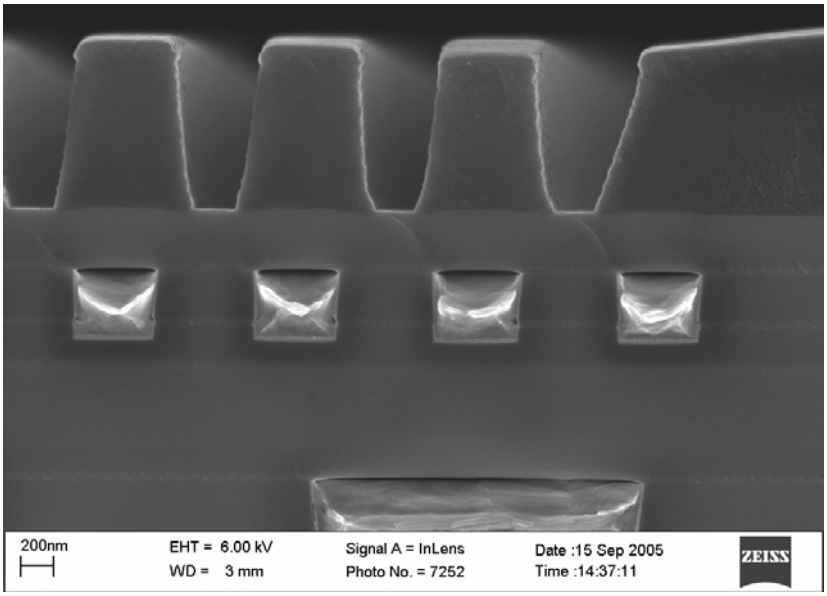


Fig. 52: SEM analysis of photoresist at structure borders

As a summary, using an additional lithography mask is a severe drawback of the approach discussed so far since it increases production costs and restricts scaling. A self-aligned process where the air gaps are solely defined by the metal lines would be much more appropriate. However, from an integration point of view, the biggest advantage of the additional lithography mask is that the air gaps may be placed wherever they are needed. For example, integrating air gaps between long bus systems would be a big benefit for the *RC*-delay, whereas the space around vias may be excluded to ensure proper via integration.

4.3 Self-aligned air gap approach in damascene metallization

4.3.1 Process steps for self-aligned air gap approach

To avoid this additional lithography step, a self-aligned air gap approach based on the selective O_3/TEOS deposition was developed. The selectivity requirements of the selective O_3/TEOS deposition process pose some limitations on the material selection. In order to be able to close the air gaps, the upper part of the metal lines has to be covered by a material which allows good oxide growth, while the side walls of the metal lines and the dielectric exposed in the line space at the base of the metal lines must consist of materials on which O_3/TEOS does not grow. Therefore, the materials as seed or base layer have to be carefully chosen for the selective O_3/TEOS air gap approach, for details see Table 6.

Basically, Cu technology uses the main conductor of metallic Cu and the barrier materials TaN/Ta or Ti/TiN. Dielectric materials are oxides (either silane-based or TEOS-based PECVD) or nitrides in older technologies, or low-k films such as a-SiC, SiOC, SiON, SiLK or others, in newer technologies. In addition, alloys such as CoWP, NiMoP are being investigated as new capping layers in advanced processing schemes mainly to improve reliability [Ish04].

The first idea of a self-aligned approach was to use Ta as a capping layer, the standard barrier material. The idea was to etch back the copper surface with a wet etch, then to deposit Ta by PVD and remove the Ta on the SiO_2 surface by CMP. The blocking point was that Ta is not dense enough to protect Cu from ozone and EKC265, which leads to massive oxidation of copper, see Fig. 53. The grainy layer around the copper lines seems to be oxidized copper. Since copper oxide is etched very fast in HF solution no decoration of the sample was performed.

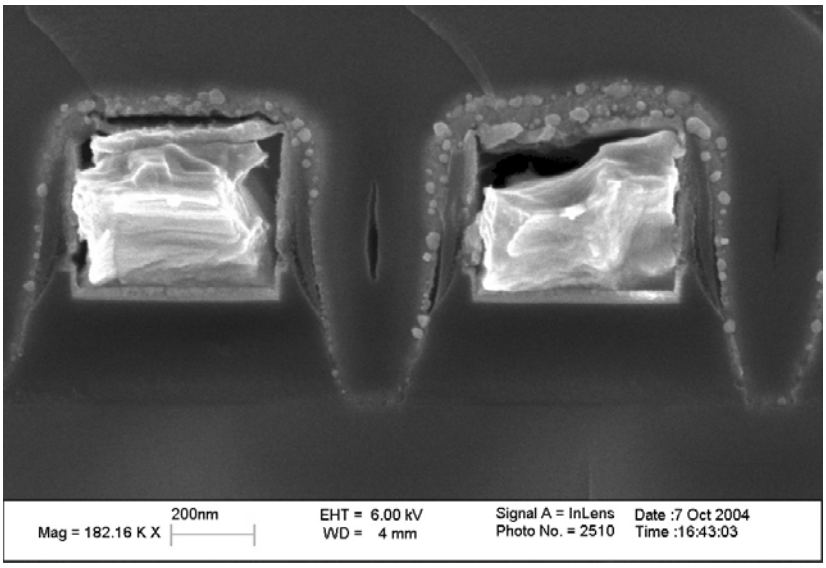


Fig. 53: Leaky Ta capping layer leading to copper oxidation

More than 100 experiments (5 lots of 25 wafers) were performed with the self-aligned process idea with a variety of cleans, wet and dry, different capping layers and different etch processes. All experiments with self-aligned air gaps were performed on the same test chip as the air gaps with lithography.

In Fig. 54, the process steps of the final self-aligned air gap approach for damascene metal lines are depicted. First, standard copper damascene structures are embedded in SiO_2. Just beneath the copper lines, the dielectric stack is modified by an additional etch stop layer and by modified TEOS SiO_2 as ILD (Fig. 54-1). Up to this step, the wafers have been processed in the production line. In order to avoid contamination of the production line and to have more samples available, the wafers were cleaved in quarters and further processing was done in a laboratory clean room separate from production. In the second step (Fig. 54-2), a selectively grown barrier capping layer of CoWP or NiMoP is deposited on the copper surface, serving later on as seed layer for the O_3/TEOS growth. The deposition of such layers is explained in the following chapter. In a next step, the IMD is removed by wet etch and, in the following dry etch process, the Si_3N_4 damascene etch stop

layer is etched to extend the air gaps beneath the metal lines (Fig. 54-3). To achieve good selectivity of the O_3/TEOS process, a Si_3N_4 spacer is formed to protect the copper and to serve as a base layer (Fig. 54-4). Spacers are formed by a conformal deposition of the material and a subsequent anisotropic etch to remove the material on the level surfaces and to keep the material at the perpendicular surfaces. After proper dry and wet cleaning, the O_3/TEOS deposition is performed to form the air gaps (Fig. 54-5). The different dry cleaning experiments will be explained in Chapter 4.3.3.

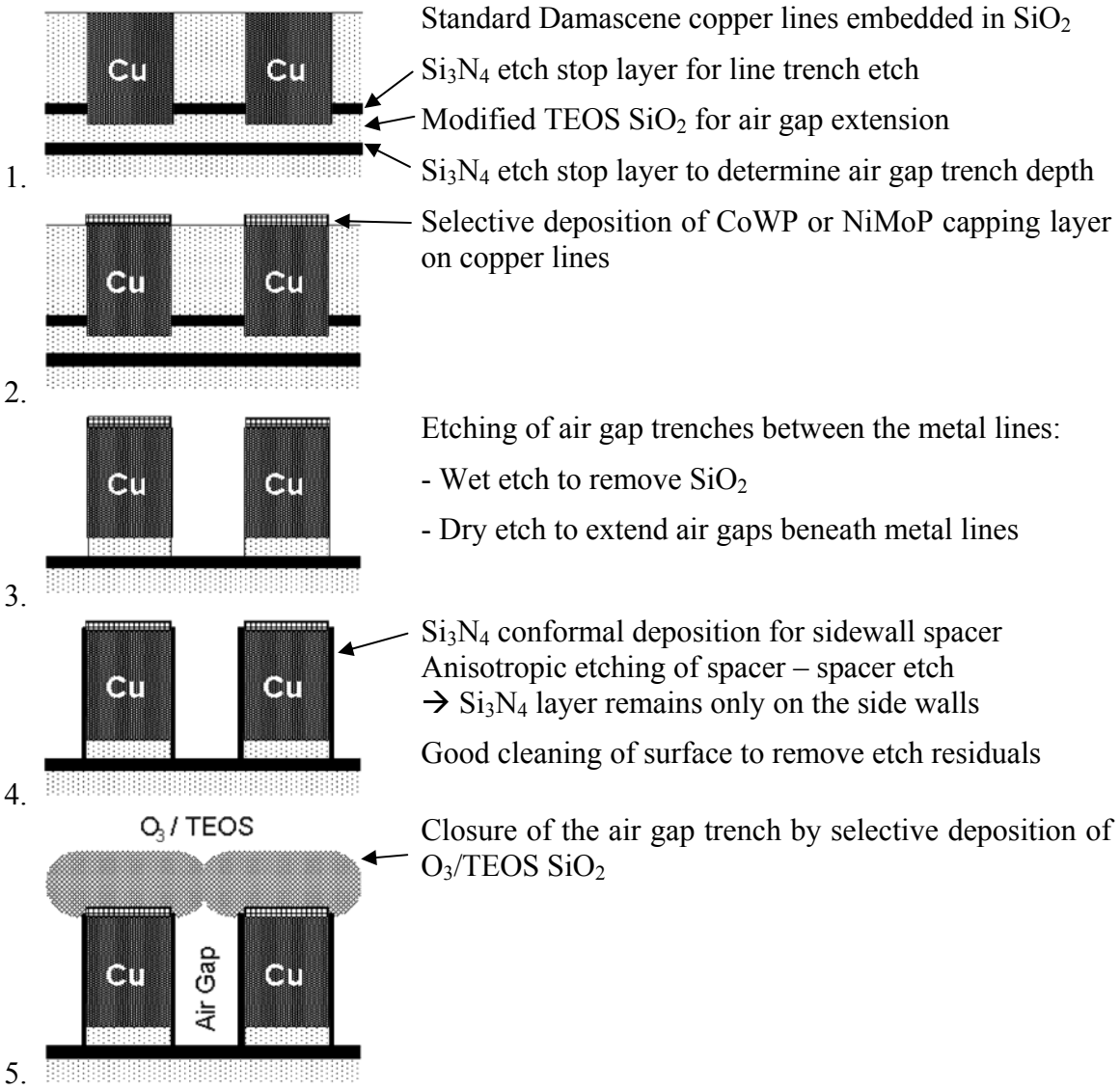


Fig. 54: Schematic process flow for fabrication of self-aligned air gaps using selective O_3/TEOS deposition in a damascene architecture

4.3.2 Properties and deposition of selective metal barriers

One of the key processes of the self-aligned air gap approach is the selective metal barrier deposition. The electroless deposition technique of cobalt or nickel-based metal coatings has been known for many years, but it has been investigated only since around 5 years as a capping barrier layer for copper metallization in the semiconductor industry. The idea is to deposit CoWP or NiMoP metallic capping layers selectively on copper to improve

electromigration properties, the adhesion of copper to the surrounding layers, and to reduce the *RC*-delay because the high-*k* dielectric capping layer can be omitted [Wir04].

For our application, the metal barrier has to provide some vital properties, such as serving as a seed layer for O_3/TEOS deposition, protection layer for copper against oxidation, plasma etch processing and etch stop layer during air gap extension beneath the metal lines.

Because neither a fabrication process nor a solution is available on the market, a customized solution was developed. The papers [Pet02] and [Ish04] served as an important basis for our recipe of the solution, for recipe details see Appendix B. The deposition of the electroless CoWP or NiMoP metallic coating is a wafer dip process in a glass dish. The optimum process conditions are a temperature between 70 - 90°C and a pH-value of 9 at room temperature. The pH-value is adjusted by the addition of diluted KOH. Further on, the reaction needs a catalyst, which can be provided by dipping the sample for 10s in a palladium solution or by adding DMAB (Dimethylamine-Boran complex) to the electroless solution. The addition of DMAB is the process of choice since it is simpler and does not require a second dip process. Further on, a slight incorporation of boron occurs in the deposited films.

Chemically, the deposition is a redox reaction. Hypophosphite as the source of phosphorous is adsorbed on the surface (ads) and oxidized under outgassing of hydrogen, leading to bubbling.

$$2H_2PO_{2\,ads}^- + 2OH_{ads}^- \Rightarrow 2H_2PO_3^- + H_2 \uparrow + 2e^- \tag{29}$$

The reduction mechanism consists of two reactions: the reduction of cobalt ions and of phosphorous. Cobalt sulfate serves as cobalt source in the deposition dilution.

$$Co^{2+} + 2e^- \Rightarrow Co \downarrow \tag{30}$$

$$H_2PO_{2\,ads}^- + e^- \Rightarrow P \downarrow + 2OH^- \tag{31}$$

These two reduction reactions lead to the deposition of cobalt and phosphorous and the whole chemical reaction can be written in a redox reaction equation.

$$Co^{2+} + 2H_2PO_{2\,ads}^- + 2OH^- \Rightarrow Co \downarrow + H_2PO_3^- + H_2 \uparrow \tag{32}$$

At the same time, tungsten is co-deposited by another reduction reaction. Sodium tungstate dihydrate or the $H_3[P(W_3O_{10})_4]$ compound serve as tungsten source.

$$WO_2^{2+} + 6H_2PO_2^- + 4H_2O \Rightarrow W \downarrow + 6H_2PO_3^- + 3H_2 + 2H^+ \tag{33}$$

As the main metal in the dilution is the cobalt compound, the metallic product mainly consists of cobalt. The redox reaction of the NiMoP deposition is alike with the substitution of cobalt by nickel and of tungsten by molybdenum [Osa89], [Sri01].

In the following figure, the deposition rate of the nickel-based and the cobalt-based solution is depicted. All depositions were performed on copper surfaces with solutions incorporating DMAB (no Pd activation) at 80°C. The layer thickness was measured by SEM inspection.

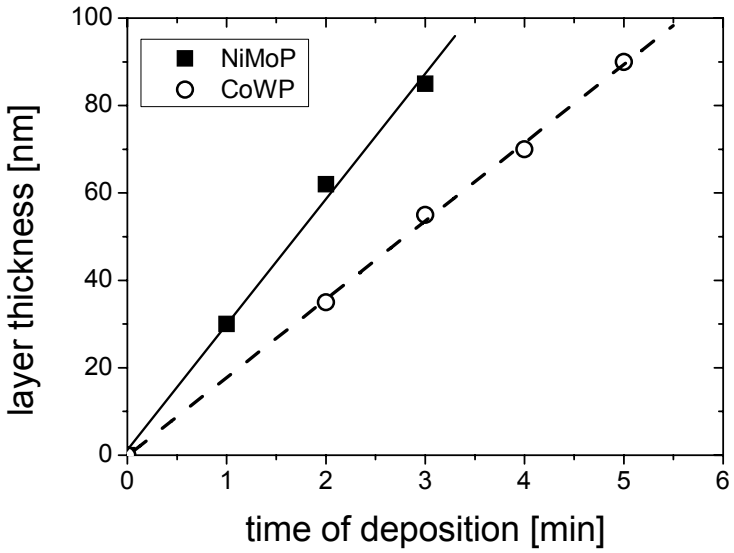


Fig. 55: Deposition rate of CoWP and NiMoP

The nickel-based solution exhibits a growth rate of 30nm/min whereas the cobalt-based solution only grows at 18nm/min. Both solutions show a linear growth rate over time.

Moreover, the composition of these films is important for their properties. For example, the refractory metal content of W/Mo has a big influence on the thermal stability, the hardness and corrosion resistance [Sri01] whereas the phosphorous content influences the electromigration and barrier properties [Wir04]. The composition of the CoWP films was analyzed on wafer pieces deposited with CoWP on top of a copper layer with an EDX detection system connected to our LEO1560 SEM. The received EDX spectra with 15kV electron beam energy can be seen in Fig. 56.

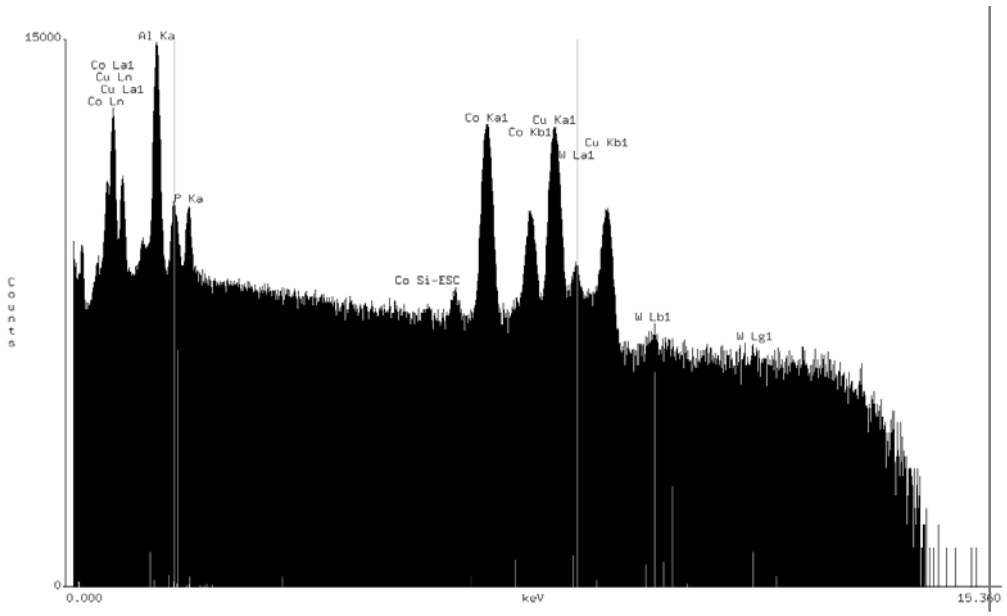


Fig. 56: EDX analysis of CoWP

It can be seen that cobalt, phosphorous, aluminum, copper and tungsten detection peaks are present in the spectra. The copper peaks are due to the copper layer under the CoWP layer. Aluminum is apparent because the probe mount is of aluminum. From the peak height of the spectra, the composition of the detected materials can be calculated via the EDX software. Table 8 shows the calculated composition of CoWP.

Table 8: Composition of CoWP according to EDX

Element	Atom %	Element Wt%
P-K	7.60	2.03
Co-K	87.97	77.21
W-L	4.43	20.76

According to the EDX analysis, the film mainly consists of cobalt (88 at%). The analysis is in good agreement to literature results of ~ 92at% Co, ~ 4at% W and ~ 4at% P [Pet02].

The composition analysis of NiMoP with EDX showed very high values of B. For further confirmation NiMoP was analyzed with ICP-MS (inductively coupled plasma mass spectrometry). The wafer sample with the NiMoP film on the copper layer is wet etched and then this solution is vaporized. Subsequently, the vaporized solution is applied to argon plasma to ionize the diluted atoms. The last process is to extract the ions out of the plasma into a mass spectrometer to identify the ions. The concentration of a sample can be determined through calibration with elemental standards. See Table 9 for the composition of NiMoP analyzed with ICP-MS.

Table 9: NiMoP composition

Element	Atom %	Element Wt%
Ni	84.11	77.88
Mo	14.12	21.39
B	0.40	0.07
P	1.37	0.67

In literature, the composition of NiMoP alloys is in the range of 65 - 90at% of nickel, 7 - 24at% of molybdenum and 2.5 - 17at% of phosphorous and boron [Wir04], [Sri01], which is in agreement with our findings.

The resilience and the barrier integrity of the CoWP alloy were tested by deposition of 100nm of O_3/TEOS on 50nm CoWP layer (with Pd activation) with an underlying thick copper layer. The whole stack was then analyzed by XPS depth profile measurements. For depth profile analysis, the measurement spot is sputtered with argon and the surface of the sputter crater is analyzed by the very surface-sensitive XPS measurement technique. The sputter time of the analysis is a measure for the sputtered thickness. It has to be mentioned that the sputter time is not linear to the depth due to different sputter rates dependent on the sputtered material. In Fig. 57, the apparent atomic concentration is depicted over the sputter time.

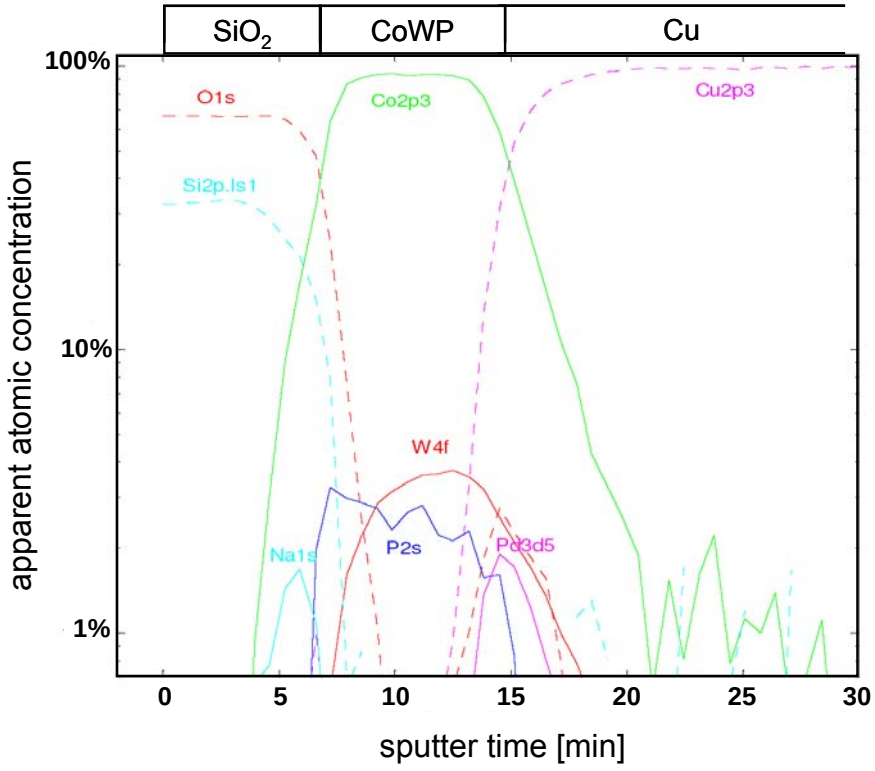


Fig. 57: XPS depth profile analysis of O_3/TEOS on CoWP and Cu

On the left side of the depth profile diagram at short sputter times, only silicon (~ 30at%) and oxygen (~ 65at%) are detected. That reflects the fact that the most upper layer is the O_3/TEOS SiO_2 layer. At 5min sputter time the interface of SiO_2 to CoWP is reached. At this point, slight sodium incorporation is observed, which can be prevented by the use of a sodium free CoWP solution. Then, after around 10min sputter time, the middle of the CoWP layer is reached with a phosphorous and tungsten concentration of 3 - 4at% and 90at% cobalt and what is most important no oxygen. This shows that the CoWP layer is not corroded by the ozone. The activation catalyst palladium was found at the interface of CoWP to copper at 15min sputter time. At this point only a very low content of oxygen is found, which prooves the good barrier properties of CoWP to protect copper from oxidation during ozone exposure.

The adhesion of the stack copper, CoWP, O_3/TEOS SiO_2 was measured with pull tests. For such a test a specific metal pin was glued to a sample wafer piece, annealed to harden the glue and then the pin was pulled from the surface and the maximum applied strength is measured. The adhesion of the stack was very good and is greater than 700kg/cm², which is the maximum the glue withstands. Consequently the glue broke and the pin was pulled off the surface.

The selectivity is one of the key aspects of the selective barrier deposition. On structured wafers the selective barrier deposition is done right after CMP of the TaN/Ta barrier. Without proper cleaning of the surface and the fact that the electroless growth is very sensitive to copper, residuals which are left over after CMP act as seed spots on the SiO_2 surface. The growth on copper is as expected, see Fig. 58.

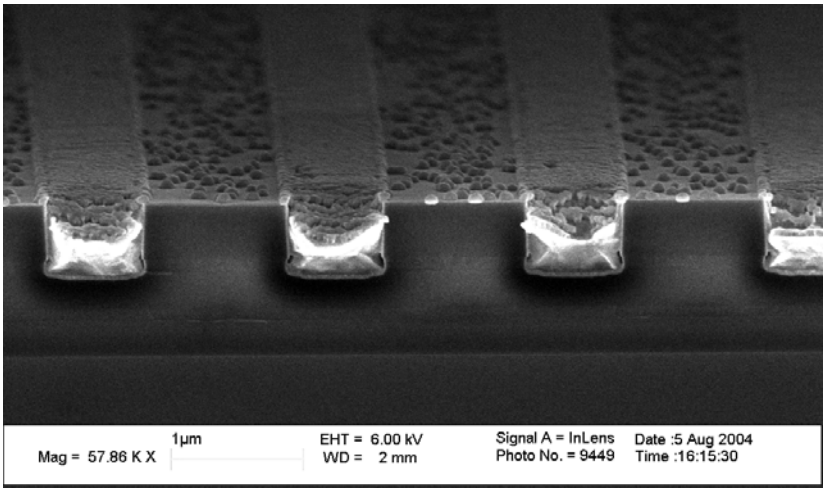


Fig. 58: Discarded CoWP deposition on SiO_2 surface without clean after CMP

To prevent the CoWP growth on the polished SiO_2 surface, a simple 5 - 20s wet cleaning step was introduced. The cleaning solution consists of diluted 2% $(NH_4)_2S_2O_8$ and slowly etches copper and therefore removes the small CMP copper residuals, see Fig. 59.

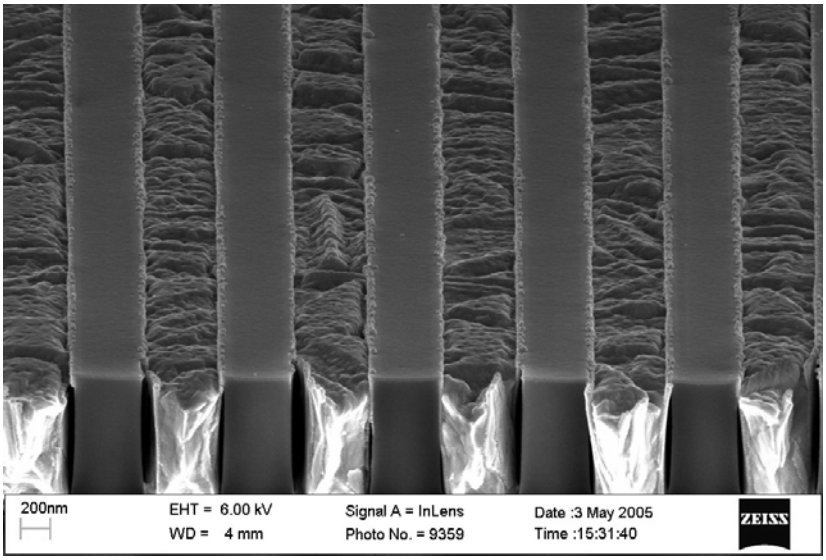


Fig. 59: CoWP deposition on a cleaned wafer

As can be seen, the clean is very effective and no unwanted deposition occurs. The CMP issues were already mentioned by Ishigami [Ish04].

4.3.3 Plasma cleaning and SEM analysis of self-aligned air gaps

Due to the presence of copper and the electroless Co or Ni alloy barrier, no EKC265 standard cleaning solution could be used because this solution dissolves these metals. The metals are dissolved because they form an electrolytic element. Nevertheless, good cleaning was necessary to remove dry etch residuals and enhance the surface selectivity of the O_3/TEOS process. Several different wet cleans and dry plasma cleans were tested. As

wet cleans, three additional solutions of EKC-tech were tested; EKC525, the standard cleaning solution for copper metallization; EKC5800, a cleaning solution for copper in combination with low-*k* materials; and CRX03, which is still in development and was provided to us by EKC. The EKC5800 solution contains 2% ammoniumhydrogen-difluoride $(NH_4)HF_2$ and is therefore etching SiO_2 because diluted ammoniumhydrogen-difluoride discharges hydrofluoric acid HF. Unfortunately, both EKC5xx solutions served as electrolytes because they are acidic and dissolved the electroless Co or Ni alloy. The CRX03 solution was not sufficient for achieving good selective growth.

For that reason, different dry plasma clean sequences were tested with O_2, O_2/N_2, N_2, NH_3, NO_2 and H_2 as plasma gases. The oxygen and nitrogen-based plasma cleans were carried out in a P5000 etching tool and the hydrogen, NO_2 and NH_3-based in a P5000 deposition tool.

In Fig. 60, a SEM image of a fully processed self aligned air gaps structure with a line space of 0.45µm and a three step cleaning sequence is depicted. The first step was a 20s 0.5% HF dip then a 3min O_2/N_2 plasma preclean and a 5min insitu H_2 clean.

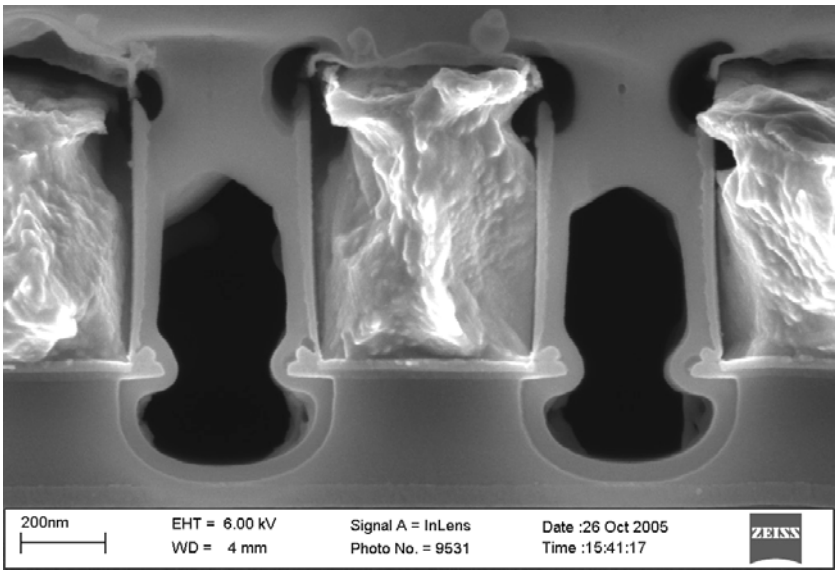


Fig. 60: SEM image of self aligned air gaps in damascene processing scheme

As can be seen, the selectivity of the O_3/TEOS deposition is not as good as it is with the EKC265 clean used with the air gaps with lithography. The unintentional sidewall deposition is in the range of 30 - 50nm which is equivalent to a selectivity of 7:1. Another issue is the minor oxidation of the corners of the copper lines, which can be seen by the decoration of the corners of SEM preparation (extensive etching of CuO in HF). Due to the long dry etching to extend the air gaps beneath the copper lines, the corners are not chemically etched but sputtered. In the following figure, a SEM cross-sectional image with reduced sputtered corners due to a shorter etch process is depicted. The sidewall deposition is with 50 - 70nm a little bit thicker but the corners of the copper lines are not oxidized.

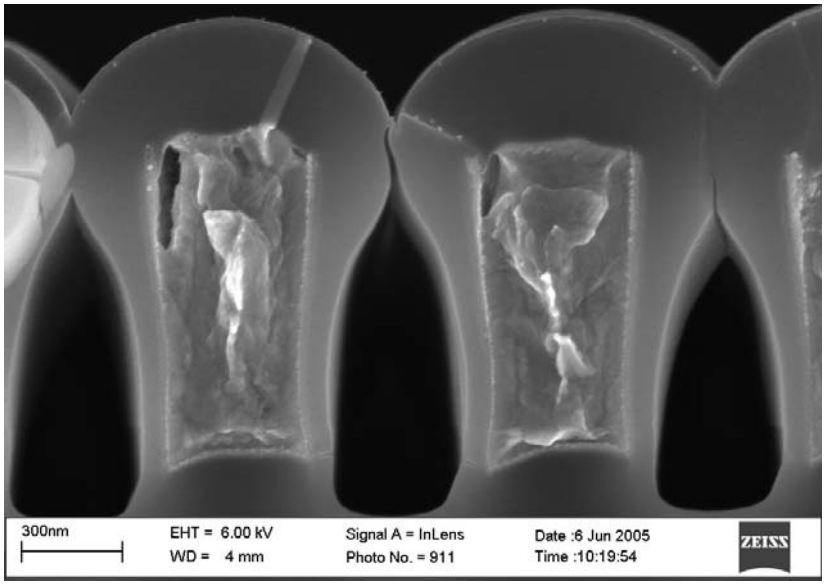


Fig. 61: SEM cross-section of self aligned air gaps in damascene metal scheme

From an integration point of view, a benefit of that process compared to the non-conformally integrated air gaps is that the tip of the air gap is beneath the line height, which allows easier via integration without opening and filling the air gaps during via etch and metal filling. When integrating such air gaps, the dip between wide spaced lines have to be filled by an additional thick dielectric deposition and CMP for planarizing the wafer surface.

4.4 Self-aligned air gap approach in RIE metallization

4.4.1 Process steps

The integration of self-aligned air gaps by the selective O_3/TEOS deposition in an Al or W RIE metallization scheme is more straightforward than in damascene metallization. Because the metal lines are etched the trenches for the air gaps are already formed. Additionally the standard wet cleaning solution EKC265 can be used because it is not abrasive against open aluminum or tungsten. Moreover no special seed layer like CoWP or NiMoP is needed; the dielectric seed layer is just integrated before metal etching.

In Fig. 62, the process steps of the self-aligned air gap approach for RIE metal lines are depicted. Initially the standard metal stack with barrier/adhesion layer, the metal layer and another adhesion/arc layer is deposited on modified TEOS SiO_2. This layer is necessary to avoid the growth of O_3/TEOS on the bottom of the future air gap. Then, on top of that standard metal stack the seed layer, a silane-based SiO_2 layer, is deposited (Fig. 62-1). The metallic stack and the seed layer are structured with a lithography and a dry etch step. The etch step may be a two step process to etch the seed layer first and then the metal stack (Fig. 62-2). It was observed that tungsten is also preventing the film growth of O_3/TEOS, therefore no coverage of the tungsten is necessary and the process becomes even simpler. For aluminum an additional spacer deposition of for example Si_3N_4, SiOC or a-SiC, and a spacer etch are required to cover the sidewalls of the aluminum lines. For details on the

spacer fabrication, see Chapter 4.3.1. Then, the trenches between the metal lines are properly wet cleaned with EKC265 and a 0.5% HF-dip, before they are finally closed by the selective O_3/TEOS process (Fig. 62-3).

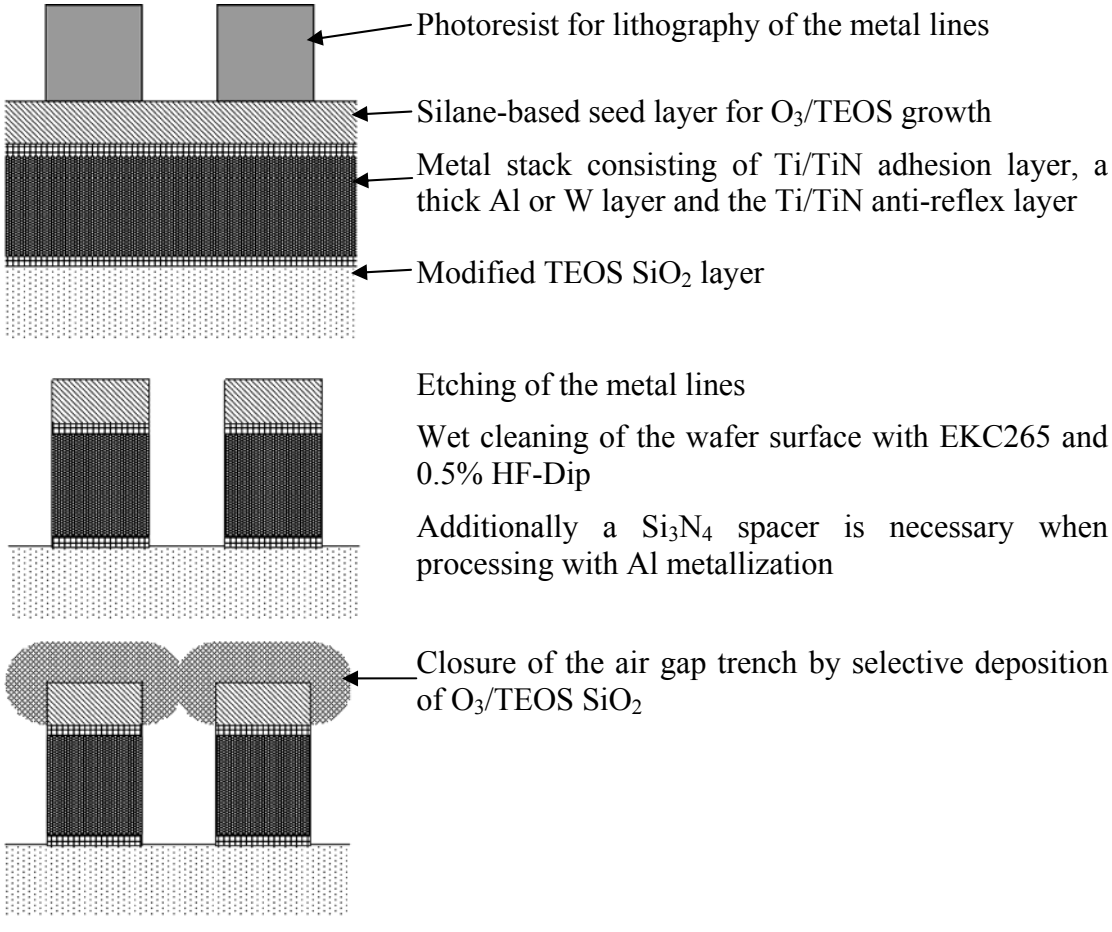


Fig. 62: Schematic process flow for fabrication of self-aligned air gaps using selective O_3/TEOS deposition in a RIE metal architecture

For integration, the whole wafer has to be planarized. This is achieved by depositing a thick dielectric layer to fill the empty spaces between far away metal lines and then the wafer is planarized by CMP.

4.4.2 Air gaps in tungsten RIE metallization

Air gaps were fabricated with the explained process with tungsten as metallization material. A different test chip for RIE metallization had to be used. This test chip comprises only two different comb structures with a line space of 0.5µm and 1.0µm, meander structures and a lot of short lines for resistance measurements. The different mask set was necessary because an inverted mask is used in damascene compared to RIE metallization. In Fig. 63, an overview of air gaps integrated in RIE tungsten metallization is illustrated. In the overview, it can be seen that after metal etch and air gap formation, a huge topography is observed, which is common for RIE metal integration. This topography can be leveled by depositing a thick dielectric layer after air gap formation and chemical mechanical polishing of the dielectric. The air gaps look very regular with the

same size and selectivity of the O_3/TEOS process, which is very favorable for integration. For integration a predictable and uniform shape of all structures is favorable so that the electrical performance does not show huge variations.

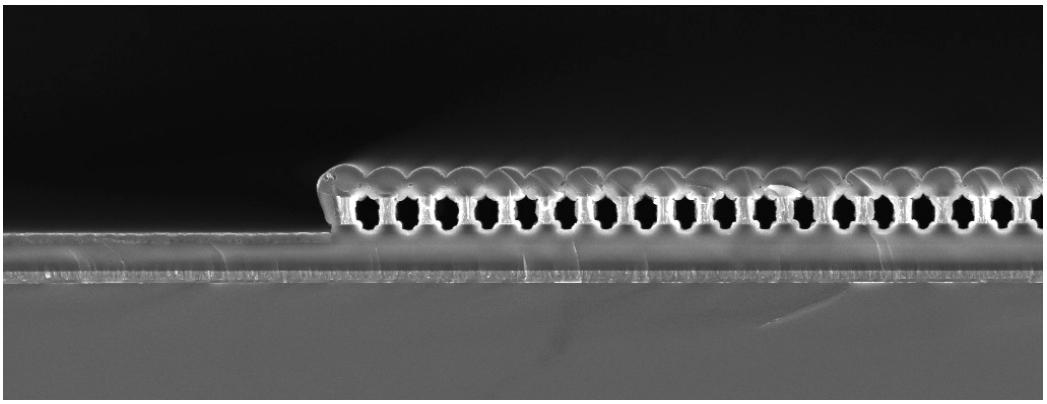


Fig. 63: SEM image of an overview of air gaps in tungsten RIE metallization

In Fig. 64, a detailed cross-sectional image of a comb structure comprising air gaps in a tungsten RIE metallization is shown. It has to be mentioned that the rough surface and the constriction of the metal lines is due to a non-standard and not optimized tungsten etch process. This is because tungsten is processed in Munich Perlach Ha84 only by the damascene technique and a standard tungsten RIE process does not exist.

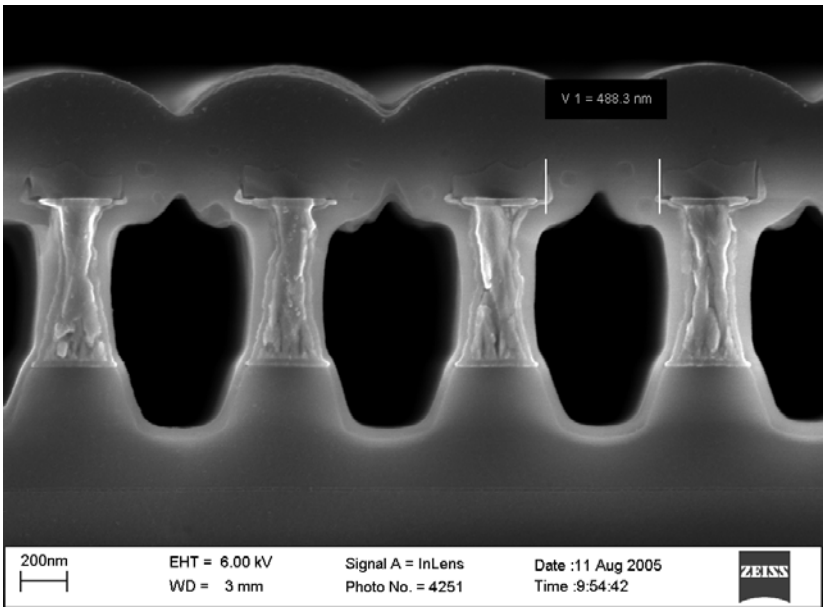


Fig. 64: SEM cross-section of air gaps in tungsten RIE metallization

It appears that the selectivity of the O_3/TEOS deposition of silane-based SiO_2 to tungsten is up to 10:1 leading to only marginal growth of 25nm oxide layer at the inner air gap surface. The high selectivity and an overetch of 250 - 300nm of the tungsten etch process resulted in air gaps occupying most of the space between the metal lines. In the depicted sample, we used a hard mask process to fabricate the tungsten metal lines. For patterning,

1.5µm silane-based SiO_2 was present on top of the tungsten film and structured with a lithography mask. Subsequently, the tungsten etch was performed with a low etch selectivity of tungsten to SiO_2. During this etch process the whole silane-based SiO_2 layer except for 100 - 200nm was consumed resulting in a rather rough surface of the rest of the hardmask. This process seems feasible for via integration with the restriction of only small overetch of the via etch process and a maximum misalignment of around 30% of the line width to prevent opening of the air gaps during via processing.

4.4.3 Air gaps in 90nm aluminum RIE metallization

The air gaps in 90nm aluminum RIE metallization were processed in Dresden on 300mm wafers. No selective O_3/TEOS deposition was used for closure of the air gaps, since this process is not available in Dresden. Instead the air gaps were closed by a non-conformal silane-based SiO_2 PECVD deposition. The metal lines were fabricated with standard processes [Web05], only the capping of the line structures was performed with a non-conformal deposition. The wafers were patterned with a standard back end of line test chip for the 90nm node comprising meander structures, comb structures, reliability structures, etc. see Chapter 4.1. In Fig. 65, air gaps in standard 90nm aluminum metallization are depicted.

The metallic stack of the interconnect lines consists of 50nm TiN, 280nm aluminum and 30nm TiN on top. According to SEM analysis, the air gap width is 70nm at the upper and lower part in the TiN layer and 90nm in the middle in the aluminum layer. The aspect ratio of the whole metal stack is very high (3.6:1). Thus the capacitance reduction effect of air gaps is strong. The uniformity of the air gaps is very good and because of the high aspect ratio and the very non-conformal process only a maximum 5nm thick SiO_2 film is deposited at the metal sidewalls.

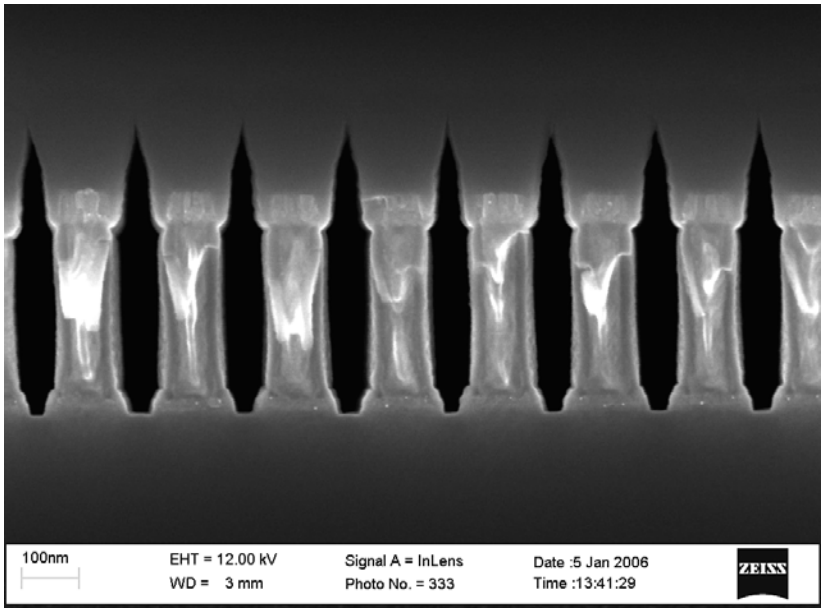


Fig. 65: Air gaps by non-conformal deposition in 90nm Al metallization

Because the growth direction of such a deposition process is mainly upwards, however, an elongated tip is formed at the top of the air gap before closure. This behavior is not

advantageous as it may result in the risk of re-opening the air gaps during CMP processing in case of varying line spaces or non-uniform CMP rates.

Unfortunately, this air gap approach implies a severe obstacle for integration, since no via misalignment is acceptable, without opening the air gaps during via etch. In actual integration schemes, a via misalignment of 30% of the line width is allowed, which translates into a misalignment of ~30nm. At the moment, it is impossible to reach 100% overlay accuracy with acceptable yields. This problem may be overcome by combining the simple non-conformal or selective O_3/TEOS air gap process with a course lithography step to integrate air gaps just were they are needed and are not bothering integration. For instance, capacitance reduction is most important in data busses or signal lines, clock signals to reduce the power dissipation or in noise sensitive lines.

One solution would be to perform this additional lithography after the non-conformal deposition, opening up the spots where air gaps are unwanted with a dry etch process and finally deposit a conformal dielectric to fill up the spaces between the open metal lines. This deposition could be performed with a HDP (high density plasma) deposition. Moreover, the mechanical strength, for example under bond pads, can be improved by excluding these areas from air gaps.

5 Electrical characterization

The used test chip for fabrication of air gaps with the selective O_3/TEOS process is a BEOL test chip for copper metallization with aluminum pads. The test chip is without active devices and comprises additional lithography layers for air gap fabrication with additional lithography. For comparison purposes, versions of all structures with air gaps and without (the so-called "full" structures) are available on the test chip. This design allows direct comparison of all electrical and physical data to the presence or absence of air gaps all fabricated with the same processes on the same wafer.

5.1 Capacitance properties

5.1.1 Capacitance simulations setup of fabricated structures

In order to compare the observed reduction of line-to-line capacitance due to air gaps with low-*k* or ultra-low-*k* materials, an effective *k*-value is usually introduced. This is to be understood as the dielectric constant of a hypothetical, uniform material into which the metal lines with the same dimensions are embedded and which leads to the same line-to-line capacitance as the air gap structure. It is not straightforward to specify the effective *k*-value of our air gap samples since they consist of a variety of materials, each with its own *k*-value. Therefore, adaptive finite element calculations were performed in order to determine k_{eff}, see Chapter 2.8.2.

In the left half of Fig. 66, a SEM images is illustrated in comparison to the distribution of the electrical potential between the conductor lines of a simulated structure.

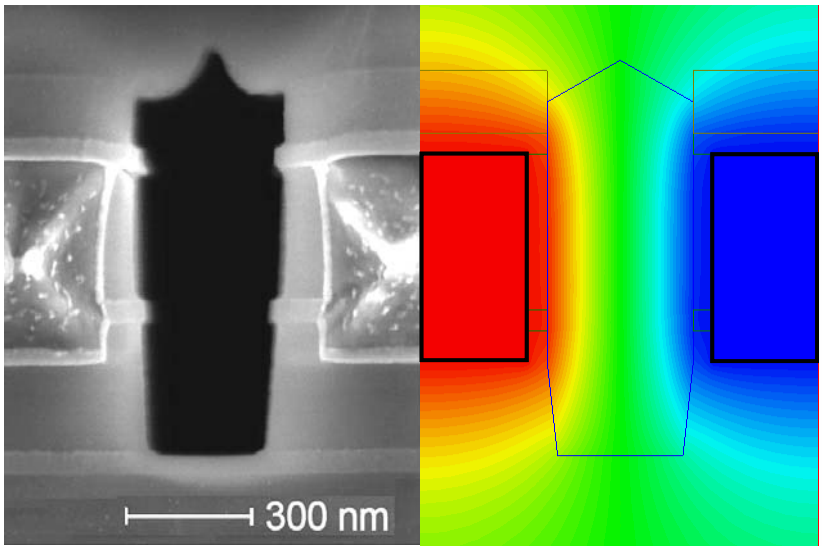


Fig. 66: Left side: SEM cross-sectional micrograph of an air gap; right side: Electrical potential values as color shades between Cu lines

In general, the air gap should be positioned such that, as many areas with a high potential gradient as possible are covered. In the right-hand side of Fig. 66, this is where the colors vary strongly over a short distance. The dielectric constants of the individual layers were measured experimentally using macroscopic test capacitor electrodes on the blanket dielectric films of interest ($k_{oxide} = 4.3$, $k_{nitride} = 7.5$). Because our measurements were made with comb structures having a large number of long fingers, periodic boundary conditions were usually assumed in 2D calculations. The unit cell repeated periodically consists of a central conductor line and two outer lines, the latter to be considered only in half, see composite Fig. 66. The central (red) and the outer lines (blue) are assumed to be at opposite potentials. The periodic boundary conditions reduce the finite elements and therefore help to master calculation time. Fig. 66 also shows the geometrical approximations made to simplify the 2D drawing. In the following chapters, simulations were performed to calculate k_{eff} and comparisons between the simulations and the measured data were conducted.

5.1.2 Capacitance measurements of air gap with lithography

Air gaps offer an interesting alternative to low-*k* or ultra-low-*k* materials in order to reduce the line-to-line capacitance in a metallization system. Electrical measurements of the line-to-line capacitance were performed by means of interdigitated comb structures. In these patterns, the metal spaces were varied between 0.45 - 1.1µm, while the air gap widths of 0.38µm and the line widths of 0.50µm were kept constant, see Chapter 4.1.2.

5.1.2.1 Results of air gaps in a single metal layer scheme

For comparison, the capacitances of air gap and full structures with different line spaces were measured and then the ratio of the capacitance of the air gap structures to that of the full structures was calculated. In Fig. 67, the capacitance ratio versus the line space is depicted. The results in Fig. 67 clearly show a decrease of the capacitance with decreasing line spaces as it is expected for the increasing fraction of air gap volume between the lines.

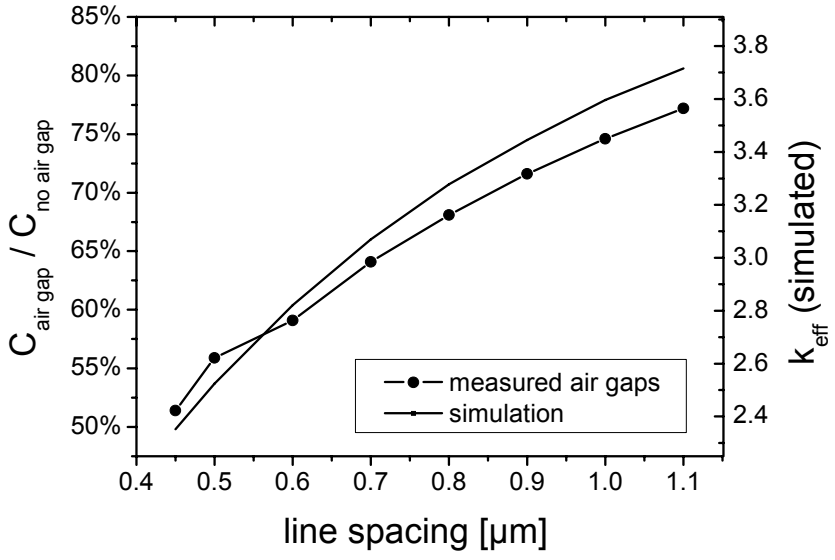


Fig. 67: Capacitance ratio of air gap to full structures and simulated k_{eff} versus line space.

In case of the most closely-spaced lines, a capacitance ratio of approximately 50% between air gap and full structures is observed. The line plot in Fig. 67 also shows the simulation results, which were performed to extract the k_{eff} value. As input for these simulations, *k*-values for the various oxides of 4.2 and for the nitride layers of 7.5 were used. Using these numbers, the effective *k*-value for the full structures varies between 4.7 (narrow line space) and 4.6 (wide line space). Therefore, it can be concluded that $k_{eff} \sim 2.4$ for the minimum line space, see Fig. 67. This is a very low value considering the use of standard materials like SiO_2 and Si_3N_4 in the integration. Such a low value has not been achieved so far by integrating copper lines into low-*k* materials. There, the continuous etch stop and capping layers degrade the effective *k*-value dramatically, which leads to k_{eff}-values even for porous materials around 2.7 [Har06]. The deviation of measured data and simulated data is below 3% and is mainly attributed to non-uniformities of the air gap and line dimensions.

The measurements above were performed at 50kHz standard measurement frequency of the *LCR*-meter, see Chapter 2.8.4. Further on the used model in the *LCR*-meter was a resistance in parallel to a capacitor. This is the most reasonable model since our test structure comprises thick metal wires to the combs which guarantee low serial resistance. Moreover measurements were carried out to investigate the dependence of the capacitance on the measurement frequency. The frequency was swept from 50Hz to 5MHz, while measuring the capacitance, see Fig. 68. The measurements were performed on six different structures with different line space and with or without air gaps.

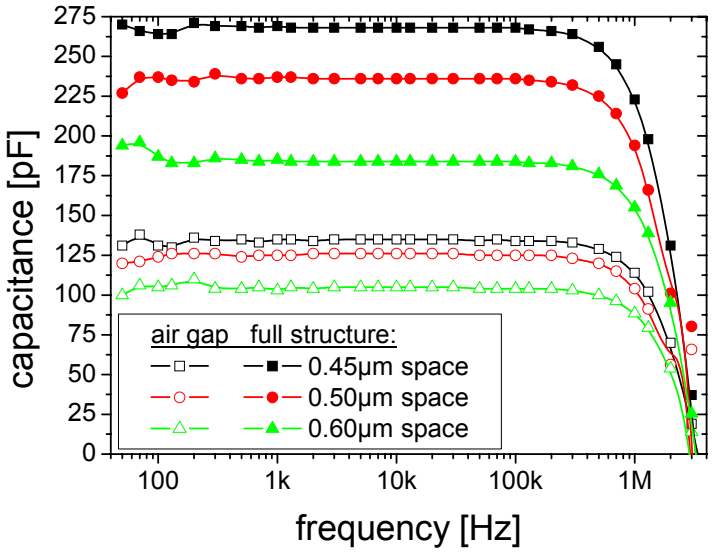


Fig. 68: Capacitance of comb structures versus measurement frequency

As can be seen, the capacitance values of all structures are fluctuating below 400Hz, are stable between 400Hz and 300kHz and drop above 500kHz. The fluctuation at low frequencies can be explained by the very low current in the nA regime that has to be measured to calculate the impedance and the loss tangent. The current is so low, because the impedance of a capacitor is very high at low frequencies. On the other hand, when rising the measurement frequency, the impedance of the capacitor is decreasing and then the series resistance of the support metal lines and the resistance of the combs itself has to be taken into account. For example, the support lines have a resistance of 50Ω and each

comb has a resistance of 250Ω, whereas the impedance of the capacitance of a 0.50µm full structure is 260Ω at 2MHz. Consequently, for higher frequencies, the model with a capacitance in parallel to a resistance is not valid any more. Comb structures are not adequate for high frequency measurements therefore the commonly used frequency is between 10 - 100kHz.

The capacitance was also measured versus the bias voltage ranging from -1MV/cm up to 1MV/cm but, as expected, no dependency was observed. Moreover, the capacitance was measured at six different temperatures between 15°C and 200°C, but the changes were below 0.5%.

For a more statistical analysis, the standard normal distribution of the capacitance ratio of air gap to full structures (x-axis) with 0.45µm and 0.50µm line space was drawn, see Fig. 69. The parameter Z of the y-axis is the inverse of the error function with $Z = 0$ indicating the average value, $Z = \pm 1$ meaning one standard deviation above or below average respectively. Each distribution consists of more than 450 data points.

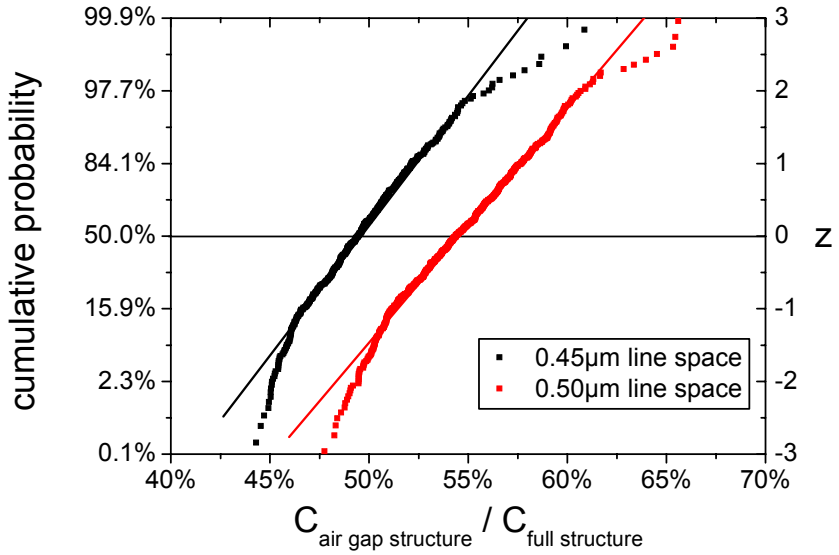


Fig. 69: Standard normal distribution of capacitance ratio of air gap to full structures

It can be seen that except for some low and high outliers, the data follow a standard normal distribution with a standard deviation of roughly ±3%. Table 10 shows the mean values and standard deviations of the capacitance ratio for line spaces of 0.45 - 0.70µm.

Table 10: Mean values and standard deviation of capacitance ratios

Structure - Line space	Mean value of capacitance ratio	Standard deviation
0.45µm	49.6%	±2.8%
0.50µm	53.4%	±3.1%
0.60µm	57.3%	±3.0%
0.70µm	62.2%	±3.3%

The significant reduction of the coupling capacitance to ~50% and the low standard deviation is very beneficial for design. For integration, it is very advantageous that these low-*k* values could be achieved without the use of new materials but with the use of very well-known standard dielectrics like SiO_2 and Si_3N_4.

5.1.2.2 Results of air gaps in a double metal layer scheme

Electrical measurements of the intermetal and interlayer capacitance were performed on comb structures. The comb structures of the first (M1) and the second (M2) metal layer were perpendicular to each other with an IMD thickness of 0.8µm. The capacitance of structures with air gaps and full structures was measured and plotted versus the inverse line space, see Fig. 70. Every data point with its error bar consists of the mean value and standard deviation of 34 dies respectively. The standard deviation across the wafer is low. Therefore, the error bars are only visible for the second metal layer.

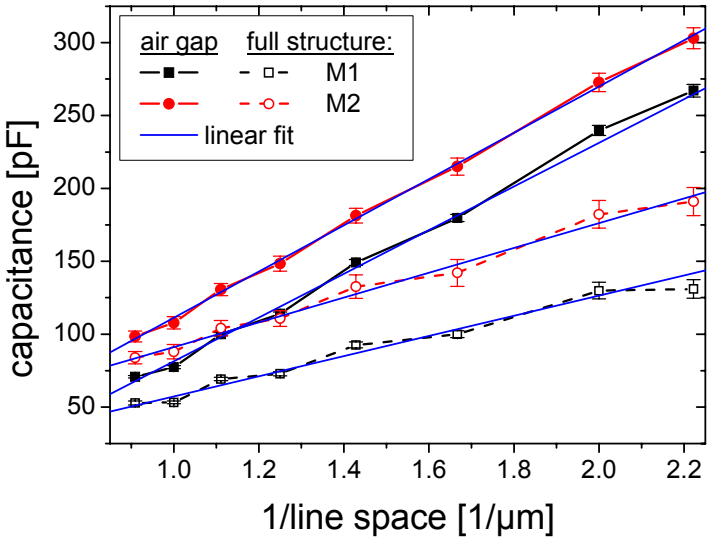


Fig. 70: Capacitance of the first and second metal layer versus 1/line space

As can be seen, the capacitance values follow a straight line in good approximation, which is in agreement with the theory that the capacitance of a plate capacitor is reciprocally proportional to the plate gap. The fitted straight lines of air gap and full structures converge with wider line space. In theory, the straight lines of air gap and full structures should intersect at the origin because of the constant air gap width, the air gaps have less impact on the capacitance at wide line spaces. In practice, the fitted lines do not intersect in the origin because there is also coupling via the other metal level and the substrate, which acts as an offset and moreover the linear fit is only valid for plate capacitors. In our case the fringe fields play an important role and cannot be neglected, but for the fabricated line spaces from 0.45 - 1.0µm the fit is appropriate.

In Fig. 71, the ratios of the capacitance of structures with air gaps to structures without air gaps are plotted. It clearly shows a decrease of the capacitance with decreasing line space as expected for the increasing fraction of air gap volume between the lines. For the most closely spaced lines, a capacitance reduction of approximately 50% – as compared to the full structure – could be obtained, corresponding to $k_{eff} = 2.3$ according to simulations. Higher capacitance ratios were found for the second metal layer (M2), corresponding to a

k_{eff} = 2.8. This is due to the incidentally smaller air gap volume in the second metal layer because of a shallower air gap trench etch. Geometry variations are also responsible that the M1 k_{eff} = 2.3 differs slightly from the value reported above for a single layer k_{eff} = 2.4, see Chapter 5.1.2.1 .Additionally, simulations on the basis of SEM images were carried out, which are, for M1, M2 and for M1 to M2, in good agreement to the measurements.

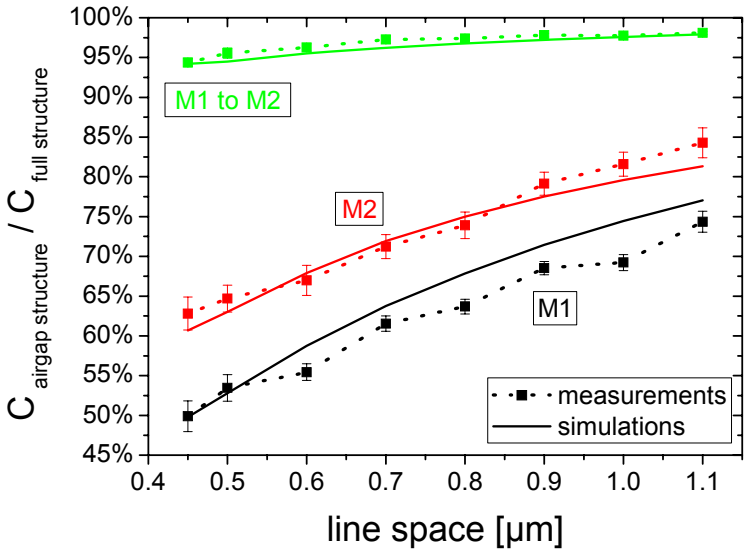


Fig. 71: Measurements and simulations of the capacitance ratio versus line space for first, second metal layer (M1, M2) and interlayer (M1 to M2).

Almost no capacitance reduction is observed for the interlayer coupling between first and second layer. This is easily understood since the air gaps are only located between lines and only a marginal reduction can be achieved due to the passing of the fringe field through the air gaps. Measurements from the first metal layer to the substrate show the same picture. The capacitance reduction in this case is approximately 5 - 10%, corresponding to a k_{eff} = 4.2.

Besides an overall reduction of the parasitic capacitance of a line, air gaps offer an additional advantage in the reduction of crosstalk. Due to their highly hybrid architecture which targets specifically the line to line capacitance C_{line} (see equation 8), crosstalk can be reduced more efficiently. With the use of low-k materials and their more isotropic reduction of k both C_{line} and C_{substr}, are reduced in parallel leading to the same crosstalk behavior without load than without low-k materials. In Table 11, a comparison of the different crosstalk behavior of full, air gap and low-k structures is depicted. $V_{x\text{-}talk}$ was calculated, the capacitance values were simulated and normalized.

Table 11: Comparison of crosstalk of air gap, full and low-k structure

Structure: (normalized values)	C_{line}	C_{substr}	$V_{x\text{-}talk}$
Full (k_{eff} = 4.6)	1	0.6	1
Air gap (k_{eff} = 2.5)	0.42	0.6	0.66
Low-k (k_{eff} = 2.5)	0.55	0.33	1

From a design standpoint of view, air gaps are very beneficial concerning crosstalk, because it is even more important to reduce the crosstalk besides the reduction of the overall coupling capacitance.

5.1.3 Capacitance measurements of self-aligned air gaps

For the self-aligned air gap experiments, the same test chip was used. For comparison purposes, two wafers were processed without air gaps but with the same CoWP capping layer and four wafers with different splits were processed with the self-aligned air gap process, explained in Chapter 4.3.1.

Electrical measurements were carried out on full and air gap wafers. Unfortunately only one third of the dies showed reasonable results. The bad dies showed low resistance across the comb structures, which is attributed to metallic CoWP particles shortening the lines of the comb structures. It has to be mentioned that the CoWP process is not a standard process yet and therefore a lot of optimization is needed. In Fig. 72, the capacitance values of the wafer with air gaps to the one without versus the line space is illustrated. Due to the low sample number and the different wafers, the standard deviation is with 5% relatively high.

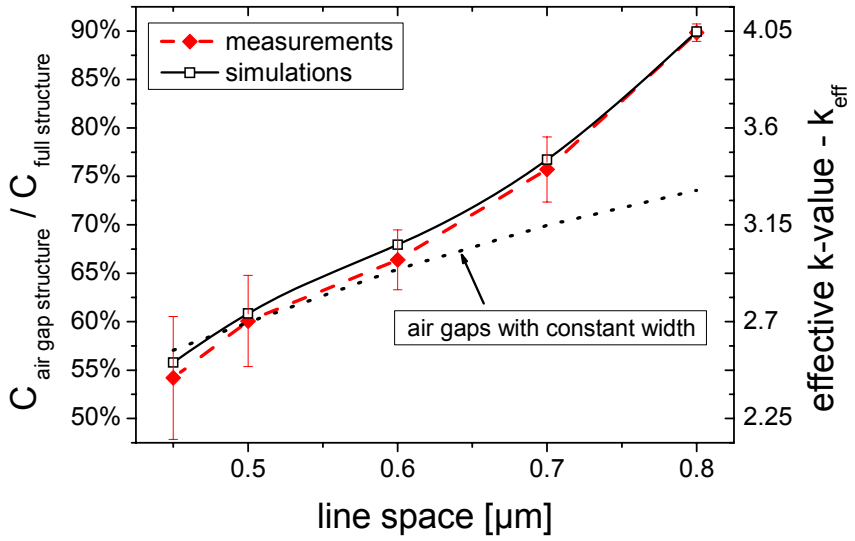


Fig. 72: Capacitance ratio of self-aligned air gaps compared to dense SiO_2

As can be seen, the shape of the graph looks different from the previous ones of the air gaps with additional lithography. This is attributed to the fact that the self-aligned air gaps become smaller with increasing line space, see Fig. 73.

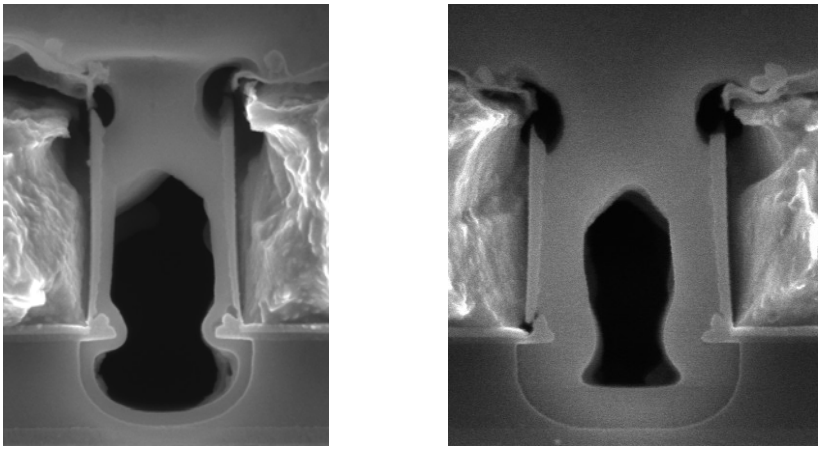


Fig. 73: SEM images of self-aligned air gaps with 0.45, 0.70µm line space

The reason is that, at wider line spaces, the gap between the lines remains open for a longer time and therefore more O_3/TEOS is deposited on the sidewalls. Fortunately for design, it is most important to reduce the capacitance at narrow line spaces. Although the selectivity of the O_3/TEOS process at the self-aligned air gaps is reduced, a k_{eff} of 2.5 could be achieved, particularly because the aspect ratio of the metal lines is higher and the air gaps extend much below the metal lines.

5.1.4 Simulations to demonstrate potential of air gaps

In addition to the calculation of the effective *k*-value, simulations offer a way to optimize geometrical parameters and thus to minimize the capacitance – a task which would be much more cumbersome in experiment. Important parameters to be considered are: metal height, spacer width, air gap height, vertical and/or lateral displacement of the air gap. In each of the following discussions, one geometrical parameter is varied while the others are held constant. Unless noted otherwise, all simulations will be based upon conventional materials such as oxide or nitride.

It has to be emphasized that the k_{eff}-value is independent of the real dimension and is only dependent on the ratios of the dimensions to each other. Moreover, the effective *k*-value does not only depend on the materials used, but also on the geometry and the arrangement of metal lines. The latter aspect is exemplified in Fig. 74 where k_{eff} is modelled for a small number of parallel metal lines separated by air gaps and compared to the data obtained for periodic boundary conditions that means an infinite array of lines and air gaps. The data clearly show that significantly different values are obtained and demonstrate that the computation method must be adapted to the measured patterns. All subsequent simulations are performed with periodic boundary conditions since we assume large, interdigitated comb structures.

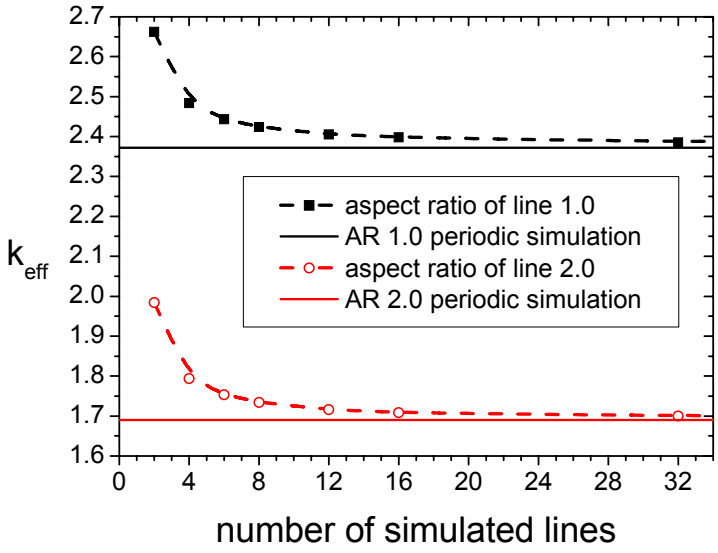


Fig. 74: k_{eff} value of metal lines with air gaps. The horizontal lines indicate the values obtained with periodic boundary conditions, i.e. infinite arrays of metal lines and air gaps.

A first parameter to be studied is the width of the spacers that are typical of our air gap approach. Fig. 75 demonstrates that, of course, the k_{eff}-value decreases when the spacer width is reduced and the air gap volume increases. However, it should be emphasized that k_{eff} does not reach 1 even for vanishing spacers since the fringing fields still contribute to the overall capacitance. The simulations in Fig. 75 were conducted with an air gap height of 1.4 times the metal line height.

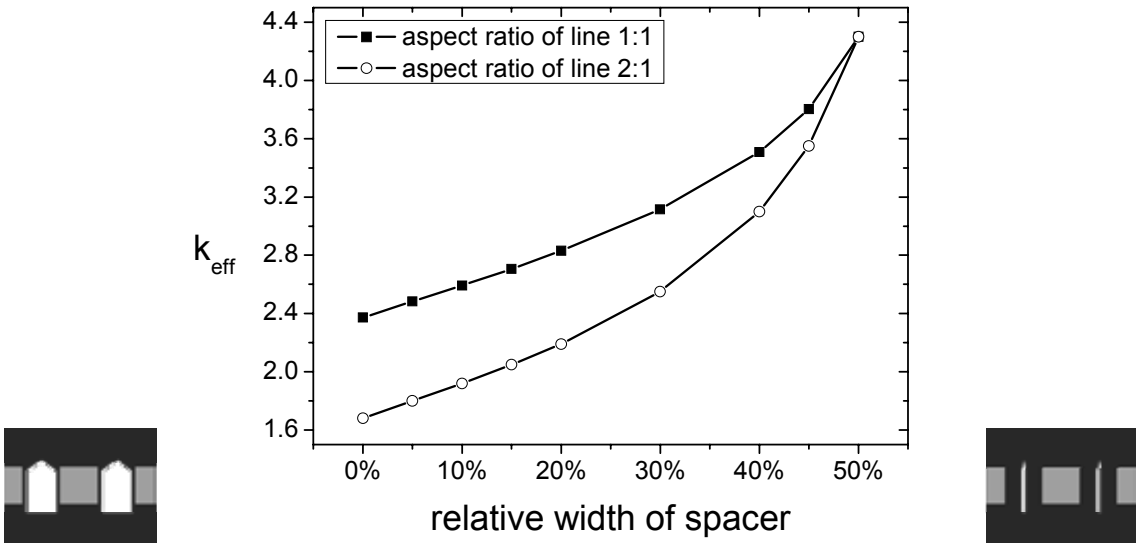


Fig. 75: k_{eff} versus SiO_2 spacer thickness relative to line space.

The pictograms symbolize the geometrical variations performed shown on the x-axis. The dark gray surfaces symbolize SiO_2, the light gray ones the metal lines and the air gaps are white colored.

With further integration, the metal line aspect ratios are expected to increase in the future. Fig. 76 shows that the k_{eff} will decrease for higher metal line aspect ratios. For an aspect ratio of 2, as predicted by the ITRS for 2016 [ITR06], the k_{eff} of air gap structures can be as low as 1.7. This can be understood from the smaller contribution of fringing fields for higher metal lines, an arrangement which better approximates the ideal case of parallel plate capacitors. In Fig. 76, data is shown for two different extensions of the air gap above and below the metal lines.

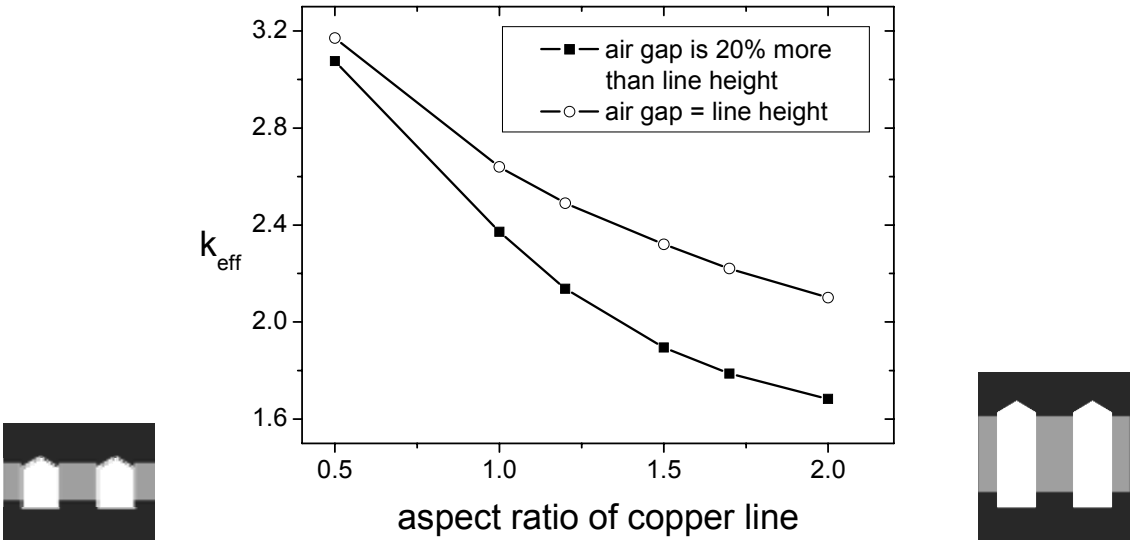


Fig. 76: k_{eff} versus aspect ratio (height / width) of the copper line.

In the next simulations, the air gap between the metal lines will be shifted up and down. This asymmetry can be a consequence of how air gaps are implemented technologically. Fig. 77 demonstrates that k_{eff} is at minimum if the air gap is centered with respect to the metal line. A slight vertical offset is due to the different shapes of air gap top and bottom surfaces in the O_3/TEOS approach.

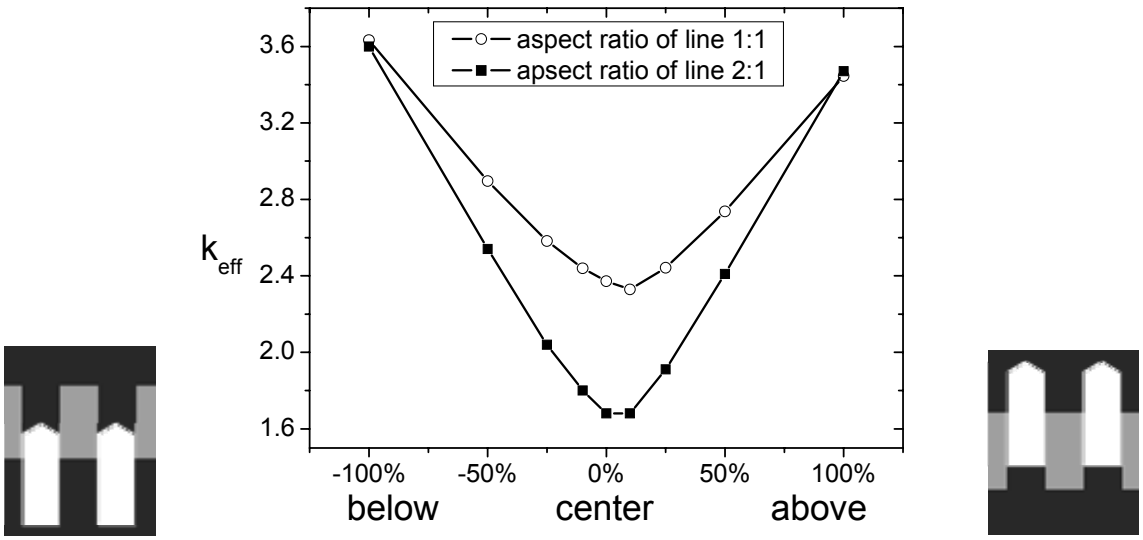


Fig. 77: k_{eff} versus vertical displacement of the air gap, relative to the metal line height.

In general, a 15 % vertical shift results only in a moderate increase of the capacitance. The air gap height is 1.4 times that of the metal line. No effect on k_{eff} is observed when air gaps that are narrower than the line-to-line spacing are shifted horizontally – a situation that may occur in the concept with lithography due to misalignment of the air gap mask.

In Fig. 78, the extension of the air gaps above and below the metal top and bottom surfaces is varied. The extension is relative to the metal line height.

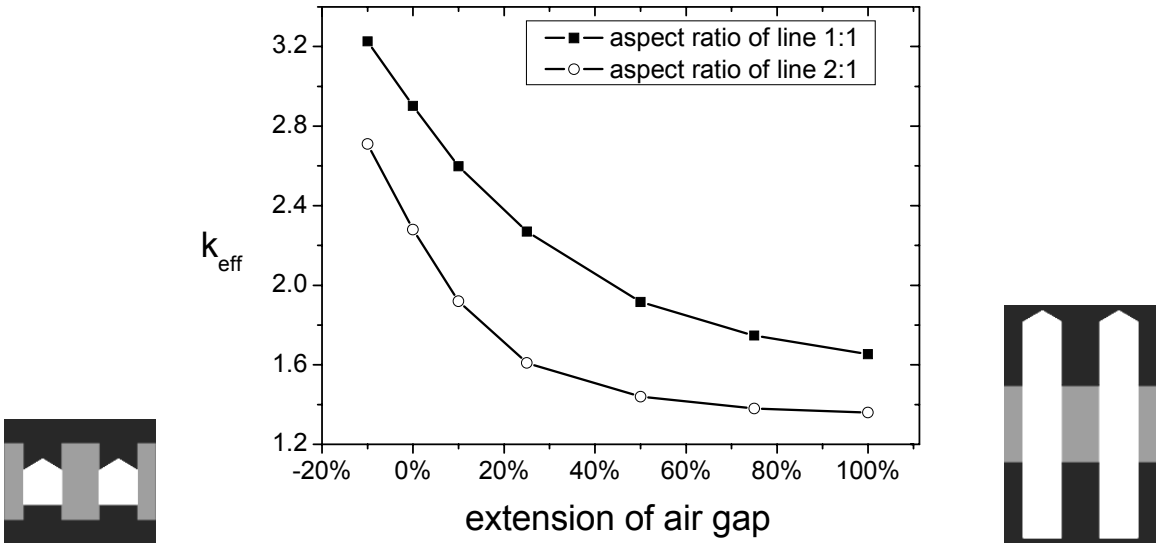


Fig. 78: k_{eff} versus air gap extension above and beneath the line relative to metal line height.

As already mentioned, the air gaps become more efficient if they are higher than the metal lines. In case of high-aspect ratio metal lines, k_{eff} approaches values as low as 1.4 although the large extensions needed are not practical. For more realistic extensions of 20%, k_{eff} would be 1.6.

For future technologies, it seems possible to reach $k_{eff} < 2.0$ by means of air gap technologies even with conventional materials. The final k_{eff} value depends strongly on the geometry which can be optimized by extending the air gaps above and below the metal lines, increasing the aspect ratio of the metal lines, and reducing or leaving out the spacer. Vertical and lateral air gap displacements are uncritical.

A further reduction of k_{eff} is possible if the conventional materials used in our approach are replaced by more advanced low-k materials. Simulations were carried out on a realistic structure with spacers with a thickness of 10% compared to the line space, see Fig. 79. A spacer is necessary in our approach to get a selective growth and to protect the metal lines from oxidation during O_3/TEOS deposition. The aspect ratio of the metal lines is 2:1 and the air gaps extend 20% above and beneath the metal lines relative to the line height. Further on the used spacer and etch stop material was an a-SiC layer with $k = 5$ and a bulk dielectric with $k = 2.2$ (e.g. porous SiLK [Del03]) instead of SiO_2. The air gap closure material is still O_3/TEOS SiO_2.

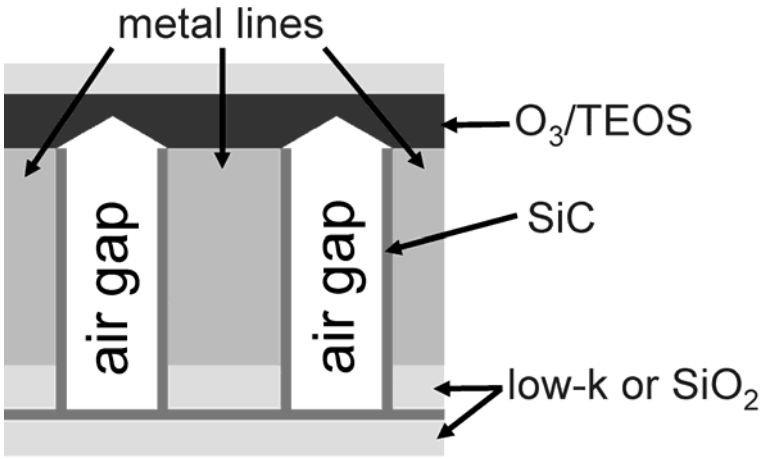


Fig. 79: Schematic of simulated air gap structures with low-*k* materials

In Table 12, the simulation results with low-*k* and SiO_2 material and a-SiC spacers to protect the metal lines are shown.

Table 12: k_{eff} values for air gaps in combination with low-*k* materials

Structure	k_{eff} with low-*k*	k_{eff} with SiO_2
Air gaps with 10% spacer (Fig. 75)	1.72	1.92
Air gaps without spacer	1.51	1.69

Although a very advanced low-*k* material ($k = 2.3$) was used in simulations, only a small further reduction of ~ 0.2 could be achieved. This can be understood since the air gaps and the O_3/TEOS closure layer are in both cases exactly the same. Moreover, since $k = 1$ is the ultimate limit, any improvements of *k* will have less effect on the *k*-value the lower the base value is. As can be seen, it seems possible to reduce k_{eff} to as low as 1.9 with realistic geometries and even with the use of standard dielectrics.

5.1.5 Simulations and measurements of air gaps in 90nm Al RIE metallization

For electrical characterization of the 90nm Al RIE metallization, no reference structures without air gaps were available. Therefore, the measurements were compared to simulated data. The wafers were fabricated in Dresden and patterned with a standard BELTS test chip (back end of line test chip). This test chip comprises comb structures used for capacitance measurements.

In Fig. 80, a SEM image is illustrated in comparison with the distribution of the electrical potential between the conductor lines of a simulated structure. The line in the center is charged with the opposite potential of the adjacent lines. As mentioned before, the air gaps are most efficient when placed where the gradient of the electric potential is high. It can be seen in Fig. 80 that the air gaps in 90nm Al RIE lines cover all critical spots with high field gradient except the bottom part of the air gap and therefore, a low k_{eff} can be expected.

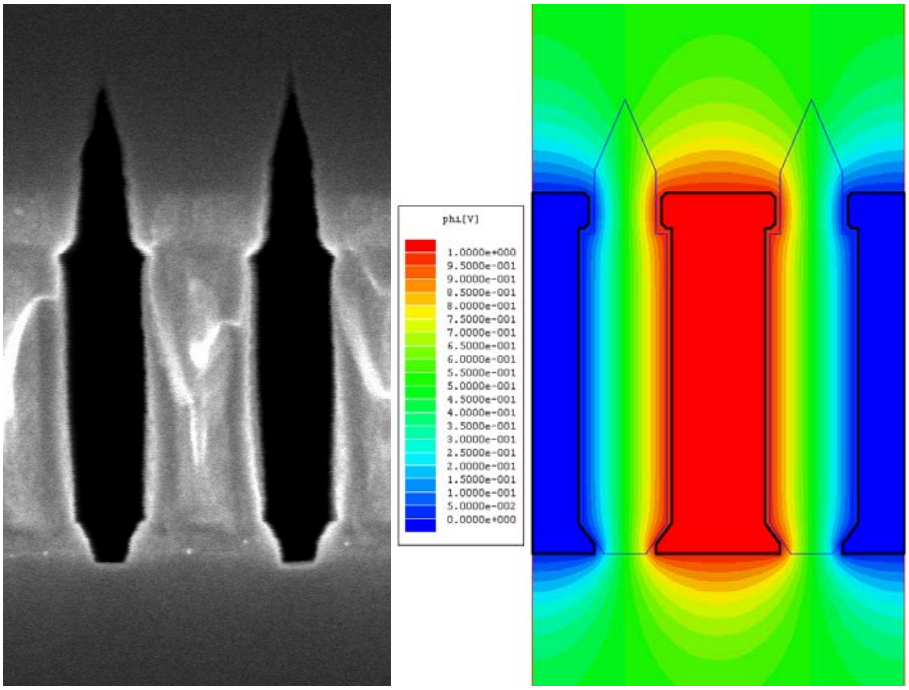


Fig. 80: Left side: SEM cross-sectional micrograph of 90nm air gaps; right side: Electrical potential between Al RIE lines.

In Table 13, the measurements of 40 structures and the simulated capacitance data for air gap and full structures are displayed.

Table 13: Measured und simulated data of air gaps in 90nm Al RIE metallization

Structure	**Measurements (40 samples)**	**Standard deviation**	**C simulated**	**Deviation: sim. – meas.**	k_{eff}
90 nm - air gap	72.40 pF	1.72%	74.14 pF	2.40%	1.77
90 nm - full	(no measured data available)		167.24pF		4.00

The deviation of the measured values to the simulated values is below 3%, which proofs a good matching of the drawn structures to the fabricated structures. Further the standard deviation of the measured 40 samples is below 2%. As can be seen, the k_{eff}-value is as low as 1.77. This is mainly attributed to the very high aspect ratio of 3.7, when including the TiN anti reflection and adhesion layer. Due to the high aspect ratio fringe fields play a minor role for the capacitance and air gaps become very efficient. Another reason for the low *k*-value is that, in contrast to damascene technology, Al RIE metallization scheme does not need high-*k* etch stop or capping layers like Si_3N_4 or a-SiC. For integration, the very low *k*-value and the fact that the structures are built with standard, well-known materials are very beneficial. The drawback for integration is that such air gaps are very critical for via integration. Therefore an additional lithography step will be needed, see Chapter 4.4.3.

5.2 Dielectric reliability performance

The dielectric properties of air gaps in comparison to full structures were also measured on large comb structures, see Chapter 4.1.2. Large comb structures are necessary to achieve a detectable current signal.

5.2.1 Dielectric breakdown of air gap and full structures

The dielectric breakdown measurements were carried out on comb structures by applying a voltage ramp with 60kV/cm steps and a settling time of 300s before the actual measurements is done. Such a long settling time is necessary to achieve steady-state conditions. The relaxation time was measured by applying a voltage and measuring the leakage current characteristic over 10mins. It could be seen in these measurements that the leakage current is clearly saturated after 300s. Due to this long settling time, the measurement time of one single structure takes up to 13h.

In Fig. 81, the current density through the dielectric is depicted versus the applied voltage at the pads. The measurements were performed at air gap and full structures with line spaces ranging from 0.5 - 0.8µm.

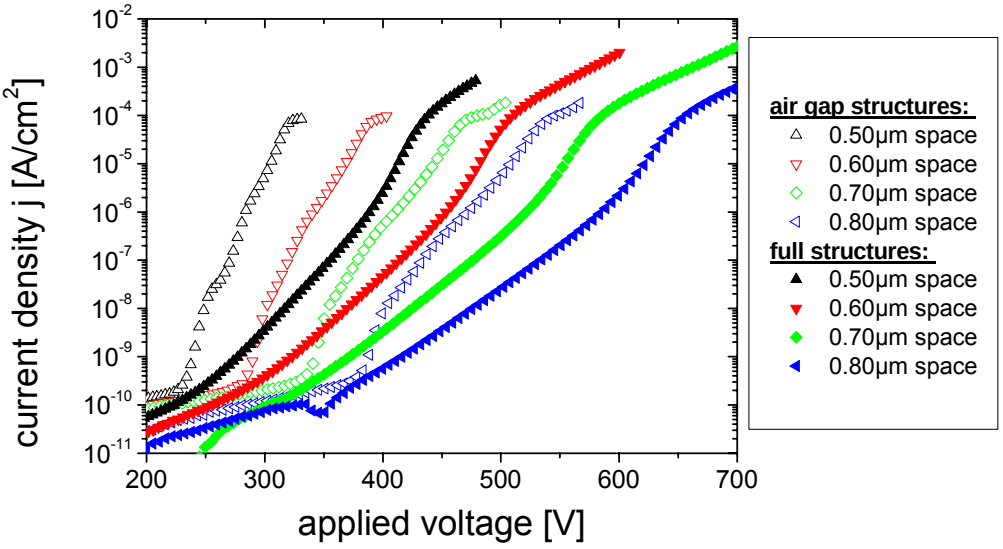


Fig. 81: Current density versus applied voltage in breakdown measurements

When comparing air gap and full structures, it can be seen that the dielectric breakdown voltage for air gap structures is lower for the same metal space. Further, samples with wider line space show higher breakdown voltages. For better comparability, the applied voltage was converted into electric field, see Fig. 82.

For an electric field of less than 3.5MV/cm, the leakage current density *j* of structures with air gaps is up to one decade higher than of full structures. For higher electric fields, the current density *j* of the air gap structures increases faster than of full structures. As a consequence, metal lines with air gaps show a lower breakdown field of E ~ 5 - 6MV/cm compared to a breakdown field of 8.5MV/cm of metal lines in a dense PECVD SiO_2. Conduction paths along the inner surface of the air gaps may be responsible for this

behavior. Etch damage during the air gap trench etch may lead to these conduction paths. Furthermore, air gap structures show a dependence of the electric field on the spacing between the lines, with lower breakdown field strength for narrower line space. Structures with wide line space have thicker spacers between the air gap and the copper lines and therefore rather behave like full structures.

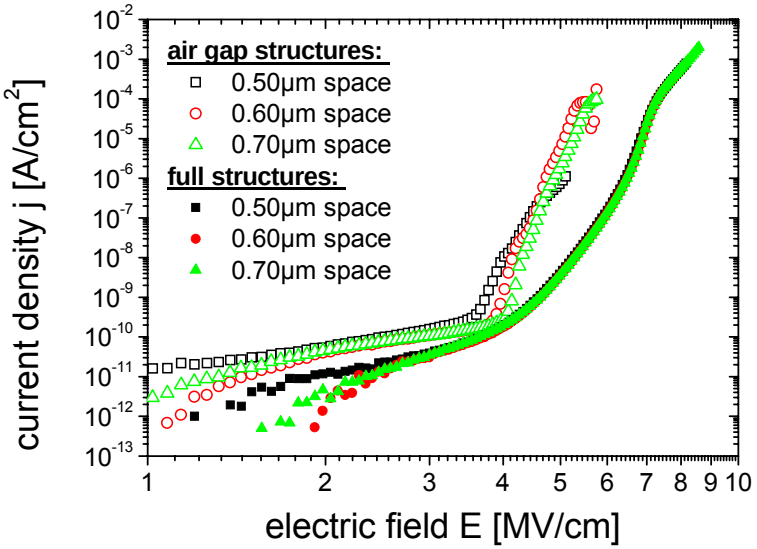


Fig. 82: Leakage current characteristics of air gap structures with different line spaces versus full structures.

For integration, the lower breakdown field of $E \sim 5$ - 6MV/cm is not an obstacle since the maximum electric field in logic or DRAM devices at the end of roadmap will be 0.5MV/cm by 2020 at the 14nm node [ITR06]. Only for Flash, the maximum field strength will be roughly 2MV/cm. In comparison with most low-*k* materials, this is a very good value since most of the low-*k* materials can only withstand 3 - 4MV/cm [Sch03a]. The same applies for the leakage current, which is higher for air gap structures but with $2 \cdot 10^{-11}$A/cm^2 at 1MV/cm one decade less than porous materials [Sch03a].

The breakdown characteristic was also measured between the first and the second metal layer. These measurements show similar results. The leakage current of air gap structures is higher and the breakdown voltage is ~ 25% lower. For integration the breakdown voltage across metal levels is of minor interest since the distance between the layers is ~ 50% more than the minimum vertical line space. For that reason the leakage current is lower, too.

5.2.2 Leakage current of air gap and full structures

To achieve a better statistic concerning leakage current density, measurements were carried out on four different comb structures: full and air gap structures located in either layer one or two each with 0.5µm line space. About 200 samples were measured of each type. The leakage current measurements were performed with a bias field strength of 1MV/cm at an elevated temperature of 125°C, and a relaxation time of 180s. In Fig. 83, the standard normal distribution of the current density data is shown along the x-axis. The parameter Z of the y-axis is the inverse of the error function with $Z = 0$ indicating the

average value, Z = +1 or Z = -1 meaning one standard deviation above or below average, respectively.

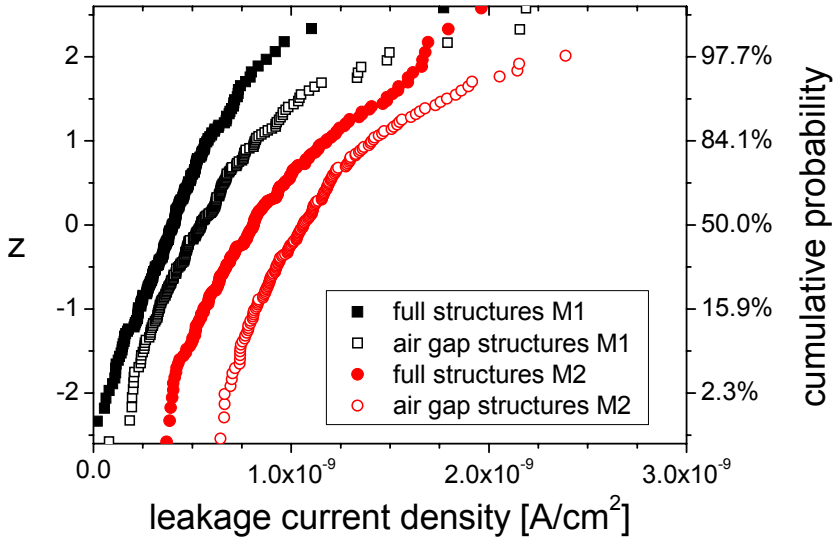


Fig. 83: Leakage current measurements at 125°C, a bias field of 1MV/cm and 180s relaxation time.

It was observed that the leakage current of air gap structures is ~ 30% higher than of full structures. Etch damage of the air gap trench may deteriorate the leakage characteristic because it leads to conduction paths along the inner surface of the air gaps. The leakage current of metal layer 2 may be higher due to conduction paths on the wafer surface. In comparison to low-*k* materials like SiOC, the leakage current levels are with $4 \cdot 10^{-9}$nA/cm^2 for SiOC below that of SiO_2 with $5 \cdot 10^{-10}$nA/cm^2 at an electric bias field of 0.8MV/cm [Yan00]. These results comply with our results with a median leakage current density of $8 \cdot 10^{-10}$nA/cm^2 for M2 at a higher electric field strength of 1MV/cm.

5.2.3 Breakdown voltage of air gaps

To find out more about the lower breakdown voltage of comb structures with air gaps, calculations were carried out to separate the breakdown voltage of the air gaps $V_{air\,gap}$ itself. This was done by calculating the breakdown voltage of the SiO_2 spacer V_{spacer} on the air gap sidewalls and subtraction of that voltage from the total applied voltage V_{app}.

$$V_{air\,gap} = V_{app} - d \cdot E_{full} \tag{34}$$

The breakdown voltage of the spacer was calculated by multiplication of the spacer thickness and the measured breakdown field strength of 8.4MV/cm (Fig. 82) of the full structures. In Table 14 the observed values for air gap structures with different line spaces between 0.45 - 1.0µm are depicted. The values for the overall breakdown voltage V_{app} are mean values out of 3 - 6 measurements.

Table 14: Breakdown voltage of air gaps

Line space of air gap structure [µm]	V_{app} [V]	Spacer width [µm]	V_{spacer} of spacer [V]	$V_{air\ gap}$ of air gap [V]
0.45	129	0.07	59	70
0.5	229	0.12	101	128
0.6	323	0.22	185	138
0.7	406	0.32	269	137
0.8	491	0.42	353	138
0.9	572	0.52	437	135
1.0	643	0.61	512	131

As can be seen, $V_{air\ gap}$, the breakdown voltage of the air gap is with 128 - 138V relatively constant between 0.5 - 1.0µm line space except the 0.45µm structure with 70V. The lower breakdown voltage can be explained by a damaged side wall SiO_2 spacer of the air gaps with 0.45µm line space. When disregarding the side wall spacer at this narrow line space, the air gap breakdown voltage is given by $V_{air\ gap} = V_{app} = 129V$, which is in very good agreement to the breakdown voltages of the structures with wider line space. In theory, the breakdown voltage should be constant for all structures with approximately 120V, see Chapter 2.9.3. This value is in good agreement to our finding of $V_{air\ gap}$ with 128 - 138V.

5.2.4 Temperature dependence of dielectric breakdown

The breakdown voltage was also measured at different temperatures between room temperature and 140°C. In particular, the breakdown field strength at 100°C is relevant for integration since it is the operating temperature. In Fig. 84, the mean value of the breakdown field strength measurements versus the temperature is depicted.

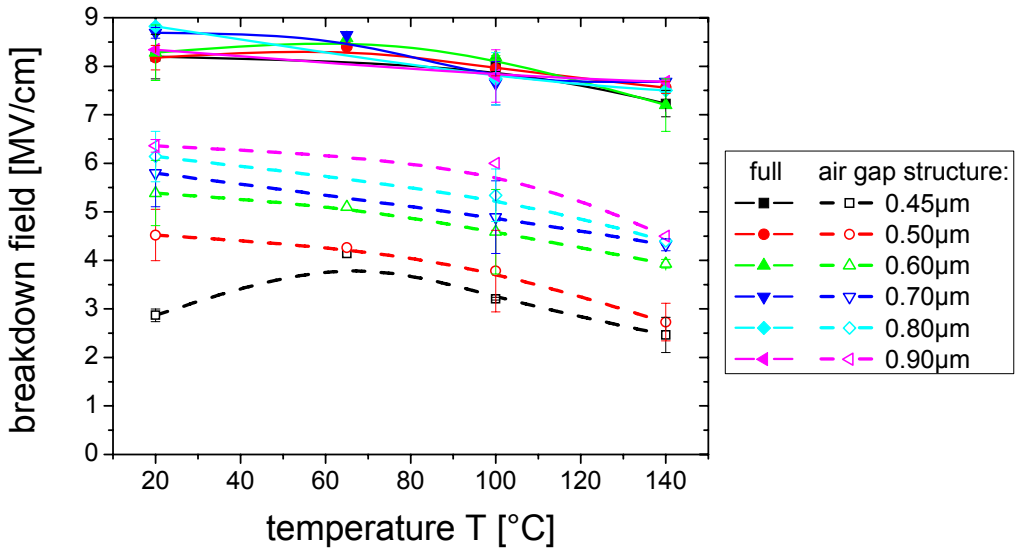


Fig. 84: Breakdown voltage versus temperature

As can be seen, the breakdown field is decreasing with the temperature increasing. This effect originates from thermal breakdown, which occurs above 180K for applied d.c. voltages [Sze81].

5.2.5 Simulations of the dielectric field distribution inside air gaps

However, for integration, the alternating current breakdown voltage is even more important. So far, no distinction has been necessary between a.c. and d.c. breakdown voltage, since in a standard one-material system both breakdown voltages should be approximately the same. In Fig. 85, the simulated field distribution of a full structure is depicted. The high field strength at the edges of the metal lines can be neglected, since the processed structures exhibit less sharp edges and therefore, no such severe field spikes will occur. The white rectangles in the simulated distributions represent the metal lines.

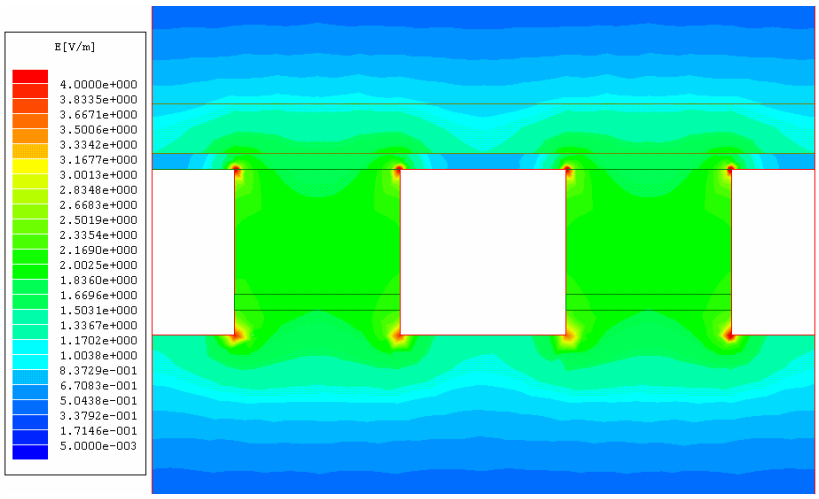


Fig. 85: Distribution of the electric field within a full structure

In Fig. 86, a simulation of the field distribution of an air gap structure is depicted.

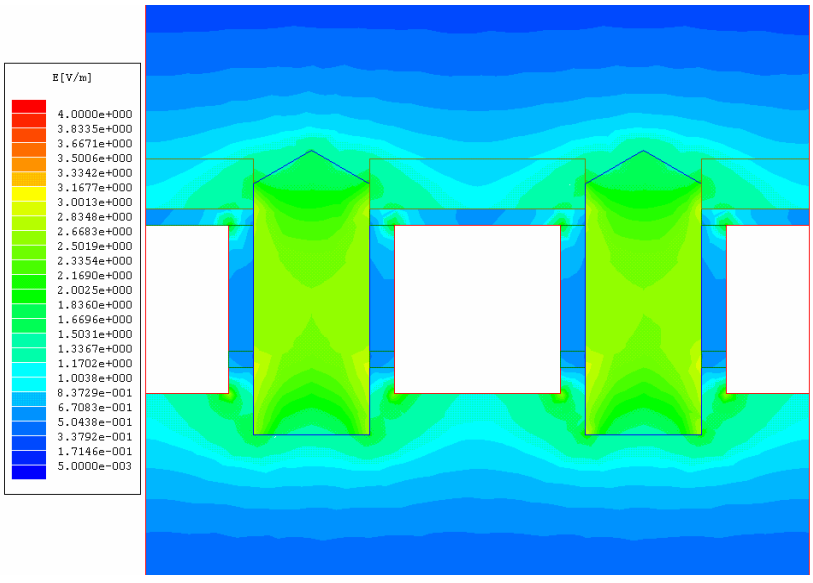


Fig. 86: Distribution of the electric field within an air gap structure

Here, the field is 30 - 40% higher than in the case of the full structures. When more than one material is in between the two capacitor electrodes, a field enhancement inside the material with the lower *k*-value occurs. This field enhancement can be explained by drawing a simple equivalent circuit of the structures, see Fig. 87. This circuit acts as a simple a.c. voltage divider. When applying a.c. voltage to this circuit, the largest voltage drop will be at the smallest capacitor. In the air gap case, this will be the capacitor with the lowest *k*-value, which is the air gap. It can easily be calculated that the electric field across the electrodes in C_{spacer} will be lower, the one in $C_{air\ gap}$ higher than in C_{full}, see Chapter 2.8.4.

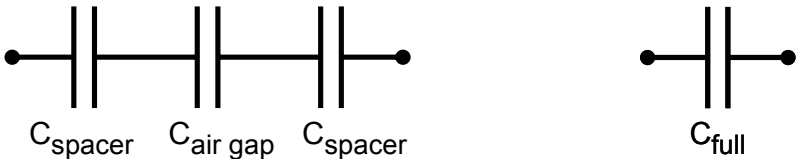


Fig. 87: Simple equivalent circuit for air gap and full structure

This effect leads to an even lower overall breakdown voltage of air gap structures, when applying a.c. voltage, and may also lead to a higher leakage current.

5.2.6 Conduction mechanism

The conduction mechanisms Frenkel-Poole or Schottky emission could be determined from the slope of the transformed *IV*-characteristic. In Fig. 88, a transformed *IV* breakdown characteristic is depicted with the square root of the electric field *E* as x-axis and the logarithm of the leakage current density divided by the electric field *E* as y-axis. The breakdown characteristic was measured on air gap and full structures with different line spaces. For additional details about the calculations and transformation, see Chapter 2.9.2 (equations 19-22).

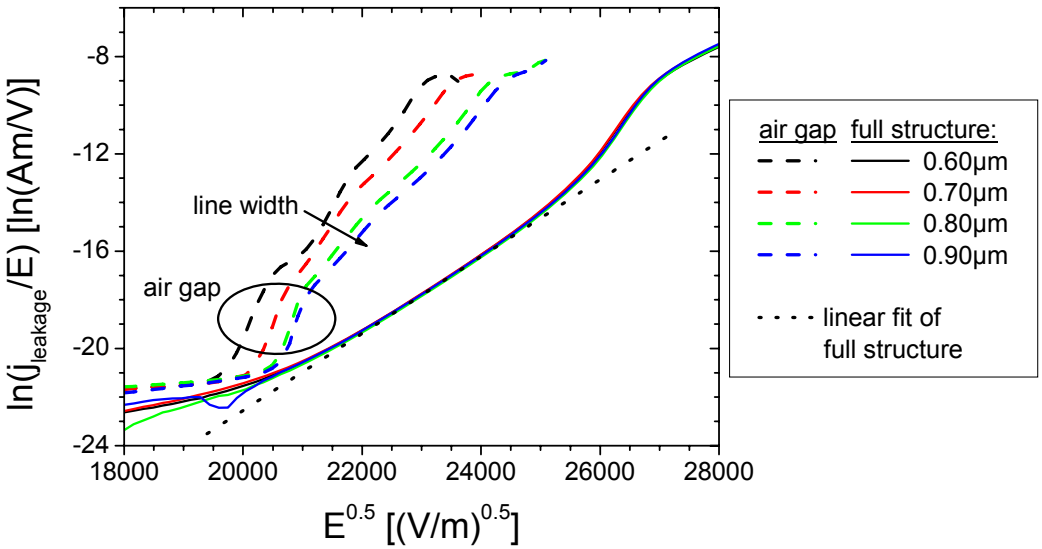


Fig. 88: Frenkel-Poole plot of an air gap and a full structure at 25°C

It can be seen that the dispersion of the Frenkel-Poole characteristic of the full structures is very narrow and consequently the line space has no influence. In general, it has to be mentioned that a higher slope in the characteristic directly translates into a lower *k*-value. For that reason, the graphs of the air gap structures showed a steeper slope at the air gap breakdown, see Fig. 88, which occurs at around 4MV/cm ($E^{0.5} = 20000$). At higher electric field strengths a flatter slope was observed when the air gap and the spacer conduct the leakage current. Moreover, the Frenkel-Poole characteristics of the air gap structures depend on the line space with a flatter slope at wide line spaces and steeper ones at narrow line spaces, leading to a higher Frenkel-Poole *k*-value for wide spaces, which is in very good agreement to the capacitance measurements.

For further investigations of that effect, more measurements at line spaces between 0.45 - 0.9µm at two different temperatures were conducted. In Fig. 89, the calculated Frenkel-Poole *k*-value for two temperatures is depicted versus line space.

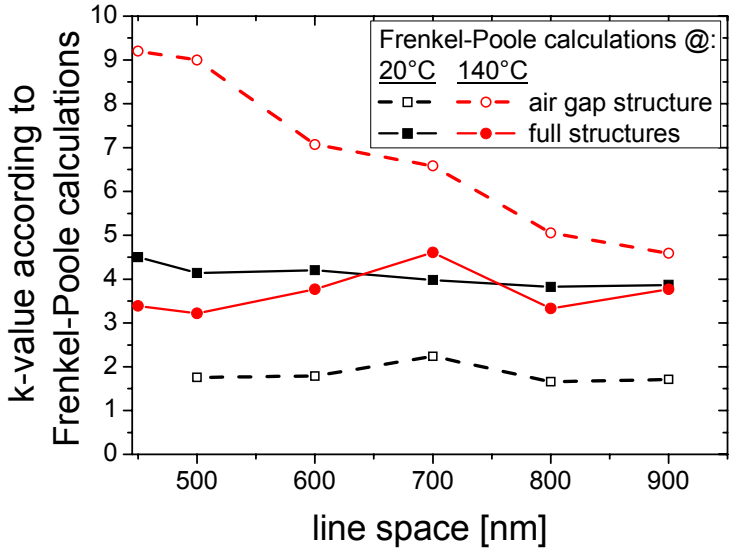


Fig. 89: *k*-value after Frenkel-Poole versus line space and temperature

It can be seen that the Frenkel-Poole *k*-value of the full structures is with 3.5 - 4.5 close to the real *k*-value. Therefore, Frenkel-Poole is the main conduction mechanism in full structures. The Frenkel-Poole conduction mechanism was observed above 4MV/cm. In comparison, this conduction mechanism usually occurs above 1MV/cm in the case of interconnects embedded in a porous ULK matrix [Guj05].

The behavior of the air gap structures is comparable to full structures for a temperature of 20°C. There, the calculated Frenkel-Poole *k*-value is approximatly 2, which is relatively close to the real *k*-value of 2.3 - 2.7. It has to be mentioned that this method is not desired for evaluating the *k*-value, but to determine the conduction mechanism. Therefore, the Frenkel-Poole *k*-value deviates from the real *k*-value.

When raising the test temperature to 140°C, the observed Frenkel-Poole *k*-value is up to four times higher than the real *k*-value. This leads to the conclusion that Schottky emission is the dominant conduction mechanism at this temperature because the Schottky emission *k*-value is always approximately four times higher than the Frenkel-Poole value, see Chapter 2.9.2. This change in the dominant conduction mechanism can be explained by

the quadratic temperature dependence of the Schottky emission. Therefore, the Schottky emission is not obvious at low temperature, but plays a major role at higher temperatures.

5.3 Resistance and resistivity of interconnects with air gaps

The via chain resistance of air gap and full structures was measured on structures comprising 200 via contacts. The resistivity of the metal lines was measured on 1mm long lines embedded in an array of 20 lines. The resistivity was calculated from the resistance values measured at two different temperatures, 25°C and 150°C. These measurements were only carried out on air gap structures fabricated with additional lithography, see Chapter 4.2.1. In Fig. 90, the distribution of the via chain measurements is plotted.

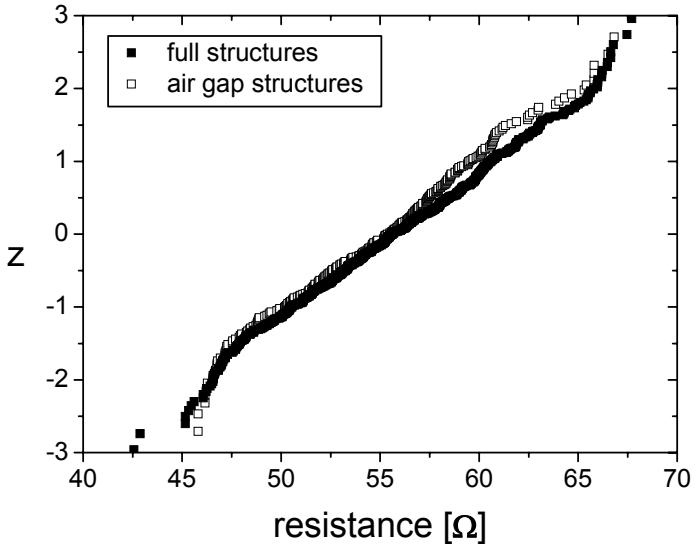


Fig. 90: Distribution of the resistance of a 200 contact via chain of air gap and full structures

As can be seen, the difference between air gap and full structures is only marginal. This result shows that copper is not oxidized during the O_3/TEOS deposition and no vias interfere with air gaps. It has to be mentioned that the used via chain structures comprised wide landing pads for via integration to avoid interfering of vias with air gaps.

For resistivity investigations, the resistance of 1mm long lines was measured at two temperatures and the resistivity was calculated. The distribution of the resistivity of air gap compared to full structures is shown in Fig. 91. For clarity, only the data for M2 is drawn and more data points are available for full than for air gap structures.

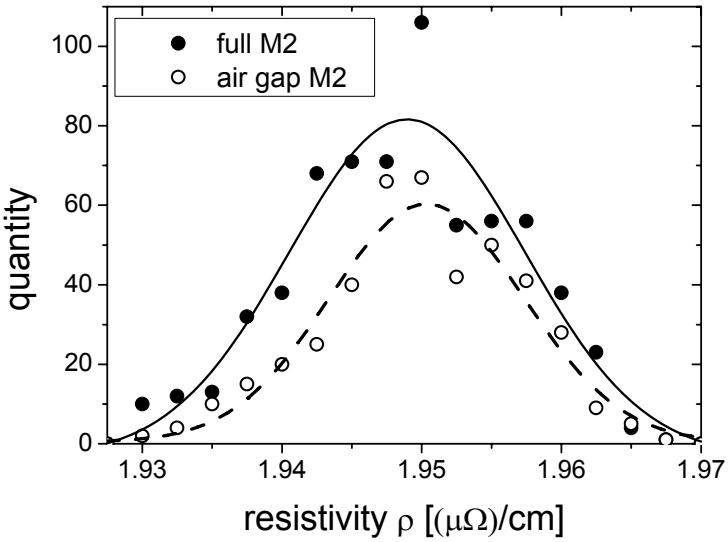


Fig. 91: Distribution of the resistivity of air gap and full structures in the second metal layer (M2)

It can be seen that there is only a marginal difference between the best Gaussian fit of air gap and full structures, consequently air gaps have only marginal influence on the resistivity of the copper lines. This behavior is beneficial for integration since a higher resistivity neither resistance would be a major drawback for air gaps.

5.4 Reliability against electromigration

The fabricated air gap structures were also subjected to tests of the electromigration properties. The electromigration tests were carried out on 1mm long line structures with 0.45µm and 0.5µm line space embedded in an array of not connected dummy lines, see Chapter 4.1.4. The fabricated wafers were diced and the 370 samples comprising the structures were packaged and bonded. Such a large number of samples was necessary to obtain a large statistical base for electromigration analysis. For each sample under test, the resistance was recorded as a function of stress time. The resistance rises sharply when an electromigration failure occurs. The time to failure (TTF) was defined as the stress time at which the resistance increased by 20% of its initial value. However, in some cases with full structures, a decrease of the resistance was observed, which will be explained below. Out of these TTF values and the stress conditions, the lifetime can be extrapolated, see Chapter 2.9.1.

5.4.1 Electromigration results

For comparison purposes, four different structures, air gap and full samples with 0.45µm and 0.5µm line space, were subjected to the same test conditions. In order to obtain a larger statistical base and since the subgroups did not show any significant difference, samples with both 0.45µm and 0.5µm line space were evaluated together.

The electromigration stress conditions were $T = 225$ - 300°C with a bias current density j of 30mA/µm² for extraction of the activation energy E_a, see Fig. 92.

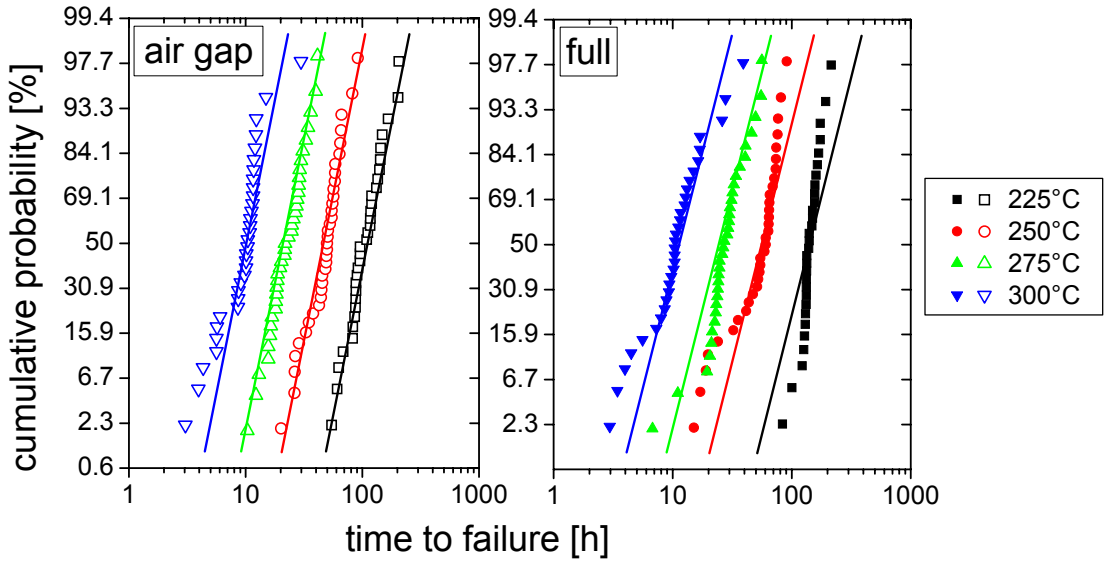


Fig. 92: TTF values versus stress temperatures for E_a-analysis of air gap (left) and full structures (right) at a current density of 30mA/µm².

The time to failure is very similar for both air gap and full samples, although the air gaps show a tighter distribution, see Figs. 92, 93. For extraction of the current density exponent *n*, the current densities *j* were varied between 15 - 45mA/µm² at a stress temperature of 250°C, see Fig. 93. It has to be mentioned that self-heating due to the high current densities was not taken into account. The self-heating effect leads to 10 - 15°C higher temperatures of the metal lines. The difference of the self-heating between air gap and full samples is with 0.5°C only marginal.

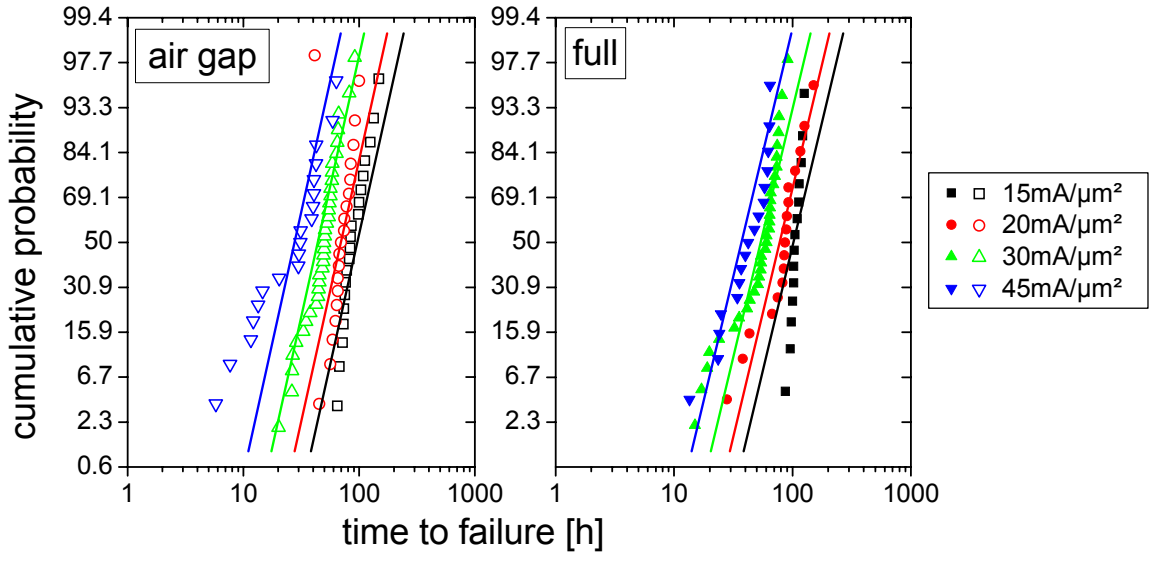


Fig. 93: TTF values versus applied current density for n-analysis of air gaps (left) and full structures (right) at 250°C stress temperature.

From the linear fits of these graphs, the activation energy and current density exponent was extracted, see Chapter 2.9.1, equation 16. By extraction of E_a and n, only small differences between the groups were noticed, see Table 14.

Table 15: E_a and n values of air gap and full structures

Structure	Activation Energy E_a [eV]	Current Density Exponent n	Lifetime at 105°C, 5mA/µm^2 [a]
Air gap	0.79 ±0.05	1.1 ±0.2	10.6
Full	0.83 ±0.07	0.9 ±0.2	9.6

The E_a-value of air gaps is a little bit lower than of the full structures, but the n-value is higher. The higher E_a value of full structures compensates almost the decreased n value, leading to comparable lifetimes. The electromigration lifetimes were extracted according to a failure probability of $5 \cdot 10^{-5}$, a current density of 5mA/µm^2 and an operating temperature of 105°C. The current density and operating temperature was chosen according to the ITRS predictions for 2010, see Chapter 2.1. The absolute lifetime is marginally higher for air gaps, but is within experimental error due to the relative small number of samples and process fluctuations due to our non-standard processes.

In future technology nodes, the current density increases by a factor of 1.8 every node. Therefore, it is very promising that air gaps do not weaken the electromigration resilience. Especially for design and integration, this fact is very important. To learn more about the failure mechanism of the samples, microscope and SEM images were taken, see following chapter.

5.4.2 Post electromigration analysis

After electromigration testing the chip packages were opened and the tested lines were inspected by in-depth analyses with optical microscope and SEM.

5.4.2.1 Void formation during electromigration stress test

The common failure mechanism in electromigration test is conducted by void nucleation and growth leading to a resistance increase, which is detected as failure of the metal line. Void growth itself is conducted by the strong electron flow, leading to a transport of copper atoms along the copper line. Void formation was observed for air gap and full structures. Fig. 94 shows a microscope image of lines damaged by voids after electromigration stress tests.

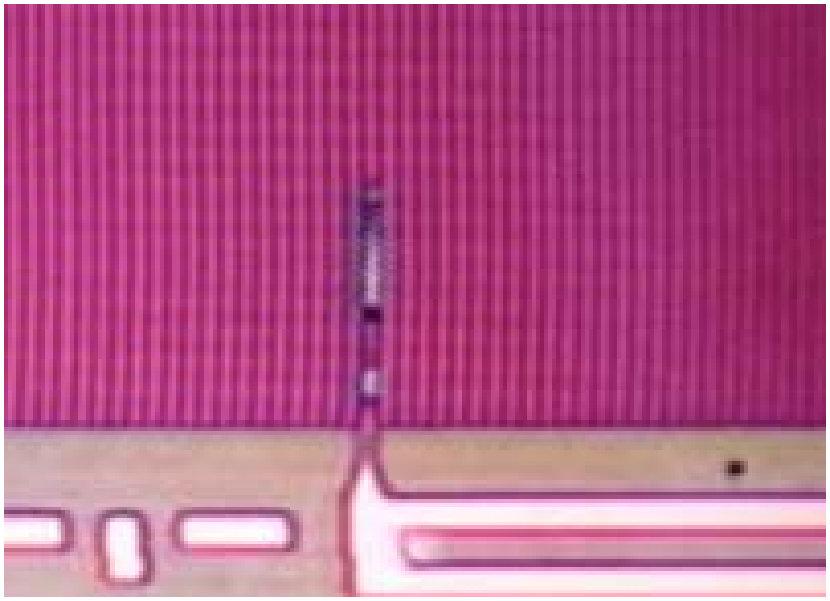


Fig. 94: Microscope image of metal lines with voids after electromigration stress

SEM analysis was done to get a more detailed picture of the damaged spots. Therefore, the small samples, which are only 2x2mm^2 in size, were removed from the package, etched in HF-solution to remove the thick passivation SiO_2 layer on top of the lines and then dry etched to remove the Si_3N_4 capping layer. For dry etching a special handle wafer with a recess was used to handle the small samples inside the process tool for 6" wafers. Fig. 95 shows a SEM image of voids after electromigration stress tests.

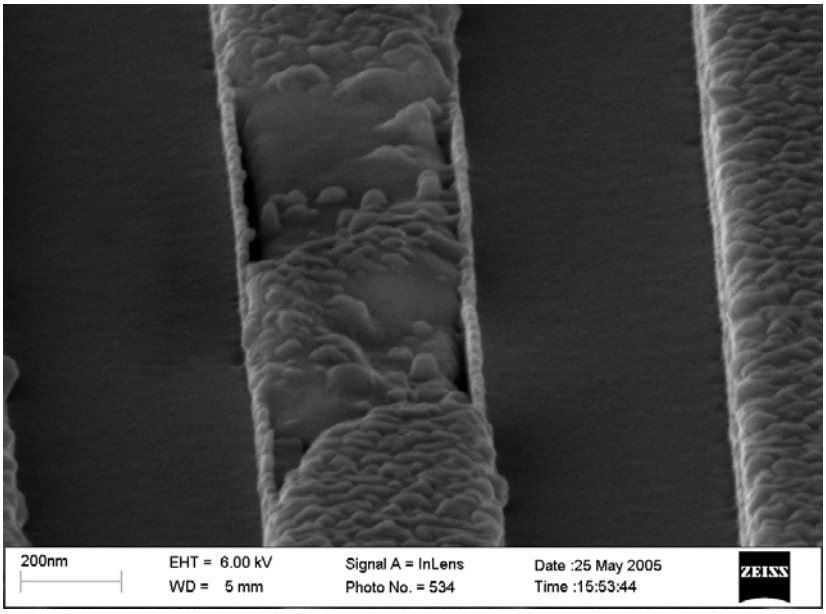


Fig. 95: SEM micrograph of voids after electromigration stress tests

It can be seen that parts of the copper of the metal line are removed, thinning the cross section of the copper line. The void formation usually takes place at the interface between

copper and the Si_3N_4 capping layer, since there, the adhesion is much lower than to the TaN/Ta barrier layer, facilitating the void growth. This weak spot is well known in electromigration stress testing and therefore new, better capping materials like self-aligned metal barriers are under consideration [Ish04].

5.4.2.2 Extrusion of copper during electromigration stress test

The second failure mechanism is extrusion of copper which is basically an accumulation of the residual copper of the void growth. In case of the full structures, these extrusions can easily be seen in microscope inspection because they form bright, light reflecting spots, see Fig. 96.

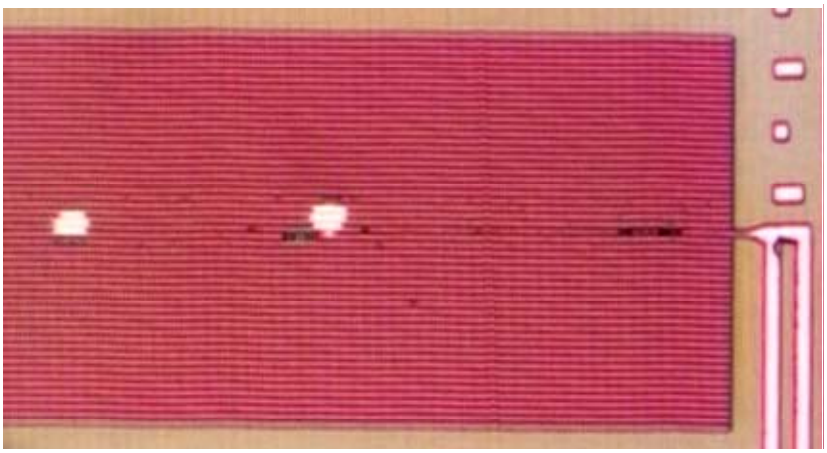


Fig. 96: Microscope image of a full structure with extruded copper during electromigration stress tests

To learn more about the exact location of the copper extrusion, SEM preparation and images were done on this sample, see Fig. 97.

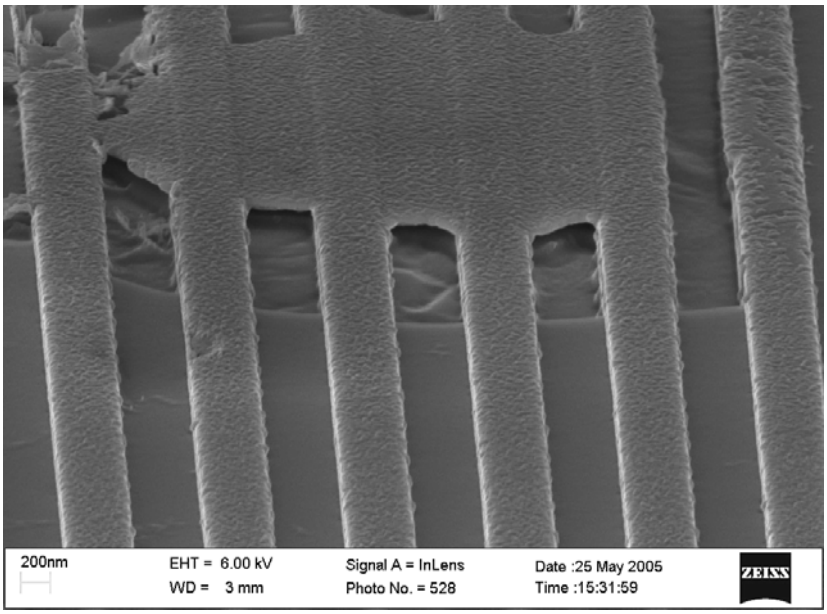


Fig. 97: SEM micrograph of typical failure mode for full structures in electromigration tests.

It can be seen that in the case of the full structures, copper extruded at the upper part of the metal line along the SiO_2 / Si_3N_4 interface. Towards the end of the lifetime, a high compressive stress is known to build up, breaking the Cu / Si_3N_4 interface and forcing a thin Cu layer into that delaminated interface [Arn01a]. If more than one of these shorts to neighboring Cu lines occurs, it can be seen in a resistance decrease because then the test line is shunted with at least one neighboring line. This behavior also explains the decrease of the resistance of some full structures during electromigration stress test, as mentioned at the beginning of this chapter. As a consequence, the TTF values were edited in a way that also a drop in resistance was counted as a fail. In general, these massive extrusions are not common in standard production chips but may be enhanced by our non-standard SiO_2 dielectrics, which are not optimized for electromigration

While a resistance drop due to extrusions was quite common for full structures, it was only rarely observed for air gap structures. There, the extruded Cu accumulated in the large air gap volume and the fail was due to voiding of the stressed line, see Fig. 98. Shorts to neighboring lines were avoided due to the dielectric spacers between the air gap and the metal lines.

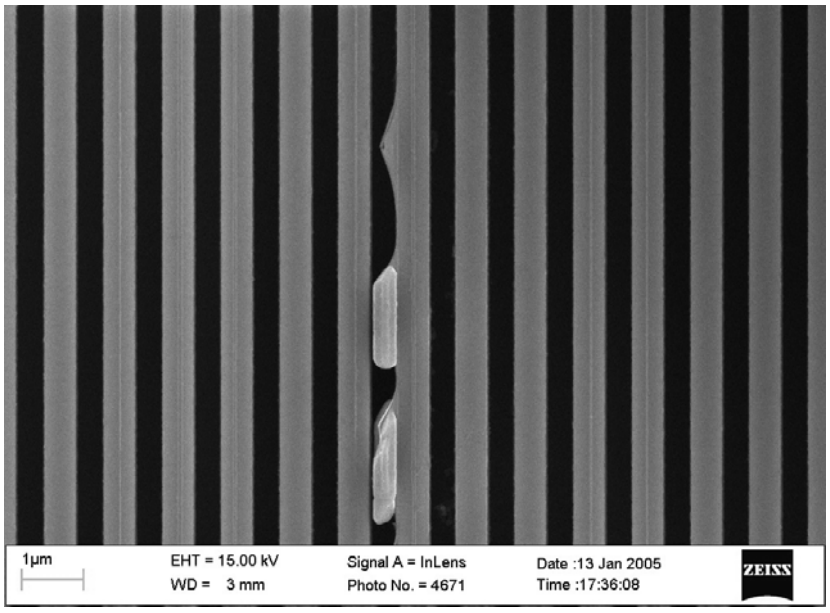


Fig. 98: SEM micrograph of typical failure mode for air gaps in electromigration tests.

Despite of these totally different failure mechanisms, both air gap structures fabricated with the selective O_3/TEOS process and structures with dense SiO_2 films show comparable electromigration lifetimes. It has to be mentioned that for more precise electromigration stress tests, extrusion monitors are necessary to detect copper extrusions inside the air gaps. Extrusions can be detected during electromigration stress tests by applying an electric field to the neighboring lines and simultaneous monitoring of the leakage current. Unfortunately, our test chip did not comprise pads to the neighboring lines and therefore extrusion monitoring was not possible. Further, it has to be mentioned that the electromigration tests were carried out on single metal level structures without vias therefore large copper reservoirs at the pads are available for copper extrusions. The vias usually serve as blocking point for the copper transport since there is the intermediate

barrier layer, which prevents copper transport across the via. Consequently, electromigration tests of air gap structures with vias will most likely fail due to voiding and show less extrusions.

5.5 Thermal conductivity with air gaps

The thermal properties of the dielectric stack are becoming more and more important due to increased joule heating because of the strong increasing current density [ITR05]. The biggest disadvantage of using gas dielectrics is their poor thermal conductivity. The heat transport perpendicular to the metallization layers should not be affected seriously, since the thermal conductivity of Cu is much higher than that of any dielectric material and therefore the heat-flow in this direction is mainly through the metal lines. However, the heat flow within the layer will be restricted by the presence of air gaps. This will mainly have an effect on metal lines loaded with a high current in an otherwise cool environment. Two different types of test structures were used to investigate the self-heating and thermal properties of the dielectric surrounding the wires.

5.5.1 Measurements of thermal properties

5.5.1.1 Self-heating measurements

The first test structures consisted of individually connected wires embedded in arrays of unconnected, floating wires with different line spaces and for comparison as full or air gap structures. The 1mm-long center line of these structures was loaded with high current densities and the temperature increase recorded by measuring the line resistance. Fig. 99 shows the measurements of the temperature increase versus line space. In order to better compare the different lines with slightly different resistances, the temperature increase for a fixed electrical power of 0.2W is shown.

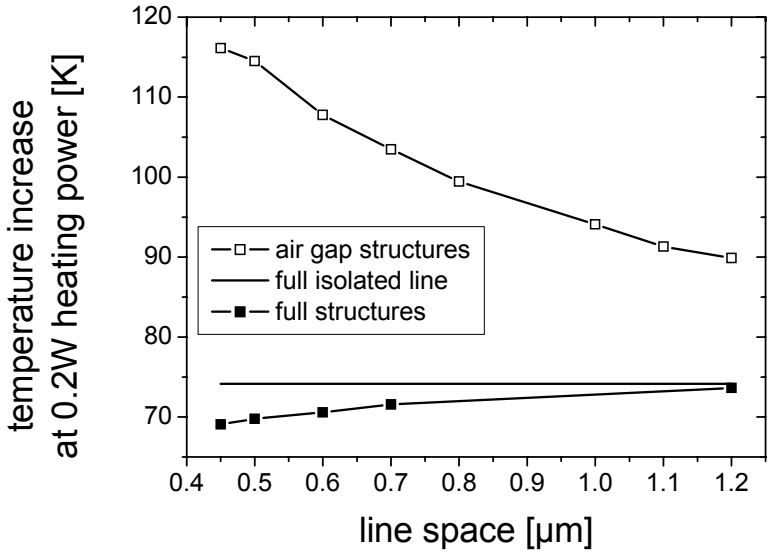


Fig. 99: Temperature increase for an applied electric power of 0.2W for lines surrounded with and without air gaps

The electrical power of 0.2W translates into an extreme high current density *j* of approximately 160mA/µm² = 16MA/cm². These very high current densities are necessary to get stable measurement results and minimize noise. Regardless of the high current density no resistance increase due to electromigration was observed when measuring the resistance before and after the current stress. For reference purposes, the horizontal line indicates the temperature increase of an isolated line embedded in solid dielectric without neighboring Cu lines. In the case of full structures, the neighboring Cu lines act as heat spreaders, which are more efficient for narrow line spaces. Consequently, the temperature increase of embedded full structures is up to 9% less then that of the isolated line. For large line spaces, the temperature of the center line approaches that of the isolated line. For air gap structures, the temperature increase is much higher, since the low thermal conducting air gaps impede the heat flux away from the stressed line. The air gap width is the same for all structures, so the larger the line space, the more solid dielectric is available between the lines for heat conduction, and therefore the lower is the temperature increase for the stressed line. For a line space of 0.5µm, the temperature increase (115K) of air gap structures is 65% higher than of full structures (70K).

5.5.1.2 Thermal crosstalk measurements

The second test structure consisted of two lines in parallel for a length of 3.62mm designed to measure the thermal flux between the metal lines, also referred to as thermal crosstalk. Here, one of the lines, the aggressor line, is loaded with a current which was increased from 0 to 20mA. The self-heating of this wire is monitored by its resistance increase. In parallel, the resistance of the second neighboring, the victim line is measured using a constant low current of only 100µA. The low current guarantees that the victim line is not self-heated and only heated by the aggressor line during crosstalk measurements. All structures are available as full or air gap structures and line spaces ranging from 0.45 - 1.2µm. The structure and measurement conditions are schematically shown in Fig. 100.

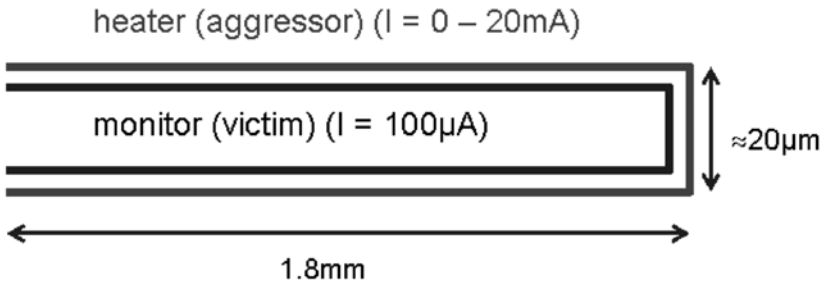


Fig. 100: Layout and test conditions for crosstalk measurements

Fig. 101 shows the temperature characteristic of such measurements of aggressor and victim lines for air gap and full structures with 0.5µm line space versus aggressor power. As can be seen, with an air gap between the neighboring lines, the aggressor line becomes hotter, whereas the victim line stays cooler in comparison with the full structure. The temperature difference of the aggressor and the victim lines is about 5K, but the difference between the full and the air gap structure is with 12% less evident than at the first experiment because here only one air gap impedes the heat flux away from the aggressor line. The increased temperature, due to Joule heating, in the interconnect stack is critical

for integration, since it can result in reliability problems, including enhanced electromigration.

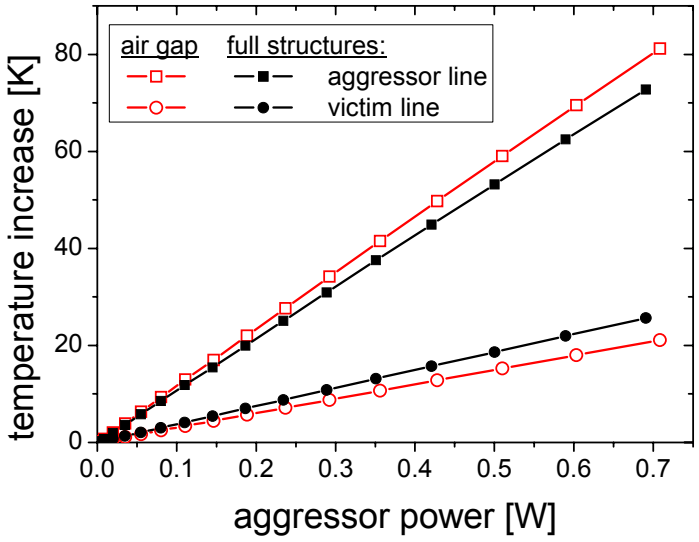


Fig. 101: Temperature increase within 0.5µm crosstalk structure versus electrical power applied to aggressor line

5.5.2 Simulations of thermal crosstalk

To confirm the experimental data, extended numerical simulations using the finite elements software package FEMLAB were carried out. The simulations have been undertaken using FIB cross-sections of the measured structures and literature values of the thermal conductivity material parameters as input. In the simulation program, the structures were drawn according to the cross-sections and every layer was characterized with its thermal conductivity coefficient. In Table 16, the literature values of thermal conductivities of various materials at room temperature are given.

In gases, heat is conducted by the molecules themselves, so gases with lighter and faster molecules, like helium, are better heat conductors than heavier gases, like nitrogen or air. Obviously, the more concentrated the gas, the better the thermal conductivity. In our case the gas in the air gaps is most likely a mixture of TEOS decomposition byproducts, helium, the TEOS carrier gas and oxygen. The pressure inside the air gaps will most likely be approximately 600Torr, the pressure of the deposition process. For simulations, the thermal conductivity value of air was used for the air gaps. As seen from this data, the thermal conductivity of SiO_2 is about 10 times better than of porous materials (porous SiLK) and more than 30 times higher than that of air. Thermal conductivity of porous materials depends on temperature, pressure, and strongly on the porosity respectively density [Str02]. The thermal conductivities of metals are much higher (up to 3800 times) than for dielectrics.

Table 16: Thermal conductivity of various materials [Del03]

Material	**Thermal conductivity coefficient λ [W/cmK]**	**Dielectric permittivity k**
Air (O, N)	0.00025	1.00059
He	0.001	1.0
Porous SiLK	0.0011	2.2
H_2	0.0018	1.0
a-SiC (amorphous)	0.0030	4.5
SiCOH (Black Diamond)	0.0036	2.9
Si_3N_4 - CVD	0.0058	7.5
SiO_2 - CVD	0.009 - 0.01	4.2
Al_2O_3	0.2	9.1
TiN	0.29	
Ta	0.54	
Si	1.24	
W	1.67	
Al	2.4	
Cu	3.9	

To compare the measured data to simulations, the air gap and full structures were drawn in FEMLAB and the temperature distribution was calculated, see Fig. 102. The left simulation shows the temperature distribution of two metal lines in dense dielectric, the right one comprising air gaps. The local temperatures are shown as color shades; the structures are indicated as black contours.

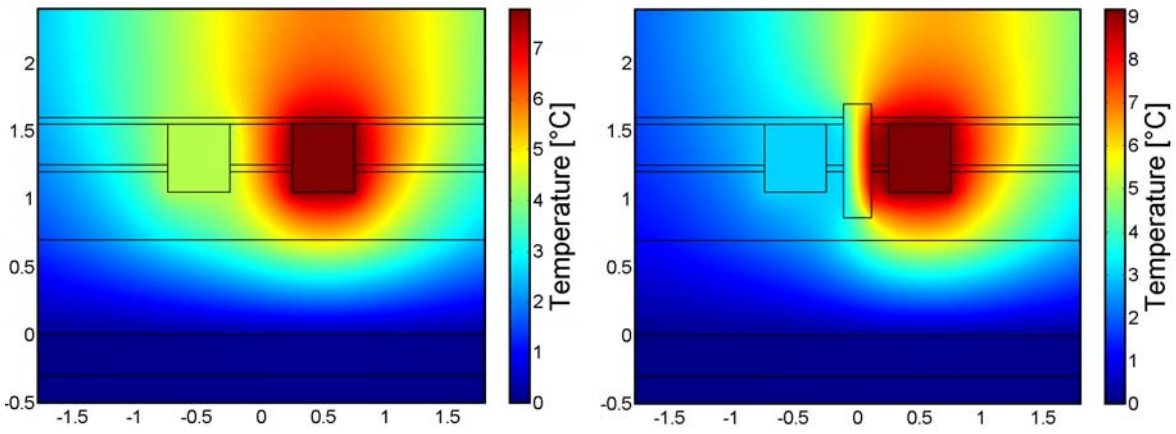


Fig. 102: Temperature distribution of simulated crosstalk structures with 0.5µm line space of full (left) and air gap (right) structures

It can be seen that the heat flow from aggressor to victim line is inhibited by the presence of the air gap resulting in a lower temperature of the victim line and a higher temperature of the aggressor line, see right side of Fig. 102. For full structures (Fig. 102 left), the thermal conduction between the lines is better due to the dense material and, therefore, the

aggressor line is 15% cooler and the victim line is hotter. It has to be mentioned that both graphs in Figure 102 have different temperature scales.

The simulations and measurements were carried out on structures with different line spaces and compared to each other. In Fig. 103, measured and simulated values of the temperature increase versus the line space are depicted for air gap and full structures. All measurements were performed with electrical power of 76mW loaded on the aggressor line.

Good agreement between experiment and simulation was found except for one sample with 0.5µm line space because of partially filled air gaps due to parasitic O_3/TEOS deposition at the metal barrier sidewalls. For that reason, this structure behaves almost like a full structure. This can happen when the air gap lithography is misaligned and consequently, the barrier is uncovered during the air gap trench etch process, see Chapter 4.2.3.

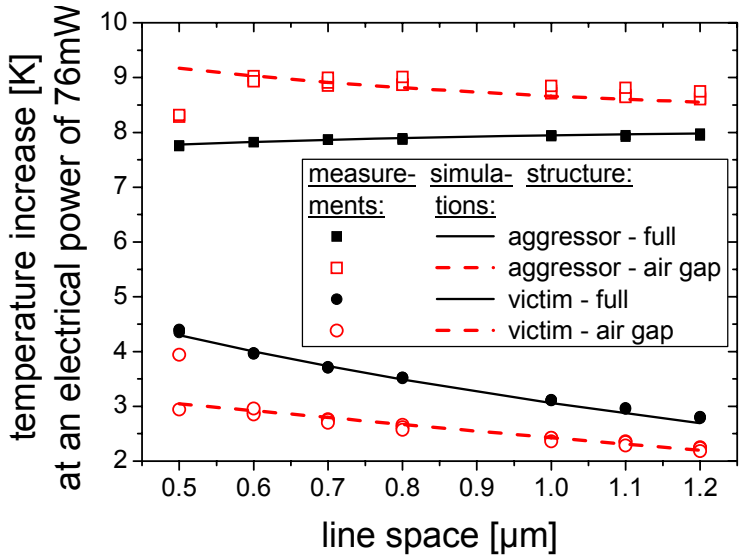


Fig. 103: Comparison of measurements and simulations of temperature increase within crosstalk structures for different line spaces

Finally, simulations with 45nm wide metal lines were performed to evaluate the effect of air gaps in future technology nodes. In Fig. 104, the temperature distribution within the structure is depicted. Here, the worst case for air gaps compared to full structures of only one aggressor line surrounded by a cool environment and a second metal level underneath was simulated. It has to be mentioned that here the temperature scale of both simulations is equal. The x- and y-axes are in µm-scale.

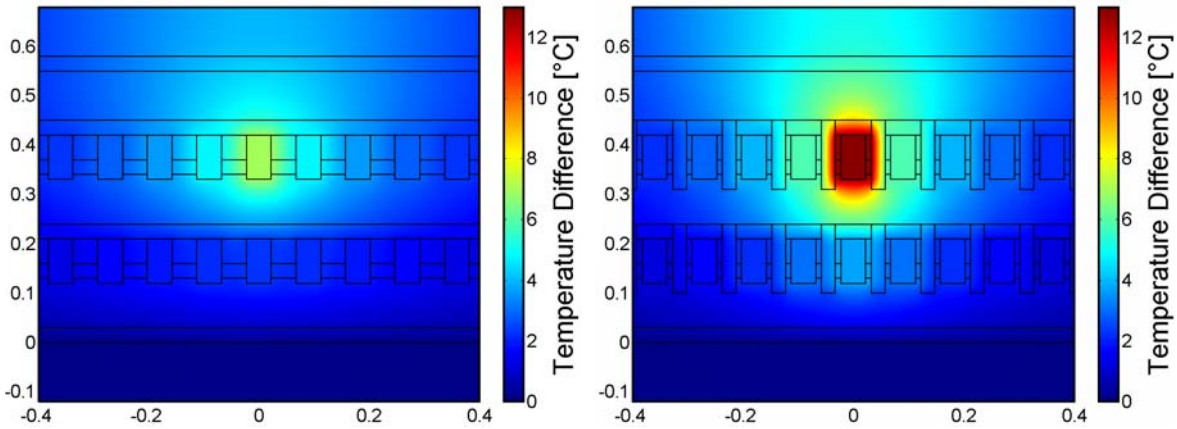


Fig. 104: Temperature distribution within 2-metal layer 45nm interconnect structures of full (left) and air gap (right) structures

Obviously, the heat flow from aggressor to victim line is massively inhibited by the presence of the air gaps resulting in an 80% increased self-heating. It has to be mentioned that for this comparison the metal lines were embedded in SiO_2 ($k = 4.2$) and Si_3N ($k = 7.5$). When comparing the air gap simulations to metal lines integrated in porous low-k materials with a very low heat conductance, like porous SiLK ($k = 2.2$) as dielectric and SiC ($k = 4.5$) as capping and etch stop layer, the temperature difference is enormous, see Fig. 105 (notice the different temperature scale).

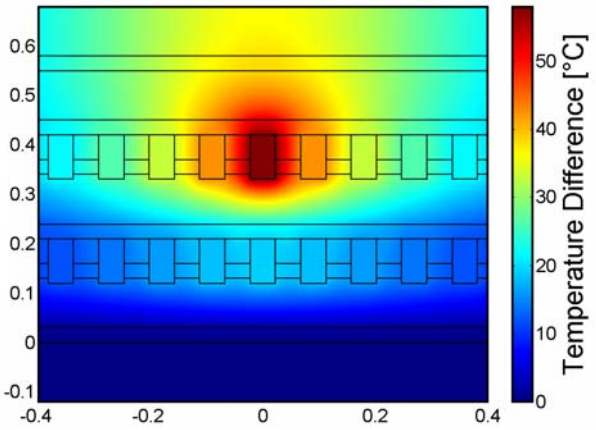


Fig. 105: Temperature distribution within 2-metal layer 45nm interconnect structures of full structures with porous low-k materials

Obviously, there is a major difference of the temperature increase of the loaded metal line of the air gap and full structure with porous low-k. The main difference between the two integration schemes is that due to the higher thermal resistance of the porous material the heat flow to the substrate is impeded and therefore the self-heating and heating of the material in lateral direction is enormous. It has to be mentioned that these simulations were performed without accounting vias and bond pads, which also contribute to the overall heat flow from the metal lines to the substrate respectively heat sink. In a real chip, the difference between the different integration schemes would therefore be slightly less evident.

For integration, this is a big advantage for air gaps, since due to the good conducting interlayer dielectric, a good heat transport to the substrate is guaranteed. Table 17 shows the temperature increase values of full structures with different dielectric materials as ILD or IMD materials in comparison to air gap structures with standard SiO_2, Si_3N_4 materials.

Table 17: Temperature increase of metal line structures with different materials

Structure	k_{eff}	Intermetal dielectric (IMD)	Interlayer dielectric (ILD)	Capping and etch stop layer	Temperature increase of loaded metal line [K]
Full standard	5.4	SiO_2	SiO_2	Si_3N_4	7.0
Full capping	4.3	SiO_2	SiO_2	a-SiC	9.3
Full low-*k*	3.8	SiOC (Black Diamond)	SiO_2	a-SiC	11.4
Full porous	3.6	porous SiLK	SiO_2	a-SiC	12.2
Air gap	2.8	SiO_2	SiO_2	Si_3N_4	12.9
Full porous	3.0	porous SiLK	porous SiLK	a-SiC	57.8

Obviously, the ILD material plays a major role in self-heating since all generated heat has to be transported through the ILD material to the substrate. This effect can best be seen when looking on simulations with porous SiLK, where a more than five times higher temperature can be seen when the SiO_2 ILD is substituted by the porous low-*k* material. It can be seen that the air gap structure has a marginally higher self-heating than the porous SiLK with the SiO_2 ILD but features a 22% lower *k*-value and moreover has the lowest $k = 2.8$ of all simulated structures. The integration scheme with porous ILD and IMD material is comparable to the gas dome system, where Wade thought of the integration of high thermal conduction paths in the form of metal columns to dissipate heat away from the metal lines [Wad99]. Especially in high performance logic devices where a low *RC*-delay is necessary and therefore porous low-*k* materials are needed, the low thermal conductance of these materials is a severe drawback.

In fact, numerical simulations involving air gap interconnect systems show that temperature rises are higher than those for homogeneous SiO_2 dielectrics and are much lower than of homogeneous low-*k* materials. Advantageous for air gaps is their highly hybrid structure compared to low-*k* integration schemes, which allows good vertical heat transport from the metal lines to the substrate because the interlayer dielectric is good heat conducting SiO_2 and inhibits horizontal heat transport due to the presence of air gaps. Especially when thinking of future three dimensional integration schemes, this feature is very valuable, since there the only way to dissipate heat is in vertical direction.

6 Conclusion

As a novel alternative to interconnect dielectrics, air gaps were investigated in detail, both in theory and in practice. In this work, simulations and calculations were performed to determine and evaluate the effective *k*-value and thermal properties of air gap structures. Further, single processes were developed, such as the electroless deposition and plasma cleaning to improve selectivity of the O_3/TEOS process. The selectivity of the selective O_3/TEOS process was analyzed on various materials and with different cleaning steps. The overall process of the self-aligned air gap process with damascene copper lines and RIE tungsten metal lines was developed and optimized. A variety of lots for development were fabricated for reliability investigations, the self-aligned process, air gaps in tungsten RIE metallization, selectivity analysis and a two metal layer integration scheme. The air gap structures were analyzed by SEM inspection and electrical measurements of the capacitance, resistance, leakage current, thermal properties, resistivity, reliability tests and breakdown voltage were performed.

The feasibility of air gap integration by the selective O_3/TEOS process in various integration schemes could be shown. In detail, it was found that the selective O_3/TEOS process is very sensitive to surface contaminations, surface preparation and etch residues. Therefore, a very good cleaning of the surface is mandatory. In future, optimization of the selective O_3/TEOS process, process tool and the cleaning processes is necessary to improve the process stability, control and sensitivity.

The additional lithography step of the air gap layer is a major disadvantage, since the alignment is very critical and the lithography mask is needed in the same resolution as the metal lines, which makes that process expensive and demanding. For that reason, a large number of experiments were performed to develop a simple self-aligned process. The drawback of self-aligned air gap processes in general is the risk of opening and filling air gaps with metal during via integration and a high topography between metal lines with wide spaces. To overcome these issues, a self-aligned process with a simple, low-resolution lithography is proposed to mask out vias and wide spaced lines. Moreover, the mechanical strength, for instance under bond pads can be improved by excluding these areas from air gaps. Another solution would be to integrate air gaps only where the capacitance reduction is most important like in data buses or signal lines, clock signals to reduce the power dissipation or in noise sensitive lines. The drawback of this approach is a more complex chip and layout design and more design rules. This approach has been shown recently with air gaps by a non-conformal dielectric deposition and would be interesting for the self-aligned air gaps by selective O_3/TEOS deposition as well.

Air gaps exhibit some outstanding electrical properties, especially in terms of reduction of capacitance and reduction of crosstalk. It could be shown that air gaps due to their hybrid structure can reduce the crosstalk between neighboring lines more effectively than a homogeneous low-*k* material. Furthermore, it could be demonstrated, that air gaps with additional lithography offer a significant reduction of k_{eff} down to 2.3 even when standard materials such as SiO_2 and Si_3N_4 are used. The self-aligned air gaps showed effective

k-values of 2.5 in the case of copper damascene metallization and 1.8 in the 90nm Al RIE case. Simulations of the effective *k*-value of air gap structures were performed to evaluate geometrical and material effects. By optimizing the geometry, it seems possible to reach $k_{eff} < 2.0$ for future technologies by means of air gap technologies even with conventional materials. The final k_{eff} value depends strongly on the geometry, which can be optimized by extending the air gaps above and below the metal lines, increasing the aspect ratio of the metal lines, and reducing or leaving out the spacer. Vertical and horizontal air gap displacements are not critical. A further reduction of k_{eff} can be achieved by combining low-*k* materials and air gaps such as SiCN or SiOF, while still avoiding the material inherent integration risks of soft or porous low-*k* materials.

Air gaps exhibit properties for leakage currents and dielectric breakdown, which are comparable or even better to structures embedded in low-*k* dielectrics. The leakage current of air gaps is higher than those of structures in dense CVD SiO_2 and can best be described by the Frenkel-Poole mechanism at room temperature and by the Schottky emission at 140°C. With 4 - 5MV/cm the breakdown voltage is lower than of dense CVD SiO_2, but still higher than the breakdown voltage of most low-*k* materials. The breakdown field is well above the maximum predicted field of 0.5MV/cm by 2020 for logic or DRAM and also above the 2MV/cm for Flash technology, as predicted by to the ITRS. The leakage current is uncritical and is comparable to or lower than that of ultra-low-*k* materials.

Air gaps integrated in a standard processing scheme and fabricated utilizing selective O_3/TEOS process show electromigration lifetimes comparable with those obtained for structures with solid SiO_2 films. Despite the different failure mechanisms, the activation energy and current density exponent of Black's equation are almost similar for air gap and full structures. In the air gap case, the lines fail due to voiding in the copper lines by concurrent agglomeration of the copper in the air gaps. The full structures fail, due to massive extrusions leading to shorts with neighboring lines. The failure mechanisms were analyzed by microscope and special preparation of the samples for SEM inspection. The fact that air gaps in SiO_2 dielectric do not degrade the electromigration lifetime is very promising for future technology nodes.

The effect of air gaps on the thermal properties of the interconnect stack was measured and simulated. The self-heating measurements show that structures comprising air gaps show higher temperature increases than those for homogeneous SiO_2 dielectric. Simulations are in good agreement to the measurements and it could be shown that the self-heating of homogeneous low-*k* materials is up to 4 times higher than that of air gap structures. Advantageous for air gaps is their highly hybrid structure, which allows good vertical heat transport from the metal lines to the substrate because the interlayer dielectric consists of the thermally well-conducting SiO_2 and only horizontal heat transport is inhibited due to the presence of air gaps. Especially when thinking of future three dimensional integration schemes, this feature is very valuable, since there good vertical heat conduction is mandatory.

All in all, these features suggest air gaps as an attractive alternative to low-*k* or ultra-low-*k* materials. The highlight of air gaps is their very low effective *k*-value in spite of the use of standard dielectrics. These dielectrics exhibit some of the best combinations of mechanical, electrical, and chemical stability properties desired for metallization integration. Unfortunately, due to an additional lithography, etch process, cleaning step and CMP planarization step the processing cost of air gaps is higher than for conventional SiO_2-based integration schemes. In comparison to ultra-low-*k* materials, air gaps may be a

competitive alternative, since these materials also need additional processes, like UV-curing steps, cleaning steps and various processes have to be modified for instance line and via trench etch, barrier deposition and dielectric CMP. Especially in the future with metal lines with higher and higher aspect ratios, air gaps will be a very effective solution to reduce capacitive coupling.

Appendix A: Die layout on wafer and mask layout

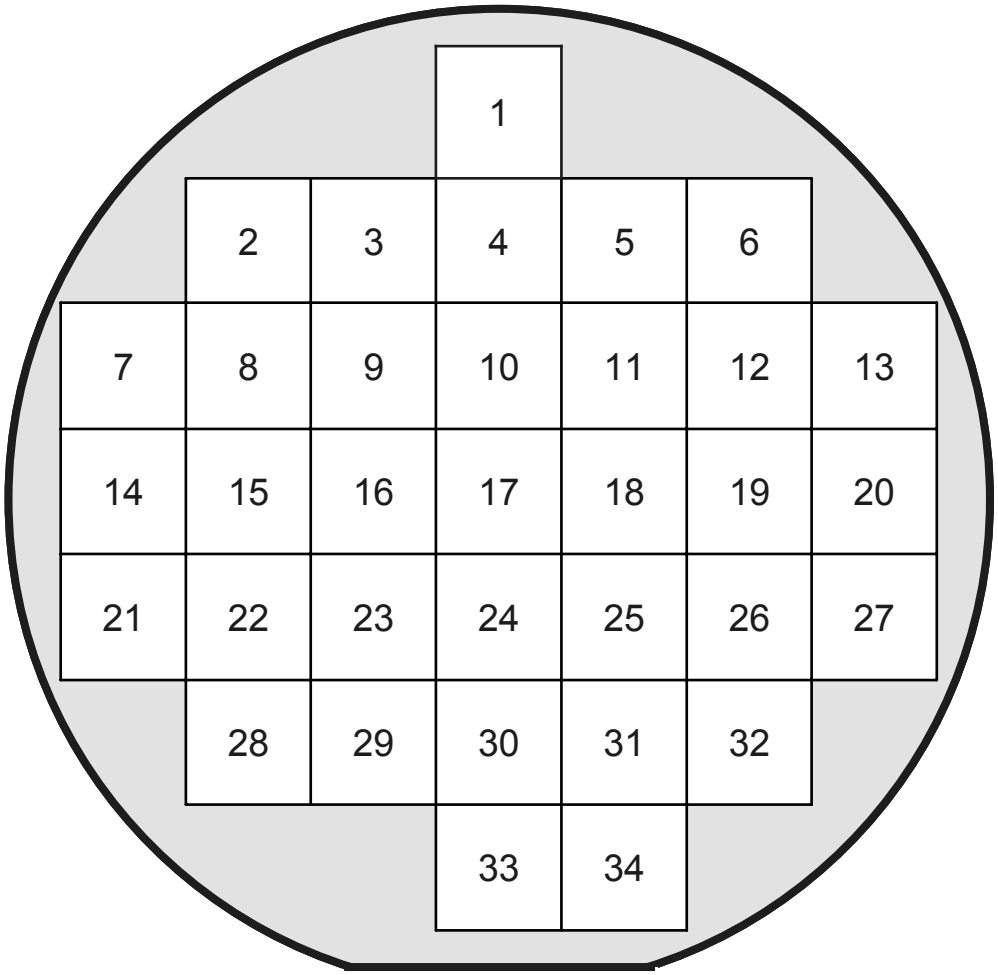


Fig. 106: Layout of dies on a 6” Wafer

Fig. 107: Layout of test chip mask

Appendix B: Structures on test chip

Table 18: Comb structures

Name/Type	Line space [µm]	Serpentine length [m]	Alignment M1 to M2
Comb Full	0.45	4.208	perpendicular
Comb Full	0.50	4.000	perpendicular
Comb Full	0.60	3.632	perpendicular
Comb Full	0.70	3.328	perpendicular
Comb Full	0.80	3.072	perpendicular
Comb Full	0.90	2.856	perpendicular
Comb Full	1.00	2.664	perpendicular
Comb Full	1.10	2.496	perpendicular
Comb Full	1.30	2.216	perpendicular
Comb Full	1.40	2.104	perpendicular
Comb Full	1.80	1.736	perpendicular
Comb Full	1.90	1.664	perpendicular
Comb Air Gap 035	0.45	4.208	perpendicular
Comb Air Gap 035	0.50	4.000	perpendicular
Comb Air Gap 040	0.45	4.208	perpendicular
Comb Air Gap 040	0.50	4.000	perpendicular
Comb Air Gap 045	0.45	4.208	perpendicular
Comb Air Gap 045	0.50	4.000	perpendicular
Comb Air Gap 050	0.45	4.208	perpendicular
Comb Air Gap 050	0.50	4.000	perpendicular
Comb Air Gap 050	0.60	3.632	perpendicular
Comb Air Gap 050	0.70	3.328	perpendicular
Comb Air Gap 050	0.80	3.072	perpendicular
Comb Air Gap 050	0.90	2.856	perpendicular
Comb Air Gap 050	1.00	2.664	perpendicular
Comb Air Gap 050	1.10	2.496	perpendicular
Comb segmented	0.45	4.208	perpendicular
Comb segmented	0.50	4.000	perpendicular
Comb segmented	0.60	3.632	perpendicular
Comb segmented	0.70	3.328	perpendicular
Comb segmented	0.80	3.072	perpendicular
Comb segmented	1.00	2.664	perpendicular
Comb Double Air Gap	1.30	2.216	perpendicular
Comb Double Air Gap	1.40	2.104	perpendicular

Comb Double Air Gap	1.80	1.736	perpendicular
Comb Double Air Gap	1.90	1.664	perpendicular
Comb Air Gap parallel	0.50	4.000	Parallel, M2 above M1
Comb Air Gap parallel	1.00	2.664	Parallel, M2 above M1
Comb Air Gap parallel	0.50	4.000	Parallel, M2 above Air Gap 1
Comb Air Gap parallel	1.00	2.664	Parallel, M2 above Air Gap 1
Comb Air Gap parallel segmented	0.50	4.000	Parallel, M2 above M1
Comb Air Gap parallel segmented	1.00	2.664	Parallel, M2 above M1
Comb Air Gap parallel segmented	0.50	4.000	Parallel, M2 above Air Gap 1
Comb Air Gap parallel segmented	1.00	2.664	Parallel, M2 above Air Gap 1
Comb Full parallel	0.50	4.000	Parallel, M2 above M1
Comb Full parallel	1.00	2.664	Parallel, M2 above M1
Comb Full parallel	0.50	4.000	Parallel, M2 above line space M1
Comb Full parallel	1.00	2.664	Parallel, M2 above line space M1

Table 19: Reliability structures

Name/Type	Line space [µm]	Adjacent material
Reliability Full	0.45	Adjacent lines
Reliability Full	0.50	Adjacent lines
Reliability Full	0.60	Adjacent lines
Reliability Full	0.70	Adjacent lines
Reliability Full	1.20	Adjacent lines
Reliability Full	0.50	Isolated
Reliability Air Gap 035	0.45	Adjacent lines
Reliability Air Gap 035	0.50	Adjacent lines
Reliability Air Gap 040	0.45	Adjacent lines
Reliability Air Gap 040	0.50	Adjacent lines
Reliability Air Gap 045	0.45	Adjacent lines
Reliability Air Gap 045	0.50	Adjacent lines
Reliability Air Gap 050	0.45	Adjacent lines
Reliability Air Gap 050	0.50	Adjacent lines
Reliability Air Gap 050	0.60	Adjacent lines
Reliability Air Gap 050	0.70	Adjacent lines
Reliability Air Gap 050	0.80	Adjacent lines
Reliability Air Gap 050	1.00	Adjacent lines
Reliability Air Gap 050	1.10	Adjacent lines
Reliability Air Gap 050	1.20	Adjacent lines

Appendix C: Process recipes

Cobalt/Tungsten alloy with Phosphorus (CoWP) according to [Pet02], [Ish04]

– amounts for 100 ml

2.3 g $CoSO_4 \cdot 7\ H_2O$

17.6 g $Na_3C_6H_5O_7 \cdot 5.5\ H_2O$ (Sodium tricitrate hydrate)

3.1 g H_3BO_3

1.9 g $NaH_2PO2 \cdot H_2O$

1.0 g $Na_2WO_4 \cdot 2\ H_2O$ or 2.0 g $H_3[P(W_3O_{10})_4]$

KOH drop by drop till pH 8.8 - 9 is achieved

Deposition performed at 80 - 90°C for 1 - 3 min. For deposition on copper surfaces must be activated by immersion of the surface at RT in a 0.4 mMol-solution of H_2PdCl_4 for 5 - 20 s.

With the addition of 300 mg (50 mMol/l) of DMAB (Dimethylamine-Boran Complex) the deposition can be performed without Pd activation. Overall the simplest and best solution is the deposition with DMAB and $H_3[P(W_3O_{10})_4]$ as the tungsten source.

Nickel/Molybdenum alloy with Phosphorus (NiMoP) according to [Wir04], [Sri01]

– amounts for 100 ml

2.6 g $NiSO_4 \cdot 6\ H_2O$

2.1 g $NaH_2PO_2 \cdot H_2O$

3.6 g $Na_3C_6H_5O_7 \cdot 5{,}5\ H_2O$ (Sodium tricitrate hydrate)

1.5 ml $C_3H_6O_3$ (Lactic acid)

0.24 g $Na_2MoO_4 \cdot 2\ H_2O$

0.3 g DMAB (Dimethylamine-Boran Complex)

NaOH and H_2SO_4 for pH-adjustment to pH = 9

Deposition was performed at 70 - 90°C for 1 - 3 min. No activation is needed.

Symbols and abbreviations

Table 20: Symbols

Symbol	Description
A	Surface area
C	Capacitance
$C_{air\ gap}$	Capacitance of air gap
C_{full}	Capacitance of full structure
C_{gate}	Gate capacitance
C_{junc}	Junction capacitance
C_{line}	Line-to-line capacitance
C_m	Material constant in Black's equation
C_{space}	Capacitance of spacer
C_{substr}	Line-to-substrate capacitance
C_{wire}	Parasitic capacitance of metal line
d	Gap space, line space
D_0	Material specific diffusion coefficient
$D_{lattice}$	Diffusivity of the lattice ions
e	Electron charge
E	Electric field strength
$\vec{E}$	Electric field vector
E_a	Activation energy for electromigration
E_{full}	Electric field strength between full structure
E_{max}	Breakdown field strength
f	Operating frequency
F	Electron wind force for electromigration
f_m	*LCR*-meter measurements frequency
I	Heat flux
j	Current density
J	Leakage current density
k (also ε_r)	Relative dielectric constant
k_b	Boltzmann constant
k_{bulk}	Bulk dielectric constant of a material
k_{eff}	Effective dielectric constant
l	Wire length
$MTTF$	Mean time to failure value
n	Current density exponent in electromigration
N	Ion density
p	pressure
P_{dis}	Power dissipation

Q	Electric charge
q	Single electron charge
R	Real part of the impedance vector
R_{dr}	Drive transistor on-resistance
R_{wire}	Resistance of metal line
T	Temperature
TTF	Time to failure
V	Voltage
$V_{air\ gap}$	Voltage drop across the air gap
V_{app}	Applied voltage
V_{dd}	Operating voltage
$V_{x\text{-}talk}$	Crosstalk signal
X	Imaginary part of the impedance vector
Z	Modulus of the impedance vector
Z_{eff}	Effective ion charge
δ	Loss tangent of dielectrics
ε_0	Dielectric constant in vacuum
τ	Signal delay time
τ_{prop}	Propagation delay
ρ	Charge density
φ	Phase shift angle
Φ_B	Work function of a metal
λ	Thermal conductivity
$\underline{Z}$	Impedance vector

Table 21: Abbreviations

Abbreviation	**Description**
a.c.	alternating current
a-CF	amorphous Fluorinated Carbon
a-SiC	amorphous Silicon Carbon
BCB	BenzoCycloButene
BELTS	Back End of Line Test chip
BEOL	Back End Of Line
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
CVD	Chemical Vapor Deposition
d.c.	direct current
DMAB	DiMethylAmine-Boran complex
DRAM	Dynamic Random Access Memory
DUT	Device Under Test
ECL	Emitter Coupled Logic

EDX	Energy Dispersive X-ray analysis
ERD	Elastic Recoil Detection
ESD	ElectroStatic Discharge
FEM	Finite Element Method
FIB	Focused Ion Beam
FPI	Fluorinated PolyImide
FSG	Fluorinated Silicon Glass
FT-IR	Fourier Transform Infrared Spectroscopy
GDDS	Gas Dome Dielectric System
HDP-CVD	High Density Plasma Chemical Vapor Deposition
HF	HydroFluoric acid
HSQ	Hydrogen SilsesQuioxane
ICP-MS	Inductively Coupled Plasma Mass Spectrometry
ILD	InterLayer Dielectric
IMD	InterMetal Dielectric
ITRS	International Technology Roadmap for Semiconductors
M1	1st Metal layer
M2	2nd Metal layer
MSQ	Methyl SilsesQuioxane
MTTF	Mean Time To Failure
NRA	Nuclear Reaction Analysis
PAE	PolyArylenEther
PECVD	Plasma Enhanced Chemical Vapor Deposition
PVD	Plasma Vapor Deposition
RBS	Rutherford Backscattering Spectrometry
RIE	Reactive Ion Etching
RTP	Rapid Thermal Processing
SACVD	Sub Atmospheric Chemical Vapor Deposition
SEM	Scanning Electron Microscope
SIMS	Secondary Ion Mass Spectroscopy
TEOS	TetraEthylOxySilane
TTF	Time To Failure
ULK	Ultra-Low-*K*
VLSI	Very Large Scale Integration
XPS	X-ray Photoelectron Spectroscopy

Figures

Tables

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  Planned in Journal for Applied Physics

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