Low Power Reference Voltages for Stepwise Display Drivers

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***Abstract*— A significant part of the energy consumed by a flat panel display is dissipated in the controlling circuitry. The column line flat panel display driver proposed in [1] has shown the high potential of stepwise charging to reduce the power dissipation while driving the column lines of the display. The driver has been extended to full dynamic resolution in [2], thus allowing market relevant image quality. In this work a method for high efficient recharging of the temporary supply sources in the driver is presented. In the proposed approach the charging current is switched to avoid static bias currents.**

I. Introduction

A. Flat Panel Displays

Fig. 1 a) depicts the common architecture of all flat panel matrix displays. Although the investigations in this work have been carried out to meet the requirements of an OLED display, the basic concept is applicable as well to all other types of active matrix displays. Displays that feature a selection transistor like T_1 in Fig. 1 b) are considered to be active displays. The proposals in this work apply to the column drivers in the display. They are also called source drivers because the sources of the selection transistors in an active matrix display are connected to the output of this driver. This output has to provide an analog voltage value which corresponds to the intensity of a color sub-pixel. However, the row or gate drivers exhibit a digital output and are not covered in this work.

In this work a total error of 10% in the final voltage level on the column line is considered acceptable. Please note that this small error leads to a high quality display and is not met by most consumer products on the market today.

B. Stepwise Charging

Stepwise charging is an approximation of adiabatic switching [3], [4] which exhibits the advantage of not needing an oscillator. The necessary voltage ramps are approximated by small voltage steps, which reduces the dissipated energy to

$$E_{\text{diss,stepwise}} = \frac{1}{N} E_{\text{diss}} \tag{1}$$

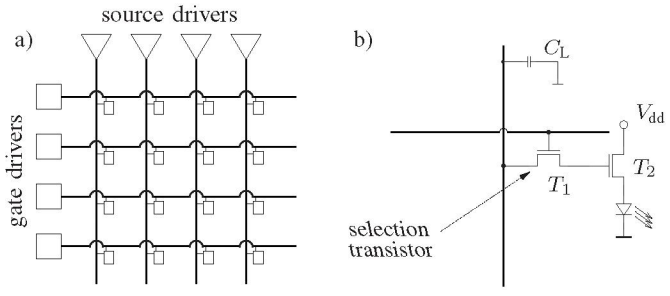

Fig. 1. a) Architecture and b) Pixel Schematic for an AM-OLED Display

where N is the number of steps. Note that this holds true only if the system is given enough time to settle. Stepwise charging is like all adiabatic switching techniques therefore a tradeoff between power and speed and most suitable in applications with limited performance requirements [5].

II. The Stepwise Driver

The basic concept of how to apply stepwise charging to the source drivers in a flat panel display has been presented at ISCAS 2004 [1]. Although the presented solution had some limitations, it clearly demonstrated the possibilities regarding power consumption.

The proposed architecture implements as many components as possible in the digital domain in order to minimize the effort in power and area for analog components. The digital registers consume significantly less energy than the analog counterparts. Although the new logic is slightly more complicated, and one DAC is needed at each line, the power consumption is negligible with respect to the bias currents of the conventional line drivers.

Stepwise charging is realized by applying a digital control signal which will switch the output to the next higher value for each time step until the desired voltage level is reached. To benefit from the possible power savings it is important to ensure that an intermediate voltage level is almost reached before the next clock edge. A significant part of the energy on the line can be recovered. Large capacitors are used to temporarily deliver energy and to recover the charge when driving analog output voltages. There is one large source capacitor C_S per reference voltage. It is charged by reference voltage sources to the appropriate voltage level during the reset period. Afterwards the whole DAC is powered from the capacitors. As there is only one reference voltage generator per display, the source capacitors could be realized as external elements.

The output is discharged stepwise by connecting the load to the appropriate reference voltages. Thus for every clock cycle the output voltage is decreased by $\frac{V_{dd}}{N}$. When the output is connected to the next lower reference voltage level some of the charge is transferred back to C_S and the corresponding reference voltage across C_S nearly restores the initial value. Of course there can be no energy transferred to the highest voltage level. The amount of energy taken from this reference voltage is prorated on the charging and discharging of the single steps. In the following reset the losses are compensated by connecting C_S to the appropriate reference voltage. It can easily be calculated that in theory, all but the highest source capacitors $C_{S\,max}$ recover charge up to their original voltage value. The energy which has been dissipated and thus has to be replaced in $C_{S\,max}$ is given by

$$E_{S\,max} = \frac{V_{dd}}{N} \cdot V_{max} \cdot C_L \tag{2}$$

where V_{max} is the voltage representing the desired pixel intensity and $C_{S\,max}$ the corresponding source capacitor.

Although this driver has been presented for a 3 bit resolution, it can easily be scaled to 4 bit.

III. Reference Recharge Circuit

When driving a large capacitive load with a biased transistor, high operating point currents are necessary to maintain timing specifications. To avoid the accompanying losses, a switched circuit is used. In conventional SRAM designs, sense amplifiers based on voltage sensing are well established because of their well-known structure, clear design effort, acceptable area and power consumption. Voltage sense amplifiers evaluate a small voltage difference which is applied at the input and converted into a logical level output signal.
The amplifier is used to decide, based on the measured voltage difference, whether another quantum of charge should be loaded onto the capacitance C_S.

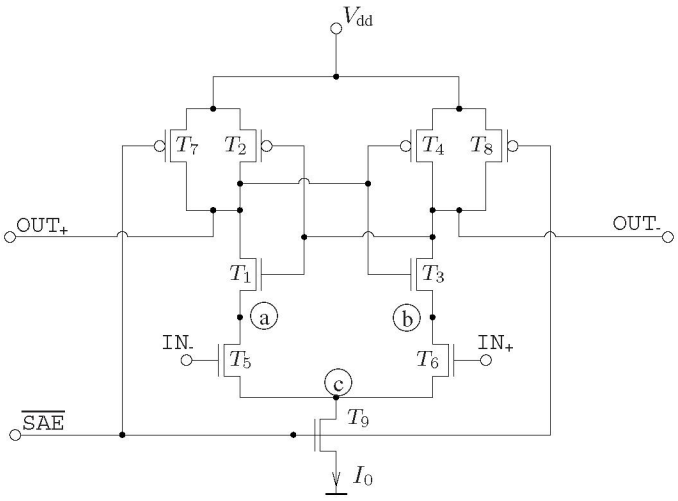

Fig. 2. Circuit Diagram of the Voltage Sense Amplifier

Voltage Sense Amplifier - Circuit Description

The sense amplifier [6] in Fig. 2 is based on a bistable circuit. The current flow through the differential input transistors T_5 and T_6 controls the serially-connected latch circuit. A small difference between the currents through T_5 and T_6 forces the system in one or the other settling point. The transient behavior is shown in Figure 3. For the present application, the input DC voltage varies between $\frac{1}{16} \cdot 5\text{V}$ and $\frac{15}{16} \cdot 5\text{V}$. This wide input range has a strong influence on the delay and accuracy of this kind of latch amplifier. Since the timing performance requirements are quite relaxed in the present application and the total delay of the amplifier is below 10ns for all operating conditions, speed is not an issue. However, accuracy is a critical parameter. The n-channel differential pair in not suitable for all input voltage levels. For this reason, the voltage sense amplifiers for the lower voltage sources are built using the complementary structure. Detailed explanations of the complementary sense amplifier are not carried out here, but can easily be derived from the previous section. In order to maintain the voltage levels V_{ref} within the specifications, the amplifier needs to be carefully designed with respect to accuracy. As the amplifier is based on a differential principle, the symmetry of the circuit is the key to high accuracy. Attention has to be drawn on matching during both design and layout.
The function of the described sense amplifier relies heavily on a high symmetry of the circuit. This includes the loads on the outputs of the circuit. The sense amplifier output nodes $\texttt{OUT}_{+/-}$ are both connected to a digital inverter and an AND-gate, although only the inverter and

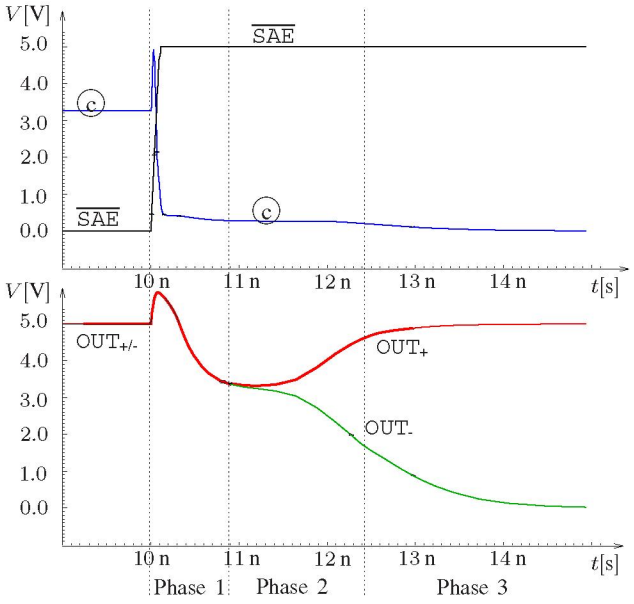

Fig. 3. Transient Behavior of the VSA

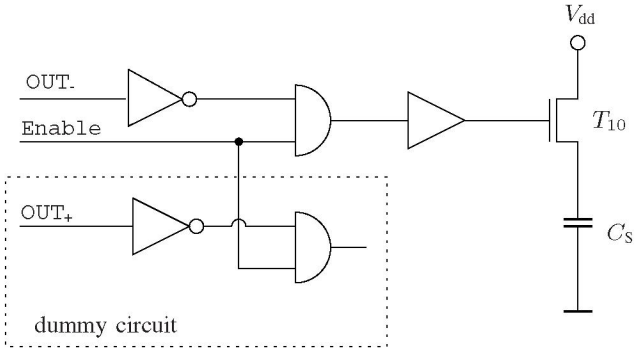

Fig. 4. Dummy Circuit and Charging Transistor T_{10}

AND-gate connected to the $\texttt{OUT}_-$ node are required for driving the next stage.
Simulations of the circuit show that a two stage dummy circuit is necessary (Figure 4). Without the dummy AND-gate an offset of more than $V_{\text{error}} = 20\text{mV}$ may occur. If the voltage sense amplifier is used without the dummy inverter at node OUT_-, fail decisions of more than $V_{\text{error}} = 300\text{mV}$ are observable. Figure 5 shows a reference voltage of $V_{\text{ref}} = 2.5V$ and the charge curve of the capacitance $C_S = 6\mu\text{F}$ versus time. It is shown that the voltage sense amplifier (VSA) with the dummy inverter and AND-gate is exactly within the limits given by the quantization. In case the voltage drop at the capacitance C_S is higher than the reference voltage, the voltage sense amplifier stops charging the capacitance.
The transistor T_{10} delivers the charging current. Therefore, it has to be implemented with an appropriate $\frac{W}{L}$. Because the short reset period requires large charging currents, T_1 is a large transistor. Detailed information on the scaling of T_{10} can be found in Section III. This transistor presents a significant input capacitance to the driving circuit. A super buffer consisting of a chain of inverters is used to control T_{10}.

Scheduling of the Charging Process

The voltage source based on a sense amplifier is controlled by two periodical input signals.The signal `SAEN` (`Sense Amplifier ENable`)

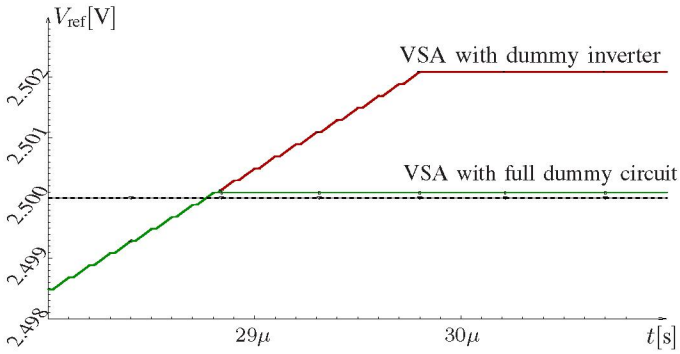

Fig. 5. Transient of a VSA with Full Dummy Circuit and Dummy Inverter

activates the sense amplifier by rendering T_9 conductive and opening T_7 and T_8. The voltage sense amplifier then evaluates the two input signals and holds its digital output value until the SAEN signal reverts. Both SAEN and Enable are periodical signals. The cycle time of these signals has been chosen to be $t_{cy} = 100ns$. This is a tradeoff between accuracy and efficiency. For shorter cycle times the quantization is finer, thus allowing for a higher accuracy. Nevertheless, the time required for the setup and evaluation of the sense amplifier is constant. Therefore, the fraction of charging time is less for short cycle times.

At the beginning of a charging cycle, a setup period of 10ns is provided to carry out precharge in the sense amplifier and settle the initial conditions. Subsequent SAEN switches to high and starts the evaluation in the sense amplifier. As the amplifier is very sensitive towards load imbalances at the outputs during this phase, the signal ON has to remain low to cut off the input capacitance of T_{10}. After the evaluation finishes, the outputs $\text{OUT}_{+/-}$ settle at either V_{dd} or GND depending on the input levels. The circuit has reached a stable operating point and the outputs can be connected to the adjacent stage. This scheduling leaves a time slot of 80ns for the actual charging.

Driving MOS Transistor T_{10}

If the voltage at the capacitance C_{S} is detected to be lower than the reference voltage V_{ref}, the driving MOS transistor is turned on for $t_{\text{charge}} \approx 80\text{ns}$. The transistor dimensions set the current onto the capacitance during this time to $I_{\text{charge}} \approx 30\text{mA}$. These values have been chosen as a trade off between accuracy and charging capability. The voltage on the capacitance increases by

$$\Delta V_{C_{\text{S}}} = \frac{Q_{\text{charge}}}{C_{\text{S}}} = \frac{I_{\text{charge}} \cdot t_{\text{charge}}}{C_{\text{S}}} = \frac{2.4\text{nAs}}{6\mu\text{F}} = 400\mu\text{V}. \quad (3)$$

Since the driving transistor is controlled by digital voltage levels, the voltage at the gate of the transistors is $v_{\text{g}} = 0\text{V}$ if the n-channel transistor is non conductive and $v_{\text{g}} = 5\text{V}$ if the n-channel transistor is conductive. For p-channel transistors, the voltages invert.

The driving transistors for the lower seven capacitances $C_{\text{S},1-7}$ are n-channel transistors. The voltage at the drain node of a conducting n-channel is V_{dd}. The voltage at the source is equal to the voltage drop at the capacitance C_{S}. Since the current i_{ds} depends on the voltage v_{gs} between gate and source of the transistor, this variation across different reference voltages $V_{\text{ref,i}}$ has to be compensated for by appropriate transistor sizing. During charging, the voltage drop between gate and source is the same as between drain and source, thus the transistor behaves like a diode and is driven in saturation mode. Therefore, the drain current i_{ds} depends on the transistor parameters as follows:

$$i_{\text{ds}} = \frac{\mu_{\text{n}} C_{\text{ox}}}{2} \left(\frac{W}{L}\right) (v_{\text{gs}} - V_{\text{th}})^2 \quad (4)$$

Eq. 4 shows the quadratic dependency of the current i_{ds} with respect to the gate source voltage v_{gs}. Assuming a constant charging current and a worst case voltage drop, a design point of $i_{\text{ds}} = I_{\text{min}} = 30mA$ at $v_{\text{gs}} = V_{\text{ref}}$ is necessary to fulfill the timing requirements. Note that a small current I_{min} is desired to minimize the voltage offset due to quantization. Nevertheless, the larger v_{gs} for higher voltage drops increases the charging current i_{ds}. This speeds up recharging and helps the system to recover from a severe voltage drop within the given time.

Once the desired voltage V_{ref} is reached, the failure caused by an additional charge quantum is given by

$$V_{\text{error}} \leq \Delta V_{C_{\text{S}}} \approx 400\mu\text{V}. \quad (5)$$

To achieve the desired resolution, the offset error V_{error} of the reference voltage V_{ref} has to be small with respect to a LSB voltage step. The error V_{error} is considered sufficiently negligible if it is less than 10% of a least significant bit voltage step.

$$V_{\text{error}} \leq 0.1(\frac{1}{255})5\text{V} \approx 2\text{mV} \quad (6)$$

With this constraint, a proper operation of the whole system is assured. The worst case error of the voltage source is smaller than 400μV (Eq. 5). Although this error is a random quantity and can not be compensated, it is small enough that it does not degrade image quality.

Since the width of the n-channel transistors increases with the square of the voltage V_{ref}, these transistors consume a lot of area for high reference voltages. To overcome this problem, p-channel transistors are used to charge the capacitances for $V_{\text{ref}} > 2.5\text{V}$. They are operating in linear mode and the dependency on the voltage over the capacitance $V_{C_{\text{S}}}$ is less than for the n-channel transistors. Despite the lower mobility μ_{p} of the p-channel transistors, the operation point allows for a smaller width. To exploit this benefit, p-channel transistors are used for charging the upper eight capacitances $C_{\text{S},8-16}$. The voltage drop between gate and source v_{gs} is constant and larger than the voltage v_{ds} ($v_{\text{sg}} = 5\text{V} > V_{\text{dd}} - V_{C_{\text{S}}}$), thus forcing the transistor into the linear operation region. The current i_{ds} is given by

$$i_{\text{ds}} = \mu_{\text{p}} C_{\text{ox}} \left(\frac{W}{L}\right) (v_{\text{gs}} - V_{\text{th,p}} - \frac{v_{\text{ds}}}{2}) v_{\text{ds}}. \quad (7)$$

The charging current i_{ds} is also quadratically dependent on v_{ds} and thus on the voltage across the capacity $V_{C_{\text{S}}}$. Note that this dependency is dominated by the linear term introduced by the high fixed gate source voltage v_{gs}. As well as for the n-channel transistor, i_{ds} is increased for large offsets, thus enabling fast recovery and high accuracy.

Many effects are omitted in the equations (4) and (7), therefore the results can only be treated as rough approximations. For this reason, the values of the $\left(\frac{W}{L}\right)$-ratio shown in Table I are not calculated but optimized by simulations.

Energy Consumption

A significant part of the energy taken from the power supply is dissipated during the charging of the column line in the corresponding switches. This energy has been discussed in Chapter II. The smaller fraction is dissipated in the reference circuit during the reset period to maintain the bias point and recharge parasitic capacitances.

The charging and discharging of the gate capacitance $C_{\text{g},T_{10}}$ of the transistor T_{10} dissipate a significant part of energy. As $C_{\text{g},T_{10}}$ is strongly dependent on the width of the transistor T_{10}, it varies over a

V_{ref}[V]	0.3125	0.625	0.9375	1.25	1.5625	1.875	2.1875	
$v_{\text{ds,n}}$[V]	4.6875	4.375	4.0625	3.75	3.4375	3.125	2.8125	
$\left(\frac{W}{L}\right)_n$	53	60	70	82	100	126	167	
V_{ref}[V]	2.5	2.8125	3.125	3.4375	3.75	4.0625	4.375	4.6875
$v_{\text{ds,p}}$[V]	2.5	2.1875	1.875	1.5625	1.25	0.9375	0.625	0.3125
$\left(\frac{W}{L}\right)_p$	122	131	143	162	191	242	345	666

TABLE I
$\left(\frac{W}{L}\right)$ OF CHARGING TRANSISTORS

wide range for different reference voltages V_{ref}. Also, the dissipation in the driving circuit varies. The inverters have to be adjusted to $C_{\text{g},T_{10}}$ to maintain the timing requirements. Note that this kind of power dissipation as well as the losses due to charging C_{S} only occur if the voltage over the capacitor $V_{C_{\text{S}}}$ is considered too low by the sense amplifier. In this case, the transistor T_{10} is rendered conductive and an additional quantum of charge is put on C_{S}.

The lowest possible energy consumption during one charging cycle ($t_{\text{cy}} = 100\text{ns}$) is achieved for a reference circuit with a low $V_{\text{ref,1}} = 0.3125\text{V}$. This circuit has only a small transistor T_{10}, thus minimizing overall parasitic capacitances. The voltage over the capacitor $V_{C_{\text{S}}}$ is assumed to be high enough; no charging of C_{S} takes place. Simulations show that in this best case the power dissipation in the reference circuit is as low as

$$E_{\text{bc}} \approx 20\text{pJ}. \tag{8}$$

The highest possible energy consumption during one charging step is achieved by the voltage source providing the highest reference voltage $V_{\text{ref,15}} = 4.6875\text{V}$. The enormous transistor T_{10} exhibits a width of $W_{10} = 666\mu\text{m}$, thus introducing a lot of parasitic capacitance into the circuit. A four stage super buffer is used to drive the capacitance $C_{\text{g},T_{10}}$. Even in the case where no charging occurs, the power dissipation is significantly higher. Assuming a low capacitor voltage which makes the charging necessary, the overall energy dissipation of the reference circuit has been simulated to be

$$E_{\text{wc}} \approx 239\text{pJ}. \tag{9}$$

Note that the energy E_{wc} does not include the charging current through T_{10}. The power dissipation in the voltage sense amplifier itself is independent of the decision of the VSA with very good approximation. However, it strongly depends on the difference between the input signals. For a bigger voltage difference between the two inputs, the evaluation speed of the VSA increases and the time for cross currents is reduced. Therefore, the values shown here are only approximations.

The entire voltage source circuitry consists of 15 different levels providing the 15 different reference voltages $V_{\text{ref,1-15}}$. During the reset time of $t_{\text{vs}} = 3\mu\text{s}$, each VSA measures the difference between the voltage reference V_{ref} and the voltage at the capacitance C_{S}. The accurate energy consumption $E_{\text{RC,comp}}$ of the complete reference circuit per reset cycle T_{cy} depends on the statistic distribution of the pixel values. Only an upper and a lower bound can be given:

$$30 \cdot 15 \cdot E_{\text{bc}} = 9\text{nJ} \leq E_{\text{RC,comp}} \leq 30 \cdot 15 \cdot E_{\text{wc}} = 126\text{nJ} \tag{10}$$

In Figure 6, the transient power of a single reference circuit P_{RC} for the best case and the worst case is depicted. In both simulations, the SAEN signal starts the evaluation of the input signals at $t = 10\text{ns}$.

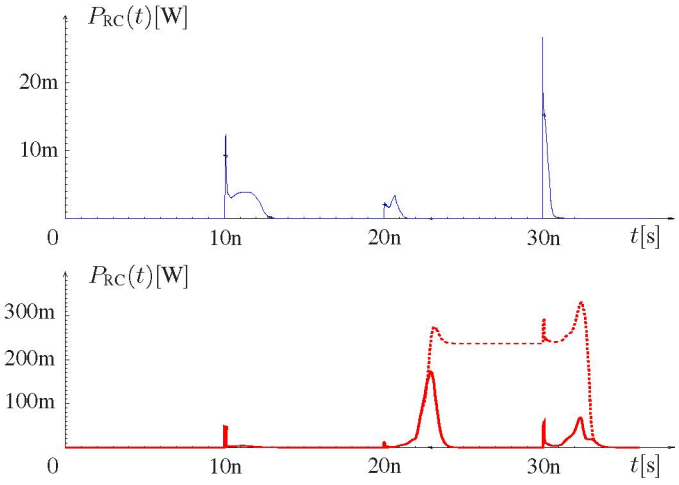

Fig. 6. Transient Power Consumption: a) Best Case b) Worst Case

The power consumed between $t = 10\text{ns}$ and $t \approx 15\text{ns}$ is exclusively consumed by the VSA and the controlling circuit. At $t = 20\text{ns}$, the ON signal becomes high and the digital circuit subsequent to the VSA begins to evaluate the controlling signal for the driving transistor. This evaluation eventually includes charging $C_{\text{g},T_{10}}$ and is finished at about $t \approx 24\text{ns}$. Both control signals, SAEN and ON, are switched off at $t = 30\text{ns}$. Note that for Figure 6, the charging period has been reduced from 80ns to 10ns. The energy consumed after $t = 30\text{ns}$ restores the initial conditions for the next measurement and switches off the driving transistor T_{10}.

In Figure 6a), the best case is depicted. The dominant source of dissipation is the evaluation of the VSA at 10ns. No power is taken from the source to charge the load capacitances C_{S} between 22ns and 30ns.

Figure 6b) shows the transient power consumed by the voltage source stage, providing the reference voltage $V_{15} = 4.6875\text{V}$. The transient power marked by the dotted line in Figure 6b) contains the power for charging the capacitance C_{S}, which can be seen as a nearly constant power consumption between $t \approx 23\text{ns}$ and $t = 30\text{ns}$.

IV. CONCLUSION

This circuit is able to maintain the levels of the reference circuit V_{ref} within the required accuracy without dissipating significant static energy. The dynamic concept of the voltage sense amplifier achieves the required performance without any static operating points. The energy dissipation of the circuit is strongly dependent on the operating parameters. The power consumption is low enough in all cases to make this circuit the appropriate solution for the proposed application.

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