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Studies of Radiation Hardness of MOS Devices for Application in a Linear Collider Vertex Detector

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Contents

Abstract

The proposed International Linear Collider (ILC) together with the Large Hadron Collider (LHC) at CERN serve as a combined tool to explore the mysteries of the universe: the former is a precision machine and the latter can be considered as a finding machine. The key component of the ILC is the vertex detector that should be placed as close as possible to the Interaction Point (IP) and has better radiation tolerance against the dominant electron-positron pair production background from beam-beam interactions. A new generation of MOS-type Depleted-Field-Effect Transistor (MOSDEPFET) active pixel detectors has been proposed and developed by Semiconductor Labor Munich for Physics and for extraterrestrial Physics in order to meet the requirements of the vertex detector at the ILC.

Since all MOS devices are susceptible to ionizing radiation, the main topic is focused on the radiation hardness of detectors, by which a series of physical processes are analyzed: e.g. surface damage due to ionizing radiation as well as damage mechanisms and their associated radiation effects. As a consequence, the main part of this thesis consists of a large number of irradiation experiments and the corresponding discussions. Finally, radiation hardness of the detectors should be improved through a set of concluded experiences that are based on a series of analysis of the characteristic parameters using different measurement techniques. The feasibility of the MOSDEPFET-based vertex detector is, therefore, predicted at ILC.

Kurzfassung

Um viele physikalischen Fragestellungen zu beantworten, wie. z.B. Higgs, SUSY and Extra Dimensions, usw., gibt es ein Standardmodel. Es hat sich bisher bewärt, jedoch bleiben einige Fragen (Higgs-Teilchen) noch offen. Diese Fragen können an einem zukünftigen Elektron-Positron-Linearbeschleuniger mit Energien von 500 bis etwa 1000 Milliarden Elektronenvolt werden. Der ILC könnte ungefähr im Jahr 2020 in Betrieb sein.

Eine wichtige Komponente des ILC ist ein Vertexdetektor, der sich um den Wechselwirkungspunkt befindet, wo Teilchen (Elektron und Positron) kollidieren. Mit dem Vertexdetektor können die Zefälle langlebiger Teilchen, wie B-Meson, rekonstruiert werden. Dies, und vieles andere, ist zur Rekonstruktion neuer Teilchen, wie dem Higgs, notwendig. Wegen der hohen Luminosität einer solchen Maschine, dem hohen Strahlungsuntergrund und der Nähe zum Wechselwirkungspunkt muss der Vetexdetektor hohen Anforderungen an die Strahlungsresistenz genügen. MOS-type Depleted-Field-Effect Transistor (MOSDEPFET) Aktive Pixel Detektoren stellen einen der besten Kandidaten für die Anwendung am Vertexdetektor im ILC dar. Diese DEPFETs wurden am Halbleiterlabor des Max-Planck-Instituts für Physik München entwickelt.

Wie alle MOS Strukturen leiden DEPFETs unter Oxidschädigung durch ionisierende Strahlung. Bisher erwiesen sich die am HLL gefertigten Strukturen als erstaunlich strahlungsresistent. Um dies genauer zu untersuchen wurden für diese Arbeit spezielle MOS Teststrukturen gefertigt, bestahlt und vermessen. Dazu wurden vor allem einige Messapparaturen für wie z.B., Strom-Spannung Messung (IV), Kapazitäts-Spannung Messung (CV) und Gated-Diode Messung entwickelt und aufgebaut. Die Messdaten wurden mit Literaturdaten verglichen und analysiert, darauf aufbauend konnte ein physikalisches Model entwickelt werden, um die Strahlenschädigungen simulieren und berechnen zu können. Zum Schluss konnten Vorschläge entwickelt werden um die Strahlenhärte der DEPFETs weiter zu verbessern, wie z.B., durch eine Reduzierung der Oxiddicke, oder Einhaltung einer bestimmten Biasbedingung an dem Gate-Kontakt (0V) und durch Produzierung einer zusätzlichen Nitrideschicht, usw. Der letzte Vorschlag war der wichtigste Punkt dieser Doktorarbeit, weil er die unerwarteten Eigenschaften der DEPFETs – eine kleine Threshold Spannung Verschiebung (ungefähr 4~5V) von DEPFETs, erklärt, welche laut Literatur wesentlich höher sein sollte. In dieser Arbeit wird nicht nur die Verwendbarkeit von MOSDEPFET am Vertexdetektor des ILC gezeigt, sie zeigt auch wie, mit einigen Verbesserungen des Designs und der Technologie diese Detektoren auch an Beschleunigern mit weit höherer Strahlenbelastung verwendet werden können.

Introduction

In order to unravel the secrets of the universe, many central topics still remain unexplored such as Higgs mechanism, Supersymmetry and top quark etc., that are expected to come from the large collider experiments made with the Large Hadron Collider (LHC) and the International Linear Collider (ILC) at the TeV energy scale: the former is a proton-proton collider built at CERN and serves as a exploring machine; the latter is electron positron collider and will be a powerful tool to explore TeV-scale physics complementary to LHC offering the experimental data with high precision.

A great deal has been learned about silicon detectors during the last few decades. The choice of this detector material has received a lot of attention in high energy physics. To date silicon material is still the first choice among the many semiconductor materials as a detector material due to its wide availability and fast readout speed with small signal rise time in the range of a few nanoseconds as well as its processing possibilities. To achieve the detector requirement of high spatial resolution, a pixel detector can be used.

The DEPFET (Depleted-Field-Effect Transistor) [1] based pixel vertex detector is an advanced semiconductor detector. DEPFET provides the combined function of detector and amplifier simultaneously. A MOS or JFET (Junction-Field-Effect Transistor) is integrated onto a detector substrate. In comparison with other pixel detectors DEPFET pixels have much better spatial, energy and time resolution even at room temperature. In a DEPFET pixel using a row-by-row readout mode, the detector has low power consumption. Signal charges are stored in the pixel until readout and multiple read out is possible. An excellent noise performance is also an outstanding property of such a detector.

Within this thesis, a new generation of MOS-type DEPFET [2] active pixel detector will be described, which meets the requirement of a vertex detector at the ILC. Due to the dominant electron-positron-pair background from beam-beam interactions, the radiation hard detectors should be developed and improved. For this reason, the knowledge of the damage mechanism and its influence on the detector performance is required. As a consequence, this thesis is focused on the radiation damages (mainly about surface damage) of MOS-structure-based devices.

As irradiation source X-rays are mainly utilized. X-rays are a form of ionizing radiation. In addition, other irradiation environments such as results from gamma ray, proton and neutron will shortly be discussed.

Normally radiation damages can be categorized into two different types depending on location and mechanism: Bulk damages mainly take place in the silicon volume due to displacement of silicon lattice atoms; surface damages are generated due to the ionization at the silicon surface. Displacement damages are generated through non-ionizing energy loss (NIEL) and can be optimized by an appropriate choice of the type of silicon, whereas

surface damages can be controlled by the improved technological design of the detectors. For a long time a large amount of experimental data about bulk damages has already been collected from R&D programs for LHC, and several corresponding models were then also developed; radiation-induced effects like change of depletion voltage, leakage current and trapping time are parameterized with good precision. Although damage mechanism about surface damages and many impressive models are already well known, there is still not a series of complementary systematic model descriptions that provide predictions about radiation damage level in advance. It is therefore the goal of this thesis to find a set of characteristic surface parameters and the associated experimental methods for their proper determination with the intention to study radiation effects on detectors developed for particle physics experiments with respect to a specific process and design.

For this reason, the aim of this thesis is not only to describe a generation mechanism for surface damages, but also to study systematically radiation effects using a set of characteristic surface parameters and the corresponding experimental methods on MOS devices and, furthermore, to make a precise prediction about the applicability of the DEPFET-based pixel vertex detector for the proposed linear collider, and at the same time to find an improved detector design.

This thesis is structured as follows:

In the first chapter a general concept of the proposed ILC project will be described. The DEPFET-based pixel vertex detector and irradiation tolerance will be briefly introduced.

The second chapter explains the Metal-Oxide-Semiconductor (MOS) structure, which is mainly utilized in the irradiation experiments. The functionality of three different MOS devices will be discussed: MOS-capacitance, MOS-DEPFET and MOS-gated diode.

In Chapter 3, the damage mechanism of MOS structures will be introduced. Models for damage generation and recovery process will be analyzed.

In Chapter 4, different experimental techniques performed on the corresponding devices will be presented. Some characteristic parameters will be analyzed in detail.

In Chapter 5, irradiation experiments will be introduced. Different irradiation sources and experimental setups are described and detailed analysis before and after irradiation will be given.

In Chapter 6, the highlight of this thesis is focused on the radiation effects on MOS structures. Radiation hardness will be discussed depending on several factors. As a consequence optimization for radiation hard detector design can be achieved.

Finally, in the chapter 7, this thesis will be summarized and an outlook of a future design technology of detectors for ILC will be given.

Chapter 1 Motivation

1.1 The Standard Model

Over the past few decades physicists have attempted to characterize the matter and energy of our universe – to understand the basic forces of nature and the components of matter.

In order to explain this mysterious nature, a large number of particle physics experiments have been performed to collect data in the past few decades. The emerging standard model [3] gives us the opportunity to describe the building blocks of matter and the fundamental interactions of particles. It is the most important basis of modern particle physics, and has received a great deal of experimental attention. According to the standard model, the matter is made up of a total of twelve fundamental particles (fermions) [4]: six quarks and six leptons. All of these particles can be divided up into three families, each containing two quarks and two leptons (see table 1.1).

Fundamental Particles	Families		
Quarks	Up 	Charm 	Top 
	Down 	Strange 	Bottom 
Leptons	Electron neutrino 	Muon neutrino 	Tau neutrino 
	Electron 	Muon 	Tau 

Table 1.1 Fundamental particles: 6 Quarks and 6 Leptons.

In general, normal matter (inclusive stellar materials) is made up of particles that come only from the first family, i.e., up and down quarks buildup the atomic nuclei and the electrons (one of the important leptons to date) contribute to the atomic construction. The other two families in this table can not be found in stable matter, but they can be recreated from intensive energy, e.g., cosmic rays or particle accelerators and they do not exist in a stable form of matter. Each of the twelve particles has corresponding antiparticles such as the antiparticle of the electron is the positron. Although particles and antiparticles have opposite electrical charges, they are actually very similar. If they interact with each other, they will annihilate one another and create radiation. In addition

to the fundamental particles, the standard model also describes three of four known fundamental interactions between the fundamental particles and makes precise predictions about the behavior of these interactions. A concise theoretical framework for the forces between these fundamental particles has been developed based on the theoretical principle of gauge invariance [5], by which Quantum Chromo Dynamics (QCD) [5] can describe very well the strong interaction that includes color-charged particles (quarks) and gluons. In addition, the electromagnetic and weak interaction can also be unified into a combined electroweak interaction that introduces a photon-mediated electromagnetic interaction and $Z/W^{+/-}$ bosons as the force mediating weak interaction. However, according to gauge principle all force-mediating particles should have no mass. This is contrary to the large mass of the W and Z bosons. For this reason, the Higgs-mechanism [5] as well as the Higgs field and particle are proposed to solve this problem, by which particles are given a mass through their interaction with the background medium – the Higgs field. The Higgs mechanism is a good model for the mass of W and Z. Fermion's masses are put by hand into the Lagrange formula [57]. A full study of the Higgs boson coupling consists of the determination of the top-quark Yukawa coupling, and of the Higgs self-coupling [57].

Despite providing an accurate description of nature by this model, there are still some unsolved physics problems. For instance: Why do different particles have different masses? By which mechanism do particles acquire mass? Although the Higgs mechanism seems to offer a solution to give particles masses, to date no experiment has directly detected the existence of the Higgs boson. Therefore, to find the Higgs particle is a challenging task of particle physics. On the other hand, there are further mysteries such as the hierarchy problem [6] and agreement of cosmology with the standard model of particle physics. For example, why is there a matter/antimatter asymmetry? The fourth fundamental interaction 'gravitation' is not included in the standard model. Meanwhile, research has already been focused on the Grand Unified Theory (GUT), in order to unify all fundamental particle interactions at large energy. The proposed Supersymmetry (SUSY) is the most popular concept. The answer to these deficiencies implies that there is new physics beyond the standard model which will hopefully be discovered at the next generation of particle accelerators.

One of them is the LHC (already finished this year), which is circular proton-proton collider with a centre of mass energy of 14 TeV. Proton collisions are mainly for two large experiments – A Toroidal LHC AparatuS (ATLAS) and Compact Muon Solenoid (CMS) – and a small experiment LHCb. In addition, a modus for heavy ion (lead ion) collision is also included. ATLAS and CMS are multipurpose experiments. Their goal is to identify the elementary particles, e.g. discover the Higgs boson and eventually SUSY particles if they really exist. The study of CP-violation in the B-system is specially made with LHCb. Quark-Gluon-Plasma is generated and investigated with heavy ion collision by ALICE.

Protons are easier to accelerate than electrons in a circular medium to a high energy (proton synchrotron), since electron acceleration is limited by the losses of synchrotron radiation. During collision a large number of new particles can be created. Although LHC

tries to look for and find them, it is still difficult to measure their properties with high precision, because the protons consist of many quarks, antiquarks and gluons and a large amount of fraction bursts out in all directions from the collision. The detailed collision processes cannot be well controlled or selected and the background, due to unexpected collision processes, is really high. For this reason, the International Linear Collider (ILC) can be considered as an ideal complement of LHC, ILC is a global project and could be constructed in the next decade. The proposed ILC will provide a variety of particle physics experiments in the future, and extend discoveries.

Detectors for collider machines should be optimized for physics precision in respect of their special environment. Therefore, detectors should be hermetic, with a good charge tracking system for following the charged particles after collision (momentum, energy and charge of produced particles with high precision). Therefore the tracking part of the detector system should be placed as close as possible to the interaction point and as a consequence, the vertex tracking may provide the jet flavor identification and accurate track reconstruction and excellent impact parameter resolution. The muon and hadron's calorimeter have to provide good resolution and granularity, especially in the electromagnetic section.

In addition, the Mont Carlo computer simulation is an important method used in particle physics experiments to design detectors and to understand their behavior and compare experimental data with theory.

1.2 ILC Project

At present many hot topics have received a great deal of attention and many driving physics questions are waiting to be answered about the Terascale in the micro-universe (the first two of the following) and in the macro-universe (the third one):

- Electroweak symmetry breaking
    - Higgs particle
- Ultimate unification of forces
    - Supersymmetry or extra space dimensions (> 4)
- Connection between particle physics and cosmology
    - Determination of the nature of cold dark matter particles

In order to unravel these mysteries of nature, particle physicists have concentrated their attention on particle accelerators. ILC is a huge linear accelerator, in which electrons and

positrons collide (Figure 1.1), whose energy is within the range of 0.5 to 1 TeV. Electrons and positrons come from opposite directions through the beam pipe in the detector. After the collision in the central point, two particles are annihilated and turn completely into energy, and new particles are generated. Since it is known more precisely about the initial conditions of particle production and there is also no remnant from collision partners (electron and positron), the results are simpler to explain than in the case of proton collision. In addition, due to the clear elementary process with less spurious interactions (background) there are more advantages of electron-positron collisions than proton-proton collisions. For this reason, LHC is a detection machine, and ILC is a precision machine. With ILC, one can measure more precisely the features of new particles, such as mass, lifetime, spin and quantum number.

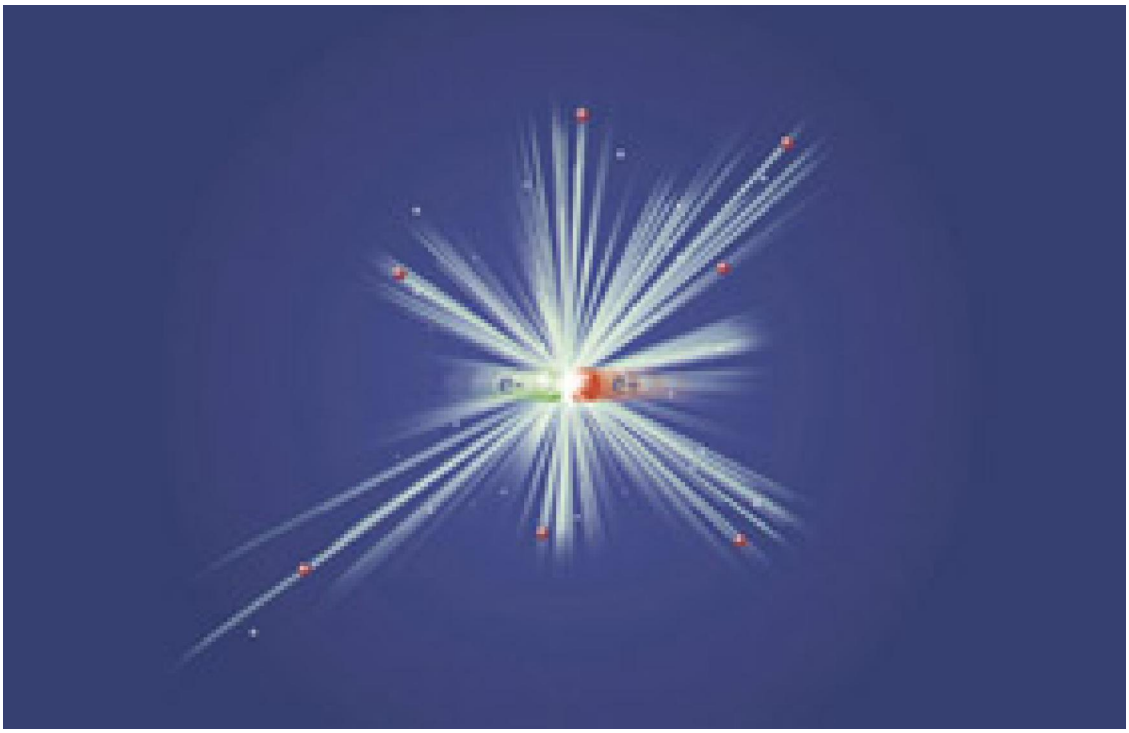


Figure 1.1 Electron positron collision [64].

LHC is already in progress. The realization and construction of such a facility for ILC is still not confirmed. However, in any case physics needs both – precision of ILC and energy of LHC.

1.2.1 Linear collider

In principle, there are two main concepts responsible for the realization of acceleration of a collider machine: the circular accelerator (circle) and the linear accelerator (straight line). The advantage of circular over linear is that in a circular medium, the beam is recycled and the circular accelerator is relatively smaller than a linear accelerator of comparable energy. However, the linear concept is mainly used for the design because energy loss in the circular ring accelerator is relevant at high energies due to synchrotron radiation. In the case of a linear accelerator (Figure 1.2), the two particles are located at two different sites and are accelerated in a straight line until they collide with each other. In this case there is no energy loss because there is no bending section.

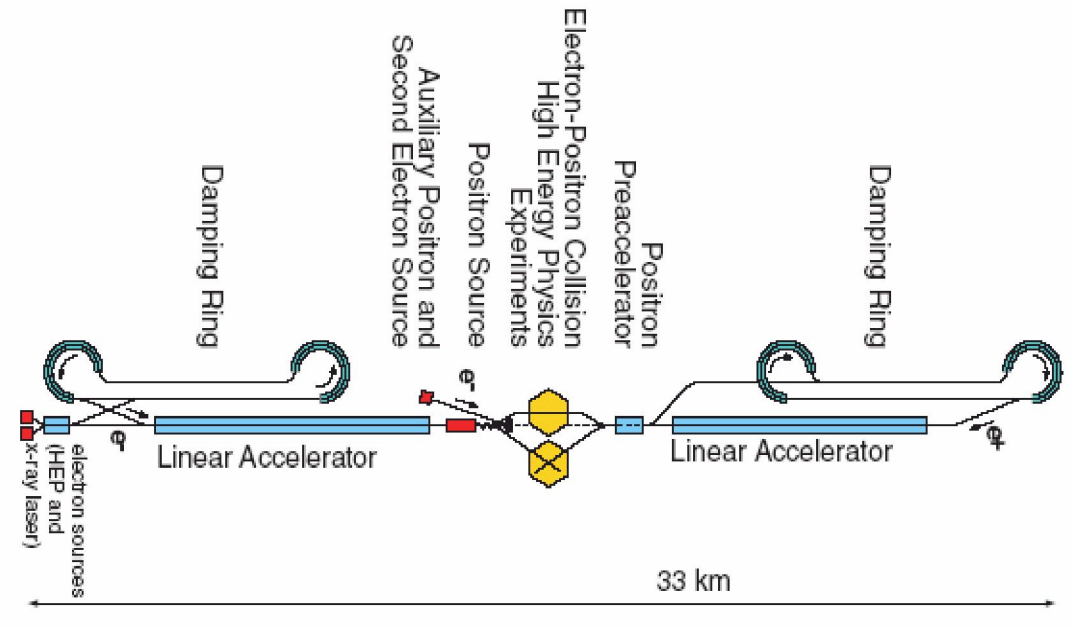


Figure 1.2 Schematical overview of TESLA facility with linear accelerator [5].

Taking into account the energy loss [7] due to the synchrotron radiation emitted by a charged particle that is accelerated on a circular ring (Figure 1.3), the following is given:

$$\Delta E \propto \frac{E^4}{R} \tag{1.1}$$

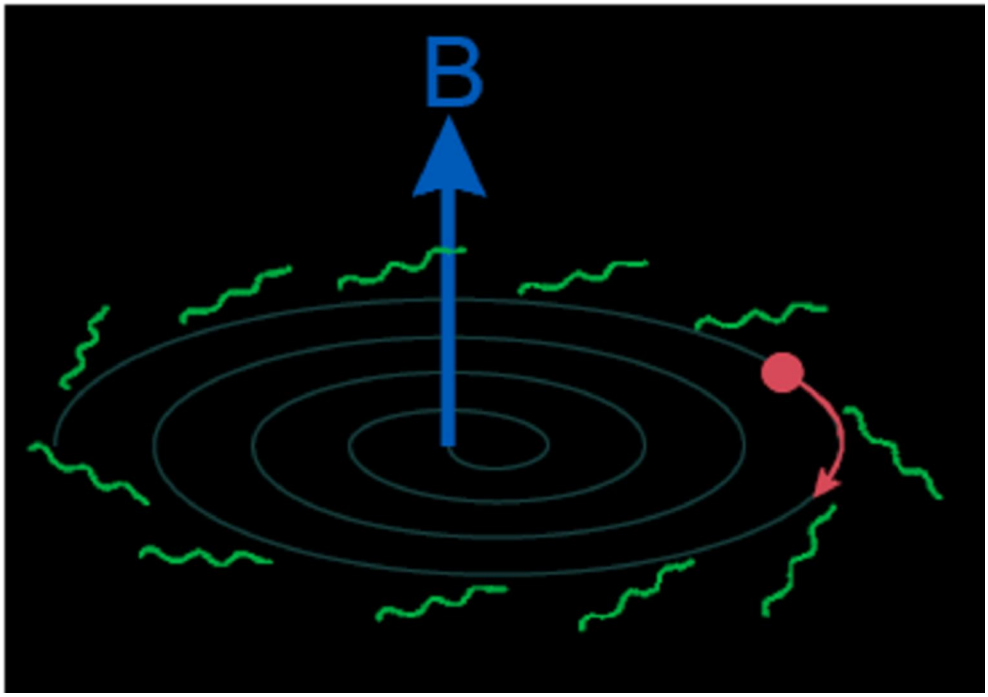


Figure 1.3 Charged particle is forced on a circular accelerator.

Where R is the radius of the circular ring. Observing the energy range and dimensions of the LEP collider at CERN, which stopped operating at the end of 2000, a list of parameters of the synchrotron radiations of a circular accelerator are shown in following Table 1.2 below.

	LEP II	Super LEP	Hyper LEP
ECMS (GeV)	180	500	2000
L (km)	27	200	3200
ΔE (GeV)	1.5	15	240

Table 1.2 Energy losses due to synchrotron radiation for different circular accelerator configurations [5].

In general, the energy losses are not so relevant for heavy particles in the high-energy region, e.g., protons. However, they can reach to about 10% per revolution for center of mass energy in the range of TeV and a radius of a million meters for electrons. From the economic point of view, this circular accelerator is not worth operating. For this reason, a linear accelerator should be operated instead of a circular one.

In the case of a linear accelerator, two important aspects have to be taken into account: the center of mass energy and luminosity. In order to meet the requirement of energy, the acceleration gradient should be much higher than that of a circular one. In addition, Figure 1.4 below shows a series of theoretical cross section for electron-positron annihilation processes with the center of mass energies up to 1 TeV. In case the collider is operated at high energies, the cross section is reduced. Since the expected event rate is

determined by both the luminosity and cross section, the luminosity of the beam must be increased to achieve a sufficient event rate.

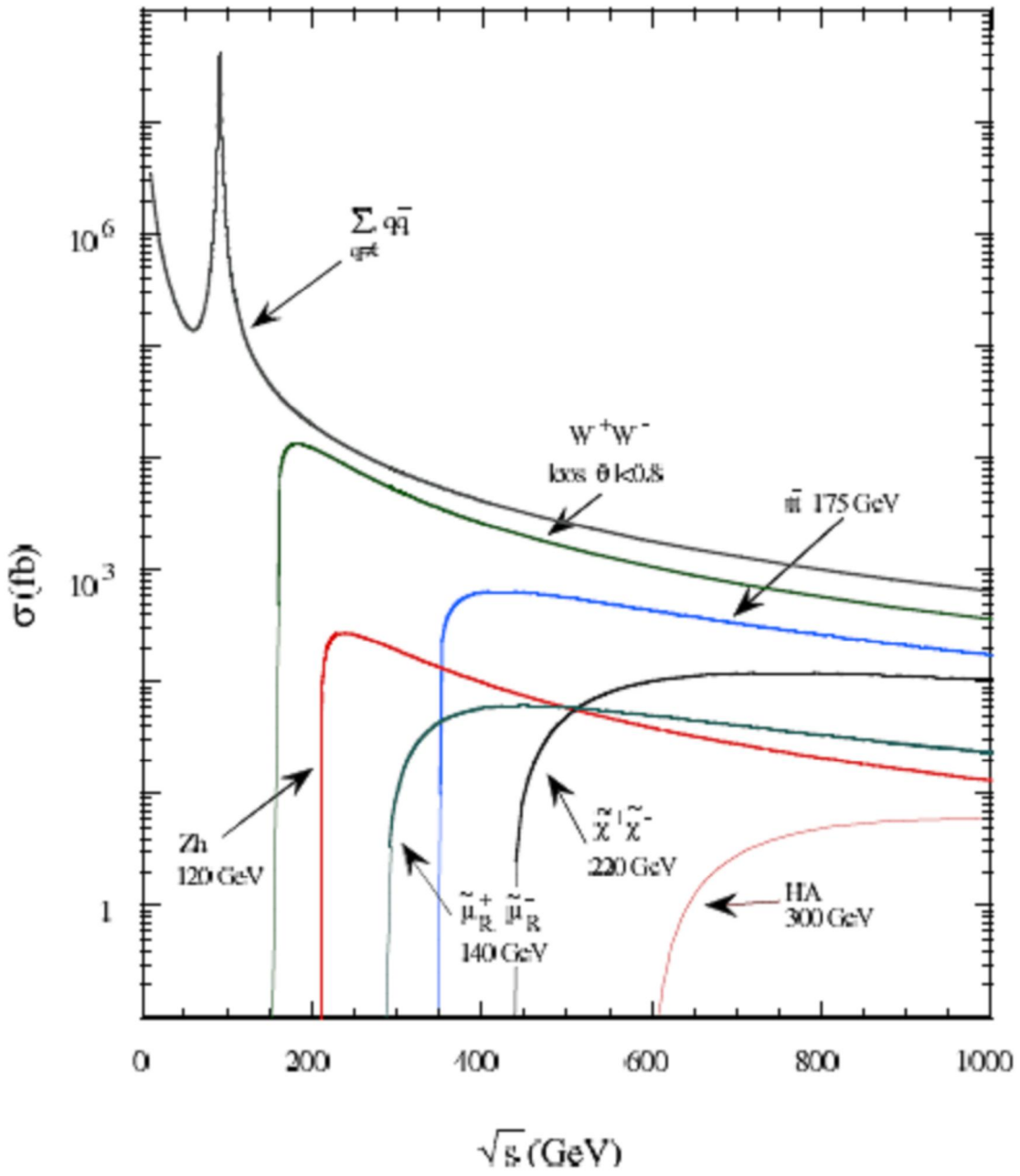


Figure 1.4 Expected cross section for selected electron-positron annihilation processes depending on the center of mass energy of the collider [8]

There have been many proposals [9] for such a machine with respect to this worldwide global project that can be distinguished by the selection of acceleration technology. After an intensive survey by an expert group (International Technology Recommendation Panel – ITRP) the superconducting RF technology for the acceleration of electrons and

positrons was chosen for the future linear collider, since then a further step towards the realization of the ILC was taken in 2004. Superconductivity technology offers zero resistance to electric current. In other words, there is no energy loss during current flow. This technology can be achieved with the superconducting material niobium at very low temperatures instead of copper structures that operate at room temperature. Thus, much better energy efficiency is achieved.

The ILC accelerator will be constructed according to this acceleration structure, which was initially proposed by the DESY in Hamburg and the TESLA (TeV Energy Superconducting Linear Accelerator) [18] technology collaboration. In the following the TESLA accelerator will be shortly introduced. A comprehensive overview of this project can be found in the TESLA Technical Design Report [10]. TESLA should include two facilities: one of them is the 33-km-long linear accelerator for particle physics that is used for the ILC project; it consists of electron and positron sources, and will be constructed for the first phase of the linear collider at 500 GeV in the center of mass. It will be extended in a second phase to 800 GeV or even more of course depending on the acceleration gradients achieved. Another is the integrated 4-km-long X-ray laser laboratory [11] that is operated as a Free Electron Laser (FEL) and will be constructed to provide coherent X-ray. Both of them are completely separated and are used as independent projects.

1.2.2 Detector concept for the international linear collider

Detector should have an excellent performance to fully exploit the physics potential at ILC. As mentioned previously, ILC is considered to be a precision machine that can measure the standard model physics processes near the electroweak energy scale and probably could find new physics beyond it. In order to take full advantage of the physics potential of the ILC, the performance of the detector components has to be optimized with respect to its special environment.

The detector at ILC should be significantly better than those at LEP and SLC accelerators. The most important requirements for the detector are summarized in the following [12]:

- Good charged track momentum
- Excellent vertex resolution for efficient b- and c-tagging
- Efficient track reconstruction in an multi-jet environment
- Good resolution provided by high granularity in the calorimeters and particular in the electromagnetic section, efficient electron and muon identification

- Hermeticity and particle-detection capabilities in the forward direction, since missing energy is the main expected signature for the characterization of SUSY and for other process of interest.

- Compatibility with a triggerless operation for maximal efficiency

At present there are three main detector concepts plus one: Large Detector Concept (LDC) from TESLA detector groups in Europe, the Silicon Detector Concept (SiD) from the US and Global Large Detector (GLD) from Asia; the fourth concept is still in progress. Figure 1.5 shows a schematic cross section through a typical detector. The main tracker in the center part of the detector is made up of a combined tracking system – Vertex Detector (VTX) / Intermediate Tracker (SIT) and Central Tracker (TPC).

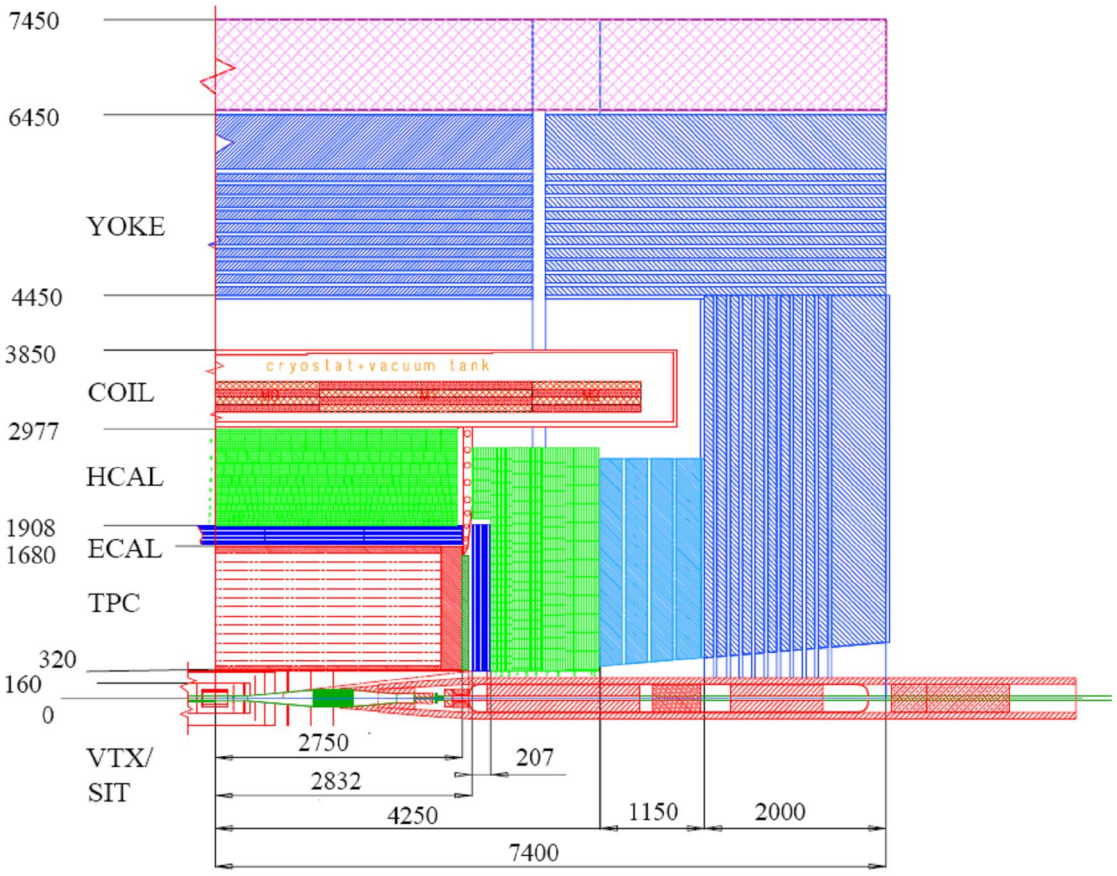


Figure 1.5 Schematic layout of a quadrant of the TESLA detector. All dimensions are in mm [12].

An electromagnetic calorimeter (ECAL) and a hadronic calorimeter (HCAL) are located direct outside of them. The magnetic field of 2-4 T provided by a coil helps to measure the momentum of charged particles and to further limit the beam-related background. With increasing field, the pair production background in the vertex detector is further reduced and the momentum measurement is improved by the tracking (providing a better resolution). It is worth having the electromagnetic calorimeter and part of the hadronic

calorimeter inside the coil to reduce the amount of the material for the detector taking consideration of the extra cost. Here the iron is used as a magnetic return yoke (muon chamber) and also as a tail catcher for hadronic showers outside HCAL. Resistive plate chambers (RPC) [13] are chosen as a choice for the detector technology. It is worth mentioning that the advantages of standalone track reconstruction are internal alignment optimization and reduction of track ambiguity.

In the following it will be discussed how these various components are optimized. As shown in Figure 1.6 a multilayer vertex detector is located as close as possible around the interaction point (IP) in the innermost part of the tracking system in order to provide an excellent impact parameter resolution. An efficient vertex detection has become the physics goal of the ILC. The physics signals are rich in secondary vertices, and event rates are limited; for this reason, the vertex detector is mainly optimized to reconstruct secondary vertices by b- and c-tagging to identify multi-b final states like ZHH and $t\bar{t}H$ and to separate $H \to c\bar{c}$ events from $H \to b\bar{b}$ decay. In addition to good impact parameter resolution the vertex detector can also provide an efficient momentum measurement. More requirements of vertex detector will be discussed in the next section in detail. Two additional layers of the silicon tracking detector (Silicon Intermediate Tracker – SIT), consisting of cylinders in the barrel, are placed between the vertex detector and the TPC to further optimize the momentum resolution of the tracking system. Seven discs in the forward region are laterally mounted along the beam pipe, since the combined vertex detector and TPC resolution degrades at low polar angle due to a shorter projected track length and additional information given by these discs makes momentum measurements more precisely. In addition, the discs can also improve the polar angle resolution in this area. The first three layers of this system that are closest to the IP are made up of active pixel sensors, and the outer four are silicon strip detectors.

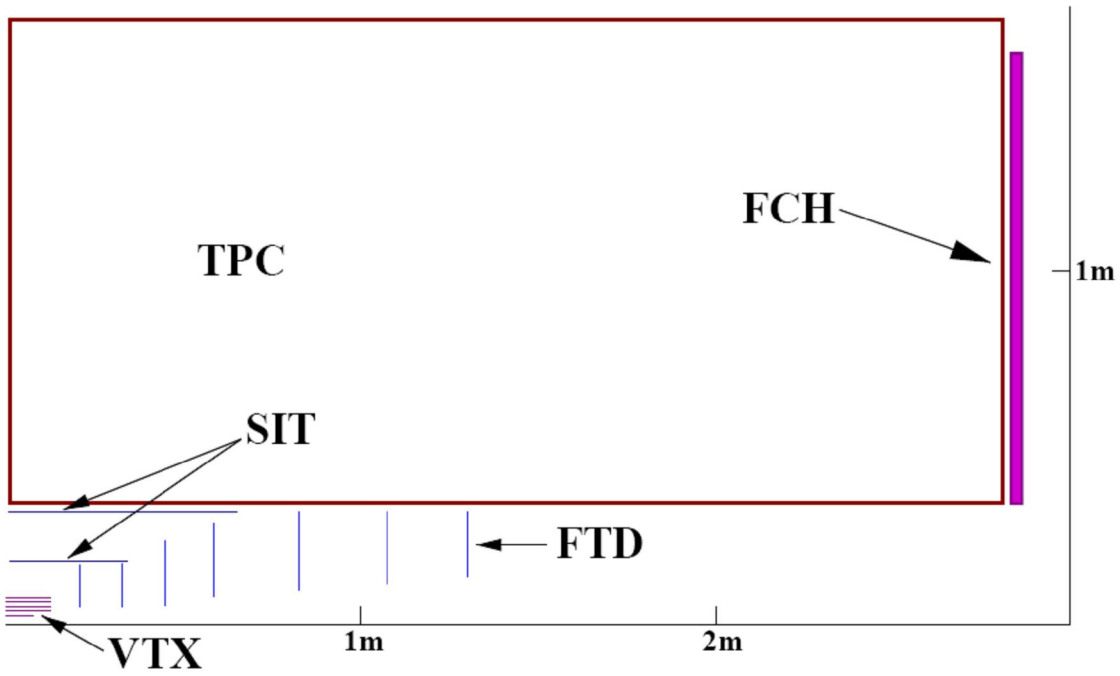


Figure 1.6 Schematic layout of the tracking system of the TESLA detector [12].

A large Time Projection Chamber (TPC) – a gaseous chamber with readout at the side via a fine segmented endplate is chosen as the central tracking device since it has many advantages compared to other techniques. The TPC provides good momentum resolution due to the large radius of the central tracker and a large number of precise spatial point measurements along the track can offer efficient pattern recognition even in a dense track environment. The TPC can enable good particle identification by measuring the specific energy loss of the charged particles. At last a TPC is easy to maintain since the endplate is divided up into small parts, which can be replaced and serviced if necessary.

A precise forward chamber is placed behind the TPC endplate (FCH) to compensate for the degraded track reconstruction performance of the TPC in the forward direction. In addition, it can also improve the momentum resolution in that region and assist the TPC in the pattern recognition. It is worth noting that the tracking system can provide an excellent momentum resolution of $\Delta(1/p) = 5\times10^{-5}(GeV/c)^{-1}$ (1/10 of LHC/LEP) in the central region [10].

As noted to meet the requirement at ILC, a detector capable of precision measurements is required. In order to fully exploit the clean experiment conditions of ILC, the detector must have the ability to present a complete picture of the newly produced particles as possible, e.g., for charged particles this is done by the tracker. How about the energy they achieve after collision? These considerations require a calorimeter with excellent performance and many important requirements, i.e., calorimeters must be significantly better in their features than the already existing identification device. For instance, in order to distinguish nearby flying particles, the calorimeter must be segmented finely, and each segmented section can be readout. Generally calorimeters are used to measure the energy of charged and neutral particles. Longitudinal and lateral segmentation enables the location of the energy deposition and makes it possible to identify not only electromagnetic and hadronic components of the showers produced by the particles but also muons. In addition, calorimeters can also be used for measuring missing energy, the characteristic signature of SUSY particles and of neutrinos.

1.2.3 DEPFET-based vertex detector for ILC experiment

As mentioned above the vertex detector in ILC experiments is located as close as possible to the interaction point. The physics motivation and requirement for the vertex detector will be dealt with in detail in the following section. Finally a proposal for MOSDEPFET-based vertex detector at ILC will be given.

Firstly the ILC needs a vertex detector with unprecedented precision that should allow efficient and good flavor identification and separation, for measuring branching ratios $H \to b\bar{b}, c\bar{c}, gg, \tau^+\tau^-$, SUSY Higgs searches such as $A \to \tau^+\tau^-$, searches for staus, top studies. It is also important to identify charm quarks for a complete reconstruction of

the kinematics, e.g., in the process $e^+e^- \to W^+W^- \to c\bar{s}l^-\nu$. In addition, physics requires an efficient b and c tagging including charge determination in a wide range of $\cos(\theta)$.

The average impact parameter of tracks of a B decay product is approximately 300 micrometers, which suggests that modest detector performance may suffice. However, this is misleading for several reasons: First of all, the average impact parameters for tau and charm particle decay products are 3–4 times smaller. In addition, improved detector systems based on the experience from LEP and SLD allow a correct assignment of all tracks to primary, secondary or tertiary vertices in order to determine the vertex mass and charge that could allow improved b/c separation and allow to separate between quark and anti quark like b or $\bar{b}$ and c or $\bar{c}$.

In vertex detectors, better tagging efficiency of the jet flavor is achieved by better spatial resolution and tracking efficiency. Vertex reconstruction is performed by extrapolating tracks measured by several layers of the detectors. In order to get a better vertex resolution and flavor tagging efficiency, the vertex detector should meet the following requirements:

- The length of the extrapolation should be as short as possible, i.e., the innermost layer should be as close to the interaction point as possible.

- In order to minimize the effect of multiple scattering, the thickness of the detector and supporting substrate should be as thin as possible, by which no cooling system should be required and material can also be saved.

According to TESLA TDR design the vertex detector would consist of nested low-mass spherical shells positioning at five different radii of a few centimeters (Figure 1.7); in every layer there is a set of detectors arranged in ladders designed in a cylindrical form. Each ladder is an array of pixel cells with readout system located at the end of ladder outside the sensitive volume and extends in length to cover a polar angle range of $|\cos\theta| \leq 0.96$ for layer 1 and 2 and $|\cos\theta| \leq 0.9$ for layer 3–5.

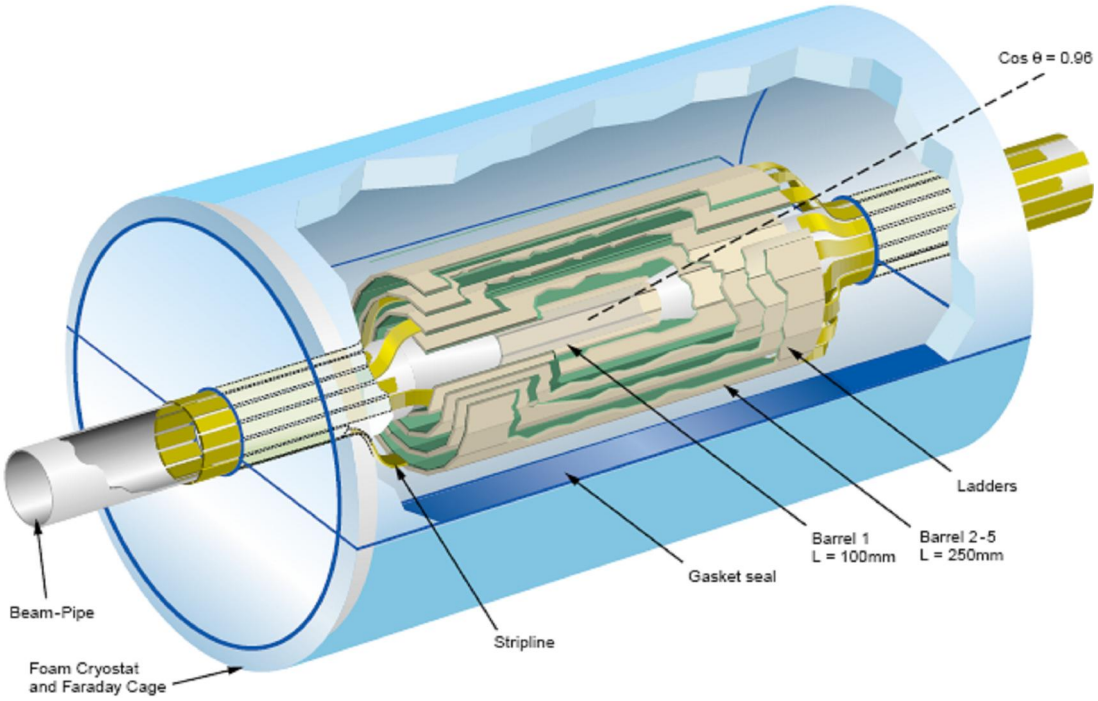


Figure 1.7 General layout of the vertex detector at ILC [16].

The impact parameter resolution is the key parameter of the vertex detector that is required separately in $r\phi$ and rz projections [17]. For a set of cylindrical detectors, this impact parameter resolution can be expressed as:

$$\sigma = \sqrt{a^2 + \left(\frac{b}{p \sin^{\frac{3}{2}} \theta}\right)^2} \tag{1.2}$$

Where the constant a depends on the point resolution and geometrical stability of the detectors and b represents the resolution degradation due to multiple scattering, which changes with track momentum p and polar angle θ.

The impact parameter resolution to be reached is $\sigma(IP_{r\phi,z}) = 5\mu m \oplus \frac{10\mu m\, GeV/c}{p \times \sin^{3/2}\theta}$. The innermost layer of this five-layer-type vertex detector, right outside the beam pipe, should be at a radius of 15mm and have a length in z of $\pm 50mm$. A summary of the radii and dimensions of all five layers can be found in Table 1.3.

Layer	Number of ladders	Radius (mm)	Ladder length (mm)	width (mm)
1	8	15.0	100	13
2	8	26.0	2×125	22
3	12	37.0	2×125	22
4	16	48.0	2×125	22
5	20	60.0	2×125	22

Table 1.3 General geometrical parameters of the MOSDEPFET-based vertex detector at ILC [61].

In addition to impact parameter resolution the detector should also have stand-alone pattern recognition and tracking capabilities for the reconstruction of tracks with low momentum. In order to achieve the desirable resolution especially at low momenta, a point resolution of less than four micrometers is required and the requirement on the material budget of a detector layer with a radiation length of less than 0.1% should also be met.

Taking into account Equation 1.2, the impact parameter resolution is determined by both the point resolution and the detector layout. The detector technology and the radius of the innermost detector layer are controlled by the expected occupancies. These are due to both the track density in jets and time structure and the background conditions of the accelerator. With respect to the time structure of the ILC beam (shown in Figure 1.8) [9], 2820 bunch are delivered within 950 microseconds with a corresponding bunch interval of 337 ns followed by a long gap of 199 ms. It is impossible to read out a full frame of a pixel sensor within a bunch spacing without integrating several bunch crossings for the detector. Without compromising pattern recognition and track reconstruction the amount of the integrated bunch crossings depends on the beam associated background.

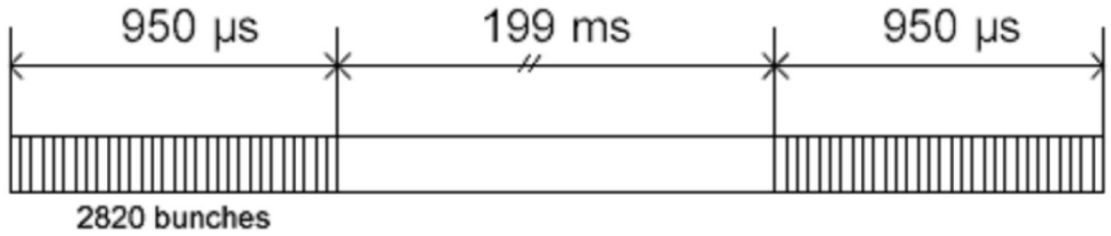


Figure 1.8 Time structure of the ILC accelerator [9].

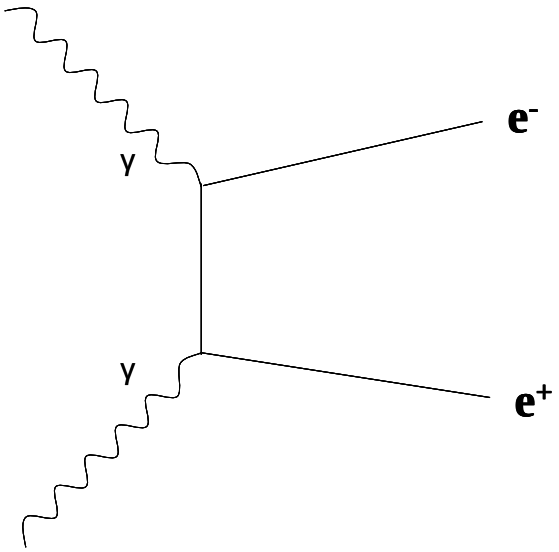
Normally the background for e^+ e^- colliders is relatively low compared to hadron colliders; however, the detector at ILC will be confronted with a considerably higher background environment than that at LEP or SLC. This higher background arises mainly

from beam-beam interactions (e^+, e^- and γ), synchrotron radiation and from muon and neutron sources. Particles from beam-beam interactions generated at the IP that cannot be shielded from the detector volume are responsible for much of the background in the detector. In principle, the beam-beam interaction leads to two main experimental consequences: Firstly, the energy distribution will be widened because of the emission of photons by a beam in the field of the oncoming beam; secondly, the subsequent background is produced by interactions of those photons. Below various physics process for the beam-beam interaction will be discussed:

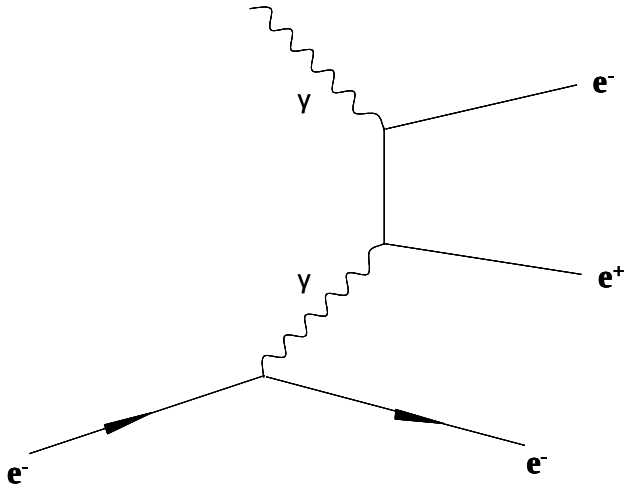
- Pair production through the interaction of a photon with the collective field of the oncoming beam is called coherent $e^+ e^-$ pair production [14]. In case of ILC detector, this contribution is of no importance.

- Pair production via the interaction with the field of an individual particle is called incoherent $e^+ e^-$ pair production [16]. The following three processes are the main source of background at the present generation of LC

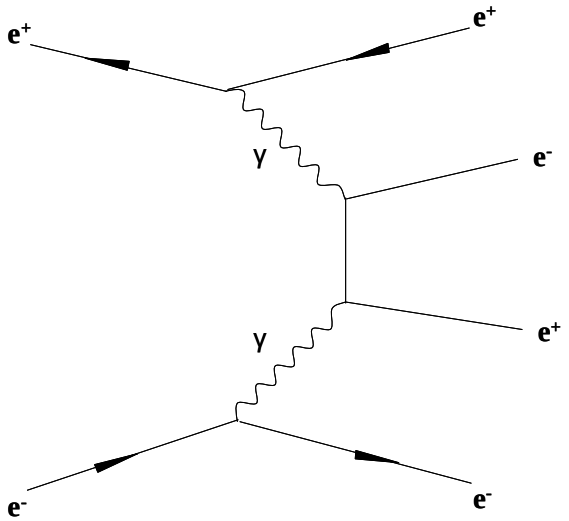
    - The Breit-Wheeler process ($\gamma\gamma \rightarrow e^+e^-$) – describes the interaction of two real photons



    - The Bethe-Heitler process ($e^{\pm}\gamma \rightarrow e^{\pm}e^+e^-$) – describes the interaction of one real and one virtual photon



- The Landau-Lifschitz process ($e^+e^- \rightarrow e^+e^-e^+e^-$) – describes the interaction of two virtual photons



The dominant $e^+ e^-$ pair background from the beam-beam interaction is confined with a small radius by the high magnetic field of 4T. For this reason, a strong peak for the background rate is found close to the IP and then it falls rapidly in layer 2-5. The beam pipe radius of the collider machine is set at 1.5cm. The pair background in layer-1 right outside the beam-pipe produces a hit density of 0.03 (0.05) hits per BX and mm^2 for $\sqrt{s} = 500\,(800) GeV$ [12].

In order to meet the requirement set by the ILC environment, a proposal using DEPFET – an active pixel sensor with an integrated amplification – is made. The basic principle of such a structure is the integration of amplifying FET transistors into a fully depleted bulk in such a way that all signal charges are collected in the 'internal gates" of the transistors

(see next chapter for details). The key features of this structure, which make it an ideal candidate for the vertex detector at ILC, are summarized as follows:

- Low pixel size ~ 20-30µm
- Fast collection of large signal
    - Charge collection arises from the fully depleted bulk
- Low noise through small capacitance (several 10 fF) of the internal gate
- High frame readout rate ~ 20kHz
- Charge generation and first amplification in a fully depleted FET
    - à Good Signal/Noise (40:1)
- No charge transfer needed (unlike in a Charge Coupled Detector (CCD))
    - à Radiation hardness against hadron irradiation
- Thinner detector of ~ 50 µm using thinner technology (HLL)*
    - à Less material ~ 0.1 %X_0 each layer
- Charge collection in "OFF" state, only one row active during readout:
    - à Low power consumption
- Production technology completely under the control of detector designers and physicists

To date, no show limits are known with respect to DEPFET – only its many advantages; for this reason it could compete with other alternative candidates – like Charged Coupled Devices (CCD), CMOS Monolithic Active Pixel Sensors (MAPS) and Hybrid Active Pixel Sensors (HAPS) – for the vertex detector at ILC. Each has its own disadvantages: CCD may be limited by the radiation tolerance and higher readout speed; CMOS sensor (MAPS) cannot be produced in large area devices; the layer thickness and power consumption of HAPS is too high.

* HLL: Semiconductor labor Munich

1.3 Irradiation Tolerance

Due to the high background the question should be considered for radiation damage to the DEPFET-based vertex detector at ILC. Therefore, a requirement of radiation hardness of about 100 krad for a 5-year life time is needed [2]. Since such detectors are produced by MOS technology and almost all of the MOS devices are sensitive to ionizing radiation, damages will be generated in the oxide and interface between silicon and SiO_2 and play an important role on the MOS-structure-based devices. The main total ionizing dose effects are summarized as follows:

- The threshold voltage shift (due to radiation-induced positive oxide charges)
- The increased subthreshold slope
- A higher low-frequency noise (due to interface traps generated between Si/SiO_2)
- The degradation of the transconductance (due to a lower mobility of the charge carriers in the channel after irradiation)

On the other hand, unlike the background at LHC, bulk damage due to NIEL (Non Ionizing Energy Loss) at ILC is arising from the neutron background, which is estimated to be at the level of 10^9 /cm^2 (1MeV-neutrons) per year. It is not so relevant for the DEPFET-based vertex detector, since there is no charge transfer (charge trapping) during the operation of DEPFET matrices. However, with increasing doses from proton or neutron sources, radiation damages will be generated in the silicon bulk volume that affect the performance of MOS devices. These bulk damages result in leakage current, which leads to a higher noise. As a consequence, a radiation tolerance against proton or neutron sources is limited to an order of magnitude of 10^{12} /cm^2.

Depending on different technologies (e.g. improved oxide processing) and irradiation conditions, the degradation of MOSDEPFET transistors is characterized by a series of parameters and experimental methods.

In order to study the radiation hardness of the detectors, several MOS test devices were constructed and irradiated.

1.4 Silicon detectors

A silicon detector is a device that uses a silicon diode operated under reverse bias to detect traversing charged particles or the absorption of photons, where the depleted zone of the silicon diode acts as a solid ionization chamber. Silicon detectors have found many applications, especially for X-ray spectroscopy and as particle detectors in high-energy physics. The passing ionizing particles ionize the silicon atoms and, therefore, create numerous electron-hole pairs along their track, which will drift to the electrodes following the electric field in the depletion zone. A minimum ionizing particle (MIP) traversing a silicon layer will create about 80 electron-hole pairs per micrometer, since the required average energy to produce an electron-hole pair is about 3.6 eV. It is about 30 eV for gases. The resulting signal can be detected by a charge sensitive amplifier. The output is proportional to the overall generated charges in the detector if the detector is fully depleted.

A comparison with other detector materials (gas detector or scintillation detector) shows that silicon is still the best choice of material for tracking purposes. On the one hand, silicon detectors have much higher density (Silicon: 2.33 g/cm^2) than gas detectors; on the other hand, their intrinsic energy resolution is much better than the scintillation detectors.

Interaction of charged particles with detector materials takes place by electromagnetic interaction with the electrons of the atom shell. Two processes are generally used to identify the particles:

- Excitation
    - Excitation of the atoms and molecules of the detector materials through charged particles à fall-back to ground state à emission of light à changing of light into electric signal (identification through e.g. Photomultiplier or Avalanche Photo Diodes)
- Ionization
    - Ionization of detector materials through charged particles à generation of free charge carriers à charge collection to the electrodes through a electric field à electric amplification through charge sensitive amplifier à registration of signals (identification through silicon detectors e.g. strip detector or pixel detector)

The energy loss for charged particles traversing materials is given by the Bethe-Bloch formula with respect to heavy particles [59]:

$$-\frac{dE}{dx}=\frac{4\pi z^2 e^4 nZ}{m\beta^2 c^2}\left(\ln\left[\frac{2m\beta^2 c^2}{I}\gamma^2\right]-\beta^2-\frac{\delta}{2}\right) \tag{1.3}$$

With

- m : rest mass of electrons
- $\beta := v/c$ relativistic velocity of particles
- $\gamma := \left(1-\beta^2\right)^{-1/2}$ Lorenz factor
- $z\,e$: electric charge of particles
- Z : atomic number of materials
- n : atom number per unit volume
  $= \rho A_0 / A$; A_0 : Avogadro-number; A : atom mass, ρ : matter density
- δ : density parameter
- I : characteristic ionization constant

The energy loss for electrons or positrons by interaction with materials is proportional with energy [59]:

$$-\frac{dE}{dx}=\frac{E}{X_0} \tag{1.4}$$

With X_0 : radiation length.

According to requirements of application areas, a highly precise measurement of particle energy is required and performed by a better proportionality of generated charges with deposed energy (X-ray spectroscopy). The main concern of high-energy physics is fast particle readout and high position resolution. A single PN-junction can be used for detection of an ionizing particle but cannot provide any position information about the particles track. For this reason it is necessary to segment the diode into an array of smaller individual PN-junctions. Depending on the type of segmentation of detector electrodes they can be classified into strip and pixel detectors, which can be produced by modern planar technology.

- Strip detectors: a type of detector based on a segmentation of the p^+/n^+ implantation into a periodic arrangement of strips. Typical dimension of the strip length is several centimeters whereas the pitch is several tens of micrometers. Normally strip detectors provide information about only one dimension position of particle track. The spatial resolution can be determined by $pitch/\sqrt{12}$ for binary readout. In order to obtain the second dimension, it is necessary to pattern the backside of detectors into the strips as shown in Figure 1.9. The disadvantage of a double-side strip detector is the presence of ambiguities if two or more particles pass the

detector simultaneously. In addition, insulation problem should also be taken into account between each n^+n strip from its neighbors for double-side strip detectors. Typical solutions against this problem are p-spray technique or p-implantation between every n^+n strip.

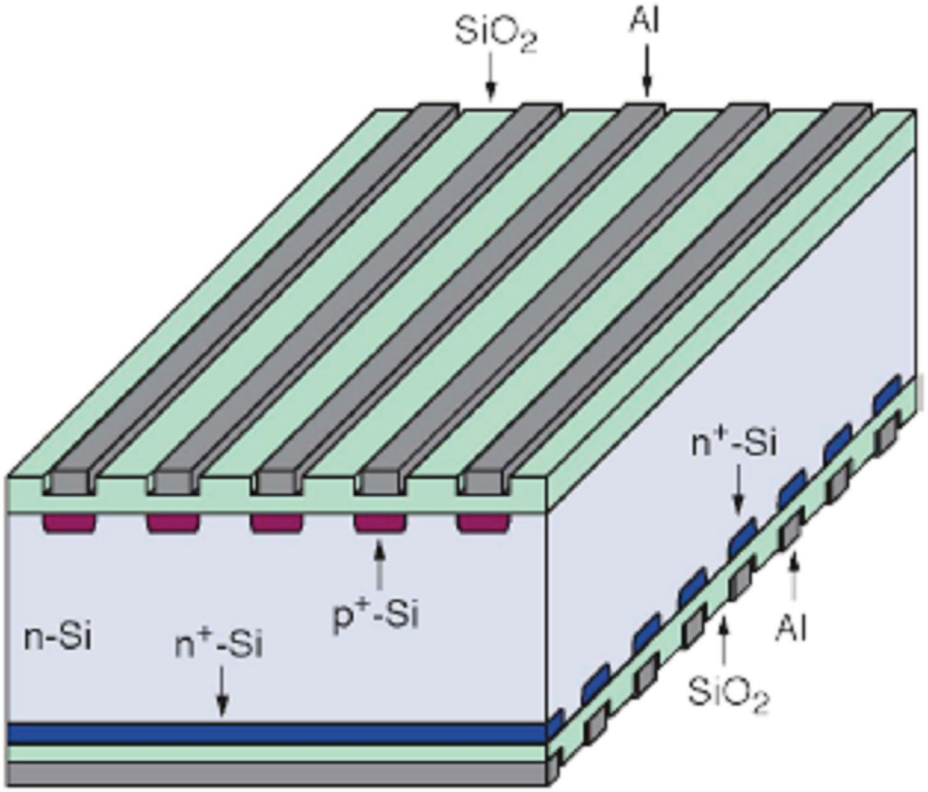


Figure 1.9. Layout of a two-dimension silicon micro strip detector [62].

- Pixel detectors: a detector produced by segmenting p^+ implantation of the strip detector into an array of diodes (Figure 1.10). Pixel detectors can provide a two-dimensional localization of particle track without ambiguities like double-side strip detectors.

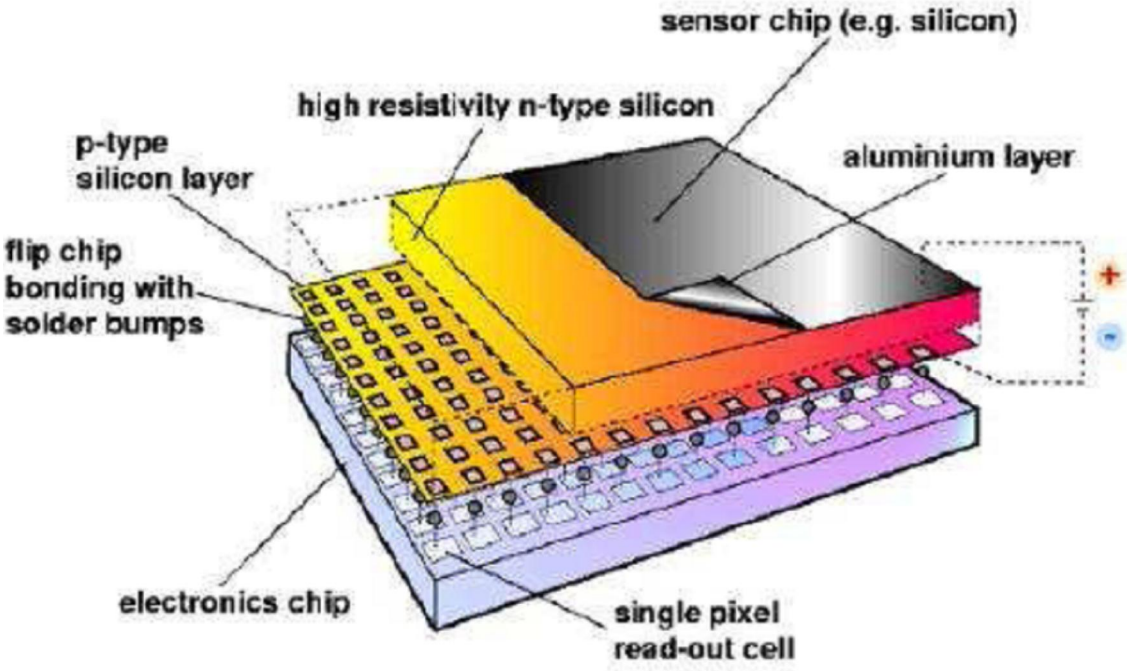


Figure 1.10. Layout of a pixel detector [63].

Chapter 2 MOS Structure

For a long time, silicon has been widely used as material in semiconductor devices. Moreover, Metal-Oxide-Semiconductor (MOS) structures became the most important component in silicon semiconductor devices, e.g. MOSCCD, MOSFET, CMOS, and so on. Study on the radiation damage of MOS-Structure under different radiation sources has received extensive attention in the past few years in order to understand the radiation-induced performance degradation of silicon devices. A great deal of effort has been made to correlate the changes in the electrical properties of irradiated silicon devices with the type and dose of irradiation. At the same time the widely used silicon detector in High Energy Physics (HEP) experiments has implied that there is a close relationship between fundamental study and technology development. A detailed analysis of radiation damage correlated with fundamental material research needs to be given in the irradiated silicon detector. Accordingly, anticipated improvement of radiation damage for future HEP experiments will be achieved through improved technological development and optimized detector design.

2.1 MOS DEPFET

The metal oxide semiconductor depleted field-effect transistor (MOSDEPFET) is one type of field-effect transistors. Principally it can be distinguished from the depletion field-effect transistor (JFET) and metal oxide semiconductor field-effect transistor (MOSFET). The highlight of DEPFET is the quite small input capacitance of only a few tens of fF, and from the point of view of functionality it simultaneously has detector and amplification properties. In the following chapter more details about MOSDEPFET will be presented.

2.1.1 Definition of a MOSDEPFET

The depleted field-effect transistor (DEPFET) was proposed in 1987 by Kemmer and Lutz [19], and experimentally confirmed by Kemmer et al. in 1990. MOS-type DEPFET offers a solution to combine depleted silicon volume and amplification level (MOSFET). These substrates are depleted by means of sideward depletion [20]. The principle of sideward depletion is represented in Figure 2.1 below. This structure is not a single PN diode, but a combination of two PN diodes contacted with each other by the same doping side to form a PNP or NPN sandwich. Considering PNP structure, if a small negative voltage is applied to both P-contact with respect to substrate (here N side in between),

there are two space charge regions generated and separated by the conducting undeleted bulk region (here N volume); in the case of higher voltage, the device volume is depleted from both sides of the PN diodes.

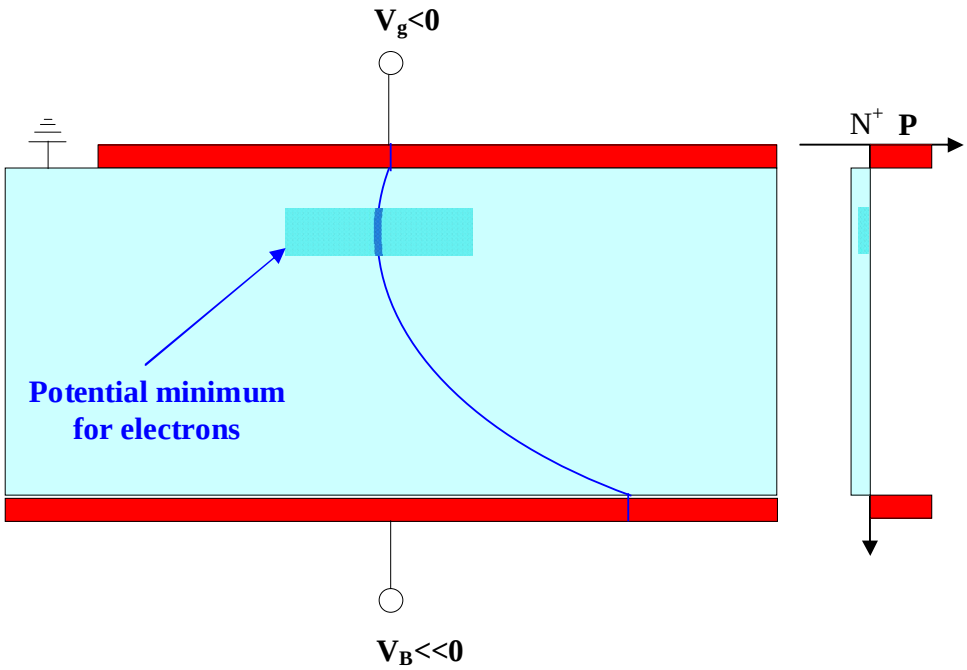


Figure 2.1 Principle of sideward depletion and distribution of doping and potential in the substrate.

When two unequal negative voltages are applied on both sides, under fully depletion a potential minimum for electrons is created assisted by an additional deep n implantation right below the gate contact (shown in the above Figure marked with sky blue), which is parallel to the front side. This potential minimum is for majority carriers: electrons in n-type silicon.

In order to analyze the behavior of MOSDEPFET, it is necessary to firstly consider a normal MOSFET that contains three terminals: Gate, Source and Drain. If the MOSFET is an n-channel MOSFET, then the source and drain are n+ regions and the substrate material is a P region. In case the gate voltage is above a threshold voltage value, electrons from the source and drain will enter the inversion layer at the interface between the P region and the oxide to form the conduction channel. If the gate voltage is below the threshold value ($V_{GS}<V_{th}$), there is only a very small subthreshold current flowing between the source and the drain. This region is called the cut-off.

The transistor is turned on and behaves like a resistor, which can be controlled by the gate voltage to the source, if $V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} - V_{th})$. It is shown in Figure 2.2 as a linear region.

$$I_D = \frac{W}{L}\mu C_{ox}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{2.1}$$

In case where the drain voltage is higher than the gate voltage ($V_{GS} > V_{th}$ and $V_{DS} > (V_{GS} - V_{th})$), the drain current reaches a saturation value (shown in Figure 2.2 called the saturation region).

$$I_D = \frac{W}{L}\mu C_{ox}(V_{GS} - V_{th})^2 \tag{2.2}$$

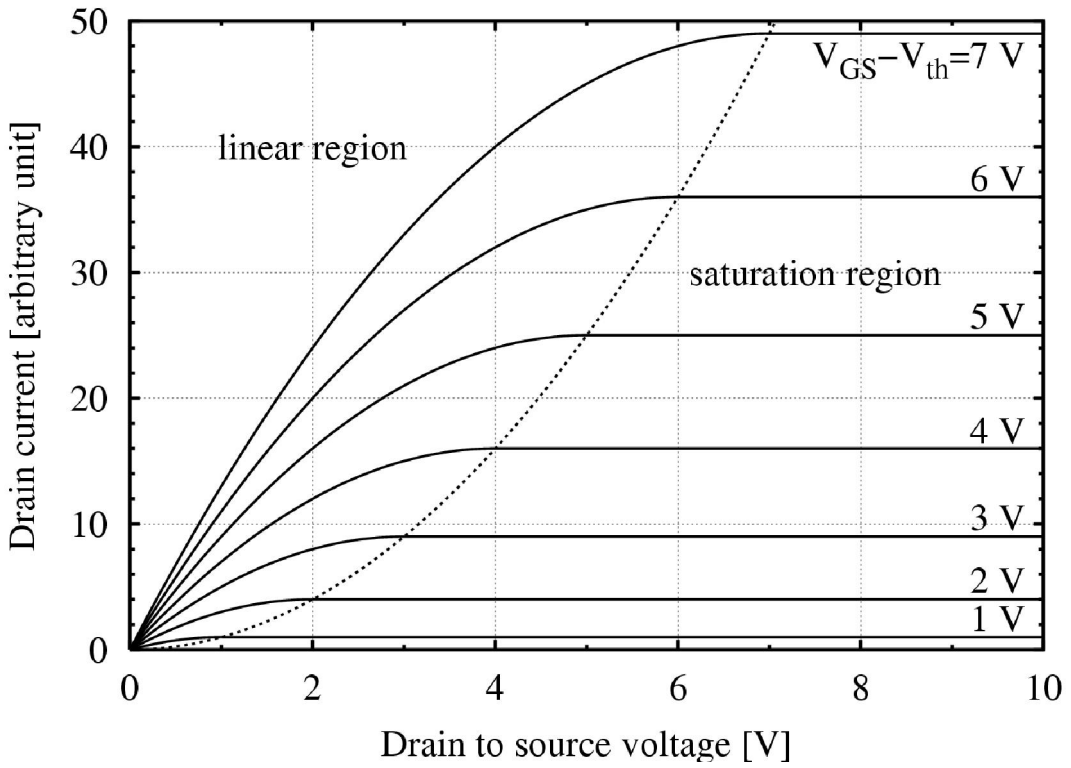


Figure 2.2. MOSFET drain current I_D vs. drain-to-source voltage V_{DS} for several values of $V_{GS} - V_{th}$; the boundary between linear and saturation modes is indicated by the dashed line [60].

Another important parameter is the transconductance, which is defined as:

$$g_m = \frac{\partial I_D}{\partial V_g} \tag{2.3}$$

Using equations 2.1 and 2.3

$$g_m = \mu C_{ox}\frac{W}{L}V_{DS} \tag{2.4}$$

It is obvious that the transconductance increases linearly with V_{DS} but does not depend on V_{GS}. For a given device geometry (channel width W and length L) and a given V_{DS}, the mobility μ depends on the carrier scattering due to the oxide charges and interface traps. Accordingly, the transconductance will be reduced due to ionizing radiation.

With respect to saturation region, combining equations 2.2 and 2.3 gives

$$g_{m_{sat}} = 2\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th}) \tag{2.5}$$

Therefore, the transconductance in the saturation region is linearly proportional to V_{GS} but does not depend on V_{DS}.

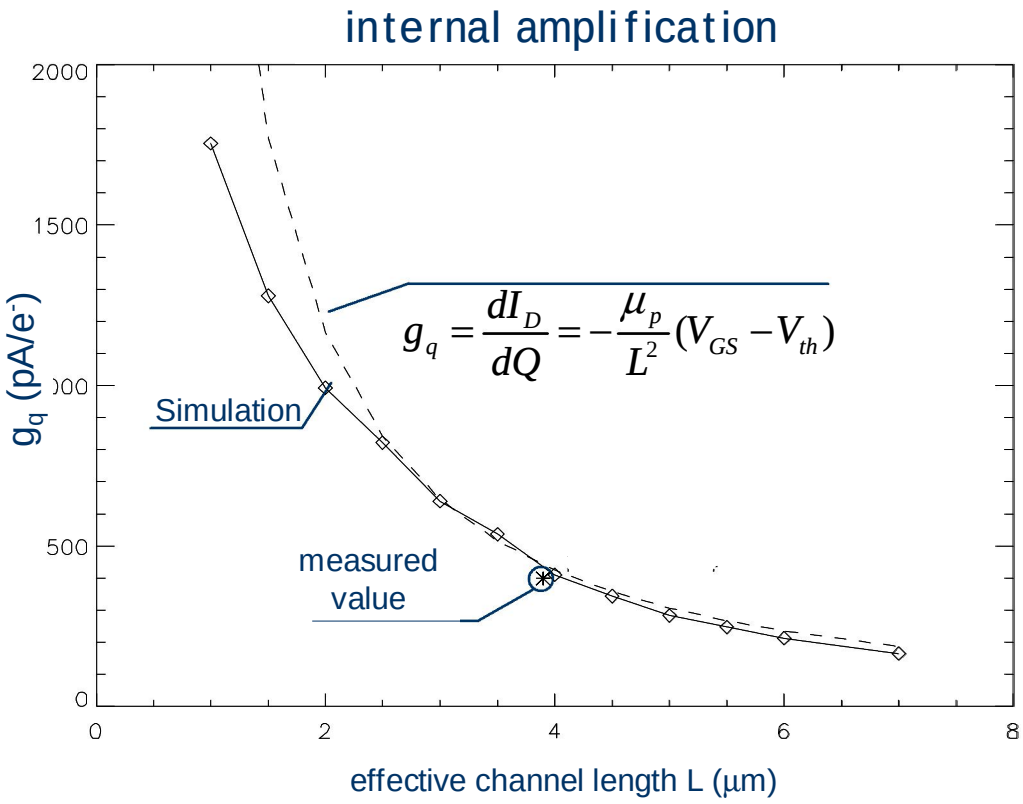


*Figure 2.3. Dependence of the charge amplification g_q on the channel length. ◊: 2 dimension TesCA simulation (50 µA drain current); *: measurements with 50 µA drain current. [Performed by Rainer Richter]*

The drain current response to a given signal charge defines the amplification of the internal gate, which can be defined as:

$$g_q = \frac{dI_D}{dq} \tag{2.6}$$

The amplification g_q is dependent on $1/L^2$ and carrier mobility for a given gate voltage [61].

2.1.2 Operation of MOSDEPFET

The MOSDEPFET principle of operation is shown in Figure 2.4 [2]. A MOS field-effect transistor is built on top of the detector substrate. Two terminals (source and drain) are connected by the transistor channel, which is created by biasing of a MOS gate contact in order to form an inversion layer at the interface between oxide and silicon. The gate voltage can steer the conductivity of the channel. By means of sideward depletion the whole substrate is fully depleted, and a potential minimum for electrons is created underneath the MOS transistor channel at a depth of about 1 micrometer. By ionizing radiation there will be electron-hole pairs generated in the depleted bulk, holes will move towards the backside of the substrate, electrons will be collected in the potential minimum (internal gate) where they are stored. These collected signal charges result in a change in the potential of the internal gate, which modulates the channel current of the transistor. The non-destructive readout mode can be repeated several times. After signals are read out, the signal charges and collected electrons in the internal gate can be removed through a positive voltage applied on the clear contact.

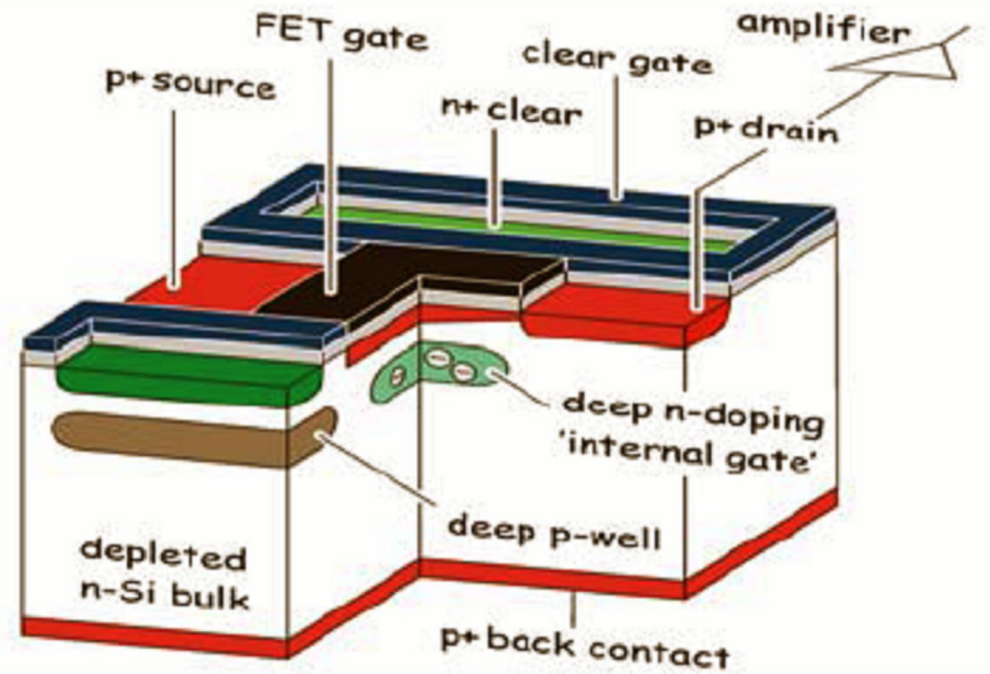


Figure 2.4 Linear MOSDEPFET with internal gate as charge collection and clear gate as clearing of signal electrons [2].

In addition, the potential barrier between the internal gate and the clear contact can be lowered by an additional clear gate (shown in Figure 2.4). If the internal gate is not located close enough to the surface, a significant fraction of the signal charges is lost in the source and drain of the transistor. As a consequence, the signal charge modulating the transistor current will be reduced. By means of an additional N-implantation underneath the transistor, the internal gate will move much closer to the transistor channel. Two available readout modes are source follower and drain readout. The latter has some attractive advantages, i.e., it offers much faster operation which is especially important for ILC experiment.

The feature of the simultaneous detection and amplification of a MOSDEPFET is important for the low noise operation.

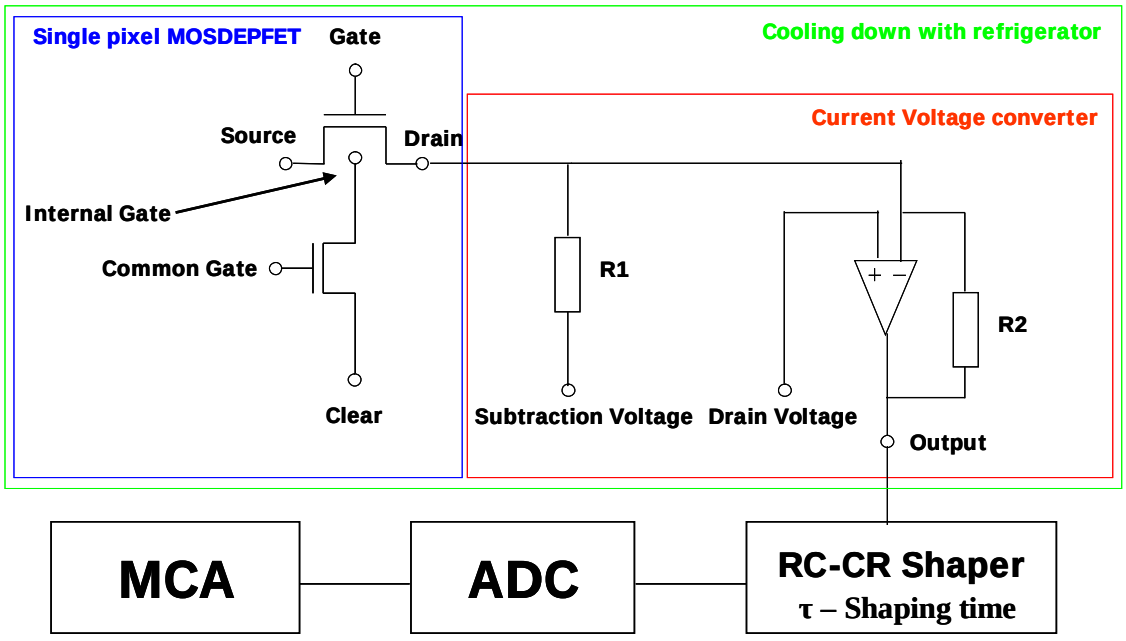


Figure 2.5 Experimental setup for the measurement of spectroscopic performance for the single-pixel MOSDEPFET.

In addition to the application of ILC, MOSDEPFET can also find use for X-ray spectroscopy [21]. Using Fe^{55} radiation, the spectroscopic performance of a DEPFET can be measured. The whole experimental setup can be found in Figure 2.5. Drain current is firstly read out using a current/voltage converter; furthermore, the signal is formed by a shaping amplifier that is operated through series differential element (CR) and integration element (RC) — differential element is used as a high-pass filter and integration element as a low-pass filter, whose characteristic parameter is the time constant:

$$\tau = RC \tag{2.7}$$

In general, the stepwise input signal can be converted into an exponential falling output signal by CR differential elements, while the RC integration element can convert the

input signal into an exponential rising output signal. Hence, a Gauss-shaped signal is achieved accordingly through a combination of a CR differential element and a couple of RC integration elements. Furthermore, the analog signal coming from the shaper is converted into digital signal by SILENA ADC. Using a multi-channel analyzer the signal can be sorted to different channels by its amplitude. Of course, in order to assign the channel number to the corresponding energy, a precision energy calibration should be done with the help of the well-known characteristic lines of the recorded spectrum. An example of the spectrum is shown below in Figure 2.6.

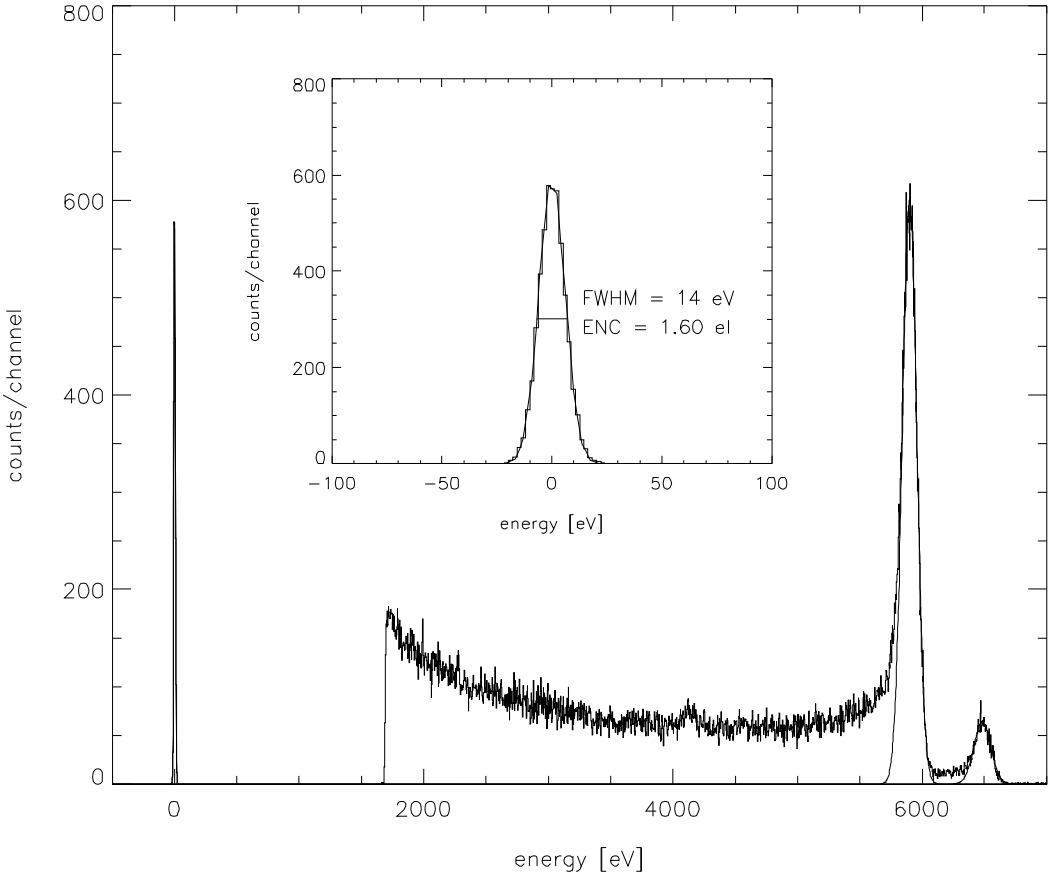


Figure 2.6 Spectroscopic performance of a linear MOS-type DEPFET (with gate length L=7um and gate width W=25um) before irradiation at room temperature, integration time is set to 10us. The insert shows the noise peak with an ENC (rms) =3.5e-(Performed by Laci Andricek).

2.1.3 Noise

Noise measured in spectroscopy can characterize the detector properties. Normally it is determined in the unit of equivalent noise charge (ENC) [25.26.27.28]. The noise of a DEPFET can be written as follows:

$$ENC^2 = \alpha \frac{8kTg_m}{3g_q^2\tau} + 2\pi a_f C_{tot}^2 + qI_{leakage} n\tau \qquad (2.8)$$

The first term of Equation 2.8 is the series white noise (or thermal noise), which depends on the integration time τ, temperature T, the transconductance of the DEPFET g_m, the charge amplification of the internal gate g_q and a factor α that depends on the exact shaping of the amplifier; the second term is series low-frequency noise, which depends on the effective capacitance C_{tot} and the normalization factor a_f; the third one is parallel noise (or called shot noise) due to the leakage current $I_{leakage}$ and integration time.

From the point of view of physical origin for the noise, series white noise is due to the resistor and is generated in the transistor. This white noise arises from the Brownian movement of the electrons in the channel and leads to different potentials and thus fluctuating voltages at the two contacts (source and drain), which can be measured as noise voltage. The low-frequency noise occurs due to the active traps located in the transistor channel, which can capture or emit charge carriers. This will affect the electric field in the transistor channel and accordingly also the current in the channel. For this reason low-frequency noise is generated. The variation of the electric field is determined by the trap density and the related capture cross-section and emission rate. The parallel noise is formed by currents that come from any electric input. The original source of parallel noise is the surface leakage current due to the interface traps induced by ionizing radiation and the leakage current from the silicon bulk due to thermal generation of electron-hole pairs. There are energy levels within the band gap due to either defects in the silicon crystal lattice or contaminations from metal foreign atoms. In general, there is an expectation of temperature-dependent leakage current — leakage current decreases in factor of two by a temperature reduction of about 7K, in the case of the energy level of the traps staying in the middle of the band gap. On the other hand, leakage current through the gate contact and also the feedback current through the feedback resistor in the preamplifier can contribute to the parallel noise.

In order to minimize the noise in the detector, it is necessary to reduce primarily the parameters like capacitance, temperature and leakage current. The capacitance can be minimized by a reduced gate area — reduced input capacitance (à reduction of low-frequency noise). As shown in Figure 2.5, the detector and readout system can be placed in a refrigerator to cool down the detector to reduce the leakage current (à reduction of the parallel noise). In addition, the noise components depending on the integration time in a manner that the first one – serial noise is proportional with the reciprocal of integration time $\sim 1/\tau$, the second one – serial low-frequency noise does not depend on the

integration time and the third one – parallel noise is direct proportional with integration time $\sim \tau$. For the sake of optimized energy resolution, a compromise between serial white noise and parallel noise due to different dependence of integration time can be found by a lower temperature. Consequently, the noise is given as a function of integration time.

2.2 MOS capacitance

In order to study the quality of the oxide, the easiest way is to use a MOS capacitance (MOS: Metal Oxide Semiconductor) [23]. The main reason to research the MOS capacitance is to understand the principle of operation as well as the detailed analysis of the MOS Field-Effect Transistor (MOSFET). The MOS structure is one of the simplest structure and most important component in many semiconductor devices and ideal probe to understand properties of the SiO_2. In this chapter the basic principle for understanding of the functionality of a MOS capacitance will be presented.

2.2.1 Definition of a MOS structure

The profile of an ideal MOS capacitance is schematically shown in Figure 2.7. On the left hand side, an equivalent circuit diagram is shown, which consists of oxide capacitance and capacitance of the depletion layer. Within the scope of this thesis, n-type silicon substrate is used to produce MOS capacitance. At first, a layer of SiO_2 is grown on the substrate at about 1050 degrees by thermal oxidation. In general, the silicon substrate has a thickness of 450 micrometers. For the gate contact two different materials are mainly used: either Aluminum or poly silicon (Figure 2.8). In the next chapter results from irradiation experiments will be generally discussed based on these two structures. Normally the gate contact is about 10 mm^2 large.

In addition, silicon nitride can be used as additional dielectrics, which have shown to have better tolerance against ionizing radiation (discussed later). On the backside an ohmic contact is made.

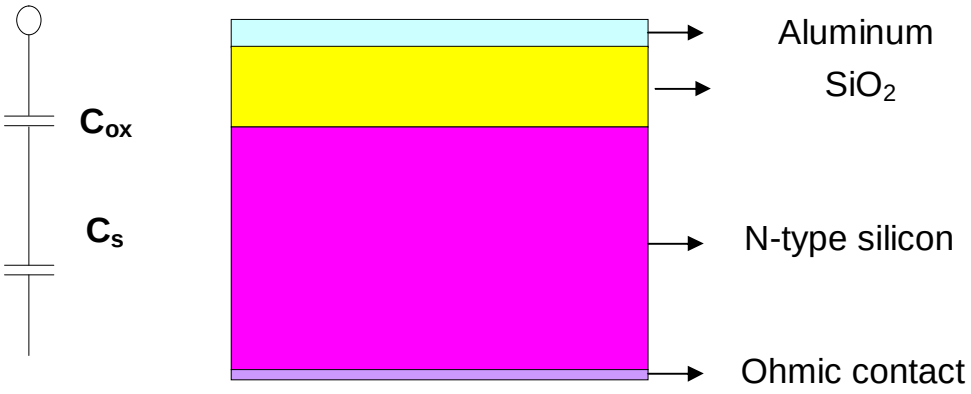


Figure 2.7 Schematic profile of a MOS capacitance (right), the equivalent circuit diagram consists of an oxide capacitance and a capacitance from the depleted layer (left).

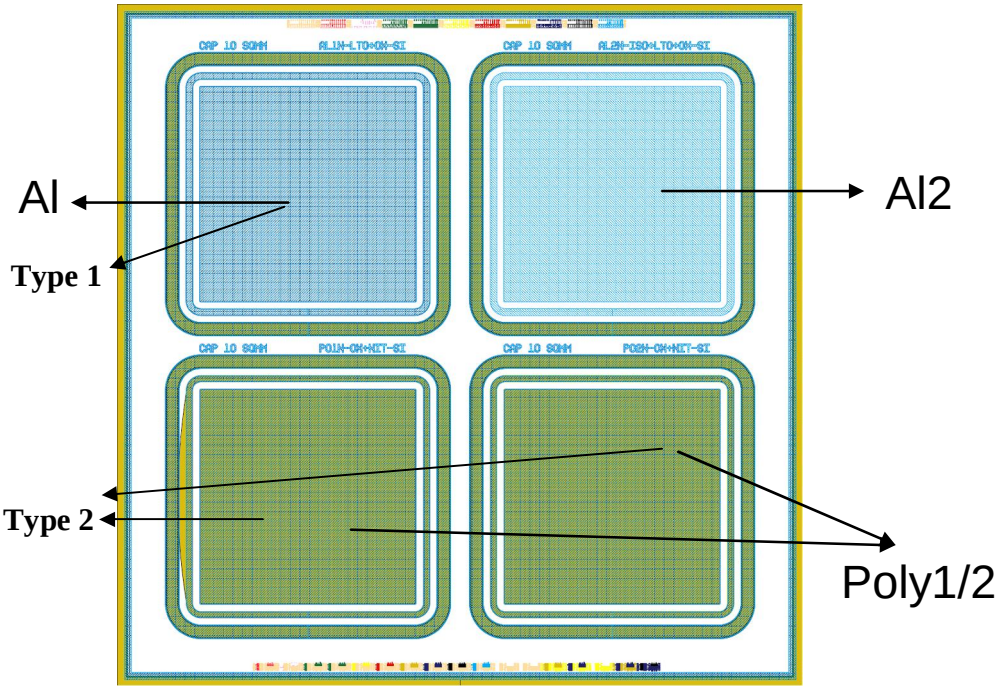
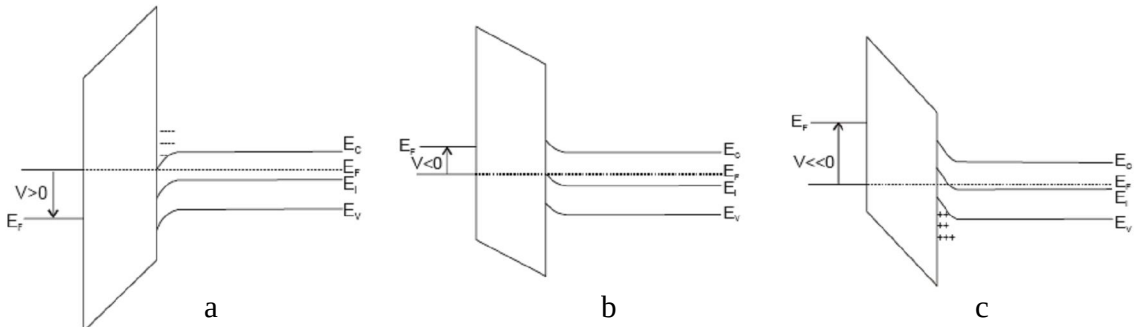


Figure 2.8 Layout of a standard MOS capacitance that consists of four different structures: Al-gate structure (top left); Al2-gate structure (top right); Poly1-gate structure (bottom left); Poly2-gate structure (bottom right).

By measurements of the MOS capacitances a lot of information about the oxide quality can be derived. A series of experimental methods are available to qualify the oxide. Here, the MOS capacitance is measured by applying a gate voltage. In the case a voltage is applied on the gate, there is a relative shift of the Fermi level between metal and semiconductor, and a space charge region will be formed. In order to understand the different bias modes of a MOS capacitor, three different bias voltages are applied: the

first one is above the flat band voltage - V_{FB}; the second one is between the flat band voltage and the threshold voltage - V_T and the last one is lower than the threshold voltage. The corresponding biasing regions are as shown in Figure 2.9: accumulation, depletion and inversion.



Accumulation	Depletion	Inversion
$\Psi_S \rangle 0$	$2\Psi_B \langle \Psi_S \langle 0$	$\Psi_S \langle 2\Psi_B$

Figure 2.9 Band diagram of a MOS capacitance, A. Accumulation, b. Depletion, c. Inversion. Ψ_B *is surface potential;* Ψ_S *is bulk potential [23].*

Accumulation

If the applied voltage on the gate is positive, the produced band deflection shows downward. The positive polarity can attract majority carriers (electrons) from the silicon substrate toward the gate. Since the oxide has a good quality and can be considered as a good insulator, electrons will move to the interface between silicon and SiO_2 and, furthermore, accumulate there. As a consequence, a negative charge Q_s is collected compared to the positive gate charge Q_G. An accumulation layer of electrons is created. It can be described by the following formula:

$$n_n = n_i e^{(Ei - E_F)/k_B T} \tag{2.9}$$

Where n_n is the concentration of charge carriers, n_i is the intrinsic concentration of charge carriers for silicon at room temperature. The concentration of electrons is exponentially proportional to the energy difference E_i-E_F. On the one hand, there are charges on the metal gate; on the other hand, the electrons are accumulated in the accumulation layer. Therefore, the MOS structure in accumulation state can be

considered as a plate capacitor. The total capacitance is equal to the oxide capacitance, and the surface potential is positive in this case as shown in Figure 2.9a.

$$\Psi_S \rangle 0$$

In general, the oxide thickness can be extracted from the oxide capacitance, which is measured by CV measurement on a MOS capacitance in accumulation. Accordingly, the oxide thickness may be calculated from C_{ox} using the following equation:

$$d_{ox} = \frac{\varepsilon_0 \varepsilon_{ox} A}{C_{ox}}$$

Compared with conventional ellipsometry [*], the oxide thickness calculation based on CV measurement is very precise, as long as the oxide capacitance is measured in accumulation, where the measured capacitance is essentially constant. In the case a high-resistance silicon substrate is used for MOS capacitance, oxide capacitance could be extracted only from low-frequency CV measurement in accumulation (discussed later).

Flat band

In this case flat band means that the energy band diagram of the silicon is flat, thus there is no bending of the band. Hence the charge carriers will not be forced to move in any direction. The surface potential is equal to zero. Ideally the flat band voltage is 0V; however, in real case it is approximately 0.5 ~ 2 V due to the difference of the work function from metal and semiconductor, and also the initial condition of the oxide charges cannot be neglected. Therefore, the flat band voltage for the real case can be calculated as follows:

$$V_{FB} = \frac{\phi_{ms}}{q} - \frac{N_{ox}}{C_{ox}} - \frac{N_{it}}{C_{ox}} \qquad (2.10)$$

Where V_{FB} is the flat band voltage that should be applied on a real MOS capacitor to achieve flat band condition, ϕ_{ms} is the work function difference between the metal (aluminum) gate and silicon, N_{ox} *and* N_{it} are the surface damages arising from oxide charges and interface traps. The surface potential is equal to zero: $\Psi_S = 0$

[*] *Ellipsometry: an optical method to measure the dielectric properties of thin films.*

Depletion

As the gate voltage changes towards negative values, which leads to an upward band bending, the majority carriers (electrons) are repelled from the Si/SiO_2 interface. Moreover, a depletion layer is developed underneath the oxide, where the majority of charge carriers become depleted. The depletion layer width increases with increasing gate voltage. The higher is the doping concentration N_D, the narrower is the space charge region. The capacitance in depletion does not remain constant and becomes sharply small. In this case, the surface potential is (shown in Figure 2.9b):

$$2\Psi_B \langle \Psi_S \langle 0 \qquad (2.11)$$

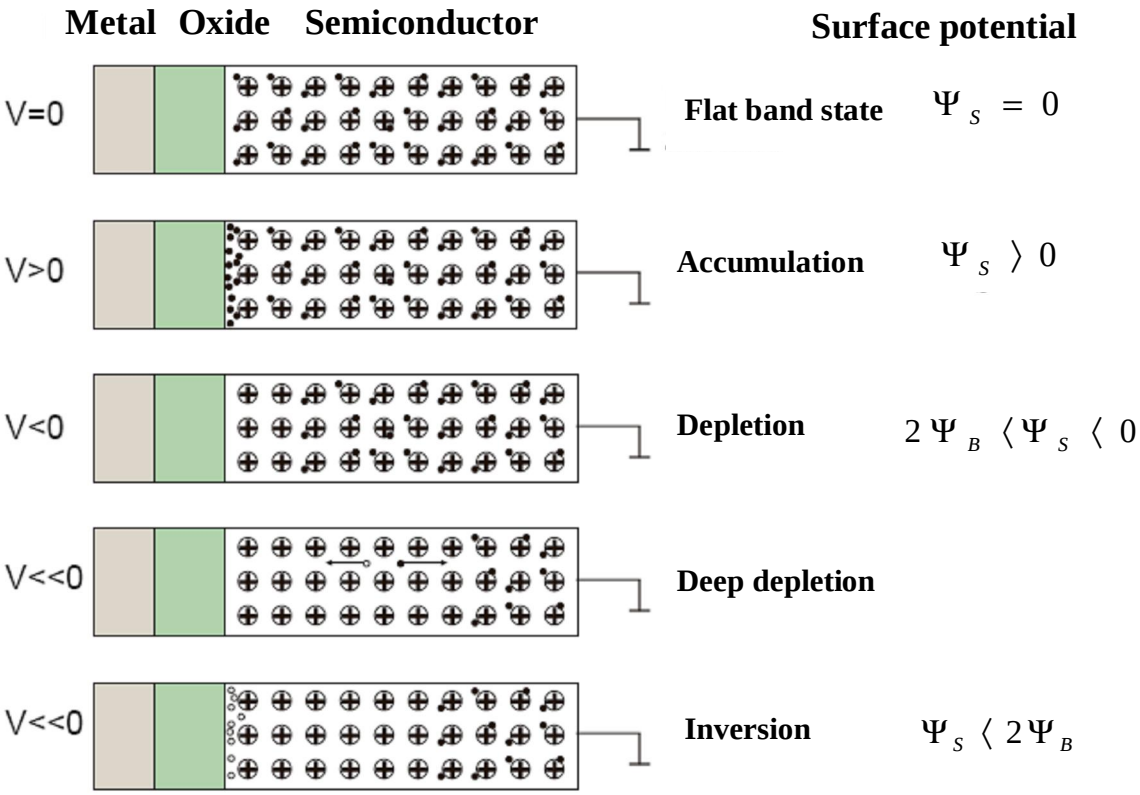


Figure 2.10 various states on the MOS Structure: flat band, Accumulation, depletion, deep depletion, Inversion [1].

Inversion

If the gate voltage changes much lower than the flat band voltage, the Fermi level crosses the intrinsic energy level E_i; this is called inversion, since the minority carriers (holes) are more than the majority carriers (electrons). This state is shown in Figure 2.10. In the case the gate voltage decreases further, the space charge region reaches its maximal value W_m. The capacitance in depletion remains constant. This is called strong inversion. In this case, the surface potential is (shown in Figure 2.9c) given as follows for n-doping material:

$$\Psi_S \langle 2\Psi_B \tag{2.12}$$

With respect to MOS capacitance, the flat band voltage V_{FB} is important (Figure 2.10), and the threshold voltage V_T for MOS-FETs in case of inversion as well, i.e. the MOS-FET remains conductive, if this voltage is applied on the gate [29].

$$V_T = -2\Psi_B - \frac{\sqrt{4qN_D\varepsilon_0\varepsilon_{Si}\Psi_B}}{C_{ox}} \tag{2.13}$$

2.2.2 Computation of a MOS capacitance

As mentioned above MOS capacitance consists of the oxide capacitance C_{ox} and the capacitance from space charge region C_s. Both are switched in series. Depending on the applied gate voltage, the total capacitance is given in equation 2.14:

$$C(V) = \frac{C_{ox}C_S(V)}{C_{ox} + C_S(V)} \tag{2.14}$$

The flat band voltage C_{FB} can be Figured out by means of Equation 2.15:

$$C_{FB} = \frac{C_{ox}C_F}{C_{ox} + C_F} \tag{2.15}$$

Where the total flat band capacity C_F is defined as [29]:

$$C_F = \frac{\varepsilon_0\varepsilon_{Si}}{L_D} \tag{2.16}$$

Where ε_0 and ε_{Si} are dielectrical constants, L_D is the Debye length and is defined by:

$$L_D = \sqrt{\frac{\varepsilon_0 \varepsilon_{Si} k_B T}{q^2 N_D}}$$

As mentioned above, for a positive gate voltage, MOS capacitance remains in accumulation. Therefore the MOS capacitance is represented by:

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{SiO2} A}{d_{ox}} \qquad (2.17)$$

The thicker the oxide, the smaller the gate surface area, and the lower the MOS capacitance. In the case where the gate voltage scans from positive to negative value, the state of a MOS capacitance will change from accumulation to depletion, and flat band is only a transition state. In depletion, electrons are pushed away from interface; as a consequence, a space charge region is produced, whose width will increase if the voltage becomes more negative. Because the capacitance of the space charge region is switched with the oxide capacitance in series, the total capacitance decreases rapidly. In inversion, an additional inversion layer is formed, which hinders a further extension of the space charge region. Accordingly, the capacitance remains constant.

2.3 Gated controlled diode

A gated controlled diode [30] is utilized to characterize the generation parameters of charge carriers in order to study the space charge region near the surface. A schematic cross section of such device is shown in Figure 2.11. It consists of an N substrate, a p+ implantation region, and rectangular gate surrounding the p+ region.

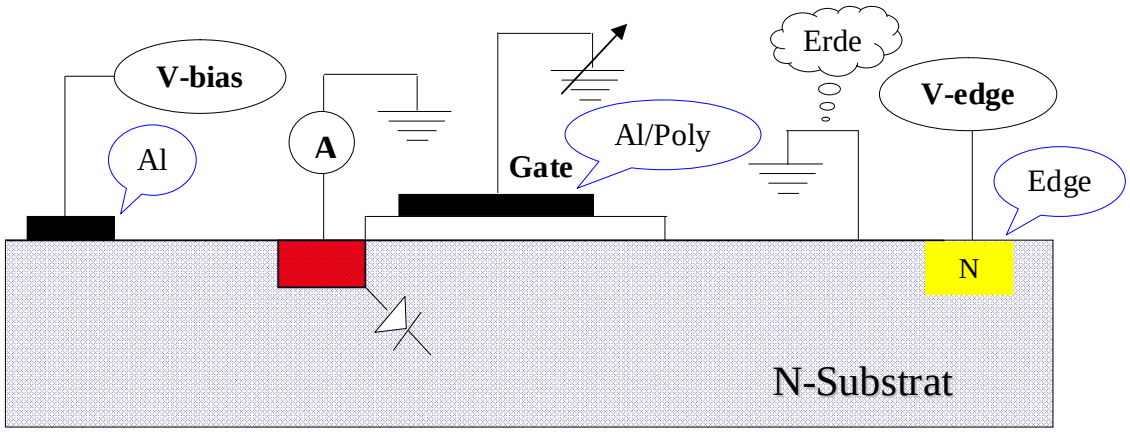


Figure 2.11 the gated controlled diode. Al /poly gate, p+ implantation region, Al contact and edge contact.

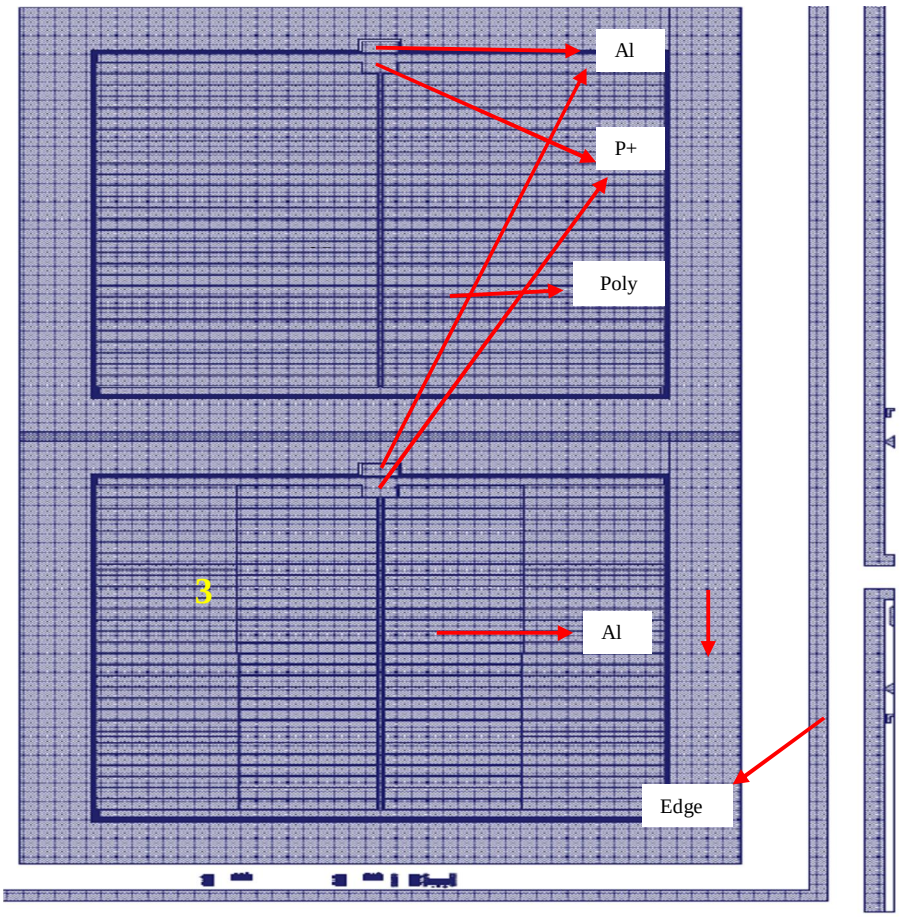


Figure 2.12 Layout design for gated controlled diode.

All terminals are shown in Figure 2.12 for biasing. In case of applying a voltage on the gated contact, the surface region under MOS contact will undergo a change from accumulation to inversion. By means of measuring the parameters, surface properties are characterized, like oxide charges and interface traps. In comparison with the results from MOS capacitance, the MOS gated controlled diode can be used not only as a reference device but also as a more precise monitor device, since many more parameters about surface properties can be controlled.

Chapter 3 Experimental methods and characteristic parameters

In this chapter, three different experimental methods corresponding to the three monitor devices mentioned above will be described in detail. Because these three monitor devices are produced on wafer by the same processing, there are no fundamental differences between the properties of these MOS devices, although various characteristic parameters are measured for each device. A List of parameters is shown below (Table 3.1), which affect the generation of surface damages in a certain way and will be discussed in the following section.

	MOS-C	**DEPFET**	**Gated diode**
N_{ox} (method)	ΔV_{FB} (CV-Measurement)	ΔV_t (IV-Measurement)	ΔV_{FB} & ΔV_g (CV-Measurement & gated diode technique)
N_{it} (method)	Stretch-out (High-low frequency based on the CV)	Subthreshold slope (Subthreshold technique)	Gated diode technique
Other parameters		Transconductance g_m (IV-Measurement)	Surface recombination velocity S_0 & Surface recombination lifetime (gated diode technique)

Table 3.1 lists of MOS devices used for characterization of radiation damage (surface damage); a couple of experiment methods and parameters with respect to each devices.

3.1 CV measurement using MOS capacitance

In the last chapter the theoretical principle of a MOS capacitance was introduced. In the following, the experimental technique will be presented to study the oxide properties on MOS structures. The whole experimental setup is shown schematically in Figure 3.1.

For the capacitance measurement, a Hewlett Packard 4284A LCR meter is used. This device allows a frequency-dependent capacitance voltage measurement in the range from 20Hz to 1MHz. Firstly an LCR meter is connected to the gate and edge of the MOS

device using bond wires. In order to extend the voltage range, an additional power supply Keithley 487 is utilized.

During CV measurement, two frequencies are used: low frequency (20 Hz) and high frequency (10 kHz). In the case of low frequency the AC voltage varies so slowly that holes collected at the interface are rapid enough to generate and recombine at the surface to recharge the inversion layer. It is also possible for charges to exchange with the inversion layer and, therefore, such a structure can still be considered as a plate capacitor.

With respect to high frequency (more than 1 kHz), the AC voltage signal varies quite rapidly, consequently holes of the inversion layer cannot be generated or recombined as fast as possible. For this reason the total capacitance is restored as a series connection of oxide capacitance and depletion capacitance under the gate.

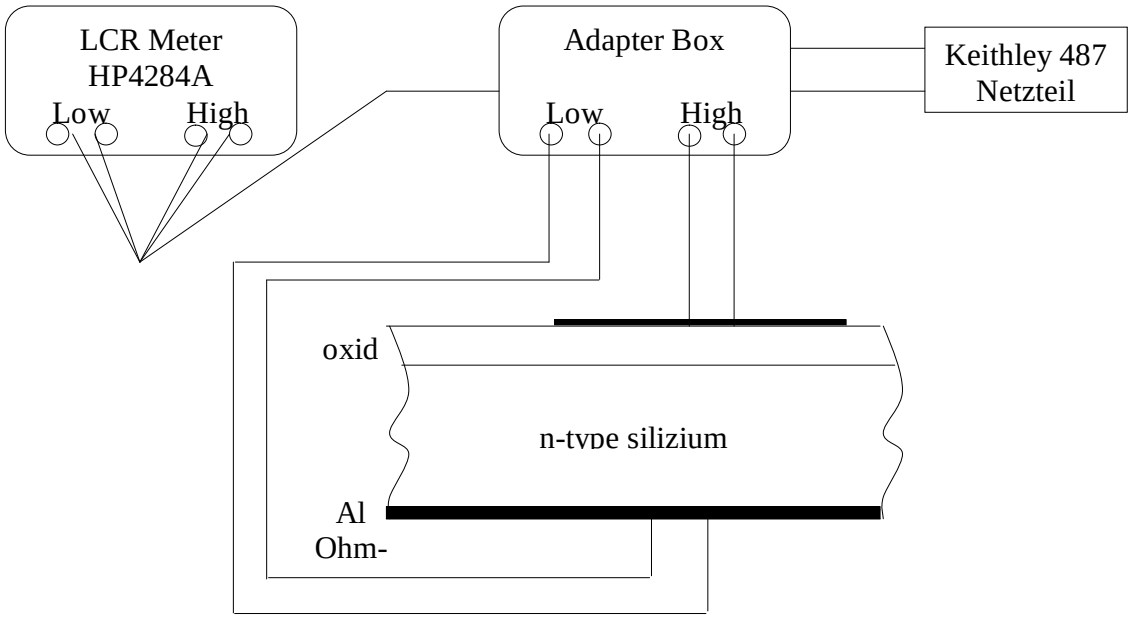


Figure 3.1 Experimental setup for capacitance voltage measurement

The MOS capacitance can be determined when a DC voltage is applied on the gate, which is superposed by a small AC voltage with amplitude of 50mV (Figure 3.2), changing from positive values to negative values under different frequencies, where the capacitance is measured. The measured CV curves depend on the frequency of the AC voltage, and these curves can distinguish themselves by the capacitance value in inversion.

The low-frequency CV measurement is performed such that the capacitance is measured by the ratio of the change in charge to the change in gate voltage. The high-frequency capacitance is obtained from a small-signal capacitance measurement at high frequency. The bias voltage on the gate is varied slowly to obtain the capacitance versus voltage.

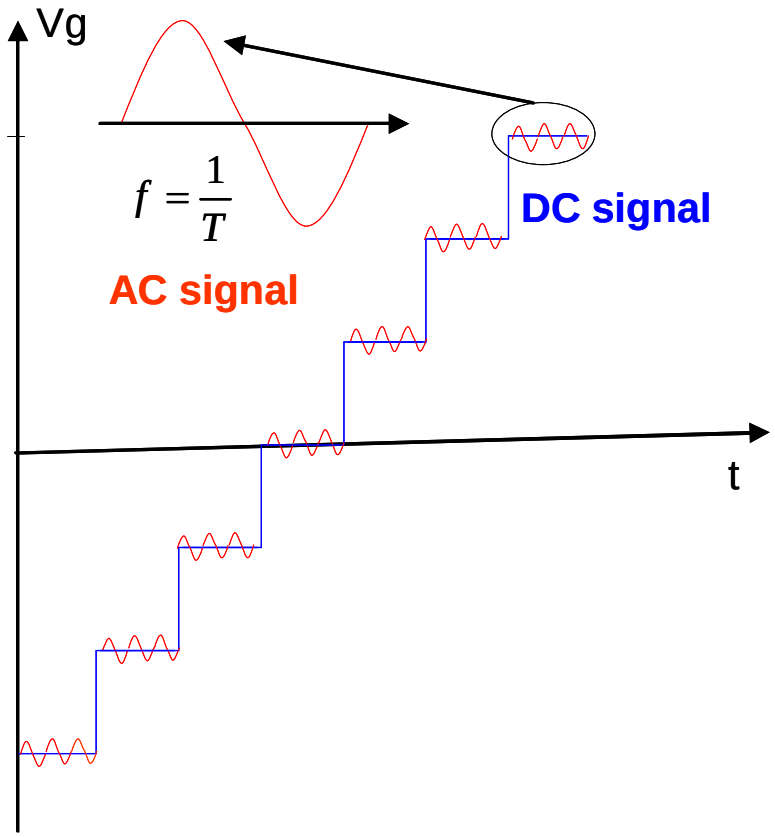


Figure 3.2 Capacitance measurement.

In this chapter the introduced silicon chip is produced on high-ohmic material ($N_D \approx 10^{12} cm^{-3}$). The capacitance voltage curves using high-/low-frequency CV measurement are shown in Figure 3.3 for a MOS capacitance. As mentioned above, the measured capacitance almost equals the oxide capacitance, since the MOS structure can be considered as a plate capacitor within the accumulation region where there is a small difference of capacitance for high-/low-frequency CV due to a relatively high resistance at the backside. With respect to inversion region, the capacitance is small because a broader intrinsic space charge region is developed for high-ohmic silicon substrate. It is also experimentally found that there is a small increase for low-frequency CV compared with HF CV due to the influence of interface traps. In the case of a silicon substrate with low resistance, the measured capacitance will significantly increase in inversion state depending on the doping concentration of the substrate.

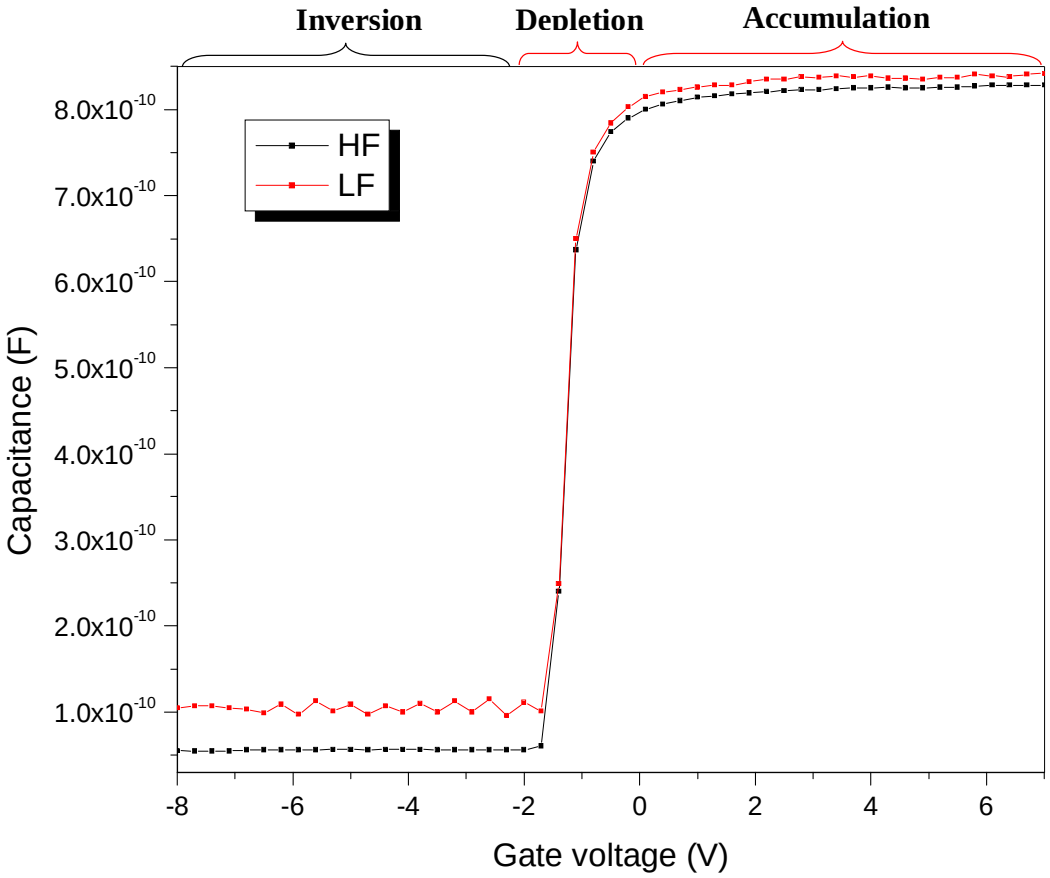


Figure 3.3 Frequency-dependent CV measurement: the capacitance does not increase in version as oxide capacitance, because a broader intrinsic space charge region is developed for high ohmic silicon. (Oxide thickness: 480nm, before irradiation).

After CV curves by high- and low frequency are measured, it is possible to read flat band voltage out from the high-frequency CV curve by means of calculated flat band capacitance C_{FB} (Figure 3.4). In this case it is possible to calculate the corresponding oxide charges N_{ox} from the difference of flat band voltage before and after irradiation. The shift of flat band voltage ΔV_{FB} due to the positive oxide charges is given by

$$\Delta V_{FB} = -\frac{q}{\varepsilon_0 \varepsilon_{SiO_2}} d_{ox} \Delta N_{ox} \qquad (3.1)$$

Where the positive oxide charges ΔN_{ox} are evaluated by integration with respect to the interface

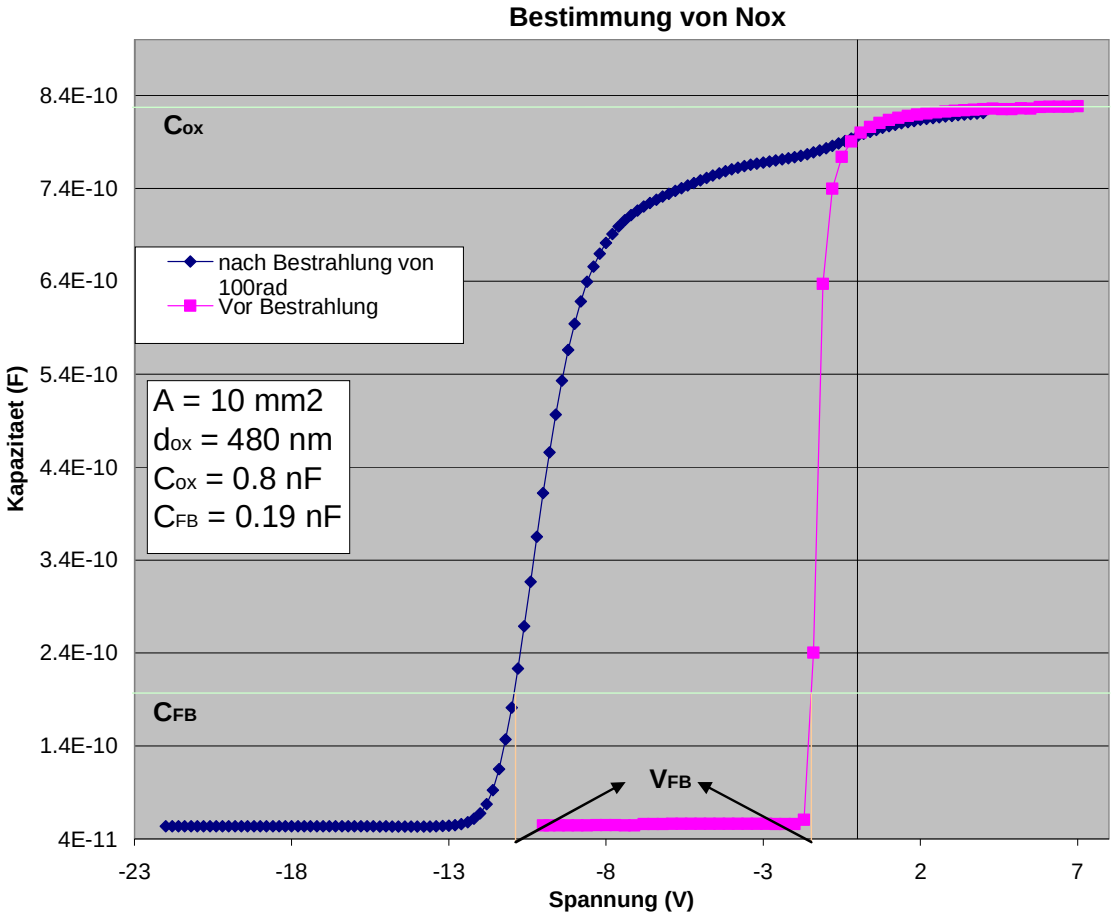


Figure 3.4 Calculation of N_{ox} by flat band voltage shift: (CV-HF-measurement).

$$\Delta N_{ox} = \frac{1}{d_{ox}} \int_0^{d_{ox}} n_{ht}(x) x dx \tag{3.2}$$

Taking into account the shift of flat band voltage of a MOS structure, it can be defined as the following expression:

$$V_{FB} = \phi_{ms} - \frac{N_{ox}}{C_{ox}} - \frac{N_{it}}{C_{ox}} \tag{3.3}$$

The first contribution arises from the work function difference between silicon and metal, while the second term is the positive oxide charges. The last one is due to the generated interface traps.

In addition, it is also possible to evaluate the interface traps by comparing these two curves at high and low frequency (Figure 3.5 & Equation 3.4) (high-/low-frequency method)

$$N_{it}(V) = \frac{1}{qA}\left(\frac{C_{LF} * C_{OX}}{C_{OX} - C_{LF}} - \frac{C_{HF} * C_{OX}}{C_{OX} - C_{HF}}\right) \tag{3.4}$$

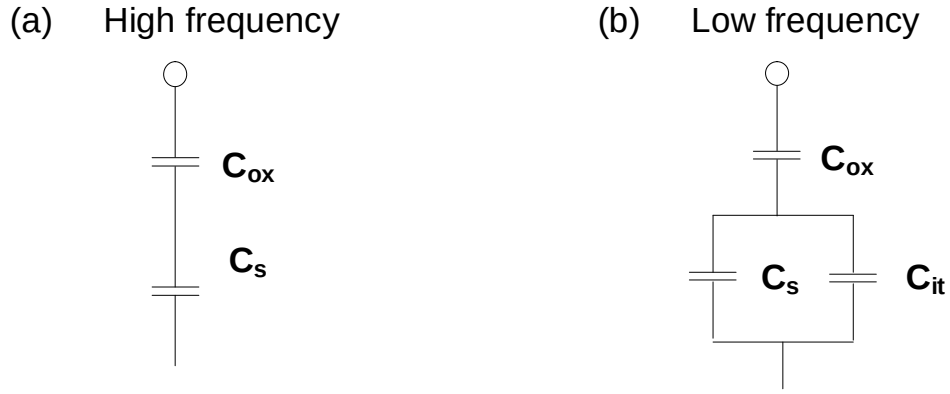


Figure 3.5 CV-measurement for evaluation of interface traps. Equivalent circuit diagram for high frequency (a) and low frequency (b)

3.2 Subthreshold technique concerning MOSDEPFET

Before discussing subthreshold technique, the concept of threshold voltage will be briefly discussed since it is an important MOSFET parameter required for the analysis of oxide properties. For a p-channel MOSDEPFET, when the gate is biased with $V_G > V_T$, the silicon surface under the gate is in accumulation or depletion – this means that the channel region is not conductive; almost no current flow between source and drain. In the case of $V_G < V_T$, a large number of holes appear near the silicon surface under the gate in the channel; therefore a conductive channel connecting source and drain is formed. However, currently there is not a unique definition for threshold voltage V_T, since there is no such unique gate voltage, at which drain current begins to flow. In general, according to the most common used definition, threshold voltage is the gate voltage when $\phi_s = 2\phi_B$, or when strong inversion starts. The threshold voltage of a p-channel MOSDEPFET is given using the following equation [29]:

$$V_T = -2\phi_B - \frac{2\sqrt{\varepsilon_0 \varepsilon_{si} q N_D \phi_B}}{C_{ox}} \tag{3.5}$$

This equation implies that V_T depends not only on the oxide thickness but also on the channel doping concentration. V_T for an ideal p-channel transistor is negative as expected. However, for the real transistor the effects of work function difference, oxide charges and interface traps must be included. For this reason, the above equation should be reformulated by:

$$V_T = V_{FB} - 2\phi_B - \frac{2\sqrt{\varepsilon_0 \varepsilon_{si} q N_D \phi_B}}{C_{ox}} \tag{3.6}$$

Where V_{FB} includes the real MOS properties:

$$V_{FB} = \phi_{ms} - \frac{N_{ox}}{C_{ox}} - \frac{N_{it}}{C_{ox}} \tag{3.7}$$

The terms ϕ_{ms} and $-N_{ht}/C_{ox} - N_{it}/C_{ox}$ are typically negative, hence, the threshold voltage for a real p-channel transistor is still negative, this means, the transistor remains 'off' even at zero gate voltage. In addition to drain current versus gate voltage, drain current as a function of drain voltage can also be measured. It is assumed that the gate voltage is above the threshold voltage, as long as the drain voltage is much smaller than the gate voltage, the inversion layer (channel) thickness remains constant under the gate, an ohmic conduction of the channel will be achieved and drain current is linearly proportional to drain voltage. With increasing drain voltage, the potential difference between the gate and surface near gate decreases until strong inversion is destroyed. This is called 'Pinch Off' from the drain. The drain current will not increase anymore and remain almost constant with further increasing drain voltage.

From the theoretical point of view, there is no current flowing from source to drain. However, there is a small current flowing through the drain, in the case the gate voltage is smaller than the threshold voltage observed experimentally. This is the subthreshold current which comes from the minority charge carriers in the channel, when the silicon surface is in weak inversion. The subthreshold current depends on the minority carrier density. The subthreshold characteristics of the MOSDEPFET can offer a possibility to evaluate interface traps. A useful parameter is the subthreshold swing S [23], delivered by the reduction of the current by one decade.

$$S = \ln(10)\left[\frac{dV_G}{d(\ln I_D)}\right] \approx \frac{kT}{q}\ln(10)\left(1 + \frac{C_{sc}}{C_{ox}}\right) \tag{3.8}$$

As mentioned above, one of the most important effects due to ionizing radiation is the shift of threshold voltage to more negative values, since radiation-induced oxide charges and interface traps are formed.

As a consequence, by measuring drain current versus gate voltage before and after irradiation, information on surface properties about oxide charges and interface traps will be provided. As depicted in Figure 3.6 below, surface damages (work function difference, oxide charges and interface traps) result in a shift of the drain current versus gate voltage along the gate voltage axis. On the other hand, the interface traps lead to a change in the slope of drain current versus gate voltage curve, and thus the subthreshold swing. It can be calculated as follows:

$$S_{post} = S_{before}\left[1 + \frac{C_{it}}{C_{ox} + C_{sc}}\right] \tag{3.9}$$

Where S_{after} and S_{before} mean the value achieved after irradiation and before irradiation, respectively, and $C_{it} = qD_{it}$ is the capacitance with respect to the interface traps. From the combination of the above equations, the interface traps can be represented as follows:

$$N_{it} = \frac{C_{ox}}{kT\ln(10)}\left(S_{post} - S_{before}\right) \tag{3.10}$$

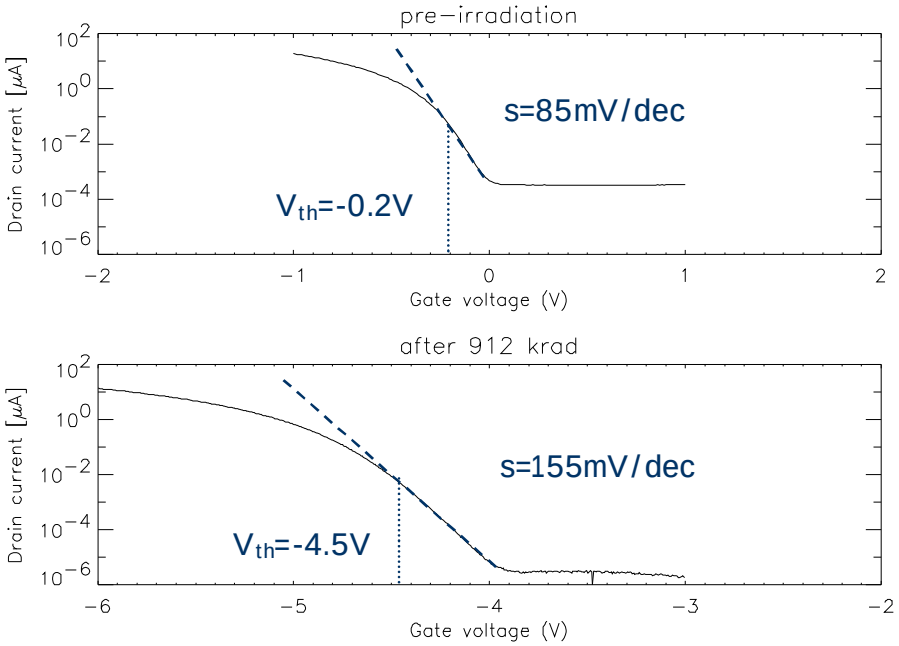


Figure 3.6 Subthreshold slopes before and after irradiation.

In addition, another important parameter is transconductance, g_m, which also characterizes the MOSDEPFET. Transconductance is controlled by the mobility of charge carriers in the channel and is influenced by carrier scattering due to surface damages after ionizing radiation.

3.3 Gated diode technique

Based on the gated controlled diode introduced above, calculation of the gate to substrate current-voltage characteristic is presented in this paragraph. Firstly, an equivalent circuit diagram of a gated controlled diode is shown in Figure 2.11. A voltage is applied on the gate contact together with picoampermeter, which is connected to the p+ contact to

measure the reverse current as a function of the gate potential at a fixed bias voltage of (10V) on the aluminum contact. Various voltages are applied on the edge contact in order to steer the generation current stage.

Generally at room temperature the reverse current of a PN junction arises from electron-hole pairs generated in the depletion region, which takes place normally at generation/recombination centers. As shown in Figure 3.7, the silicon surface under the gate is in accumulation at positive gate voltage. As a consequence, a small generation current I_{pn} is measured, which comes from those centers within the depletion region of the PN junction directly underneath the p+ implanted region. With decreasing gate voltage the surface under the gate goes into depletion, hence, another contribution to the generation current comes from the centers within the surface depletion region, which is built up by the field-induced junction under the surface. This contribution I_{FIJ} increases with growing width of surface depletion region as indicated by the red dashed line in Figure 3.7. Moreover, generation/recombination centers from interface traps I_{it} provide a much larger contribution to the total generation current, which leads to step in the reverse current versus gate voltage. At the onset of the strong inversion, the generation/recombination centers are occupied by holes; therefore, the reverse current decrease significantly, although not to its original value, i.e., higher than in case of accumulation. The point of onset of depletion is shifted with various edge voltages. The reverse current during depletion and weak inversion increases slightly with increasing edge voltage, since the width of the PN junction under the p+ implant region increases with growing edge voltage, and the contribution arising from the PN junction in accumulation is increasing.

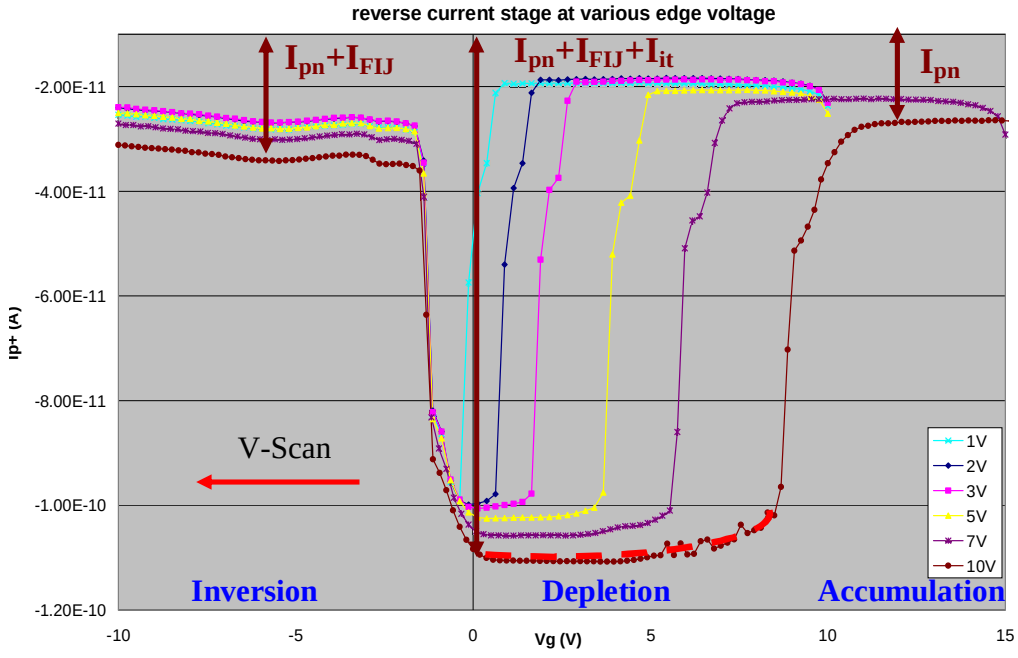


Figure 3.7 Generation current stage depending on different voltage applied on the edge.

From the interface generation current measured on the gated controlled diode it is convenient to calculate the surface recombination velocity s_0.

$$s_0 = \frac{I_{it}}{qn_i A} \tag{3.11}$$

Where q the elementary charge, n_i is the intrinsic charge carrier concentration, A is the gate area. Furthermore, interface traps density is determined by following equation [43]:

$$D_{it} = \frac{s_0}{\sigma_{n/p} v_{th} \pi kT} \tag{3.12}$$

Where $\sigma_{n/p}$ is the capture cross section of electrons or holes in the interface, v_{th} is the thermal velocity, k is the Boltzmann constant, and T is the temperature.

In case of ionizing radiation, the oxide charges can be determined by the shift of the reverse current step, almost the same as in the case of MOS capacitors (Equation 3.1).

Chapter 4 Damage mechanism

As mentioned above, all MOS structures are inherently susceptible to ionizing radiation. The main total ionizing dose effects are the change of electrical parameters, e.g. flat band voltage (threshold voltage), leakage current, transconductance, etc. The primary reason to study MOS structures is to understand their principle of operation and evaluate the MOS processing, since the MOS structures are simple to produce and widely used in various detector devices, like MOSCCD, MOSDEPFET, CMOS, etc. A lot about the ideal MOS structure of a capacitance has already been discussed in the previous chapter. In the case of non-ideal conditions in MOS capacitances (real capacitors), a lot of attention should be focused on the MOS structures. This means that the characteristics of the MOS devices should depend on the properties of oxide and its interface between silicon and SiO_2. In addition, nitride can also be used as dielectrics for an additional insulator layer between oxide and gate material; this is the MNOS (metal nitride oxide silicon) structure. At first, the production of such dielectrics – oxide and nitride — will be briefly described, and then the defects in the dielectrics will be described in detail also including the physical models, by which the damage mechanism will be comprehensively explained with respect to ionizing radiation.

4.1 Oxide

In the following, the oxide properties and the production of thermal oxide will be described [24]. One of the important advantages of silicon are the properties of oxide. In general, SiO_2 is used as dielectrics, insulator, and passivation layer on the silicon surface and especially to control the implantation process. The reason for the utilization of SiO_2 is as follows:

- Simple to produce in the application (fabrication)
- Good knowledge on the physical and chemical properties
- High voltage stability
- High quality at the interface with silicon (low concentration of defects)

4.1.1 Properties of thermal oxide

With the help of oxidation, one can produce a layer of SiO_2 on silicon. With respect to MOS technology there are a series of requirements on the oxide:

- Interface with low surface states*
- High breakdown voltage
- Stability under influence of electrical field and elevated temperatures

A list of electrical and physical properties for SiO_2 and silicon are presented in Table 4.1 [31].

	SiO_2	Silicon
Crystal structure	Amorphous	Diamond
Atom/molecule (cm^{-3})	$2.3*10^{22}$	$5*10^{22}$
Density (g/cm^3)	2.27	2.33
Dielectric constant	3.9	11.7
Resistivity (ohm cm)	10^{14} to 10^{16}	10^{-2} to 10^{5} (depending on doping)
Band gap (eV)	8	1.1
Breakdown field (MV/cm)	10	
Energy for pair production (eV)	18	3.7
Melting point (Celsius)	1700	1415

Table 4.1 Electrical and physical properties of SiO_2 and silicon.

From the point of view of the periodic lattice structure, each silicon atom has in principle four neighbor silicon atoms surrounding it. However, there is a significant number of silicon atoms near the surface Si/O, which are not regularly arranged like the periodic lattice structure due to oxide processing on the silicon substrate. This means that silicon atoms are only partially bonded by atoms nearby, so that there are free valences remaining that are called dangling bonds. They can react with other impurities (like H or O). It will also contribute to interface traps (discussed later). Oxide produced by high-quality processing can serve not only as a barrier against diffusion of charge carriers but also as a mask preventing lateral doping implantations.

MOS devices are produced by thermal oxidation — SiO_2 is usually produced in oxygen or water-vapor atmosphere using one of the most common techniques, which can be classified as dry oxidation and wet oxidation. In general, freshly cleaned silicon wafer can form a very thin oxide layer in oxygen or water vapor atmosphere at room temperature, the native oxide. With increasing temperature the growth will be accelerated to produce a thick oxide layer.

* *Here surface states mean interface traps which are located at the interface Si/O.*

In the oxygen atmosphere (dry oxidation): oxygen diffuses through the existing oxide further to the interface Si/O, and reacts with silicon atom to create SiO_2 [32]:

$$Si + O_2 \Leftrightarrow SiO_2 \tag{4.1}$$

In a water-vapor atmosphere (wet oxidation):

$$Si + H_2O \Leftrightarrow SiO_2 + H_2 \tag{4.2}$$

A typical oxidation process takes place between 900 and 1200 Celsius at atmospheric pressure. With respect to both reactions above, the growth always happens at the interface between silicon and the already existing oxide layer. Since a relatively small silicon atom connects with two oxygen atoms, the SiO_2 molecule is about two times thicker than the silicon. As a consequence, about 43% of silicon is consumed for this procedure [29]. For example, an oxide layer with 100 nm thickness is produced by a silicon layer of about 43 nm.

Oxide, produced by dry oxidation process, exhibits better electrical properties concerning the breakdown voltage and interface traps than in case of wet oxidation. However, the growth velocity is much faster in water-vapor atmosphere than in oxygen atmosphere. A large number of factors can influence the growth velocity of SiO_2 on the silicon, such as temperature, substrate orientation and doping, etc. [31]. Nitrogen is often required for the temper process which takes place directly after oxidation. It is done typically at the same temperature in the nitrogen atmosphere in order to reduce the density of defects in the oxide.

4.1.2 Defects in the oxide

During oxidation there are a series of defects, which are located spatially in the oxide bulk and interface. An overview of defects is given in Figure 4.1 below, their concentration depends on the different parameters, such as oxidation process, silicon material and so on.

MOS structures are highly sensitive to a variety of impurities, e.g. by wafer processing or oxidation. In the SiO_2 region (bulk oxide), there are mobile ion charges like alkali-contaminations, especially sodium ions (Na^+) can be identified as positively charged ions and always exist in the environment. In addition, there are negative ions and heavy metal impurities. They are all electrically active and mobile at high temperature. By performing thermal stress measurements mobile charges are determined by a shift of repeatedly measured CV curves, since the positive ion charges drift towards the gate contact at increased temperature (up to 200 Celsius) by the applied negative gate voltage, while a positive voltage attracts the negative ion charges towards the gate. However, with the present oxidation process these impurities do not play an important role.

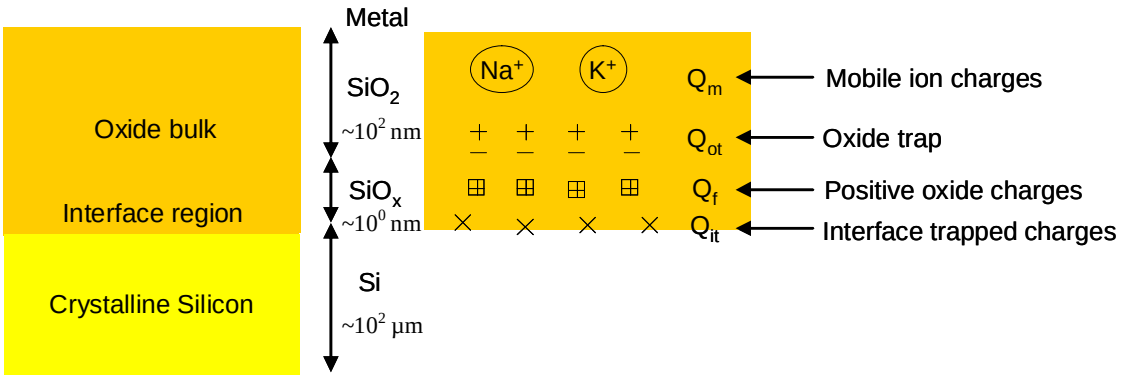


Figure 4.1 Layer profile of a MOS structure: bulk oxide (SiO_2), interface region (SiO_x) and mono-crystal silicon (left). List of defects in the oxide and interface (right).

Other defects are fixed oxide traps, which are located within the whole bulk oxide. They arise either from the defects of thermal oxidation: residual moisture – water vapor, which results in hydroxyl groups by reaction with bridging oxygen atoms:

$$H_2O + Si - O - Si \rightarrow Si - OH + OH - Si \tag{4.3}$$

or from chemical contaminations (sodium atom) and probably silicon atoms (incomplete oxidized Si). These fixed oxide traps can capture electrons or holes that come from ionizing radiation, it can be determined by CV measurements. A positive fixed charge at the Si/O interface shifts the flat band voltage to more negative values, and is equal to the charge divided by the oxide capacitance C_{ox}. Therefore it is possible to determine their density using shift of CV curves on MOS structures, as long as no other charge is present.

The interface region is located between mono-crystal silicon and bulk oxide, and extends only up to a few nanometers, where positive oxide charges and interface traps are mainly formed. Due to imperfect lattice structure at the crystal interface trivalent silicon ($\equiv Si \cdot$) builds up electric active defects, which become inactive by hydrogen annealing, since the silicon bond is saturated by a reaction with hydrogen:

$$\equiv Si \cdot + H \leftrightarrow \equiv Si - H \tag{4.4}$$

At high temperatures (about 400 Celsius) hydrogen dissociates from silicon hydrogen bond again [33]. Due to interface traps energy levels are created in the silicon band gap, they may be charged positively, negatively or neutral – amphoteric. The interface traps depend on the applied gate voltage. Hence interface traps could be evaluated from the stretch-out form of the measured CV curve using combined high- and low-frequency methods (shown in Figure 4.2 left). Usually the distribution of interface traps density as a function of the energy band gap looks like a U form (Figure 4.2 right) [34] that monotonically increases with energy towards the band edges from a minimum near mid gap. Similar as positive oxide charges, interface traps are generated during ionizing radiation in the oxide. Increasing interface traps may cause a higher leakage current [35],

which makes low-frequency CV measurement not work properly and accordingly degrades the detector properties. More about the generation process will be discussed in the next paragraph.

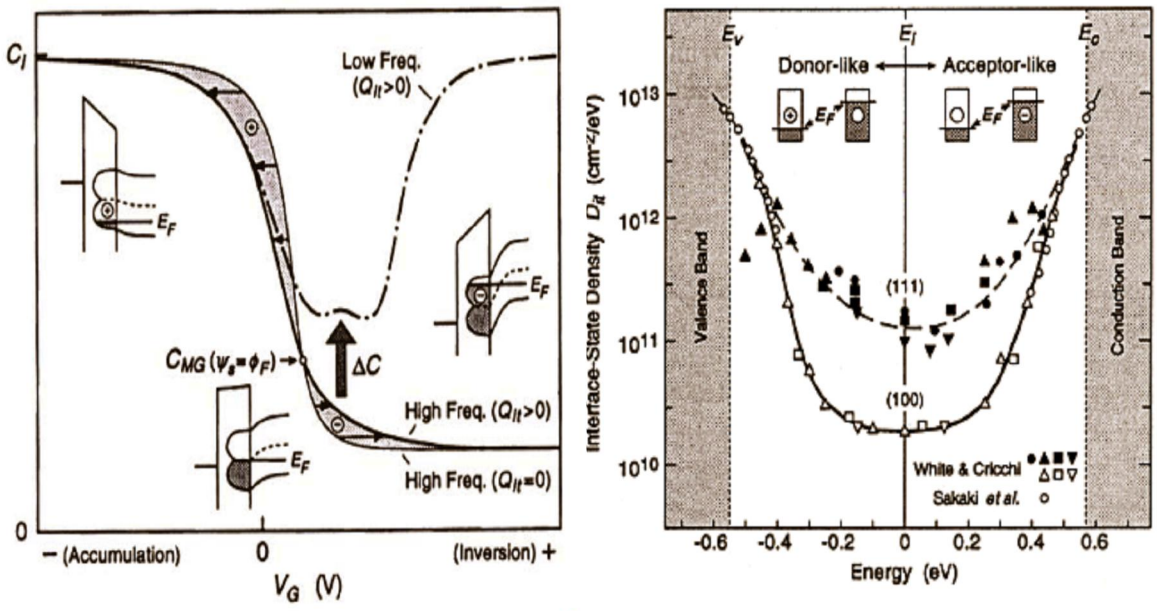


Figure 4.2 Determination of interface traps by stretch-out form from combined high/low-frequency CV measurement (left), U shaped distribution of interface traps in the energy band gap (right) with strong increase at both band edges, and substrate orientation-dependent interface traps density [34].*

In summary, all defects in the oxide influence the electrical properties of MOS structures in different ways. Among them all defects associated with hydrogen are most important, since they can participate in the reaction of generation of interface traps, which degrade the electrical performance of detector devices. The defect density in the oxide depends on various parameters, mainly on the processing of the devices, and also on the starting substrate, oxidation processing and so on. In the Chapter 6, a comprehensive overview will be given about the radiation hardness.

* *Usually the slope of the measured CV lines look like more flat due to interface traps than in case of without interface traps.*

4.2 Nitride

In general, nitride is a chemical compound of nitrogen. A large number of applications of nitride can be found, e.g., silicon nitride. In the following section, the properties of silicon nitride and its corresponding production technology will be briefly introduced. It can be used either as an insulator layer or as an oxidation mask. As a passivation layer in the silicon technology, it is much better than SiO_2 since it is a significantly better diffusion barrier against hydrogen atoms and sodium ions. It can also be used as an additional dielectrics between metal and SiO_2 in a capacitor to create an MNOS (metal nitride oxide semiconductor) structure, which is investigated in this thesis.

4.2.1 Nitride properties

Silicon nitride is a hard solid material, and has a low thermal expansion coefficient. It has high mechanical strength and is resistant to deformation at room temperature as well as at elevated temperatures. It is difficult to produce a silicon nitride since this material is made up of covalent bond atoms; for this reason it does not readily melt and can hardly be heated but between 1750 and 1900 Celsius, while it dissociates into silicon and nitrogen over 1900 Celsius [65].

Key properties of silicon nitride are summarized:

- High mechanical strength over a wide temperature range
- Good fracture toughness
- Good resistance against oxidation

Compared to SiO_2 a series of electrical and physical properties can be found in Table 4.2:

	Silicon nitride	SiO_2
Crystal structure	Amorphous	Amorphous
Density (g/cm^3)	3.1	2.27
Dielectrica constant	~7.4	3.9
Resistivity (ohm cm)	10^{14}	10^{14} to 10^{16}
Band gap (eV)	5	8
Breakdown field (MV/cm)	<10	10
Energy for pair production (eV)	15	18
Melting point (Celsius)	1900	1700

Table 4.2 Electrical and physical properties of silicon nitride and SiO_2 [66].

Normally silicon nitride can be produced by direct reaction between silicon and nitrogen at high temperatures. In microelectronics silicon nitride is usually produced using CVD (Chemical Vapor Deposition). The two most commonly used variants are LPCVD (Low Pressure Chemical Vapor Deposition) and PECVD (Plasma enhanced Chemical Vapor Deposition). LPCVD nitride produced at 700–800 Celsius has been most commonly used in crystalline silicon technology. In case the devices (with aluminum) can not be produced at such high temperature, PECVD is used to produce nitride that takes place at temperatures in the range of 350–400 Celsius.

The major importance of MNOS devices is charge storage properties for the memory application. The MNOS structure is made by firstly growing a thermal oxide layer and subsequently depositing a silicon nitride layer on (100) orientation N-type silicon with doping concentration of about 10^{12} cm^{-3} as shown in Figure 4.3.

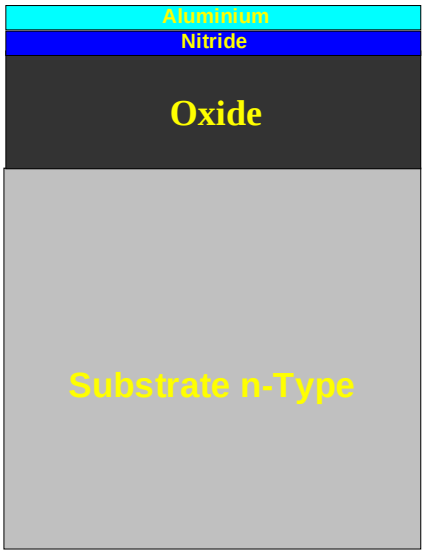


Figure 4.3 Layer profile of an Al-gate structure MOS capacitance: it consists of aluminum gate contact, thin nitride and oxide layer and n-type silicon substrate.

4.2.2 Defects in the nitride

From the microscopic point of view, there are various defects in the silicon nitride bulk as well as in the interface region between silicon nitride and SiO_2 of an MNOS structure. Several previous studies on the properties of nitrogen dangling bonds in amorphous silicon nitride films have suggested that hydrogen can passivate largely the nitride dangling bonds and traps (precursors) in the films [54]. The NH bonds can then dissociate by a high-temperature deposition or after deposition annealing (T > 500°C),

leaving behind charged nitride (bond). It is same as interface traps between silicon and SiO_2. The nitride dangling bond is found to be an electrically active point defect. Its electrical properties can be explained by assuming that the nitride defect can be cycled between its charge states: positive, negative, and neutral.

Defects in silicon nitride can be identified as charge trapping centers, the nitride layer exhibits charge storage characteristics for both electrons and holes, accordingly it is necessary to investigate the charge trapping mechanism in such an dielectric layer of an MNOS structure.

The standard methods for studying trapping properties of dielectrics have been avalanche injection, i.e., carriers are accelerated into the dielectric layer and are then trapped. The trap density and capture cross section can be determined by charging kinetics [58]. Depending on defect concentration of the dielectrics, different experimental methods can be assigned. A combination of the avalanche injection with the photo current voltage method is the most effective way to determine the trap distribution for relative low defect dielectric layer, while the centroid measurement technique combined with the photo IV method is chosen for highly defective dielectrics. According to previous assumptions, a uniform trap density in the nitride should be found. However, measurements from Y.C. Park, et. al. have demonstrated that bulk densities of traps are quite identical of about 10^{18} cm^{-3}, independent of the deposition method. A significant contribution of the traps arises from the silicon dangling bonds. Concerning different nitrides, both LPCVD and PECVD nitrides have relative large interface traps density of about 10^{19} cm^{-3} (equivalent to an area density of about 10^{13} cm^{-2}), which is distributed at the interface and extending about 10nm into silicon nitride bulk. PECVD nitride has a relative lower interface trap density than LPCVD nitride deposited at high temperatures.

4.3 Physical model

Before introducing an appropriate physical model for the damage mechanism [23], it is necessary to take a look at the generation and transport process of radiation-induced charges. When ionizing radiation goes through the oxide, it will lose its energy by the photo effect. The deposed energy in the oxide may generate electron-hole pairs. On average, about 18eV of energy deposed in the oxide is needed to create an electron-hole pair [42]. Therefore it is not difficult to determine the amount of charges produced by ionizing radiation. Electrons due to ionizing radiation have a faster mobility (temperature and field dependence) in the oxide than holes. The mobility of electrons in SiO_2 is about 20 $cm^2V^{-1}s^{-1}$ at room temperature [23]. At high fields the velocity will saturate at around 10^7cm/s. In comparison, the mobility of holes is strongly temperature and field dependent but is much less than that of electrons. Normally it is about 10^{-4}-10^{-11} $cm^2V^{-1}s^{-1}$ depending on the temperature and field [23]. For this reason, the induced electrons can be swept out of the oxide bulk within the first picoseconds [23]. At the same time, a part of

the almost unmovable holes recombines with electrons depending strongly on the applied electric field and the energy and kind of incident particles. Electron-hole pairs are separated under the influence of electric fields, the separated charges migrate towards the reverse directions depending on the corresponding field. Without any electric field the recombination process of electron-hole pairs becomes significantly enhanced. Holes that escape the initial recombination have a relatively small mobility, and just stay there where they are generated. As a result, they cause a negative voltage shift on the MOS devices (short-term effect). In a time period of order of seconds these remaining holes can migrate through the oxide by the stochastic hopping process. In the case these holes move to the interface (at a positive gate voltage), some of them will be trapped in the hole trap sites, which result in a negative voltage shift that remain a long time (on the order of hours to years) and can be determined by previous explained CV measurement (long-term effect).

As discussed previously, the study on the MOS structure exposed to ionizing radiation shows a significant increase of positive oxide charges as well as interface traps. Positive oxide charges on the MOS structures cause a flat band voltage shift to negative value. To date some of the surface damage mechanisms are known. Here in this section it is still necessary to understand the basic mechanism of ionizing radiation-induced damage before one starts to evaluate the MOS structure. Moreover, several corresponding models will also be discussed, e.g. the Dimaria model, Hydrogen model, Injection model and Stress model [23], which attempt to explain the whole generation process for radiation damage in the oxide comprehensively.

Positive oxide charges

From the point of view of a physical nature, according to present evidences these hole traps arise from intrinsic defects, e.g. an oxygen vacancy defect – strained Si-Si bond. Due to incomplete growth, the Si/O interface is extremely sharp, strained Si-Si bonds are located within the transition region extending to a few nanometers from the interface. In other words, there are much less strained bonds in radiation hard oxide than in the case of radiation soft oxide. The strained Si-Si bond in the transition region can be easily broken up by ionizing radiation, and then the induced hole can recombine with one of the bonding electrons, as a result the positively charged structure turns into the E' center (Equation 4.5) [43.44], with one of the silicon atoms retaining the remaining electron from the broken bond [23]:

$$\equiv Si - Si \equiv \; + \; h^{+} \xrightarrow{Irradiation} \equiv Si \cdot \mathrm{K}\; {}^{+}Si \equiv \; {}_{\text{(E' center)}} \qquad (4.5)$$

Where $\equiv Si - Si \equiv$ denotes the strained silicon-silicon bond. The following Figure 4.4 shows the hole trapping process and generation of E' center.

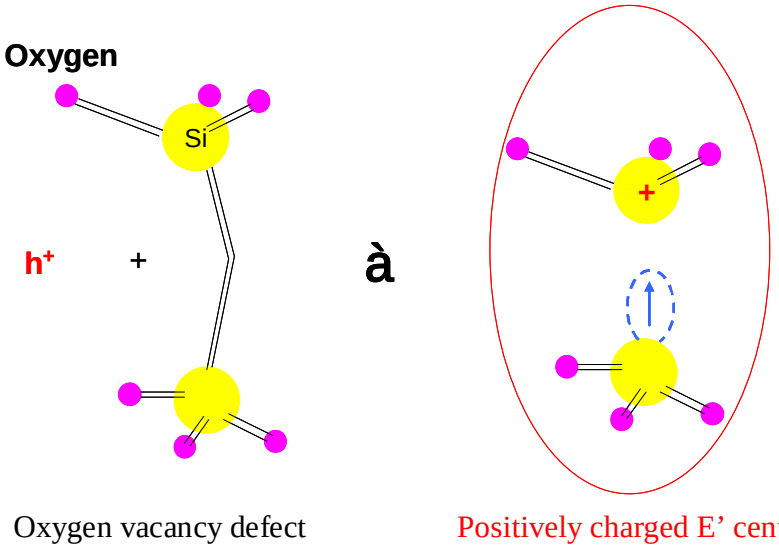


Figure 4.4 Generation process of E' center by capturing a hole in the oxygen vacancy defect.

From the point of view of macroscopic properties, the radiation-induced electron-hole pairs will be firstly separated under the influence of electric field by exposing MOS structure to ionizing radiation, and then some fraction of holes have enough time to migrate through the bulk oxide, and finally are trapped near the interface, causing a negative voltage shift in their electrical characteristics (V_T or V_{FB}) on the MOS devices that can persist for hours to years [45]. The following paragraph is focused on the buildup of voltage shifts due to positive oxide charges. The whole process of surface damages due to ionizing radiation is shown in Figure 4.5.

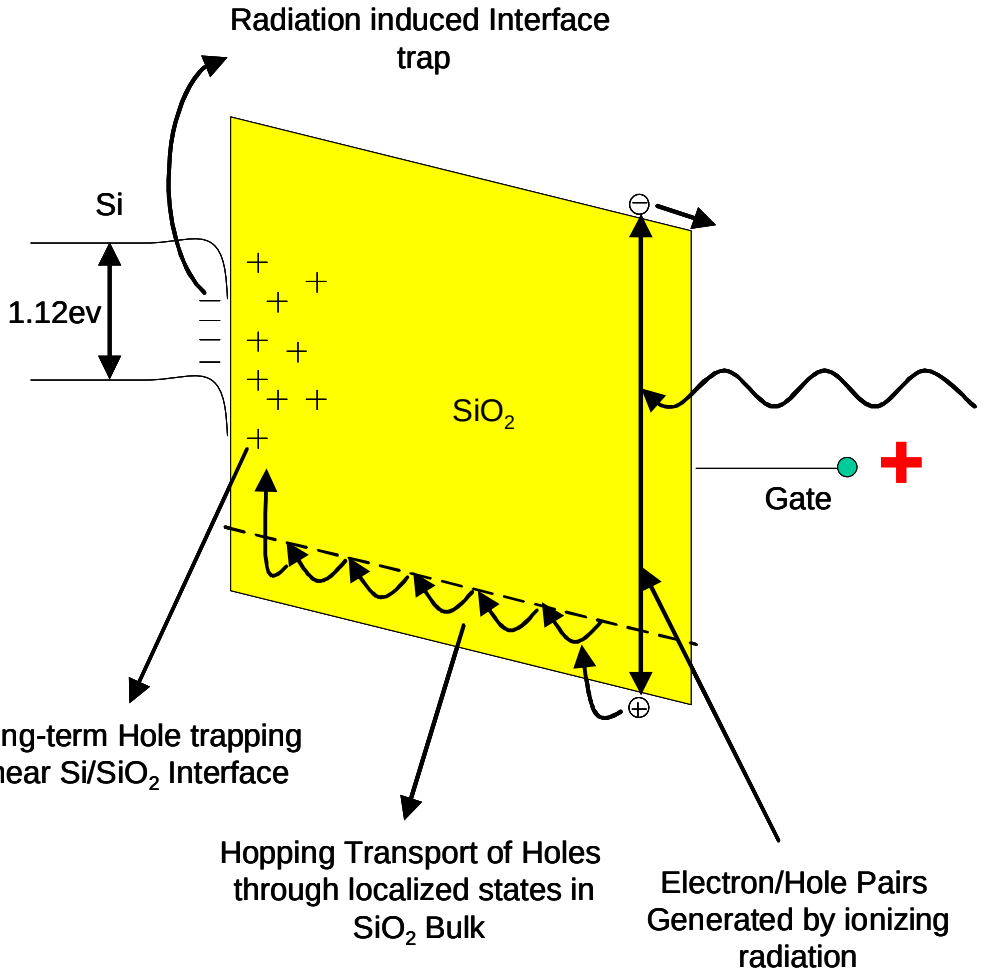


Figure 4.5 Ionizing radiation-induced positive oxide charges as well as interface traps in the oxide.

As illustrated in the Figure 4.5, a MOS structure is irradiated by X-ray under positive gate voltage. Trapping processes occur near the interface region and extend into the oxide up to a few nanometers. The remaining holes drift further into the silicon substrate and recombine with electrons in the silicon. Most of the holes generated by ionizing radiation are captured by hole traps within the region near the interface and can finally be partly annealed through the tunneling process. For an irradiation under negative gate voltage, the holes induced in the SiO_2 will drift to the gate and can still build up positive oxide charges. However, it is significantly smaller than in case of positive gate voltage, since the hole traps are mainly distributed near the interface. In case of a zero gate voltage, the recombination process will play an important role. Firstly, it includes the recombination of free electrons with free holes. Secondly, the generated electrons will also pass through the trapped holes and result in the recombination of a fraction of trapped holes depending on the applied gate voltage. Typical charge buildup characteristics of the MOS devices are shown in the Figure 4.6.

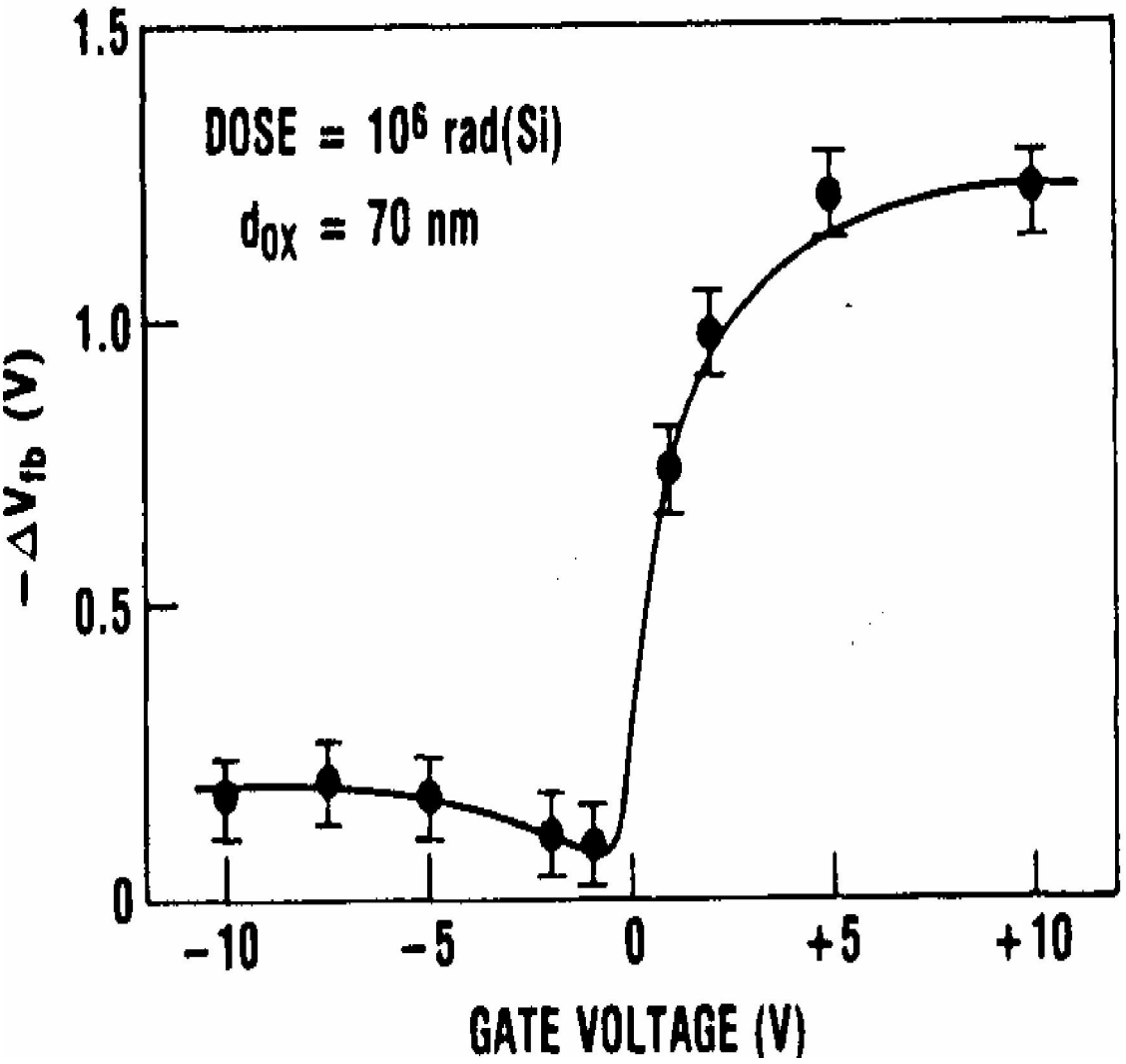


Figure 4.6 Radiation-induced flat band voltage shifts in a MOS capacitor as a function of gate voltage during irradiation [23].

The charge generation process (positive oxide charges) can be described by the following incremental form according to the Dimaria model [23.46]:

$$\Delta N_{ox}(x,\Delta D) = f_h \sigma_{ht}\left[\overline{N_{ht}(x)} - N_{ht}(x)\right] - f_e \sigma_r N_{ht}(x) \tag{4.6}$$

Where D is radiation dose with $D = R \times t$, R is the dose rate, and t is the irradiation time, $\overline{N_{ht}}$ is the local density of hole traps (precursors), and σ_{ht} is the effective hole trapping cross section, σ_r is the capture cross section of hole traps for recombination of an electron with a trapped hole, f_h and f_e are the fluences per unit dose of radiation-induced holes and electrons, respectively, and N_{ht} is the density of trapped holes. The

quantity in brackets is the density of unoccupied hole traps. The capture process becomes dominant in the case of a positive gate voltage. Moreover, without any biasing of the gate the recombination process cannot be neglected. For simplification the following assumptions are made [46]:

1. In general, the fluence of generated holes f_h per unit dose is equal to that of electrons (pair wise creation) f_e: $f_h = f_e$.
2. The capture cross section σ_r is approximately a factor of two smaller than the capture cross section of hole traps for capturing holes σ_{ht}.

Based the assumptions stated above, the equation 4.6 can be solved, which can further be simplified into Equation 4.8 [46]:

$$N_{ox}(D) = N_{ht}(D=0) + \frac{\sigma_{ht}}{\sigma_r + \sigma_{ht}} \overline{N_{ht}} \left(1 - e^{-(\sigma_r + \sigma_{ht}) f_h D}\right) \tag{4.7}$$

$$N_{ox}(D) = N_{ht}(D=0) + \overline{N_{ht}} \left(1 - e^{-\sigma_{ht} f_h D}\right) \tag{4.8}$$

This result describes a dose-dependent capture process of holes on the oxygen vacancy defects. Using equations 3.1 and 3.2 an irradiation dose-dependent correlation for the flat band voltage shift can be calculated. Assuming that the initial state of defects before irradiation is usually small and can be neglected, one can give a simplified expression of positive oxide charges:

$$N_{ox}(D) = \overline{N_{ht}} \left(1 - e^{-\sigma_{ht} f_h D}\right) \tag{4.9}$$

The radiation-generated positive oxide charges result in the flat band voltage shift of a MOS capacitor. The magnitude of this shift will decrease as the oxide thickness is reduced. In general, the buildup of the positive oxide charges follows a power law dependence d_{ox}^{n}. Many studies over the range of oxide thickness from a few nanometers to around 100nm have been reported by Saks et al. [23]. As shown in the Figure 4.7, a square-law dependence of radiation-generated flat band voltage shift (d_{ox} > 10nm) was observed. With respect to much thinner oxide thickness (d_{ox} < 10nm), a tunnel process for trapped holes becomes relevant. Accordingly, this shift will decrease sharply.

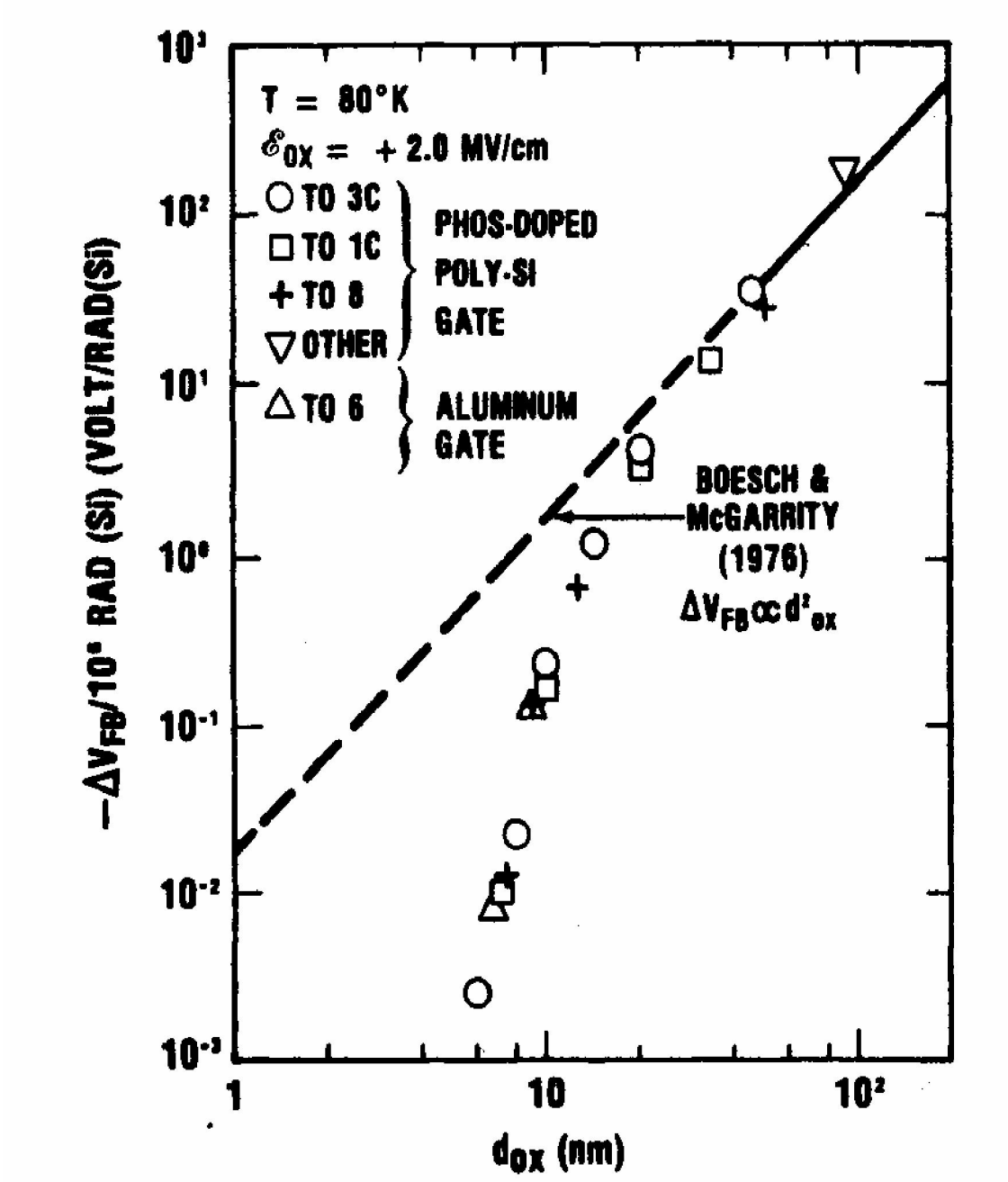


Figure 4.7 Flat band voltage shifts per unit dose as a function of oxide thickness for various MOS capacitors irradiated in a Co60 source at 80K. The d_{ox}^2 dependence can be found for thicker oxides [23].

Interface traps

Due to incomplete oxidation there are some strained silicon bonds (dangling bonds), which can serve as interface traps with energy levels distributed in the forbidden band gap between oxide and silicon, whose concentration is about $10^{10}cm^{-2}$ depending on various influence factors, i.e., wafer processing, oxidation processing and substrate material, etc. In general, all interface traps are located within 1-2 atomic bond distances (~0.5nm) from the silicon lattice [50]. As a result, electrons and holes can interact with interface traps. On the other hand, interface traps are as mentioned above amphoteric, i.e., depending on the position of trap level with respect to the Fermi level, their charge state can be positive, neutral or negative — donors or acceptors. When a donor trap level is below the Fermi level, it is occupied by an electron and shows neutral charge state. When it is located above the Fermi level, it will give up an electron and consequently be positive. An acceptor trap level works in a similar way being negative in occupying an electron and neutral when releasing an electron. Another property is the U-shaped distribution of the interface traps density across the silicon energy band gap. Interface traps density for <100> material is an order of magnitude smaller than for <111> material. In the following, a model is proposed illustrating the generation process of interface traps and the annealing process.

At the moment, many models have been proposed to describe the generation process of interface traps due to ionizing radiation. Three most popular models for the generation of interface traps are:

1) Hydrogen model (McLean model) [23]: this model introduces a two-step process. In the first step the trivalent silicon is passivated by hydrogen during the annealing process before ionizing radiation. The hydrogen complex can be broken up due to irradiation and initiate the production of trivalent silicon. In the second step, radiation-induced hole drifts through the oxide towards the interface and react with the trivalent silicon from the first phase to form the interface traps.

2) Injection model [23]: this model describes conversion of trapped holes at the SiO_2/Si interface into interface traps with the help of electron injection by the ionizing radiation or tunneling process from silicon. According to this model, the capture of electrons by the trapped holes is not a simple recombination process, since holes and electrons recombine in a certain way to form an interfacial structural change with a dangling bond and as a result serve as an interface traps.

3) Stress model [23]: this model associates with stress — bond strain gradient model (BSG). It describes the strained Si-O bond can be firstly broken up by a trapped hole induced by irradiation. One part of the remnant is the dangling silicon bond that results in hole traps; the other part of the remnant is a non- bridging oxygen defect that may move towards the interface, which is enhanced by OH groups. Dangling silicon bonds result in interface traps after migration of the defects. To

date although there is still discussion as to whether the BSG model is the right damage mechanism, the concept according to this model is acceptable considering the defect propagation that is driven by strain gradient.

Among these above three models, the hydrogen model is in the largest part for explaining the generation of interface traps and it is described in detail for the following [23].

This two-step process introduced by McLean has been proven to be able to explain the experimental results successfully. Hydrogen is the most important component for the generation of interface traps. It can passivate the silicon dangling bond and may be dissociated from the silicon bond by ionizing radiation, especially positively charged hydrogen obtained by capturing a hole for neutral hydrogen (i.e. proton). This is why the radiation-generated interface traps reach their maximum under positive gate voltage compared with the other polarities (negative and zero gate voltage). As a result, two important series of reactions that contribute to the generation of interface traps designated with red rectangle (shown in the following two set of reactions) will be introduced here:

i. The first reaction occurs directly in the interface region: as discussed above, holes are generated by exposure to ionizing radiation and are, furthermore, separated by the positive gate voltage and drift towards interface through repeated capture and emission process (hopping transport). Normally, before ionizing radiation there are already some process-induced interface traps (e.g. trivalent silicon), which are passivated by hydrogen in the annealing process. However, due to irradiation they can be broken up and result in interface traps [(1)]. A neutral hydrogen atom released from silicon bonds can capture a radiation-induced hole to create a proton [(2)], which can react further with a Si-H bond to form an interface trap [(3)]. By irradiation under positive, electrons will be supplied for the generation of interface traps [(3/4)], which arise mainly from silicon, also from ionizing radiation [51]. For this reason, interface traps may be positively or neutral or negatively charged.

$$\left.\begin{array}{l} \equiv Si - H + h^+ \rightarrow \boxed{\equiv Si^+} + H\cdot \quad (1) \\ H\cdot + h^+ \rightarrow H^+ \quad (2) \\ \boxed{\equiv Si^+} + e^- \rightarrow \boxed{\equiv Si\cdot} \quad (4) \end{array}\right\} \text{à} \left\{\begin{array}{l} H^+ + e^- + \equiv Si - H \rightarrow \boxed{\equiv Si\cdot} + H_2 \\ H^+ + \equiv Si - H \rightarrow \boxed{\equiv Si^+} + H_2 \end{array}\right\} (3)$$

ii. Another contribution occurs in the transition region where a non-stoichiometric composition is present during the oxidation (near interface region). All defects associated with hydrogen or hydroxyl (OH) are of major importance since they can be dissociated by ionizing radiation to create either direct interface traps [(5)] or the important component (proton) [(6)] needed for interface traps, which can migrate further to the interface to react with a Si-H bond [52].

$$(6)\ \left\{\begin{array}{c} \equiv Si-OH+h^{+} \rightarrow \equiv Si-O\cdot+H^{+} \\ \equiv Si-H-Si\equiv+h^{+} \rightarrow \equiv Si-Si\equiv+H^{+} \\ (5)\ \equiv Si-OH \xrightarrow{Irradiation} \boxed{\equiv Si^{+}}+OH^{-} \end{array}\right\} \text{à}\ \equiv Si^{+}+e^{-} \rightarrow \boxed{\equiv Si\cdot}\ (4)$$

Or through migration of proton to the interface for further reaction

$$\left.\begin{array}{l} H^{+}+e^{-}+\equiv Si-H \rightarrow \boxed{\equiv Si\cdot}+H_2 \\ H^{+}+\equiv Si-H \rightarrow \boxed{\equiv Si^{+}}+H_2 \end{array}\right\}\ (3)$$

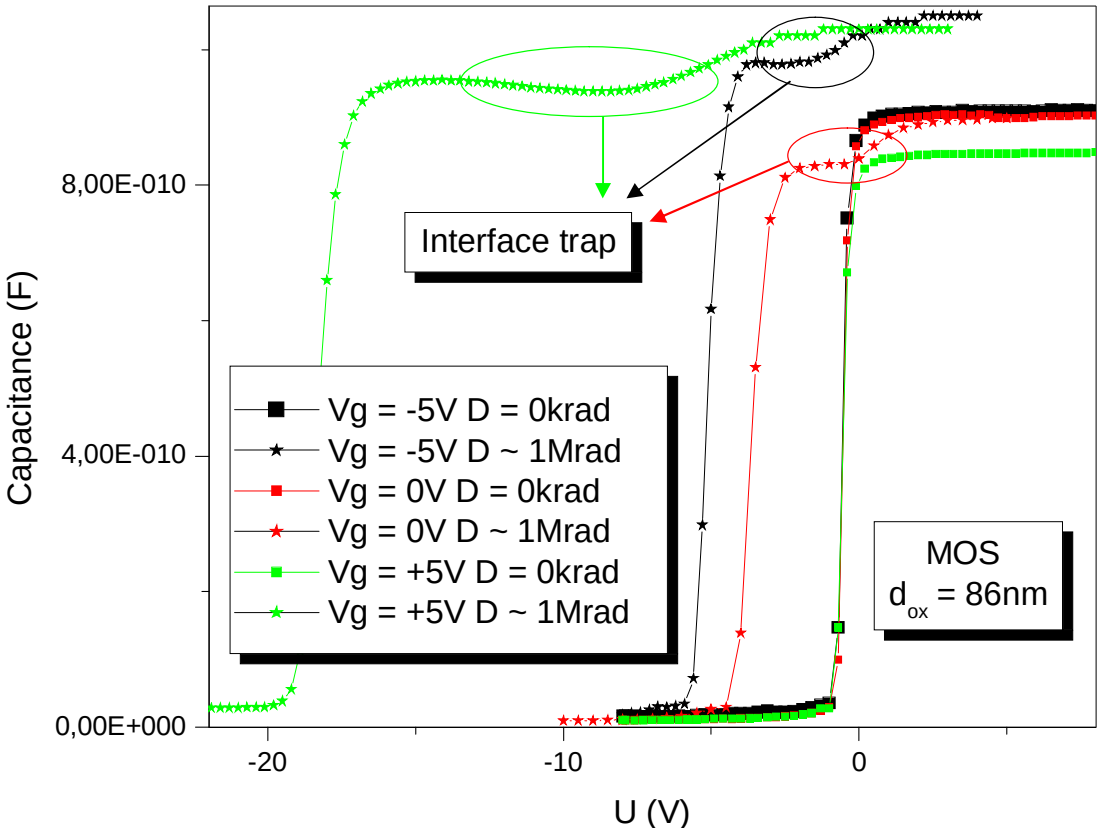


Figure 4.8 Irradiation experiment of a MOS structure with 86nm oxide. The CV (HF) lines are plotted before and after irradiation of about 1Mrad under different gate polarity. The shoulders designated with ellipse denote that the interface traps are energetically distributed near the conduction band.

In a word, the primary origin of interface traps can be traced back to the mechanical stress during the processing or oxidation and also abnormal chemical composition at the interface region (defects complexes). Since hole or proton can migrate to the interface region near the interface under the influence of an applied positive gate voltage, a maximum of interface traps generation is accordingly observed by irradiation

experiments; in the case of negative gate polarity the damage is reduced, since not only positive ions and holes drift to the gate electrode but also hydroxyl (OH) mentioned above move back to the interface captured by trivalent silicon. At zero field, a minimum of damage is achieved because the recombination of electron-hole pairs is enhanced.

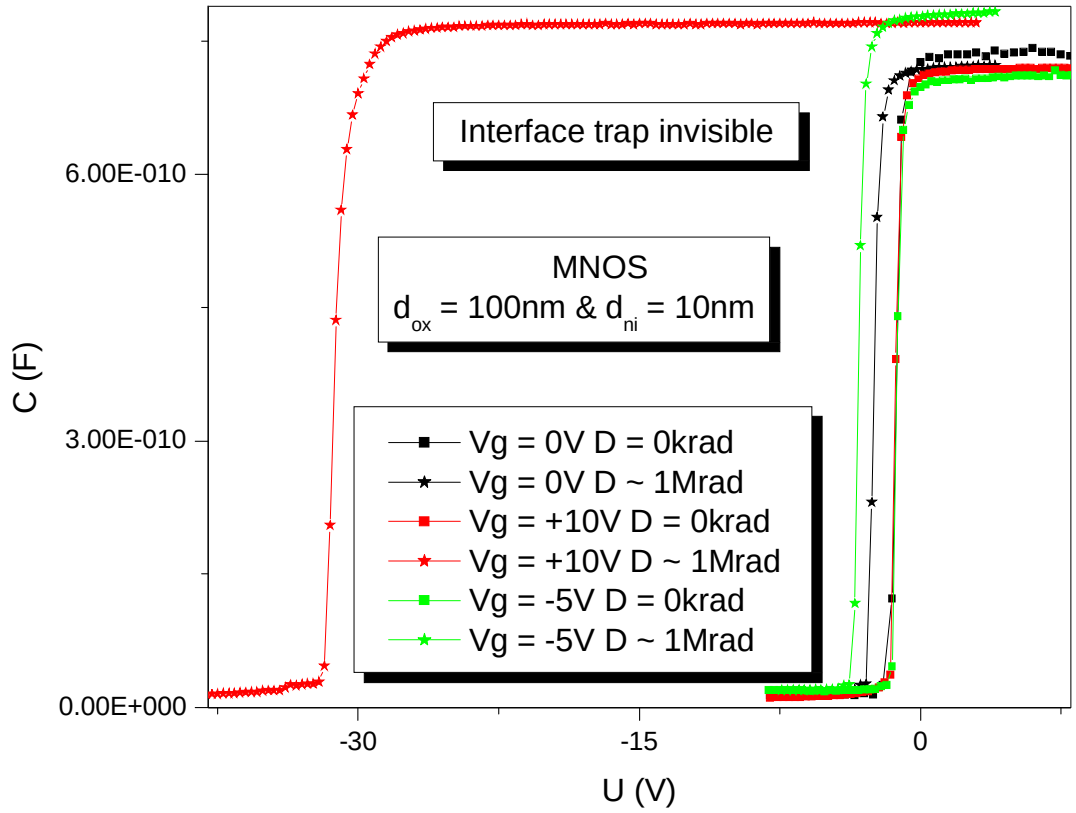


Figure 4.9 Irradiation experiment of an MNOS structure with 100nm oxide and 10nm nitride. The CV (HF) lines are plotted before and after irradiation of about 1Mrad under different gate polarity.

Figure 4.8 shows the radiation damages of a MOS structure under different gate voltages measured by CV measurement. As mentioned previously, the positive oxide charges may affect the CV lines in such a way that the flat band voltage shift varies with increasing radiation dose to more negative values measured by high-frequency CV measurement, while the interface traps can also affect the form of the high-frequency CV (Figure 4.2 left), since interface traps are amphoteric, and have energy levels in the whole silicon energy band gap. It is visible in Figure 4.8 that the shoulders (marked with ellipse line in three different colors) occur by irradiation. They can be traced back to the interface traps that are generated at the Si/O interface. These interface traps are distributed within the energy level between the mid-gap level and conduction band and thus exhibit positive charge. In addition, they make the flat band voltage shift of low-frequency CV to more negative values. Moreover, the capacitance value of the CV lines can be considered as the oxide capacitance C_{ox} in accumulation (see Chapter 2), however, in reality before irradiation it is experimentally found to be much less than C_{ox} because such a MOS

structure has a higher ohmic contact at the backside. After irradiation, it can increase to a certain extent due to interface traps if a gate voltage is applied, but it still does not reach C_{ox} as it should be. In the case of zero gate voltage, interface traps reach their minimum value and accordingly the capacitance value does not increase significantly.

Similar to Figure 4.8, Figure 4.9 also shows the radiation damages of an MNOS structure under different gate voltages. No shoulders can be observed in the measured high-frequency CV lines. It is probably that interface traps generated at the Si/O interface is energetically located at the energy band middle and exhibits zero charge. Furthermore, the capacitance value of the CV lines can still be observed to increase after irradiation if the gate is biased. In the case of zero gate voltage, there is no increase of capacitance value observable.

Chapter 5 Irradiation experiments

In this chapter, the complete experimental setup for the study of radiation hardness will be described. All of the irradiation experiments are performed using X-ray at the Max-Planck-Institute for physics Semiconductor Labor Munich (CaliFa) and at the Forschungszentrum Karlsruhe. The X-ray setups are initially calibrated with the help of staff from both institutes. Hence, the procedure of calibration will not be described in detail. Other irradiation experiments, e.g. proton/neutron/gamma ray, will also be introduced in this chapter. The main goal of these irradiation experiments is to characterize the radiation hardness of MOS structures produced on different devices. Of course, all of the test chips should be irradiated under the same conditions in order to achieve relatively reproducible radiation effects and to extract the correlation of radiation hardness depending on the characteristic parameters.

5.1 Photon irradiations

X-rays are a type of electromagnetic radiation. They are useful in many application areas (e.g. medical, science and space). The basic source of X-ray is using X-ray tube. Normally electrons emitted from cathode collide with the tungsten target (or molybdenum) and can further accelerate electrons, ions and nuclei within the target material, and a small portion of the energy released is radiated. As a result, X-rays are formed and emitted out of the tube along the path perpendicular to the electron beam.

The spectral lines generated depend on the target material and, therefore, are called characteristic lines. They come about through transitions from upper shells of an atom into lower shells. This means that the interior electrons of atom are kicked out by the incoming energetic electrons. Consequently the generated vacancies will be occupied by electrons from the outer shell. The released energy is equal to the difference between these two energy levels and occurs in form of characteristic Bremstrahlung with discrete wave lengths. In addition, there are also continuum spectrums by the electrons due to scattering of electrons near the nuclei. The total spectrums of the X-ray tube are characteristic lines superposed by continuum spectra.

In general, gamma rays also belong to X-rays, which are distinguished from X-rays only by a different generation process: i.e. X-ray photons are generated by energetic electron processes and gamma rays by transitions within atomic nuclei. With the generated X-rays MOS devices are irradiated. Generally, X-rays are absorbed in the material by three different effects depending on its energy distribution: photo electrical effect, Compton scattering and pair production [39]. Normally there are only surface damages produced by X-ray, however, not only surface damages but also bulk damages (displacement

damage — point defects) in the silicon bulk can be produced by high energetic gamma rays; this is due to secondary electrons by Compton scattering.

5.2 Proton/neutron

Protons are charged particles. Not only surface damages but also bulk damages will be generated due to the charged particles. A series of parameters will be changed due to bulk damages, such as doping concentration (related to the depletion voltage) of material and volume generation current (related to leakage current and further to noise).

Another particle irradiation comparable with protons is neutron irradiation that does not result in any surface damages in the oxide layer, since the charge state of neutron is zero. Due to NIEL (Non-Ionising-Energy-Loss) neutrons can displace an atom out of its lattice site resulting in interstitials and vacancies in silicon bulk, both can move through the lattice and lead to point defects [40]. A high concentration of the accumulated point defects can result in the clusters. For this reason, surface damage is not an issue under such irradiation environment. Furthermore, it is possible to distinguish between bulk damage and surface damage using neutron as irradiation source compared with proton irradiations under the same radiation dose.

For example, using irradiation facilities at CERN, 24GeV proton beams are produced by a proton synchrotron, neutron of about 1MeV are available in reactors.

In order to compare the damage efficiency of different radiation sources with different particles and different particle fluencies, it is common practice to define the hardness factor κ in such a way that it compares the damage produced by a certain irradiation to the damage that would have been produced by neutron of 1MeV at the same fluencies [41].

As shown in Figure 5.1 the damage function D(E) for neutrons, protons, pions and electrons in an energy range from some meV to 10 GeV for the thermal neutrons is given [41]. At lower energy, the proton damage function becomes the most important due to Coulomb interaction that contributes very small for very high energies in the GeV range. Instead nuclear reactions are principally the same for protons and neutrons.

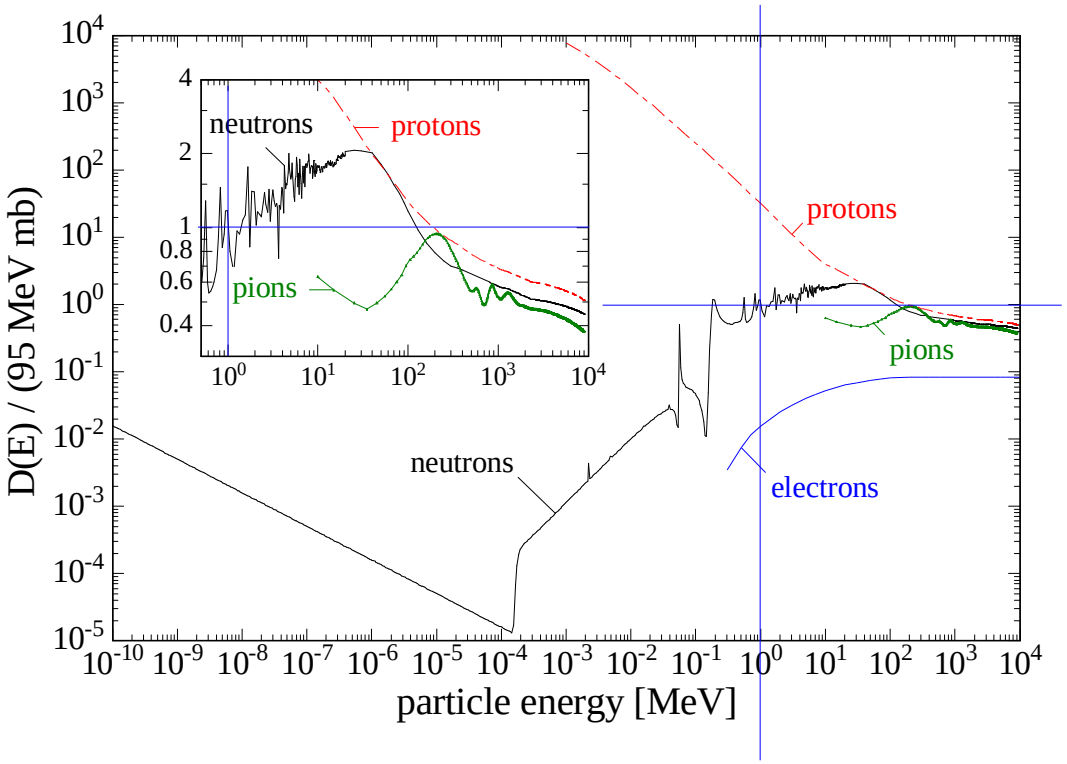


Figure 5.1. Displacement damage functions D(E) normalized to 95 MeVmb for neutrons. Due to the normalization to 95 MeVmb the ordinate represents the damage equivalent to 1MeV neutrons. The insert displays a zoomed part of the Figure [41].

5.3 Experimental setup

As mentioned above, two different setups for generating X-rays will be introduced in this paragraph: CaliFa in Munich and the Roentgen facility in Forschungszentrum Karlsruhe.

- Roentgen facility (CaliFa): it serves for studies of the radiation hardness of devices. The total setup is highly evacuated for low-energy measurements (lower than 1 keV) and also to prevent the attenuation of X-ray through the path.
  - X-ray tube produced by Seifert: one can get a higher photon dose, which is used for irradiation experiments.

The CaliFa is shown in Figure 5.2. The setup on the left hand side is the high flux X-ray tube, which can offer a high flux of photon for the irradiation. In order to calculate the radiation damage that depends on the radiation dose, one has to know the photon dose of the X-ray tube. It is also necessary to calibrate the X-ray tube before any irradiation

measurements. During the irradiation experiments a molybdenum target is used. The output of X-ray tube is set by 30kV and 30mA. The dose rate is 9 krad/h.

Figure 5.2 CaliFa setup in Semiconductor Labor Munich, which can provide X-ray irradiation with energy of about 17 keV.

Due to the much higher photon flux of the X-rays it is difficult to measure the spectrum of the tube for the further calibration. Therefore, an additional zirconium iris is installed in front of the detector in order to reduce the count rate in such a way that the detector can record the spectrum of the tube. Due to the zirconium iris the flux of the tube is reduced to an appropriate value for the capture of spectrum; furthermore, the reduced flux will not change the form of spectrum, but rather the intensity. After the real spectrum of the X-ray tube is measured (Figure 5.3), one can calculate the count rate of the photons from the spectrum. In addition, the measurement time, dead time and area of the detector have to be considered.

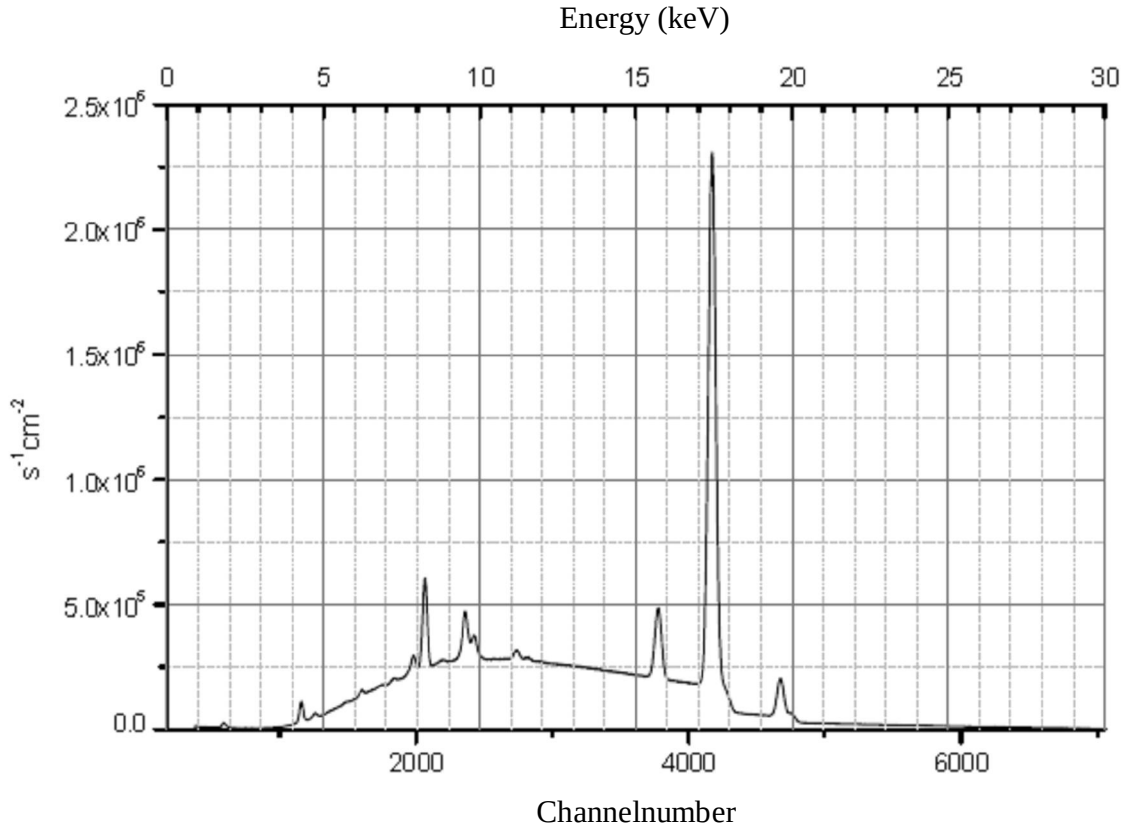


Figure 5.3 the measured spectrum of CaliFa setup in Semiconductor Labor Munich, by which a molybdenum-tube is used.

In order to check the calibration, a PN diode is used that is produced at the semiconductor labor. The PN diode is completely depleted and the photocurrent of the diode is measured and compared to the above one. Difference from these two approaches is about 15% [22], which is acceptable.

The international system of units for radiation dose is Gray (Gy). The radiation dose is defined as quotient of absorbed energy E and the mass of the material m: $D = dE/dm$. This means: 1Gy = 1 Joule per kilogram [41]. However, Rad. Used as the unit of the irradiation experiments has already been widely accepted in the literature. The relation between rad. and Gray is: 1 Gy = 100 rad. The dose rate of this x-ray tube is set to 9 krad/h.

- The X-ray irradiation facility in the institute for experiment nuclear physics Karlsruhe (IEKP) at Forschungszentrum Karlsruhe: Generally it was built to study radiation damages (ionizing radiation). The X-ray source is also a high flux X-ray tube.

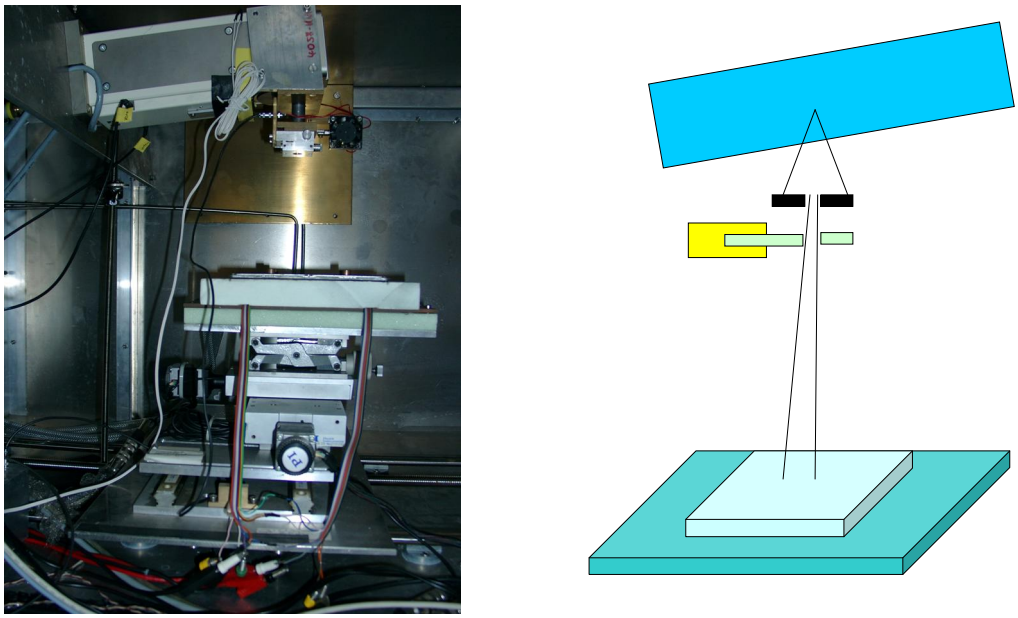


Figure 5.4 X-ray setup: it consists of an X-ray tube, an adjustable collimator, shutter and XY probe station.

In order to achieve a focused X-ray beam, an adjustable collimator is built directly underneath the tube (Figure 5.4). The achieved focused beam point is about 1.6 cm in diameter so that the MOS devices (8*8 mm^2) can be mounted on an aluminum carrier that is located in the center area of the XY probe station to make the dose variation across the devices as small as possible. A computer controlled shutter is located very close to the collimator to switch the irradiation. Compared with X-ray tube in the CaliFa setup, a Tungsten as target is used to achieve the maximum output, which has a relative low characteristic energy. Of course a water-cooling system is also inevitable for the X-ray tube and HV generator. The output of this X-ray tube is set by 60kV & 25mA.

Using the calibration diode one can check the beam profile and the radiation dose for the irradiated devices. The used diodes were calibrated in an already known X-ray system at CERN. In addition, the corresponding radiation dose rate was determined using a certified dosimeter with an ionization chamber as sensitive devices. For the sake of protection of the tube the average dose rate is about 148 krad/h, although the maximum dose rate is 177.6 krad/h during the irradiation process. In comparison to the CaliFa, the sample can be irradiated up to about 1Mrad within seven hours instead of seven days.

Chapter 6 Irradiation of MOS-Structures

The goal of this thesis is focused on the radiation effects. Radiation damage is already known in many MOS devices through experimental determination. Within the scope of study of radiation damage, radiation effects on the MOS devices have been the central topic for many years. Considering ionizing radiation, for enough energy of photon quanta or charged incident particles not only electron-hole pairs but also bond breaking of atoms can occur mainly in silicon and silicon dielectrics.

		MOS-C				**MOS-DEPFET**		**MOS-Gated diode**			
Wafer	Silicon substrate (bulk)	450 (μm)				450 (μm)		450 (μm)			
	Gate contact and dielectrics (surface)	Al gate Type 1		Poly gate Type 2		Poly gate		Al gate Type 3		Poly gate Type 4	
		TO	LTO	TO	Nitride	TO	Nitride	TO	LTO	TO	Nitride
PXD4		180 (nm)	300 (nm)	180 (nm)	30 (nm)	180 (nm)	30 (nm)	180 (nm)	300 (nm)	180 (nm)	30 (nm)

DIO-318 A	MOS	86 Oxide (nm)	Type 5
DIO-318 B	MNOS	86 Oxide + 10 Nitride (nm)	Type 6
DIO-318 C	MOS	100 Oxide (nm)	Type 7
DIO-318 D	MNOS	100 Oxide + 10 Nitride (nm)	Type 8

Table 6.1 Dimensions of MOS devices used for characterization of radiation damage. PXD4 and DIO-318ABCD are project name.

In order to study the radiation effects on MOS structures, many MOS devices are irradiated, and a great deal of useful information can be gathered by using ionizing radiation as a tool. Since MOS devices mentioned below are produced in the same processing, it is thus useful for the comparison of the experimental results with the same structure profile. On the other hand, it is also good to understand the radiation effects using different characteristic parameters for the corresponding devices. MOS devices used in this chapter are the standard MOS capacitance, MOSDEPFET and MOS gated diodes (Figure 6.1). Each device has to be mounted to an appropriate carrier for the wire bonding in order to obtain the electrical contact with external measurement devices. The MOS capacitance and MOS gated diode can be adhered to a cubic copper box with five pins on each side, from which thinner wires can be bonded to the surface of MOS devices. MOSDEPFET has to be glued on a ceramic carrier with twenty aluminum pins on each side. Bulk and surface parameters of MOS devices are described in Table 6.1.

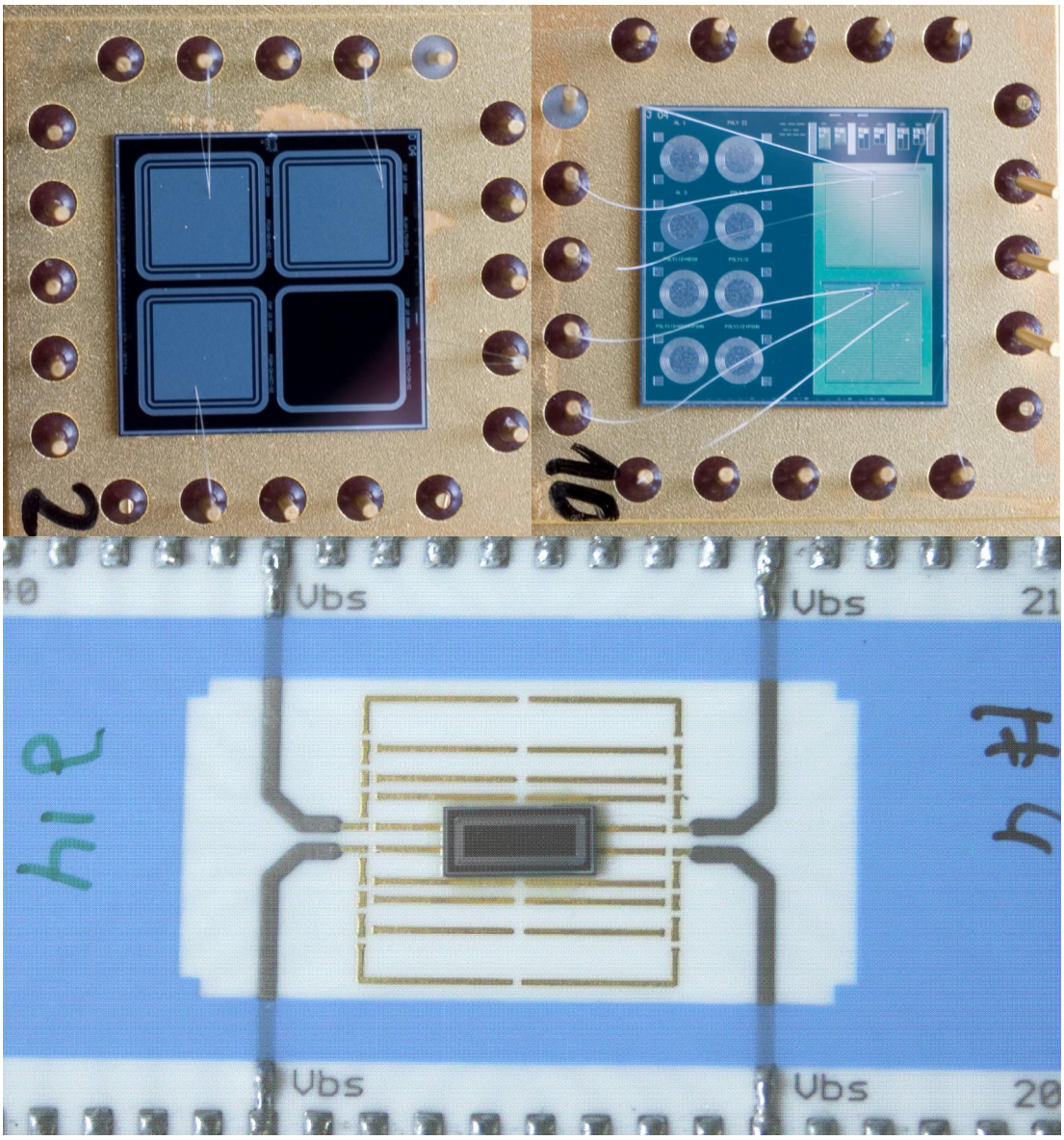


Figure 6.1 Real MOS-devices: standard MOS capacitance (top left); MOS gated diode (top right); single MOSDEPFET (bottom).

6.1 Dose

Radiation dose is the most important parameter that records the radiation level absorbed in the material. In the case of the samples used in this thesis the generated surface damages increase almost linearly with the increasing radiation dose at low dose up to

about 10^5 rad. With further increasing dose the surface damages increase slower and finally will saturate.

Standard MOS capacitance

The positive oxide charges are a part of surface damages resulting in a shift of flat band voltage towards more negative values shown in Figure 6.2 (for N-doping substrate, for P-doping substrate the CV curves look like exactly reversed).

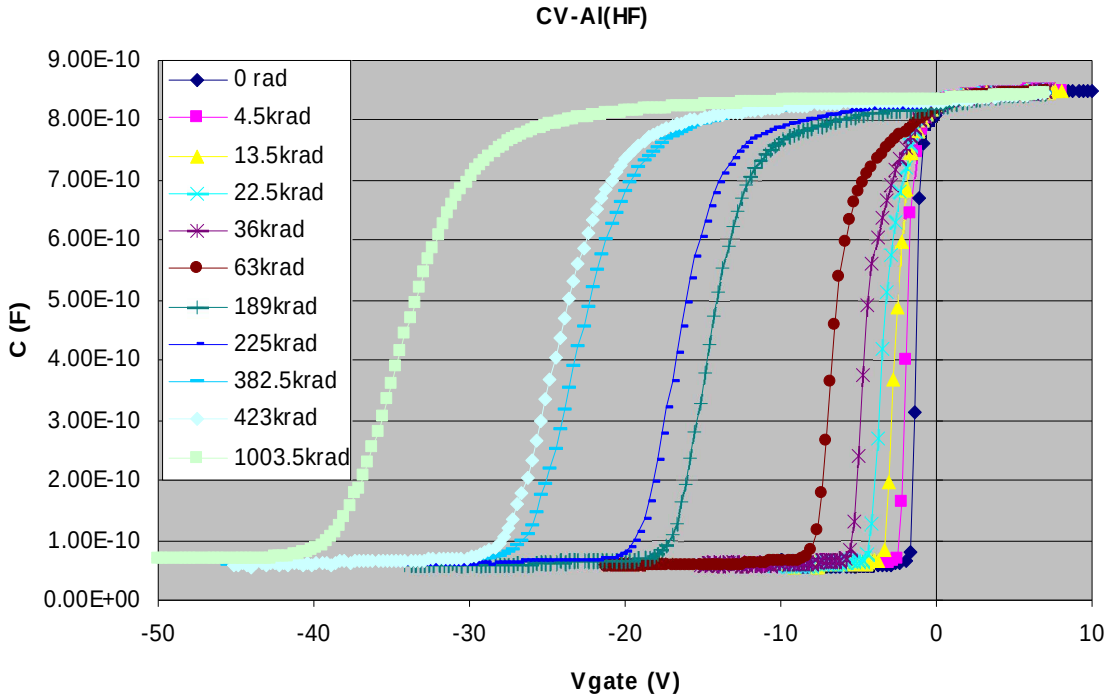


Figure 6.2 Shift of flat band voltage: CV measurement at high frequency for Al-gate MOS structure (type 1).

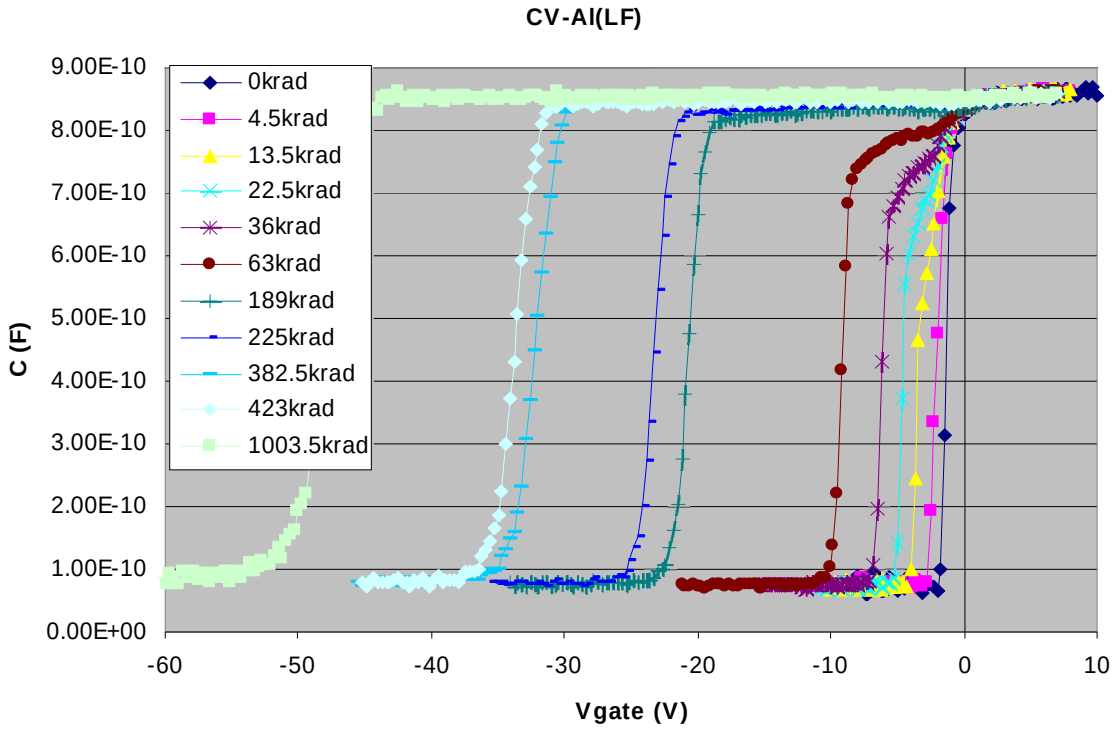


Figure 6.3 Shift of flat band voltage: CV measurement at low frequency for Al-gate MOS structure (type 1).

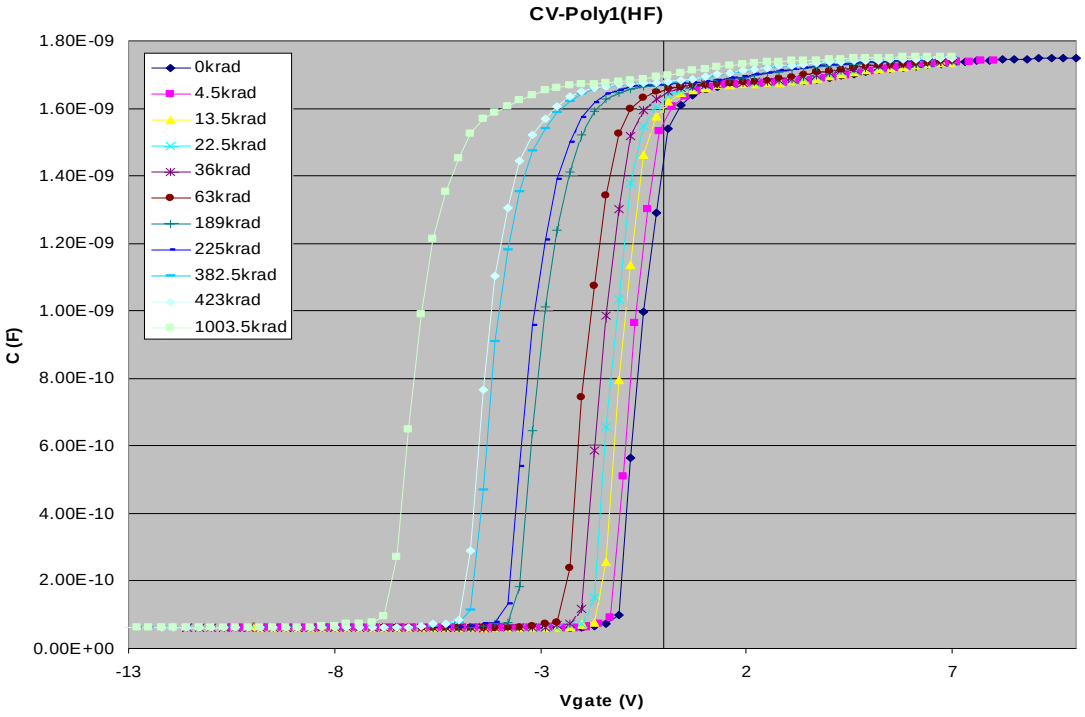


Figure 6.4 Shift of flat band voltage: CV measurement at high frequency for Poly-gate MOS-structure (type 2).

As shown in Figures 6.3 and 6.4, CV curves with different color correspond to different radiation dose. From the shifts of flat band voltage extracted from high-frequency CV curves the positive oxide charges can be determined since it is assumed that the interface traps cannot follow the high-frequency signal and accordingly cannot be detected. On the other hand, interface traps can be determined from the comparison of high-low frequency CV curves (stretch-out form).

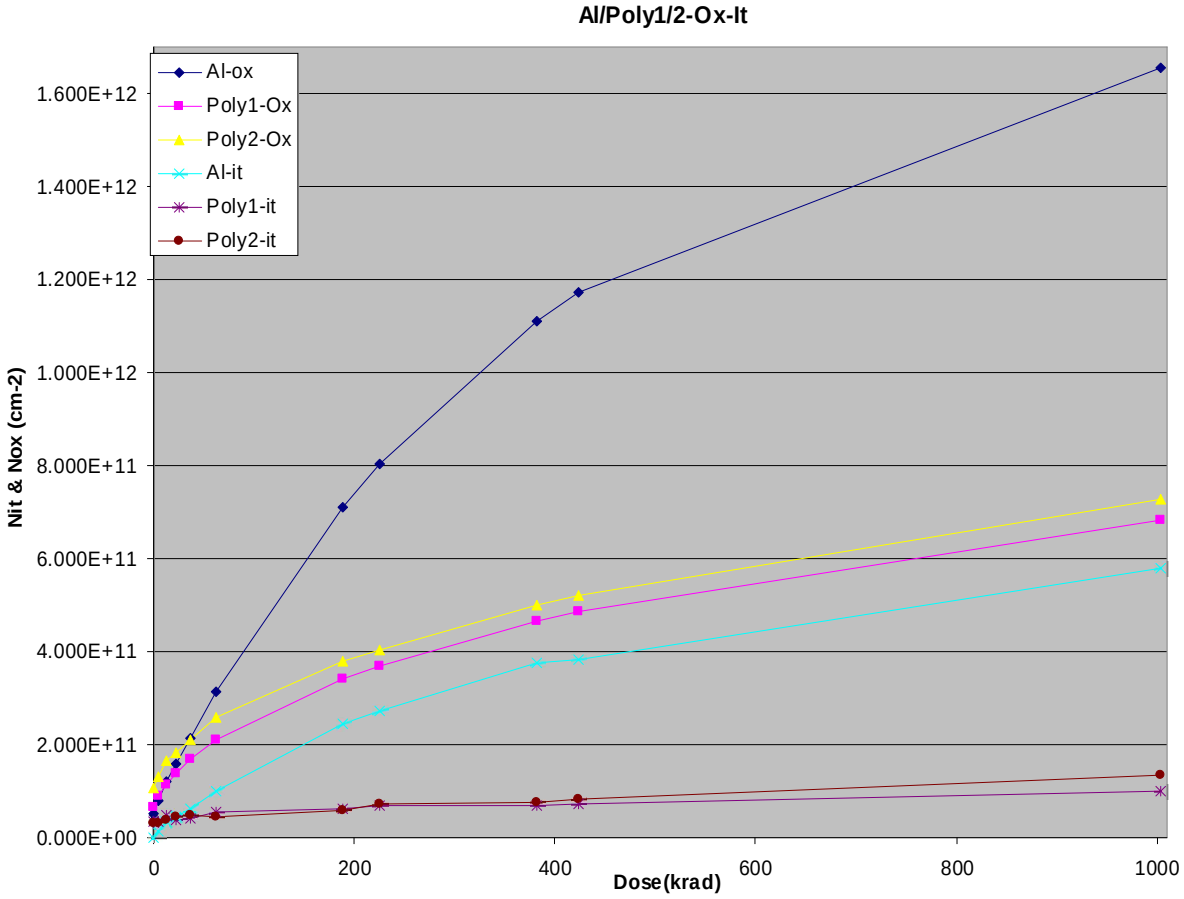


Figure 6.5 Surface damage as function of radiation dose: positive oxide charges (N_{ox}) and interface traps (N_{it}) for Al- and Poly-gate structure (type 1/2) show an exponential increase with dose.

Surface damages are plotted in Figure 6.5 with oxide charges and interface traps concentration as a function of radiation dose. Surface damages increase almost linearly in the lower radiation dose region and further becomes exponential proportional with increasing dose. Both types of surface damages (Positive oxide charges and interface traps) for Al-gate structure are much higher than those of Poly-gate structure, because the oxide thickness in Al-gate structure is much thicker than that of Poly-gate structure

The radiation-generated positive oxide charges have been already discussed previously by Equation 4.9:

$$N_{ox}(D) = \overline{N_{ht}}\left(1 - e^{-\sigma_{ht} f_h D}\right)$$

In order to analyse the radiation damages quantitative, discussion of this formula is given below. The fluence of electron or hole due to ionizing radiation per unit dose depends on the oxide thickness and electric field, and is factorized as:

$$f_h = d_{ox} \times K_g(E) \times f_y(E_{ox}) \tag{6.1}$$

Where K_g is energy-dependent charge generation constant in the oxide layer, f_y is the fractional charge yield and depends on the electric field. d_{ox} is the oxide thickness. Benedetto et al. have evaluated these parameters as $K_g \approx 1.3 * 10^{-6} \left[C / cm^3 / rad(SiO_2)\right]$ and f_y is given by an empirical expression in case of X-ray irradiation [24]:

$$f_y(E_{ox}) = \frac{1}{1 + \frac{1.3}{0.113 + E_{ox}}} \tag{6.2}$$

Where E_{ox} is the electric field in the oxide and in megavolts per centimeter:

$$E_{ox} = \frac{V_{ox}}{d_{ox}} \tag{6.3}$$

The field dependent effective hole trapping cross section describes the efficiency of hole capture by the traps in the oxide, and is observed to behave as:

$$\sigma_{ht}(E_{ox}) = \frac{\sigma_0}{E_{ox}^n} \tag{6.4}$$

Another important parameter σ_r is the cross section for recombination of electrons with trapped holes, which is also electric field dependent and can be considered as an essential parameter for the process of electron-hole recombination via the hole traps. Consequently it has a major importance in the limit of hole trapping at relative high doses and is also responsible for the saturation effect of the flat band voltage.

In the exponential expression, the quantity $\sigma_{ht} f_h$ is electric field dependent and can be factorized as:

$$\sigma_{ht} f_h = d_{ox} \times K_g(E) \times f_y(E_{ox}) \times \sigma_{ht}(E_{ox}) \tag{6.5}$$

According to Equation 4.9 given previously, the shift of the flat band voltage can be determined by the following form:

$$\Delta V_{FB}(MOS) = -\frac{N_{ox}}{C_{ox}} = -\frac{\overline{N_{ht}}}{C_{ox}}\left[1-\exp(-\sigma_{ht} f_h D)\right] \tag{6.6}$$

$\Delta V_{FB}(MOS)$ is the contribution of flat band voltage that comes only from the positive oxide charges measured by high-frequency CV method. It is obviously dose-dependent in an exponential way. Figures 6.6 and 6.7 show a series of lines that denote the dose-dependent flat band voltage shift at different gate voltages, these lines are measured on two MOS capacitances with 86 nm and 100 nm oxide layer thickness.

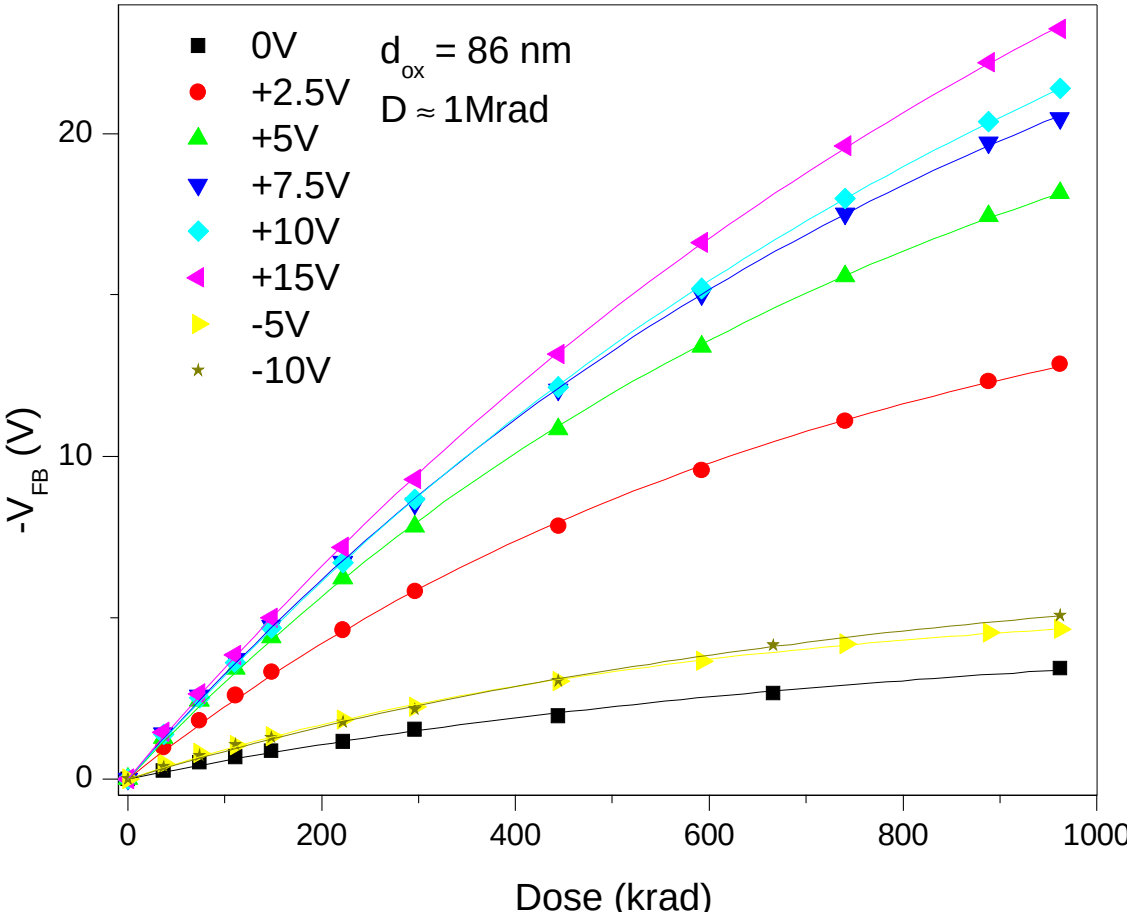


Figure 6.6 MOS structure of 86nm oxide thickness (type 5) under ionizing radiation up to about 1Mrad with different gate voltages. Points represent the measurements, while the lines denote the exponential fitting with Equation 6.6 for the shift of flat band voltage.

The constant factor N_{ht}/C_{ox} is determined by the hole traps (precursors at the Si/O interface), which represents the saturation value of the flat band voltage shift of a MOS structure at the corresponding gate voltage.

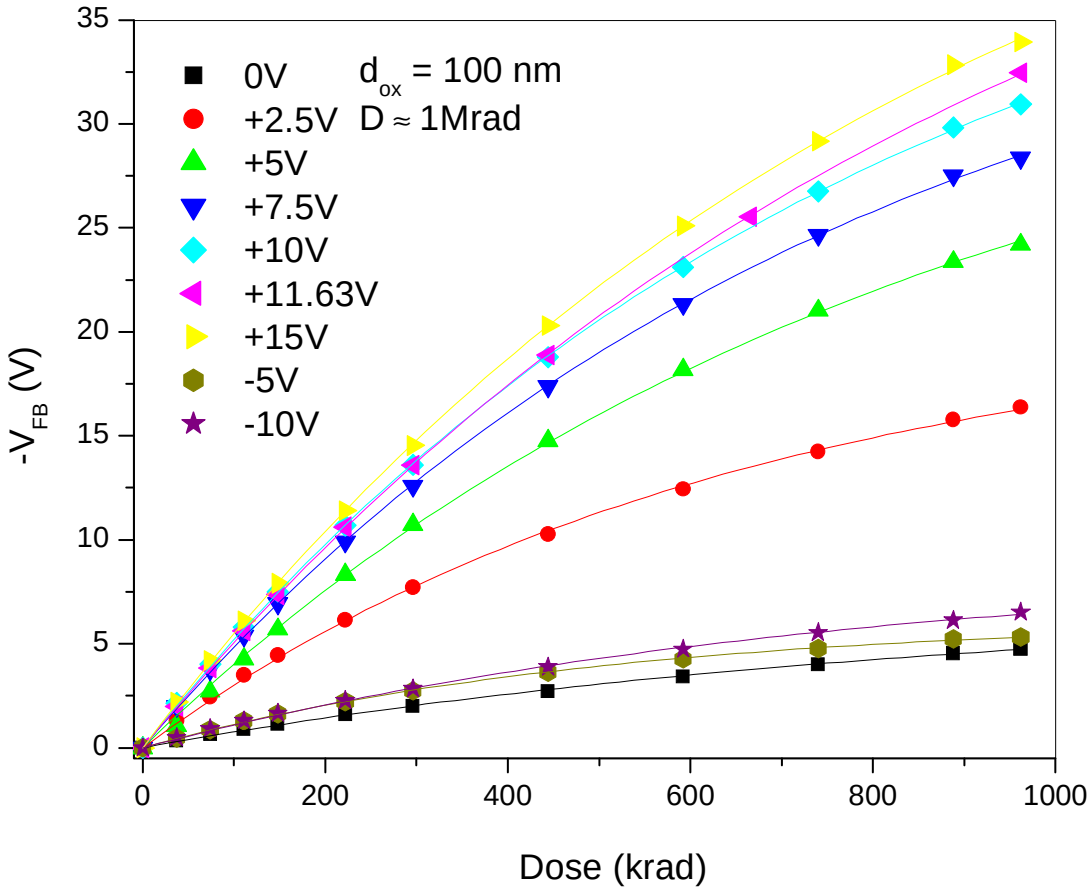


Figure 6.7 MOS structure of 100nm oxide thickness (type 7) under ionizing radiation up to about 1Mrad with different gate voltage. Points represent the measurement data, while the lines denote the exponential fitting with equation 6.6 for the shift of flat band voltage.

MOS			
86 nm	Type 5	100 nm	Type 7
Vg (V)	N_{ht}/C_{ox} (V)	Vg (V)	N_{ht}/C_{ox} (V)
-10	7.2	-10	9
-5	5.7	-5	6.3
0	4.8	0	7.2
2.5	17.4	2.5	21
5	26.6	5	32
10	36.5	10	44.6
15	40.9	15	51.6

Table 6.2 A list of factors N_{ht}/C_{ox} as a function of the applied gate voltage of a MOS structure with 86/100 nm oxide.

From Equations 6.2, 6.4 and 6.5,

$$\sigma_{ht} f_h = \frac{d_{ox} \times K_g(E) \times \sigma_0}{\left(1 + \frac{1.3}{0.113 + E_{ox}}\right) \times {E_{ox}}^n} \tag{6.7}$$

Figure 6.8 shows the quantity $\sigma_{ht} f_h$ as a function of electric field, which are extracted by the exponential fitting of dose-dependent flat band voltage shift. It is experimentally observed that this value decreases with increasing electric field, although the capture cross section of hole traps is inversely proportionality to the electric field. In other words, the flat band voltage shift will increase faster, i.e., it will reach its saturation value at relative lower electric field with increasing radiation dose, if it is assumed that the factor N_{ht}/C_{ox} is the same for each electric field.

In reality, this factor N_{ht}/C_{ox} will increase significantly with the increasing electric field (see Table 6.2), although N_{ht} clearly should not vary with the field. The higher the electric field the more holes will move to the Si/O interface to create positive oxide charges, more hole traps (precursors) at the Si/O interface are consumed.

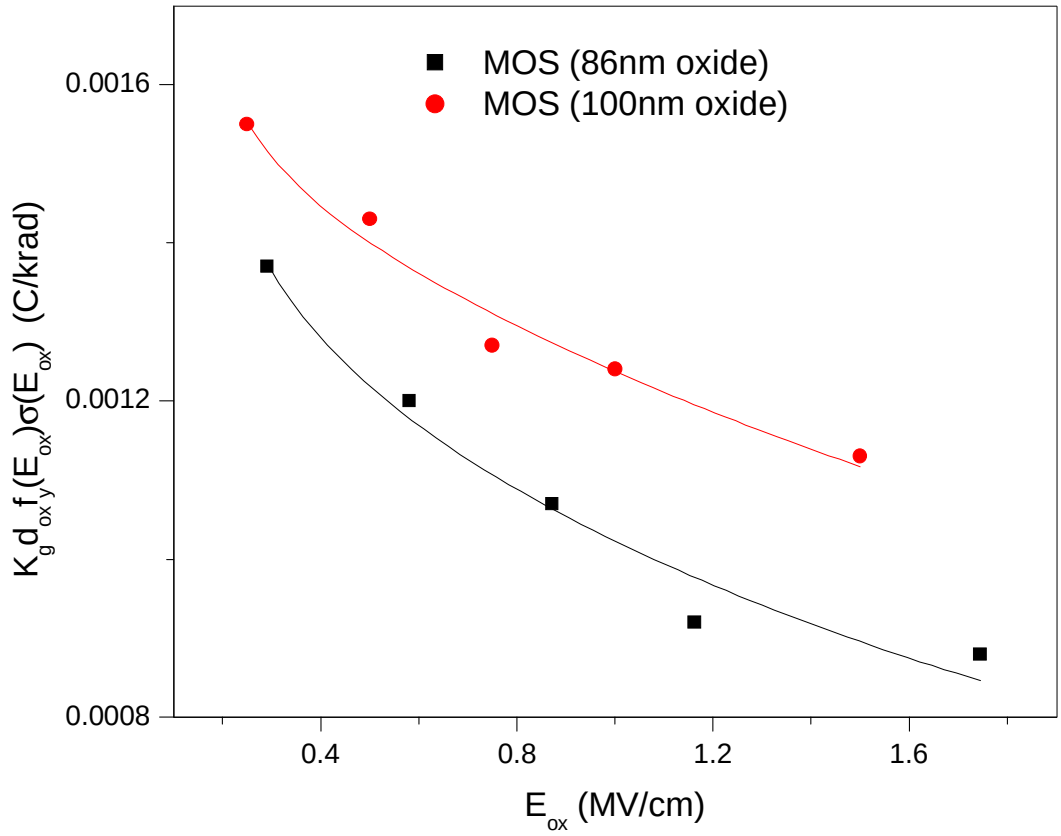


Figure 6.8 Fitting of the factor $\sigma_{ht} f_h$ for different oxide thickness (type 5/7) using Equation 6.7.

Accordingly these two factors discussed above compete to determine the shape of the exponential line: with increasing radiation dose the flat band voltage shift will increase slower and reach saturation earlier at lower electric field than at higher field.

The capture cross section of hole traps (see Table 6.3) extracted from these two different MOS capacitances (86nm and 100nm oxide thickness) is about $3*10^{-14}$ cm^2 at 1MV/cm and the field dependency is between $E_{ox}^{-0.7}$ and $E_{ox}^{-0.78}$ (Figure 6.9). The accuracy of the obtained capture cross section is about 10%.

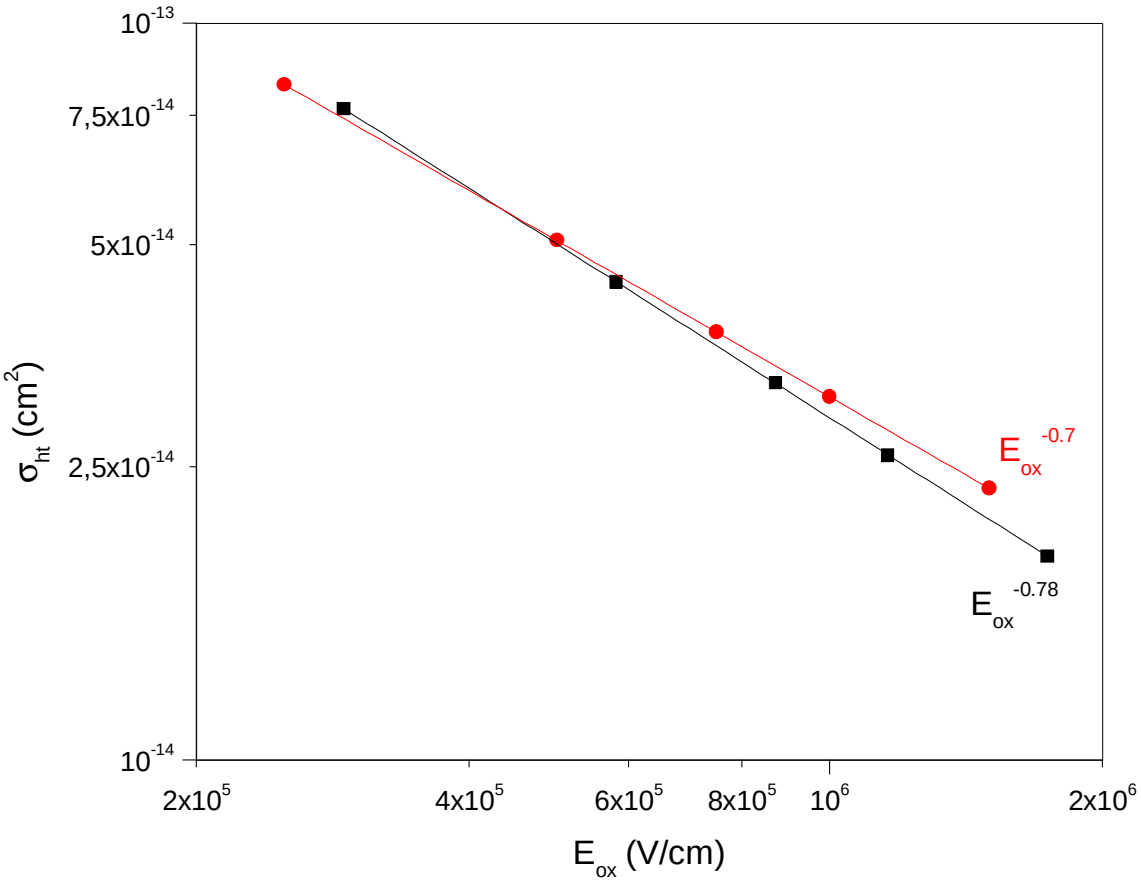


Figure 6.9 Oxide field dependence of the capture cross-section hole trap in SiO_2 determined from different wafers using Equation 6.4. Type 5 ($Eox^{-0.78}$) and type 7($Eox^{-0.7}$).

	d_{ox} (nm)	n	σ_0 (cm^2)	σ_{ht} (at 1MV/cm) (cm^2)
1	86	0.78	1.4 E-09	3 E-14
2	100	0.7	5.2 E-10	3.1 E-14

Table 6.3 Fitting results for capture cross section of hole traps.

MOSDEPFET

For MOSDEPFET one uses the threshold voltage as characteristic parameter instead of flat band voltage. It behaves with increasing radiation dose in the same manner as that of a MOS capacitance (Figure 6.10).

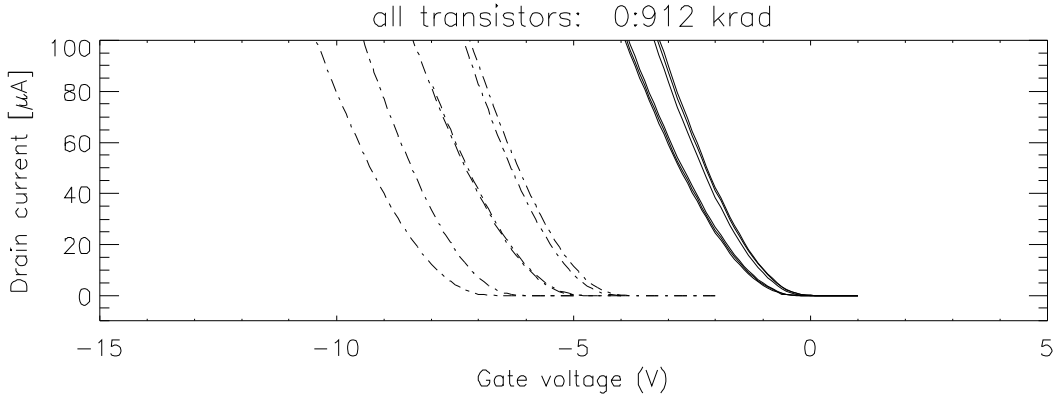


Figure 6.10 Characteristics of a p-channel MOSDEPFET (drain current vs. gate voltage). Shift of threshold voltage to more negative value with increasing radiation dose [2].

Applying different gate voltages (above or below the threshold voltage) on the gate contact make MOSDEPFET in ‘ON’ or ‘OFF’ state. As a consequence, the measured positive oxide charges extracted from the shift of threshold voltage vary also in different power states. If it stays in ‘OFF’ state, the threshold voltage shifts is about 4-5 V at around 1 Mrad,

For ”ON” state there are relatively more positive oxide charges generated, which is reflected by a large shift of the threshold voltage. The radiation-induced damages can be recovered to a certain extent through RT annealing for a few days direct after irradiation. Since the MOSDEPFET always stays in OFF state during the operation due to the special readout system with only one row active, the radiation damages generated are almost minimal. Moreover, the saturation effect can also be observed from the Figure 6.11 at about 1 Mrad.

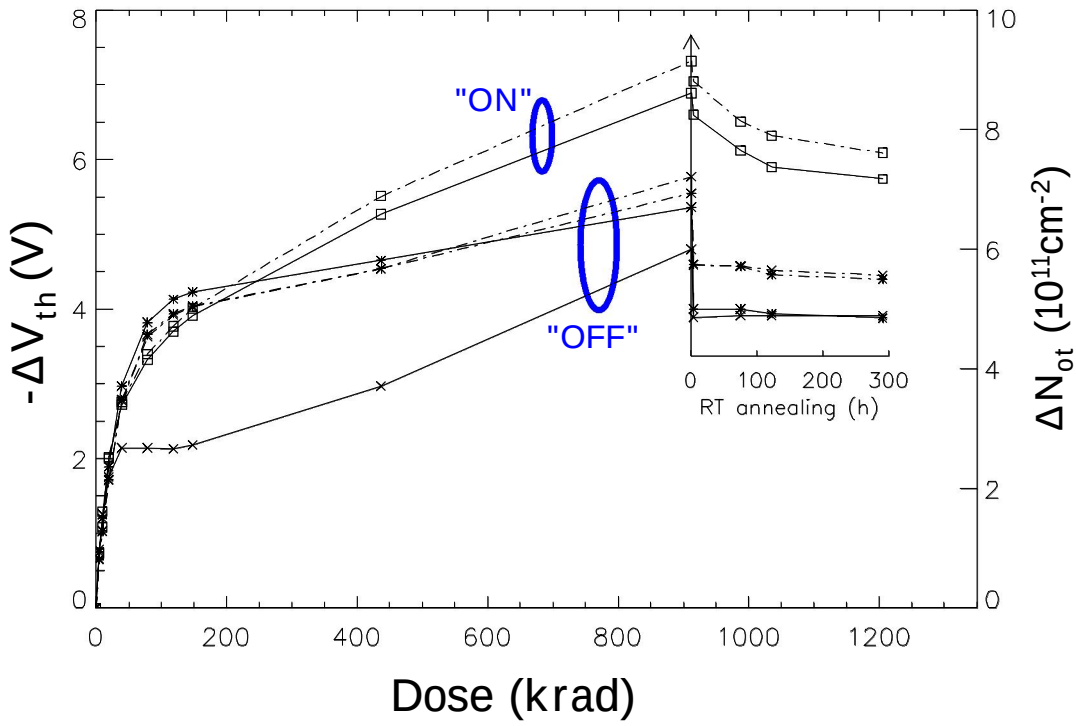


Figure 6.11 Transistor stays in ON or OFF state depending on different biasing applied on the external contact. The radiation induced shift of threshold voltage shows a large value in ON state than in OFF state. Annealing occurs after irradiation during days [2].

MOS gated diode

Unlike the above two MOS devices, the characteristic parameter monitoring the radiation-induced positive oxide charges is the surface generation current (Figure 6.12 and 6.13).

As discussed previously the surface generation current as a function of gate voltage shows a peak at the depletion region mainly due to the interface traps, and it also shifts to a more negative direction that reflects the corresponding positive oxide charges generated in the oxide. This MOS gated diode is irradiated under the same condition as the MOS capacitance in order to compare the extracted experimental results. In addition, surface damages are also experimentally observed through other parameters (surface recombination velocity, capture cross section and lifetime).

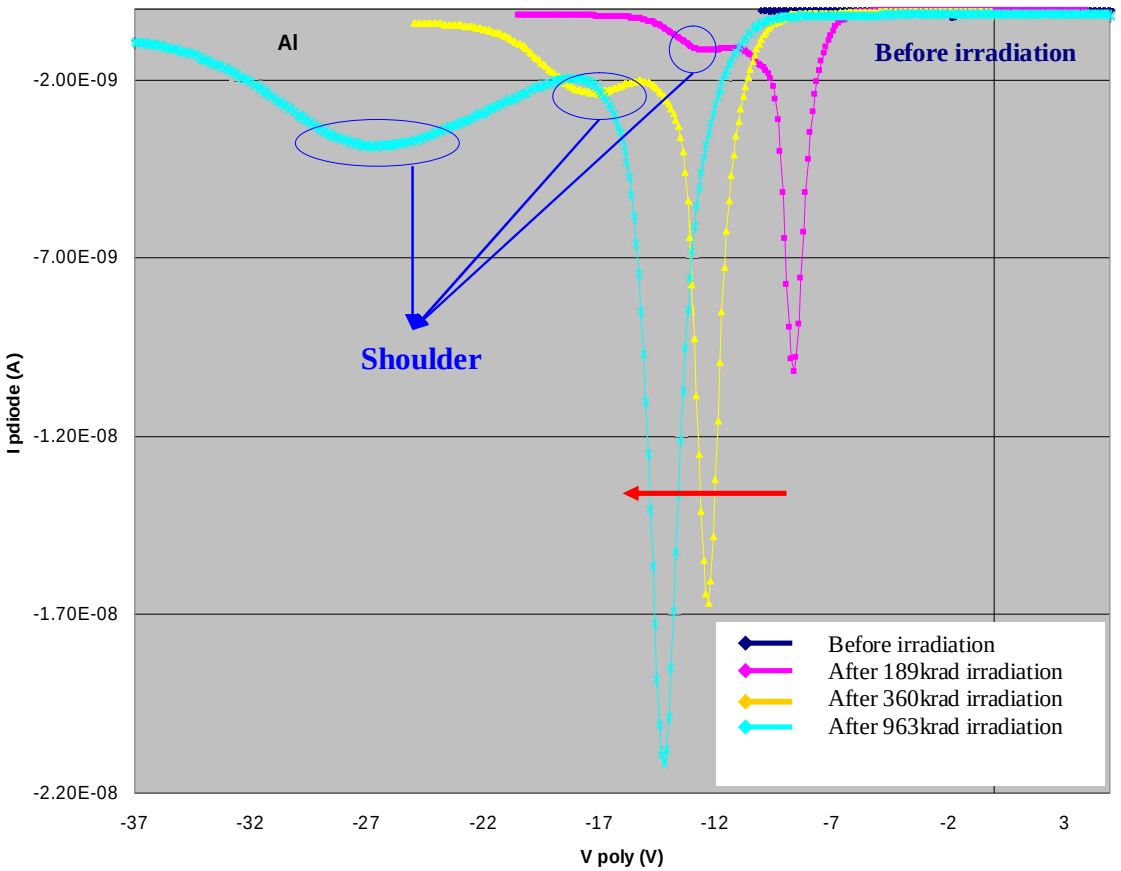


Figure 6.12 Shift of surface generation current for an Al gate structure (type 3) measured using the gated controlled diode technique.

There is a shoulder in the curves of Figure 6.12, which becomes larger and broader with increasing radiation dose, whose occurrence can be explained by a small difference in the layer profile. As shown in Figure 3.8 previously, normally the gate dielectrics (thermal oxide) should overlap the p+ region slightly to prevent a potential barrier. However, there is a small gap between p+ implantation and oxide under the gate that is not defined. For this reason, the measured shift is significantly smaller in the case of Al-gate structure on a MOS capacitance than it is expected. This means one part of radiation induced positive oxide charges for gated diode al-gate structure can not be measured by the information only from the peak of generation current, that is to say, the shoulder also has to be taken into account for the contribution of the positive oxide charges. Comparing Figures 6.5 and 6.14, the results are almost the same for the Poly-gate structure between MOS capacitance and MOS gated diode with respect to the shift value (positive oxide charges).

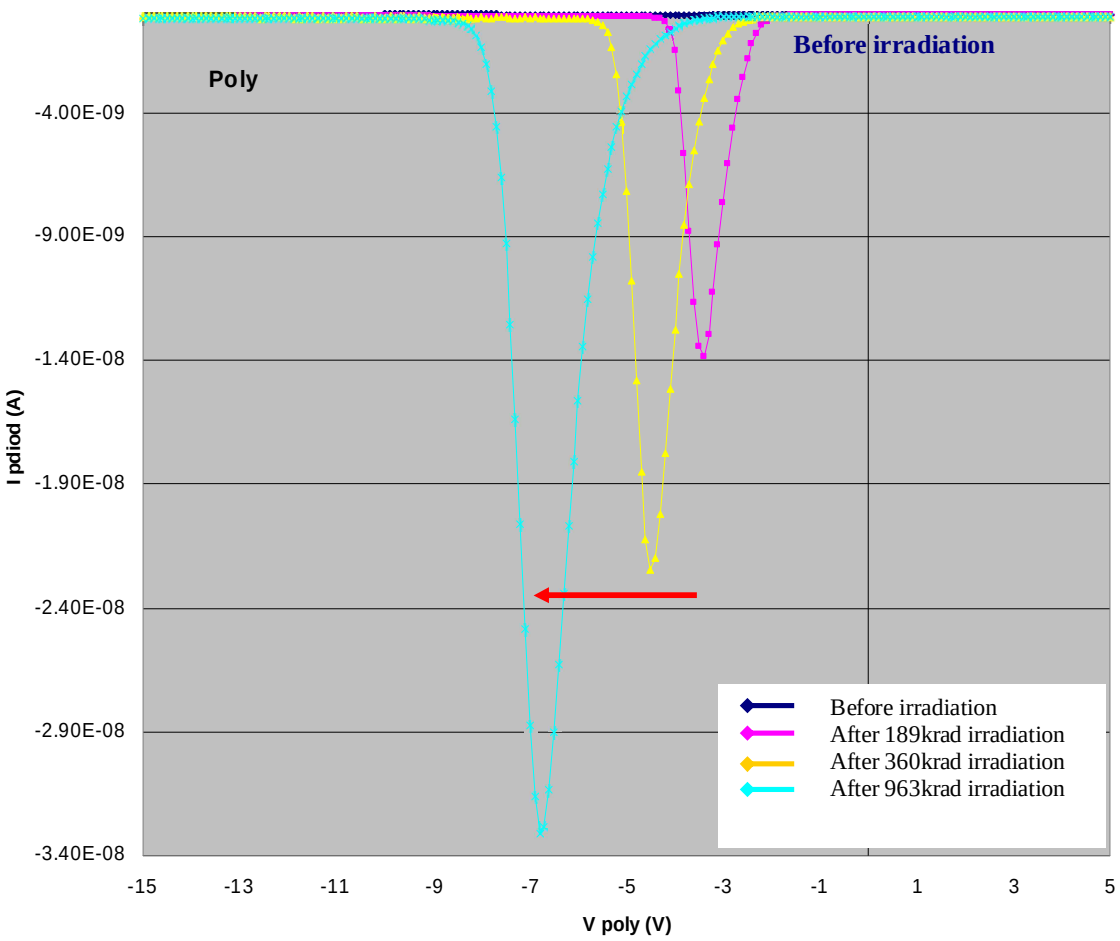


Figure 6.13 Shift of surface generation current for a Poly-gate structure (type 4) measured using gated controlled diode technique.

Interface traps can be extracted from the surface generation current peak as explained in Chapter 3.3. The comparison between MOS capacitance and MOS gated diode has revealed that the calculated interface traps on the Poly-gate structure are reproducible between these two MOS devices, but not for the Al-gate structure as discussed above due to the special profile if only the peak region of the generation current is considered. As shown in Figure 6.14, the damages inclusive positive oxide charges and interface traps begin to show the saturation at about 1 Mrad.

In general, surface damages observed in MOS devices are comparable because they are processed the same way.

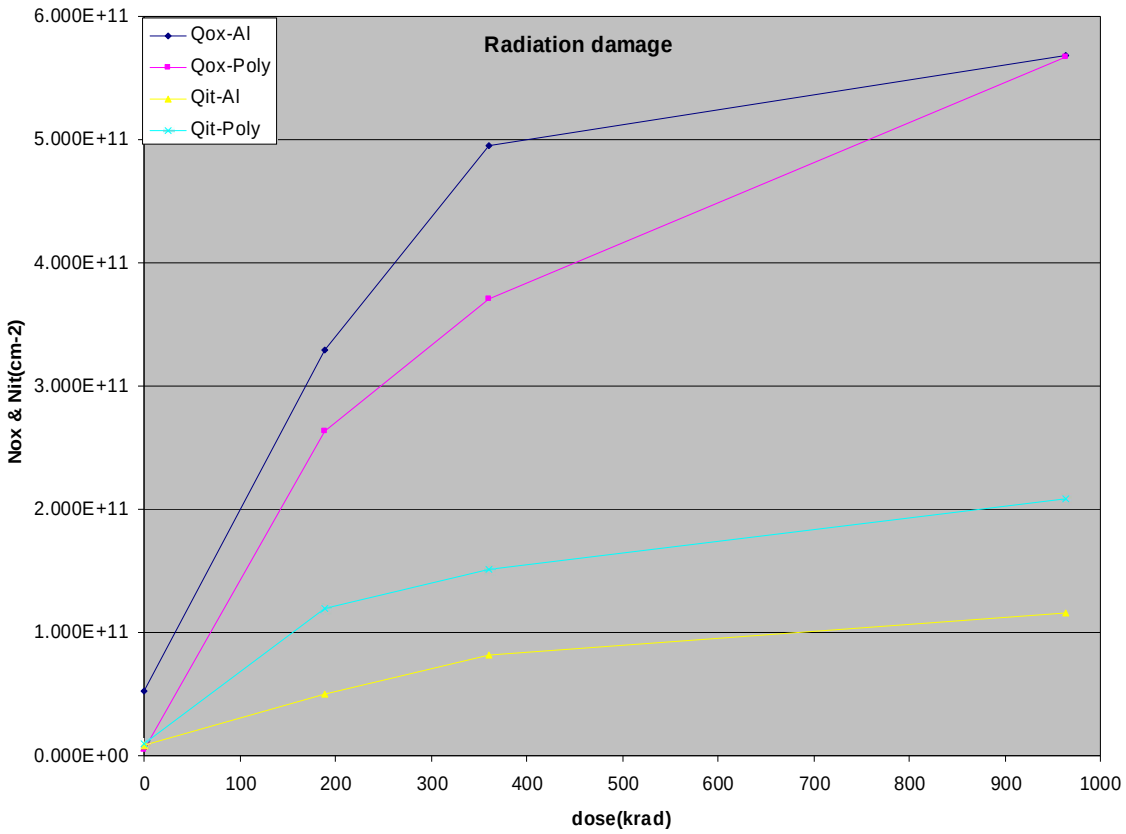


Figure 6.14 Summary of the radiation damage for the MOS gated diode on two-gate structures: Al gate and Poly gate (type 3/4).

6.2 Dose rate

The previous discussion has shown that surface damage is induced due to ionizing radiation and increases with radiation dose. Another important factor will affect the radiation response: dose rate – in order to achieve a given radiation dose (1Mrad). Irradiation time is accordingly different with respect to different dose rate. The following section will concentrate on this subject to see if there is really a dose rate effect.

The samples are irradiated with two radiation dose rates. The experimental setups have already been introduced previously and are shown again below:

- CaliFa setup of Semiconductor Labor in Munich: dose rate is 9 krad/h
- X-ray setup at research center in Karlsruhe: dose rate is 148 krad/h

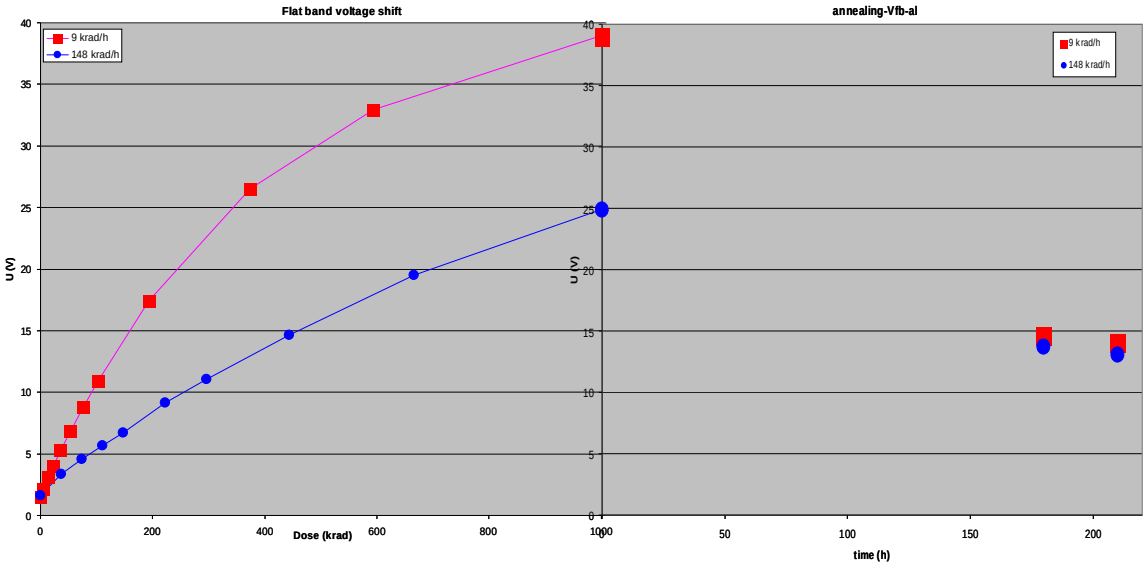


Figure 6.15 Flat band voltage shift due to positive oxide charges as a function of the radiation dose and after irradiation anneal time for MOS capacitances with 180nm thermal oxide plus 300 LTO (type 1), which is irradiated up to a dose of 1 Mrad at two different radiation dose rates (9 krad/h [red] & 148 krad/h [blue]). Irradiation and annealing process are performed at 0V bias.

Samples are irradiated with these two radiation dose rates (Figure 6.15) up to a dose of 1 Mrad, followed by annealing at room temperature for more than a week. During irradiation and annealing the samples are biased with 0V. A larger flat band voltage shift due to positive oxide charges is measured by the high-frequency capacitance voltage method for the lower radiation dose rate direct after irradiation. The red square data points denote the irradiation with a dose rate of 9 krad/h, whereas the blue circles represent a higher dose rate of 148 krad/h. It is suggested that the large increase in shift of flat band voltage might result from

I. A real dependence on the radiation dose rate

II. Additional charge sheet generated in the oxide bulk

In Figure 6.16 the generation and transport of electron-hole pairs under two different radiation environments are shown. In general, at the beginning of the irradiation there are only a few electron-hole pairs generated in the whole oxide bulk. Some fraction of the holes can escape the initial recombination with electrons and stay for a short time (typically at room temperature for seconds) at the place where they are generated. This results in a shift of the measured flat band voltage. Afterwards the holes undergo a stochastic hopping transport through the oxide to the interface in response to electric fields, and then are captured in long-term trapping sites to create the positive oxide charges. Taking into account the time required for generation of holes and transport to the interface region, in the case when the former is faster than the latter – high dose rate (148 krad/h), an additional space charge sheet of holes will be probably formed in the oxide

bulk that prevents from the new coming hole generated between this charge sheet and gate contact, and leads to a reduced generation of surface damages. Contrary, for low dose rate (9 krad/h) no such a positive charge sheet will be formed within the oxide layer, and an enhanced generation of surface damage will take place.

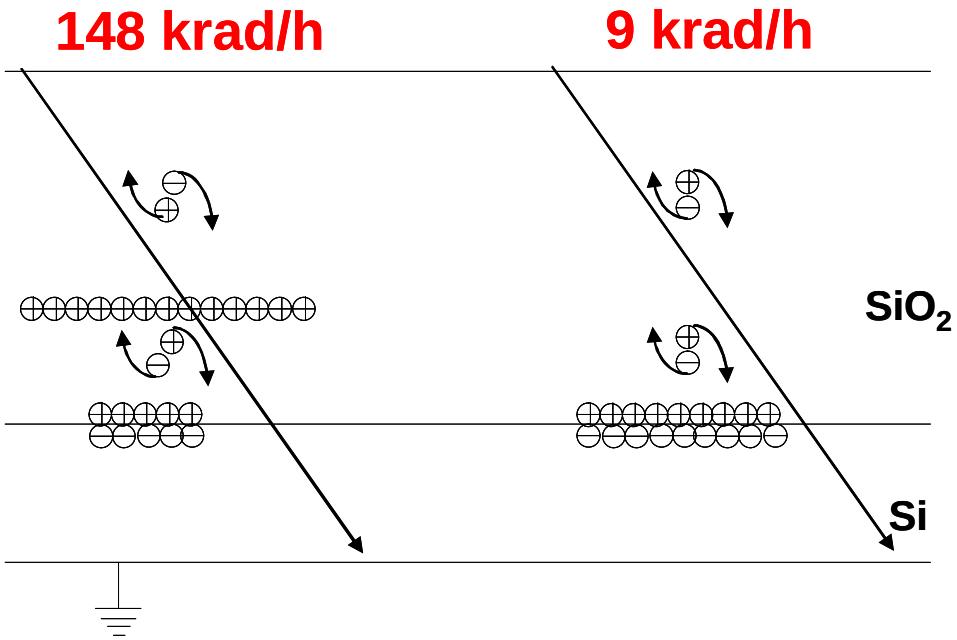


Figure 6.16 Schematic structure for the generation of positive oxide charges with two different radiation dose rates: 148 krad/h & 9 krad/h.

Further examination of such dose-rate effects reveals that the annealing time is not dependent on the dose rate. Furthermore, the end state of surface damages after a certain time period (days typically at room temperature) is almost the same independent of the dose rate. For this reason, there are no real dose-rate effects for the generation of positive oxide charges. For the other part of surface damages – interface traps – one could not find any evidence for dose-rate effects [23]. In short: dose rate effects affect the surface damages only during the irradiation but not for a longer period.

6.3 Bias conditions

In order to study the biasing dependent radiation damages, different gate polarities are applied. Samples are irradiated up to about 1 Mrad. The shift of flat band voltage associated with positive oxide charges extracted from the high-frequency CV measurement shows different results.

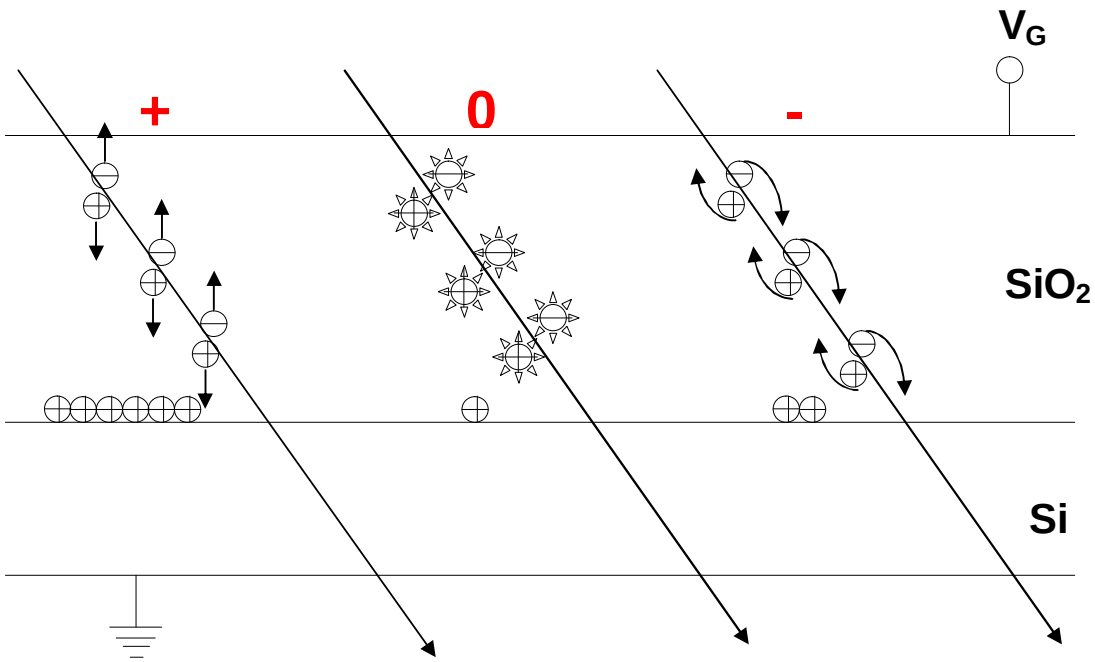


Figure 6.17 Generation of electrons and holes throughout the oxide layer under different gate polarity.

As depicted in Figure 6.17 without any external electric field applied on the gate, electrons and holes generated by ionization are not separated by the electric field and a large fraction of electrons and holes will recombine. Hence, the number of positive oxide charges trapped at the interface reaches its minimum compared with other gate polarities.

If an external voltage is applied on the gate, the generated electron-hole pairs will be separated under the influence of the electric field and drift in the corresponding direction. As a consequence, the recombination effect is not relevant. Assuming that the hole traps (precursors) responsible for the hole trapping are mainly distributed at the interface Si/O, the positive oxide charges measured under positive gate polarity is dominant higher than in the case of negative gate polarity.

As discussed previously, according to the Dimaria model the calculated concentration of positive oxide charges is given by Equation 4.9. This factor α can be defined as the product of an electric-field-dependent capture cross section of traps and recombination of electrons with trapped holes and the hole fluency that depends on the oxide thickness and also the electric field:

$$\alpha = (\sigma_r + \sigma_{ht}) f_h \tag{6.8}$$

In the case of positive gate voltages (Figure 6.18), i.e., $E_{ox} > 0$: the recombination effect is not so dominant. For this reason, the cross section for recombination of electrons with holes is significantly smaller than that of hole trapping:

$$\sigma_{ht} >> \sigma_r \tag{6.9}$$

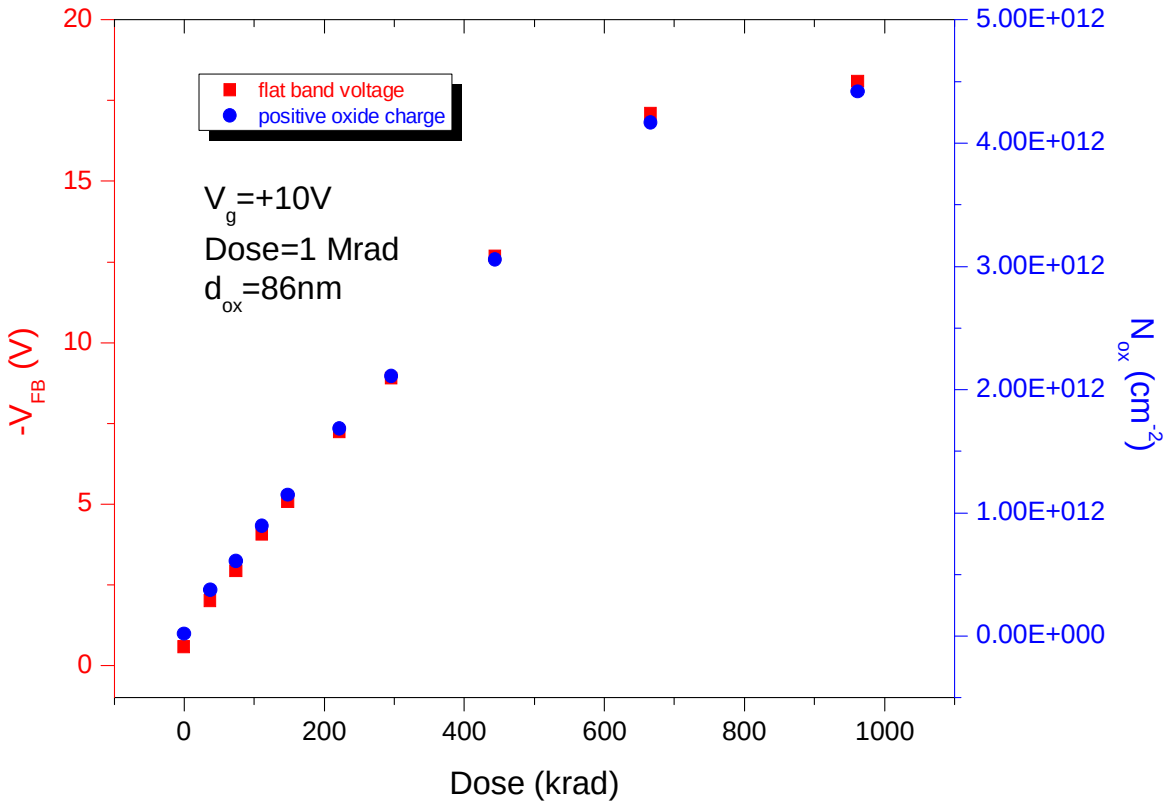


Figure 6.18 Shift of flat band voltage & positive oxide charges concentration as a function of radiation dose for MOS capacitance with 86 nm thermal oxide (type 5) to a dose of 1 Mrad (SiO_2) at gate voltage of +10V.

Consequently, the trapped hole density is given by:

$$n_{ht}^{+}(D \sim D_{sat}) = n_{ht}(D=0) + N_{ht}^{+}\left(1 - e^{-\alpha^{+} D}\right) \tag{6.10}$$

Where the factor α in this case is $\alpha^{+} \approx \sigma_{ht} f_h^{+}$, since the recombination effect does not play a role.

The red data points denote the flat band voltage for the MOS capacitance with 86 nm thermal oxide, which is irradiated up to about 1 Mrad under a gate voltage of +10V. The blue one represents the corresponding concentration of positive oxide charges.

For the reverse polarity at the gate contact (Figure 6.19), i.e., $E_{ox} < 0$: the factor α should be defined in the same manner as positive polarity $\alpha^{-} \approx \sigma_{ht} f_h^{-}$. Therefore, the trapped hole density is given as:

$$n_{ht}^{-}(D \sim D_{sat}) = n_{ht}(D=0) + N_{ht}^{-}\left(1 - e^{-\alpha^{-} D}\right) \qquad (6.11)$$

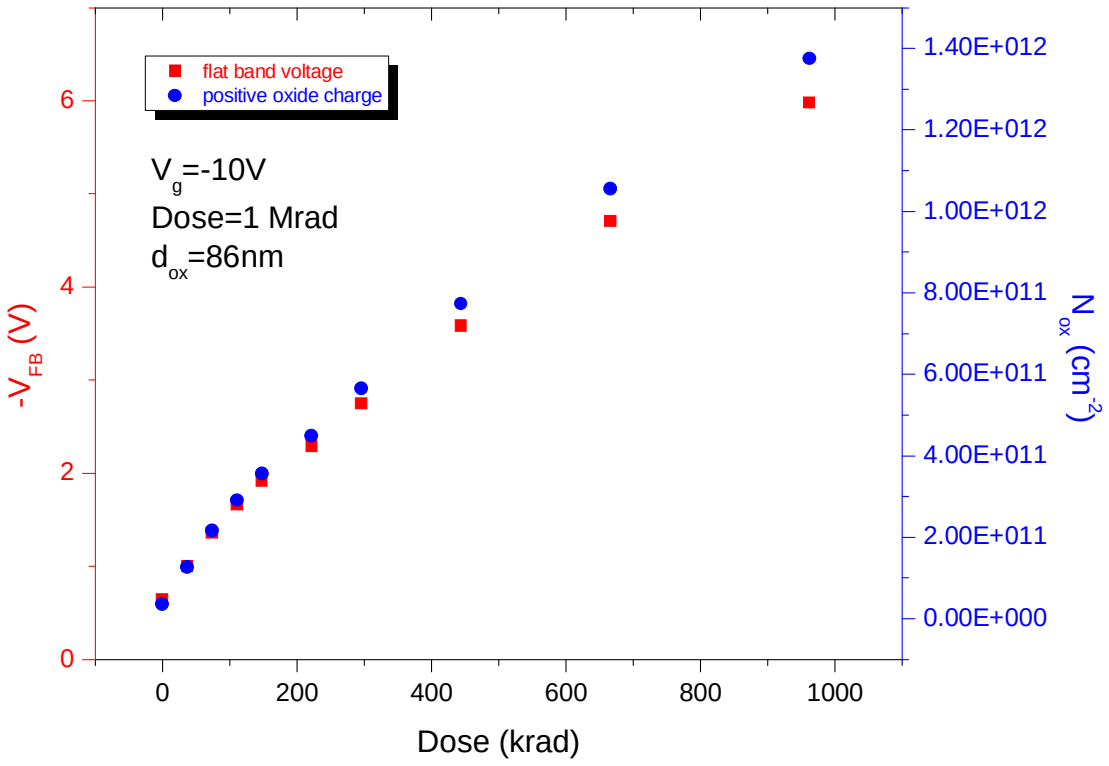


Figure 6.19 Shift of flat band voltage & positive oxide charges concentration as a function of radiation dose for MOS capacitance with 86 nm thermal oxide (type 5) to a dose of 1 Mrad (SiO_2) at gate voltage of -10V.

For $E_{ox} = 0$ (Figure 6.20): the recombination effect can not be neglected as discussed above, and $n_{ht}(t)$ is present with $\alpha^{0} \approx (\sigma_{ht} + \sigma_r) f_h^{0}$:

$$n_{ht}^{0}(D \sim D_{sat}) = n_{ht}(D=0) + \frac{\sigma_{ht}}{\sigma_r + \sigma_{ht}} N_{ht}^{0}\left(1 - e^{-\alpha^{0} D}\right) \qquad (6.12)$$

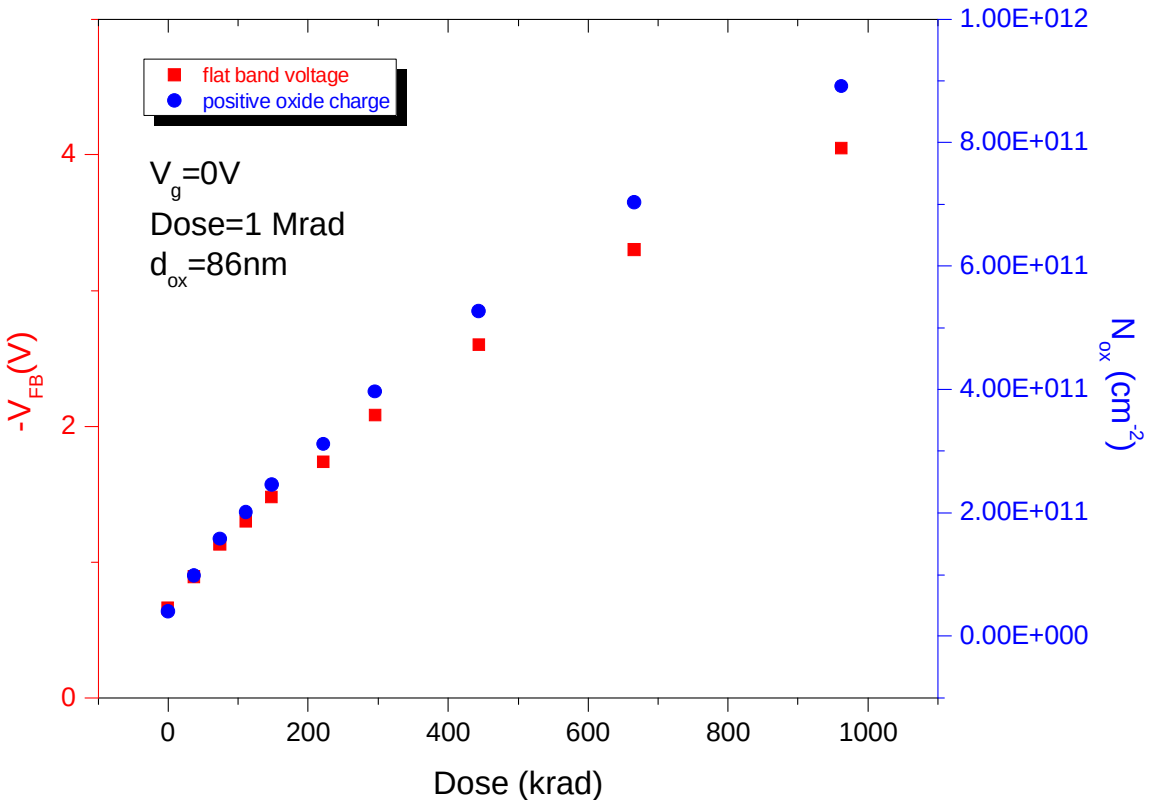


Figure 6.20 Shift of flat band voltage & positive oxide charges concentration as a function of radiation dose for MOS capacitance with 86 nm thermal oxide (type 5) to a dose of 1 Mrad (SiO_2) at zero gate voltage.

As mentioned above, the hole traps are mainly distributed at the interface Si/O; on the other hand, the recombination effect is enhanced at zero electric field, consequently the measured shift of flat band voltage at saturation associated with positive oxide charges can be written as follows:

$$n_{ht}^{+}\left(D \sim D_{sat}\right) > n_{ht}^{-}\left(D \sim D_{sat}\right) > n_{ht}^{0}\left(D \sim D_{sat}\right) \qquad (6.13)$$

As shown in Figure 6.21, the data points characterize the electric-field-dependent flat band voltage shift and positive oxide charges concentration.

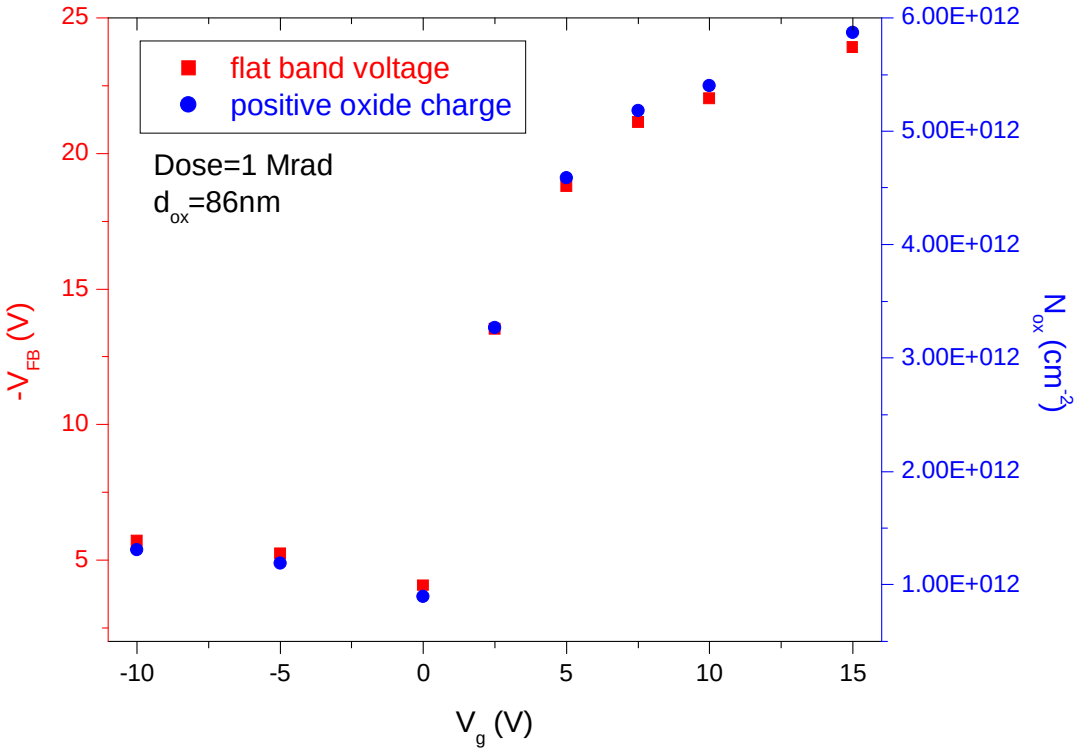


Figure 6.21 Shift of flat band voltage & positive oxide charges concentration as a function of the applied gate voltage for MOS capacitance with 86 nm thermal oxide (type 5) to a dose of 1 Mrad (SiO_2).

6.4 Oxide thickness

In general, surface damages vary with different oxide thicknesses for MOS devices. In order to measure this dependence — d_{ox}^{n} — one has to take into account Equation 4.6. This oxide thickness dependency can change with different gate polarity.

In the case of a positive gate voltage, Equation 4.6 can be simplified under the following three assumptions:

- The local hole trap density $N_{ht}(x)$ is homogeneously distributed in a certain distance Δx, which is assumed to be near the interface Si/O $\Delta x << d_{ox} : N_{ht}(x) \approx \overline{N_{ht}(\Delta x)}$ (homogeneous)

- The electron-hole pairs are generated homogeneously throughout the oxide bulk and are separated under the influence of the electric field; the induced holes can be swept to the Si/SiO_2 interface (positive gate voltage).

- The recombination effect of electrons with trapped holes can be neglected, the capture process is strong than the recombination process: $\sigma_{ht} >> \sigma_r$ & $n_{ht} << \overline{N_{ht}}$ (n_{ht}: trapped holes; $\overline{N_{ht}}$: hole traps)

    - The fraction of the trapped holes in the oxide is given by the product of capture cross section σ_{ht} and density of hole traps in the interface region $\overline{N_{ht}(\Delta x)}$

$$f_T = \sigma_{ht} \overline{N_{ht}(\Delta x)} \tag{6.14}$$

    - The hole fluence passing through the hole traps is generally equal to the number of the generated holes throughout the oxide bulk:

$$f_h = d_{ox} N(E, E_{ox}, D) \tag{6.15}$$

The hole fluence depends on the oxide thickness d_{ox} and radiation-induced charge carriers $N(E, E_{ox}, D)$ that depend on the radiation energy E, electric field E_{ox} and radiation dose D.

Derived from equation 3.2, 6.14 und 6.15 positive oxide charges concentration is given by:

$$\Delta N_{ox} = \frac{1}{d_{ox}} \int_0^{d_{ox}} n_{ht}(x) x dx = f_h f_T \tag{6.16}$$

Combining equations 3.1 and 6.16 the oxide thickness dependency is as following:

$$\Delta V_{ox} = -\frac{q}{\varepsilon_0 \varepsilon_{SiO_2}} d_{ox} \Delta N_{ox} = -\frac{q}{\varepsilon_0 \varepsilon_{SiO_2}} N(E, E_{ox}, D) f_T d_{ox}^2 \tag{6.17}$$

The exponential value of the oxide thickness dependency d_{ox}^n can be determined to 1.7~1.9, which is very close to the theoretical square dependency of the oxide thickness (Figure 6.22).

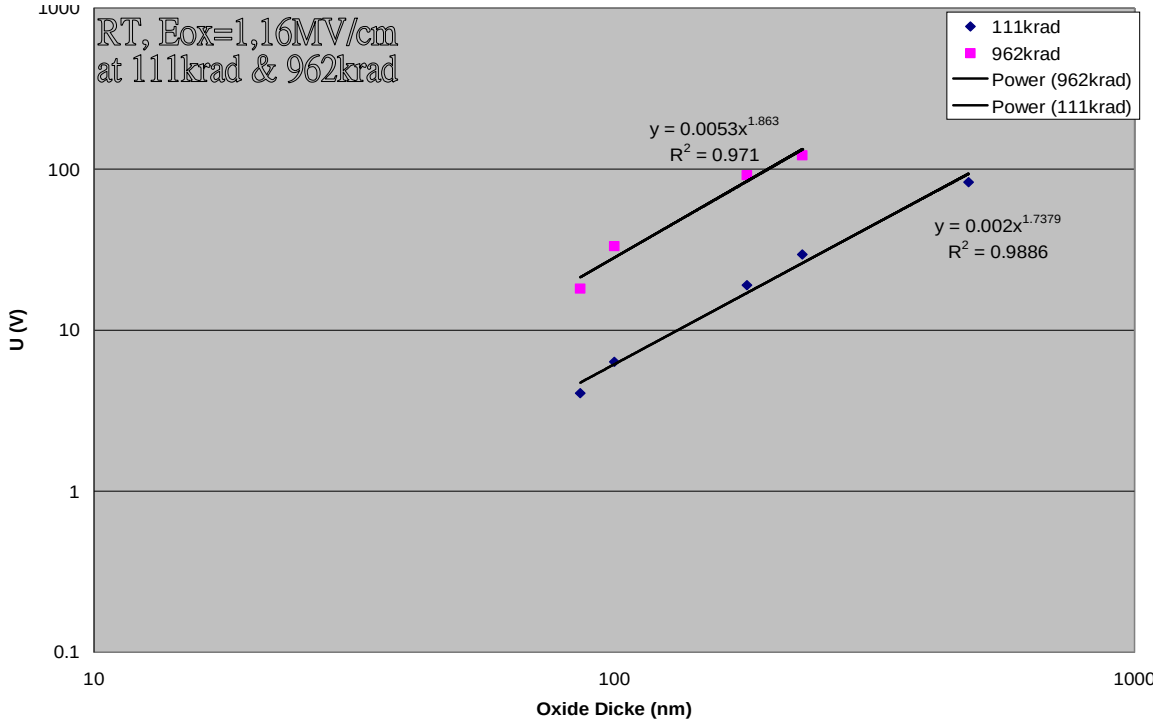


Figure 6.22 Oxide thickness dependency d_{ox}^{n}, n is calculated at about 1.7 to 1.9 under positive gate voltage for MOS capacitances with different oxide thickness with irradiation by two different doses (111krad and 962krad). Power (962krad) and power (111krad) are fitting results.

In the case of zero voltage applied on the gate, the above three assumptions must be somehow modified and can be simplified (Figure 6.23):

- The local hole trap density $N_{ht}(x)$ is homogeneously distributed in a certain distance Δx, which is assumed near the interface region $\Delta x << d_{ox} : N_{ht}(x) \approx \overline{N_{ht}(\Delta x)}$

- The electron-hole pairs are homogeneously generated throughout the oxide bulk and afterwards just stay at the place where they are generated.

- The recombination effect cannot be neglected, the hole capture process takes place more weakly than in the case of non-zero gate voltage, the trapped holes are much more lower than the hole traps (precursors): $n_{ht} << \overline{N_{ht}}$

    - The trapped holes in the oxide are given below, the second term of the below formula arises from the recombination effect of electrons with trapped holes:

$$f_T = \sigma_{ht} \overline{N_{ht}} \Delta x - \sigma_r n_{ht} \Delta x \qquad (6.18)$$

- The hole fluence passes through the hole traps is generally only equal to the number of generated holes near the interface region due to ionizing radiation:

$$f_h = \Delta x N(E, E_{ox}, D) \tag{6.19}$$

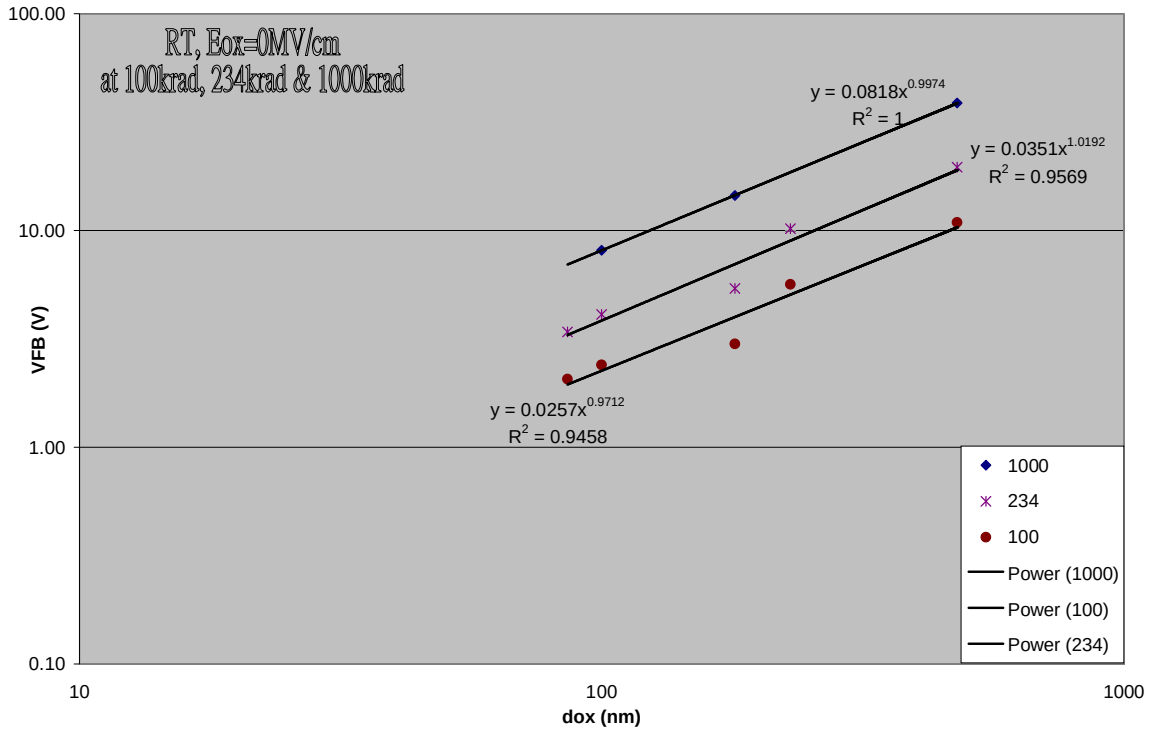


Figure 6.23 Oxide thickness dependence d_{ox}^{n}, n calculated at about 1 under zero gate voltage for MOS capacitances with different oxide thickness and irradiation by two different doses (111krad and 962krad). Power (1000), power (234) and power (100) are fitting results.

As calculated above, combining the equations 3.1, 6.18 and 6.19 the oxide thickness dependence can be formulated as:

$$\Delta V_{ox} = -\frac{q}{\varepsilon_0 \varepsilon_{SiO_2}} d_{ox} \Delta N_{ox} = -\frac{q}{\varepsilon_0 \varepsilon_{SiO_2}} N(E, E_{ox}, D) f_T \Delta x d_{ox} \tag{6.20}$$

Since N_{ox} is proportional to the oxide thickness and total dose, it can be given as:

$$\Delta N_{ox} \propto d_{ox}^{b} \tag{6.21}$$

Where b is sub-linear proportional value, which can be calculated from the flat band voltage shifts ΔV_{FB} in MOS capacitors with three different oxide thicknesses (Figure 6.24).

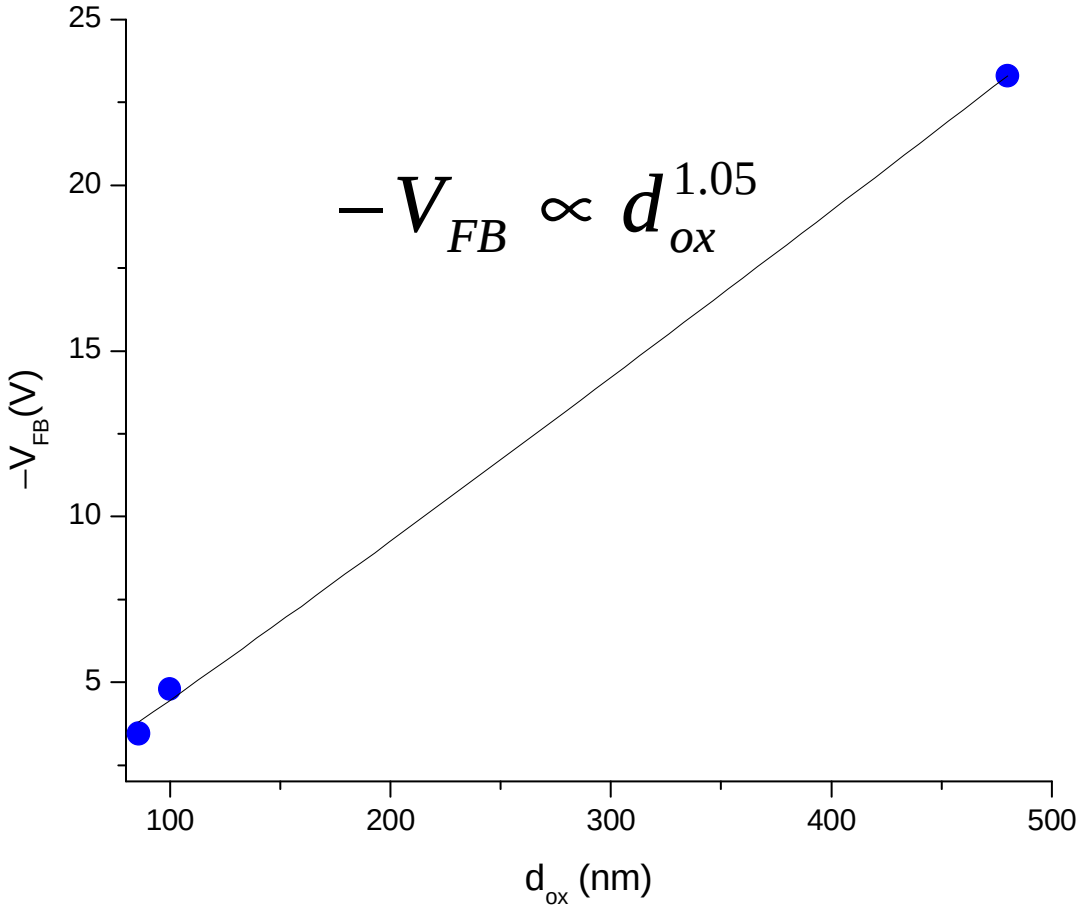


Figure 6.24. Flat band voltage shift of a MOS capacitor as a function of three different oxide thicknesses at about 1Mrad (SiO_2). Bias during irradiation is 0V.

The small value of $b \approx 0.05$ indicates that the number of holes trapped at the Si/O interface depends more weakly on the oxide thickness in case of zero gate bias condition.

From 6.20 and 6.21, the flat band voltage shift of a MOS capacitor can be expressed as:

$$\Delta V_{FB} = -0.03\, d_{ox}^{1.05} \qquad (6.22)$$

6.5 Nitride layer

It is of major importance that the radiation hardness has been improved for an MNOS structure in comparison with a MOS structure of the same oxide thickness. The composite dielectrics can be produced by adding an additional insulator layer namely nitride over the SiO_2. The advantage of nitride is that it has a relative higher dielectric constant than that of the SiO_2. The charge trapping under ionizing radiation will be studied in the following section by the flat band voltage shift using a simple charge trap model.

Firstly, in order to investigate the effect of ionizing radiation in silicon nitride/SiO_2 (N/O) of an MNOS structure, a large amount of irradiation experiments have already been performed. It has been suggested that the N/O combined dielectrics films are less sensitive to ionizing radiation than pure oxide films with the same oxide thickness, whereas only holes can significantly be trapped in the oxide layer and electron trapping can be neglected in SiO_2 due to a smaller capture cross section. The charge storage properties can be described by the charge trapping effect in the dual dielectric structures that has already received a lot of attention since MNOS structures have found their application in nonvolatile memories. Based on charge generation and trapping in the dielectrics a model associated with flat band voltage shift has also been designed to demonstrate the improved radiation hardness (minimization of flat band voltage shift due to ionizing radiation) through this additional nitride layer [55].

In Figure 6.25, an energy band diagram for an MNOS and a MOS structure before irradiation without any external gate voltage is shown. Oxide quality in the bulk oxide and SiO_2/Si interface should theoretically be the same for MOS and MNOS structures. However, experimental results show a more negative flat band voltage for an MNOS structure than that of a MOS structure. Accordingly, this reveals that there are effective positive charges trapped in the interface between nitride and oxide. The MOS structure produced by using modern silicon technology in the semiconductor laboratory has a positive oxide charges concentration of around 10^{10} cm^{-2} before ionizing radiation, while that of MNOS is in the order of 10^{12} cm^{-2}. As discussed previously, the charge trap densities (here mainly hole trapping for MOS) are spatially extended from Si/O interface into oxide bulk of a few nanometers. However, MOS structures exhibit a lower trap density than MNOS structures, since there are more defects at N/O interface for an MNOS than a MOS structure.

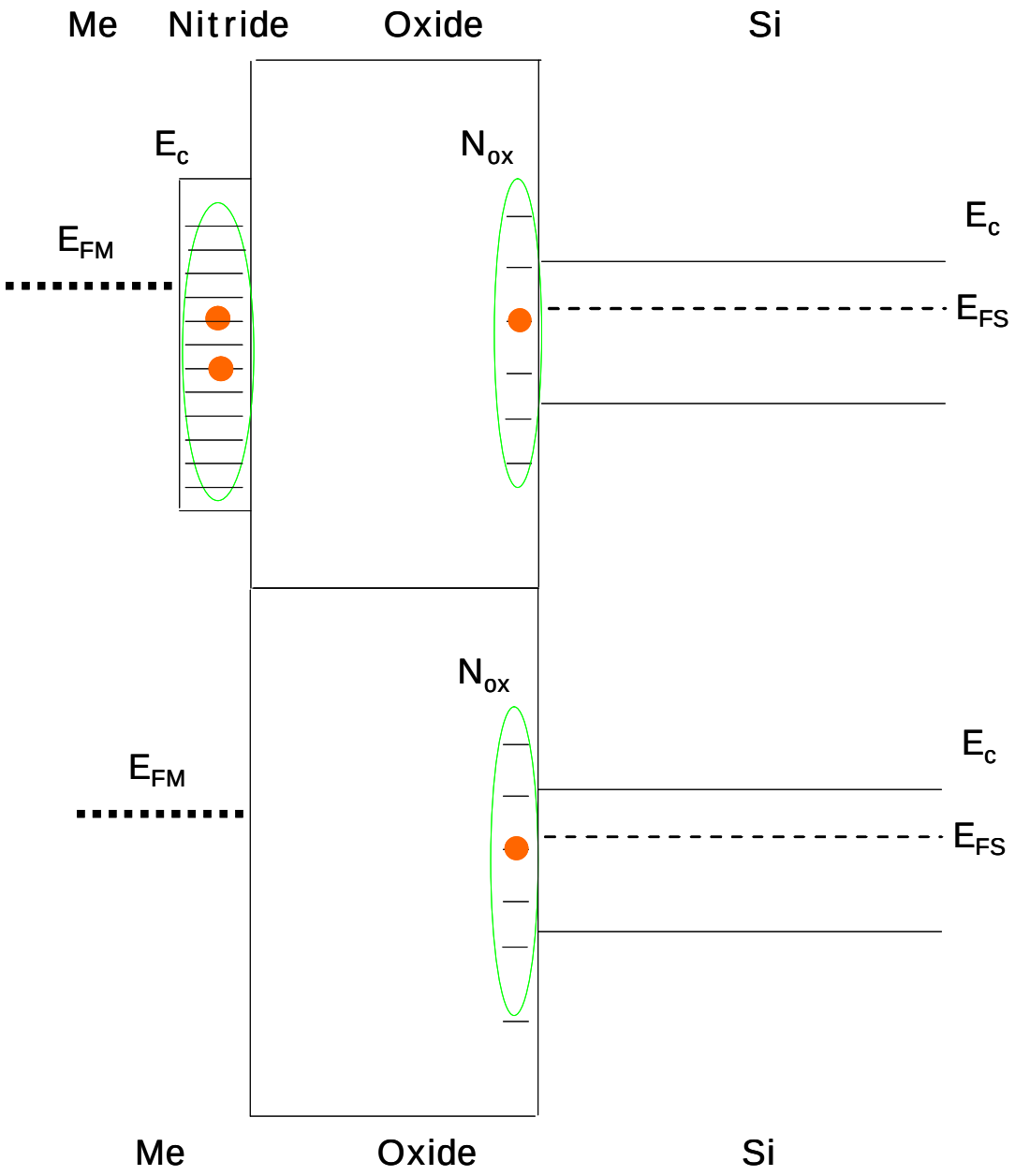


Figure 6.25 Energy band diagram for MNOS and MOS structure before irradiation. The initial state of surface damage is depicted at the interface between N/O and Si/O. E_{FM} is Fermi level of metal, E_C is the conduction band, E_{FS} is Fermi level of silicon, N_{ox} is the trapped carriers in the oxide.

During ionizing radiation, electron-hole pairs are generated throughout both dielectrics layers. Under the influence of an electric field in an MNOS structure, some of the electron-hole pairs that can escape the initial recombination will be transported to the corresponding directions and be captured in the layers. The trapped charges in the nitride layer can be considered as a sheet charge with an effective area charge density of N_{ni}

projected to the N/O interface. It is the same as the trapped charges in the oxide layer, which can also be represented as a sheet charge with an effective areal charge density of N_{ox} projected to the Si/O interface. For this reason, the flat band voltage shift due to the trapped charges in the combined nitride oxide dielectrics layers can be formulated as:

$$V_{MNOS} = \phi_{ms} / q - \frac{Q_{ox0}}{C_{eq,ox}} - \frac{Q_{ox}}{C_{eq,ox}} - \frac{Q_{ni}}{C_{ni}} \tag{6.23}$$

Where the effective capacitance $C_{eq,ox}$ is a series combination of the oxide capacitance C_{ox} and the nitride capacitance C_{ni} with an effective oxide thickness $d_{eq,ox}$:

$$C_{eq,ox} = \frac{\varepsilon_{ox}}{d_{eq,ox}} A \tag{6.24}$$

$$d_{eq,ox} = d_{ni} \frac{\varepsilon_{ox}}{\varepsilon_{ni}} + d_{ox} \tag{6.25}$$

For positive-bias irradiation (shown in Figure 6.26 left), the holes generated in the oxide layer will drift towards the Si/O interface. The electrons generated in the oxide layer are swept to the nitride layer easily since no electron barrier exists at the nitride oxide interface. Due to the large density and capture cross section of both electron and hole traps in the nitride layer, a significant part of the electron-hole pairs generated in the nitride will be trapped near their generation sites. However, some of the holes generated in the nitride layer will move to the nitride oxide interface and accumulate there since there is a hole barrier at the interface [55]. Some of them will recombine with the electrons from the oxide and some of them will be captured by the traps at the interface.

In this case, the charge of N_{ox} is mostly due to hole trapping at the oxide silicon interface. In contrast to this, the negative charges due to the electrons from the oxide layer and the positive charges due to the holes from the nitride compete to determine both the magnitude and the sign of N_{ni}. The effective charged carriers in the nitride of an MNOS structure are electrons in this thesis.

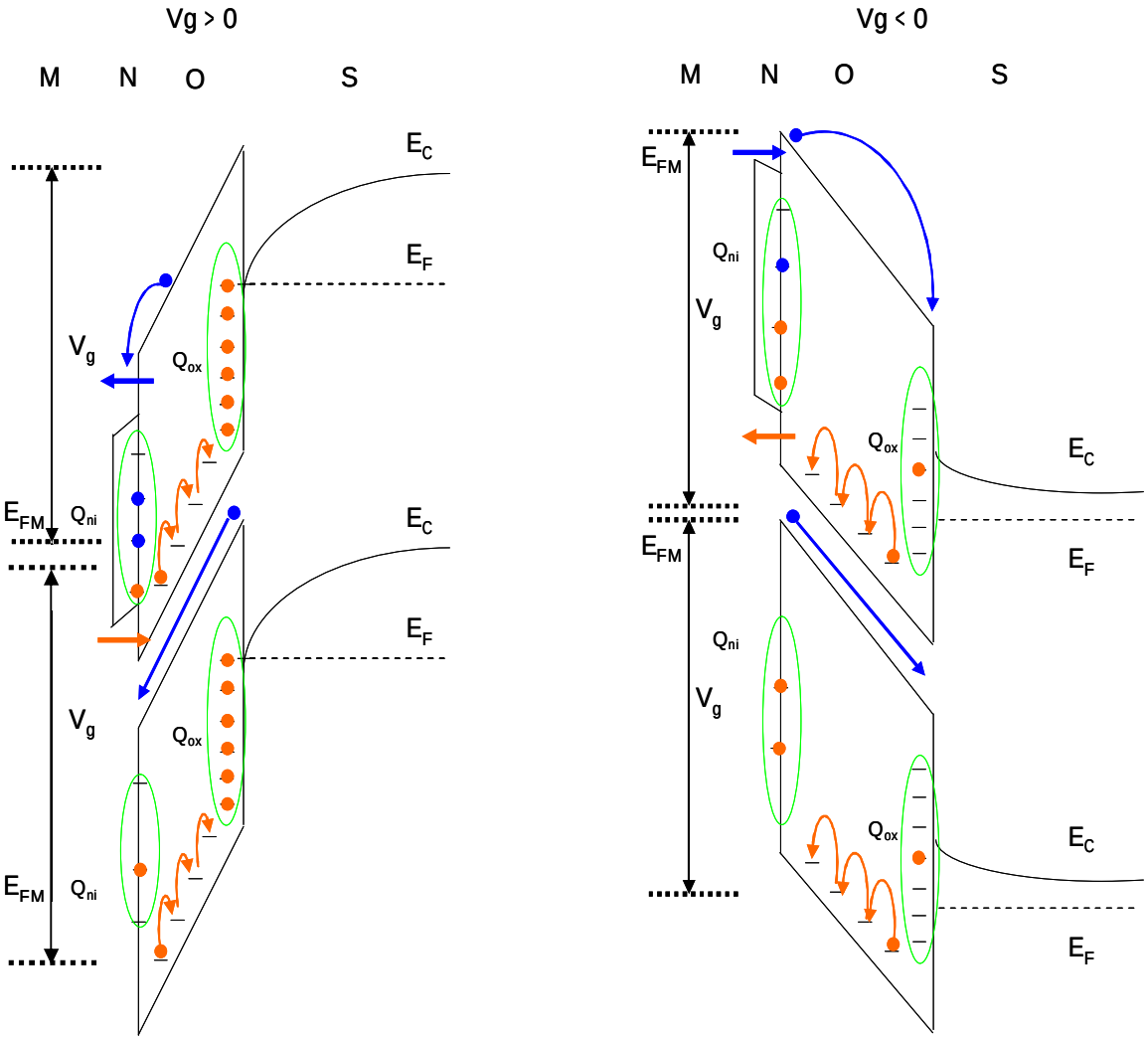


Figure 6.26 Energy band diagram for MNOS and MOS structure with different gate polarity: Positive gate voltage (left) and negative gate voltage (right). Damage generation process of surface damage take places in the interface region. E_C and E_F are the conduction band and Fermi level of silicon, E_{FM} is the Fermi level of metal. Nox and Nni are trapped carriers in the oxide and nitride, V_g is the gate voltage.

The total number of holes generated in the oxide that escape initial recombination is mainly proportional to the oxide thickness d_{ox} and free charge yield f_y and charge generation constant K_g that have been discussed previously (equations 6.1 and 6.2). Based on this, it is assumed that an increment of charge ΔN_{ox} generated per unit dose is proportional to the hole fluence (f_h) incident on the hole traps, the effective cross section of hole traps (σ_{ht}) and unoccupied hole trap densities $\left[\overline{N_{ox,h}(x)} - N_{ox,h}(x)\right]$, where the first two terms are electric field dependent.

$$\Delta N_{ox}(x,\Delta D) = f_{ox,h}(d_{ox},E_{ox})\times\sigma_{ox,h}(E_{ox})\times\left[\overline{N_{ox,h}(x)}-N_{ox,h}(x)\right]$$
$$= \left[A(d_{ox},D)\times\gamma(E)\times f_y(E_{ox})\right]\times\sigma_{ox,h}(E_{ox})\times\left[\overline{N_{ox,h}(x)}-N_{ox,h}(x)\right] \quad (6.26)$$

Where the electric field in the oxide E_{ox} should be calculated as:

$$E_{ox} = \frac{V_{ox}}{d_{ox}} = \frac{V_g}{d_{eq,ox}} = \frac{V_g}{d_{ni}\frac{\varepsilon_{ox}}{\varepsilon_{ni}} + d_{ox}} \quad (6.27)$$

According to Equation 6.5 the flat band voltage shift due to hole trapping in the oxide is given:

$$\Delta V_{FB}(MNOS) = -\frac{N_{ox}}{C_{eff.,ox}} = -\frac{\overline{N_{ox,h}}}{C_{eff.,ox}}\left[1-\exp(-\sigma_{ox,h}f_{ox,h}D)\right] \quad (6.28)$$

The charge N_{ni} in the nitride layer can be separated into two components:

- Negative component due to electron trapping $N_{ni,e}$
- Positive component due to hole trapping $N_{ni,h}$

$$\Delta N_{ni}(x,\Delta D) = \Delta N_{ni,e} + \Delta N_{ni,h} \quad (6.29)$$

In the case of a positive gate voltage, most electrons trapped at the nitride oxide interface arise from the oxide layer. Consequently, $N_{ni,e}$ is mainly determined by the electrons generated in the oxide and will be expressed in the same way as N_{ox}:

$$\Delta N_{ni,e}(x,\Delta D) = f_{ox,e}(d_{ox},E_{ox})\times\sigma_{ni,e}(E_{ni})\times\left[\overline{N_{ni,e}(x)}-N_{ni,e}(x)\right]$$
$$= \left[A(d_{ox},D)\times\gamma(E)\times f_y(E_{ox})\right]\times\sigma_{ni,e}(E_{ni})\times\left[\overline{N_{ni,e}(x)}-N_{ni,e}(x)\right] \quad (6.30)$$

Where E_{ni} is electric field in the nitride layer which is defined as:

$$E_{ni} = \frac{V_g}{d_{eq,ni}} = \frac{V_{ni}}{d_{ni}} \quad (6.31)$$

The positive component $N_{ni,h}$ is mainly due to the holes generated in the nitride layer and trapped at the nitride oxide interface. Within the scope of this thesis the nitride layer

thickness is 10nm, which is comparable with the scale of the distribution of charge traps in the nitride (~10nm).

$$\begin{aligned}\Delta N_{ni,h}(x,\Delta D) &= f_{ni,h}(d_{ni},E_{ni})\times\sigma_{ni,h}(E_{ni})\times\left[\overline{N_{ni,h}(x)}-N_{ni,h}(x)\right]\\ &= \left[A(d_{ni},D)\times\gamma(E)\times f_y(E_{ni})\right]\times\sigma_{ni,h}(E_{ni})\times\left[\overline{N_{ni,h}(x)}-N_{ni,h}(x)\right]\end{aligned} \tag{6.32}$$

For simplification, an effective charge trapping in the nitride as well as nitride oxide interface can be expressed as:

$$\begin{aligned}\Delta N_{ni,eff.}(x,\Delta D) &= \left(-f_{ox,e}\times\sigma_{ni,e}(E_{ni})+f_{ni,h}\times\sigma_{ni,h}(E_{ni})\right)\times\left(\overline{N_{ni}(x)}-N_{ni,eff.}(x)\right)\\ &= f_{ni,eff.}\times\sigma_{ni,eff.}\times\left(\overline{N_{ni}(x)}-N_{ni,eff.}(x)\right)\end{aligned} \tag{6.33}$$

Combining and solving Equations 6.30 and 6.32, the flat band voltage shift due to charge trapping in the nitride is given as:

$$\Delta V_{FB}(MNOS) = -\frac{N_{ni,eff.}}{C_{ni}} = -\frac{\overline{N_{ni,eff.}}}{C_{ni}}\left[1-\exp(-\sigma_{ni,eff.}f_{ni,eff.}D)\right] \tag{6.34}$$

Where $N_{ni,eff.}/C_{ni}$ >0 denotes that the effective trapped charge is a hole, and $N_{ni,eff.}/C_{ni}$ <0 for electron trapping.

Taking into account all of the charge trapping in the dielectrics of an MNOS structure after irradiation, the flat band voltage shift can be determined:

$$\begin{aligned}\Delta V_{FB}(MNOS) = -\left(\frac{N_{ox}}{C_{eff.,ox}}+\frac{N_{ni}}{C_{ni}}\right) = -\Bigg\{&\frac{\overline{N_{ox,h}}}{C_{eff.,ox}}\left[1-\exp(-\sigma_{ox,h}f_{ox,h}D)\right]+\\ &\frac{\overline{N_{ni,eff.}}}{C_{ni}}\left[1-\exp(-\sigma_{ni,eff.}f_{ni,eff.}D)\right]\Bigg\}\end{aligned} \tag{6.35}$$

Figure 6.26 (right) shows a negative-bias irradiation. The holes generated in the oxide will move towards the N/O interface instead of Si/O interface (positive gate voltage) and be trapped there, while electrons generated in the nitride will move towards the N/O interface. A part of them will be trapped directly at the N/O interface, and the other will go further into the oxide and can recombine with the trapped hole. An expression for the flat band voltage shift can be derived in a similar way to that at positive gate voltage.

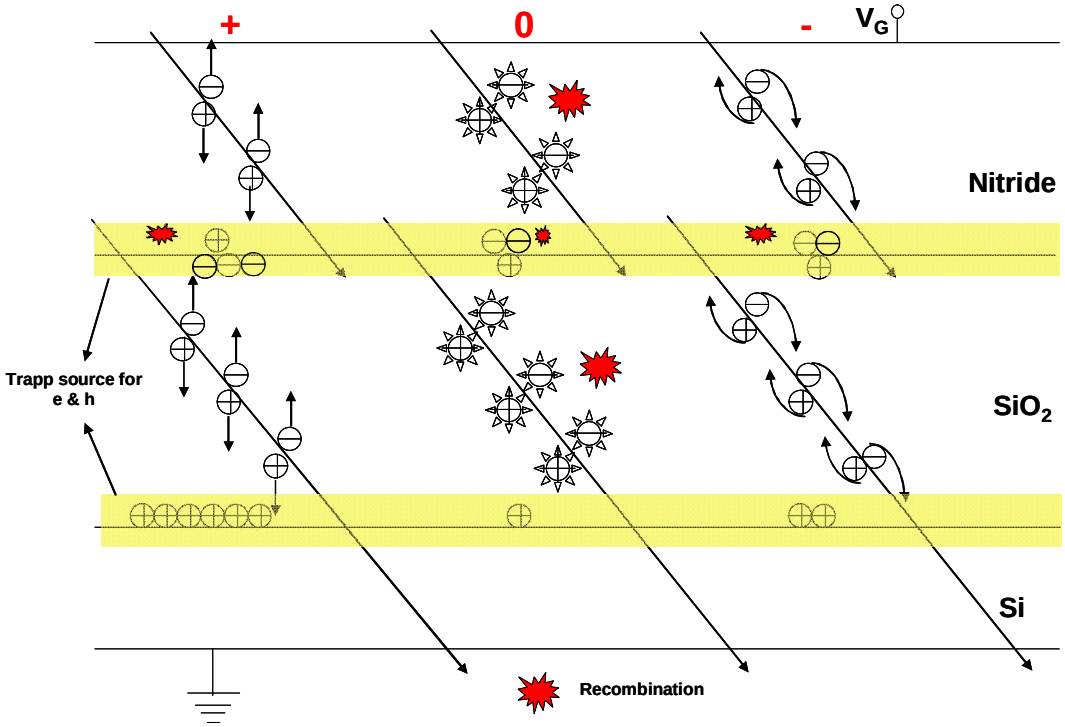


Figure 6.27 Spatial description about the generation, transportation and recombination process of electron-hole pairs due to ionizing radiation in the MNOS structure. The traps (precursors) are distributed in the interface marked as yellow region.

A minimum flat band voltage shift can be reached by performing the irradiation at zero gate voltage, since the recombination process plays a significant role, i.e., few electrons or holes can escape the recombination process direct when they are generated due to ionizing radiation compared to the biased irradiation. In addition, there are always recombination processes taking place at the N/O interface irrespective of gate voltage, since not only electrons but also holes will be incident on the traps that are distributed near the N/O interface. An overview of these recombination processes for three different bias conditions is given in Figure 6.27. Red regions represent the recombination processes. The yellow region denotes the N/O and Si/O interface where traps (precursors) are mainly located.

The MNOS structures investigated in this thesis are 86nm oxide with 10nm nitride and 100nm oxide with 10 nm nitride. Figures 6.28 and 6.29 show the flat band voltage shift of MNOS structures; the samples are biased at different gate voltages during irradiation. As mentioned previously, the flat band voltage shift slowly begins to saturate at doses higher than 1Mrad (SiO_2). The electric field dependent factor $\sigma_{ht} f_h$ in the exponential expression is shown in Figure 6.30.

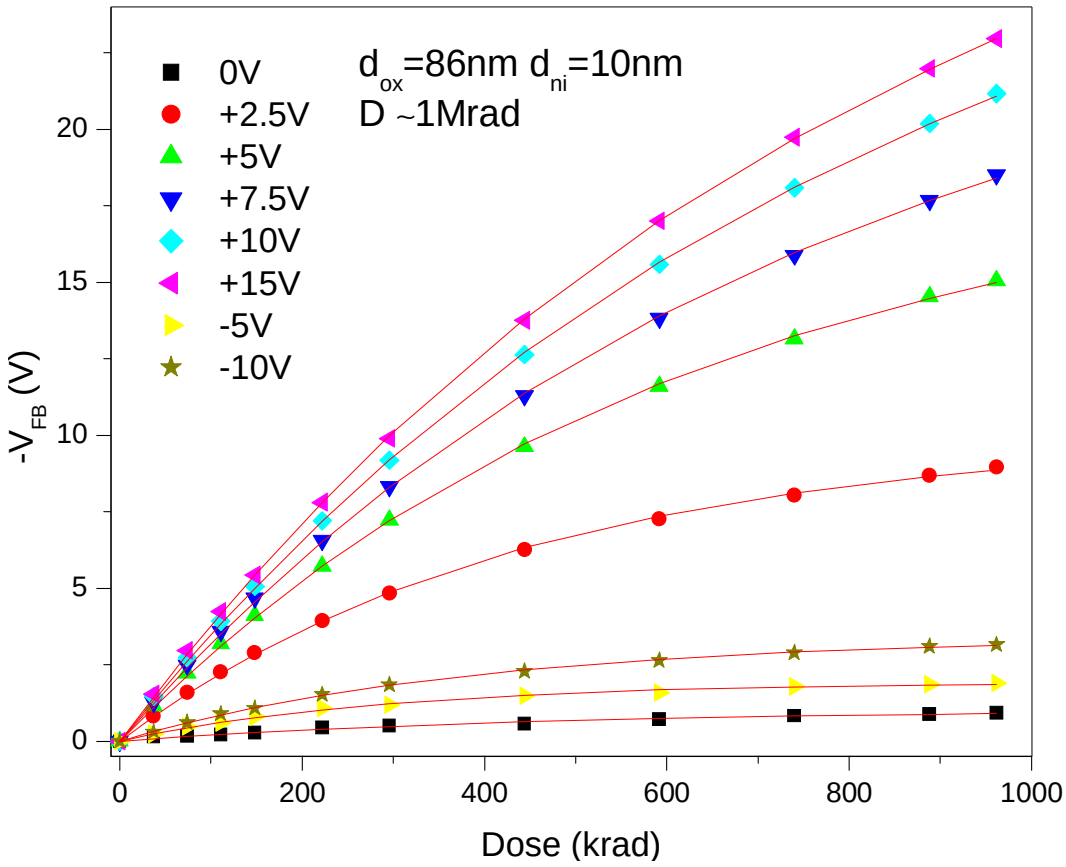


Figure 6.28 MNOS structure with 86nm oxide and 10nm nitride (type 6) under ionizing radiation up to about 1Mrad with different gate voltage. Points represent the measurement data, while the lines denote the exponential fitting of flat band voltage shift using Equation 6.35.

	d_{ox}/d_{ni} (nm)	N	σ_0 (cm^2)	σ_{ht} (at 1MV/cm) (cm^2)
1	86/10	0.93	1.4 E-08	3.6 E-14
2	100/10	0.9	8.3 E-09	3.6 E-14

Table 6.4 Fitting results for the capture cross section of hole traps.

The obtained capture cross section of hole traps of an MNOS structure is listed in Table 6.4. Here it represents the hole traps at the Si/O interface and hence it should be comparable with that of MOS structure: $3.6*10^{-14}$ cm^2 at 1MV/cm. However, a slightly different field dependence is found: $\sim E_{ox}^{-0.9}$ (Figure 6.31)

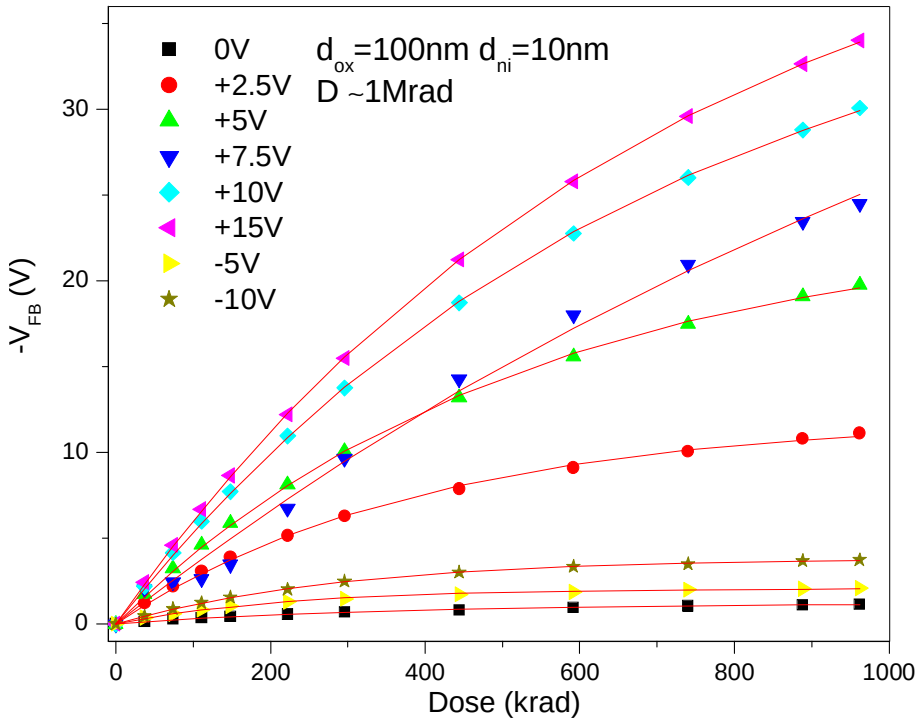


Figure 6.29 MNOS structure with 100nm oxide and 10nm nitride (type 8) under ionizing radiation up to about 1Mrad with different gate voltages. Points represent the measurement data, while the lines denote the exponential fitting of flat band voltage shift using Equation 6.35.

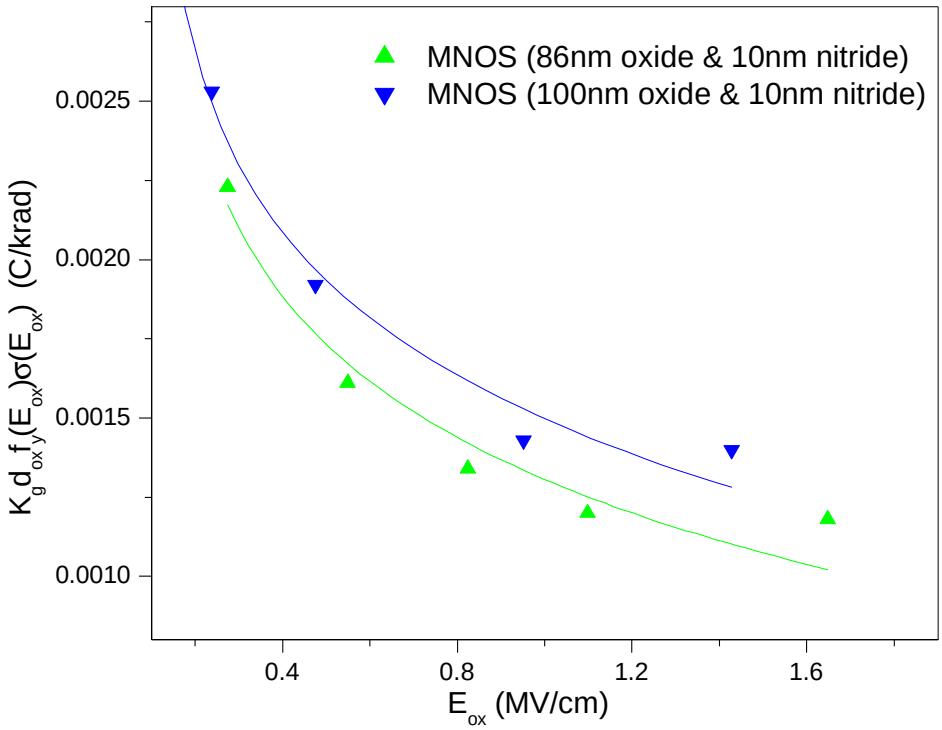


Figure 6.30 Fitting results of $\sigma_{ht} f_h$ for different combinations of oxide and nitride (type 6/8) using Equation 6.7.

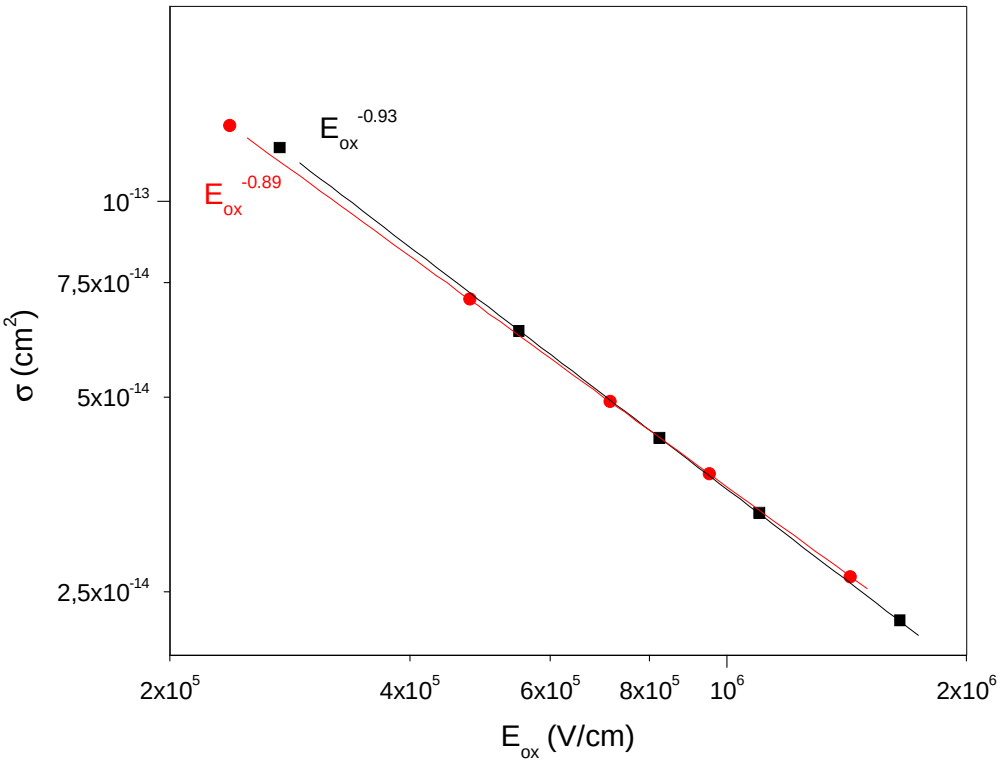


Figure 6.31 Oxide field dependence of the capture cross section of hole trap in SiO_2 determined by different wafers using Equation 6.4: Type 6 ~ $E_{ox}^{-0.93}$; Type 8 ~ $E_{ox}^{-0.89}$.

MNOS					
86/10 nm	Tpye 6		100/10 nm	Type 8	
Vg (V)	$N_{ox}/C_{eff.ox}$ (V)	$N_{eff.,ni}/C_{ni}$ (V)	Vg (V)	$N_{ox}/C_{eff.ox}$ (V)	$N_{eff.,ni}/C_{ni}$ (V)
-10	7.7	-4.3	-10	8.6	-4.7
-5	5.5	-3.6	-5	6.6	-4.5
0	4.9	-3.9	0	7.1	-5.9
2.5	19	-9	2.5	21	-9
5	28.7	-9.7	5	36.4	-13.2
10	41.2	-10.4	10	49.7	-9.7
15	46.2	-12.4	15	54.4	-11.6

Table 6.5 A list of N_{ht}/C_{ox} of an MNOS structure with 86/100 nm oxide and with 10 nm nitride (type 6/8) at different gate voltage.

Table 6.5 shows the values obtained to the factor $N_{ox}/C_{eff.ox}$ of an MNOS structure. As mentioned previously, the hole traps are mainly distributed at the interface especially at Si/O interface irrespective of MOS or MNOS structures, where the amount of the available hole traps (precursors) should be the same. However, the term $N_{ox}/C_{eff.ox}$ varies with different gate voltage since it is affected by hole fluencies, i.e., the higher the positive voltage applied on the gate, the more holes move to the Si/O interface and

accordingly more hole traps (precursors) are consumed to create positive oxide charges there. The higher the negative gate voltage, the more holes are separated from electron-hole pairs to move to the interface. However, trapped holes in this case are significantly smaller than in case of positive gate voltage, since hole traps (precursors) are fewer at O/Al than at Si/O interface. In the case of zero gate voltage, the holes escaping from electron-hole pair generation/recombination are located throughout the whole oxide bulk and are consequently least.

Weakly dependent of oxide thickness and comparing tables 6.2 and 6.5, the factor $N_{ox}/C_{eff.ox}$ is comparable with N_{ox}/C_{ox} in case of negative and zero gate voltage, while the factor $N_{ox}/C_{eff.ox}$ becomes significantly higher than N_{ox}/C_{ox} for positive gate voltages. Two relatively reasonable explanations are given as cause: firstly, the oxide capacitance is slightly higher than the effective oxide capacitance due to the effective oxide thickness; the second is that a small part of holes generated in the nitride may moves into the oxide for positive gate voltage, whereas holes arising from oxide may also drift into the nitride for negative gate voltages. Zero gate voltage can be explained in a similar way to negative gate voltage. With the help of fitting data from a MOS capacitor (Figure 6.24 and Equation 6.21), the effective charge trapping in the nitride can be made.

It is assumed that the Si/O interface in an MNOS behaves the same as that of a MOS capacitor. From 6.24, 6.25 and 6.35, the flat band voltage shift of an MNOS capacitor at about 1Mrad can be expressed as:

$$\Delta V_{FB}(MNOS) = -\left(\frac{N_{ox}}{C_{eff.,ox}} + \frac{N_{ni}}{C_{ni}}\right) = -\left[\frac{(\varepsilon_{ni} d_{ox} + \varepsilon_{ox} d_{ni})}{\varepsilon_{ni}} \times 0.03 \times d_{ox}^{0.05} + \frac{d_{ni}}{\varepsilon_{ni}}(N_{ni})\right] \qquad (6.36)$$

Where the first term stands for the shift from the positive oxide charges in the oxide, the second term denotes that from the charge trapping in the nitride, which can also be calculated from the flat band voltage shifts ΔV_{FB} in MNOS capacitors with three different oxide thicknesses (pink and purple points in the Figure 6.32).

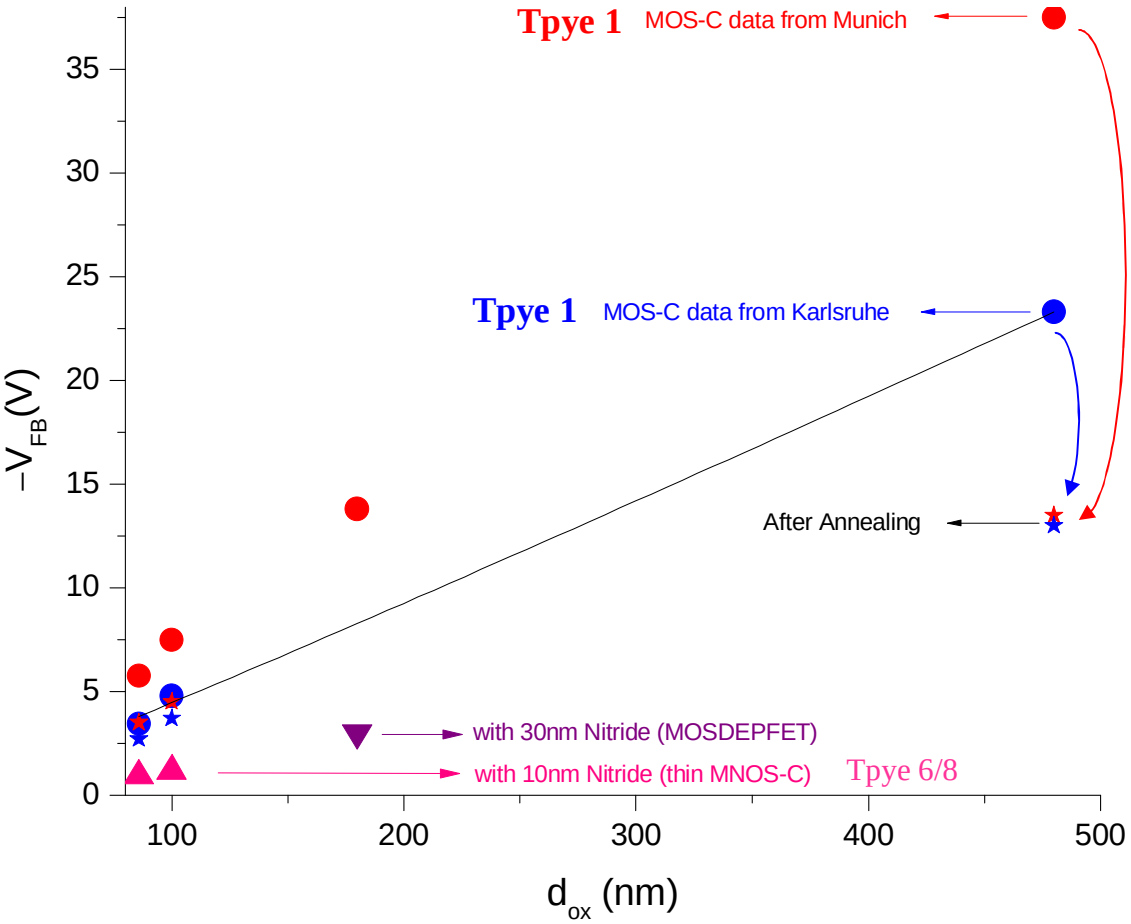


Figure 6.32. Flat band voltage shift of a MOS and an MNOS capacitor as a function of different oxide thicknesses at about 1Mrad (SiO_2). Bias during irradiation is 0V.

As shown in the Figure 6.32, the red circles denote the measurement data of a MOS capacitor direct after the irradiation of about 1Mrad obtained by CaliFa in Munich. The blue circles are MOS-C data measured directly after irradiation in Forschungszentrum Karlsruhe. These two different X-Ray facilities are already discussed in the Chapter 5. Although different ΔV_{FB} (red and blue) for the same device can be observed (dose rate effect), these differences will disappear after a long term annealing process (more than one week at room temperature). The pink triangles mean the flat band voltage shifts of MNOS capacitors with two different oxide/nitride combinations. The purple down triangle denotes the measurement data in case of a MOSDEPFET. The calculated flat band voltage shifts using (Eq. 6.36) are compared with the experimental results. For a zero gate voltage irradiation, Equation 6.36 can be determined as follow:

$$\Delta V_{FB}(MNOS) = -\left(\frac{N_{ox}}{C_{eff.,ox}} + \frac{N_{ni}}{C_{ni}}\right) = -\left[\frac{\left(\varepsilon_{ni} d_{ox} + \varepsilon_{ox} d_{ni}\right)}{\varepsilon_{ni}} \times 0.03 \times d_{ox}^{0.05} + d_{ni}\left(4.45 d_{ni}^{0.05} - 4.2 d_{ox}^{0.05}\right)\right] \tag{6.37}$$

The charge trapping in the nitride consists of two components: the effective hole trapping (positive sign) in the nitride layer and the effective electron trapping (negative sign) – both compete to determine the final effective charge trapping in the nitride. As discussed above, induced holes (escaping from the recombination) in the oxide will stay in the oxide lead to positive oxide charge, whereas electrons will drift to the nitride and make a large contribution to the electron trapping in the nitride, since electrons move faster than holes; furthermore, the number of trapped holes in the nitride depend on the nitride thickness, which is significantly thinner than the oxide thickness. For this reason, the final effective trapped charges are electrons in the nitride. The trapped electrons are relatively less under negative and zero biases and will become more increasing under positive gate voltage since the oxide layer is much thicker than the nitride layer and serves as a large electron source for trapping in the nitride.

The radiation induced trapped charges in an MNOS structure have been summarized for different nitride oxide thickness combinations.

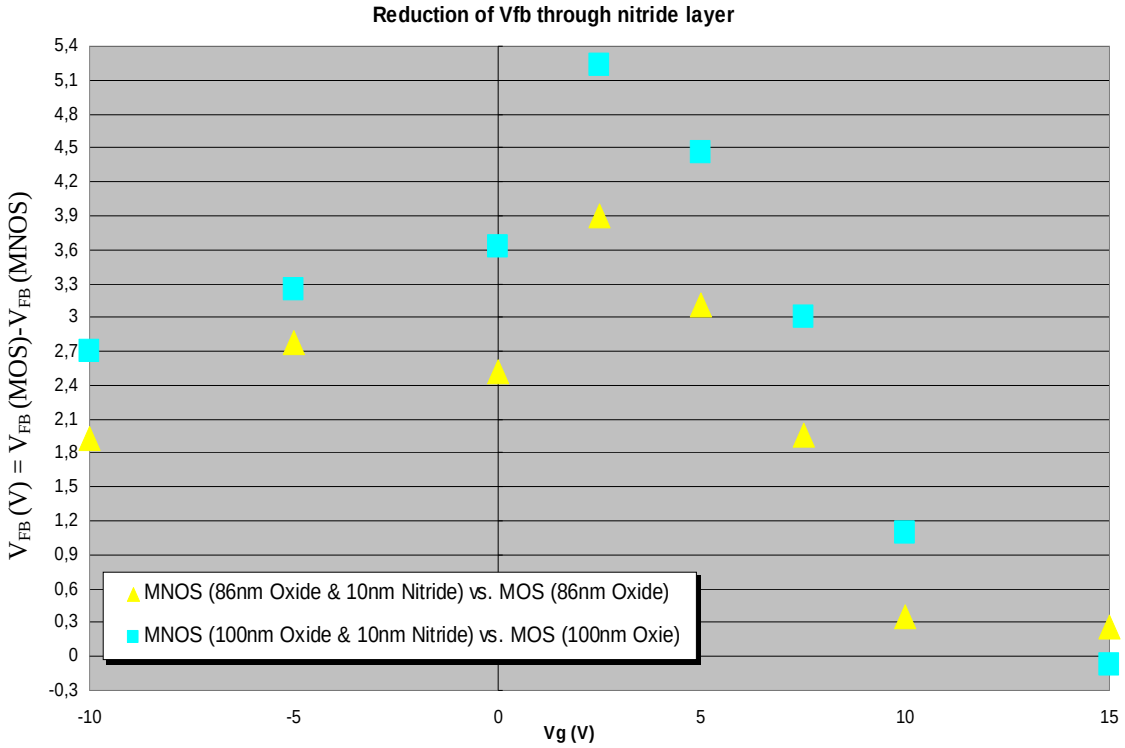


Figure 6.33 Reduction of flat band voltage shift due to nitride layer. MNOS of 86nm oxide and 10nm nitride (type 6) is compared with MOS of 86nm oxide (type 5) marked with yellow triangular, while MNOS of 100nm oxide and 10nm nitride (type 8) is compared with MOS of 100nm oxide (type 7) marked with a light-blue square.

It can be seen in Figure 6.33 that the flat band voltage shift of an MNOS structure due to ionizing radiation is less than that of a MOS structure of the same oxide thickness. The gate-voltage-dependent reduction of the flat band voltage shift is determined. It reaches its maximum value at a relative small positive gate voltage of about +2.5V irrespective of

different N/O thickness combinations. In reality this gate-voltage-dependent change of the flat band voltage shift can be traced back to the electric-field dependence. The calculation of the flat band voltage shift of a MOS (or an MNOS) has already been discussed in the previous chapter according to the charge trap model. For this reason, the electric-field-dependent reduction of V_{FB} is present once more in Figure 6.34.

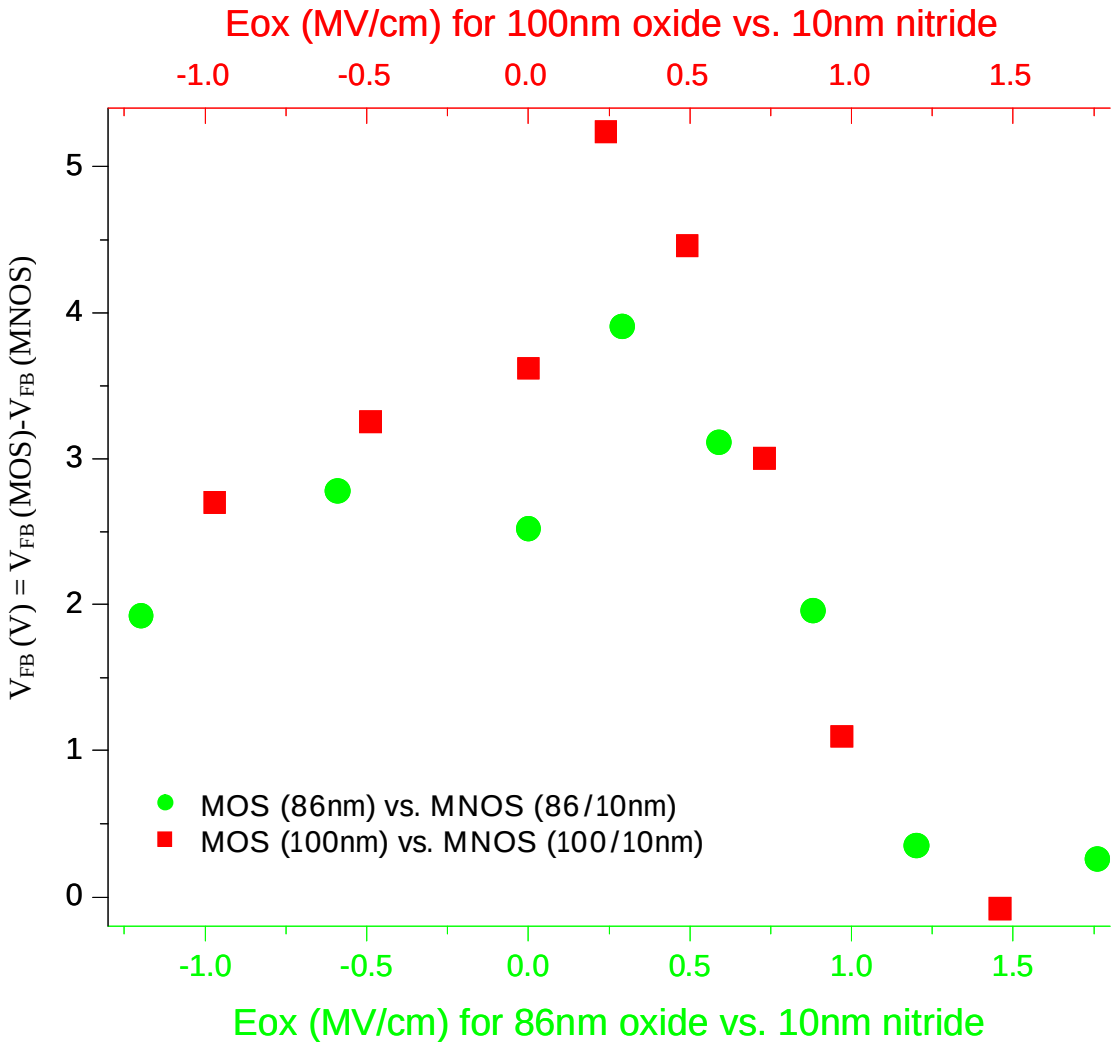


Figure 6.34 Electric field dependent reduction of V_{FB} (V_{FB} [MOS]-V_{FB} [MNOS]). Green points represent the data for comparison of V_{FB} between MNOS (86nm oxide and 10nm nitride) (type 7) and MOS (86nm oxide) (type 5); red squares denote that of MNOS (100nm oxide and 10nm nitride) (type 8) and MOS (100nm oxide) (type 6).

Table 6.6 shows a list of determined flat band voltage shift measured on different chips under different gate polarities. It is obviously that the flat band voltage shift will be reduced independent of gate biases if an MNOS and a MOS structure with the same oxide thickness are compared. However, the amount of the reduction is a function of the electric field.

Chip thickness (nm)		Electrically measured equivalent oxide thickness (CV)	Pre-Rad V_{FB}(V)	Post-Rad ΔV_{FB}(V) ~1Mrad Vg=-10V	Post-Rad ΔV_{FB}(V) ~1Mrad Vg=-5V	Post-Rad ΔV_{FB}(V) ~1Mrad Vg=0V	Post-Rad ΔV_{FB}(V) ~1Mrad Vg=+2.5V	Post-Rad ΔV_{FB}(V) ~1Mrad Vg=+5V	Post-Rad ΔV_{FB}(V) ~1Mrad Vg=+7.5V	Post-Rad ΔV_{FB}(V) ~1Mrad Vg=+10V	Post-Rad ΔV_{FB}(V) ~1Mrad Vg=+15V
Equivalent Oxide thickness	Oxide/Nitride thickness										
86	86	76 ± 2	-0,6	5.1	4.7	3.4	12.9	18.2	20.5	21.4	23.2
91	86/10	85 ± 2	-1,3	3.1	1.9	0.9	9	15	18.5	21	23
100	100	95 ± 2	-0,7	6.4	5.3	4.8	16.4	24.2	28.4	31.2	33.9
105	100/10	103 ± 1.5	-1.4	3.7	2.1	1.2	11.1	19.8	24.5	30.1	34

Table 6.6 Determination of flat band voltage shift for different N/O combination before- and after-irradiation.

For positive gate voltages: with respect to charge trapping in the nitride, electron trapping is significantly more important than hole trapping, since electrons mainly arise from the oxide due to ionizing radiation. The reduction of flat band voltage reaches its maximum at relative small positive voltage (about 2-3V), since most the generated electrons in the oxide bulk will move to the N/O interface and remain there trapped; while holes generated in the nitride bulk will move to the N/O interface and stay there due to a hole barrier. Moreover, the contribution of V_{FB} arising from electron trapping in the nitride and hole trapping in the oxide are inverse and the absolute value of V_{FB} is principally determined by this formula N_{ox}/C_{ox} (trapped charges in the oxide) and N_{ni}/C_{ni} (trapped charges in the nitride). Because C_{ni} is dominantly higher than C_{ox}, the reduction of V_{FB} through electron trapping is compensated by hole (from nitride) trapping in the oxide. For negative gate voltage: the reduction of flat band voltage remains small. Most of the electrons generated in the nitride can be trapped at the N/O interface; while holes generated in the oxide bulk will be mostly trapped in the oxide near the N/O. for zero gate voltage, it can be considered as a case similar to negative voltage.

6.6 Other parameters affected by radiation

In addition to the characteristic parameters that reflect the radiation response of MOS devices discussed previously (flat band voltage for MOS capacitance; threshold voltage for MOSDEPFET; surface generation current for MOS gated diode), some other important parameters will be introduced in this section: e.g. breakdown voltage, trans-conductance, surface recombination velocity of electron or holes (depends on the doping type of substrates used in the MOS devices) and lifetime, etc.

MOS-Capacitance

Oxide as well as nitride can be considered as a good insulator to produce the dielectrics layer between metal and semiconductor (silicon). In general, oxide breakdown refers to the destruction of an oxide layer in MOS devices. It may happen through high voltage applied on the gate of a MOS device.

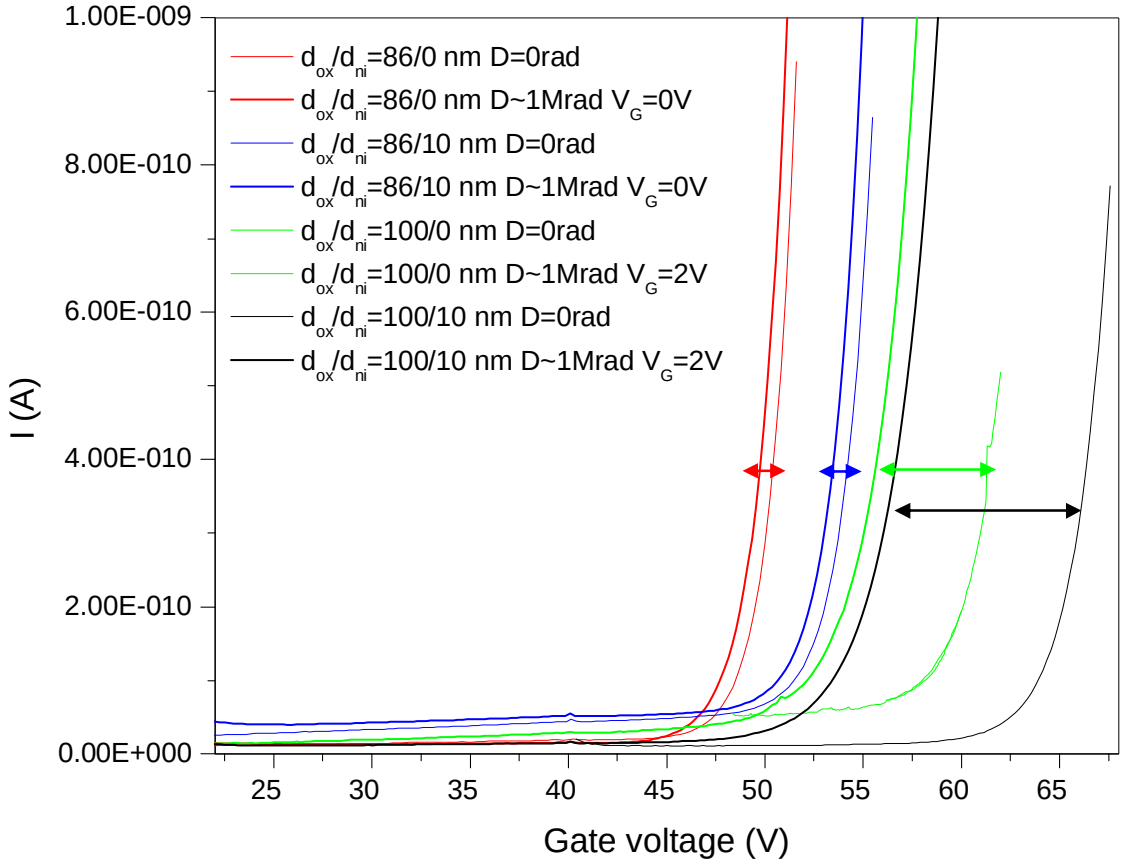


Figure 6.35. Changing of breakdown voltage for MOS structure (type 5-8). Thin lines mean IV before irradiation, while thick lines mean IV after irradiation.

For this reason, any characteristic measurements like CV measurement should be performed below the breakdown voltage, which can characterize the oxide quality. Usually an oxide layer can break down around 10 MV/cm depending on the oxide quality. The breakdown voltage can be calculated using the electric field (breakdown field) for different oxide thickness.

It is experimentally observed that this parameter (breakdown field) will be changed after irradiation. As shown in Figure 6.35, four thin lines in different colors represent MOS structures with different oxide/nitride thickness before irradiation. In this case, the electric field of oxide breakdown is about 6 MV/cm. However, it is obvious that the oxide quality will be degraded by surface damages, since the electric field of oxide breakdown is reduced as well as the breakdown voltage. In the case of zero gate voltage during the irradiation, the radiation induced damages remain minimal compared to positive gate voltage. For this reason, the oxide quality is more degraded by irradiation at positive gate voltage than at zero voltage. The electric field of oxide breakdown is reduced by around 0.3 MV/cm for 0V irradiation and about 0.6 MV/cm for 2V irradiation.

MOSDEPFET

Concerning a p-channel MOSDEPFET exposed by gamma ray (Co^{60}) at energy of 1.17 MeV and 1.33 MeV, a lot of information about radiation response can be extracted from the transistor characteristics: drain current as a function of gate voltage. For instance, the positive oxide charges are determined by the shift of threshold voltage; the interface traps can be calculated with subthreshold technique using the subthreshold swing.

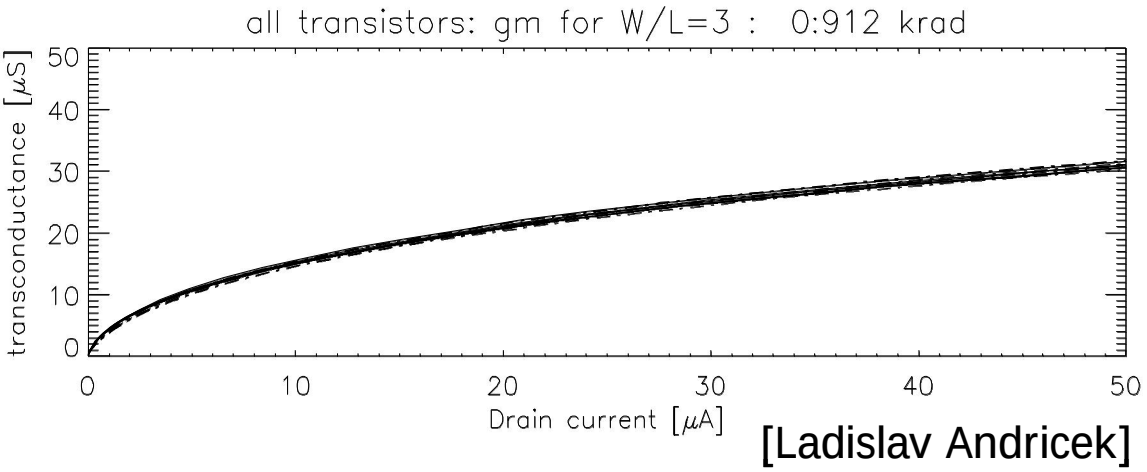


Figure 6.36 Change of the transconductance for a p-channel MOSDEPFET under gamma ray irradiation from Co^{60} source at 1.17MeV and 1.33 MeV up to a dose of 912 krad [2].

As depicted in Figure 6.36, transconductance as a function of drain current is plotted for all measured transistors. No change in the transconductance can be observed for gamma ray irradiation. Since one of the important consequences of the ionizing radiation is the degradation of the transconductance, which comes from the reduced mobility of the charge carriers due to carrier scattering with interface traps, no degradation of transconductance can be explained by considerably low concentration of interface traps.

In addition, another important issue is the spectroscopic performance of the MOSDEPFET measured with an Fe^{55} radiation source before and after irradiation. The measured spectrum is shown in Figure 2.6. Before irradiation, an equivalent noise charge in the noise peak is obtained by 1.6 e^- (rms) [61].

After irradiation the measured spectrum shows an equivalent noise charge in the noise peak of 3.5 e^- (rms) at room temperature (Figure 6.37). This means a relative smaller increase of about 2 e^- equivalent noise charge is obtained by ionizing radiation even up to about 1 Mrad. This small increase in the noise arises from the induced interface traps that will raise the low frequency noise (1/f).

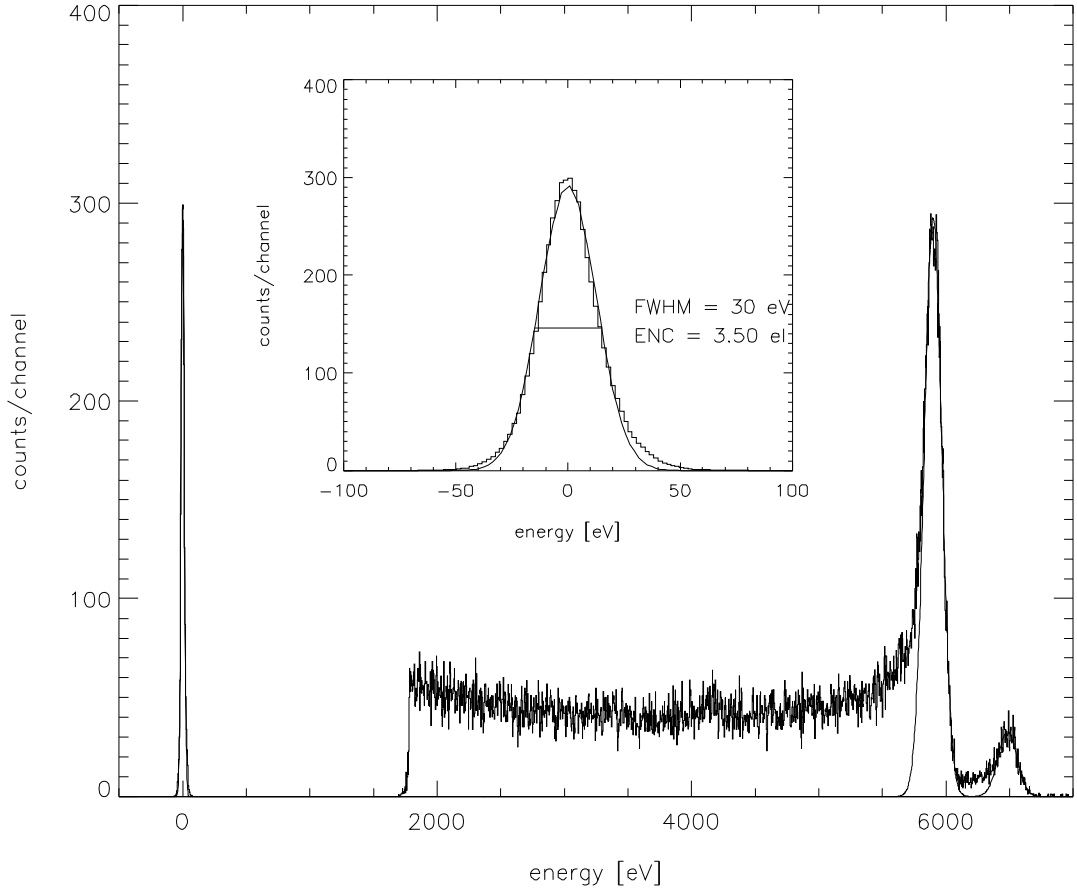
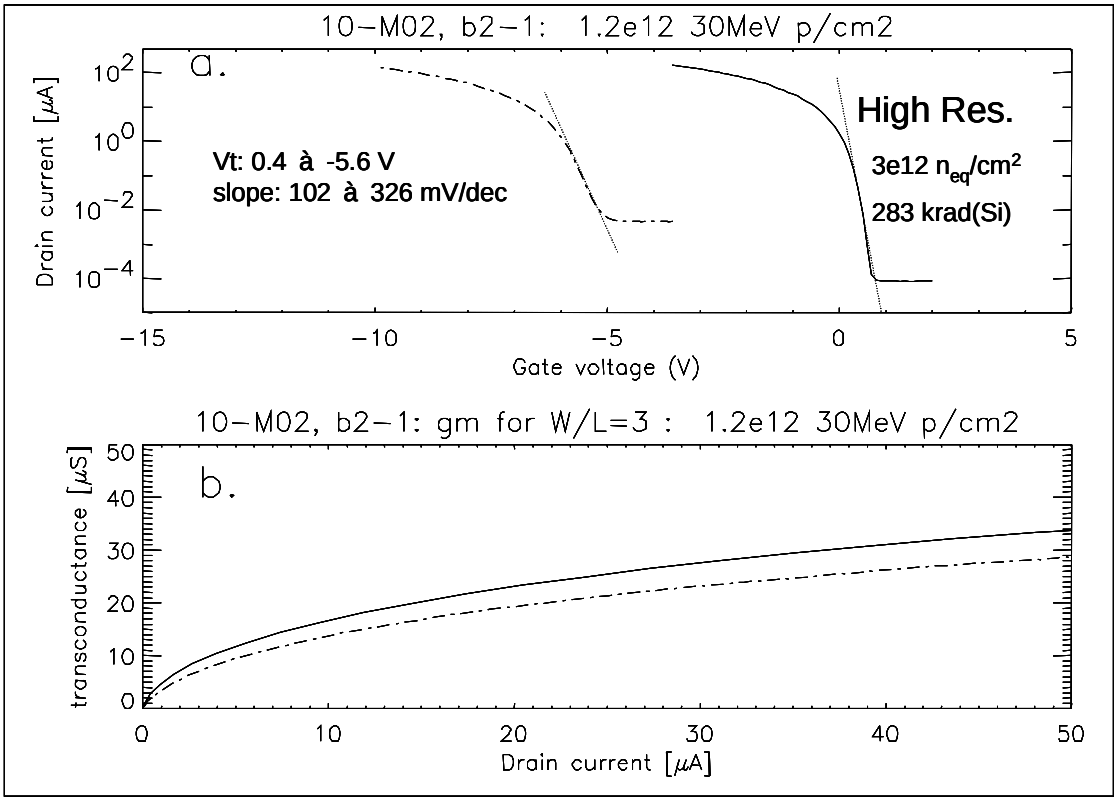


Figure 6.37 Figure 2.6 Spectroscopic performance of a linear MOS-type DEPFET (with gate length L=7um and gate width W=25um) after irradiation of up to 913 krad exposed by Co^{60} source at room temperature, integration time is set to 10us. The insert shows the noise peak with an ENC (rms) =3.5e^- (Performed by Laci Andricek) [61].

It is clearly to show the potential of the MOSDEFEPT for both X-ray spectroscopy and the vertex detector at the ILC. For this reason, other radiation sources have also been utilized to test the radiation hardness of this device, for instance – proton/neutron irradiation.

In the case of proton irradiation, samples are irradiated by proton at 30 MeV up to 1.2 *10^{12} p/cm^2, which can be recalculated to 3*10^{12} (1MeV neutron equivalent) in order to compare the radiation response of such devices between proton and neutron irradiation (Figure 5.2). Radiation dose in silicon is equivalent to 283 krad. According to the expectation of ILC of 8.5*10^{10} cm^{-2} $year^{-1}$ (1 MeV neutron equivalent), the radiation tolerance against proton irradiation environment corresponds to about more than 30 years.



[Stefan Rummel]

*Figure 6.38 Change of the transconductance for a p-channel MOSDEPFET under proton irradiation up to a dose of 283 krad in silicon, proton fluency is1.2 *10^{12} p/cm^2 at 30 MeV. (Performed by Stefan Rummel)*

It is shown in Figure 6.38 that the shift of threshold voltage is about 5 V after irradiation from the measured characteristic curves, which points out the positive oxide charges trapped in the oxide. An increase of subthreshold slope denotes the induced interface traps that result in an enhanced low-frequency noise (1/f). The degraded charge carrier mobility leads to a reduced transconductance of about 15%.

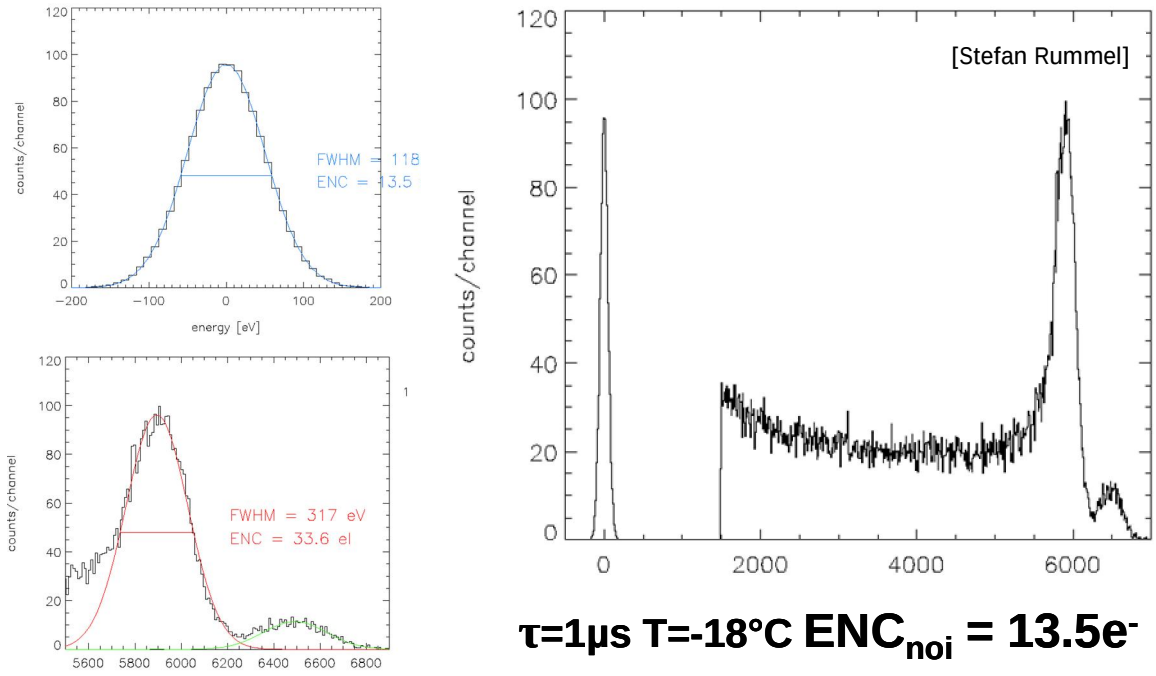


*Figure 6.39 Spectroscopic performance of a double pixel MOSDEPFET with gate length L=6um and W/L=3 after proton irradiation at 30 MeV of up to a dose of 283 krad in silicon, proton fluency is1.2 *10^{12} p/cm^2 source at low temperature, integration time is set to 1us. (Performed by Stefan Rummel)*

The spectroscopic performance shows an equivalent noise charge in the noise peak of about 5 e^- (rms) before the proton irradiation. There are not only surface damages due to ionizing radiation (charged proton) but also bulk damages generated due to (NIEL). Since bulk damages lead to an increased leakage current, and the third term (I_L) from Equation 2.2 in equivalent noise charge will increase the noise to a larger extent than the first term (thermal noise), it is better to measure the equivalent noise charge at smaller integration time and lower temperature, which is about 13.5 e^- (rms) with integration time of 1us and temperature of -18 Celsius (Figure 6.39). The separated Kα Kβ peak measured with Fe^{55} source demonstrates a good radiation tolerance against proton irradiation up to fluency of 1.2 *10^{12} p/cm^2.

Unlike proton irradiation, neutrons are not ionizing. The dominant consequence of neutron irradiation is only the bulk damages (Figure 6.40). Samples are irradiated by neutron at 1-20 MeV up to 1.6 *10^{11} n/cm^2, which can be recalculated to 2.4*10^{11} (1MeV neutron equivalent). As discussed above, the radiation tolerance against the neutron irradiation environment for the application of ILC corresponds to about 3 years.

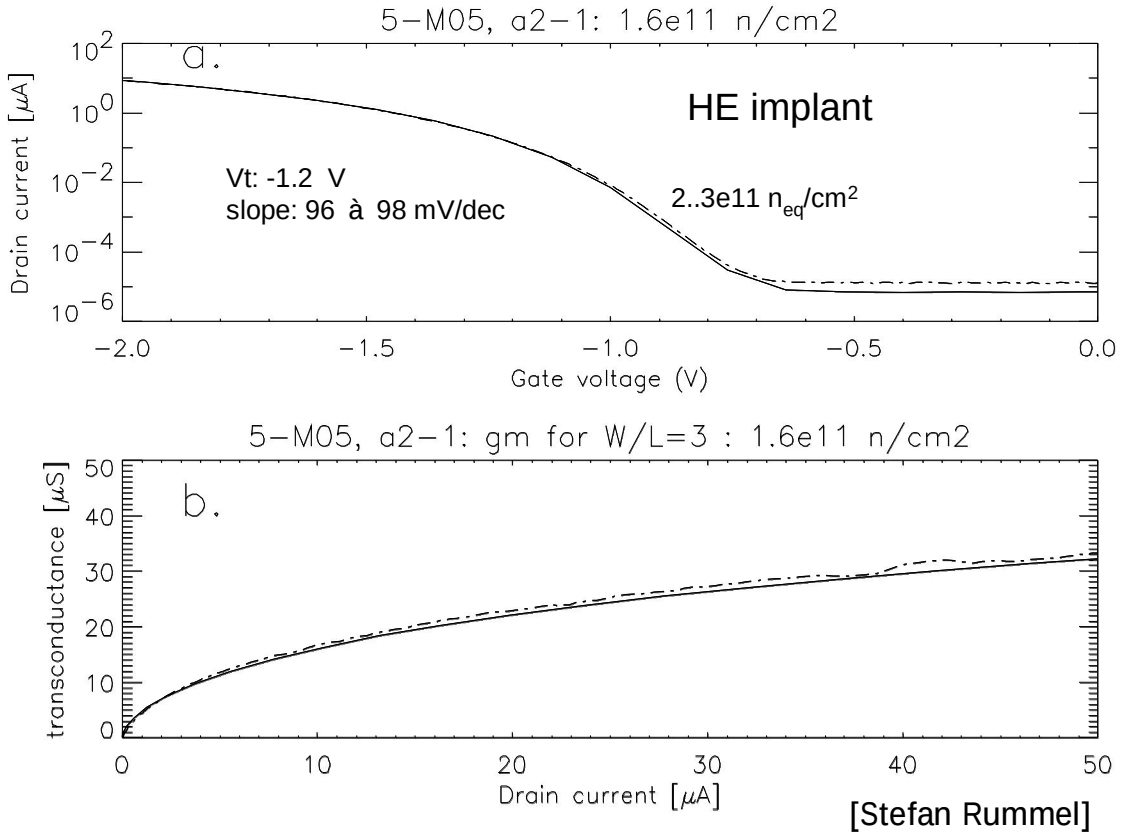


*Figure 6.40 Change of the transconductance for a p-channel MOSDEPFET under neutron irradiation with a neutron fluence of 1.6 *10^{11} n/cm^2 at 1-20 MeV. (Performed by Stefan Rummel)*

Since there is no surface damage generated in the oxide bulk and interface region, the threshold voltage does not change any more, and there is also no observable change of subthreshold slope after irradiation. Due to no contribution from interface traps the measured trans-conductance does not degrade.

The spectroscopic performance after neutron irradiation is measured with an Fe^{55} radiation source. The increasing noise that comes from leakage current due to bulk damage can be reduced significantly by cooling down to -18 Celsius, while the thermal noise decreases with longer integration time. The equivalent noise charge is about 3.1 e^- (rms) at 6 Celsius with integration time of 6 us (Figure 6.42). The same as proton irradiation a good radiation tolerance against neutron environment is achieved up to a neutron fluency of 1.6 *10^{11} n/cm^2 with respect to the separated Kα Kβ peak.

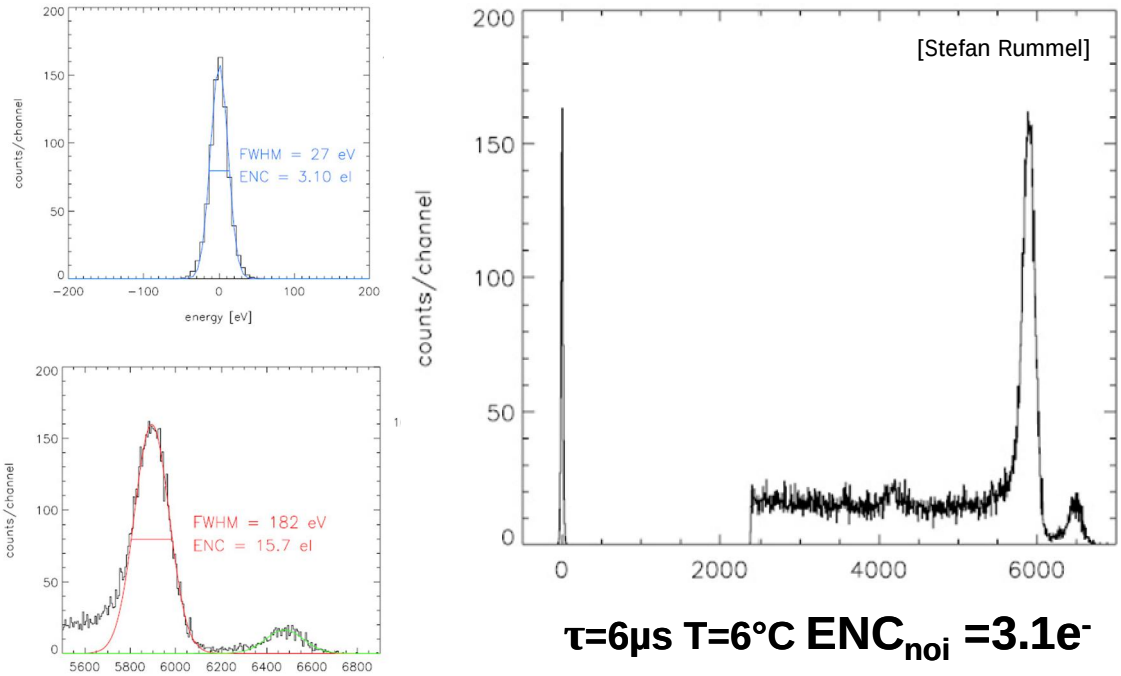


*Figure 6.41 Spectroscopic performance of a double pixel MOSDEPFET with gate length L=6um and W/L=3 after neutron irradiation at 20 MeV with a neutron fluency of 1.6 *10^{11} n/cm^2 at temperature of 6 Celsius, integration time is set to 6us. (Performed by Stefan Rummel)*

In general, in order to avoid the influence of interface traps with respect to the internal gate region, normally a high-energy implantation technique is used to produce the internal gate deep in the substrate bulk from Si/O interface, which somehow results in a slightly reduced threshold voltage of about 1V comparing with that of samples without HE implantation.

MOS gated diode

In addition to surface generation current there are other characteristic parameters that can reflect the radiation response on the MOS gated diode: surface recombination velocity and lifetime and capture cross section of electrons or holes (depending on the type of substrate used for the MOS devices).

Ionizing radiation-induced interface traps associated with a generation/recombination process is of major importance since it affects the reverse current at the silicon surface, which degrades the electric performance of MOS devices. Surface recombination velocity is a parameter that can characterize the silicon surface state related to interface traps N_{it}. It can be determined by the density of recombination centers associated with the density of interface traps and by the effective capture cross section of electrons or holes at the interface. According to Equation 3.11 the surface recombination velocity can be calculated directly from the surface generation current measurement.

Where q is the elementary charge, n_i is the intrinsic charge carrier concentration, A is the gate area. Furthermore, the effective capture cross section can also be obtained by surface recombination velocity and interface traps density, whose precision depends on the experimental determination of s_0 and N_{it}:

$$\sigma_{n/p} = \frac{s_0}{v_{th} \pi kTN_{it}} \tag{6.38}$$

Where v_{th} is thermal velocity, k is Boltzmann constant, T is the temperature and N_{it} is interface traps density. As depicted in Figure 6.42, surface recombination velocity and capture cross section increase with radiation dose and saturate at about 1 Mrad.

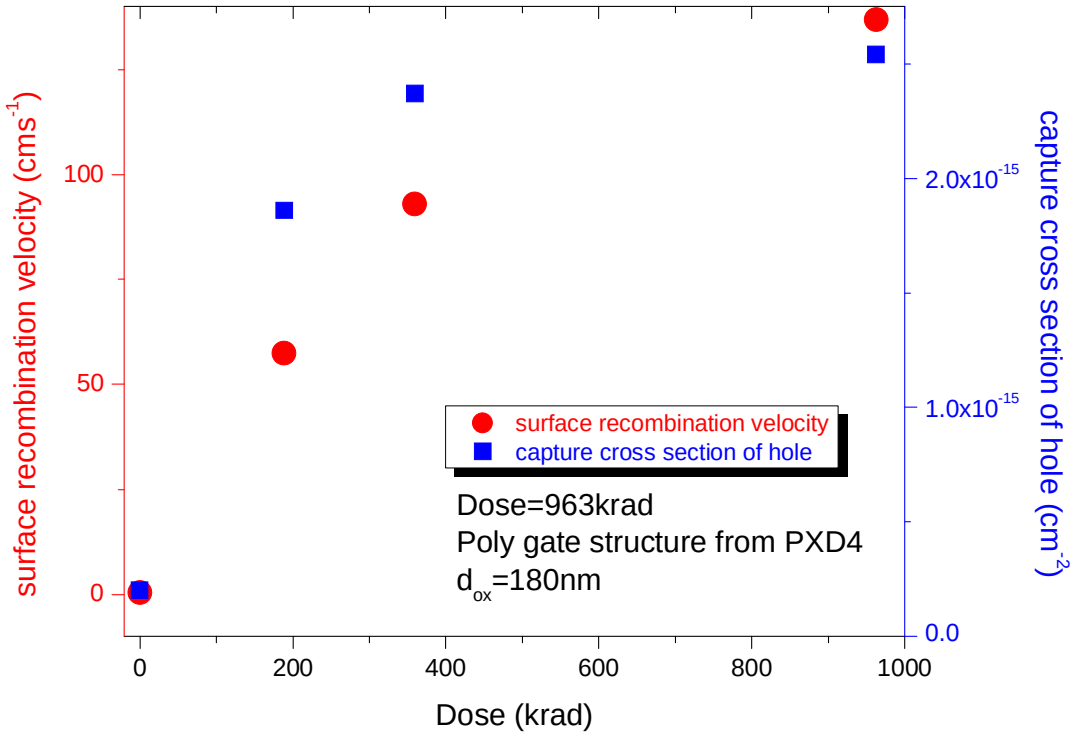


Figure 6.42 Surface recombination velocity and capture cross section of hole as a function of radiation dose for the Poly-gate structure on the MOS gated diode (type 4). Radiation dose is up to 963 krad.

The effective lifetime of holes in the depletion region at the silicon surface is calculated from experimental extracted surface recombination velocity and silicon depletion region width:

$$\tau = \frac{d_{depl.}}{s_0} = \frac{qn_i A d_{depl.}}{I_{it}} \tag{6.39}$$

Where $d_{depl.}$ is the width of silicon depletion region under the gate dielectrics. Figure 6.43 denotes that the effective lifetime is longer before irradiation and becomes considerably shorter direct after irradiation, which reflects the recombination process depends strongly on the interface traps due to ionizing radiation.

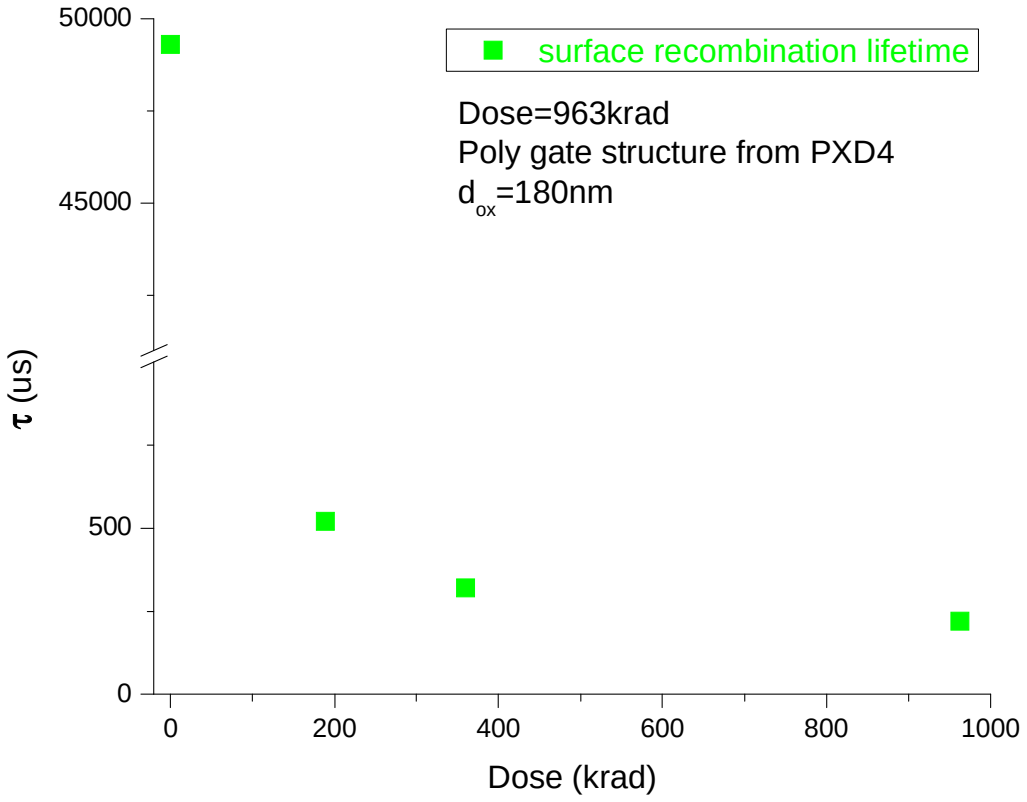


Figure 6.43 The effective lifetime Tau of hole as a function of radiation dose for the Poly-gate structure on the MOS gated diode (type 4).

6.7 Saturation of surface damage

As shown in Figure 6.5 previously, surface damages (positive oxide charges and interface traps) are plotted as a function of radiation dose. For doses below 10^5 rad (SiO_2), the shift extracted from the characteristic parameters changes almost linearly with dose; however, it becomes exponential at higher doses and will saturate at even higher doses. This saturation effect is a very common feature of MOS devices under ionizing radiation; of course it depends on the MOS device processing and irradiation conditions. It is experimentally observed for both types of surface damages: positive oxide charges and interface traps.

Normally the amount of surface damages depends on hole traps (precursors) at the interface region or just the vicinity (a few nanometers from the interface) and electron-hole pairs. As mentioned previously, the ionizing radiation-induced electron-hole pairs can be firstly generated and separated under the electric field, and then the from the recombination escaped holes move toward the interface region and react with strained Si-Si bond to build positive oxide charges. Another part of holes are captured by hydrogen that comes from silicon complexes and go further into the interface to form an interface traps with silicon dangling bonds or trivalent silicon. In general, at lower radiation dose level only the generation process for surface damages takes place. However, with increasing dose, several other processes become also important and lead to a nonlinear dependence of trapping, i.e., up about a few 100 Krad, the recombination effect and detrapping effect play an important role (Figure 6.44).

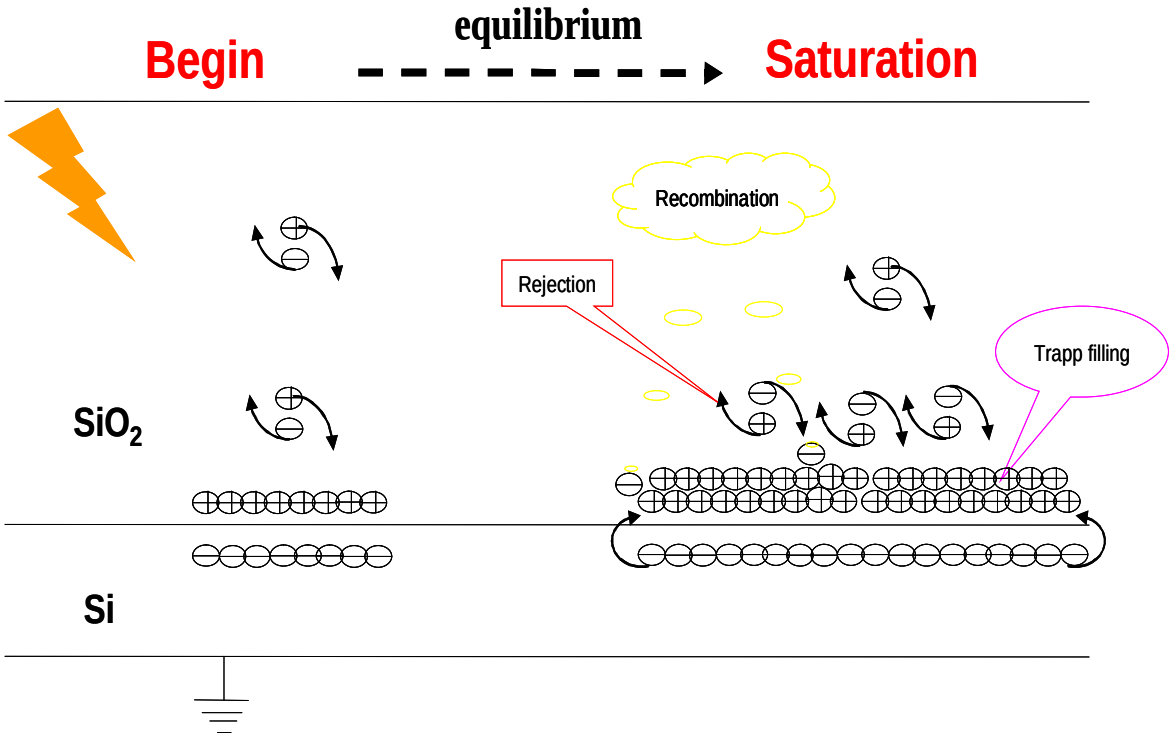


Figure 6.44 Saturation effect for surface damage at about 1 Mrad.

At the beginning of the irradiation process, there are only a few positive oxide charges trapped near the interface region, which induce another type of charge carriers (electrons) in the silicon. With time more and more induced holes accumulate in the oxide trap during the irradiation, the new holes can be either trapped in the oxide defects or just simply be rejected away; the new generated electrons can recombine with the positively trapped holes. For this reason, the local yield of electron-hole pairs due to ionizing radiation will be suppressed and result in an enhanced recombination effect. Equilibrium between trapping and recombination is finally advised that is responsible for the saturation effect of surface damages.

6.8 Annealing

During processing characteristic defects that can create interface traps can be passivated by hydrogen or hydroxide, consequently interface traps density can be significantly reduced through the annealing process (annealing during processing) at relative high temperature (about 400 Celsius), which use either forming gas H_2/N_2 or water-vapor atmosphere. For this reason, recovery of interface traps shows thermal annealing. It is worth mentioning that any high-temperature process later on will result in a release of passivated silicon bonds to increase the defect density again.

The holes trapped in the SiO_2 of a MOS structure after irradiation is not permanently trapped there. They are annealing during ramping from seconds to years. At present, two fundamental processes are responsible for the annealing of positive oxide charges:

1. Thermal annealing: the removal or recombination of trapped holes occurs rapidly at elevated temperature (starting from 100 Celsius) due to thermal generation of charge carriers in the oxide.

2. Tunnel annealing: compared with thermal annealing, the removal process takes place slowly typically at room temperature through tunneling of electrons from the silicon into the SiO_2/Si interface [47.48.49].

Thermal annealing generally describes a thermally related recovery process. The radiation-induced damages (defects) can be reduced through the application of standard thermal annealing procedures. The information of damage annealing can be given by performing various methods, like Thermal Stimulated Current (TSC), Deep Level Transient Spectroscopy (DLTS) etc. In the following many details will be introduced to describe tunneling. In general, most of the irradiation experiments take place at room temperature. Therefore, the thermal annealing is strongly suppressed. Instead, the tunnel annealing will play an important role for the removal of trapped holes. As stated above the tunnel annealing comes about when electrons from silicon tunnel into the SiO_2/Si interface and, furthermore, recombine with the trapped holes there. Holes can be removed within a distance $X_m(t)$ from interface extending into oxide. Because of exponential damping of the tunnel probability, this depth increases logarithmically with time [47]:

$$X_m(t) = \frac{1}{2\beta} \ln\left(\frac{t}{t_0}\right) \tag{6.40}$$

Where β is the tunneling barrier height parameter, t_0 is a time scale parameter.

In order to solve Equation 3.2 an exponential decay with respect to the density of the trapped holes has to be assumed [47]:

$$n_{ht}(x) = n_{ht}^{0} \exp(\lambda_t x) \tag{6.41}$$

Where n_{ht}^{0} is the density of trapped holes in the interface directly after irradiation, and λ_t^{-1} is the characteristic length for the distribution of occupied traps.

Using equations 6.40 and 6.41, one achieves a time-dependent recovery process by integration of the trap distribution from the interface to $X_m(t)$:

$$\Delta N_{ox}(t) = \int_0^{X_m(t)} n_{ht}^{0} \exp(\lambda_t x) dx = \frac{n_{ht}^{0}}{\lambda_t}\left[\left(\frac{t}{t_0}\right)^{\frac{\lambda_t}{2\beta}} - 1\right] \tag{6.42}$$

Hence the distribution of the oxide charges is:

$$N_{ox}(t) = N_{ox}(t=0) - \frac{n_{ht}^{0}}{\lambda_t}\left[\left(\frac{t}{t_0}\right)^{\frac{\lambda_t}{2\beta}} - 1\right] \tag{6.43}$$

$N_{ox}(t=0)$ is the oxide charges density per unit area at time t = 0 directly after irradiation (The beginning of annealing process). It is assumed that hole traps in the oxide are homogenously distributed at least in the tunneling distance from interface and the tunneling depth is much smaller than the oxide thickness:

$$X_m(t) << d_{ox} \ (\lambda \to 0) \tag{6.44}$$

The Equation 6.43 can be simplified like:

$$\Delta N_{ox}(t) = \frac{n_{ht}^{0}}{2\beta} \ln\left(\frac{t}{t_0}\right) \tag{6.45}$$

Deriving the flat band voltage shift due to positive oxide charges from Equation 3.1 results in:

$$\Delta V_{ox} = -\frac{q}{\varepsilon_0 \varepsilon_{SiO_2}} d_{ox} \Delta N_{ox} = -\frac{q d_{ox} n_{ht}^{0}}{2\varepsilon_0 \varepsilon_{SiO_2} \beta} \ln\left(\frac{t}{t_0}\right) \tag{6.46}$$

In this case not only the density of positive oxide charges per area N_{ox}, but also the flat band voltage shift V_{ox} decreases proportional to ln(t) (Figure 6.45). In reality, E' centers are not homogenously distributed in the oxide; instead, the density decreases rapidly with

increasing distance from the SiO_2/Si interface. Trapped holes near the gate contact can also be removed by tunneling process. Because the concentration of hole traps near the gate is significant smaller than at the interface, this case is not so relevant for oxides with moderate thickness. However, for much thinner oxides (e.g. a few nanometers) that effect becomes important.

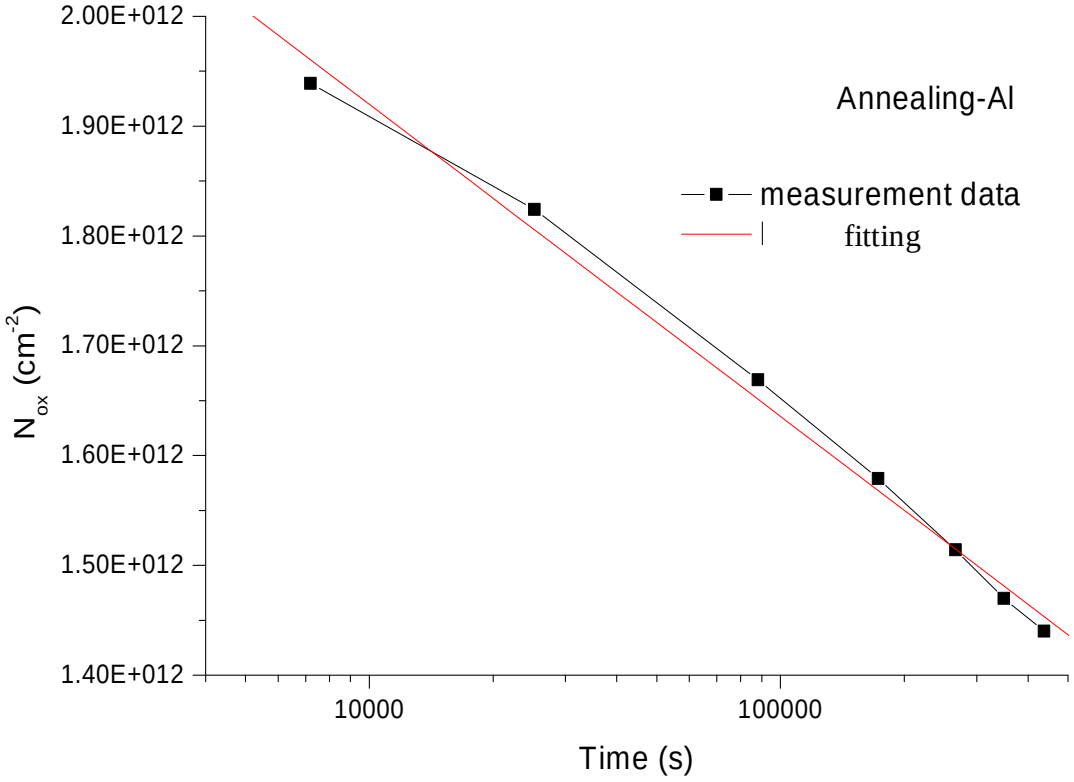


Figure 6.45 Recovery process of positive oxide charges: only a small portion of N_{ox} is removed through tunnel annealing. Time dependence of N_{ox} is a logarithmic.

Normally the temperature of the tunneling process is not fixed with much precision, typically at room temperature. At moderate elevated temperature a transition phase may happen, i.e. both of two annealing processes have an effect on ΔV_{ox}. In addition, tunneling process depends also on the applied field, since the barrier changes. It is clear that the tunneling effect will be dominantly enhanced by positively applied gate voltage compared with the case of zero gate voltage. In the case of negative gate voltage the tunneling of electrons will be strongly suppressed.

At highly elevated temperatures (higher than 100 Celsius) the thermal annealing plays a more important role than the tunnel annealing. Both annealing processes for the trapped holes depend on the temperature and the applied field. From the point of view of the recovery process of the trapped holes they distinguish themselves through the energy level and distribution of the hole traps. With respect to both structures MOS and MNOS,

a large number of hole traps are accumulated at the Si/O interface; whereas a small part of hole traps are located at O/Al interface. For MNOS structures, both electron and hole traps can be found at the N/O interface, due to its charge storage characteristics the trapped electrons or holes are difficult to be annealed under normal circumstances. For this reason, the annealing process of a MOS or an MNOS structure at room temperature mainly involves positive oxide charges at Si/O interface region, which can be annealed due to tunnel annealing.

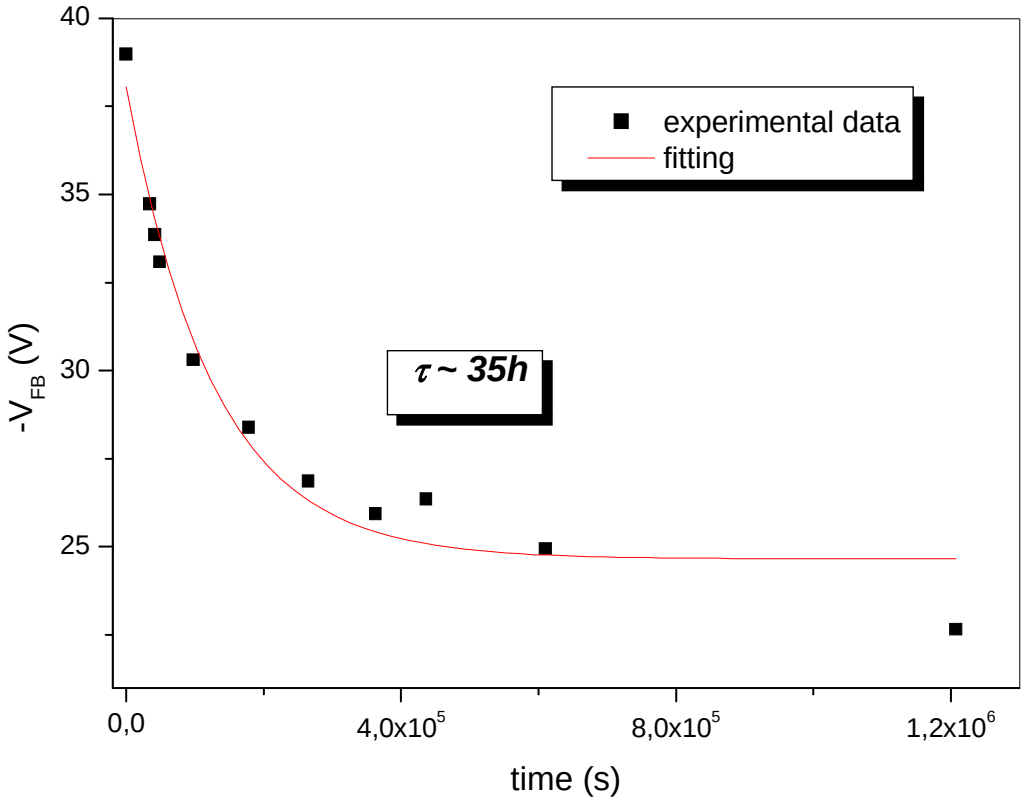


Figure 6.46 Annealing of the positive oxide charges of a MOS structure (type 1) under 0V gate voltage after an irradiation (X-ray) of about 1 Mrad determined by flat band voltage shift (CV-measurement).

The flat band voltage shift can also be expressed as a function of time in linear form instead of logarithm form (Figure 6.46). It appears as an exponential decay with an exponential time constant τ.

As discussed above, tunnel annealing at room temperature can be somehow accelerated under positive gate voltage compared with zero gate voltage during annealing and be retarded under negative gate voltage, since tunneling charge carriers are electrons from silicon surface into the Si/O interface.

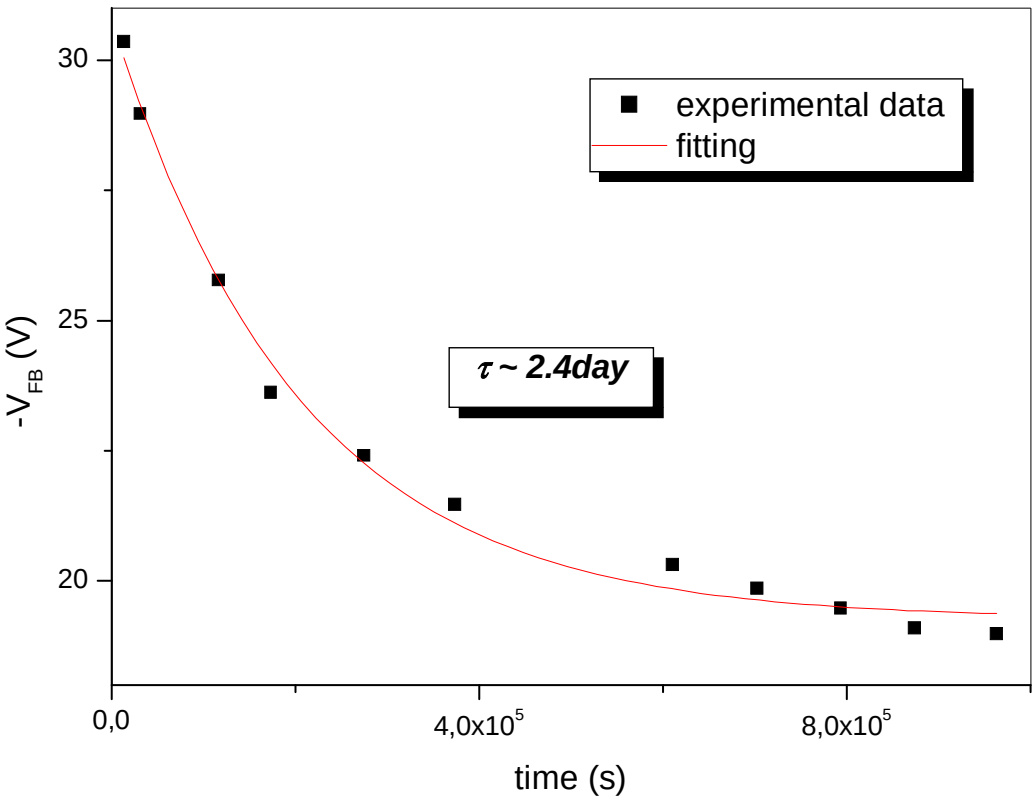


Figure 6.47 Annealing of the positive oxide charges of a MOS structure (type 1) under -5V gate voltage after an irradiation (X-ray) of about 1 Mrad determined by flat band voltage shifts (CV-measurement).

Figures 6.46 and 6.47 show the exponential decay form of the flat band voltage shift of a MOS structure under different gate voltages. The time constant changes from about 35h (about 1.5 days) under 0V to about 2.4 days under -5V.

For an MNOS structure, the tunnel annealing process will be decelerated under both zero and negative gate voltage because of trapped electrons in the nitride can also be considered as negative gate voltage.

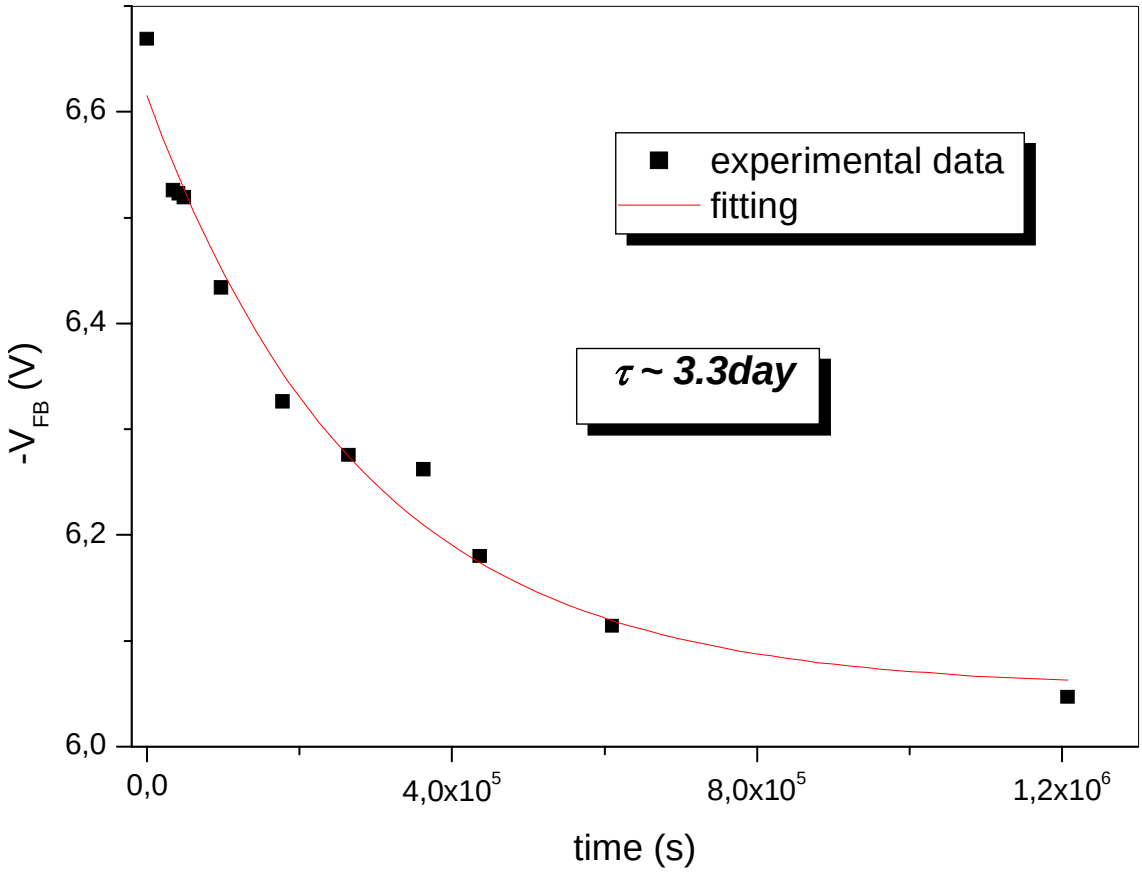


Figure 6.48 Annealing of the positive oxide charges of an MNOS structure (type 2) under 0V gate voltage after an irradiation (X-ray) of about 1 Mrad, which is determined by flat band voltage shift (CV-measurement).

In Figures 6.48 and 6.49, the measured flat band voltage shift as a function of time after irradiation is plotted. The time constant τ is here about 3.3 days under 0V and -5V.

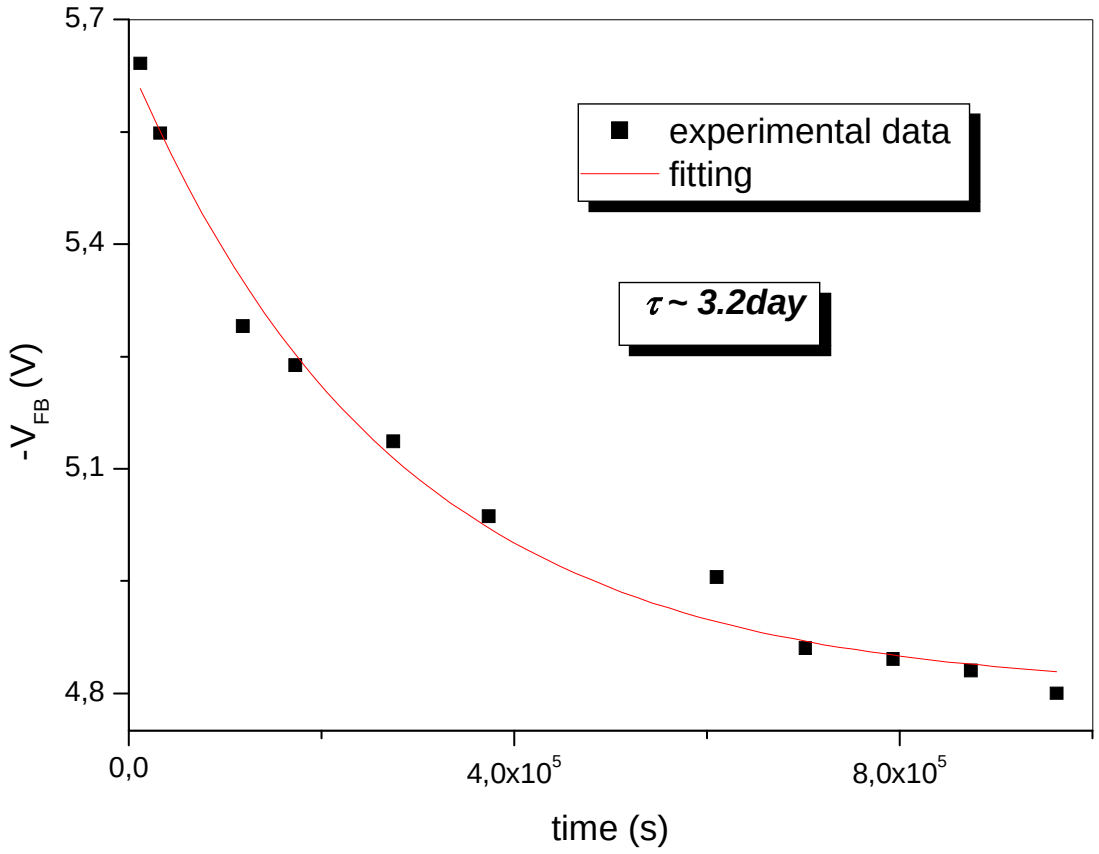


Figure 6.49 Annealing of the positive oxide charges of an MNOS structure (type 2) under -5V gate voltage after an irradiation (X-ray) of about 1 Mrad, which is determined by flat band voltage shift (CV-measurement).

Figure 6.50 shows that the annealing process of a MOS structure (with 100nm oxide) and an MNOS structure (with 100nm oxide and 10nm nitride) is performed directly after irradiation at room temperature under different gate biases in a certain time sequence. The first step (marked with a blue dashed line) denotes the annealing process taking place under floating state. In this case, trapped electrons in the nitride layer can be considered as a negative voltage applied on the gate contact that will decelerate the tunnel annealing for an MNOS structure. The second step represents that a gate voltage (+5V) is applied during the annealing process, and thus this process is accelerated for MOS but not for MNOS. In the third step the gate voltage is changed from +5V to +10V, and it is found that annealing process is accelerated for both structures, since the applied gate voltage is high enough to compensate the electron trapping effect for an MNOS structure. Finally the annealing process is performed under 0V, and the annealing process for MNOS is retarded again due to electron trapping effect.

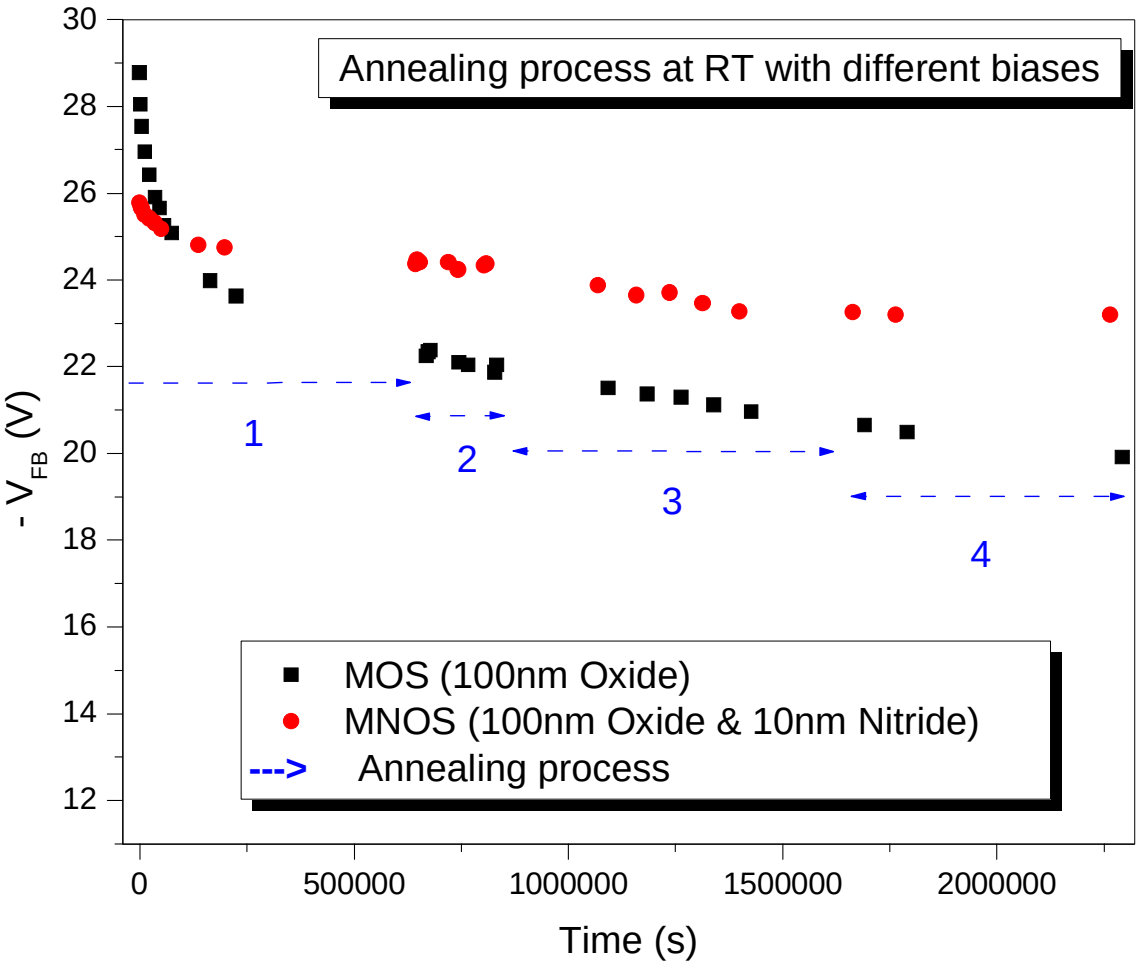


Figure 6.50 Annealing processes of a MOS (type 6) and an MNOS structure (type 8) under room temperature under different gate biases. The flat band voltage shift is plotted as a function of time.

6.9 Surface damages affected by other factors

In general, the surface damages depend on many factors, in addition to a couple of parameters discussed in the previously section the following factors will also take effect in different manners:

- Oxidation processing: In order to produce radiation hard MOS devices, a good quality of oxide does play an important role. For this reason, a great deal of attention should be paid to the improvement of oxidation parameters for the oxidation processing. It is already well known that silicon lattice orientation can

make a major contribution to the radiation hardness of oxide layers, i.e., if <100> orientated silicon material is used as the substrate of MOS devices, the surface damage can be reached by an order of magnitude (of at least 10) due to different silicon atom density. In addition, other factors; e.g., oxidation temperature, annealing temperature and gas. In this case especially the hydrogen temper process becomes significantly important at the end of the oxidation processing, since electric active silicon bonds that serve as interface traps can be saturated with hydrogen and are, thus, electric inactive.

  - Within the scope of this thesis, the oxide used is mainly thermal oxide, which involves dry oxidation or wet oxidation. The only difference between these two oxidation processes is the different reaction object: oxygen or water (water vapor). In general, the oxide produced by dry oxidation exhibits better radiation tolerance comparing with that by wet oxidation, since silicon hydrogen complex can be built up through wet oxidation, for instance, Si-OH or Si-H-Si or Si-H, which can contribute to the interface traps as mentioned previously. In other words, the released hydrogen due to irradiation is a major source of protons that turn finally into interface traps. Within the scope of this thesis, MOS devices with oxide layer produced by dry oxidation are studied.

- Annealing process (during and after the irradiation – tunnel annealing) can reduce surface damages at room temperature. It has already been observed experimentally that the positive oxide charges can be partly recovered due to tunnel annealing after irradiation at room temperature. Another component of surface damages namely interface traps might also be annealed at elevated temperature because of thermal annealing (during processing).

- Cooling down might be also useful for the minimization of noise and the thus improved signal noise ratio with respect to the performance of the MOS devices.

6.10 Radiation hardness

To data the radiation responses of MOS materials or devices due to total ionizing dose (TID) have been reviewed. Generally, the physical processes about the radiation damages and damage mechanism are really complex, with many parameters involved. However, the studies of the mechanisms have been achieved markedly, and a better understanding of radiation effects on MOS devices could help to improve the radiation hardness of detectors for the application in high energy physics, e.g., the DEPFET-based vertex detector used at ILC.

Taking into account ionizing radiation on MOS devices, a summary of descriptions about the whole physical generation processes of radiation damages as well as their mechanism are given in Figure 6.52, by which radiation damages due to ionizing radiation on MOS devices can be systematically analyzed in order to achieve better radiation hardness. With respect to radiation hardness a lot of attention should be focused on the following points for hardening:

A. For oxide processing

1. Using <100> silicon substrate

   à To lower defect density

2. Oxy-nitride instead of oxide (e.g. MNOS)

   à To compensate hole trapping using electron trapping in the nitride

3. Deuterium ambience instead of hydrogen [36.37.38]

   à To anneal silicon bond resulting in Si-D (instead of Si-H) and to make it harder to dissociate

4. Cleaner, low-growth-temperature oxide (LTO) & optimum growth temperature around 1000 Celsius for dry oxidation

   à To reduce the density of hole traps in the oxide

5. Reduction of temperature and the amount of hydrogen (post-oxidation)
   à To minimize the possibility of dissociation of Si-H (Si-D) and the amount of hydrogen

6. Smaller device dimensions

   § Reduction of the oxide thickness (d_{ox})

   à To reduce the sensitivity of MOS structures to irradiation

   à To decrease ΔV_{th} or ΔV_{FB} (ΔV_{ox} & ΔV_{it}) ~ d_{ox}^{n} (n~2 for positive gate voltage; n~1 for zero gate voltage.)

7. Using silicon substrate material with fewer defects and contaminations

B. For the operation conditions

1. Using zero gate voltage during irradiation: recombination effect becomes dominant (distribution of hole traps (precursors) at Si/O interface).

   à Surface damage reaches its minimum value

2. Small positive gate voltage for MNOS structure (about 2-3V)

   à Effective charges trapped are electrons in the nitride

3. Annealing at RT at any time (weak annealing)

   à To reduce surface damage to a small extent (time constant of recovery ~ a few days)

4. Irradiation up to a few hundreds kilorad

   à Surface damage starts to increase slowly and begins to saturate

Concerning MOSDEPFET used as vertex detector at ILC, the following points should be considered according to hardening:

- Choice of material and processing should be done as in (A)
  - Small dimension - Thinner oxide layer (~100nm)
  - Better oxide quality with lower defect (Thermal oxide)
  - Radiation hardness due to nitride layer (~10nm) (electron trapping)
- MOSDEPFET stays mostly in "off" state (B)
  - Lower surface damage due to zero gate voltage
  - Radiation tolerance (discussed in Chapter 1) around a few hundreds kilorad corresponding to > 5 years

MOS-devices (~ 1Mrad X-ray)	V_{FB} (V_G = 0)	V_{FB} (V_G < 0)
MOSDEPFET (d_{ox}/d_{ni}=180/30 nm)	~4-5V	~6-7V
MOS-capacitance (d_{ox}/d_{ni}=100/10 nm)	~2-3V	~3-4V

Table 6.7 The flat band voltage shift between MOSDEPFET and MOS-capacitance is compared under different gate voltage after about 1Mrad irradiation.

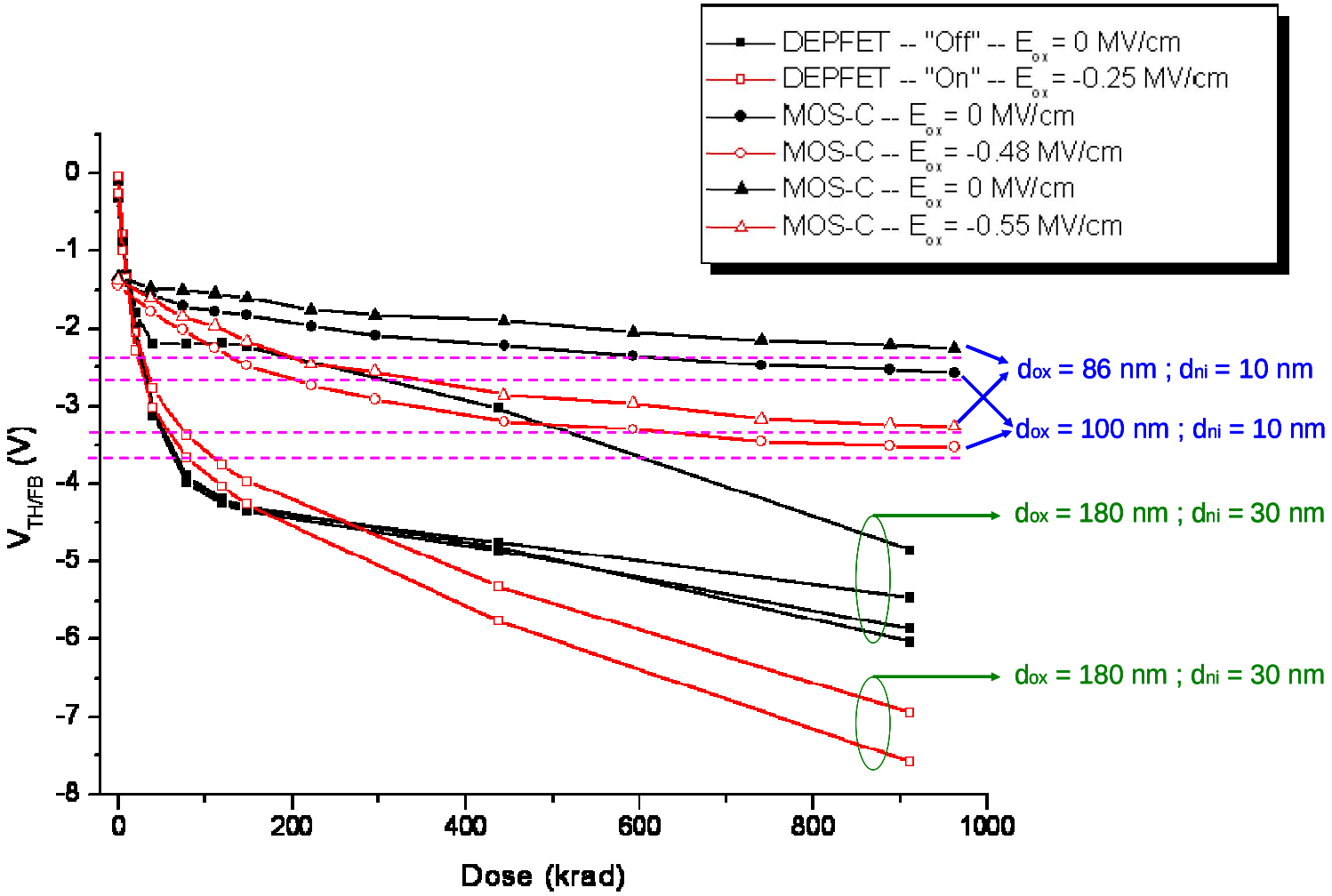


Figure 6.51 Threshold voltage shifts of DEPFETs and Flat band voltage shifts of MOS-C as a function of radiation dose. Squares denote data of DEPFETs (Red: irradiation under the influence of negative electric field – "ON"; Black: irradiation for zero electric field – "OFF"). Triangles and circles describe data of MOS-C with different dielectrics composition. Pink lines present the saturation values corresponding to the irradiation on MOS-C.

It is experimentally observed that an MNOS structure with 100nm oxide and 10nm nitride with Vg = 0V has better radiation tolerance against X-ray (~ 20KeV), i.e., V_{FB} is around 2~3V; N_{ox} is around $4*10^{11}$ cm^{-2}. Since the number of e-h pairs generated by irradiation in the oxide is about $8*10^{13}$ $/cm^2$, the trapped charge in SiO_2 is extremely low at about 0.5%.

Finally to summarize the feasibility of DEPFET-based vertex detector at ILC, one could find that firstly the shift of threshold voltage caused by radiation-induced charge build up in the oxide and interface region is about 5V up to around 1Mrad, which can be reduced by a reduction of the dielectrics layer (Table 6.7). As shown in the Figure 6.51 threshold voltage shifts of DEPFETs and flat band voltage shifts of MOS-C as a function of radiation dose are given. Squares denote data of DEPFETs (Red: irradiation under the influence of negative electric field – "ON"; Black: irradiation for zero electric field – "OFF"). Triangles and circles describe data of MOS-C with different dielectrics composition. Pink lines represent the saturation values corresponding to the irradiation on MOS-C. In principle, this shift can be easily compensated by lower gate switcher voltage. Secondly, build up of interface traps at Si/O result in an increased subthreshold slope and possibly a higher low-frequency noise. However, there is no change of transconductance g_m measured by subthreshold technique after about 1Mrad Gamma-ray irradiation (Figure 6.36) due to a lower mobility of the charge carriers in the channel, which arises from the bearable small amount of the interface traps; thirdly, it is still acceptable that up to 1Mrad gamma-ray irradiation adds only about 2 e^- noise at long shaping times (Figures 2.6 and 6.37), this noise can also be reduced by cooling; fourthly, the measured internal amplification g_q agree very well with simulation (Figure 2.3). Combining the above notes for radiation hardness (e.g. thinner oxide, zero biasing etc.), radiation tolerance against ionizing radiation could be further improved. For this reason, MOS-type DEPFET with its spectroscopic performance and better radiation hardness can serve as a promising candidate to fulfill the challenging requirements for the vertex detection at the ILC.

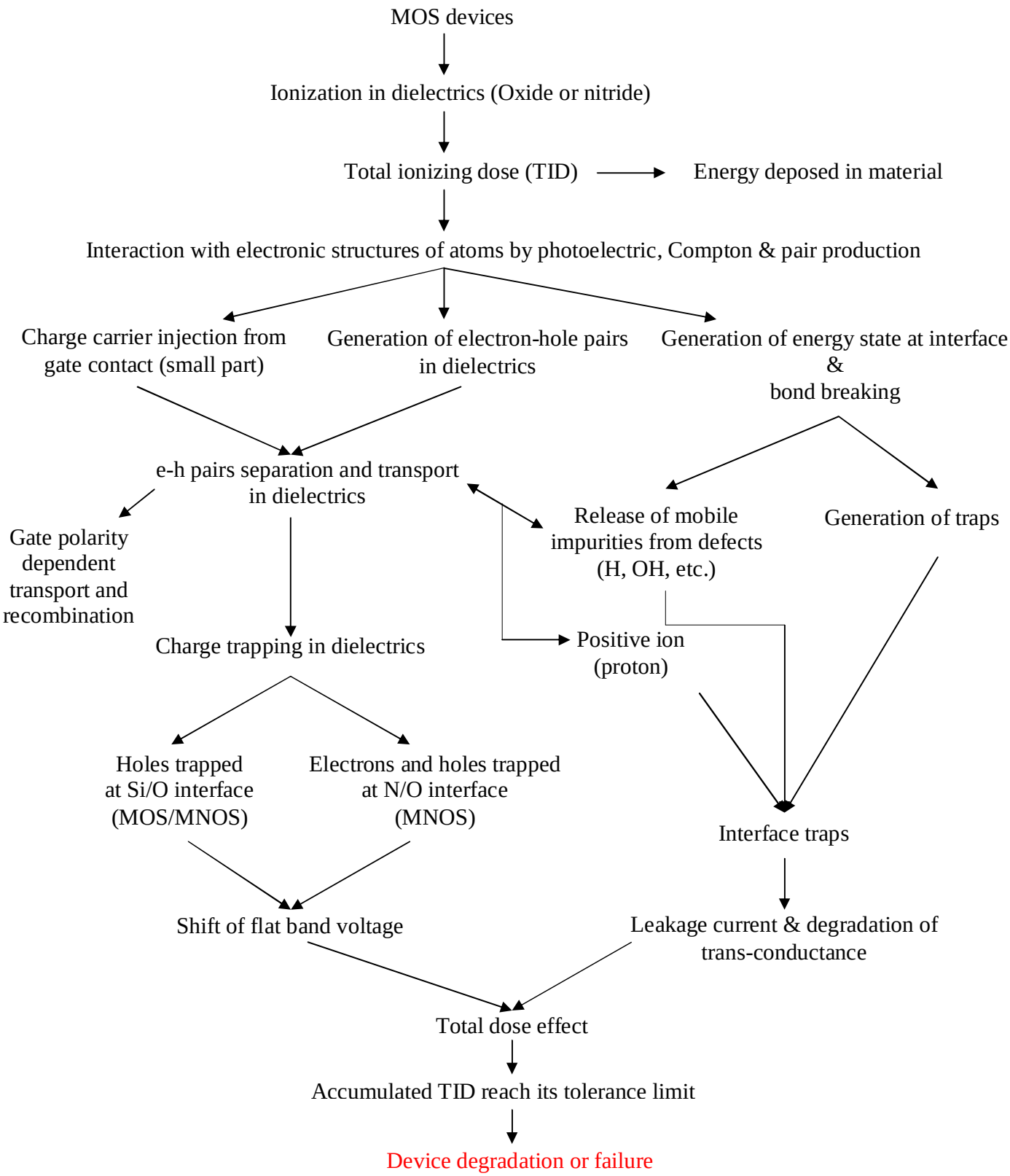


Figure 6.52 Schematic diagram illustrating the possible processes by which ionizing radiation on an MOS device results in the surface damages.

In this chapter a large number of irradiation experiments on the MOS devices are performed, by which many data are collected for the following analysis. Various radiation effects in MOS- and MNOS devices are analyzed for different combinations of oxide and nitride thicknesses: like radiation dose dependent saturation of radiation damage, thickness- and bias dependence, especially the improved radiation hardness through additional nitride layer and annealing effect, etc. Many results agree very well with literature: like square dependence of oxide thickness under positive biasing condition and gate voltage dependent flat band voltage shift, etc. Finally, a model is given to predict the flat band voltage shift as a function of total dose of a MOS device. Based on this analytical model the physical mechanism of the radiation induced damage can be studied. Moreover, several approaches are summarized for the optimized radiation hardness of MOS devices. It is worth mentioning that the highlight of this thesis is focused on the nitride layer, since an improvement of radiation hardness of MOS devices is really achieved by this layer compared to the MOS devices without nitride layer: this nitride layer explains the results unexpected — low amount of threshold voltage shift (about 4~5V) of the DEPFETs, which from literatures (Figure 4.7) would have been much higher. In the future, experiments are required to be systematically performed for the research of the transport of electrons and holes as well as charge trapping and traps distribution in the nitride. One can accordingly achieve a better combination of the thickness of nitride and oxide to further minimize the radiation damages. Finally an improved radiation hardness of detectors for even higher irradiation fluence can be achieved.

Chapter 7 Conclusion and Outlook

To date the proton-proton collider (LHC) has already been installed at the European Laboratory for Particle Physics at CERN in Geneva, while it is still not decided where and when to install the international linear collider (ILC). However, this electron-positron collider, the ILC should be constructed and operated as the next major project of the particle physics. Using unprecedented technology the ILC would complement the LHC ideally. Using knowledge discovered at the LHC (finding machine), the ILC (precision machine) could provide more accurate measurements. The vertex detector and calorimeter are two challenges in the ILC. Especially, many requirements of the technology for the vertex detector are needed. The innermost component of the vertex detector has to be placed as close to the interaction point as possible. For this reason, radiation hardness of the materials and high resolution must be fulfilled. The vertex detector consisting of five layers could provide a clear identification of the spatial coordinates of the particle tracks.

MOSDEPFET is one of the most possible detector candidates for the ILC due to its challenging advantages, by which particle detection and signal amplification can be simultaneously fulfilled using integration of a field effect transistor in a fully depleted silicon detector, where charge generation and collection take place. Using thinning technology proposed by staff at the Semiconductor Labor Munich, the DEPFET detector can be produced on fifty-micrometer-thick detector devices that still provide an excellent signal noise ratio. Moreover, it can reduce not only the multiple scattering effects but also the requirement on cooling. Of major importance is the radiation hardness of MOSDEPFET at the ILC under the dominant background, which can be achieved by improving oxide quality of the MOS structure. For this reason, the main goal of this thesis is firstly to study radiation damage mainly due to ionizing radiation, and then to understand the physical damage mechanisms; furthermore to provide a set of comprehensive analysis about radiation damage as a function of total ionizing dose (TID) and finally to find solutions to optimize the radiation hard detectors for high energy physics. For this purposes, a systematic study of ionizing radiation effects on MOS devices are performed such as MOS-capacitance, MOS-DEPFET and MOS-Gate-Diode.

Within the scope of this thesis, surface damages are generated due to ionizing radiation using X-ray of 17.44KeV that are produced by CaliFa facility in Munich and X-ray setup of around 20KeV in Forschungszentrum Karlsruhe. The energy of X-ray is high enough to penetrate the full depth of oxide films but too low to produce bulk damage in silicon volume. In addition, proton and neutron irradiation are performed to produce both surface and bulk damages.

A systematic and comprehensive analysis of radiation effects of surface damages results in the following conclusions. Generally, MOS devices are susceptible to ionizing radiation and thus the performance parameters will be degraded, i.e., from the macroscopic point of view, they will undergo a shift in threshold voltage (V_T) or flat

band voltage (V_{FB}), a degradation in transconductance and in signal to noise ratio. All of these can be traced back to the surface damages that are generated in the oxide layer and its interface region.

The surface damages are made up of trapped charge in the oxide, interface traps and oxide bulk traps. Due to improved oxide technology the last one can be controlled to a lesser extent. After electron-hole pairs are generated by the deposed energy in the oxide, they can recombine within the oxide or be transported through the oxide. As electrons drift out of the oxide with a much higher mobility compared with holes, holes undergo a complicated stochastic hopping process, and can be partly trapped that result in a positive oxide charges. In addition, a fraction of holes will drift further to the interface and react with electrons and defects to create interface traps that have three different charge states: positive, negative and neutral depending on the energetic location within the silicon band gap. Since an electron has a relative small capture cross section, the dominant charge trapping within the oxide is hole, whereas nitride exhibits the charge storage characteristic for both electrons and holes. Within this thesis the effective charge in the nitride is electron. The generated surface damages are not permanent in MOS devices but changing with time after irradiation. This time-dependent phenomena are called annealing processes that depend on the temperature and bias conditions on the gate contact of MOS devices. In general, tunnel annealing does play an important role at room temperature, while thermal annealing takes effect at the elevated temperature of above 100 Celsius. Furthermore, positive gate voltage will accelerate the annealing process, whereas an effective negative gate voltage will retard annealing.

Surface damages can be studied by different measurement techniques associated with MOS devices. For example, concerning MOS capacitance, positive oxide charges are measured by the shift of flat band voltage using HF CV technique, while interface traps are determined by combined high-low-frequency CV measurement, gate diode technique for gate diode and subthreshold technique for DEPFET. Based on models for oxide damages proposed by Dimaria and Mclean previously, a new systematical analysis with these models are made for the combined dielectrics layer (nitride & oxide) that provide a better solution to radiation hardness of MOS devices. Based on the models proposed in this work, radiation damages as a function of the radiation dose can be fitted with the exponential function up to about 1Mrad. Radiation damages can be predicted for the radiation dose more than this value (D>1Mrad) by an extrapolation of this function (Equation 6.6) (Figure 7.1).

Since the number of electron-hole pairs can be determined by the amount of energy deposed in the oxide, surface damages should be proportional to the radiation dose. As mentioned above, it increases as exponential dependence and begins to saturate at dose higher than 1Mrad. Although various irradiation facilities provide different radiation dose rate, and thus the surface damages direct after irradiation is determined to a different level, there is still no real dose rate effect observed after a period of time (annealing). It is of major importance that the amount of surface damages depends on the applied gate voltage – more exactly the electric field. In the case of zero gate voltage surface damages can reach their minimum value. On the contrary, the maximum is achieved by positive

gate voltage. Nevertheless, using an MNOS structure instead of a pure MOS structure, the flat band voltage shift is reduced at most by a relatively small positive gate voltage (around 2-3V for an effective oxide thickness of about 100nm).

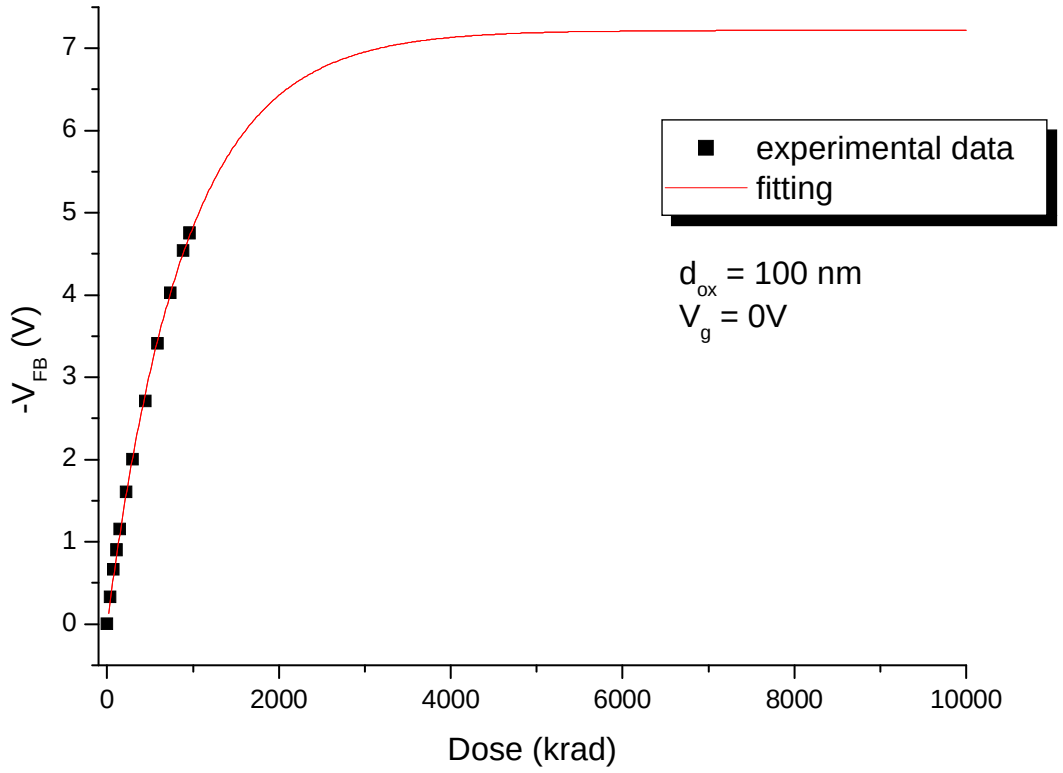


Figure 7.1 flat band voltage shift as a function of radiation dose (black points) on a MOS capacitor (type 7) with 0V biasing. The saturation point is extrapolated to 10Mrad.

Through a thorough analysis and understanding about radiation damage mechanisms and the associated radiation effects, radiation hardness of the MOS devices is further optimized by the following conclusions. It can be classified into two categories: the first is the extern, i.e., independent of MOS devices, like bias condition, radiation dose and dose rate; the second is the intern depending on MOS devices, like choice of material and oxide processing history. Among them it is worth mentioning that nitride layer can improve the radiation hardness of MOS devices. Based on the analysis about radiation damages on the MOS devices, MOSDEPFET could be an optimal option for the vertex detector at international linear collider with a large number of advantages especially in radiation hardness.

Appendix A Frequency dependency of CV measurement before and after irradiation

In order to evaluate a MOS structure, capacitance voltage measurements can provide much information about this structure. To better understand CV measurements one has to firstly realize a frequency dependence of the measurement. This frequency dependence occurs primarily in inversion since the minority carriers require a certain time to generate in the inversion layer, and accordingly they cannot follow the highly changing AC voltage signal.

High frequency measurements are used to determine the positive oxide charges of a MOS capacitance. In order to avoid the influence of interface traps it should generally be performed at a frequency as higher as possible. However in the real case it is experimentally available up to 1 MHz. In case the frequency of HF CV measurement is not high enough that still a part of interface traps can contribute to flat band voltage shift that will lead to incorrect determination of positive oxide charges, i.e., it is mostly overestimated. Moreover, it is also experimentally observed that the stretch out form of a HF CV curve can result in wrong readout of the flat band voltage shift.

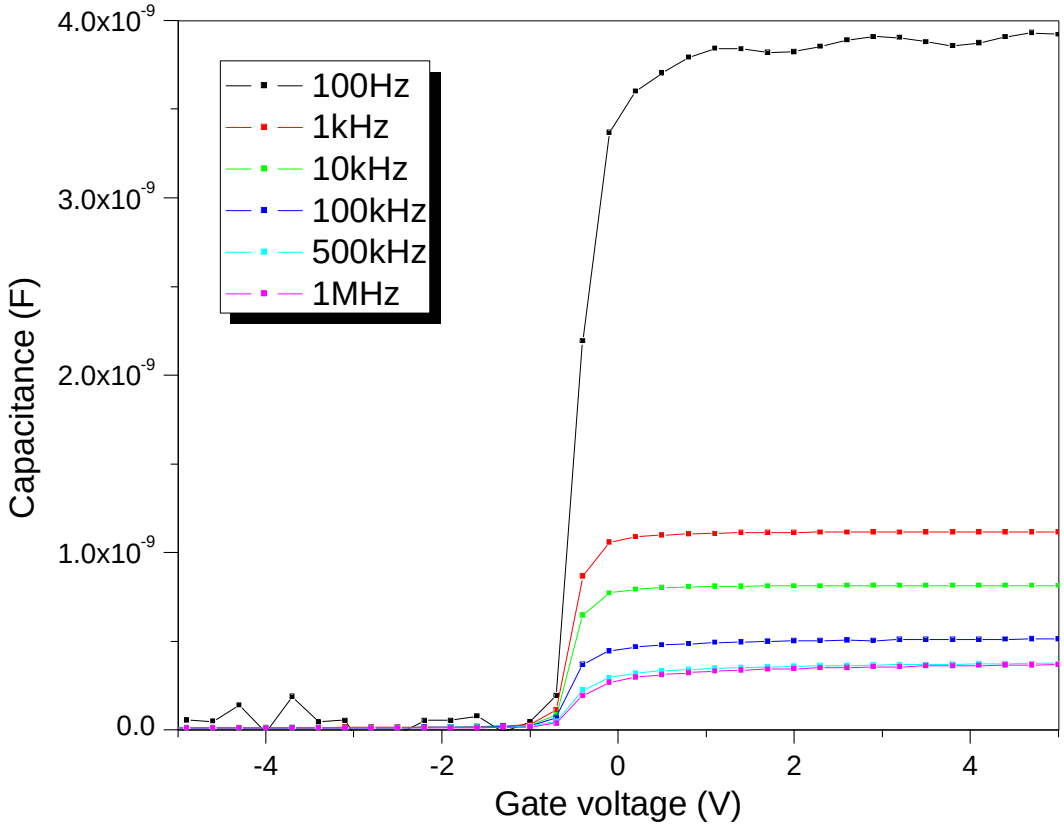


Figure A1. Frequency-dependent capacitance voltage measurement of a MOS capacitance before irradiation.

In addition it is practically impossible to use the CV measurement at such high frequencies above 100 kHz, since the capacitance value measured in accumulation is not equal to oxide capacitance as expected due to both high backside resistance [22] and high measurement frequency. Within the scope of this thesis, high-frequency CV measurement is normally performed at 10 kHz. As shown in Figure A1, CV curves of a MOS capacitance have been measured before irradiation as a function of measurement frequencies (from 100 Hz to 1MHz). A significant large frequency-dependent difference of capacitance value in accumulation can be found, while an enlarged view of Figure A1 is depicted in Figure A2 within the flat band region.

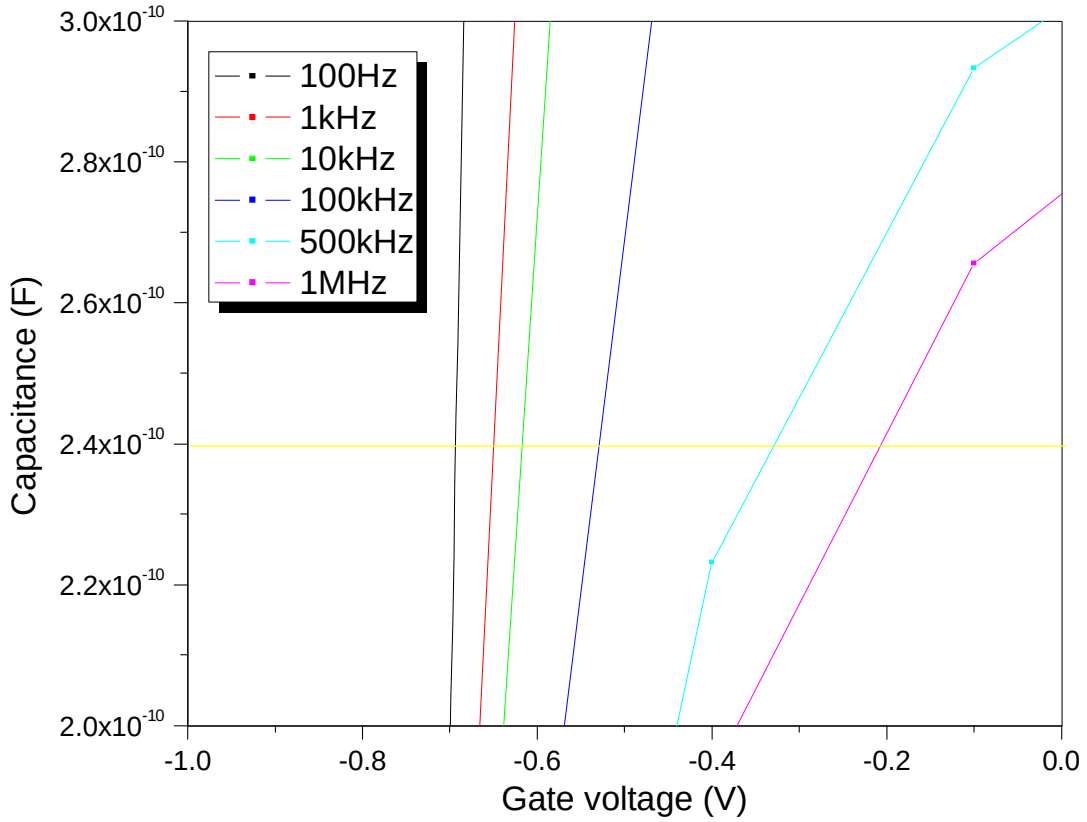


Figure A2. Enlarged view of Figure A1.

It is obviously observed that the frequency-dependent CV characteristics at above 100 kHz shows a degradation both in accumulation and in depletion most probably due to the high resistance of the silicon substrate. In order to evaluate the surface damages, it is of major importance to readout the flat band voltage for the determination of positive oxide charges using HF CV measurement. As discussed previously it is determined by the corresponding flat band capacitance that is marked by the yellow straight line in Figure A2. A relative small difference between the true flat band voltage and the value extracted from the curves is obtained at smaller frequencies like 10 kHz and 1 kHz, which is below 0.1V. Obviously, this systematic error is completely negligible.

After an X-ray irradiation of about 1Mrad CV measurements are performed on the MOS capacitance of the same one used before that is shown in Figure A3.

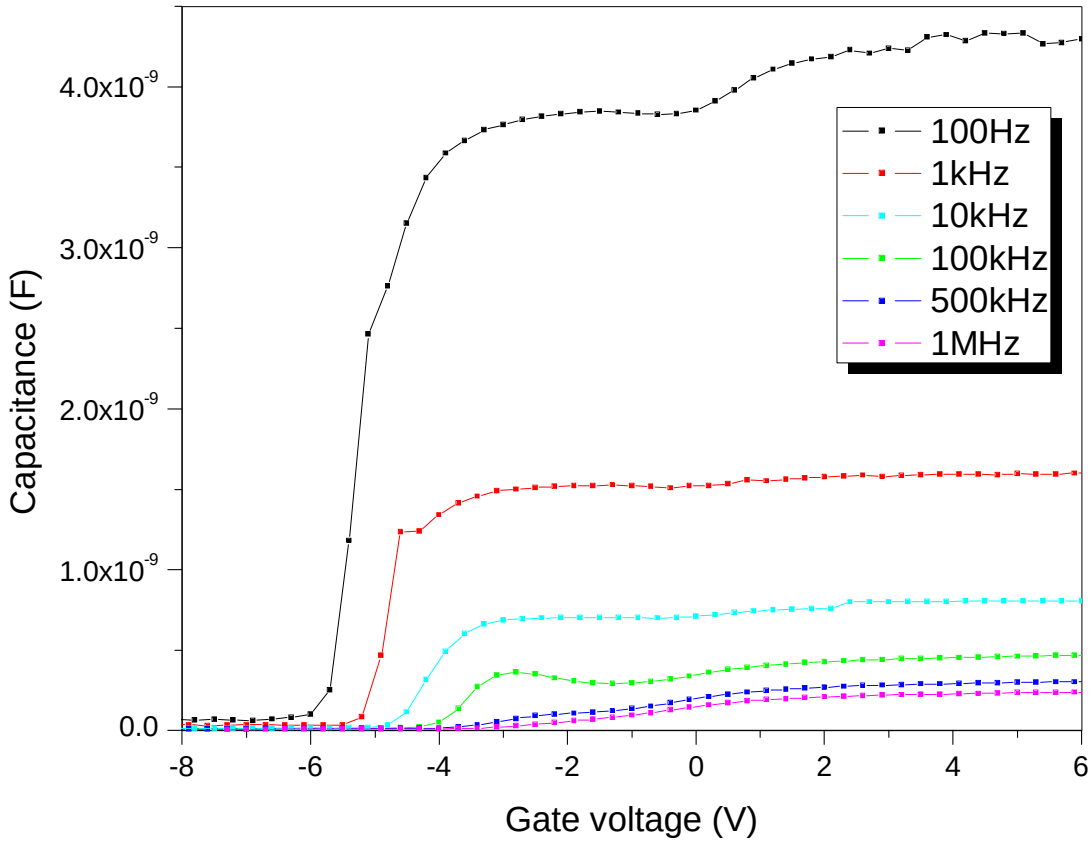


Figure A3. Frequency-dependent capacitance voltage measurement of a MOS capacitance after irradiation of about 1Mrad.

It is observed that all characteristics CV curves are shifted to more negative value along the x-axis due to positive oxide charges compared with unirradiated MOS capacitance. Furthermore, frequency-dependent CV curves are separated to a large extent in depletion. The corresponding flat band voltage strongly varies depending on the measurement frequencies. An enlarged view in depletion associated with flat band voltage is given in Figure A4. The difference in flat band voltage measured between 100 kHz and 10 kHz is below about 0.8V, which is not negligibly small compared with the true value of about 4V and should thus be considered. The CV characteristics at higher frequencies above 100 kHz look almost flat, by which the flat band voltage is not correct any more. In summary, the systematic errors arising from frequency-dependent CV measurement are negligibly small before irradiation but have to be considered after irradiation.

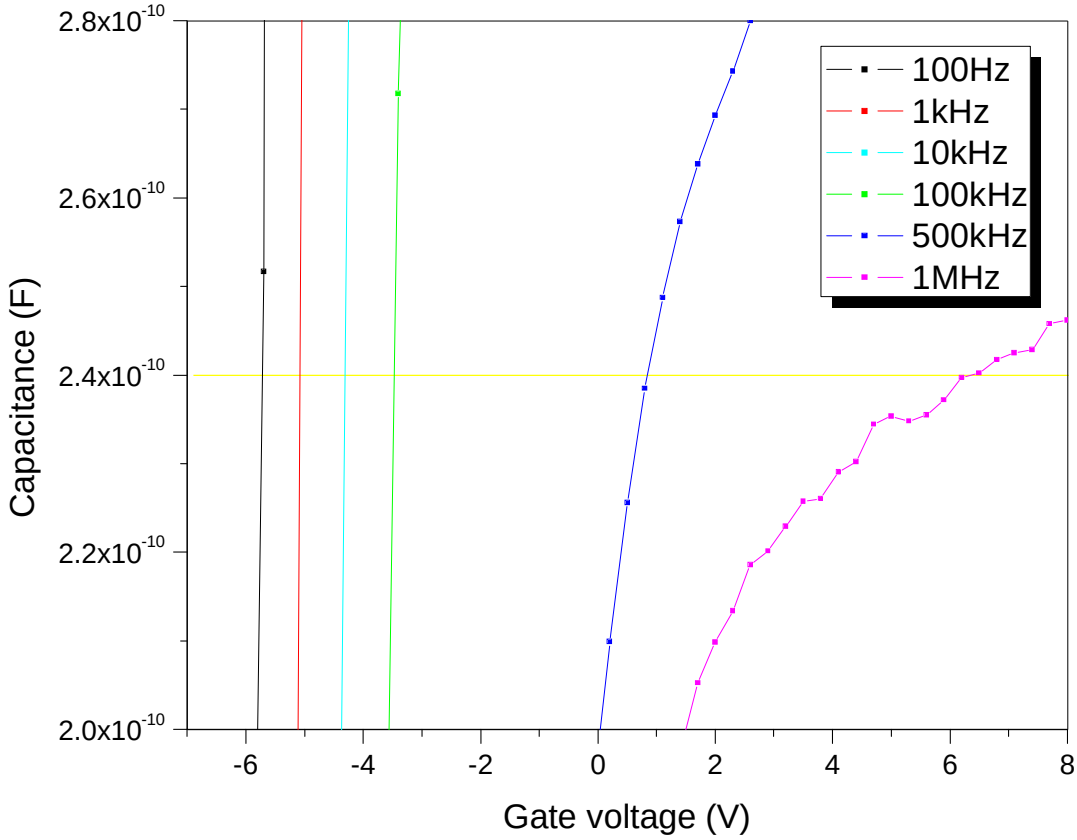


Figure A4. Enlarged view of Figure A3.

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Symbol	Bedeutung	Einheit
A	Area of gate contact	cm^2
C	Capacitance	F
C_F	Flat band capacitance of silicon	F/cm^2
C_{FB}	Flat band capacitance	F/cm^2
C_{it}	Capacitance of interface traps	F/cm^2
C_{ox}	Capacitance of oxide	F/cm^2
C_{ni}	Capacitance of nitride	F/cm^2
d_{ox}	Oxide thickness	nm
d_{ni}	Nitride thickness	nm
E_C	Energy of conduction band	eV
E_F	Fermi energy	eV
E_g	Energy band gap	eV
E_w	Photon energy	eV
E_i	Intrinsic energy	eV
ENC	Equivalent noise charge	
E_V	Energy of valence band	eV
f_e	Fluency of electron	$cm^{-2}s^{-1}$
f_h	Fluency of hole	$cm^{-2}s^{-1}$
F	Fano factor	
FWHM	Full Width Half Maximum	eV
g_m	Trans-conductance	1/Ω
I	Current	A
I_L	Leakage current	A
I_g	Generation current	A
L_D	Debye length	cm
m_{eff}	Effective masse	kg
ne	Concentration of electron	cm^{-3}
N_D	Doping concentration of donator	cm^{-3}
n_e	Number of signal electron	
n_{ht}	Trapped hole	cm^{-3}
$\overline{N_{ht}}$	Hole trap (precursor)	cm^{-3}
N_i	Intrinsic concentration of electron	cm^{-3}
q	Elementary charge	C
N_{ox}	Positive oxide charges	cm^{-2}
N_{it}	Interface traps	cm^{-2}
R	Resistivity	Ω

s_0	Surface recombination velocity	cm/s
t	Time	s
T	Temperature	K
U	Voltage	V
V_{FB}	Flat band voltage	V
V_G	Gate voltage	V
V_{th}	Thermal velocity	cm/s
W	Energy of pair production	eV
W	Width of space charge region	µm
W_m	Maximal width of space charge region	µm
E	Electric field	V/cm
E_{ox}	Electric field of oxide	V/cm
E_{ni}	Electric field of nitride	V/cm
B	Parameter of tunnel barrier	nm^{-1}
Λ	Wave length	m
λ_t^{-1}	Characteristic length	nm
μ_n	Mobility of electron	$cm^2V^{-1}s^{-1}$
μ_p	Mobility of hole	$cm^2V^{-1}s^{-1}$
σ_h	Capture cross section of hole	cm^2
σ_e	Capture cross section of electron	cm^2
σ_{eff}	Effective capture cross section	cm^2
τ_g	Generation lifetime	s
τ_r	Recombination lifetime	s
φ_m	Work function of metal	V
φ_{ms}	Difference of work function between metal and semiconductor	V
φ_S	Work function of semiconductor	V
Ψ	Potential	V
Ψ_B	Volumen potential	V
Ψ_S	Surface potential	V
ε_0	Dielectrics constant of vacuum	F/cm
ε_{ox}	Dielectrics constant of oxide	F/cm
ε_{si}	Dielectrics constant of silicon	F/cm
ε_{ni}	Dielectrics constant of nitride	F/cm
k_B	Boltzmann constant	J/K

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Erklärung

Hiermit erkläre ich, daß ich die vorliegende Doktorarbeit selbständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt, sowie Zitate und Ergebnisse Anderer kenntlich gemacht habe.

München, 30.10.2008	Wei, Qingyu
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Ort, Datum	Unterschrift