Enhanced Prediction of Energy Losses during adiabatic Charging

A. Schlaffer, J. A. Nossek
Institute for Network Theory and Circuit Design
Technical University of Munich
Arcisstr. 21, D-80290 Munich
E-Mail: Andreas.Schlaffer@nws.e-technik.tu-muenchen.de

Abstract

Since its more general introduction, adiabatic charging [1] has been considered to have a more or less unlimited potential to reduce the power consumption of a CMOS circuit. The prediction was that when reducing operation speed the power consumption could be decreased unlimited, in extreme down to zero. However, if *static losses* are considered, too, a limit for the achievable minimum power consumption occurs, stating an *optimum charging time* with minimal power consumption, that is different from infinity, in opposition to the well known considerations used up to now.

A linear network model giving the reason for such losses is introduced in this article, together with a closed formula for the prediction of the power consumption of such a circuit. From this formula the optimum charging time and minimal power consumption can be derived, in closed form, too. Further on it is shown, that for such circuits with static losses the well-known linear charging ramps do no longer form the optimal waveform for charging with low losses. These waveforms can be derived by variational calculus.

By comparing the predicted energy losses to simulation results gained by using the models of a standard CMOS process it is shown that the linear model holds in the interesting range of charging times, giving a rather precise description.

1 Introduction

The main idea of adiabatic charging is based on a circuit like shown in Fig. 1. Whenever the capacitor is charged or discharged through a resistor abruptly, an unavoidable amount of energy

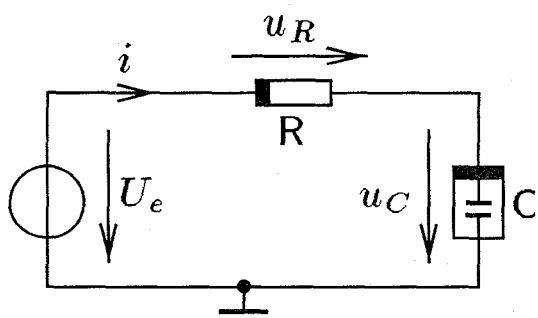

Figure 1: CMOS charging model

$$E_{diss} = \frac{1}{2} C U_H^2; \tag{1}$$

is dissipated in the resistor. If, however, the capacitor is not charged abruptly, but following a voltage ramp with the duration T, the losses reduce down to

$$E_{diss} = \frac{RC}{T} C U_H^2. \tag{2}$$

Note that the dissipated energy can be reduced down to zero by enlarging the rise time T up to infinity.

However, in all recent works [4, 2, 6, 3] a limit for the achievable minimum power dissipation occurs, showing that for longer rise times the prediction of (2) does no longer hold.

2 Static dissipation model

The reason for this development can be searched in short-circuit paths which will cause static power dissipation as long as the supply voltage φ is turned on. Those short circuit paths occur because in realistic circuits, there will always be switched off transistors in parallel to the capacitor to be charged, like shown in Fig. 2. This circuit can be considered either a simple NOT-gate or part of a bigger logical function. For further examination we shall assume that the transmission gate initially is turned on, whereas the single NMOSFET is turned off, thus enabling the power supply φ to charge the initally discharged load capacitor.

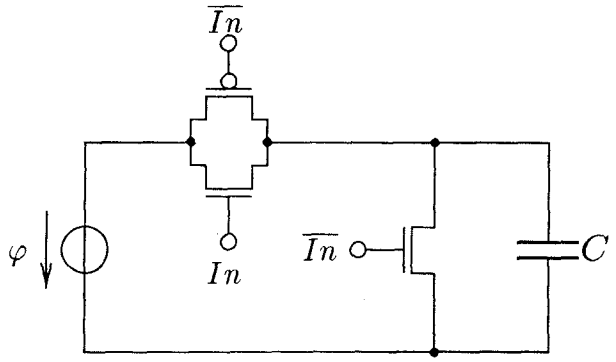

Figure 2: Charging with static dissipation

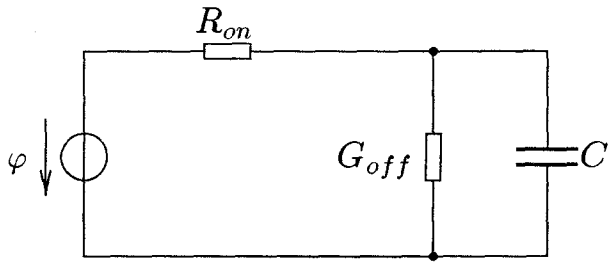

Figure 3: Linear model for charging with static dissipation

Question may arise wether the NMOSFET is truly necessary, in the adiabatic paradigm as proposed in [1] such a pull-down network is avoided. However, practical approaches show that it is unavoidable in most cases due to the following reason: If we consider the transmission gate to be turned off and the supply voltage φ to be rising, there will always be a parasitic capacitance in parallel to the transmission gate that is not negligible. Thus, if the pull-down NMOSFET is left out, we will have the case of a capacitive voltage divider, that means, that the output voltage will follow the supply, rising to a fraction to it. For dynamic logic, for example clocked logic, this effect is called "charge sharing" [5] and it will cause severe static power dissipation in following logic stages, that will be half turned on. Thus we really need those pull down transistors.

However, if we use detailed transistor equations for this model, the resulting differential equations will no longer be solvable in closed form, thus disabling us to make quantitative predictions about the performance of the circuit. If we regard measured data of the turned-on transmission gate, keep in mind that voltage drop will be rather low here, thus we can easily use linearised models, and the turned-off NMOSFET, we see that a linearised model won't be far from reality. Fig. 3 shows such a linearised model, which will be subject to further examination, this model will be called a "leaky circuit" in the following.

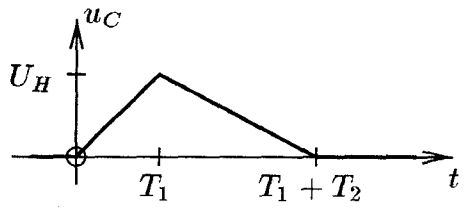

Figure 4: Triangular supply pulse

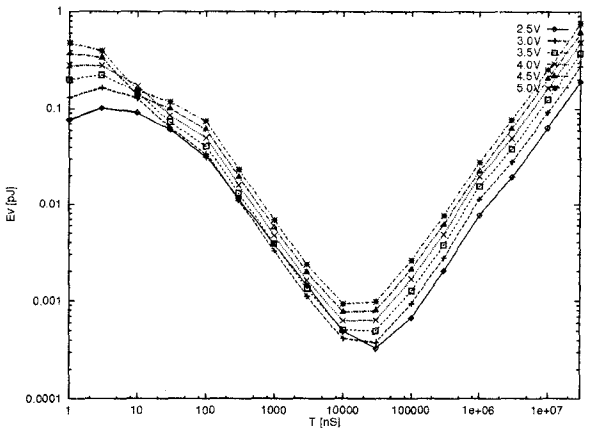

Figure 5: Power dissipation of leaky circuit

3 Power dissipation for ramping waveforms

In fact, for such a leaky circuit, the optimal charging waveform will no longer be a ramp any more. However, the ramping waveform still holds the advantage over the actually optimal waveform to be easy to realize and still improves power dissipation a lot. So the power dissipation for a leaky circuit charged by using a ramping waveform is examined in this section. Note that in most of the previous works the ramping waveform, which is an optimal solution for nonleaky circuits *only*

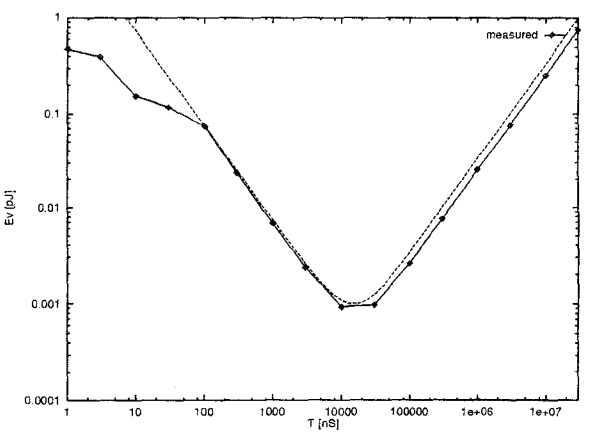

Figure 6: Actual and predicted power dissipation

for the capacitor voltage, not for the supply voltage, simply was considered the optimal waveform for the supply voltage, too. The slight error leads to the fact that the power dissipation formulae do not hold for short charging times. Nevertheless, ramps will be taken for the supply voltages here, too. Exact formulae for the power dissipation can be derived for this case, but in the region interesting for adiabatic operation they do hold no advantages over the approximations presented in the following, except being much more clumsy. It simply has to be kept in mind that the formulae do not hold for short ramp durations.

To drive the leaky circuit with ramp pulses, the capacitor voltage u_C will have the waveform of a triangular impulse

$$u_C(t) = \begin{cases} 0; & t < 0; \\ \frac{U_H}{T_1} t; & 0 \le t < T_1; \\ U_H(1 + \frac{T_1}{T_2}) - \frac{U_H}{T_2} t; & T_1 \le t < T_1 + T_2; \\ 0; & t \ge T_1 + T_2; \end{cases} \quad (3)$$

which is sketched in Fig. 4. As we will see later, the optimum slopes for charging and discharging differ, so we have to consider a different time interval for charging T_1 than for discharging T_2. If this capacitor voltage waveform is used, the expression for the power dissipated momentarily in the circuit

$$P_{diss} = R_{on}(C\dot{u}_C + G_{off}u_C)^2 + G_{off}u_C^2; \quad (4)$$

can easily be used to compute the energy dissipation. Since if u_C as well as $\dot{u}_C$ are zero the dissipated power P_{diss} is zero, too, we can limit the integration to determine the total energy dissipated E_{diss} to the interval $0 < t < T_1 + T_2$:

$$\begin{aligned} E_{diss} &= E_1 + E_2 \\ &= \int_0^{T_1} P_{diss}dt + \int_{T_1}^{T_1+T_2} P_{diss}dt. \end{aligned} \quad (5)$$

The energy E_1 dissipated during the first interval $0 < t < T_1$, that is the energy dissipated during charging, comes to

$$\boxed{\begin{aligned} E_1 &= U_H^2\Big(\frac{R_{on}C^2}{T_1} + R_{on}G_{off}C + \\ &\quad + \frac{1}{3}(R_{on}G_{off}^2 + G_{off})T_1\Big) \end{aligned}} \quad (6)$$

From the condition

$$\frac{dE_1}{dT_1} = 0; \quad (7)$$

the optimum charging time can be derived:

$$\boxed{T_{1opt} = C\sqrt{\frac{2R_{on}}{R_{on}G_{off}^2 + G_{off}}}} \quad (8)$$

For the discharging interval $T_1 < t < T_1 + T_2$, the energy dissipation E_2 is a little bit smaller, since the discharging current does not need to be delivered through the load resistor in a whole:

$$\boxed{\begin{aligned} E_2 &= U_H^2\Big(\frac{R_{on}C^2}{T_2} - R_{on}G_{off}C + \\ &\quad + \frac{1}{3}(R_{on}G_{off}^2 + G_{off})T_2\Big) \end{aligned}} \quad (9)$$

The optimum discharging time therefore is slightly longer

$$\boxed{T_{2opt} = C\sqrt{\frac{3R_{on}}{R_{on}G_{off}^2 + G_{off}}}} \quad (10)$$

As can easily be derived from (8) and (10), the ratio between T_{1opt} and T_{2opt} is constant:

$$\boxed{\frac{T_{1opt}}{T_{2opt}} = \sqrt{\frac{2}{3}}.} \quad (11)$$

If we use the optimum times both for charging and discharging, the minimum achievable power dissipation will be:

$$\boxed{E_{dissmin} = \sqrt{\frac{25}{18}}U_H^2 C\sqrt{R_{on}(R_{on}G_{off}^2 + G_{off})}.} \quad (12)$$

Fig. 5 finally shows simulation results using HSPICE on MOSFET models level 6 extracted from a real existing 1μ process. The characteristics of the transmission gate and the NMOSFET lead to the values of $R_{on} \approx 3k\Omega$ and $G_{off} \approx 2pS$. The load capacitance, consisted of a linear capacitor and the parasitic capacitances of the NMOSFET, is $C \approx 0.2pF$. This leads to a predicted optimum charging time of $T_{1opt} \approx 11\mu s$, a prediction that in fact holds. The simulation had been carried out for a number of different supply voltages and it can be clearly seen, that voltage reduction may be used *in addition* to the adiabatic charging principles to improve performance.

Note that for short charging times the formulae do no longer hold, since during the simulation not the capacitor voltage, but the input voltage was made the optimum ramp. For very short times the capacitor voltage will no longer follow this ramp, so power dissipation will start to decrease again, as can be seen in Fig. 5. However, the decrease is connected with the fact that the capacitor voltage will no longer rise sufficiently, so this region of operation has no practical use.

Finally, Fig. 6 shows a comparison between a measured curve of power dissipation, shown in a straight line with sample points, and the calculated dissipation shown in a dashed line. The curves coincide to a large degree, except the region for short ramp duration as

mentioned before, so it becomes clear that equations *(6) and (9)* are useful to describe the actual behaviour of the circuitry.

4 Conclusion

It has been shown, that for CMOS circuits with leak conductances the abilities of adiabatic principles to lower power dissipation are limited. It does no longer make sense to make the ramping time for the supply voltage "as long as possible", instead, an optimal time should be chosen. This optimal time can easily be derived from measured process data. The supply voltage may be reduced, additionally, to further decrease the dissipated power.

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