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Investigation of DEPFET as Vertex Detector at ILC
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Intrinsic properties, radiation hardness
and
alternative readout schemes

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„By three methods we may learn wisdom:
first, by reflection, which is noblest;
second, by imitation, which is easiest;
and third by experience, which is the bitterest.“
Confucius

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Abstract

The International Linear Collider (ILC) is supposed to be the next generation lepton collider. The detectors at ILC are intended to be precision instruments improving the performance in impact parameter (IP), momentum and energy resolution significantly compared to previous detectors at lepton colliders. To achieve this goal it is necessary to develop new detector technologies or pushing existing technologies to their technological edges. Regarding the Vertex detector (VTX) this implies challenges in resolution, material budget, power consumption and readout speed.

A promising technology for the Vertex detector is the Depleted Field Effect Transistor (DEPFET). The DEPFET is a semiconductor device with in-pixel amplification integrated on a fully depleted bulk. This allows building detectors with intrinsically high SNR due to the large sensitive volume and the small input capacitance at the first amplifier.

To reach the ambitious performance goals it is important to understand its various features: clear performance, internal amplification, noise and radiation hardness.

The intrinsic noise is analyzed, showing that the contribution of the DEPFET is below $50e^-$ at the required speed. Moreover it is possible to show that the internal amplification could be further improved to more than $1nA/e^-$ using the standard DEPFET technology.

The clear performance is investigated on matrix level utilizing a dedicated setup for single pixel testing which allows direct insight into the DEPFET operation, without the complexity of the full readout system. It is possible to show that a full clear could be achieved with a voltage pulse of 10V. Furthermore a novel clear concept - the capacitive coupled clear gate - is demonstrated.

The radiation hardness is studied with respect to the system performance utilizing various irradiations with ionizing and non ionizing particles. The impact on the bulk as well as the interface damage is investigated.

Up to now the readout is performed with Correlated Double Sampling (CDS), to achieve even higher readout speeds this work investigates new readout schemes to reach this goal.

The input parameters to judge the performance of the new readout methods are on the one hand the intrinsic properties of the DEPFET, internal amplification, charge handling capacity, noise and leakage current.

Besides this conceptual investigations the new readout scheme is also experimentally validated on single pixel level.

Chapter 1

Introduction

One of the great achievements of particle physics in the last century was the development of the Standard Model (SM). The fundamental forces in nature, electro-magnetism, strong and weak force are precisely described by the Standard Model. The three ingredients of the SM are the Quantum Electrodynamics (QED), Quantum Chromodynamics (QCD) and the Electroweak theory which incorporates the effects electromagnetism and of the weak force.

QED, the relativistic field theory of electromagnetism allows predicting the anomalous magnetic moment of the electron. This prediction is in excellent agreement with the experimental value to a relative precision better than 10^{-10} [34, 14, 62]. The QED thus belongs to one of the best tested theories in physics.

Quantumchromodynamics (QCD) gives insight into the interaction between quarks and gluons. The quark model allows ordering the zoo of mesons and baryons discovered in the last decades. One of the greatest achievements of the QCD is the prediction of the scaling violation of the structure functions of the nucleons. Moreover the running of the strong coupling constant was measured over a wide range of momenta, which confirmed QCD[20].

Besides this it was possible to develop a theory connecting the weak interaction and electromagnetism within the Standard Model - The electroweak theory. The electroweak theory is able to predict many observables in high energy physics like the width of the Z resonance, the relationship of the masses between the heavy vector bosons and also the parity violation of the weak force.

Even if the Standard Model is extremely successful in its predictions there are still open questions. Currently physicists all over the world are trying to find answers to the following questions:

1. How do particles acquire mass?
2. Is there an universal interaction including QED, QCD, the weak force and even gravity?
3. Are there new forms of matter like Supersymmetric particles?
4. Which is the nature of dark mater indicated by the rotation of galaxies and cosmic microwave background?

5. What is the nature of Dark Energy which currently dominates the evolution of our universe?

6. Do we live in a four dimensional world? Are there further compactified dimensions?

One important tool to answer them will be the International Linear Collider (ILC). The ILC is the next generation e^-e^+ collider which will enlighten some of these questions or measure the properties of particles discovered at the LHC with high precision.

Due to the point like nature of e^-e^+ the initial state is well defined with respect to energy and particle content. The absence of QCD background like in Hadron colliders allows building a precision instrument optimized towards excellent performance in calorimetry, tracking and vertexing.

For the vertex detector this means an excellent impact parameter (IP) resolution. This requires a reduction of the multiple scattering to a minimum by introducing a tight limit to the material budget, which implies the absence of active cooling which leads to a strong limit on the power consumption. Only cooling by cold gas stream will be possible.

Besides these requirements a high granularity is necessary to achieve a sufficient single point resolution. Even if lepton colliders are believed to be background free, there is still background due to the highly focused beams which are producing beamstrahlung photons which convert into electron positron pairs. This background leads to radiation damage in the vertex detector but also to background signals.

The pattern recognition requires that the occupancy of the detectors remains below 1% resulting in a severe limit in readout speed.

Detector used in previous experiments like silicon strip- or hybrid- detectors and CCDs will fail to fulfill at least one of the mentioned requirements. To achieve these demanding goals it is necessary to develop new detector types or push existing ones to their technological limits.

A promising technology for a Vertex detector is the Depleted Field Effect Transistor (DEPFET). The DEPFET is an intimate fusion of high resistivity silicon, thus able to be fully depleted, with an integrated Field Effect Transistor in each Pixel providing the first amplification.

The charge of a traversing particle is collected in a potential minimum under the gate of the transistor which is created via an additional implantation leading to a positive space charge. Charge collected in the potential minimum, the so called internal gate, modulates the transistor current thus resulting in a measurable signal.

This concept allows building detectors with a large sensitive volume generating a large signal for the detection of charged particles. The in-pixel amplification reduces parasitic capacitances to its minimum allowing a low noise operation.

Internal amplification To achieve the required performance with respect to the efficiency and resolution a sufficient signal to noise ratio (SNR) is required.

The signal achieved with the DEPFET depends on several parameters: the internal amplification (g_q) and the efficiency a charge could be removed from of the internal gate (clear performance). The internal amplification was investigated on several test structures, showing that a further increase of the internal amplification beyond 1nA/e^- is possible.

Clear performance The clear performance is evaluated utilizing the novel comparison method (chapter 11). The clear performance is very sensitive to the applied voltage on the clear and the clear gate. The clear gate is an additional MOS structure which provides a lateral potential barrier for the internal gate. The measurements are showing that the whole charge could be removed from the internal gate with a pulse height of 10V. However the measurement revealed a new feature of the DEPFET - a modulation of the internal amplification with the applied clear gate voltage.

Capacitive coupled clear gate In addition a new approach to improve the clear performance is investigated. The capacitive coupled clear gate (CCCG is achieved by an additional capacitor, on pixel level, which couples the clear gate to the clear. This allows reducing the barrier height between the internal gate and clearing thus improving the clear performance. The CCCG structures are showing a very promising performance and a significant increase of the signal currents.

Intrinsic noise A high SNR requires a large signal but also a sufficient small noise. The intrinsic noise contribution of the DEPFET is studied in chapter 6, taking into account a possible increase of low frequency noise due to irradiation and a possible reduction of the transconductance, showing that the contribution of the DEPFET is as low as $50e^-$ at 50MHz bandwidth.

Radiation hardness Since the DEPEFT is a Metal Oxide Semiconductor (MOS) device on a silicon substrate it is susceptible to both nonionizing as well as ionizing radiation damage. The nonionzising radiation (NIEL) damage leads to an increase of leakage current causing an additional shot noise.

The ionizing radiation causes a buildup of positive charge in the oxides leading to a shift of the operation parameters of the device. Ionizing radiation also produces an increase in low frequency noise due to an increased number of interface states. This could lead to a decreased transconductance of the transistor g_m. These effects are studied using low energetic x-rays and protons.

Measurements to access these issues are presented in chapter 14 and 15.

In addition the effects of inhomogeneous irradiation on the systems performance were investigated making use of irradiation results and the g_q measurements. The results of these studies are presented in chapter 16.

Alternative readout schemes The challenging readout speed requirements make it also necessary to investigate new possibilities to increase it. Up to now the readout is performed via the Correlated Double Sampling (CDS) which

leads to a long readout cycle since two samples and a clear pulse are needed to process a row. Alternative schemes which could substantially improve the readout speed are investigated in chapter 18. It is shown that these schemes are able to improve the readout speed and also the clear performance of a DEPFET based vertex detector.

Outlook This work shows that the DEPFET is a serious candidate for the ILC vertex detector. The most challenging issues are related to the inhomogeneous irradiation expected at ILC and the readout speed requirements. As pointed out in the chapters 14 and 15 it is feasible to preserve the excellent properties of the DEPFET over a live time of at least 5 years in the outer layers. Chapter 18 shows that the readout speed of a DEPFET based Vertex detector could be further increased utilizing alternative readout schemes.

Chapter 2

ILC Project

The strategy to answer the questions, raised in the introduction, is twofold. On the one hand by building a hadron collider with an energy reach up to 14TeV, which is able to find the first signatures of new particles and physics, on the other the ILC, which could investigate this new phenomena with great precision. While the first mentioned collider - the LHC - is already in commissioning the R&D for the ILC is still under way.

2.1 The physics case

The physics program at the ILC could be divided into two main topics - on the one hand precision measurements with already known particles and phenomena and on the other the exploration of new physics, possibly new particles from Super Symmetry (SUSY) where the ILC is able to reach a parameter space complementary to the one of the experiments at the Large Hadron Collider (LHC). The achievable precision allows also to be sensitive to new physics at even higher energy scales than 500GeV, since loop corrections which stem from new physics will already contribute at lower energies.

The advantages of a lepton collider could be summarized as follow:

- well defined center of mass (CM) energy - no energy distribution of partons like in proton collisions
- full center of mass energy available in collisions
- leptons - point like particles - in initial state - no underlying event
- well defined spin/helicity polarized beams possible and planned

Figure 2.1 shows the cross section for various processes in both pp and e^-e^+ collisions. Interesting processes in pp collisions like $t\bar{t}$ production are more than 10 orders of magnitude smaller than the total cross section while the difference in e^-e^+ is only one order of magnitude. In addition the large cross sections for jets in pp collisions are a source of irreducible backgrounds when studying

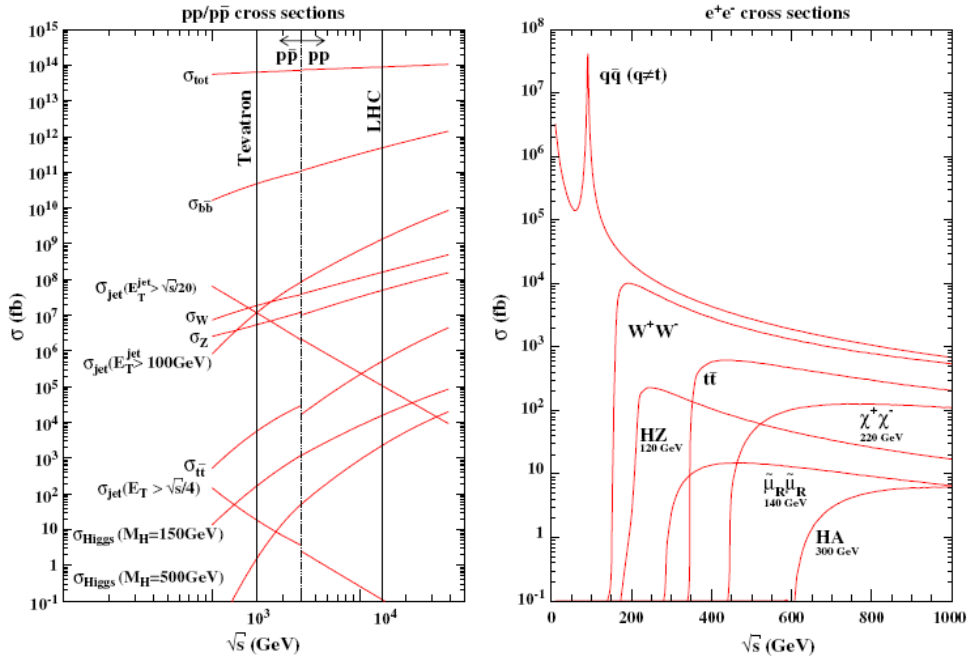


Figure 2.1: Cross section for pp and e^+e^- collisions [88]

hadronic final states, thus e^-e^+ collisions are providing a cleaner environment to study physics.

In the next paragraphs a few examples of the physics program of the ILC are introduced. More information can be found in [27, 9, 6]

The origin of mass In the standard model of particle physics it is not possible to introduce the masses terms in form $m\bar{\Psi}\Psi$ since such term are equivalent to

$$m\left(\bar{\Psi}_{right}\Psi_{left} + \bar{\Psi}_{left}\Psi_{right}\right).$$

These terms would immediately destroy the $SU(2)_L$ gauge symmetry which acts only on the left handed particles. To overcome this problem a new field is introduced in the Standard Model: the Higgs field.

The Higgs mechanism allows introducing masses for Fermions and Quarks into the SM, by coupling the Higgs field to the particles which should acquire mass. This mechanism is not able to predict the masses but it preserves the symmetry $SU(2)_L \times U(1)_Y$ and is able to describe the symmetry breaking when the potential of the Higgs field acquires a non vanishing vacuum expectation value. In addition the symmetry breaking leads to the creation of two massive Bosons, the W and Z.

The Higgs boson is the last missing particle in the SM which has not been detected yet. It is expected that it will be found at the LHC.

The ILC could provide complementary precision measurements of a light Higgs boson like the Yukawa couplings, quantum numbers, like spin and CP,

and will be able to measure the Higgs potential. The ILC will also allow a decay mode independent observation of the Higgs Boson in the Higgsstrahlungs channel $ZH \rightarrow \mu\mu X$. The ILC will allow to fully establish the Higgs mechanism.

Super Symmetry Super Symmetry (SUSY) introduces a new symmetry connecting fermions and bosons, introducing a super partner to each particle. The Super Symmetry is evidently broken since none of these particles are detected up to now.

Nevertheless Super Symmetry has some interesting features like introducing new heavy stable particles which could serve as dark matter candidate. Super Symmetric corrections to the running coupling of the SM changes them in way that the three coupling constants $\alpha_{weak}, \alpha_{strong}$ and α_{em} are becoming equal at a certain energy thus offering a possibility for unification.

The ILC will be able to probe a parameter space complementary to the LHC. The low background and the hermetical detectors will enable a precise examination of missing energy events, which is the standard signature of SUSY.

Nature of dark Matter The measurements of WMAP a precision survey of the Cosmic Microwave Background (CMB) [45], the rotation curves of galaxies and the collective motion in galaxy clusters, already observed in 1937 [94] show a strong indication that besides the common Baryonic matter a new form of weakly interacting and gravitating matter exists.

Known candidates for this problem like Neutrinos were already ruled out. Super symmetry offers a solution to this problem since it predicts new heavy, stable and weakly interaction particles in its spectrum, the so called Neutralinos. If such particles exist the ILC will be able to detect them and precisely measure their properties.

Heavy Quark Physics The ILC will allow measuring the properties of the heavy quarks with high precision. The Top-Higgs Yukawa coupling could for example be determined to 1% precision [88]. This may allow getting deeper insight into the symmetry breaking mechanism. Moreover the V_{tb} matrix element in the CKM matrix could be measured and the top mass itself could be determined precisely which is an important input parameter in many calculations.

New Physics Besides the introduced scenarios there are others including new physics besides the mainstream, like Higgs-less scenarios, extra dimensions and string theory.

2.2 The Linear collider

To achieve the energy of 500 GeV and finally 1 TeV in an upgrade scenario, a circular machine like LEP will not be able to provide the necessary energy, since accelerated charges emit synchrotron radiation. The power is given by the relativistic Larmor formula:

Figure 2.2: Niob cavity [2]

$$P = \frac{e^2\gamma^2}{6\pi\epsilon_0 m^2 c^3}\left[\left(\frac{d\mathbf{p}}{dt}\right)^2 - \beta^2\left(\frac{dp}{dt}\right)^2\right] \quad [71].$$

For a perpendicular accelerated charge the second term could be neglected, since the increase in energy for each turn is small compared to the vectorial change in momentum, leading to:

$$P \propto \frac{e^2\gamma^4}{r}.$$

Thus the energy loss is proportional to γ^4. Evidently protons are much less susceptible to this energy loss due to their higher mass compared to electrons - $\gamma = E/m$.

To cope with this problem it would be necessary to provide an enormous power to compensate the losses or increasing the radius of the machine significantly - both possibilities would be prohibitive due to their costs. The solution to this problem is a linear collider.

Two technologies are currently studied as possibility. A warm machine, the so called Compact Linear Collider concept CLIC - which would be immediately able to go into the multi TeV region and a cold technology with super conducting cavities of the TESLA type [23].

A crucial role for a linear collider is the achievable gradient for the acceleration since they directly determine the length and the cost of the machine. Picture 2.2 shows a typical super conducting cavity made of Niob. An important issue towards high gradients and low breakdown probability is the surface quality of the cavity.

A further important parameter defined by the machine is the timing of the beam. The described technologies are not able to work continuously; in case of the ILC technology the beam consists out of bunch trains with a length of 1ms and a repetitions rate of 5Hz. The 199ms between the trains are without any interactions. The beam is not continuous while this millisecond it consists of several thousand bunches with a spacing of around 200ns. The plot in Figure 3.4 shows the described bunch structure of the ILC. The time structure is a very important input parameter for the detector development especially for the Vertex detector VTX, see Chapter 3 and for some tracking detectors like Time Projections Chambers (TPC´s).

Picture 2.3 shows an overview of the machine layout. The overall site length is about 31 km for 500 GeV. Starting from the electron source the particles are

Parameter	Unit	Baseline	CLIC 500
Center of mass energy	GeV	200-500	500
Peak luminosity L	cm^2s^{-1}	2×10^{34}	2.1×10^{34}
$L_{0.1}$	cm^2s^{-1}	1.5×10^{34}	1.4×10^{34}
Pulse rate	Hz	5	50
Pulse length	μs	1000	0.177
Number bunches per pulse		2820	354
Beam size ($\sigma_x \times \sigma_y$ RMS)	nm	640 x 5.7	
Beam size σ_z	μm	0.5	
Accelerating gradient	MV/m	31.5	≈ 80

Table 2.1: Important ILC machine parameters and CLIC for comparison, from [22] and [25]

pre accelerated and feed into the damping ring were the emittance of the incoming beam is reduced to achieve the emittance required for the final luminosity. The out coming beam is then brought to the main linac where it is accelerated to the nominal energy.

The positrons are produced by pair creation from gamma photons, produced by an undulator in the beam line of the electrons, hitting a target. The positrons are captured and transported to the damping ring similar to the electrons.

Another important parameter of a collider is the luminosity. The luminosity for bunches with N particles colliding with frequency f and spatial dimensions $\sigma_x \sigma y$ is given by

$$L = \frac{N^2 f}{4\pi\sigma_x \sigma y} \times H_D$$

Where the first term describes the luminosity for head on collisions and the luminosity enhancement factor H_D takes into account the increase in luminosity due to the attraction of the opposite charged particles in the colliding bunches. H_D is typically in the order 1-2.

The ability to detect rare event is directly related to the luminosity since the productions rate $\dot{n}$ is connected to L by

$$\dot{n} = L\sigma$$

where σ is the cross section of the process.

2.3 Detector concepts

Since results from a single experiment are not regarded to be fully trustful it is foreseen to have two detectors at the ILC, which use different approaches to reach their physics goals. This will allow performing independent cross checks and will provide two independent data sets with different systematic errors. The achieved redundancy is the basis that the discoveries will be accepted.

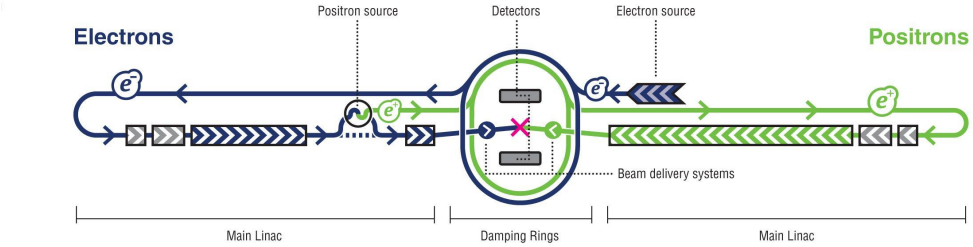


Figure 2.3: ILC machine layout from [2]

Currently three different detector concepts are under investigation the SID [8], ILD [1] a merger of GLD [7] and LDC concept and the so called 4th concept [28] - a summary of all concepts could be found in [17]. The main difference in these detectors is the tracker and calorimetry while vertex detectors are quite similar in all three concepts.

The next paragraphs introduce the various sub detectors, their working principle and the performance goals. Table gives 2.2 a summery.

Vertex detector The vertex detector consists of 5 layers in the barrel region in all concepts. The SID detector is additionally equipped with discs in the forward region which offer superior performance over long barrels, since the long barrels are disadvantageous for the measurement of shallow tracks due to the increased multiple scattering and the decrease in resolution due to landau fluctuation. A more detailed discussion dealing with the tasks and requirements of a vertex detector is presented in chapter 3.

Tracking system The aim of the tracking system is the momentum measurement. Since the momentum is connected to the curvature of the tracks via

$$p\,[GeV/c] = 0.3 \frac{r}{[1/m]} \frac{B}{[T]} [33],$$

it is necessary to have large lever arms for the precise measurement of the curvature.

The detectors for the ILC are using two different tracking detectors. The SID utilizes 5 layers of silicon strip detectors while the others intend to use a time projection chamber (TPC) as main tracker. The silicon strip detectors offer a precise position resolution with a limited number of space points whereas the TPC offers a moderate position resolution but a large number of space points and possibility for particle identification via dE/dx for low momenta.

The concepts aim for an overall momentum resolution of

$$\delta\left(\frac{1}{p_t}\right) \leq 5 \cdot 10^{-5} p\,(\mathrm{GeV/c})^{-1}\,.$$

Calorimetry - ECAL The tracker is followed by the electromagnetic calorimeter. The task of the calorimeters is energy measurement. Photons and electrons interact with the material and create secondary particles via pair creation and bremsstrahlung - a shower develops. The secondary particles are absorbed in the calorimeter. The characteristic length for this process is the radiation length X_0 e.g. 35mm for tungsten [10]. The three concepts are planning to use electromagnetic calorimeter with a depth of around 30 radiations length. ILD and SID are using fine granularity silicon tungsten sampling calorimeter employing the particle flow concept. The 4th concept is using a crystal calorimeter thus getting rid of the sampling fluctuations.

The energy resolution should be

$$\frac{\delta E}{E} \leq 0.10 \frac{1}{\sqrt{E\,(\mathrm{GeV})}} \oplus 0.01$$

Calorimetry - HCAL The hadronic calorimeter (HCAL) measures the strong interacting particles e.g. neutrons, pions and kaons. The strong interaction is characterized by the nuclear interaction length λ (e.g. 17cm for iron). Iron is commonly used since it effectively serves as return yoke for the magnetic field. A difficulty involved is the fact that the sensitivity of the calorimeter is different for hadronic component and the electromagnetic component created for example by the decay of neutral pions into photons. Thus a "compensation" must be provided.

The HCAL is made of an iron absorber consisting of 40 layers in case of ILD and SID, while the 4th concept is using a different approach with dual readout allowing them to distinguish hadronic from electromagnetic components and thus providing a compensation on software level.

The energy resolution should be

$$\frac{\delta E}{E} \leq 0.5 \frac{1}{\sqrt{E\,(\mathrm{GeV})}} \oplus 0.04$$

Muon system The task of the muon system is identification of the muons. Moreover it should provide some momentum resolution and a hardware trigger. ILD and SID intend use an instrumented return yoke with resistive plate chambers (RPC) while the 4th concept where no return yoke is foreseen will use gas based tracking.

Forward The forward direction is instrumented similar like the barrel region, which is described in the previous paragraphs. The vertex detector is extended by discs in the SID and 4th concept while in the ILD the long barrel modules provide a sufficient angular coverage. The tracker is extended by additional discs in the ILD concept to extend the coverage from the TPC. The calorimeter in the end caps is similar to the barrel region, see figure 2.4.

At very low angles ranging from 27.5 mrad to 5mrad the luminosity calorimeter is placed. The luminosity calorimeter (lumical) extends the coverage of the

end caps thus increasing the angular coverage for physics and will also enable luminosity measurements via small angle Bahaba scattering.

An important issue, regarding the design of the forward region, is the mask which shield the inner detector against the backscattered e^-e^+ from the quadruple close to the experiment. The backscattered pairs are an important background for the vertex detector.

	ILD (GLD,LDC)	**SID**	**4th**
Magnetic field	4T solenoid	5T solenoid	Dual solenoid 3.5T inner detector, 1.5T in Muon system
Vertex detector	5 barrel layer	5 Barrel layer and 4 end cap discs	5 barrel layer and 4 end cap discs
Intermediate tracking	2 Layer Si strips	-	-
Main tracker	TPC	5 Layer Si strips	TPC or drift chamber
ECAL	30 layer Si/W sampling	30 Layer Si W Sampling, $29X_0$	Cristal
HCAL	40 layer Fe / scintillator readout	40 layer Fe, RPC Readout	Dual readout
Muon system	Return yoke with RPCs	Return yoke with RPCs and scintillator strips	Tracking in gas

Table 2.2: Comparison of the three Detector concepts [17]

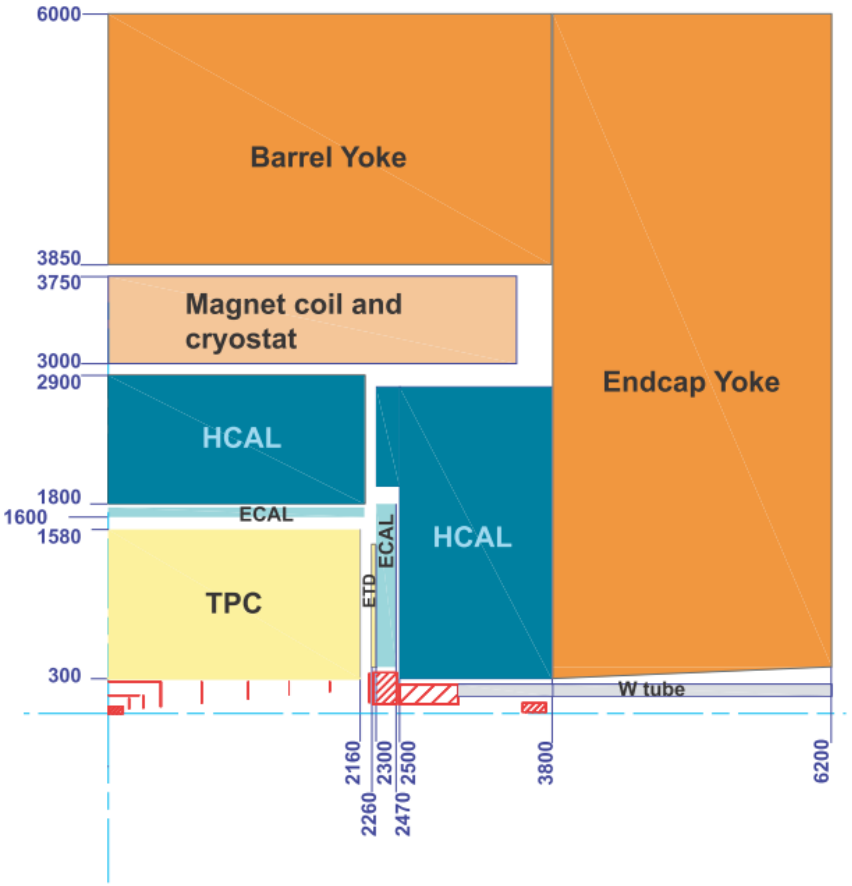


Figure 2.4: LDC Layout [91]

Chapter 3

ILC Vertex detector

This chapter describes the innermost detector system. The first section introduces the working principle of the Vertex detector in general. An important issue for the Vertex detector is the beam related background. Since it has major impact on the requirements a separate section 3.2 is dedicated to this. The requirements for ILC VTX derived from the physics goals are introduced in section 3.3, discussing the power and material budget, resolution and speed.

3.1 Working principle

The aim of the Vertex detector is the identification of heavy quarks measuring the displacement of secondary vertices with respect to the interaction point. More elaborate methods like the vertex charge technique will allow distinguishing quarks from anti quarks. Moreover the Vertex detector provides some momentum resolution.

Sketch 3.1 shows a typical set of tracks generated by an interaction at the interaction point (IP) generating a heavy Meson with bottom content decaying with a typical life time of $1.5ps$ [10] thus traveling a finite distance. Assuming a relativistic particle traveling with approximately the speed of light a displacement of $450\mu m$ has to be detected. Back extrapolation of tracks stemming from particles generated at a secondary or tertiary vertex will show a certain displacement from the interaction point the so called impact parameter d_0. A precise expression for the relation between lifetime t, decay angle θ in the rest frame and impact parameter is

$$d = ct\frac{\beta \sin(\theta)}{1 + \beta \cos(\theta)}[24]. \tag{3.1}$$

Assuming a finite point resolution of the detector $\sigma_{1,2}$ the extrapolation error of two planes, sitting in r_1 and r_2 distance from the interaction point, is given by

$$\sigma^2_{geom} = \left(\frac{\sigma_1 r_2}{r_2 - r_1}\right)^2 + \left(\frac{\sigma_2 r_1}{r_2 - r_1}\right)^2 [50] \tag{3.2}$$

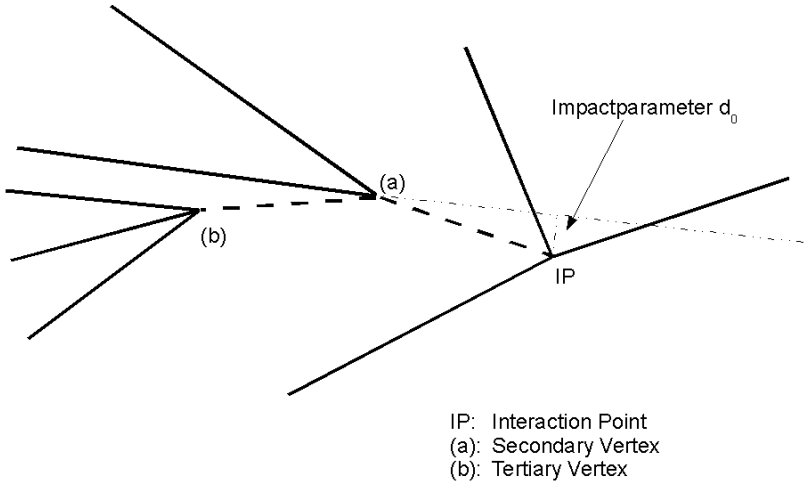


Figure 3.1: Typical vertex topology

Evidently the first layer should be as close as possible to the interaction point, i.e. making r_1 small and the lever arm should be as long as possible, i.e making $r_2 - r_1$ large.

However there is a second contribution decreasing the achievable impact parameter resolution: the multiple scattering. A charged particle undergoes several interactions. While traversing the detector it is losing energy governed by the Bethe-Bloch formula [33] leading to a charge signal in the detector and the angle of the particle is changed in a statistical way. The RMS value of the angle when a particle traverses perpendicularly a layer with material content X_j measured terms of radiation length is given by

$$\Delta\Theta_j = \frac{0.0136}{p\,[GeV/c]}\sqrt{\frac{X_j}{X_0}}\left[1 + 0.038\ln\left(\frac{X_j}{X_0}\right)\right]\,[50] \tag{3.3}$$

Thus the degradation of the multiple scattering (MS) on the impact parameter resolution σ_{MS} is given by weighting the angle with the lever arm of each layer resulting in

$$\sigma_{MS}^2 = \sum \left(R_j \Delta\Theta_j\right)^2 \quad [50] \tag{3.4}$$

Usually the IP resolution is given by parameterization using a fixed term and the multiple scattering term taking into account that particles traversing the detector under a shallow angle are stronger affected by multiple scattering.

Finally the impact parameter resolution could be expressed by

$$\sigma_{d_0} = \sigma^2_{geom} + \sigma^2_{MS} = \sigma^2_{fixed} + \left(\frac{\widetilde{\sigma_{MS}}}{p \sin(\theta)^{\frac{3}{2}}} \right)^2 \tag{3.5}$$

Summarizing this section one can conclude that an optimal vertex detector

- has excellent single point resolution
- is placed as close as possible to the IP
- has minimal material in front (beam pipe) and consists itself of a minimal amount of material

3.2 Background

Commonly Lepton Collider are regarded as very clean concerning beam related background. However there are several processes which lead to the creation of photons and finally to low energy e^+e^- pairs in the detector. The most prominent processes are

- synchrotron radiation "beamstrahlung"
- coherent pair production
- incoherent pair production.

The necessary luminosity requires a strong focusing both in x and y in the order of a few tens of nm, see table on page 9. If a particle goes through the collective field of a bunch, which could be in the order of kilo Tesla [92], it is likely that a particle emits synchrotron radiation. The number of emitted photons could be related to the beam parameter by

$$n_\gamma \approx 2.54 \left[\frac{\alpha \sigma_z}{\lambda_e \gamma} \right] \frac{\Gamma_{avr}}{\sqrt{1 + \Gamma_{avr}^{\frac{2}{3}}}} \text{ [93]} \tag{3.6}$$

with

$$\Gamma_{avr} \approx \frac{5}{6} \frac{N r_e \lambda_e \gamma}{\sigma_z \left(\sigma_x + \sigma_y \right)} \text{ [93]} \tag{3.7}$$

where $\sigma_z \sigma_x \sigma_y$ measure the geometry of bunch, N is the number of particles in a bunch, with the Compton wavelength λ_e and r_e the classical electron radius.

These photons are carrying a considerable amount of energy thus leading to a degradation in the energy spectrum of the collider and could convert into e^-e^+ in the strong electromagnetic field of the bunch. This process is called coherent pair production.

In case of the incoherent pair production single particles and photons create backgrounds via the following QED processes

- $\gamma_{BS}\gamma_{BS} \rightarrow e^-e^+$ Breit-Wheeler

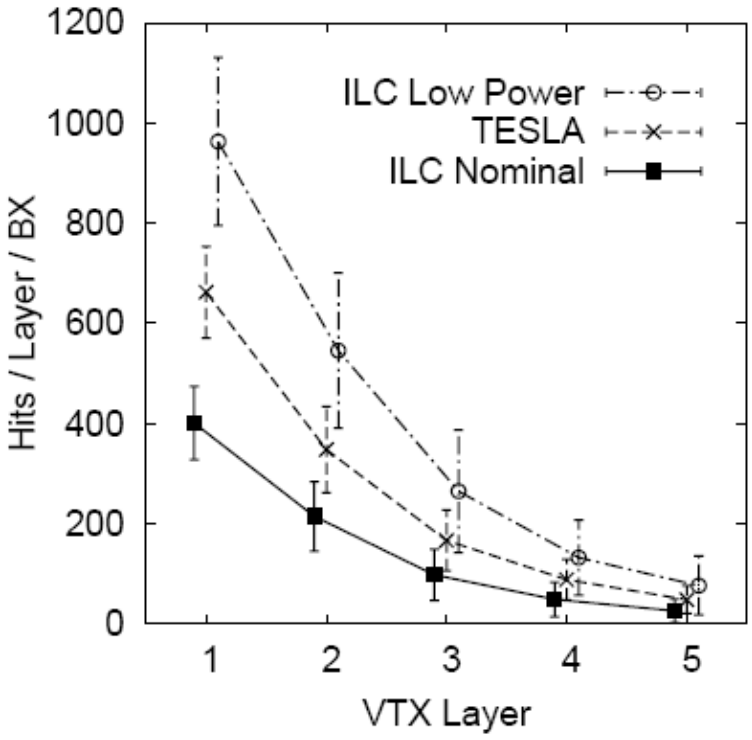


Figure 3.2: Background his for various machine layouts [84]

- $e^{\pm}\gamma_{BS} \rightarrow e^{\pm}e^{-}e^{+}$ Bethe-Heitler
- $e^{-}e^{+} \rightarrow e^{-}e^{+}e^{-}e^{+}$ Landau-Lifshitz

While the Beamstrahlungs photons are well collimated along the beam axis the electron-positron pairs are less collimated and could produce hits in the Vertex detector. Since the electron-positron spectrum is pronounced at low energies the pairs are confined around the axis due to the magnetic field of the detector thus leading to a strong dependence on the radius. This behavior although limits the inner radius of the Vertex detector. Figure 3.2 shows the number of background hits in the detector per bunch crossing and layer for various layouts of the machine.

3.3 Detector requirements

As pointed out in the first section an ideal Vertex detector should have minimal mass, close to the IP and should have excellent point resolution. In reality this is not possible due to many reasons:

- material is necessary to create some signal in the detector
- the minimal distance to the IP is limited by background
- electrical power feed into the detector must be removed by cooling

- beam pipe is necessary

The next subsections will introduce these issues and discuss the impact on the detector design in more detail.

3.3.1 Resolution

As pointed out in section 3.1 the figure of merit of a Vertex detector is the impact parameter resolution. To achieve a precise tag for b-Mesons as well as for the faster decaying c-Mesons the IP resolution should be better than

$$\sigma_z \leq \sigma_{0z} \oplus \frac{\sigma_{1z}}{p \sin(\theta)^{\frac{5}{2}}} \tag{3.8}$$

with a fixed term of $\sigma_{0z} = 5\mu m$ and the multiple scattering contribution better than $\sigma_{1z} \leq 10\mu$m in z. This means in terms of single point resolution a resolution of around 5μm. To achieve this value typical pixel sizes are in the range of $(15 - 25)\mu\text{m}^2$ depending on the charge sharing behavior of the detector. Simulations show that a DEPFET with a pixel size of $24\mu\text{m}^2$ will satisfy this requirement.

3.3.2 Material budget

To achieve the multiple scattering contribution of 10μm it is necessary to reduce the material to a minimum. Significant contributions to the material in the detector are

- the beam pipe
- the mechanical structure for mounting
- the detector itself and the ASICs within the acceptance
- the cabling for power and signal distribution
- the cooling system
- the module, e.g. support for thin detectors, blocking capacitors

Regarding the mechanical issues R&D is still underway. For the Detector point of view already settled numbers are available. In the barrel region it is necessary to have a material budget of $0.1\%\text{X}_0$ to achieve the required resolution, this is equivalent to silicon of 100μm thickness. A DEPFET based module with a thickness of the active part of 50μm and a rigid silicon frame will fulfill this requirement, see chapter 7.

3.3.3 Power dissipation

The material budget affects possible cooling schemes, cooling pipes would exceed the required budget. To cope with this a cold gas stream is regarded as solution for cooling, but this limits the maximal power dissipation of the detector, because a fast gas stream could cause vibrations due to turbulence. Simulations showed that a laminar cold gas stream could provide around 100W of cooling power for the whole Vertex detector including the forward discs.

However the final numbers will strongly depend on the used detector and on the acceptable operation temperature.

3.3.4 Readout speed

The readout speed determines the number of hits accumulated during the integration time. Obviously the occupancy - the number of hits per unit area - is inversely proportional to the readout speed.

The analysis assigns the hits in the Vertex detector to tracks - the paths of particles traversed the detector. This pattern recognition is spoiled when the fraction of hits accumulated in the detector are beyond a limit of around 1%. At higher occupancies the probability of a hit assigned to a wrong track increases dramatically. These fake tracks are limiting the performance of the vertex detector.

The readout speed requirements are driven by the expected background rates introduced in section 3.2, since these are the dominant source of hits.

A further input parameter to define the readout speed is the time structure of the colliding beams. Figure 3.4 shows the timing of the incoming beam. The collisions occur in approximately 1ms followed by a quite phase of 199ms, in the active phase the beam is not continuous, it consists of 2820 bunches with a distance of 337ns.

In the Tesla technical design report (TDR) it was assumed that an integration of 150BX equivalent to a frame time of 50μs is sufficient to preserve the efficiency of the pattern recognition. More resent simulation carried out however show that this timing scheme has to be revisited, for example see [19].

The plots in figure 3.3 are showing the efficiency of the tracking for different integration times. The analysis was based on the reconstruction of $t\bar{t}$ events with in presence of background. A typical event consists of 66 tracks, in the scenario with longest integration time already 44 tracks of an event where fake tracks, thus it is evident that the integration time has to be shorter. A integration time of 75BX ($25\mu s$) in the inner, 225BX ($75\mu s$) in the second and 300BX ($100\mu s$) in the outer layers is now regarded as sufficient.

3.3.5 Radiation hardness

Evidently the detector is exposed to ionizing and also non ionizing radiation while operation thus requiring the detector to preserve its efficiency during operation. One could identify two main sources of radiation

	NIEL $\left[\frac{1MeV_{n_{equiv.}}}{acm^2}\right]$	Ion. Dose $\left[\frac{Rad_{Si0_2}}{a}\right]$
Neutrons	$\approx 10^9$	-
Electrons	$8.5 \cdot 10^{10}$	$\approx 50 \times 10^3$

Table 3.1: Expected neutron fluency and ionizing dose at ILC [91]

- electron positron pairs from beamstrahlung
- electron positron pairs backscattered from beam calorimeter
- neutrons created in the calorimeters

While the neutrons only cause non ionizing radiation damage the electrons even with energies of several tens of MeV causes both ionizing and non ionizing radiation damage.

Table 3.1 gives a summary, of the expected doses in the inner layer of the Vertex detector assuming 1.7×10^{12}Hits/cm^2/a [91] background hits which are equivalent to 400 Hits/BX and one year operation in the inner layer (extracted from figure 3.2). Obviously the radiation from this source is significantly lower in the outer layers.

Figure 3.5 shows the estimated doses for the different layers taking into account background hits per layer and the geometry from 3.2.

A detailed study on the impact of this radiation on the performance of a DEPFET based Vertex detector is carried out in the chapters 14 and 15.

3.4 Layout

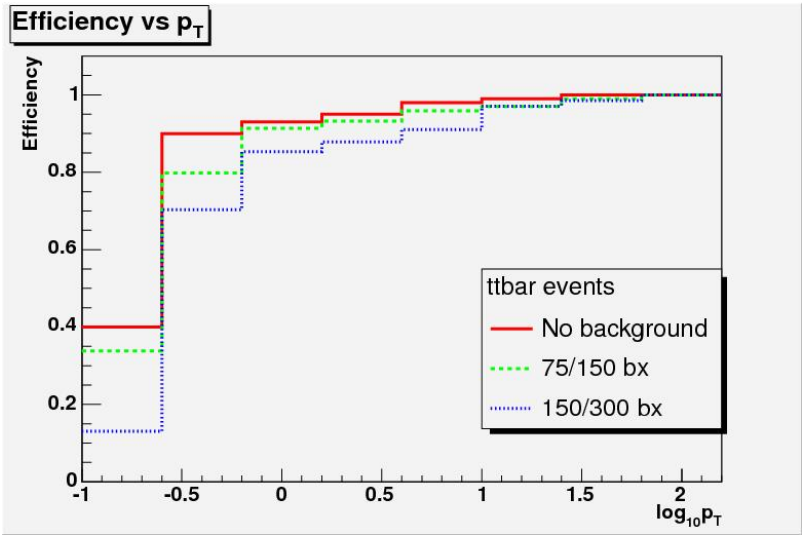
The considerations in the previous sections lead to a design summarized in the following table:

Layer	Radius $[mm]$	L x W $\left[mm^2\right]$	Number of ladders $[R\phi \times z]$	Frame time $[\mu s]$	
				Tesla	ILC rev.
1	15	100 x 13	8/1	50	≈ 25
2	26	125 x 22	8/2	250	$\approx$75
3	37	125 x 22	12/2	250	$\approx$100
4	48	125 x 22	16/2	250	$\approx$100
5	60	125 x 22	20/2	250	$\approx$100

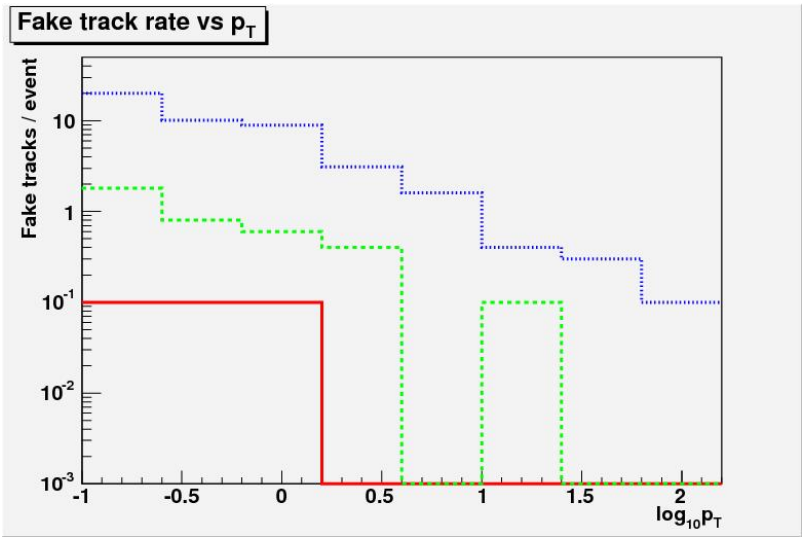
Table 3.2: Geometry and timing of the ILC vertex detector

Picture 3.6 shows the assembly of the vertex detector with long barrels like proposed for the ILD detector concept. Some technologies like CCDs will

require strong cooling to cope with the radiation damage. The shown foam cryostat is not necessary in case of DEPFET since the detector could operate close to room temperature even after radiation damage, see chapter 14.1.



(a) Efficiency of reconstruction vs. p_t



(b) Fake track rate

Figure 3.3: Efficiency of reconstruction and fake track rate for various integration times [61]

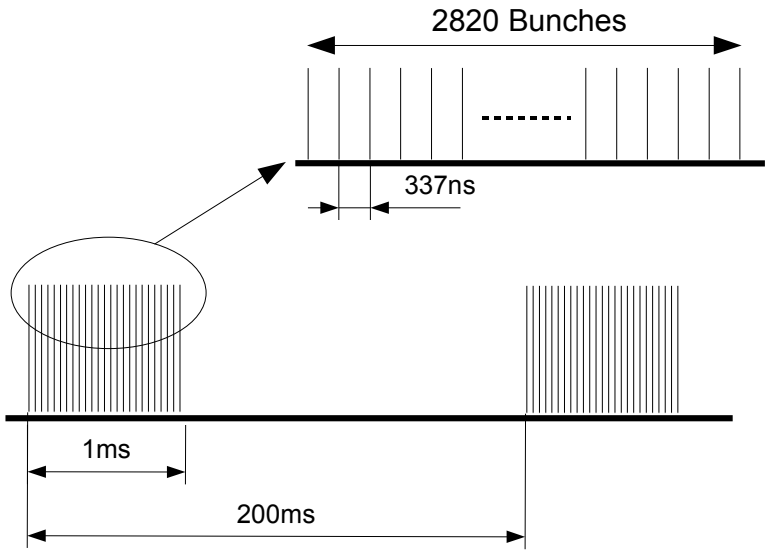


Figure 3.4: ILC time structure

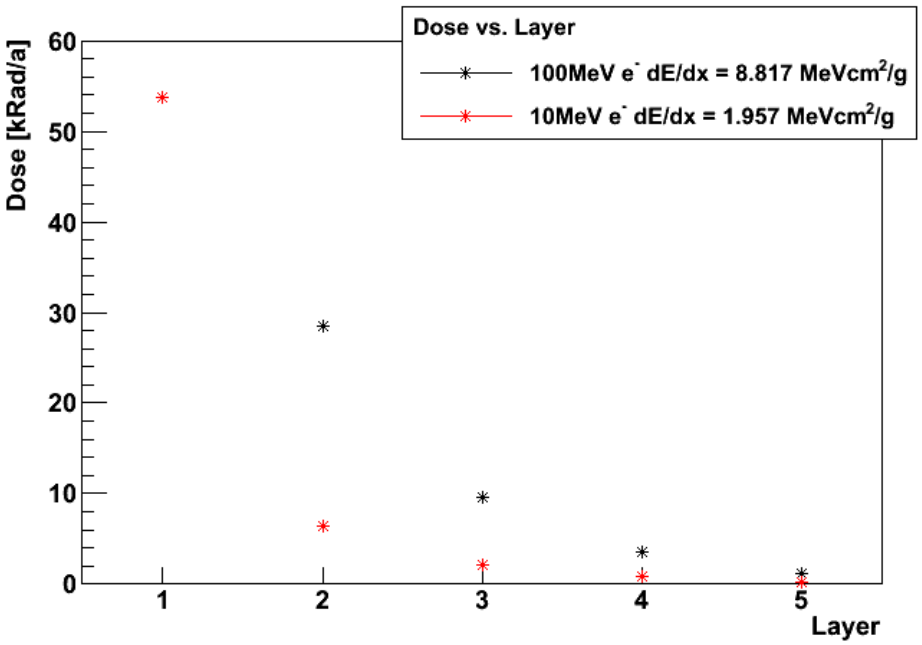


Figure 3.5: Annual dose for the different layers; the decrease is significantly steeper than the hits/BX/layer in figure 3.2 - the number of hits/layer is decreasing and the area of the layers is increasing towards the outer layers; the red stars assume an energy loss for 10MeV electrons; the black stars are for 100MeV electrons where the energy loss is increased due to bremsstrahlung

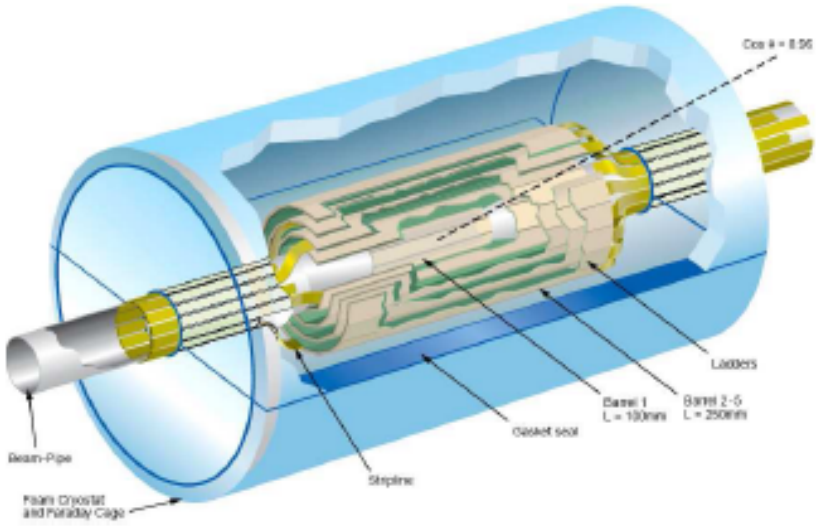


Figure 3.6: Vertex detector with long barrels [18]

Chapter 4

The DEPFET concept

The Depleted Field Effect Transistor DEPFET was proposed by Lutz and Kemmer in 1987 [40] and the first working devices were demonstrated in 1989 [39].

The DEPFET is based on the principle of sidewards depletion described in section 4.1.

The evolution from a sidewards depleted device towards the DEPFET is shown in the following section. The field effect transistor (FET) as main constituent of the DEPFET and the signal generation is introduced in section 4.3.

After the working principles are presented various readout methods to create a measurable signal - a voltage or current step - are discussed with respect to the timing requirements.

The arrangement of the single DEPFET pixels into matrices and the signal processing of these matrices is highlighted in section 4.5.

An important issue related to the operation of the DEPFET is the clear process, which will be analyzed in detail in the main part, is introduced in section 4.6.

4.1 Sidewards depletion

The principle of sidewards depletion was introduced by Gatti and Rehak in 1984 [32]. The idea of this principle is depicted in figure 4.1, by introducing a second p++ implant on a n bulk material it is possible to deplete the volume of the semiconductor from both sides. Since the depth of the depleted volume is proportion to $\sqrt{U_{dep}}$ the whole volume could be depleted using a quarter of the voltage necessary for a simple diode.

Another feature of the sidewards depletion could be seen if the potential distribution inside the depleted volume is investigated using the Laplace equation

$$\Delta\Phi = -\frac{\rho}{\epsilon_0} = \frac{qN_D}{\epsilon\epsilon_0}.$$

Assuming that both electrodes on potential U_{upper} and U_{lower} and the volume is (over)depleted thus a space charge of N_D is present. In this case the potential could be calculated by two consecutive integrations. Taking into account the boundary conditions this leads to

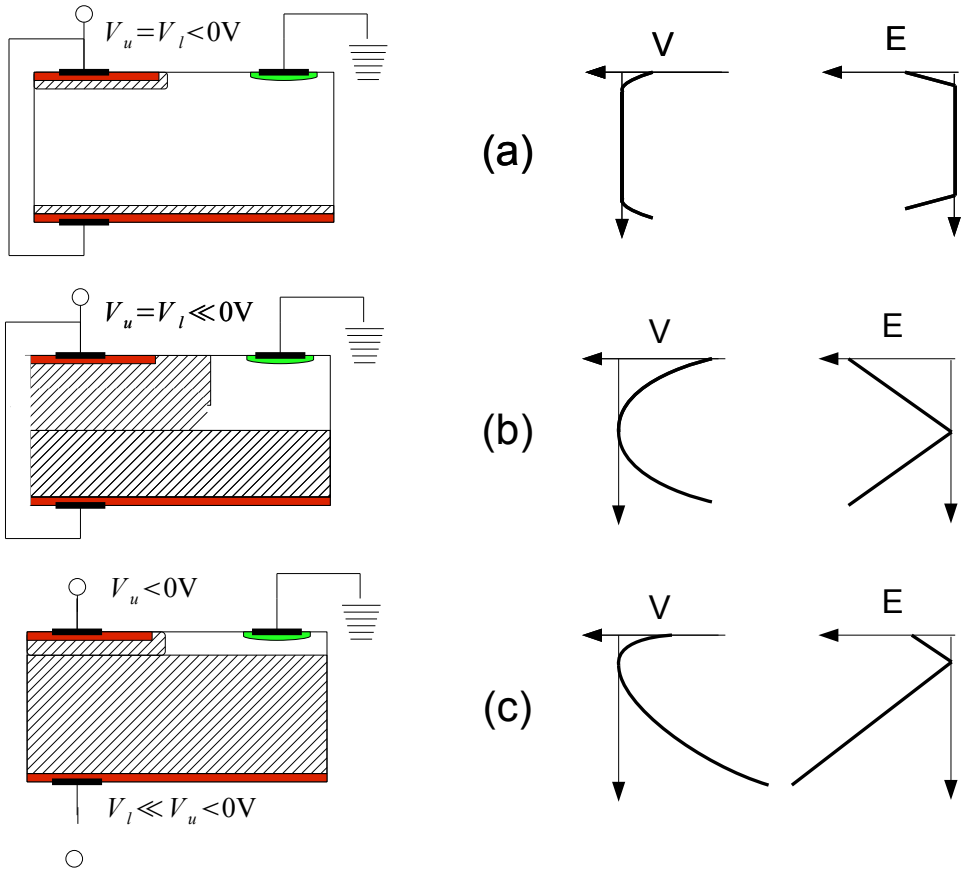


Figure 4.1: Sidewards depletion

$$\Phi(y) = \frac{y^2}{2}\frac{qN_D}{\epsilon\epsilon_0} + y\left(\frac{U_{upper} - U_{lower}}{d} - \frac{d}{2}\frac{qN_D}{\epsilon\epsilon_0}\right) + U_{lower}.$$

Calculating the potential distribution along y it is found that a potential minimum for electrons is created were both depletion zones are in contact.

The minimum is found at

$$y_{min} = \frac{d}{2} + \frac{\epsilon\epsilon_0}{qN_D d}\left(U_{upper} - U_{lower}\right)$$

The sidewards depletion is not only used in the DEPFET, it allows building devices like fully depleted PN-CCD´s [76] and (controlled) drift chambers which are based on this principle too.

If the voltage on the upper side is decreased and the lower voltage increased [case (c) in figure 4.1] the potential minimum could be moved close to the upper surface. The next steps towards the DEPFET device are described in the next section.

4.2 DEPFET working principle

This section gives an overview of the DEPFET working principle starting from the sidewards depletion, a description of the various operation stages could be found in [30].

The evolution from the sidewards depletion to the DEPFET is shown in picture 4.2. By structuring the p implant one can achieve a structure shown in (a) if no further lateral structuring is done and a potential gradient is applied to the strips this structure could be used as drift chamber.

The next steps towards the final device are shown in (b). By introducing a MOS structure between the p implants a FET is formed. The potential minimum is achieved by an additional n implant under the gate which leads to a further decrease of the potential in this pocket thus forming the potential minimum the "internal gate".

Evidently in thermal equilibrium the internal gate is filled with electrons. To remove them an additional n+ contact is introduced as shown in 4.2(c). By applying a positive voltage to this contact, in the following called clear contact, it is possible to remove the charge from internal gate.

The confinement of charges in the internal gate is provided by the previous mentioned n implant under it. The implant provides a positive space charge in the internal gate thus leading to an attractive potential. In addition a MOS structure is places on the edges, the "Clear Gate". By applying a negative potential to the clear gate a potential barrier is created which prevents charges to flow from the internal gate into the nearby clear contact.

To prevent charge flowing directly into the clear contact a further p implant is introduced below the clear. The "deep p" provides a negative space charge. A sketch of the final device is depicted in figure 4.2b.

4.3 The MOSFET

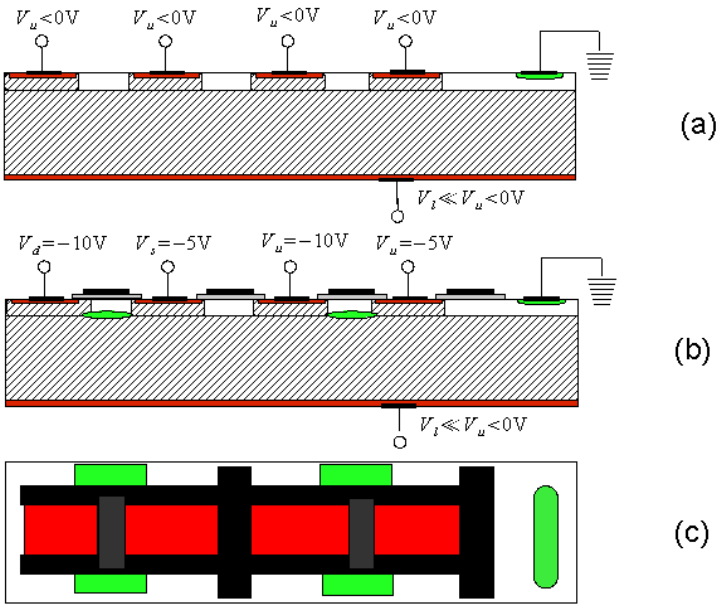
Since the integrated Field Effect Transistor (FET) is the major part of a DEPFET pixel this section introduces the properties of an FET - namely the

- current voltage characteristic
- influence of charge in the internal gate
- small signal parameters g_m and g_g.

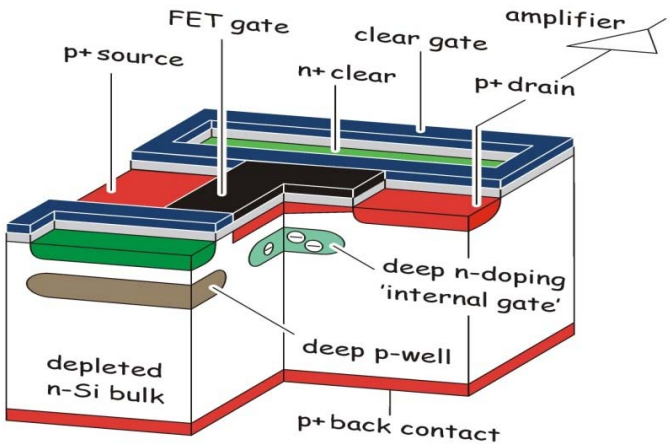
The current voltage characteristic of a standard FET is derived in the appendix C. In case of the DEFPET one has to take into account the charge in the internal gate.

A further complication is the fact that there are additional parasitic capacitances to neighboring electrodes. The electrodes which have to be considered are the backside contact the source and drain contact.

The backside is far away from the internal gate typically 50 to 450 micron depending on the thickness of the detector thus the capacitive coupling to



(a) Evolution from a sidewards depleted device towards the DEPFET



(b) Final DEPFET device

Figure 4.2: Evolution from a sidewards depleted device towards the DEPFET and the final device

the internal gate could be neglected since the distance to the channel is much smaller. More important is the nearby source contact where a stronger parasitic coupling can be expected. This is also pronounced since the charge in the internal gate is closer to the source due to the repulsive potential of the drain.

Assuming that each carrier in the internal gate influences a carrier in the channel of the FET the current voltage (charge) characteristics could be derived by introducing an equivalent voltage change on the external gate. A charge Q in the internal gate is equivalent to a change in U_{gs} of Q/C_{ox}. A more realistic model could be achieved by introducing a reduction factor f which introduces the effect of parasitic coupling to neighboring electrode.

The drain source current flowing through a DEPFET transistor can be modeled as

$$I_{ds} = \frac{1}{2}\frac{W}{L}\mu_p C'_{ox}\left(f\frac{Q_{sig}}{C_{ox}} + V_{gs} - V_{THR}\right)^2 \text{ [41, 48]}. \tag{4.1}$$

Besides the term $\frac{Q_{sig}}{C'_{ox}}$ the current voltage characteristics of the DEPFET is similar to a conventional FET. The current for typical parameters of the DEFPET is depicted in figure 4.3a. The plot shows two cases of the threshold voltage - -0.2V (typical value) and -2.2V (e.g. due increased by ionizing radiation).

From this formula it is possible to derive the small signal parameter. The transconductance g_m can be calculated by deriving with respect to V_{gs}. The internal amplification g_q is obtained by deriving with respect to the charge in the internal gate Q_{sig}.

Both quantities can be expressed as:

$$g_m = \frac{W}{L}\mu_p C'_{ox}\left(f\frac{Q_{sig}}{C_{ox}} + U_{gs} - V_{THR}\right) \tag{4.2}$$

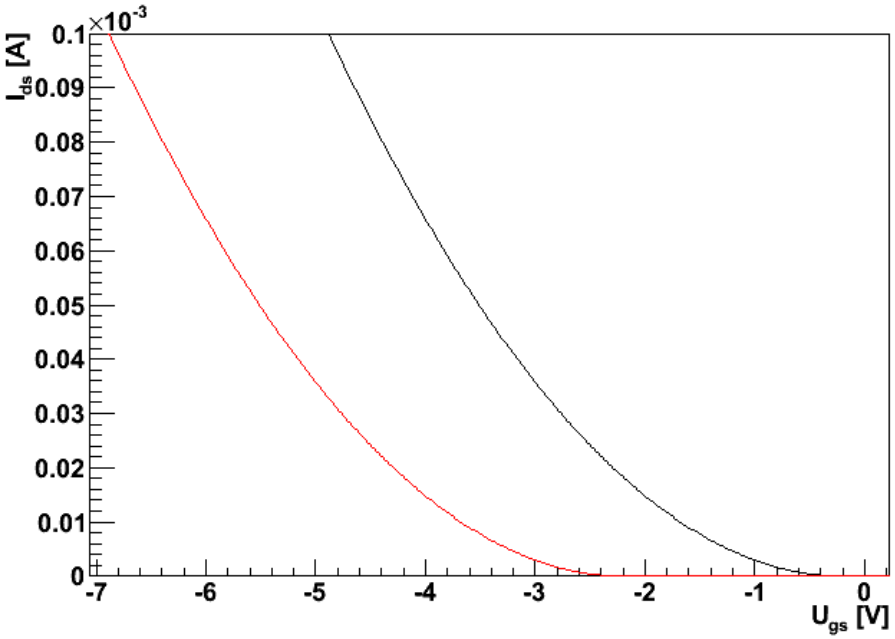
$$g_q = \frac{1}{L^2}\mu_p f\left(f\frac{Q_{sig}}{C_{ox}} + V_{gs} - V_{THR}\right) \tag{4.3}$$

Evidently both quantities are proportional to each other. Calculated values for representative parameters are depicted in figure 4.3b. The formulas suggest a linear increase of both g_m and g_q with the gate-source voltage. Whether this model is valid is investigated in chapter 9.

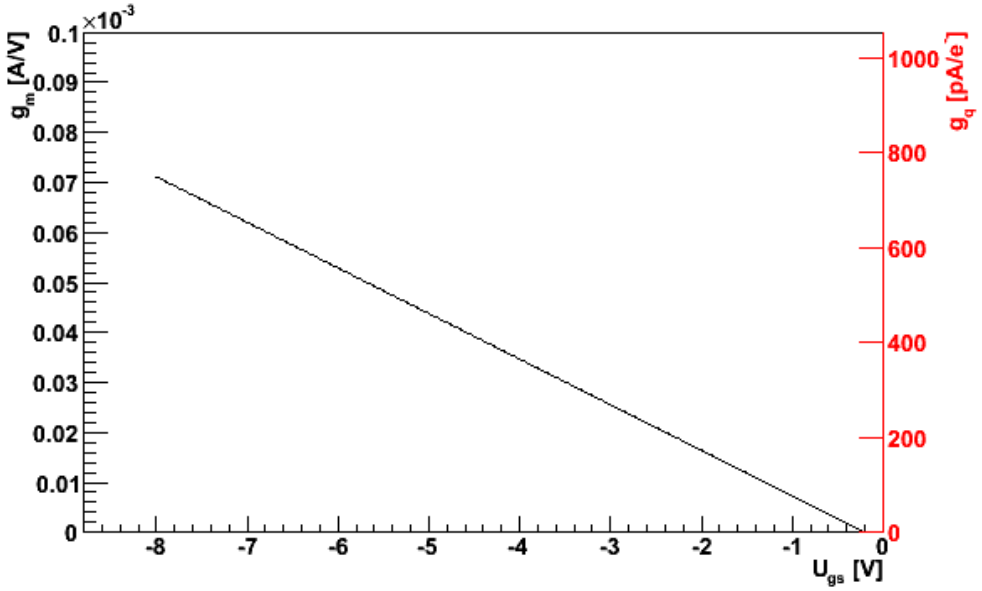
In addition this model predicts that the transconductance and the internal amplification depend also on the signal charge in the internal gate. Thus the response to charge is nonlinear. However for typical operation parameters U_{gs} of $\approx$ 3V and a charge of O(10^4e) the nonlinear term could be neglected.

4.4 Readout concepts

Like for a conventional FET there are different circuits to build an amplifier [78]. In case of the DEPFET the Source Follower, also known as Common Drain, and the Drain readout (aka "Common Source") are most commonly used. The two possibilities and their limitations are discussed in the following paragraphs.



(a) Current I_{ds}



(b) Small signal parameter g_m and g_q

Figure 4.3: Drain source current I_{ds} calculated for two threshold voltages -0.2V and -2.2V (equation 4.1) and the small signal parameter g_m and g_q for V_t=-0.2V (equation 4.2 and 4.3). The mobility is taken as 150cm^2/Vs, W/L 18/5, d_{ox} = 200nm

Source follower The circuit of a Source follower is shown in figure 4.4a. In this case the drain is put on a fixed potential (common drain) while the Source of the FET is biased with a current source. The gate is also set to a fixed potential. This means that the potential of the source is sensitive to charge in the internal gate.

After settling of the potential on the source it is possible to calculate the source voltage from the current voltage characteristics, see formula 4.1. By requiring that U_{gs} - relative to the fixed gate potential - satisfies the current voltage relation:

$$U_{gs} = \frac{Q_{int}}{C_{ox}} - U_{thr} - \sqrt{\left(I_{bias}\frac{2L}{\mu W}\right)}. \tag{4.4}$$

The charge to voltage conversion gain of the source follower readout G is

$$G = \frac{dU_{gs}}{dQ} = \frac{1}{C_{ox}}. \tag{4.5}$$

For the application in high energy physics where the speed is a major requirement, see 3.3, the dynamic behavior has to be investigated too. The rise time of the source follower configuration is approximately given by

$$\tau \approx \frac{C_{load} + C_{gs}}{g_m}.[54] \tag{4.6}$$

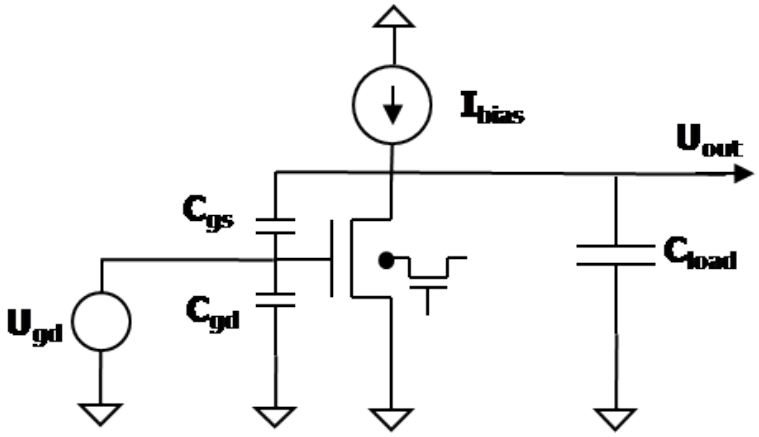
Where C_{load} is the capacitance at the output of the amplifier, see figure 4.4a. The load capacitance is given by the sum of all parasitic capacitances with respect to ground. In the case of the DEPFET matrix the capacitance is expected to be in the order of 50pF for a length of 6cm (half of the length of a module in the inner layer). Thus C_{load} is the dominating contribution in formula 4.6 since the gate-source capacitance C_{gs} is typically around 15fF for a transistor with a W/L of $20\mu m/6\mu m$ and 180nm oxide. The transconductance of a DEPFET with this parameters could be estimated to $50\mu S$. Taking this into account the load capacitance already limits the rise time to $1\mu s$. This is much more than allowed by the ILC requirements introduced in section 3.3.4.

Drain readout The circuit of a DEFPET in drain readout is shown in figure 4.4b. The case of this readout the potentials of the ports (gate, source and drain) are fixed. The source and gate are directly connected to a fixed potential while the drain potential is fixed via an amplifier a cascode or directly via a transimpedance amplifier. The configuration is sensitive to changes in the current flowing through the DEPFET thus the signal is

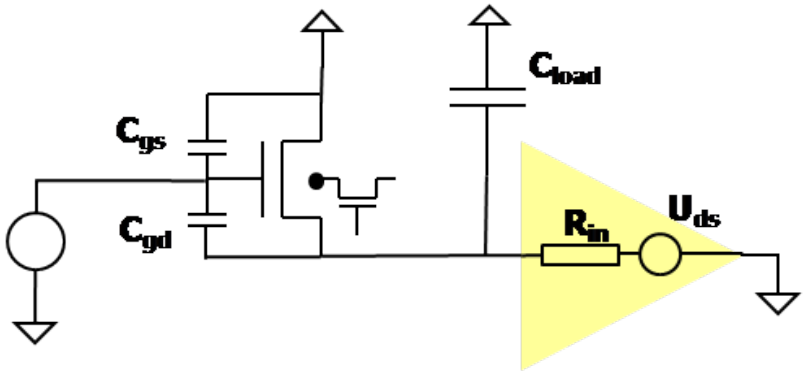
$$\Delta I_{ds} = Q_{int} * g_q. \tag{4.7}$$

The settling time of the drain readout is given by

$$\tau = C_{load} * R_{in}. \tag{4.8}$$



(a) Source follower



(b) Drain readout

Figure 4.4: Source follower and drain readout

Evidently the load capacitance is still a limiting factor of the speed. However the input resistance of the amplifier could be made small since a technology allowing small feature sizes could be used to build the amplifier. In case of the CURO a input resistance of $\approx 100\Omega$ is realized [81]. In this case a settling time of 5ns could be achieved with the same load capacitance of 50pF, which is sufficient for the requirements in high energy physics.

Even if the drain readout is intrinsically fast a further complication arises from the finite resistance of the metal lines ($\approx 300\Omega, 5\text{cm}$) on the detector. Together with the parasitic capacities they also pose a limit on the speed.

4.5 Matrix operation

Matrix layout The DEPFET matrix is arranged of pixel cells like shown in figure 4.5. The drains of each column are connected separate to one metal line. The Clear Gate in figure 4.9 is common for the whole matrix this is realized by connections on poly silicon level.

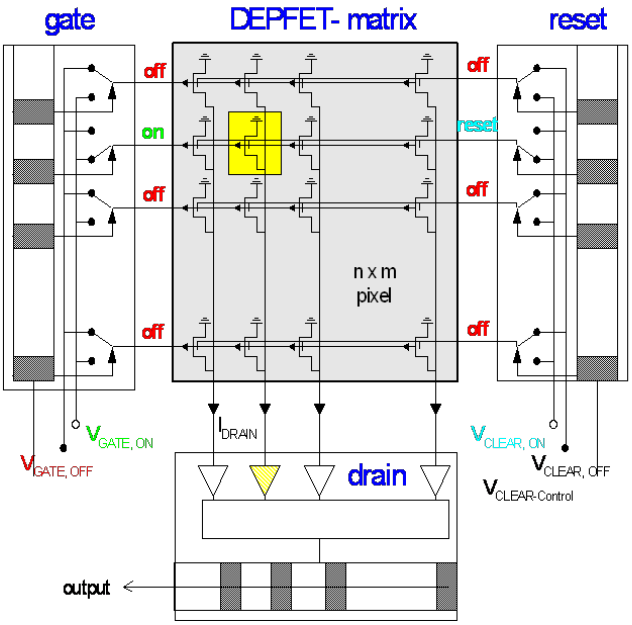


Figure 4.5: DEPFET matrix layout

Matrix readout The readout is performed (double)row wise. One row is enabled by the steering chips shown in figure 4.5 while the rest of the matrix is still in off state. The remaining rows are still sensitive.

The current through the selected row is measured by the frontend. After sampling of the current a clear pulse is applied to the selected row, which removes the charge from the internal gate and the current is measured again. The difference of both currents is proportional to the charge in the internal gate.

The readout concept allows processing a complete row in parallel. Each column has its own amplifier - the readout is called column parallel.

When the whole matrix is read out this process starts again. Since each row reflects a different time slice the sequence is called "rolling shutter" mode.

4.6 Clear concepts

An important aspect in the operation of the DEPFET is the clear process. This process removes the charge collected in the internal gate. First investigations regarding the clear process were made in [41, 54]. The timing was analyzed in [68]. The section gives an rough overview.

Two distinct clear concepts are existing, the continuous clear and the clocked clear.

In the continuous clear also known as overflow mode the charge is removed continuously from the internal gate. This mode would lead to charge losses in the commonly used rolling shutter mode. Thus for matrix operation the second clear mode the clocked clear is the standard one.

In the clocked clear mode a clear pulse is applied periodically to a pixel. The charge arriving in the pixel after a clear pulse is stored until the next pulse arrives.

The clear process has significant impact on the system performance, since noise as well as signal heights are depending on the clear. This can be understood by the fact that the signal is derived by the difference of two consecutive samples of the current flowing through the DEPFET before and after the clear. If charge remains after the clear process these difference is smaller thus the signal is reduced. Moreover the remaining charge serves as a variation of the first current sample for the following measurements thus increasing the noise.

If the clear removes the charge completely from the internal gate this state is called "full clear". In contrast to other detectors the DEPFET is able achieve a full clear since no metal contacts are in contact with the signal charge. This means that the DEPFET can be operated as reset noise free device [59].

To achieve a full clear the potentials of the clear pulse and the clear gate must be optimized. .

4.6.1 Clocked clear mode

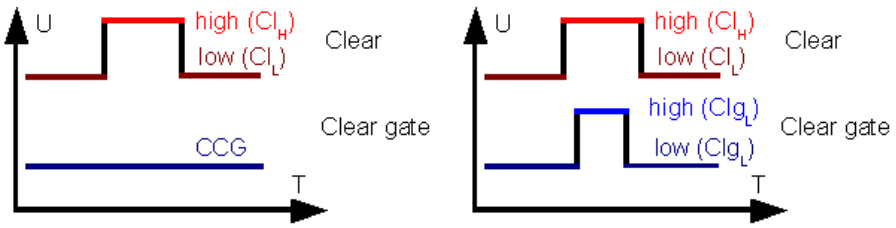
Basically three different configurations for the clocked clear are existing. These modes differ in the usage of the clear gate. The potential applied to the clear gate determines the potential barrier between the internal gate and the clear. Thus the clear process depends strongly on this potential.

The behavior of a pixel in clocked clear mode is depicted 4.7a. The picture shows a screen shoot of an oscilloscope. The readout is performed with an inverting amplifier thus when a signal arrives, marked with the red arrow, the current is increased. The clear pulse removes the signal from the internal gate and the current is back on its zero level. The slope of the output is due to the leakage current which continuously flows into the internal gate.

Clocked clear gate In the clocked clear gate configuration a positive voltage pulse is applied to the clear gate together with the clear pulse. This allows a full clear with a minimum clear voltage. The disadvantages of this configuration are the increased complexity since a third voltage must be switched to control the matrix. Furthermore the timing of the pulse on the clear gate is critically. The clear gate pulse should be at least as long as the clear pulse to prevent charge flowing back into the internal gate.

Common clear gate The common clear gate was introduced to avoid the difficulties involved in the clocked clear gate configuration. The drawback of common clear gate is the loss of an additional free parameter for optimization - the clear gate low value applied in the integration phase. One common potential must be optimized in a way that a proper g_q is achieved in the readout phase and a full clear with a reasonable low clear voltage. Measurements show that the g_q is significantly modulated by the clear gate voltage, see chapter 11.

Capacitive coupled clear gate The capacitive coupled clear gate configuration is a new design introduced to combine the simplicity of the common clear gate configuration with the superior clear performance of the clocked clear gate. This is achieved by a capacitive coupling of the clear with the clear gate. A detailed study of the performance of this concept is presented in chapter 12.



(a) Common clear gate (b) Clocked clear gate

Figure 4.6: Definition of the levels related to common clear gate and clocked clear gate operation

4.6.2 Continuous clear mode

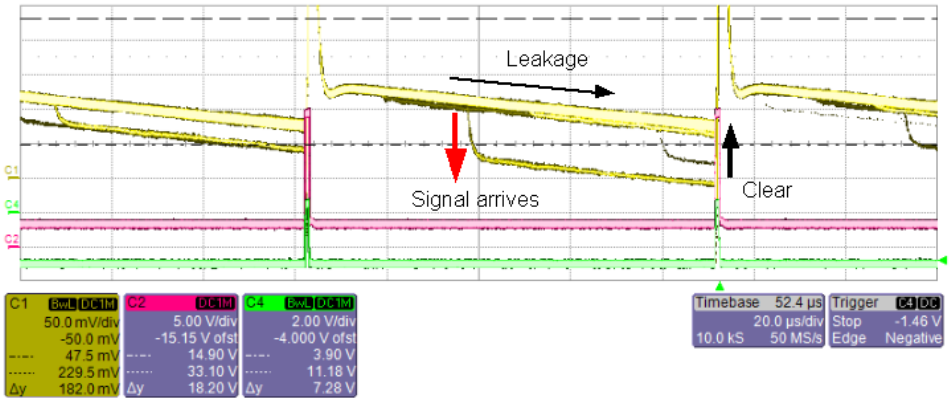
In this mode the potentials applied to the clear and clear gate are chosen in a way that the internal gate still is a potential minimum for electrons. Arriving charge is collected in the internal gate and continuously removed. This mode does not allow matrix operation when the time constant of the decay is of the same order of magnitude as the frame time. Figure 4.7b shows a screen shot of the output of a pixel in this mode.

4.7 DEPFET for ILC

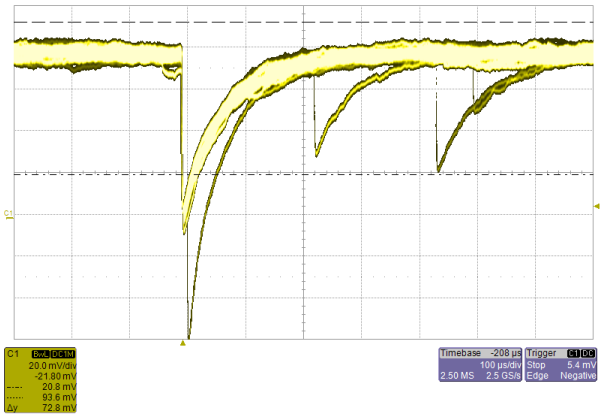
The previous sections introduced the DEPFET in general. This section will focus on the development of the DEPFET device dedicated to application in high energy physics.

The special requirements for the ILC and HEP in general are:

- fast readout:
  - fast charge collection
  - fast clear
- small pixel sizes:
  - compact layout
  - additional layers for routing
- radiation hardness



(a) Clocked clear operation (Integration time 100μs; Horizontal axis 20μs/div; Yellow output of the DEPFET 50mV/div; Purple: Clear pulse 5V/div; Green: Clear gate pulse 2V/div)



(b) Continuous clear (Horizontal axis: 100μs/div; Yellow: DEPFET output 20mV/div)

Figure 4.7: Clear modes of DEPFET sensors. In clocked clear gate mode the charge is removed periodically when applying the clear pulse. The time between two clears serves as integration time - the charge is stored. In case of the continuous clear the charge is removed with a certain decay time.

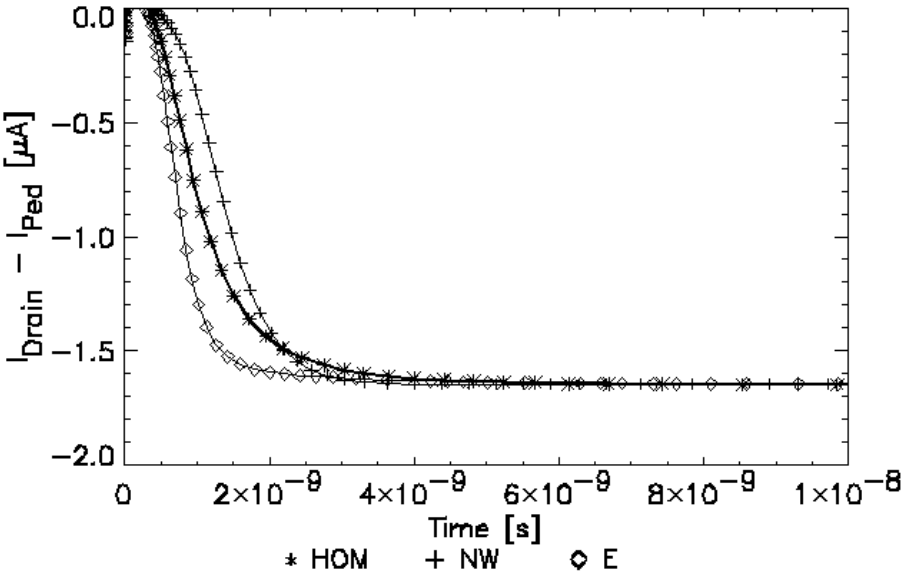


Figure 4.8: Simulated charge collection with ME implantation and an additional field shaper, the lines correspond to different points of incidence of the simulated charge (1600 e^-), from [30]

4.7.1 Requirements

The fast readout with row processing times of approximately 50ns requires both a short charge collection time and a fast clear process.

Charge collection time The short charge collection time is already obtained due to the charge collection by drift. Thus each fully depleted detector exhibits this feature.

A closer look however shows that close to the electronic side of the DEPFET regions with low electrical fields existing. This means that the charge collection is partially due to diffusion. This leads to an increase of the charge collection time. The simulated response of a DEPFET pixel to a charge of 1600e- is depicted in 4.8. After optimization with additional drift fields a charge collection time of 4ns is achieved.

Clear process Also the clear process needs special attention. The time to perform a full clear must be small compared to the row processing time. To achieve a fast clear with moderate voltages it is necessary to have a high reach-through of the electrical field of the clear towards the internal gate. This assures that the charge is collected by drift and not by diffusion.

An important device related parameter which determines the required clear

voltage is the depth of the internal gate. The closer the internal gate is located to the external gate the higher is the coupling towards the external gate. To remove the charge higher fields are necessary to overcome this barrier.

Two measures to assure a full clear at moderate clear voltage have been investigated in the last prototyping productions PXD4 and PXD5:

- HE (high energy implant; PXD4)
- ME (medium energy implant; PXD5)

The depth of the internal gate can be varied with the mentioned additional (global) implantations. In the PXD4 production the HE (high energy) implantation has been investigated. It moved the internal gate 1000nm below the channel (600nm without HE).

In the latest production PXD5 the ME (medium energy) implantations has been used. The ME is a tradeoff between HE and without HE.

However with increasing depth the coupling of the internal gate toward the channel is suffering. The parasitic coupling towards neighboring electrodes is increased which leads to a decrease of the internal amplification.

Small pixel sizes To obtain the required pixel of $24 \cdot 24\mu\text{m}^2$ a technology allowing to use two poly silicon layer and two metal layer for routing has been developed.

Besides this it was necessary to develop a layout allowing a compact design. The commonly used circular structures [41, 49] does not allow pixel sizes sufficient for the ILC. Moreover the circular structures suffer under a long clear times O(100ns) and small internal amplification.

The solution to this problem are the linear structures proposed in [63]. The linear structures allow a periodic coverage of the whole area with pixels. Two neighboring columns share a common clear contact. A further reduction in size is achieved by combining two adjacent rows into double pixels with a common source and distinct drains.

Radiation hardness Also the radiation hardness requirements of the ILC and in HEP in general also triggered developments to increase the radiation hardness of the DEPFET technology, see chapter 17.

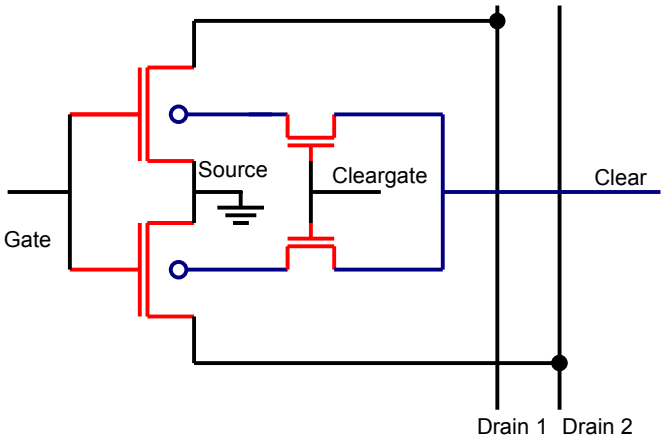
4.7.2 ILC layout

Double pixel layout The previous considerations lead to the layout depicted in figure 4.9. The basic building block of a matrix is shown: the double cell.

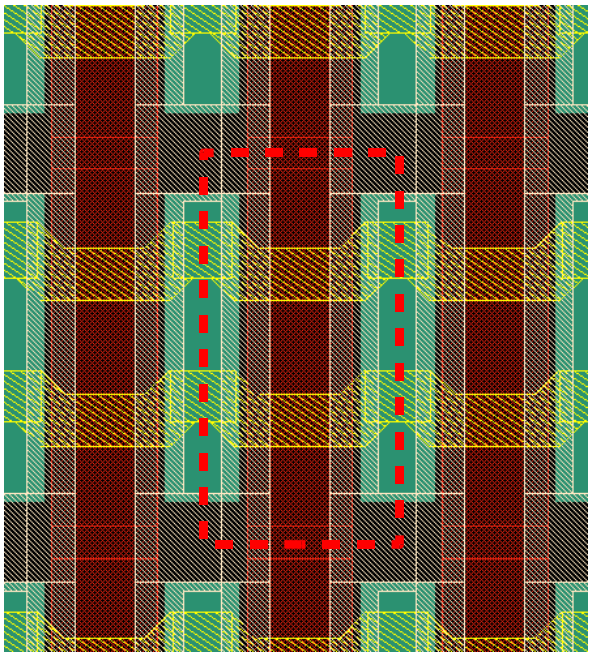
The double cell has a common source and gate. Each double cell shares common steering voltages - the clear, clear gate and gate. The two drains are connected to separate drain buses.

Besides the compact design it is possible to increase the readout speed by a factor two due to the simultaneous processing of two rows. The drawback of this approach is decrease of the readout pitch to 12μm for a pixel size of 24μm.

Pixel sizes down to 20μm have been produced.



(a) Schematic of a double cell



(b) Layout of a double cell

Figure 4.9: DEPFET double pixel structure [63]; Double pixel cell indicated in red - two adjacent cells of a row share a common clear contact (in green), each cell has a common source, source and drain implantation in red, gate in yellow; the metal layers are not shown.

Chapter 5

DEPFET based applications

This chapter gives a short summary of applications of the DEFPET detector concept besides ILC.

Most of the applications heavily exploit the following properties of the DEFPET technology:

- low input capacitance
- very low leakage current of $\approx 100 pA/cm^2$ at room temperature
- thin entrance windows, allowing x-ray detection down to carbon (250eV).

These attributes make the DEPFET attractive for various x-ray imaging projects introduced in 5.1.

A slightly adapted variant of the DEPFET which has an approximately logarithmic response is envisaged as focal plane detector for the free electron laser XFEL, see 5.3.

The repetitive non destructive readout (RNDR) allows to beat the noise limits posed by the low frequency noise. This permits to achieve noise figures better than $0.3e^-$ [89].

Also in high energy physics a new application emerged - the upgrade of the silicon vertex detector (SVD) of the Belle experiment located at KEK in Japan.

Even beyond the mentioned applications the DEPFET is continuously improved and new flavors like gateable devices are developed.

5.1 DEPFET in X-ray imaging

The requirements in x-ray imaging for space applications are determined by the resolution of the optics and the required energy resolution. The coarse angular resolution of the x-ray optics allows using large pixels without challenge the performance of the instrument.

Moreover large pixels reduce charge sharing thus leading to a better noise performance. The frame rates for such imagers could be high while still having a row rate below 1MHz. These applications are much slower compared to detectors in high energy physics or at XFEL.

The physical limit of the achievable energy resolution is given by the Fano limit (counting statistics of the created charge carriers) thus a readout noise of $\approx 3.5e^-$, like reported in [79], allows a Fano limited measurement.

IXO IXO (former XEUS) is a satellite based x-ray observatory. It is intended to study for example black holes and their evolution and the formation large structures [15].

Besides instruments for high time resolution astronomy, hard x-ray detection and a calorimeter, the IXO mission will use DEPFET a based wide field imager. It will consist of a matrix of 1024*1024 with a pixel size of $75 \cdot 75\mu\text{m}^2$. The use of active pixel sensors allows new readout schemes like the definition of region of interests where the frame rate is increased.

Bepi Colombo is a planetary mission to mercury. The MIXS instrument will measure fluorescence photons from the mercury surface excited by solar protons. This allows to investigate the chemical composition of the mercury surface [80].

The focal plane detector of this instrument is like for Simbol-X, a combination of a drift structure with a DEPFET. The detector consist of an array with 64*64 pixels and a size of $300 \cdot 300\mu\text{m}^2$.

5.2 RNDR

The repetitive non destructive readout allows reducing the noise below the physical limits due to low frequency noise. A single measurement is limited by this noise; by repeating independent measurements on the same charge this limit could be overcome.

The RNDR structure consists of two neighboring DEPFETs connected with a transfer gate. By applying the roper potentials the charge collected in one DEPFET could be moved to the neighboring one thus allowing independent measurements. An ENC of $0.28e^-$ has been achieved, allowing the detection of single optical photons [89].

5.3 FEL instrumentation

The instrumentation on free electron lasers like the XFEL requires extremely high dynamic ranges. Since many photons are collected by a pixel the figure of merit is not the maximal achievable resolution given by the Fano noise, these applications require the Poison limited counting of photons in range from one to $O(10^4)$ photons.

The "analog compression" DEPFET achieves this large dynamic range with a increase of the size of the internal gate and a appropriate shape of the internal gate potential [49].

Small charges are directly located under the gate thus having a large amplification and large charges are distributed broadly thus having a small amplification. In this way a logarithmic response could be achieved.

The bunch structure of XFEL is similar to that one of TESLA. The aim of the detector is to have a time resolution which allows a separation of individual bunches. The goal is a frame time of 200ns. To achieve this a hybrid approach will be used. Each pixel will have its own readout channel with amplifier, ADC and digital storage.

5.4 Belle upgrade

Besides the ILC a second application in high energy physics is envisaged for the DEPFET - the upgrade of the silicon vertex detector at the Belle experiment at KEKB; the SuperBelle project. KEKB is a b-factory operating at the $\Gamma(4S)$ resonance at a center of mass energy of 10.5GeV. It is foreseen to upgrade the luminosity towards $10^{36}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ an increase of two order of magnitude.

Due to the low center of mass energy the momenta of the particles are limited compared to ILC where an excellent IP resolution is essential over a broad momenta range. However low momentum tracks suffer from strong multiple scattering therefore the pixel size could be large without affecting the IP resolution.

The backgrounds at SuperBelle have different origin than at ILC. The colliding beam are quite large O(1μm) so that beamstrahlung does not play a role, see equation 3.6.

Synchrotron radiation created by the beam optics and beam gas interaction is the dominant source of background in the detector. To achieve a reasonable occupancy a frame rate of $10\mu s$ is required. Taking into account the larger pixel size of $75 \cdot 50\mu m^2$ and the possibly of a fourfold readout (larger pixel allow more metal lines) a row rate 12.5MHz (80ns) will allow the frame time of $10\mu s$.

Radiation hardness is also an issue for SuperBelle. The expected ionizing dose is around 1-5 MRad per year thus being significantly higher than for ILC.

Chapter 6

Noise in semiconductor devices

A limiting factor in virtually every measurement is noise. In case of position sensitive detectors like the DEPFET it limits both the detection efficiency and the position resolution of the detector. This chapter introduces the basic physics behind the noise, the different sources and discusses them with respect the figure of merit the equivalent noise charge (ENC).

For further reading [74, 48] could be recommended.

6.1 Impact of noise to the system performance

6.1.1 Efficiency and fake hit rate

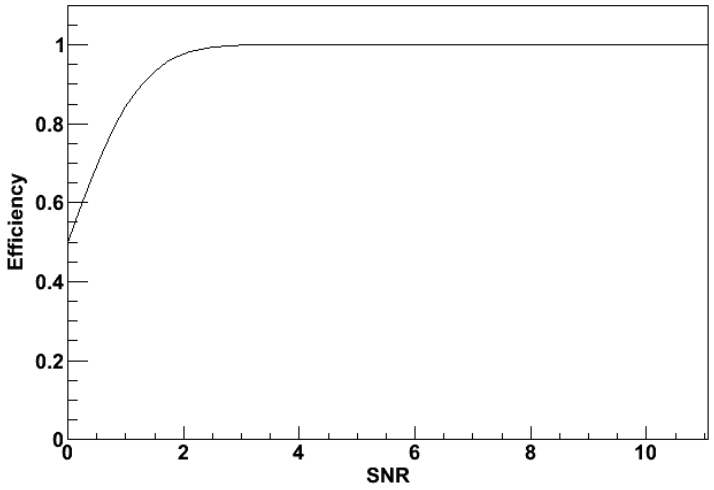
A important aspect related to the noise is the efficiency of detection and the fake hit rate. The efficiency gives the fraction of particles which are actually detected.

Hits below the threshold are regarded as noise - error of the second kind. Fake hits are produced when a fluctuation is assigned to a hit - error of the first kind.

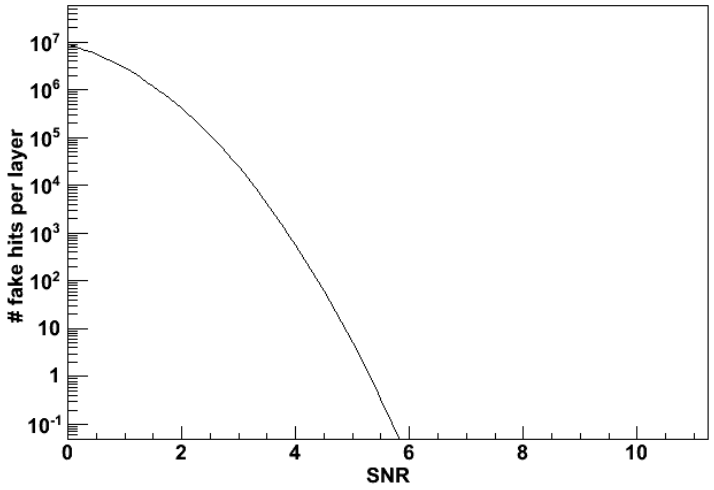
Figure 6.1 shows both the efficiency and fake hit rate versus the SNR. The calculation assumed Gaussian noise as well as a Gaussian distribution of the signal. This is an idealization; in reality the noise could have non Gaussian contributions ("heavy tails"), which further increase the number of fake hits.

The number of fake hits is calculated via $p_{fake}N_{pixel}$ as product of the probability to assign a noise fluctuation as hit and the number of pixel in a layer. 18M pixels were assumed which is equivalent to the number of pixel in the first layer.

Conclusion At a SNR of 4 the number of fake hits is already as high as the number of background hits per bunch crossing in the first layer (400 Hits/BX) - doubling the occupancy and the required bandwidth of a zero suppressed



(a) Efficiency vs. SNR



(b) Number of fake hits per readout in the inner layer

Figure 6.1: Calculated efficiency and fake hit rate vs. SNR

readout. This simple analysis shows that a low SNR could have a severe impact on the performance of a detector.

6.1.2 Resolution

As seen in section 3.3 the single point resolution is an important parameter to reach the required impact parameter resolution.

A simple algorithm to calculate the position from the measured cluster is the center of gravity (COG). Assuming a size of the cluster of at least 2 the position can be calculated by

$$X_{cog} = \frac{\sum x_i S_i}{\sum S_i}, \tag{6.1}$$

where x_i are the coordinate of each pixel and S_i the respective signal of the pixel.

By applying the error propagation formula the error of such a position measurement could be derived as

$$\sigma_{X_{cog}} = \sqrt{\sum_i \left(\frac{x_i}{\sum S_j} - \frac{\sum S_j x_j}{\sum {S_j}^2} \right)^2 \sigma_s^2}. \tag{6.2}$$

σ_s is the variance of the signals S_i. Assuming that the cluster consists of two hits it is possible to simplify the formula to

$$\frac{\sigma_{X_{cog}}}{P} = \frac{1}{SNR} \sqrt{1 - 2\frac{x_{cog}}{P} + 2\left(\frac{x_{cog}}{P}\right)^2} \text{ [82]}. \tag{6.3}$$

P is the pitch of the detector.

This analysis assumes that the noise is not correlated which is true in case of the DEPFET, where the coupling (capacitive) is very small, thus correlations are also expected to be small. This is different to strip detectors where strong correlations are found [47]. In addition the signal fluctuation due to δ-rays are neglected.

The commonly used η algorithm shows the same behavior with respect to the SNR [82]. Thus the dependence of the resolution on the SNR is quite general.

The following chapters will show a broad analysis of the DEPFET with respect to the intrinsic noise, internal amplification and clear performance - the necessary ingredients to achieve an optimal SNR.

6.2 Noise sources in semiconductor detectors

Semiconductor detectors are affected by the following sources of noise:

- white noise
- low frequency noise

- shot noise

Noise could be described by its spectral power density dP_n/df. For circuit analysis the voltage- and current spectral densities $e_n = dv_n/df$ and di_n/df (i_n) are commonly used. The overall voltage noise could be calculated as

$$v_n^2 = \int_0^\infty e_n^2 A^2\,(f)\,df \tag{6.4}$$

and similar for the current. A(f) is frequency depended gain of circuit. The formula simply exhibits the statistical character of the noise - the overall noise is obtained by calculating the quadratic sum in each frequency interval.

6.2.1 Thermal noise

Thermal or white noise is present in ohmic resistors as well as transistors. One can show that the power density of a resistor is equal to $dP_n/df = 4kT$ the deviation is found in textbooks like [48]. The spectral density is independent of the frequency, this holds up to a few GHz. For the investigations in the following it could be regarded is constant.

The respective densities for the voltage and current noise are given by:

$$v_n^2 \equiv e_n^2 = 4kTR \quad \text{and} \quad i_n^2 \equiv i_n^2 = \frac{4kT}{R}. \tag{6.5}$$

In case of a transistor the noise is given by

$$e_n^2 = \frac{\gamma 4kT}{g_m} \quad \text{and} \quad i_n^2 = \gamma 4kT g_m. \tag{6.6}$$

γ is an semi empirical factor. Textbooks give it typically as 2/3, real devices show a range between 0.5-1.

6.2.2 Low frequency noise

The source of low frequency noise also referred as 1/f noise is trapping and detrapping of carriers in dielectrics and semiconductors [36]. Especially MOSFETs are a strong source of low frequency noise, since the charge carriers are close to the surface where the trap density is high.

A single trap exhibits a Lorentzian noise spectrum, with a time constant τ depending on the energy level of the trap. Averaging the spectrum over many different time constant leads to a 1/f behavior of the spectral density, see for example [52]. The spectral density is commonly parameterized as

$$e_{n1/f} = \frac{A_f}{f}. \tag{6.7}$$

The formula shows that a simple low pass response which limits the white noise is not sufficient to limit the low frequency noise. To limit the contribution a low frequency cut off must be provided. A limited measurement time already provides a cutoff frequency of $\approx 1/T_{measure}$.

6.2.3 Shot noise

Shot noise is created by charge carriers, which are statistically created in a device, crossing a barrier. Typical representatives are the gate leakage current in JFETs and the reverse bias current in pn diodes. The current through an ohmic resistor exhibits no shot noise since the current flows due to the collective movement of free carriers.

Continuous readout The spectral density is given by

$$i_{shot}^2 = 2eI. \tag{6.8}$$

The formula is beneficial when dealing with time-continuous systems like RC-CR shaper.

Integrating readout In an integrating device like the DEPFET in matrix operation (see section 4.5) the shot noise could be directly derived from the poison statistics. When a leakage current I is integrated for a time T the number of collected charge carrier is IT/e. The standard deviation of this average value is given by

$$\sigma_{shot} = \sqrt{\frac{IT}{e}}. \tag{6.9}$$

Temperature dependence The leakage current in semiconductors is strongly depended on the temperature:

$$I_{leak} \propto T^2 \exp \frac{-E_g}{2kT}. \tag{6.10}$$

The energy gap in silicon is 1.2eV. Evidently the dependence is dominated by the exponential term for temperatures close to room temperature. Moreover it depends strongly on the number of mid gap states. This leads to a strong dependence on the processing and a sensitivity to radiation damage.

6.3 Response of readout schemes

The last section introduced the various noise sources and their origin. The different spectral densities however, are not sufficient to calculate the overall noise, see formula 6.4, since the frequency dependent gain is not further specified. The section introduces this quantity in case of the RC-CR shaping and the correlated double sampling (CDS).

6.3.1 Response of RC-CR shaping

RC-CR shaping is commonly used in shaping amplifier, the shaping is achieved by consecutive RC-CR elements, low pass - high pass filter thus being equivalent to a band pass providing efficient limitation of the bandwidth. This limits the contribution of the white noise as well of the shot noise.

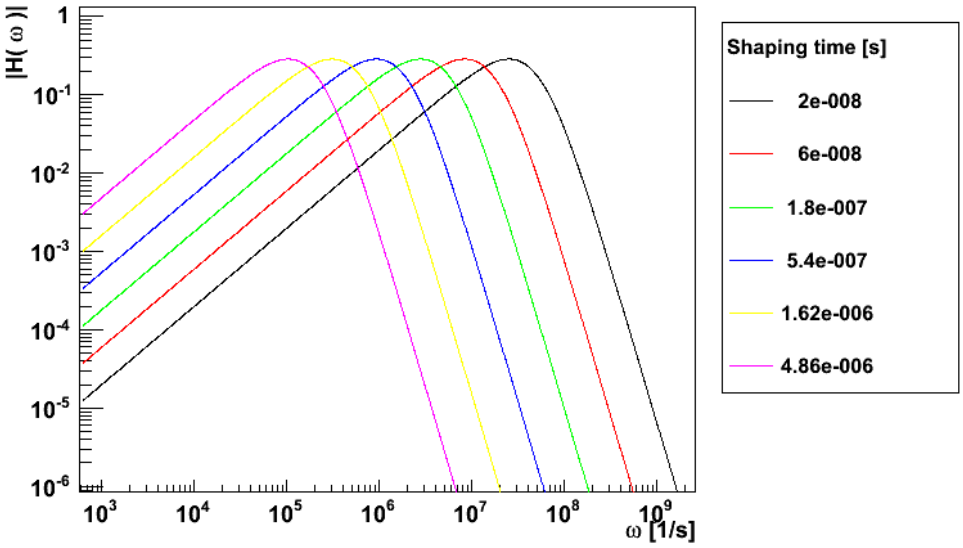


Figure 6.2: Response of time continuous RC – CR^4 shaping

Typically a single differentiator C-R - is followed by n R-C elements. The response of this configuration is

$$H(\omega) = \left[\frac{j\omega\tau}{1+j\omega\tau}\right]\left[\frac{1}{1+j\omega\tau}\right]^n \text{[69]}. \tag{6.11}$$

τ is the RC time. Commonly a first differentiator (C-R) is followed by an 4-fold integrator (R-C). The absolute value of for RC – CR^4 is depicted in figure 6.2.

Noise and RC-CR shaping The overall noise in the spectroscopic chain taking into account the previously mentions contributions commonly expressed in the following form:

$$ENC = \sqrt{\alpha\frac{2kT}{g_m}C_{ox}^2 A_1 \frac{1}{\tau} + 2\pi a_f C_{ox}^2 A_2 + I_L A_3 \tau} \text{ [31]} \tag{6.12}$$

The numerical factors A_i are depending on the concrete implementation of the shaper, numbers for various schemes could be found in [31].

In case of the DEPFET it is more convenient to use a different parameterization:

$$ENC = \sqrt{\alpha 2kT\frac{g_m}{g_q^2}A_1 \frac{1}{\tau} + 2\pi a_f C_{tot}^2 A_2 + I_L A_3 \tau} \tag{6.13}$$

This expression accounts for the fact that exact proportionally is not valid for all operation conditions, see chapter 9. Both equations a equivalent as long as $g_q = 1/C_{ox}g_m$ holds.

Discussion The total capacitance C_{tot} is the capacitance where the charge is collected. This capacitance determines the effective voltage change $\delta U = Q/C_{tot}$ and thus the signal.

In the general case this capacitance is the sum of the gate source capacitance of the readout transistor and additional capacitances due to connections (traces on a circuit board, pads and bond wires).

In case of the DEPFET it is approximately the oxide capacitance C_{ox}.

Since the capacitance shows up in two of the summands it is important to keep it as small as possible.

However it is also possible to perform a tradeoff between the capacitance and g_m in case of the white noise via scaling of the transistor, which also improves the 1/f noise due to the reduced area of the transistor[1].

The second summand is independent of the bandwidth, since a decrease in bandwidth is balanced with the equivalent increase in 1/f noise. This is also visible in figure 6.2 - a decrease of the shaping time, in the figure a factor 3 per graph, leads to a translation of the curve along the x axis. This means that the bandwidth is changed by the same factor.

6.3.2 Response of CDS

The correlated double sampling is standard method for the signal processing of DEPFET matrices. By taking the difference of two consecutive current or voltage samples before and after the clear the pedestal currents are efficiently removed but also the low frequency is suppressed. The latter could be simply understood by assuming that a fluctuation with a certain frequency and amplitude is present on the signal. By subtracting two samples close to each other in time the amplitude of this fluctuation is reduced the smaller the time difference is.

The response CDS is

$$H(\omega)^2_{CDS} = 2\left(1 - cos\left(\omega\tau_{cds}\right)\right). \tag{6.14}$$

The formula shows that CDS provides a high pass response but for higher frequency no further bandwidth limitation. However the electronics which performs the CDS is bandwidth limited - in case of the CURO see [81] - around 50 MHz.

The response of low pass filter of n^{th} order with cutoff frequency ω_{cut} is given by:

$$H(\omega)^2_{LP} = \frac{1}{\left(1 + \left(\frac{\omega}{\omega_{cut}}\right)^2\right)^n}. \tag{6.15}$$

In frequency space the final response is simply the product of both formulas:

$$H(\omega)^2_{final} = H(\omega)^2_{LP} \cdot H(\omega)^2_{CDS}. \tag{6.16}$$

[1] 1/f depend on the number of interface states thus on the area

CDS and thermal noise The thermal noise of a readout using CDS could be calculated analytically for a first order low pass filter leading to

$$u^2_{thermal} = 2e^2_n \omega_{cut} \left(1 - \exp\left(-\omega_{cut}\tau_{CDS}\right)\right). \tag{6.17}$$

This formula reveals two features:

- CDS increases the white noise by a factor of $\sqrt{2}$ compared to a single sample
- the noise is decreased when $\omega_{cut}\tau_{CDS} \geq 1$

The first is due to the difference of two independent samples. The second feature is only an artifact since $\omega_{cut}\tau_{CDS} \geq 1$ means that the samples are taken faster than the settling time of the low pass filter. Thus the signal is reduced.

CDS and 1/f noise The contribution of low frequency noise could be calculated similarly:

$$u^2_{1/f} = \int_0^\infty \frac{a_f^2}{\omega} H\left(\omega\right)^2_{final} d\omega \tag{6.18}$$

CDS and leakage current Leakage current is accumulated before the readout phase, thus is not to distinguishable from signal. The difference of the two samples before and after the clear exhibits the full contribution of the shot noise.

The shot noise is given by:

$$ENC_{shot} = \sqrt{T_{int}\frac{I_{leak}}{e}}. \tag{6.19}$$

The formula shows that the contribution of shot noise becomes smaller the faster the readout is performed.

Chapter 7

R&D towards an ILC module

This chapter gives an overview of the research and development towards an ILC module. It is foreseen to construct a full silicon module. The thin silicon is supported by a frame. This concept allows reducing the material in the active area to a minimum. Moreover additional support structures like rigid foams are not necessary.

The first section describes the thinning technology. The steering ASICs are directly connected to this module. A interconnection technology for this purpose is shown in the second section.

Section 7.3 deals with the ASIC development: the frontend and the switcher ASICs. The switchers are of special importance since they determine the accessible parameter space for the clear process.

7.1 Thinning technology

The material budget requires that the thickness of the DEPFET matrices is reduced towards 50 to 100 μm. The double sided processing in the DEPFET technology makes it necessary to develop a compatible thinning technology. Processes which are used for the thinning of CMOS ASICs or CMOS based MAPS [19] are not compatible with the DEPFET technology.

Process flow The process flow of the thinning technology is shown in figure 7.1. The process utilizes two wafers a handling wafer for mechanical stability and a top wafer where pixels are placed. A commercial available wafer to wafer bonding technology is used to make a mechanical connection of both wafers, the top wafer has already the backside implants. After the bonding a strong mechanical connection is established allowing grinding and polishing the top wafer to the desired thickness, step (b).

After the thinning the resulting wafer could be processed on the top side. Alignment marks, visible in infrared light, on the backside allow a precise adjustment with respect to the top side. When the top side processing is finished the surface is passivated and the backside passivation is opened for the further processing. Finally the handle wafer is removed via deep anisotropic etching. The remaining handle wafer serves as frame for the thin silicon foils.

The bow under gravity of a full sized mechanical sample was measured. It was found that due to build in stress a bow of 100μm exists. The change under gravity is around 20μm. This means that the module could be regarded as mechanically rigid.

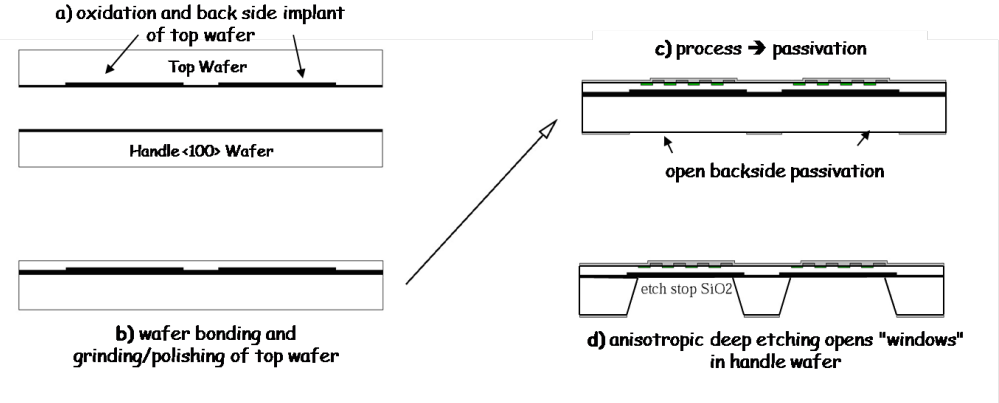


Figure 7.1: Process flow of the thinning technology, taken from [12]

Electrical characteristics Besides the mechanical issues it is important that the excellent leakage currents are preserved while processing. An increase of leakage would have direct impact on the system performance since the shot noise would increase.

A batch of diodes has been processed to investigate this issue. The distribution of the measured leakage currents is shown in figure 7.2. The results show that, besides a few exceptions, the current density remains excellent.

7.2 Interconnection technology

As shown in chapter 4 steering ASICs are essential for the operation of a matrix. The requirements for the interconnections are driven by the reliability and the pitches of the connection. Wire bonds may be unreliable when operated with variable currents in a strong magnetic field, see [21].

For research and development a gold stud bump bond technology is currently investigated. A mechanical sample chip with gold stud bonds in depicted in figure 7.3.

7.3 ASIC development

7.3.1 Frontend

The frontend performs the correlated double sampling. The digitization is performed in an external ADC or directly on the chip. The frontends are based on

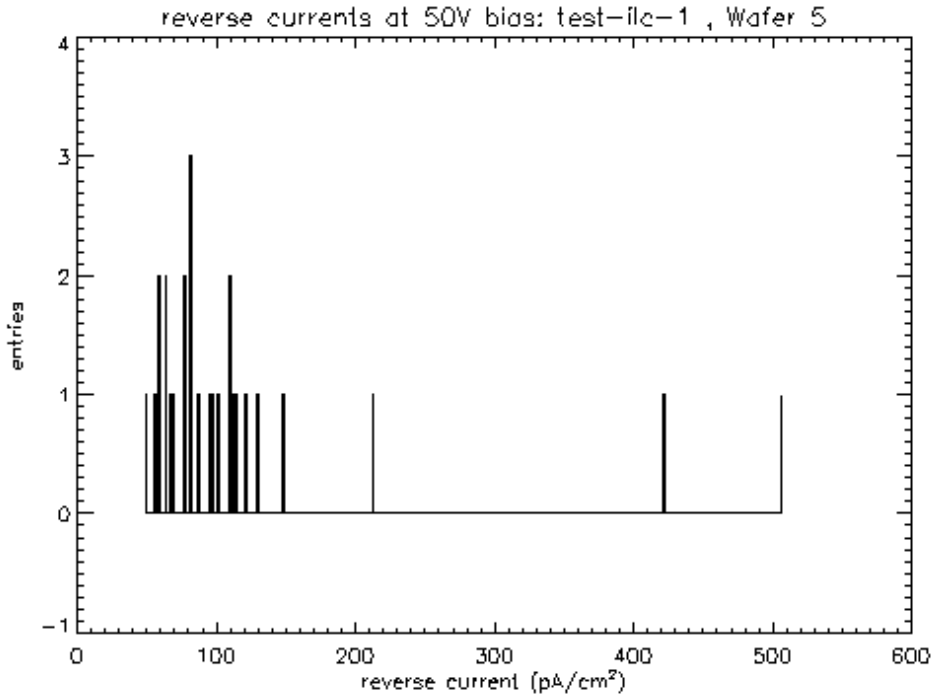


Figure 7.2: Leakage current after thinning, taken from [12]

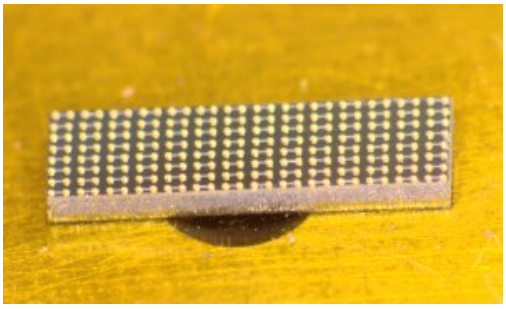


Figure 7.3: Mechanical sample with gold studs

the drain readout, as introduced in section 4.4, to meet the timing requirements.

CURO The CUrent ROout (CURO) belongs to the first generation of frontend chips [81]. A a layout of one of the 128 channels is shown in figure 7.4. The first building block is the cascode, which provides a low impedance input. The dynamic range of the cascode is sufficient to sink the whole current of a DEPFET.

Measurements are performed in the following way: Current of the first sample is stored in a memory cell, the clear is performed and the current of the DEPFET is subtracted from the current in the storage cell. The remaining signal current is stored in one of two current buffers. This design allows reducing the speed of these buffers by a factor 2. The signal currents are stored in an analog memory. A multiplexer allows processing the signal currents externally. Optionally an integrated zero suppression allows making a simple clustering.

The CURO has an equivalent input noise of 110nA. Assuming a g_g of $500pA/e^-$ a noise of $220e^-$ is achieved. As pointed out in 8 the intrinsic noise of the DEPFET is significantly smaller thus the noise is dominated by the frontend.

A processing time of 280ns per row has been achieved with the CURO with is related to the fact that for R&D the full analog information is used and thus the readout is limited by the multiplexer.

DCD The Drain Current Digitizer (DCD) is intended to overcome the limitations of the CURO. The DCD allows separating the hit finding from the analog processing. The concept allows using a technology well suited for analog electronics for the DCD and a fast technology with small feature sizes for the digital data processing.

The layout of the DCD is shown in figure 7.5. The first stage performs an analog difference of the two currents similar to the CURO. The cascodes are improved providing a lower noise and adapted to the expected load capacitance. In the following step the signal current is immediately digitized with an 8Bit ADC per pixel (actually two ADC working at half of the speed). An algorithmic ADC is used due to the small size.

The digitized signals are distributed via 6 LVDS links operating at 600MHz. In the first stage a FPGA will be used for data processing. This allows studying algorithms for fast analysis - pedestal subtraction, common mode correction and clustering. In a second step this algorithms will be implemented in a dedicated digital chip.

The performance goal of the current DCD generation is to achieve an equivalent input noise of 50nA at a row processing time of 80ns.

7.3.2 Switcher

The switcher ASICs provide the steering strobes for the DEPFET on the gate and the clear. The switcher must withstand the expected radiation while pre-

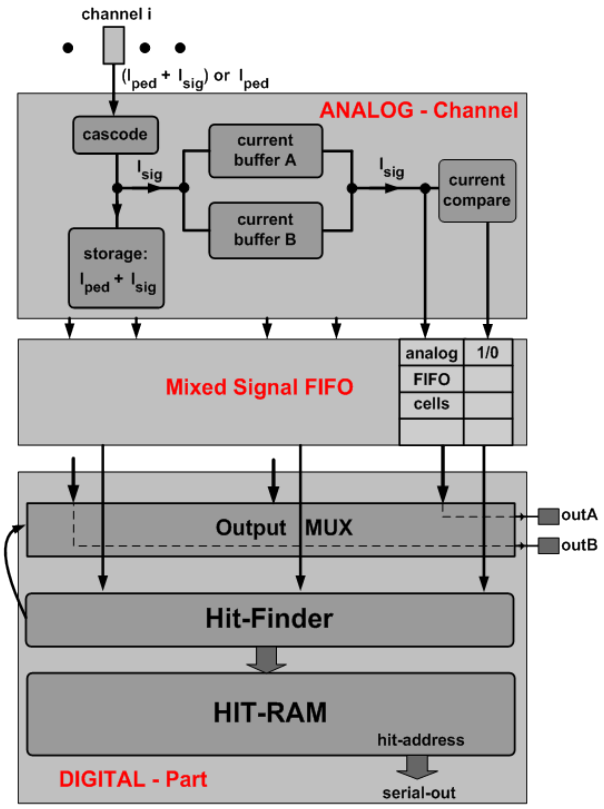


Figure 7.4: Layout of a CURO channel. The cascode provides a low impedance input, the CDS is performed analog via current storage cells. The output current are stored in a mixed signal FIFO and can be directly multiplexed out or processed via an digital hit finder [81]

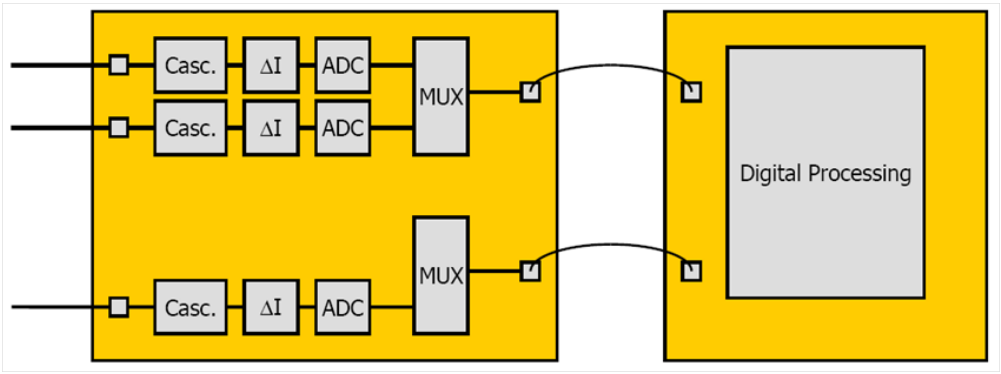


Figure 7.5: Layout of the DCD. After the analog CDS the signal current are directly digitized with an 8bit ADC per channel. Zero suppression can be implemented in a dedicated digital signal processor ASIC

serving the speed and have to provide a voltages in range of ≈ 10V. The difficulties involved in the development of such circuits are the radiation hardness combined with large voltages required for the operation of DEPFT. Modern CMOS processes are intrinsic radiation hard due to their thin oxides (≈10nm). However these thin oxides reducing the operation voltages.

The accessible parameter space of switcher ASICs is limited. An important question related to this is: What are the required voltages to perform a complete clear? Chapter 11 finds an answer to this.

Switcher 2 The switcher 2 is produced in a high voltage technology thus allowing to switch up to 22V [56]. But the radiation hardness is only $\approx 20kRad$. This version is widely used for the characterization in test beams as well as in the laboratory.

Switcher 3 The switcher 3 was intended to overcome the limitations of the previous generation. The radiation hardness is achieved by the use of a radiation hard $0.25\mu m$ technology. However the supply voltage is only 3.3V, far below the voltage to achieve a full clear.

This disadvantage is avoided by utilizing a special feature of the technology which allows isolating the transistors against the bulk. This allows to build a chain of transistors in which a single transistor experience only a voltage drop in the allowed range, see figure 7.6.

The AC coupling reduces the power dissipation to a minimum since no standing current are flowing when the switcher is in off state. Experimental tests showed that the switcher 3 can handle up to 12V without damage.

A hybrid incorporating the switcher 3 was developed within this thesis [66].

Switcher 4 The most recent development for this purpose is the switcher 4. The switcher 4 is intended to increase the switching capabilities further utilizing a special type of MOS transistors; the Double diffused MOS - DMOS [58]. A rough sketch demonstrating the principle of a DMOS is shown in figure 7.7. The thick oxides close to the drain allow the FET to withstand high gate-drain voltages. The thick p- region limits the maximal fields around the source since the voltage drops occur over this region.

The switcher 4 is still under development. The expected voltage range of more than 20V makes him very attractive, since this switcher would allow to access a parameter space where the internal amplification and the clear performance is optimal, see chapter 11.

Switcher 5 The switcher 5 is the successor of the switcher 4. It is based on the same technology thus allowing switching the same voltages as its predecessor. Furthermore it is optimized for the requirements of high energy physics namely: integrated level shifter will allow to set voltages digitally for each ASIC independently [57].

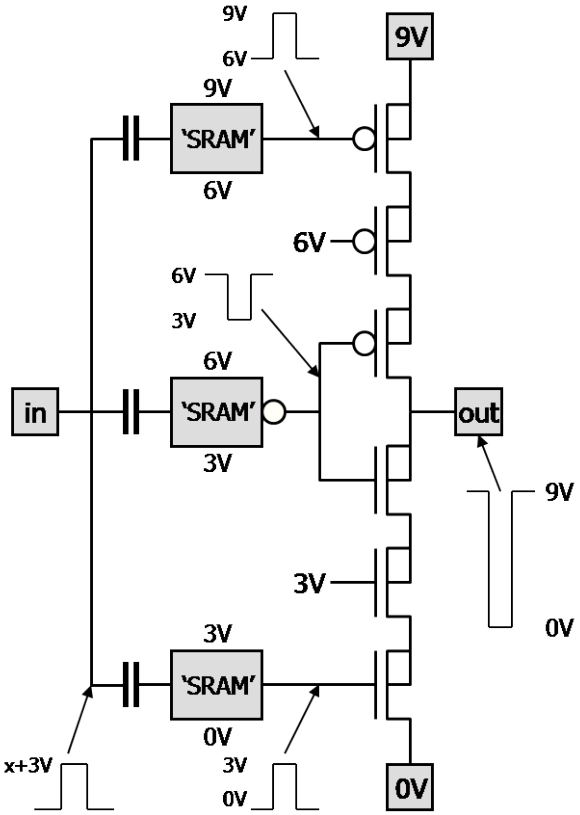


Figure 7.6: Switcher 3 schematic [29]

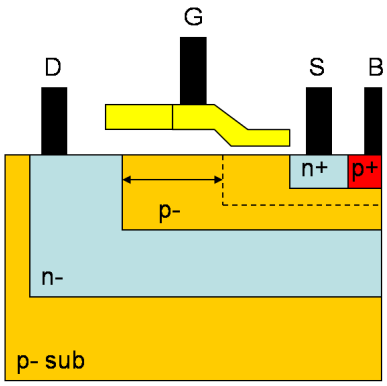


Figure 7.7: High voltage DMOS transistor, taken from [58]

The switcher 5 will allow to adapt the steering voltages with high spatial granularity as required from the radiation damage and possible inhomogeneities, see 16.

7.4 Module layout

The layout of a full module is shown in figure 7.8. The readout direction is along the long side of a module. This allows placing the power consuming frontend ASICs at the end of a ladder. The drawback of this approach is the high capacitive load at the frontend due to the long readout line and the high row rate necessary to meet the frame time requirements.

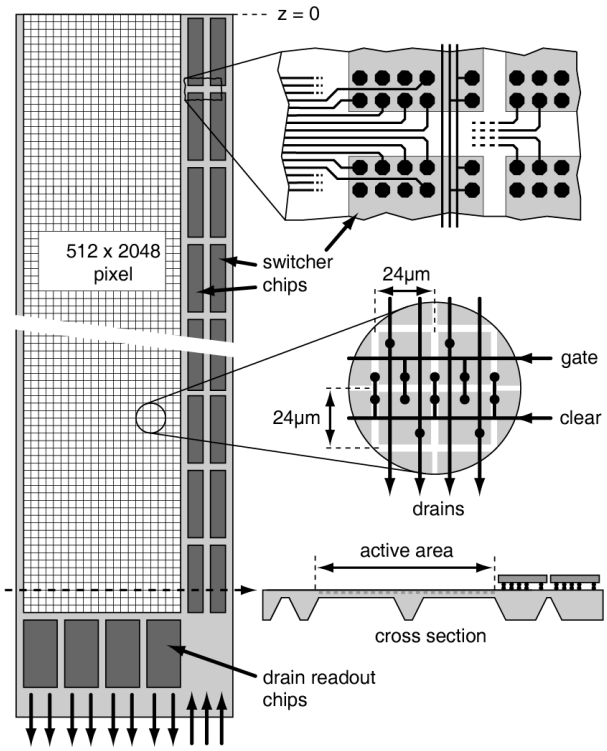
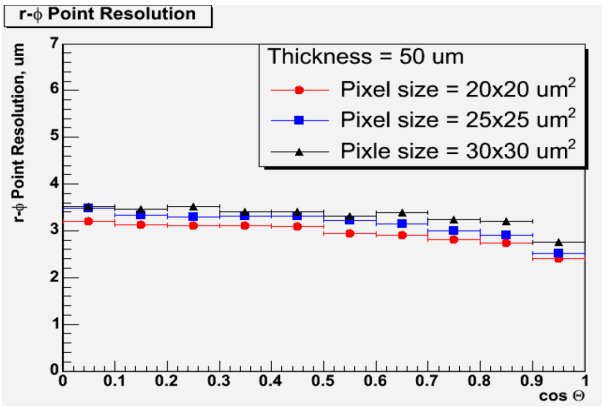


Figure 7.8: Layout of a half module in layer 1

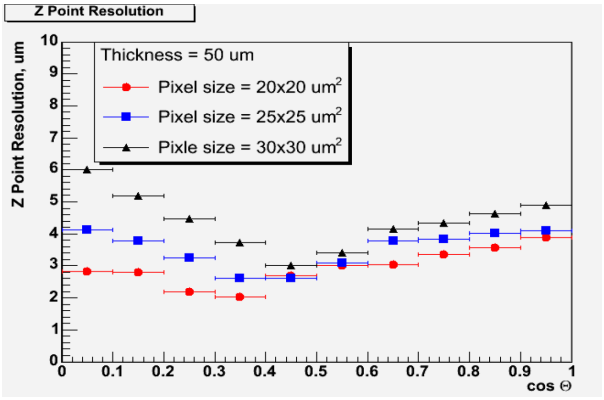
7.5 Performance of a DEPFET VTX detector

Various simulations have been carried out to evaluate the performance of a DEPFET based vertex detector. The impact parameter resolutions as well as the stability of the pattern recognition were studied within the ILD framework. The simulation of detector included the a realistic model for

- the charge sharing between pixels,
- Lorentz angle in magnetic field and



(a) Resolution in $r - \phi$



(b) Resolution in z

Figure 7.9: Single point resolution of thin DEPFET sensors, from [61]

- drift and diffusion;

allowing to simulate the expected point resolution. A crosscheck for the existing thick detector ($450\mu m$) was performed, showing that the simulation is reliable. A readout noise of $100e^-$ was assumed for the analysis.

Figure 7.9 shows the expected single point resolution in $r - \phi$ and z. While the first is homogeneous over the hole range the latter shows a optimum. This could be understood by the fact that the diffusion, which increases the charge cloud, is reduced in thin devices. In case of perpendicular traces the resolution is limited by the pixel size - digital limit. The further increase could be attributed to the further increase of the shallow tracks where the resolution suffers under landau fluctuations.

However the overall performance measured by the impact parameter resolution, see figure 7.10, shows that the requirements for the ILC are meet, compare to 3.3.

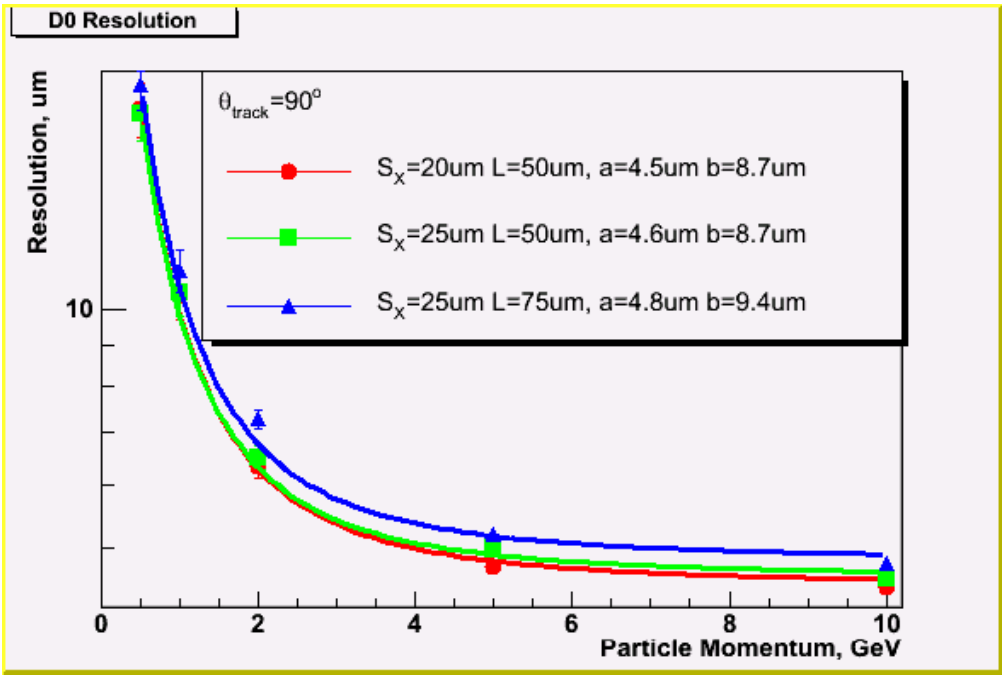


Figure 7.10: d_0 resolution, from [61]

Part I

DEPFET intrinsic properties

Chapter 8

Intrinsic noise of the DEPFET

This chapter presents the measurements of the noise contributions from low frequency noise, shot noise and white noise; considering the timing requirements for the ILC.

Special attention is given to the noise overall noise contribution at high bandwidth.

8.1 Leakage

The leakage current contributing to the shot noise has two sources: bulk generated leakage and surface generated leakage current. The measurement of the leakage current could be performed in two ways:

- direct current measurement on diode structures
- measurement on pixel level

While the first allows a direct measurement of the bulk generated leakage current, the second allows measuring both quantities in parallel. To judge the contribution to the noise it is advantageous to work on the pixel level since all type of leakage are present.

Setup The leakage current measurements were performed with the single pixel setup. This setup allows to investigate single pixels of dedicated single pixel structures or mini matrices with appropriate biasing.

Details about the single pixel setup could be found in [90].

Measurement The measurement was performed in the following way: the device under test was fully biased, a periodic clear was applied. A reference spectrum with Fe^{55}, which provides a signal of about 1620e$^-$ (5.9keV), was taken for calibration.

Two sampling strobes close after and before the consecutive clear allow a direct measurement of the charge flown into the internal gate.

Picture 8.1 shows a screen shot of an oscilloscope. The time is on the horizontal axis and the amplitude on the vertical. The amplifier is inverting thus higher current refers to lower voltage levels.

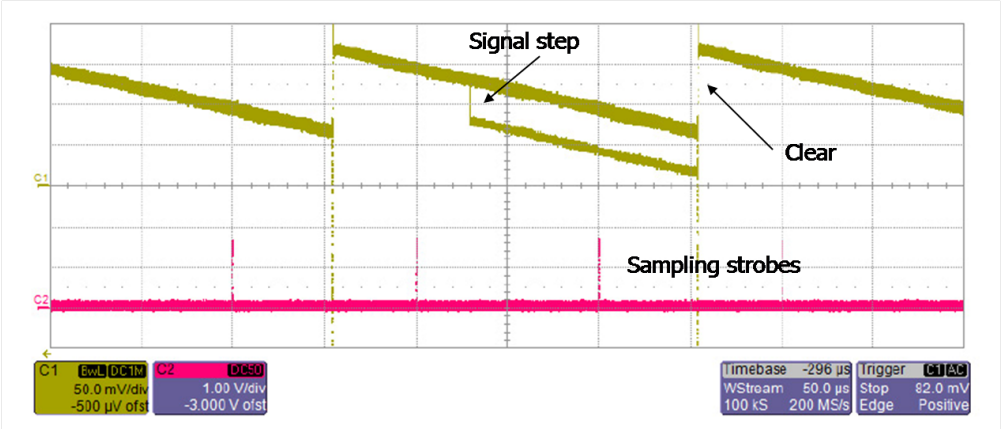


Figure 8.1: Method for leakage measurement; Yellow output of the DEPFET (50mV/div); Purple sampling strobes to trigger the ADC; Horizontal axis 50μs/div. Leakage current flowing into the pixel leads to the linear decrease visible (inverting amplifier). By comparison with a known signal charge - here Fe^{55} - the leakage can be directly measured.

The leakage current could be calculated as follows:

$$I_{leak} = \frac{S_1 - S_2}{d_{K_\alpha} - d_{noise}} \frac{1620}{T_{int}}. \tag{8.1}$$

T_{int} is the time between two samples and S_1 and S_2 are the amplitudes of the samples in $[ADU]$. $d_{K_\alpha} - d_{noise}$ is the distance of the noise peak and K_α peak measured in ADU.

Result A typical matrix exhibits a leakage current of 15fA per pixel at room temperature. Together with a frame time of 100μs a shot noise of below 4.3e$^-$ could be calculated.

The respective wafer had an leakage current of $200 pA/cm^2$. Taking into account the pixel size of the device of $24 \cdot 36 \mu m^2$ the shot noise contribution is expected to be 1.8fA per pixel.

Comparing the two numbers it seems that in the unirradiated state the leakage current is dominated by surface generation. The overall contribution to the noise is negligible. This situation changes when radiation damage is regarded, see chapter 14.

8.2 Low frequency noise

The low frequency noise is not directly accessible like the shot noise. Two variant are currently used:

- direct measurement with a spectrum analyzer
- indirect as noise floor of a shaper measurement

The first method is described in [60], while the second makes use of formula 6.12 where the low frequency component is visible as fixed term. Thus fitting it to a measurement with variable shaping time could also reveal the contribution of low frequency noise.

The results utilizing the first way are presented in chapter 19.2 where the low frequency noise contribution is calculated for various times between the samples. The calculation shows that the 1/f contribution for 40ns between the samples is 0.9nA which is equivalent to 2-3e depending on the internal amplification.

8.3 White noise at high BW

This section is the central section in this chapter. As seen in the first two section the low frequency noise and the leakage currents of secondary importance. The section will investigate the dominant noise source - the white noise.

8.3.1 Setup

The setup to measure the noise of the DEPFET at high bandwidth utilizes a low noise transimpedance amplifier from the type AD8015 [11]. This amplifier has a wide band noise of 26nA from 0 to 100MHz which provides an equivalent noise charge 26e^- for 1nA/e^- gain.

The second stage of the amplifier is made of an operational amplifier AD8129 which provides an additional amplification of 10 and the capability to drive the ADC which is terminated with 50 Ohm. The ADC has a 3dB bandwidth of 120MHz [35] which is fast enough for the envisaged measurements.

The bandwidth limitation was performed with low pass filter. A limitation of the used single pixel setup is the high capacitive load at the input of the amplifier due to the long traces on the circuit board.

The low pass filters are build from SMD components in the package size 1206 or even 0603 which have very small parasitic capacitance and inductance[1]. The usage of wired components is prohibitive due to their large parasitic impedances.

Determination of the setup bandwidth The experimental evaluation of the setup bandwidth is not trivial since parasitic capacitances have significant impact on it. This requires that the measurement is as close as possible to the final situation.

Finally the measurement was performed in the following way: The setup was used without any changes. The device under test (DUT) was biased normally besides the gate. The gate of the DUT was directly connected to a function generator providing the DC bias and a sinusoidal stimulus. Thus the current to voltage conversion was performed on DUT level and the setup is unchanged.

The amplitude depended gain could be derived as

[1] Even small SMD components have a parasitic capacitance of 200fF, at a frequency of 100MHz, the impedance of this capacitance is already as low as 8kΩ thus dominating e.g. the impedance of high valued resistors

$$G(f) = \frac{A(f)}{A(0)} \tag{8.2}$$

where $A(f)$ is amplitude of the stimulus at the output of the amplifier.

Figure 8.2 shows the measured gain for various low pass filters. The response of the filters up to LP04 is flat and shows a fast drop off. However the amplifier at the full bandwidth (depicted in red) and the filter LP01 (depicted in blue) show an enhancement of the gain of around 3dB at high frequency. This behavior also called "ringing" is acceptable as long as the amplifier is stable and shows no oscillations which is the case.

For a better comparison the quantity equivalent noise bandwidth ENB could be used. The ENB is defined as

$$ENB = \int_0^\infty A^2(f)\, df. \tag{8.3}$$

Thus the contribution of white noise could be simply expressed as

$$u_n = \sqrt{ENB * e_n}. \tag{8.4}$$

For example a first order low pass filter has an equivalent noise bandwidth of $\pi/2 f_{cut}$.

The measured -3dB bandwidth were corrected in the following way:

$$BW_{corr} = \int_0^{f_{-3dB}} A^2(f)\, df \tag{8.5}$$

The corrected bandwidth incorporates the fact that noise contributes stronger to the overall noise in the region of the ringing. The corrections are of the level of 20% for the three configurations with the highest bandwidth.

Intrinsic noise of the setup Since the amplifier has finite noise it is necessary to measure it. The intrinsic was evaluated in the following way: The DUT was turned off. Thus no current is flowing any more.

Due to the layout of the amplifier which allows adjusting the DC working point via the current subtraction resistor the amplifier could remain in the same state as in the actual measurement situations. All noise contributions (Amplifier, bias subtraction resistor and capacitive load) are still contributing.

8.3.2 Measurement

The measurements where performed on several test structures from the PXD4 production. Table 8.1 shows a summary of the investigated pixel structures. PXD4 J14 is a single pixel test chip with DEPFETS of variable gate length.

The HE implantation was used to improve the clear performance by increasing the depth of the internal gate. However it also reduced the gain since the parasitic couplings were increased too. The used structures, see table 8.1, are

Structure	W [μm]	L [μm]
PXD4 J14	20	4
PXD4 J14	20	5
PXD4 J14	20	6

Table 8.1: Structures where the noise contribution of the DEPFET were evaluated

without this implantation. The parameter space accessible with the single pixel setup allows performing a full clear with these structures.

The presented results are performed with correlated double sampling with a time of 800ns between samples at the maximal bandwidth. The relative long time is due to the fact that amplifier is outside its dynamic range for a short period while the clear pulse is applied. When a positive pulse is applied to the clear the transistor current is changed too. This is a similar effect like the steering capability of the bulk in a conventional FET.

8.3.3 Results

The results are shown in figure 8.3. Three different quantities are depicted - the overall noise ENC_{all}, the contribution from the amplifier ENC_{amp},measured as described in 8.3.1 and the difference calculated as

$$ENC_{DEPFET} = \sqrt{ENC_{all}^2 - ENC_{amp}^2}.$$

Amplifier contribution Evidently the amplifier contribution is the lowest in case of the $4\mu m$ device since it shows an g_q of around 900pA/e^-, see chapter 9. So the calculation of the difference is expected to perform well. This is different in a situation where a difference of two number with similar value is performed.

High frequency noise The measured noise at a frequency of 50MHz is around 45e^- for the $4\mu m$ device and 35e^- for the other. Even without performing the difference, as a conservative estimation, the first device has an noise below 50e^- and the other below 55e^-.

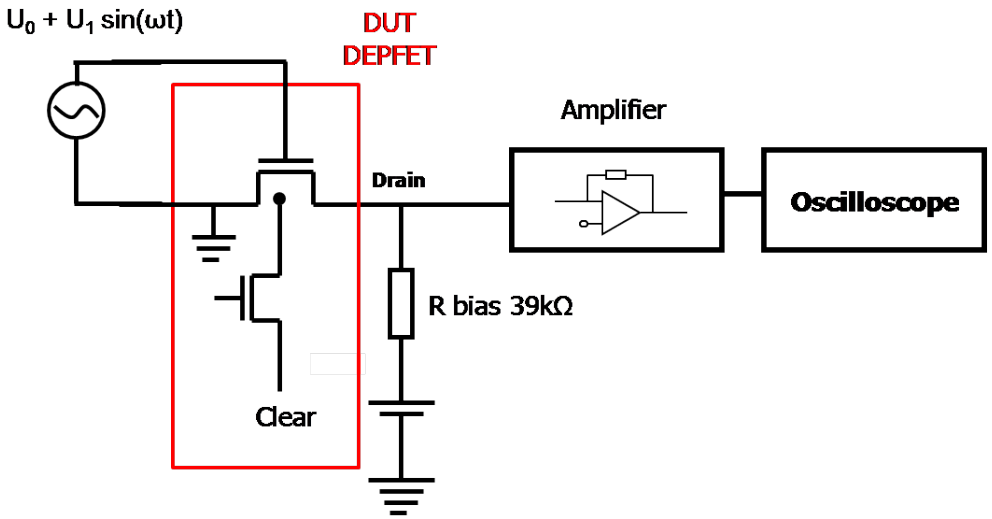
8.4 Summary of the intrinsic noise of the DEFPET

The analysis presented show that the white noise of the DEPFET is the dominating source of noise directly originate from the device.

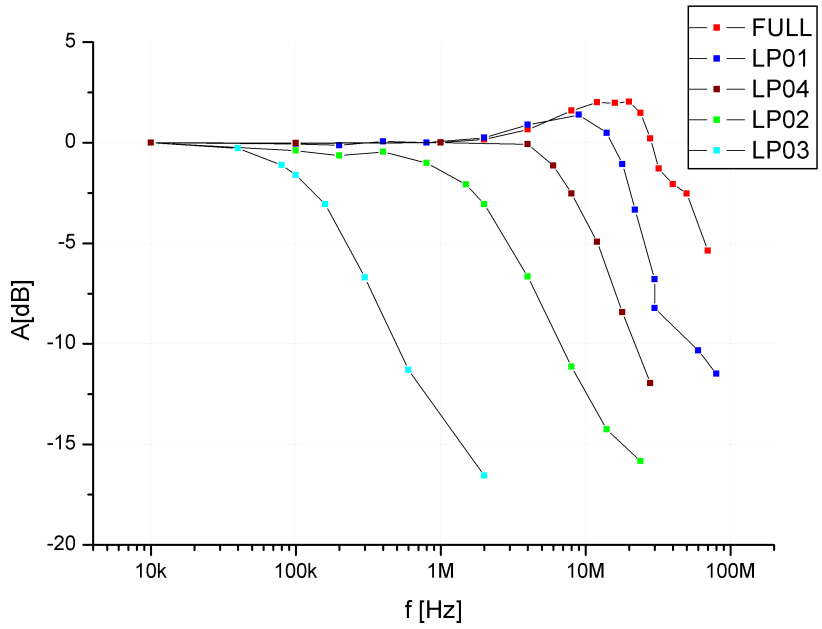
The leakage current and the low frequency noise are both below 5e^- thus being insignificant. However since both quantities are degraded with irradiation this analysis must be revised when radiation damage is regarded. This is performed in chapter 14 and 15.

The overall intrinsic noise of the DEPFET at a speed of 50MHz was demonstrated to be better than $50e^-$. The final performance goal is to achieve a SNR high enough to have efficient detection of particles with a 50 micron thick detector. This thickness gives a signal of $4000e^-$ for minimal ionizing particles. Assuming the worst case scenario of equal charge sharing between two neighboring pixel a detector with an overall noise of $100e^-$ would have a SNR 20.

This consideration shows that the low intrinsic noise gives enough room to allow additional contributions from the fronted electronics.

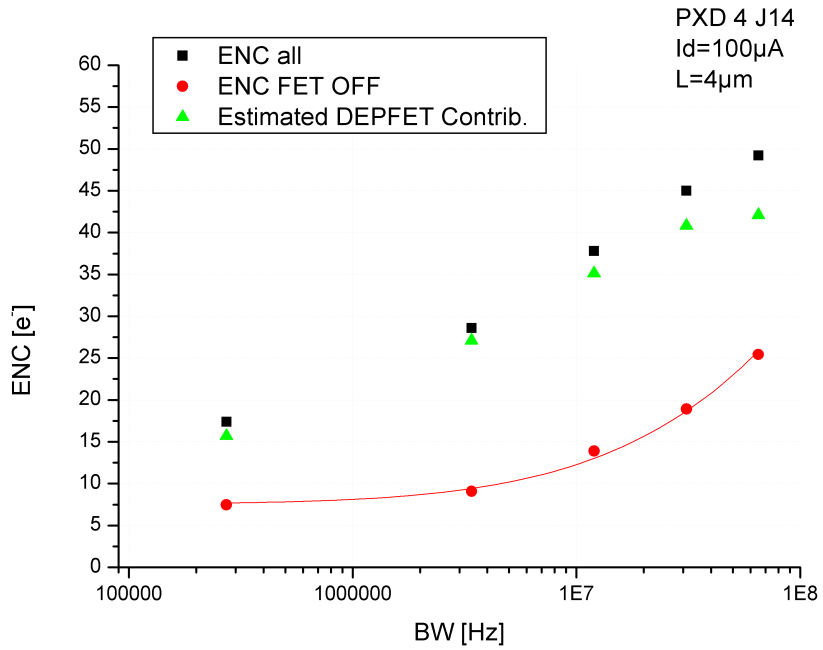


(a) Determination of the bandwidth

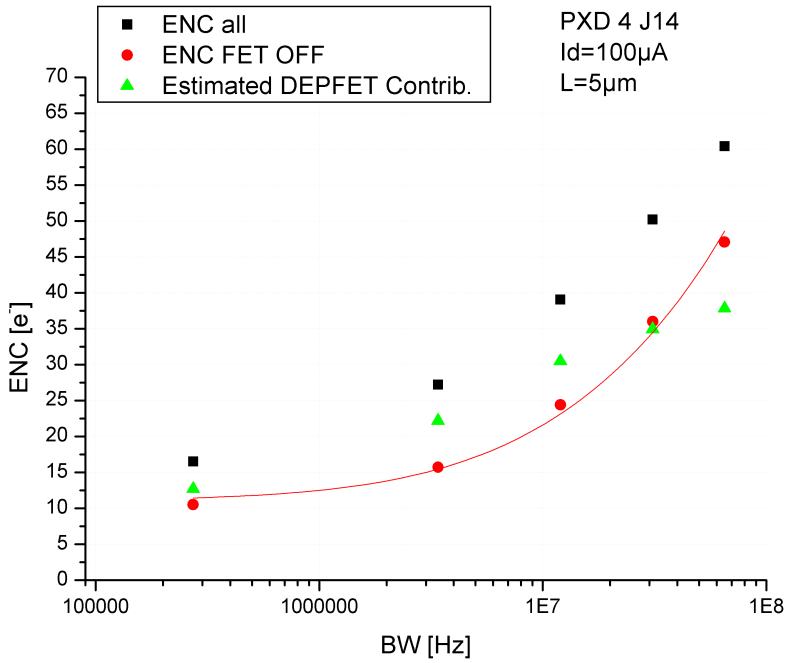


(b) Measured response

Figure 8.2: Characterization of the fast setup. Bandwidth determination by applying an external stimulus (sine) to the gate of the DUT and response for various low pass filter



(a) L = 4 μm



(b) L = 5 μm

Figure 8.3: Noise of PXD4 J14 at high bandwidth

Chapter 9

Internal Amplification

The chapter deals with internal amplification - the gain of the DEPFET. It introduces the importance of this parameter in the first section. The measurement method is presented in the following section. An extensive study of the gain is presented in the following chapter, showing that a gain 1.3nA/e$^-$ is already possible with the current technologies without changes. The dependence on the geometry and the biasing of the DEPFET is studied and compared with a theoretical model. Furthermore the limitations of the model presented in chapter 4.3 and appendix C are investigated.

9.1 Internal amplification and noise

The importance of the internal amplification could be demonstrated by examine a generic two stage amplifier like shown in 9.1. The input signal S_1 is amplified by the first stage with amplification A_1 and an equivalent input noise N_1. The second stage provides a gain of A_2 and an input noise of N_2.

The signal to noise ratio (SNR) after the first stage is S_1/N_1. The overall signal to noise is

$$\left(\frac{S}{N}\right)_{final} = \frac{S_1 A_1 A_2}{\sqrt{(N_1 A_1 A_2)^2 + (N_2 A_2)^2}} = \left(\frac{S}{N_1}\right) \frac{1}{\sqrt{1 + \left(\frac{N_2}{A_1 N_1}\right)^2}}. \tag{9.1}$$

Evidently the maximal achievable SNR is limited by the SNR of the first stage. On the other hand the limiting factor is currently the frontend.

By looking at the limit of a noisy second stage $N_1 << N_2$ the previous formula could be simplified to

$$\left(\frac{S}{N}\right) = \frac{S_1 A_1}{N_2}. \tag{9.2}$$

In this limit a doubling of the amplification of the first stage the overall SNR of the hole chain doubled. As long as the noise is dominated by the frontend, see section 7.3, the SNR of the detector could be improved by increasing the amplification of the first stage namely: the DEPFET.

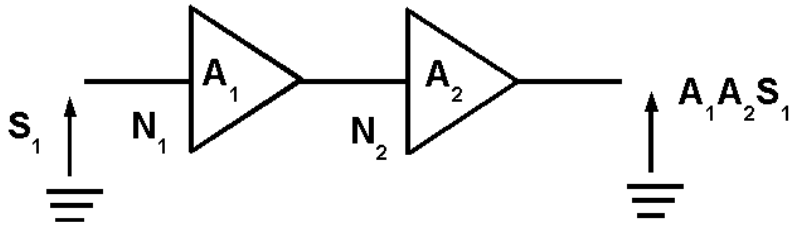


Figure 9.1: Noise in a two stage amplifier

9.2 Measurement of the internal amplification

The measurement of the internal amplification was performed with the single pixel setup which allows investigating dedicated single pixel structures as well as mini matrices.

The single pixel setup allows to distinguish g_q variations due to incomplete clear from variations caused by changes of control parameter. This makes these measurements attractive compared to measurements on large matrices where the readout sequence less flexible and the parameter space for the operation is limited.

Calibration of the amplifier The measurement of the internal amplification requires an absolute calibration of the amplifier, this is contrary to the noise measurements where the amplitude of known signal charge is compared to the width of the noise peak. To achieve this, a known current must be injected at the input of the transimpedance amplifier. Due to the layout of the amplifier a certain current could be produced by changing the subtraction voltage.

A typical plot with a calibration curve in shown in 9.2a. The achieved inverse sensitivity is S=1.49 nA/ADU.

Measurement The measurement is performed using a Fe55 source which provides a signal of $5.9\text{keV}/3.65\frac{\text{e}^-}{\text{keV}} = 1616\text{e}^-$. A typical spectrum is shown in 9.2b, since the pixel are small and no clustering is possible a lot of split events are visible. Nevertheless a clear peak, indicating events where full charge was collected in a pixel, is visible.

The evaluation of the position is performed using a appropriate fitting function. A simple fit with a Gaussian is slightly misleading since the peak sits on an asymmetric background. To get rid of this effect theoretically motivated fit function has been used - the primary events have a Gaussian distribution, the number of splits at a certain position x is proportional to the number of primary events above x. Thus the background is expected to proportional to the error function.

By evaluating the separation of the signal peak from the noise peak the g_q could be easily calculated via

Structure	W [μm]	L [μm]	comment.
PXD4 J14	20	4	non. HE
PXD4 J14	20	5	non. HE
PXD4 J14	20	6	non. HE
PXD4 J14	20	7	non. HE
PXD5 F10	9	4.4	ME
PXD5 F11	15	4.4	ME
PXD5 F12	25	4.4	ME
PXD5 F11	15	5.8	ME

Table 9.1: Evaluated pixel structures

$$g_q = \frac{Ph_{sig} - Ph_{noise}}{S}. \tag{9.3}$$

9.3 Internal amplification studies

Various test structures have been investigated table 9.1 shows an overview. The gain of the structures was investigated with respect to

- gate length L
- gate width W
- current dependence

For the further discussions formula 4.3 is well suited, since the comparisons between different devices is better performed at a similar current. By substituting the term in the brackets the following equation could be derived:

$$g_q = \sqrt{\mu_h \frac{1}{L^3 W C_{ox}^{'}} I_{ds}}. \tag{9.4}$$

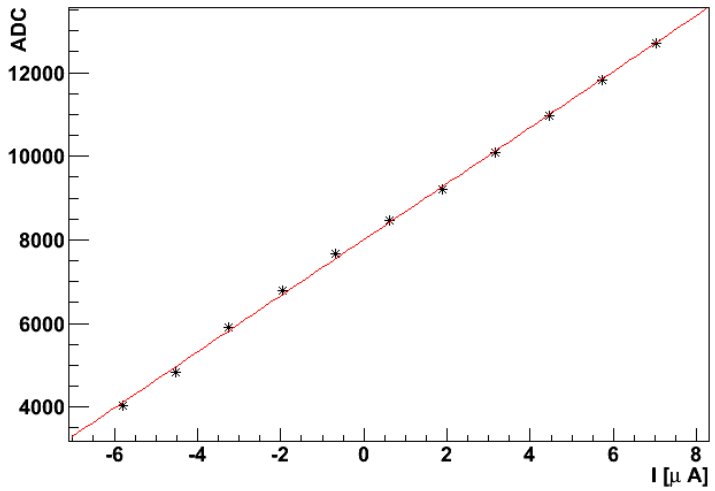
The equivalent formula for the g_m is

$$g_m = \sqrt{\mu_h C_{ox}^{'} \frac{W}{L} I_{ds}}. \tag{9.5}$$

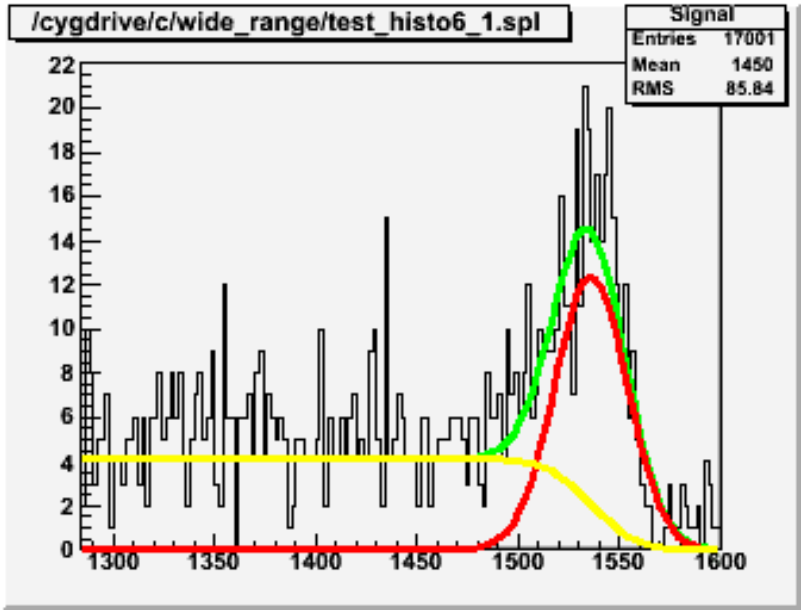
The quotient g_q/g_m for a given device at a fixed current is

$$\frac{g_q}{g_m} \mid_{I_{ds}} = \frac{1}{WLC_{ox}^{'}} = \frac{1}{C_{ox}}. \tag{9.6}$$

$C_{ox}^{'}$ is the sheet capacitance of the oxide and C_{ox} the absolute capacitance. The calculation shows that the transconductance is proportional to the internal amplification.



(a) Calibration curve



(b) Dedicated fit

Figure 9.2: Typical calibration curve showing the injected current versus the ADC code; Signal and background fit for a CDS measurement

9.3.1 Results

This subsection gives a summary of the measurements performed. The detailed discussion is done in the following subsections 9.3.3-9.3.4.

Figure 9.3a shows the internal amplification versus the drain current for J14 test structure, with variable gate length. As expected from equation 9.4 the gain increases with the current and with shorter gate length. Qualitatively the presented model is confirmed. However a closer look to the current dependence already reveals a difference to the expectation, this issue is discussed in the next subsection.

9.3.2 Current dependence

The gain in figure 9.3a is plotted semi logarithmically, thus the functional dependence on the drain source current is approximately of the form $A+B\log I_{ds}$. Evidently a contradiction to the expectation, see equation 9.4.

Mobility reduction

A necessary condition to achieve a high gain is a reasonable mobility of the charge carrier in the channel. Both g_m and g_q are sensible to variations in the mobility. The transconductance of the FET is depicted in figure 9.4. Equation 4.2 in chapter 4.3 predicts a linear dependence of the transconductance on gate source voltage beyond the threshold. The measured transconductance however is only linear for small gate source voltages and shows a slower increase at higher voltages.

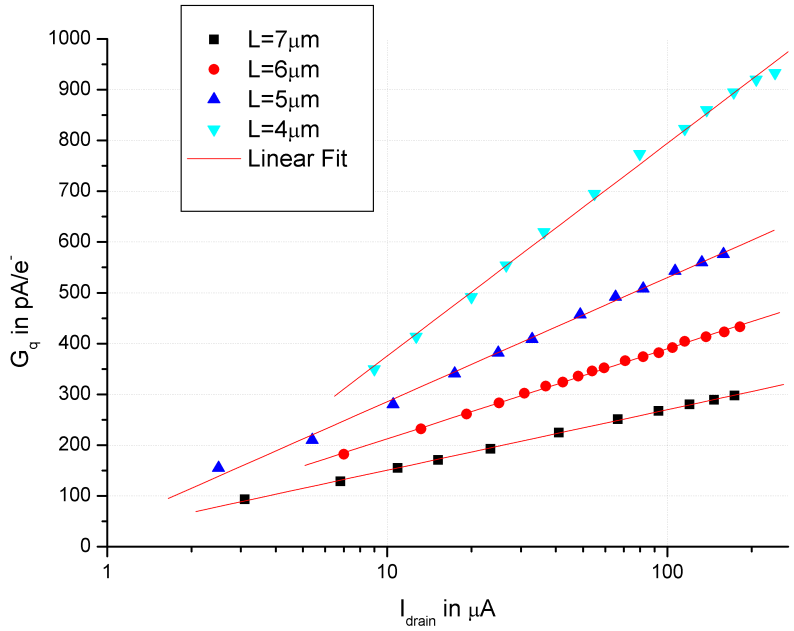
This deviation could be attributed to a mobility reduction in the normal field of the FET. The reduction is due to the fact that the holes in the channel are getting closer to the interface by an increase of the gate-source voltage. The interface states and surface roughness of the oxide leading to an increase in scattering and thus a decrease in mobility [38].

Efficiency of influence

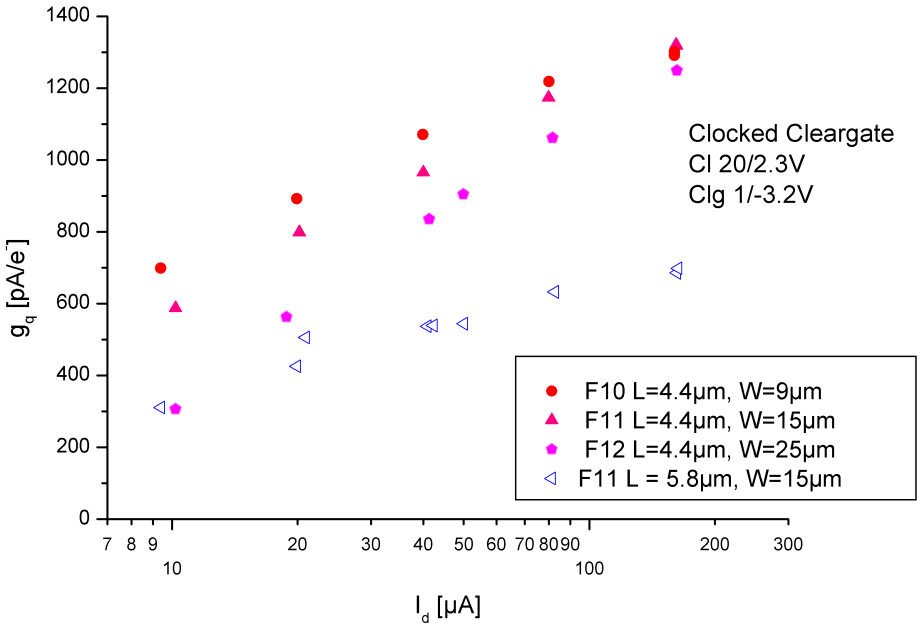
In principle the internal amplification and transconductance should be proportional to each other (equation 9.6). A numerical scaling to match them was performed in figure 9.5a showing that for small gate source voltages the proportionality is realized. But for higher voltages a deviation is visible, which shows that a second effect occurs.

The basic model assumes that each charge carrier in the internal gate influences a carrier in the channel. As pointed out a correction factor f must be applied. The internal gate is a potential minimum created by appropriate implantations and operation voltages a dependence on the latter can explain this deviation.

Increasing the gate voltage (actually the gate voltage becomes more negative) the repulsion moves the potential minimum closer to the source. This leads to a decreased efficiency for the charge influence.



(a) g_q PXD 4 J 14 vs. I_{ds}



(b) g_q PXD5 F10/F11/F12 vs. I_{ds}

Figure 9.3: Internal amplification of different DEPFET design variants [67]

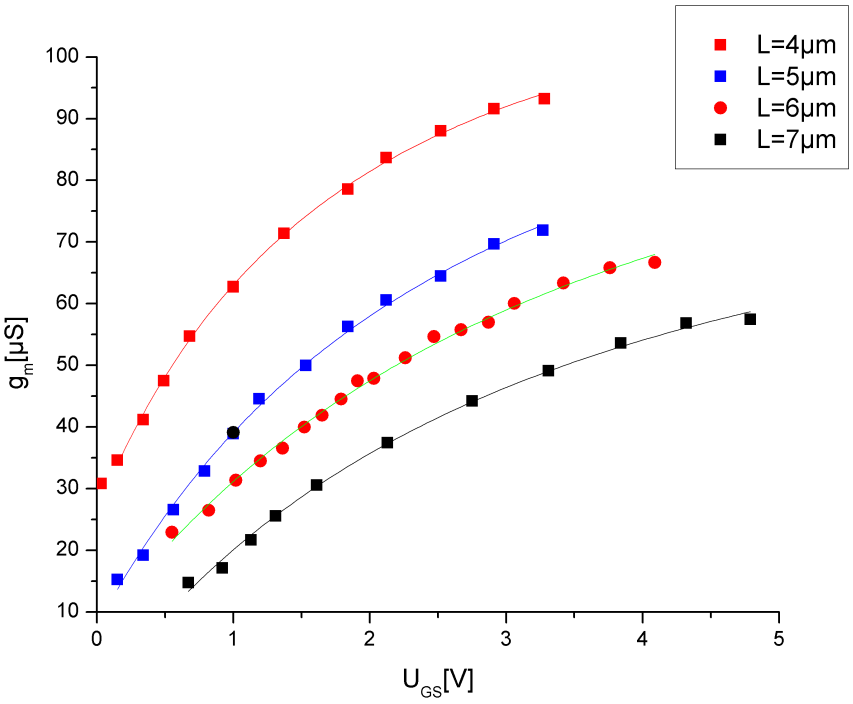


Figure 9.4: Transconductance of various DEPFET pixels

The effective coupling f/C_{ox} is calculated for the measured values is depicted in figure 9.5b. The oxide capacitance was calculated using a oxide thickness of 200nm and the geometry assuming an under etch of $0.5\mu m$. The inverse capacitance is depicted as solid line showing the model predicts the right order of magnitude.

9.3.3 Gate length dependence

A shorter gate length leads to a decrease in the channel resistance thus to an increase in g_m as well as g_q. The g_m scales only with $1/L$ while the g_q is affected twofold: the charge density in channel is increased and the channel becomes shorter.

The dependence was investigated using the PXD4 J14 structure mentioned in table 9.1. The results of this measurement were compared to a simulation. The measurements shown in figure 9.3a are compared the this simulation and are in good agreement, see figure 9.6. The diamonds mark the simulated values while the lower solid line are the measured values for 50μA and the upper solid line for 100μA

9.3.4 Gate width dependence

The gate width dependence was studied using the single pixel structures F10-F12 from the PXD5 production. Formula 9.4 predicts that the internal amplification is $\propto \sqrt{I_{ds}/W} = \sqrt{j_{lin}}$. Diagram 9.7 illustrates this behavior.

9.4 Discussion

Gain The presented measurements show that a significant increase in gain could be achieved by a further decrease of the gate length of the DEPFET. A gain of up to 1.3nA/e$^-$ was achieved, the highest reported up to now.

Taking into account that the currently used standard matrices, with a gate length of $6\mu m$ achieve a amplification of 450pA/e$^-$ in optimal configuration and around (300-380)pA/e$^-$ in common clear gate configuration. A further scaling could significantly improve the SNR of DEFPET detector systems.

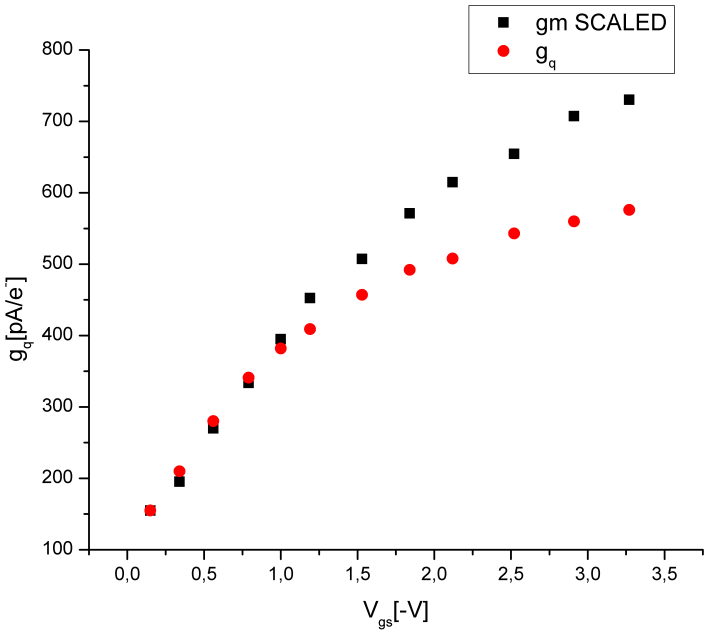
The investigated structures are produced with the standard DEPFET technology. However feature sizes in the below $\approx 4\mu$m suffer under an increased roughness of the edges due to the wet etching process currently used. It is expected that the dispersion on large matrices will be significantly higher when going towards smaller feature sizes.

An improvement of this issue could be achieved by using dry etching. Dry etching or plasma etching could significantly reduce the roughness. Thus large and homogeneous matrices could be produced.

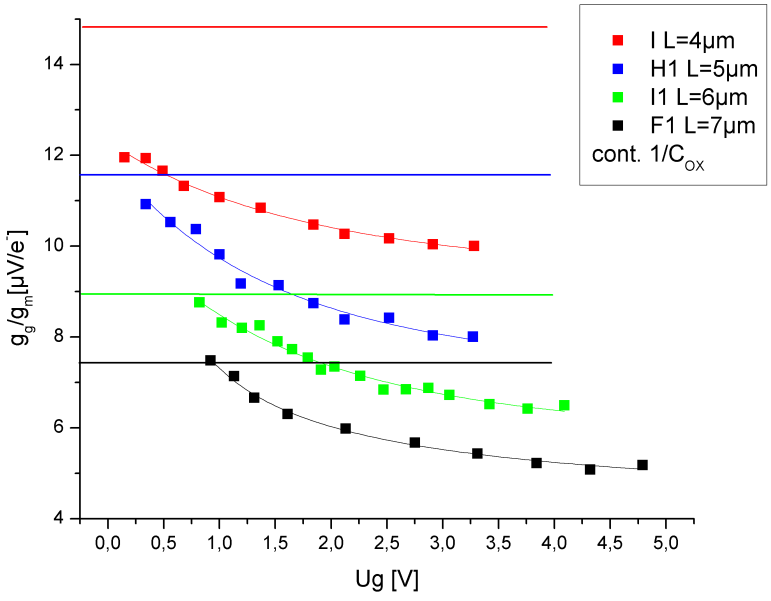
Current dependence As pointed out the slower increase of the g_q with drain current could be attributed to a mobility reduction in the lateral field and the reduction in the charge influence efficiency due to the repulsive potential of the gate.

The exact knowledge of current dependence is also important when the oxide thickness is reduced to improve the radiation hardness. The reduction in gain must be counterbalanced by increasing the current or the gate length.

Geometry dependence The dependence on the gate width is close to the expected predictions of the simulation.



(a) Comparison g_m and g_q



(b) Effective coupling

Figure 9.5: Influence of the gate source voltage on the effective coupling of signal charges on the transistor channel, the solid lines show the inverse oxide capacitance for the respective structures

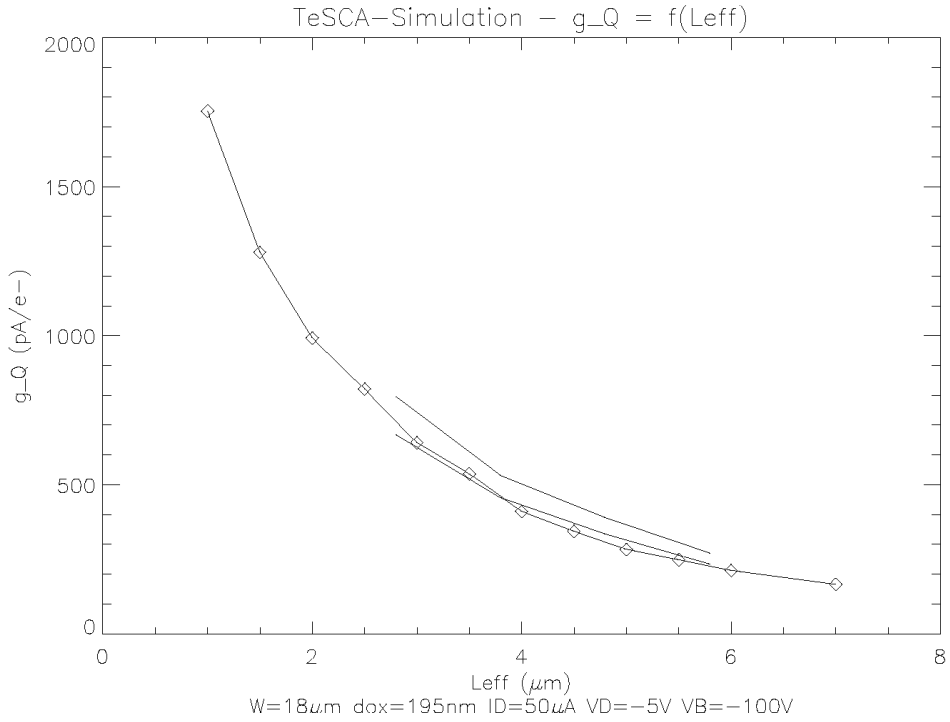


Figure 9.6: Comparison of simulated g_q and measured vs. gate length, simulated by Rainer Richter

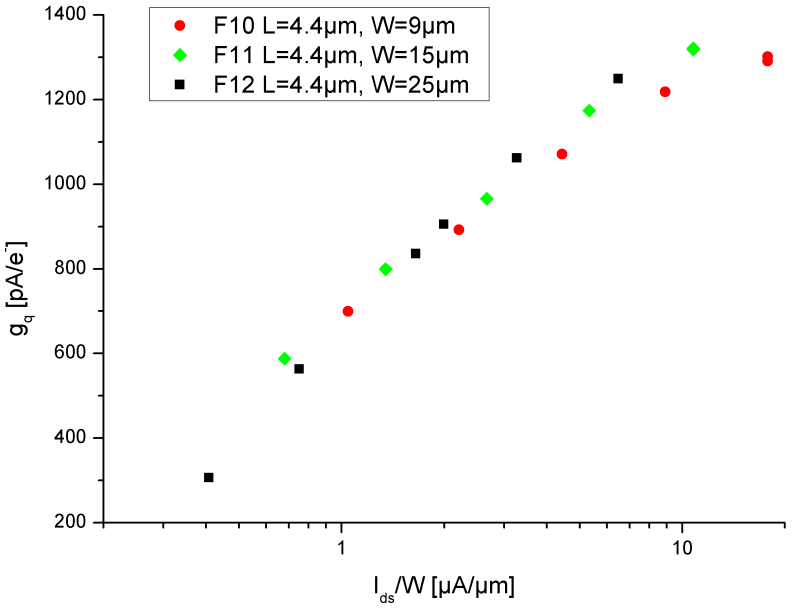


Figure 9.7: Internal amplification vs. current density

Chapter 10

Dynamic range

The dynamic range or charge handling capacity of the DEPFET is an important quantity when dealing with large signal charges. A charge beyond this limit would directly flow into the clear contact, since the clear contact offers the most positive potential for electrons.

In the conventional readout scheme as presented in 4.5 the probability that a single pixel is hit by two particles within a frame is very low.[1] Moreover the reduced thickness leads also to small signals. Thus in this case the charge handling capacity is not an issue.

However alternative readout approaches require that many hits must be accumulated in a pixel. Thus an finite capacity could give a rise to inefficiency. Moreover, study of this quantity in dependence of the operational parameter gives a direct measure for the potential depth and barrier height of the internal gate and the dependence on clear gate potential, clear low value and the implantation in the internal gate.

10.1 Measurement

10.1.1 Method

The direct way to measure the dynamic range is to investigate fill curves. The DEPFET is illuminated with a LED providing a constant current into the internal gate. The current could be measured similar to leakage, as described in chapter 8.1.

A fill curve including the measurement of the fill time is depicted in figure 10.1. The external gate is set close to the threshold. The capacity of the internal gate is given by

$$N_{e^-} = T_{fill}\frac{I}{e}. \tag{10.1}$$

[1] An occupancy of ≈1% is envisaged

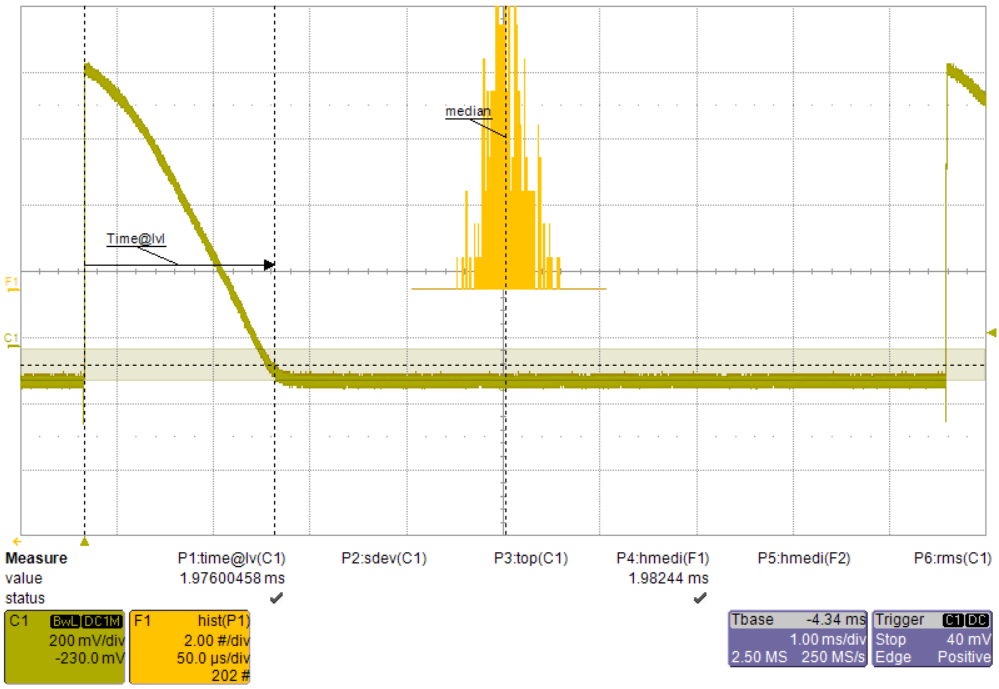


Figure 10.1: Dynamic range estimations via fill time measurement; To create a constant current the device under test is illuminated with a LED; Green: fill curve (200mV/div, 1ms/div); Yellow: histogram with measured fill times (50μs/div)

10.1.2 Results

Figure 10.2 shows the results of the measurement obtained with structure U12 (W/L 11/6). The capacity of the internal gate is determined by the barrier height towards the clear contact. Two parameters play an important role: the gate potential and the clear gate potential. The lower the gate potential the lower the potential in the internal gate is. The clear gate sets the potential difference to the clear contact.

The measurement reveals also an interesting feature: the increase at -2500mV, this could be attributed to an extension of the internal gate under the source.

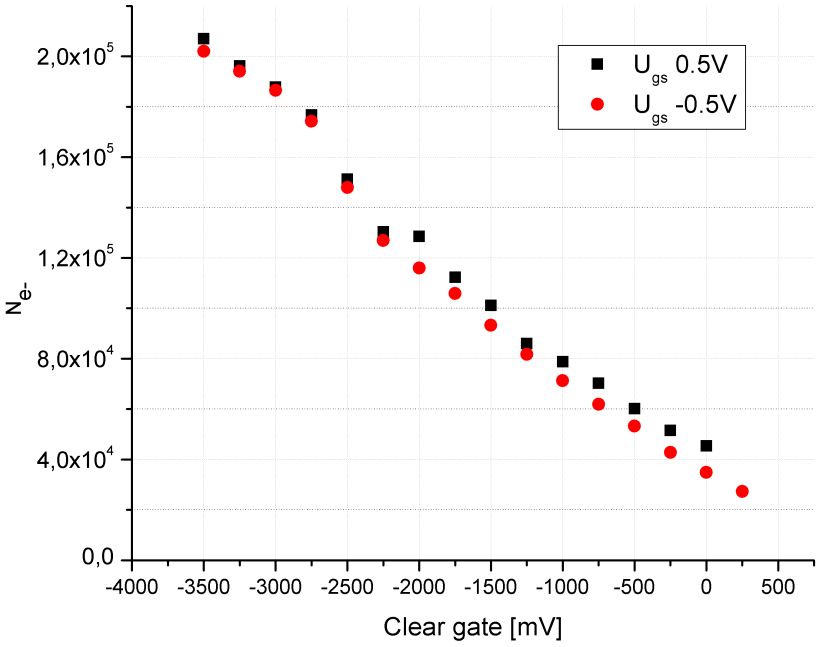


Figure 10.2: Capacity of the internal gate of U12

10.2 Interpretation

The measurement show that capacity of the internal gate for a clear gate voltage of -500mV, which is necessary to achieve a full clear with the Switcher 2, is beyond $5 \cdot 10^4 e^-$. The dynamic range is an important input parameter for the alternative readout concepts presented in chapter 18.

In addition the measurement demonstrates that the barrier height internal gate - clear is determined by the clear gate voltage. Thus also the clear performance is expected to show a strong dependence on the clear gate voltage.

Chapter 11

Clear behavior

This chapter deals with the clear performance of the DEPFET detector, the efficiency a charge is removed out of the internal gate, in the common clear gate configuration. The first section gives an overview over the impact of the clear performance on the system performance - reduction of signal and increase in noise. Section 11.1.2 gives an introduction in the measurement method used. The following sections are discussing the obtained results, with respect to the parameter space accessible with the switcher ASICs (see chapter 7.3) and the observed g_q modulation.

11.1 Clear performance

11.1.1 System performance

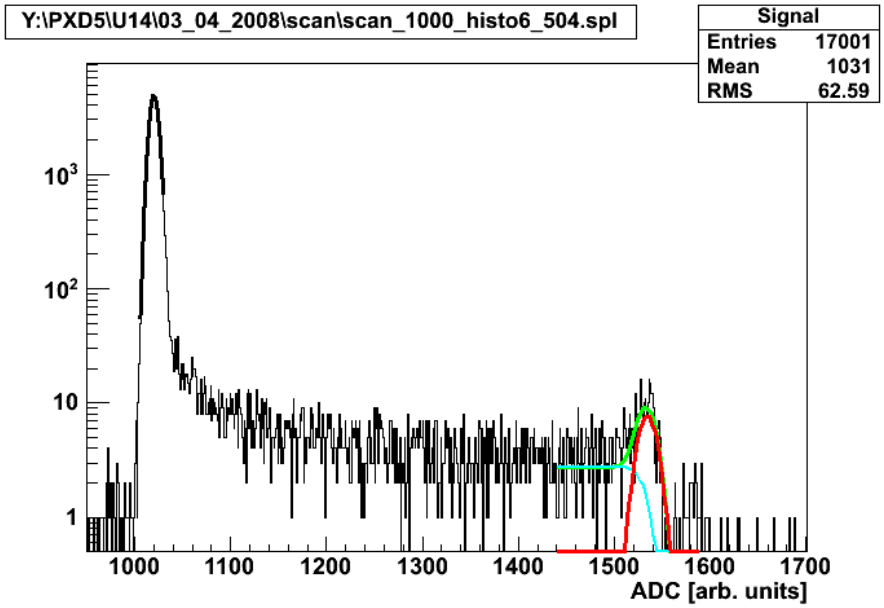
The clear performance is an important quantity for the overall performance of the detector, since both signal and noise are depending on it.

By using correlated double sampling the sample before the clear is subtracted from the sample after the clear. The difference is used as measure of the charge collected in the pixel. A remaining charge after the clear thus leads to a decrease of the signal by the same amount. The effect is demonstrated in figure 11.1.

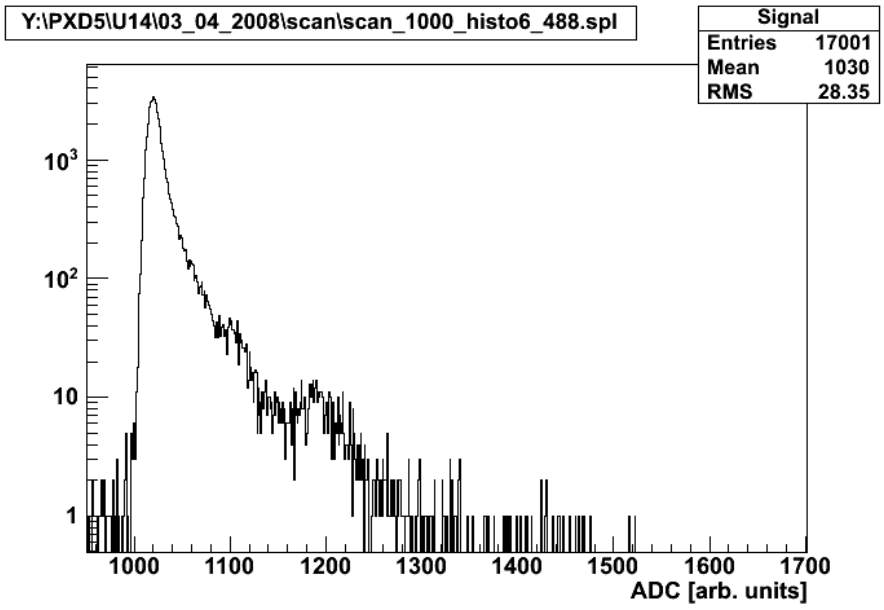
Moreover the remaining charge leads to a change of the baseline for the next integration time. An applied threshold, appropriate for a full clear, will lead to fake hits in presence of incomplete clear. This effect leads to an increase of the effective noise - the so called reset noise.

11.1.2 The comparison method

Several methods to judge the clear performance are available, up to now a common method is to link a minimum noise level to the state of a full clear [68]. However the measurement is very sensitive to the noise of the amplifier used, a small increase in noise is not detectable due to a large offset. Above all this method does not take into account the signal therefore neglecting an important quantity.



(a) Full clear, clear high 20V, clear gate -2.6V



(b) Incomplete clear, clear high 13.6V, clear gate -2.6V

Figure 11.1: Two Fe^{55} spectra demonstrating the impact of the incomplete clear. The incomplete clear is achieved by reducing the clear high from 20V to 13.6V. In case of the incomplete clear the signal pulse height is significantly reduced and non Gaussian tails on the noise peak are visible.

The measurements presented in this chapter use the following ansatz: via the comparison of the pulse heights of a correlated double sampling (CDS) with a clear in between and a correlated double sampling within the integration time, in the flowing called ICDS.

The principle is depicted in figure 11.2. The CDS pulse height is derived by a difference of the samples S3-S2 and the ICDS value via S1-S2.

Using both values one can derive an effective gain, in the following called ${g_q}^{CDS}$, which incorporates the lost signal due to an incomplete clear via

$$g_q \equiv g_q^{CDS} = \frac{S2 - S3}{N_e Gain_{amp}} \tag{11.1}$$

and

$$g_q^{ICDS} = \frac{S2 - S1}{N_e Gain_{amp}}. \tag{11.2}$$

The quantity which allows distinguishing a full clear from an incomplete clear is the "fraction" f:

$$f = \frac{g_q^{CDS}}{g_q^{ICDS}}. \tag{11.3}$$

A full clear is achieved when both g_q^{CDS} and g_q^{ICDS} have the same value. The quotient of the amplification derived with ICDS and CDS is a direct measure for the efficiency of the clear process. If the fraction is equal to 1 a full clear is achieved.

This method is also robust in presence of leakage current. Assuming a sequence without photons the measured signal is given by the leakage current - this is valid for the CDS and ICDS gain - these sequences form the noise peak. A sequence with photons exhibits the signal due to leakage current and charge from the photon. By calculating the difference the leakage current contribution is removed.

11.2 In CCG configuration

The common clear gate is the standard clear configuration in the PXD5 production and will be continued in the next production. The section shows results of clear performance measurements based on mini matrices.

One important issue is the clear high level necessary to achieve a full clear, since the switcher ASICS have a limited voltage range see chapter 7. Measurements attributed to this are presented in the next section.

11.2.1 Clear high level

Using the comparison method introduced in 11.1.2 the necessary clear high level to achieve a full clear was investigated in dependence of the clear gate level.

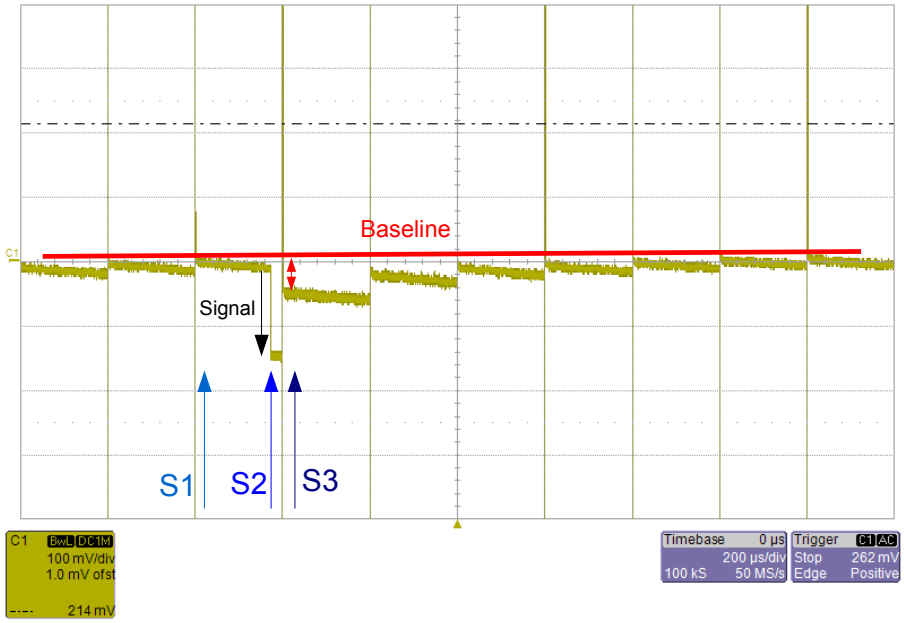


Figure 11.2: Sequence showing an incomplete clear and the proposed method for investigation via the comparison of correlated double samplings with and without clear; the baseline of the shown sequence is reached after several clear pulses

The device under test was the mini matrix U14 with a pixel size of 24μm - the nominal size for the vertex detector at ILC.

Figure 11.3 shows the results of both the noise and the fraction, for the definition see equation 11.3. The region of full clear is clearly visible - the upper red corner. This confirms the measurements in the previous chapter - the potential barrier could be set via the clear gate.

The equivalent noise charge is depicted in the figure below, which shows that a full clear not necessarily means lowest noise. For clear gate values of 0V an increase in noise is visible.

The reason for this behavior could be found in figure 11.4 where the internal amplification is displayed. Both the g_q^{CDS} and the g_q^{ICDS} show a decrease of the amplification for higher clear gate voltages.

This means that the increase of the noise in presence of a complete clear is related to the presence of a dominating noise source (the amplifier) and a decrease of the gain.

Interpretation The measurements show that a full clear could be achieved, with a proper setting of the clear gate potential, with levels below 10V. However the decrease of the gain needs further investigations, which are documented in the section 11.2.3.

11.2.2 Clear low level

The clear low level is important for two reasons:

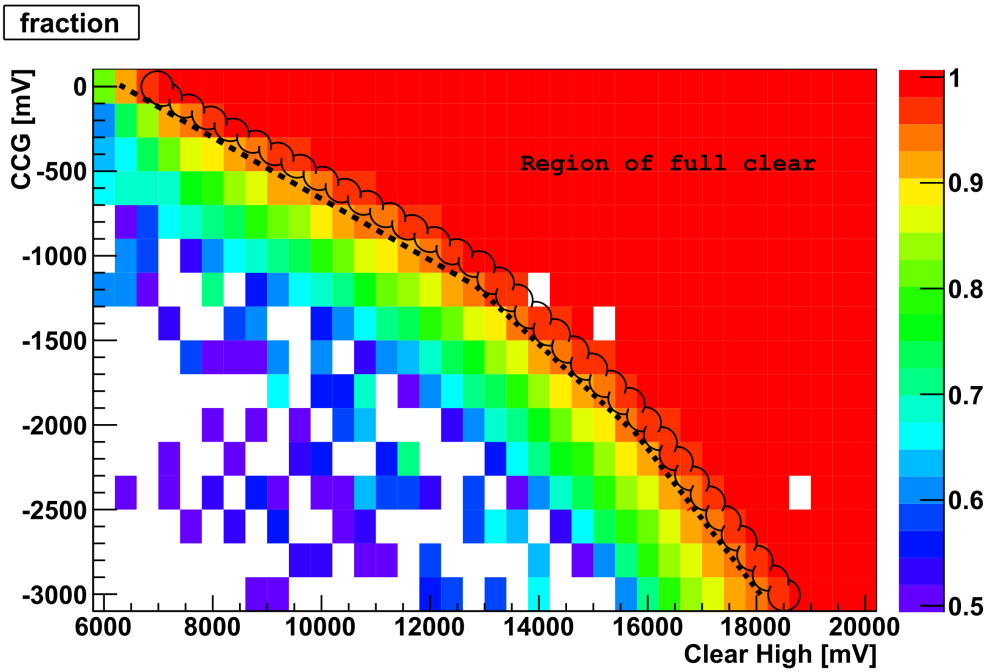
- to high values lead to charge losses and finally a continuous clear
- to low values lead to back injection - electrons are emitted from the clear contact and collected in the internal gate.

While the first leads to a slow loss of charge with increasing clear the second is very sensitive to the wrong settings since the internal gate is filled quickly. The back injection depends on the clear low value and the clear gate setting which determine the potential barrier for electrons to flow back. By simultaneously decreasing both parameters the potential barrier could be preserved.

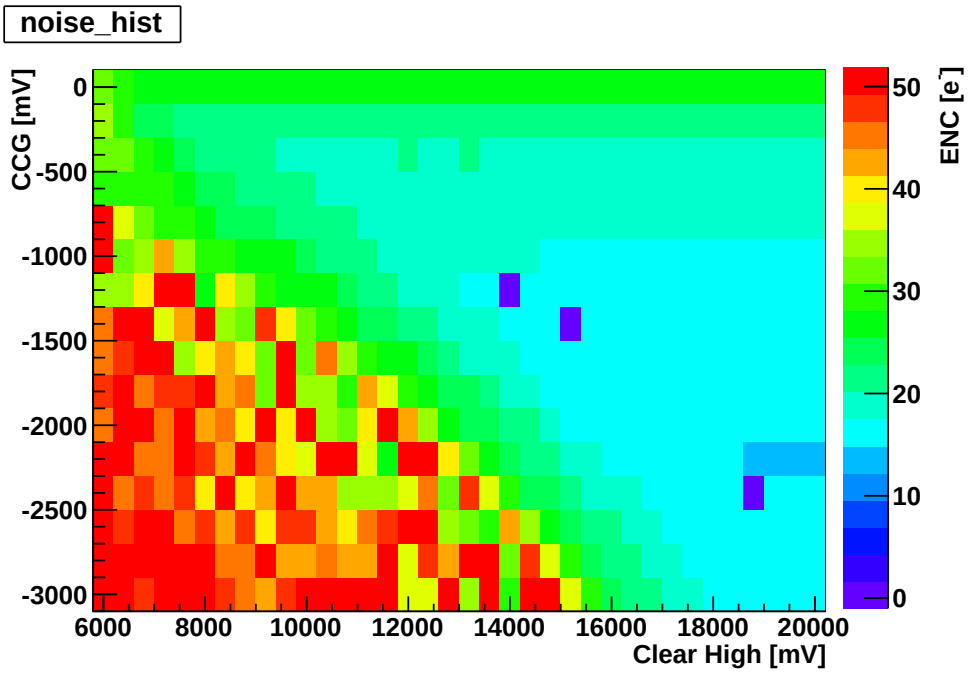
The clear low level also sets the maximum clear level when operating with the Switcher 3 since the voltage difference of both values is limited to 10V.

Measurement A systematic scan was performed to study the DEPFET response over a wide range in the clear gate - clear low parameter space. The clear high voltage was set to 18V - ensuring that a full clear is achieved over the full range. The results are shown in figure 11.5.

The most prominent feature of this scan is the strong increase of current in the upper left. This could be attributed to back injection - by decreasing the clear low voltage at a given clear gate potential, an increase in leakage current could be observed.

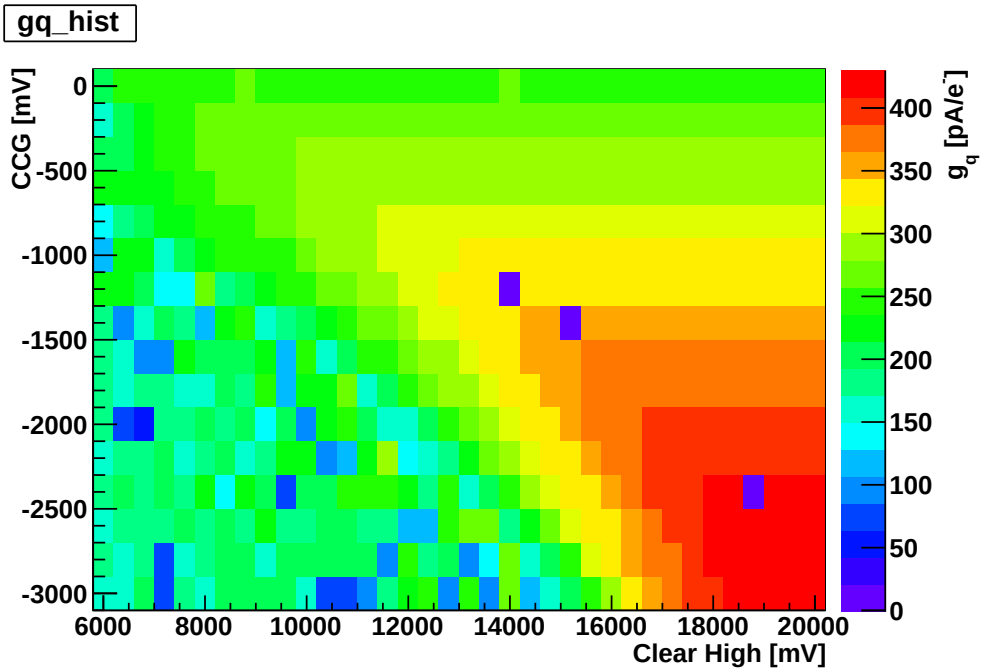


(a) Fraction of ICDS and CDS g_q

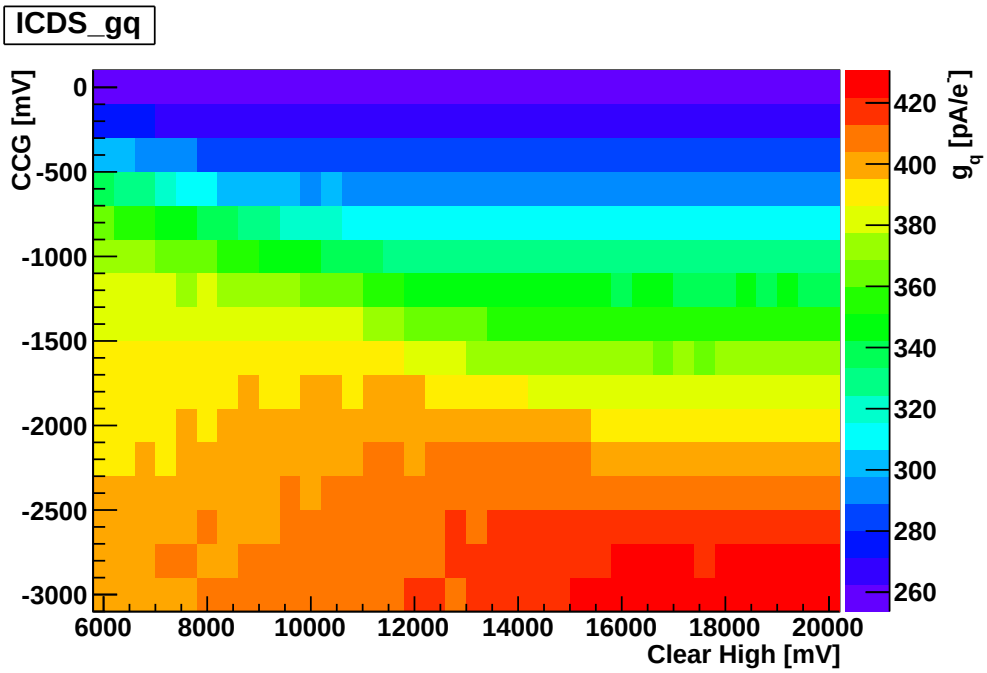


(b) Noise

Figure 11.3: Noise and clear performance of U14; the region of a full clear is by the curly line; the noise shows a strong increase in the region of an incomplete clear but also towards low clear gate values. The latter effect is related to the decrease of g_q, see 11.2.3



(a) g_q^{CDS}



(b) g_q^{ICDS}

Figure 11.4: Internal amplification of U14 derived from CDS and ICDS in dependence of clear high value and clear gate level

A voltage difference of at least 4V between clear low and clear gate is required to prevent back injection.

The lowering of the gain with the clear gate voltage is also visible in this measurement for the whole clear low range.

11.2.3 Gain modulation with clear gate

Both the measurements in section 11.2.1 and 11.2.2 showed a the modulation of the gain with the clear value - an unexpected phenomena.

Charge loss A first assumption is that the decrease is caused by charge loss into the clear contact - which would require a charge loss of 70% - the amount of the measured modulation. This extend must be visible in the spectra.

The peak in the spectra is related to photons which interact close to the internal gate. Thus the full charge is collected in a single pixel. This means that the modulation of the internal amplification is due to a loss of charge after collection. This would be visible since the setup allows to continuously monitoring the fill level of the internal gate. Moreover the statistical distribution of the interaction time with respect to the clear would lead to smearing of the signal peak.

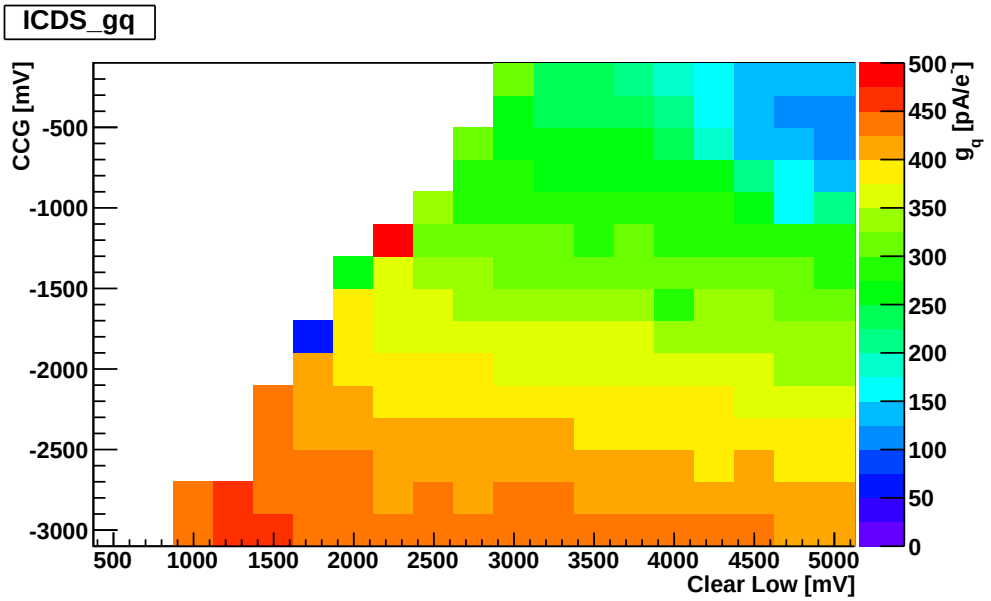
Figure shows 11.6 three spectra at representative points. The single peaks are well defined in each spectrum and show no indication for strong charge losses.

Current reduction A second possibility which could lead to a decrease of the gain is a parasitic steering of the clear gate. The transistor channel close to the clear gate could experience a decrease in current when fringe fields from clear gate reduce the electrical field in the channel, which lead to a decrease of the charge density. However expected variation of the field is small since the coupling towards the gate (200nm dielectric) is expected to be much stronger. Also the experimental observed variation depicted in figure 11.5b, for a given clear low value, is only on the percent level which could not explain this dramatic effect.

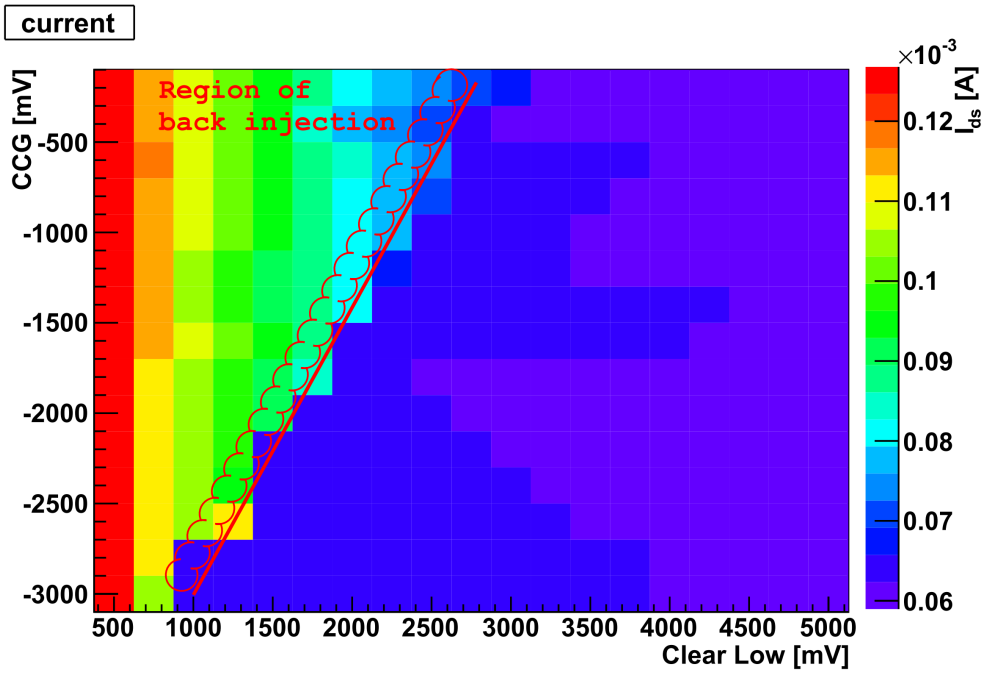
Device dependence A device dependence was investigated with a matrix of the type U25 - this matrix has a pixel size of $24 \cdot 36\mu\text{m}^2$ - having the same gate length but different width of 10.8μm.

Figure 11.7 shows a slice of the histogram from 11.5 for various clear low values and a similar slices for the second device under test U25.

The measurement shows that both devices exhibit the same behavior - a continuous decrease of the amplification with the clear gate voltage. However the absolute extend is around 70 % for the short channel width and 40 % for the long one. This is a strong indication that this behavior is related to the channel width W.

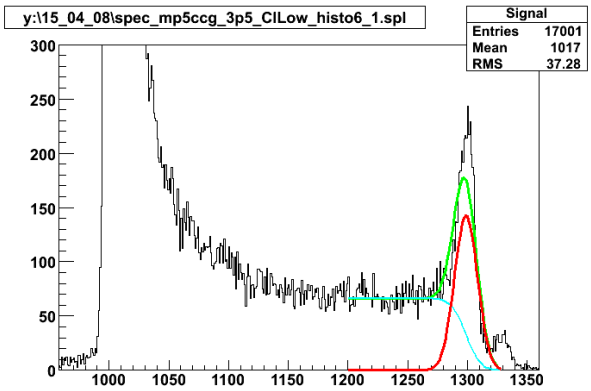


(a) $ICDS_{g_q}$

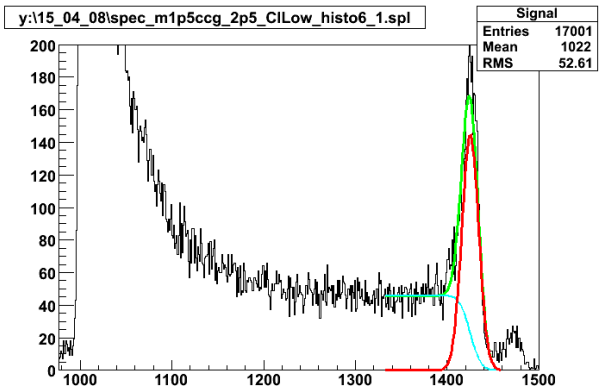


(b) Current in pixel

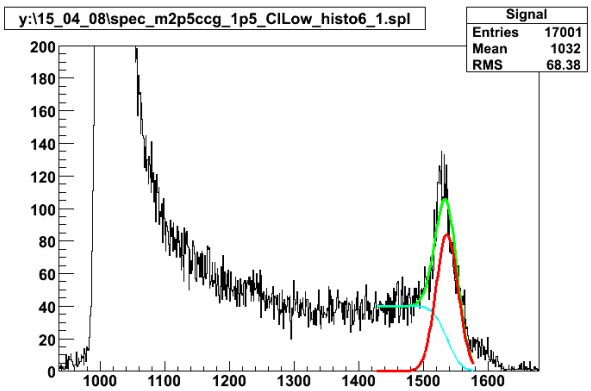
Figure 11.5: Amplification and current in U14 showing the region of back injection, the modulation of the g_q and a systematic decrease of gain with higher clear low values



(a) Spectrum at clear gate / clear low -0.5V / 3.5V



(b) Spectrum at clear gate / clear low -1.5V / 2.5V



(c) Spectrum at clear gate / clear low -2.5V / 1.5V

Figure 11.6: Spectra taken at different point in clear low - clear gate parameter space. The signal peak is well defined for each setting showing that the measured gain variation is not an effect of charge loss

Explanation The clear gate provides a repulsive potential on the edge of the internal gate defining the potential barrier towards the clear contact. By going towards more negative potentials fringe fields lead to squeeze of internal gate laterally, thus effectively reducing the width of the internal gate.

The improvement could be attributed to the change of influence efficiency: In the squeezed configuration the charge is centered in the middle of the internal gate thus the parasitic couplings towards the clear gate are reduced.

11.3 Summary

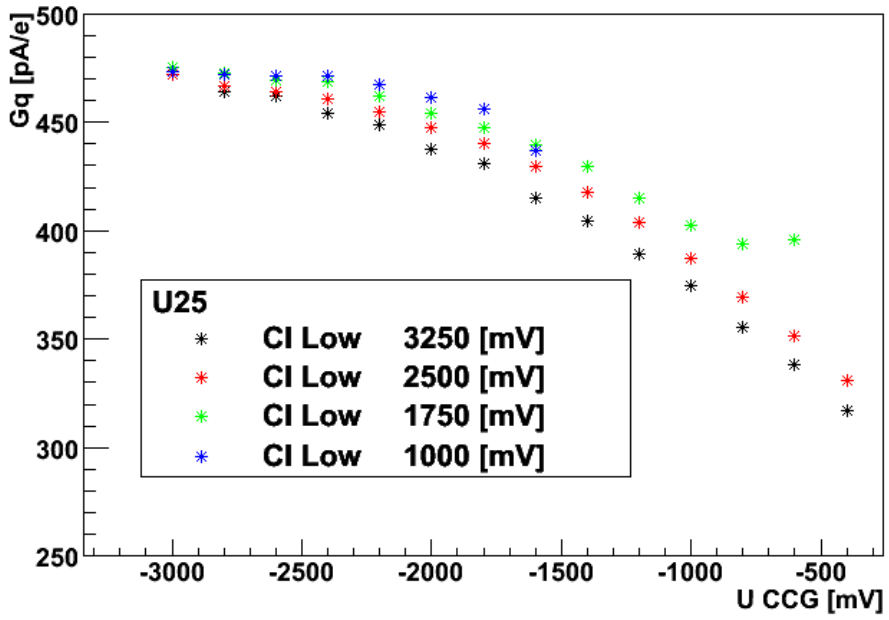
The chapter showed the importance of the clear performance for the SNR.

The comparison method is successfully applied investigate the clear performance of the new DEPFET generation from the PXD5 production.

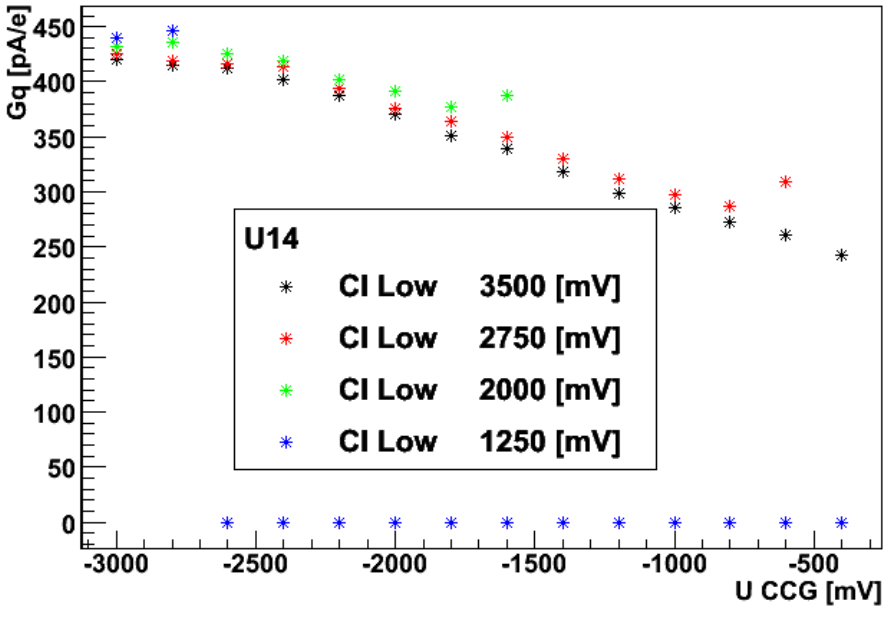
It is demonstrated that a full clear is possible with a clear high level of 10V which allows the use of the new radiation hard Switcher 3.

However the new method revealed also a new feature - a modulation of the gain with by the clear gate voltage.

This is the main reason why the standard matrices achieve an amplification of around $280 - 360\text{pA}/\text{e}^-$ [70], while single pixel measurements achieve more than $450\text{pA}/\text{e}^-$ with the same geometry of the FET.



(a) g_q modulation for U25 W=10.8μm



(b) g_q modulation for U14 W=7.4μm

Figure 11.7: g_q modulation for two similar devices with different gate width

Chapter 12

Capacitive coupled clear gate

The capacitive coupled clear gate (CCCG) is a novel approach to combine the simplicity of the common clear gate configuration with the superior clear performance of the clocked clear gate configuration [64, 3]. The coupling is achieved by a capacitor integrated in the pixel. A detailed description is given in section 12.1.

It is possible to measure the effective coupling directly utilizing a dedicated test structure. These measurements are presented in section 12.2. Moreover a comparison with the expected coupling extracted from the layout is given.

Section 12.3 demonstrates the superior performance of the CCCG on matrix level. Showing that the capacitive coupled clear gate is able to improve the signal level significantly compared to conventional matrices in common clear gate configuration. Also a first spectroscopic measurement of Fe^{55} on a CURO based system is presented.

12.1 CCCG

The capacitive coupling is achieved by an additional overlap between the clear contact and a poly silcon 2 ("poly 2") sheet forming a capacitor. The working point of the clear gate is fixed via a resistor on the edge of the sensor - the biasing resistor R_{cg}. The layout of a cell is shown in figure 12.2. The poly 2 sheet is marked in red. The time constant of the resistor capacitor network must be chosen in way that the RC time of the bias resistor and the capacitance of the row $\tau_{R_{cg}C_{row}} >> T_{row}$ to ensure that the clear gate pulse has a sufficient length.

An equivalent circuit of the CCCG configuration is shown in picture 12.1. The desired coupling $C_{CG-Clear}$ is shown, but also the parasitic coupling between gate and clear gate $C_{CG-Source}$ and the other contacts. The source is set to ground so this coupling is evident. Since the drain and gate are also referenced to ground via a low impedance connection these couplings must be also included.

This parasitic coupling is due to overlaps on implantation (n+ clear), poly and metal level. Since the gate is switched from positive to negative voltage, vice versa to the clear, the potential change on the clear gate is effectively reduced.

The layout of cell is depicted in figure 12.2. The red rectangle indicates the poly silicon plane for the coupling.

The voltage change on the clear gate is given by

$$\delta U_{cg} = \frac{C_{cg-gate}\delta U_{gs} + C_{cg-clear}\delta U_{clear}}{C_{cg-gate} + C_{cg-drain} + C_{cg-source} + C_{cg-clear}}. \tag{12.1}$$

This formula reflects the characteristics of a capacitive voltage divider. The time constant involved is

$$\tau = \left(C_{cg-gate} + C_{cg-drain} + C_{cg-source} + C_{cg-clear}\right) R_{cg} = C_{tot} R_{cg}. \tag{12.2}$$

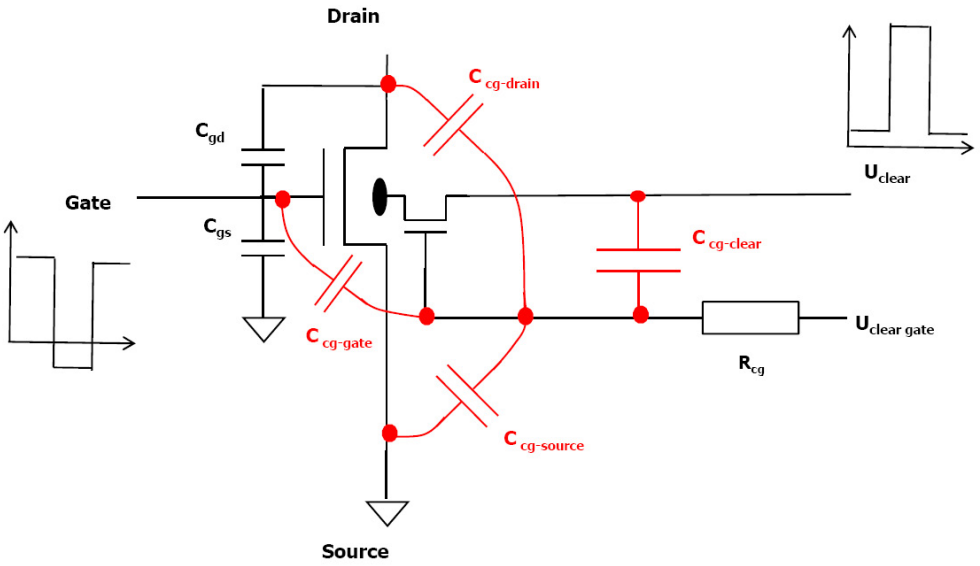


Figure 12.1: Overview of parasitic and intended couplings in CCCG configuration

12.2 Direct measurement of the coupling

A direct measurement of the absolute coupling was possible with help of a dedicated test structure. The direct measurement of the clear gate level with a probe would be difficult since a probe including appropriate pads would add a large additional capacitance which significantly alters the picture shown in figure 12.1.

The test structure uses an additional PMOS transistor, providing a high input impedance, directly connected to the clear gate. The layout is depicted in figure 12.3. An estimate of the introduced capacitance due to the overlaps of the metal line connecting the transistor and the capacitance itself lead to 45fF.

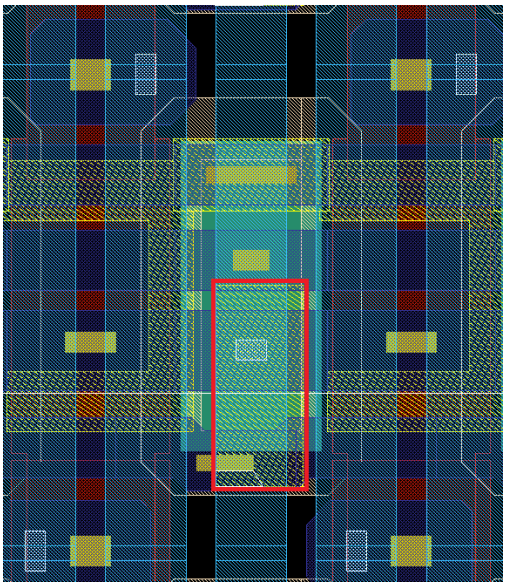


Figure 12.2: Layout CCCG pixel cell including layer Metal 1 /2, Poly 1/2 , source - drain- and clear implantation [3]

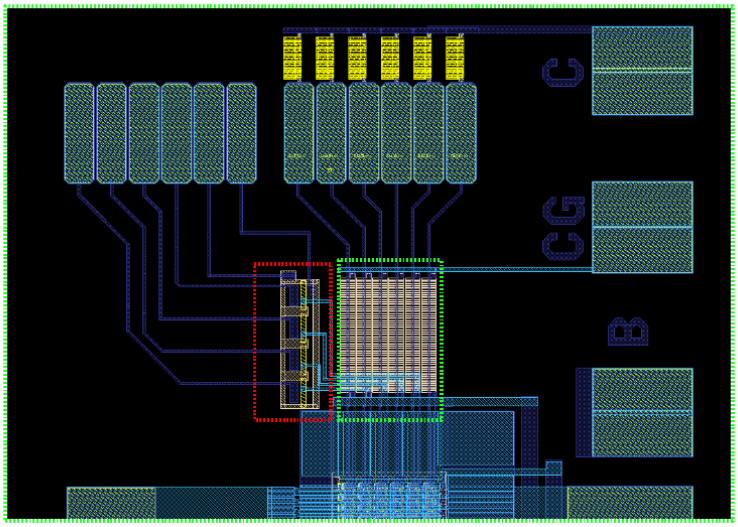
12.2.1 Setup

Readout board To investigate the structure a dedicated readout board was developed within this thesis. Special attention was drawn to clear and gate connectors to be able to use clear and gate pulses with a width of O(20ns). The detector was fully biased during operation - including drain source, backside and bulk voltage.

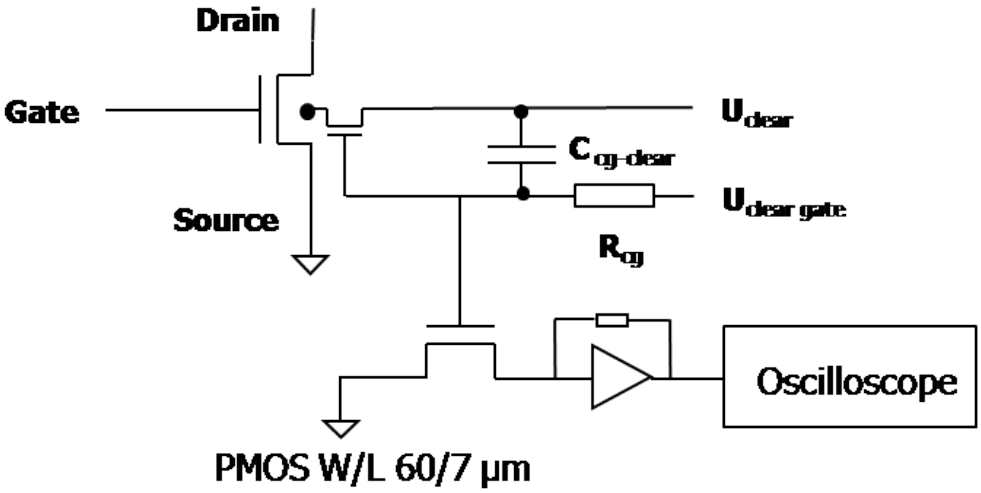
Crosstalk Since fast signals are investigated already small parasitic capacitance on board level could provide a low impedance path for high frequency components thus leading to crosstalk.

The crosstalk was investigated using the fully equipped readout board without the test structure. A 10V pulse with 3ns rise time was applied to the clear and gate input and the response of the amplifier was measured showing that the amplitude at the output is below 15mV, see figure 12.4. This is small compared to expected signals consequently playing no role for the interpretation of the results.

Calibration Since the readout is performed in drain readout, the source follower has voltage gain 1, the current voltage characteristic of the PMOS must be measured. By varying the clear gate voltage the drain through the PMOS could be directly measured. The calibration curve is depicted in figure 12.5. The source was held at ground for this measurement. The second step is the calibration of the transimpedance amplifier connected to the PMOS. The curve shown in figure 12.5b shows a linear relationship to the input current over 20μA



(a) CCCG test structure [3], in red the readout transistor and in green the bias resistors



(b) Schematic of the test structure showing the PMOS connected to the clear gate

Figure 12.3: Layout and schematic of the CCCG test structure

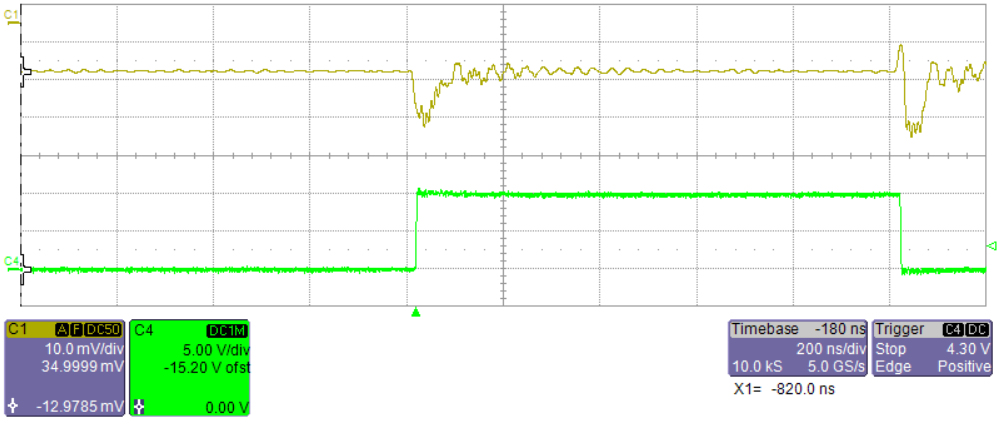


Figure 12.4: Crosstalk of a pulse applied to the clear connector. Yellow trace: signal taken with 10mV/div; green trace: pulse applied 5V/div; the horizontal axis: time 200ns/div

and an overall dynamic range of 100μA with some deviation from linearity.

12.2.2 Measurement

Coupling Figure 12.6 shows the amplitude of the voltage change at the clear gate plotted against the peak to peak value of the applied pulses at the gate and clear. The black curve represents the remaining effective coupling when the clear and gate pulses have the same amplitude but different sign, which is close to the conditions in a matrix.

The measured couplings are 207 mV/V for the clear and 160 mV/V for the gate. The measured remaining coupling was measured to 64mV/V which is 26 percent larger than expected for the separate measurements.

RC - time The RC time of the clear gate gives direct access to the total capacitance. The resistor, which was directly measured at a similar structure, has a value of 58kΩ. The measured decay time from 90% to 10% of the amplitude is 1.4μs. The time constant is given by $tau = t_{90/10}/2.19$ thus being 0.64μs. The total capacitance is C_{tot} 11.0pF.

12.2.3 Comparison with Layout

The involved capacities could be independently estimated from the layout. In principle software tools are available to extract the capacities automatically from the layout. However these tools assume that planarization steps are applied which are not used in the DEFPET technology.

A rough estimate could be derived from the following assumption. The dielectrics between the poly silicon layers and the bulk have a thickness of 200nm and between the metal layers 500nm. The capacitances are dominated by overlapping not by coupling over the bulk which acts as dielectric in full depletion. The important sources for the capacitance are overlaps of

- implantations - metal
- implantations - poly silicon
- poly silicon - poly silicon
- poly silicon - metal
- metal - metal.

For the analysis following assumptions were made:

- d_{Si0_2} Metal - Metal 500nm
- d_{Si0_2} Poly silicon - Poly silicon 200nm
- under etch of 500nm

Table 12.1 gives a summary of the extracted capacities.

Network	Capacitance per cell $[fF]$	Capacitance per matrix $[pF]$
CG-Gate	26.1	1.67
CG -Clear	31.4	2.01
CG -Source	27.04	1.73
CG - Drain	42.3	2.71
Sum:		8.12

Table 12.1: Couplings between the various networks in the CCCG structure

Calculation of the couplings With the extracted capacities it is possible to calculate the couplings directly. The ratio of the coupling to the clear $\delta_{cg-clear}$ and to the gate $\delta_{cg-gate}$ are given by

$$\frac{\delta_{cg-cl}}{\delta_{cg-gate}} = \frac{C_{cg-cl}}{C_{cg-gate}}. \tag{12.3}$$

This is a direct consequence of equation 12.1.

Using the values from table 12.1 a ratio of 1.20 can be calculated. The measured couplings give 1.29, a deviation of 7%, which is in good agreement. A source of inaccuracy is the fact that the extraction procedure used assumes that the conducting structures have zero thickness. In reality the poly silicon is .5μm thick and the metal layers 1μm.

The absolute coupling could be calculated to 247mV/V and 200mV/V, both are 20% larger than measured. This could be attributed to the fact that the overall capacitance is underestimated which is also suggested by the independent measurement via the RC time.

12.2.4 Impact on matrix operation

The first part of the section showed that the capacitive coupled clear gate is working and the measured coupling could be understood to a precision of $\leq 20\%$, taking into account the intended and parasitic capacities on matrix level.

The coupling of the clear and the gate to the clear gate is of similar size. Thus the effective coupling is limited to ≈ 400mV. Since the amplitude of both the clear and the gate is around 10V.

This is an important input for the optimization. The gate off voltage is currently set 5V above the threshold. Thus a lowering of the gate off voltage would allow increasing the voltage swing on the clear gate without affecting the off state of the transistors.

The setup allows also to simulate the time dependence of a readout sequence, shown in figure 12.7. The observed response has an interesting consequence: As pointed out in the previous chapter a modulation of the g_q with the clear gate voltage is observed. Thus the capacitive coupled clear gate offers a twofold improvement - improved clear performance and improved gain due to the lowering of the clear gate voltage during readout.

12.3 Matrix measurement

This section presents a performance test of a capacitive coupled clear gate matrix with 64x128 pixels. The matrix is divided into two parts - one with the coupling and another where the bias resistors are removed. Since the clear gate has a low impedance connection to the power supply, the involved time constant is small thus the coupling is effectively turned off. This allows a direct comparison of both types.

The matrix is mounted on a CURO based systems with the Switcher 2, see section ASIC development 7.3. A detailed description of the system is given for example in [44].

The evaluation of the matrix measurements requires several steps to obtain a pulse height distribution. The used analysis is based on C code from Jaap Velthuis, the program was adapted to windows, an improved clustering was added and the common mode correction was implemented in a more robust way, since the original algorithm lead to instabilities for split events [70]. An overview of the analysis steps is given in appendix D.

12.3.1 Matrix optimization

Since the performance of a CURO based system is very sensitive to variations in the gain of the DEPFET a systematic optimizations is required. In a first step the gate on and off voltages are set, the clear high is chosen as high as possible. The remaining parameters - clear gate voltage and clear low voltage must be systematically scanned since they are crucial for the SNR. The fixed parameters are summarized in table 12.2.

The results of the optimization procedure are depicted in figure 12.8 and 12.9. The main parameters are the noise and the pulse height achieved with a given charge. A cadmium source was used to generate a signal of 22keV ($6028e^-$).

Results Evidently the noise of both parts of the matrix is similar around 13.5 ADU in the optimal region - clear gate 6.7V and clear low 9.8V. Thus it is sufficient to compare the pulse heights for each point. This is as expected since the ADC value is proportional to the output current noise of the system, which is dominated by the fronted.

The strong increase of the noise in the lower right corner could be attributed to back injection. In the lower left corner the incomplete clear process leads to an increase of the noise.

However the pulse heights are quite different at the optimum: $\approx$ 270ADU for the uncoupled part and $\approx$ 360ADU for the coupled one. An interesting fact is that the position of the optimum for the clear gate parameter differs only by 0.2V. Which is unexpected since the capacitive coupling is expected to allow an operation at lower clear gate voltages.

Taking into account the investigation performed in section 12.2 this can be understood: The applied voltage steps on the gate and clear are of similar height - 11.2V on the clear and 11V on the gate. Thus the remaining voltage step on the clear gate is only $\approx$ 0.5V. The significant improvement of the pulse height is achieved due to the lowering of the clear gate voltage prior to the clear. The clear gate potential is decreased by 160mV/V*11V = 1.76V. The increase could be attributed to improvement of the gain due to the effective lower clear gate potential, compare to chapter 11.2.3 - gain modulation due to clear gate.

Port	Level [V]
Source	7
Gate (On/Off)	(2/13)
Clear high	21
Bulk	15
Backside	200

Table 12.2: Operation parameter for matrix operation used for the optimization. Please note that the source voltage is at 7V - to compare the parameters to the single pixel setup the voltages must be related to source level.

12.3.2 Performance of the CCCG matrix

The following measurements demonstrate the performance of the CCCG matrix. The measurements were taken at the optimal setting.

Figure 12.10 show the spectrum of a Cd122 source for the upper and lower half of the matrix. Evidently the coupled half shows a significant improved performance.

Using the gain of the CURO based system of 7.9 nA/ADU [43] an internal amplification of 470pA/e$^-$ could be calculated.

Since the noise is dominated by the CURO the ENC using the CCCG matrix is lowered from $\approx$ 340e$^-$to 225e$^-$ with respect to the standard matrices.

12.3.3 Iron 55 spectrum

The low noise also allows the detection of Fe^{55} for the first time with a CURO based system. The spectrum is shown in figure 12.11. The seed threshold was intentionally set to 3σ to see the onset of noise hits. Nevertheless a shoulder is clearly visible.

To check if these hits are really associated with x-ray photons and not by non Gaussian fluctuations a second measurement with 1000 frames (3000 in the previous measurement) and no source has been performed utilizing the same analysis - seed and neighbor cut. An overall number of 770 hits has been detected. By scaling it to 3000 frames an excess of 6200 hits is found in the source measurement showing that the measured spectrum indeed originates from iron 55 photons.

12.4 CCCG Summary

The chapter demonstrates a new clear concept which improves the clear performance via a capacitive coupling.

The first part showed the direct measurement of the coupling using a dedicated readout board and a test structure. A intended coupling of 208mV/V between the clear - clear gate is achieved. However also a parasitic coupling of 160mV/V towards the gate is observed.

A comparison with layout data demonstrated that the measured values are within the expectations and also the parasitic coupling could be understood.

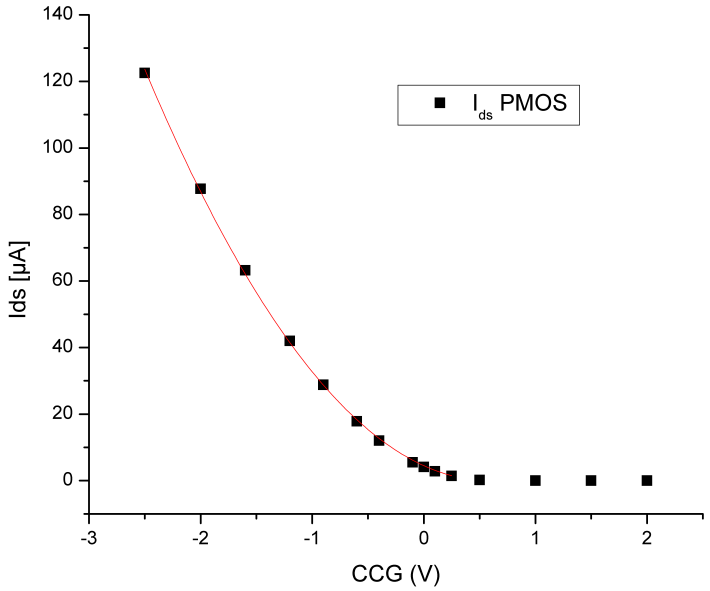
The second part demonstrated the performance of the CCCG design in actual source measurements. After optimization an internal amplification of 470pA/e$^-$ was measured. Which is close to the required value of 500pA/e$^-$ to achieve an ENC of 100e$^-$ with an external noise of 50nA - as expected for the DCD.

The significant improvement could be attributed to two effects: the improved clear due to the effective increase in clear gate voltage while applying the clear pulse and to the effective decrease of the clear gate while applying the gate select pulse, due to the parasitic coupling. The latter is due to the gain modulation, see section 11.2.3.

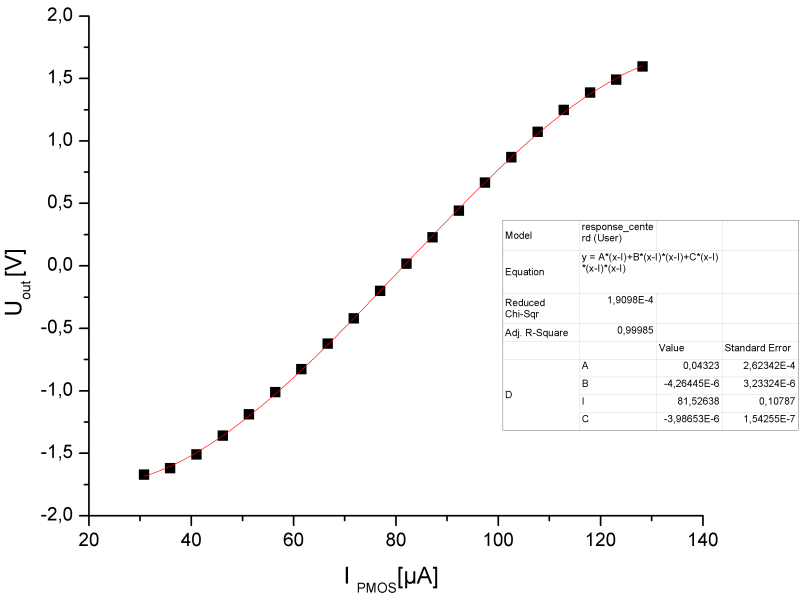
The ENC is lowered due to the increased gain to $225e^-$ allowing the detection of Fe^{55} x-ray photons with a CURO based system for the first time.

In addition the CCCG matrix was successfully used as device under test in the test beam 2008 showing the best SNR out of 6 planes [42].

In the next production the gained insight can be used for further optimization.



(a) Calibration curve of the PMOS transistor



(b) Calibration curve for the transimpedance amplifier connected to the PMOS

Figure 12.5: Calibration of the readout board for the CCCG test structure

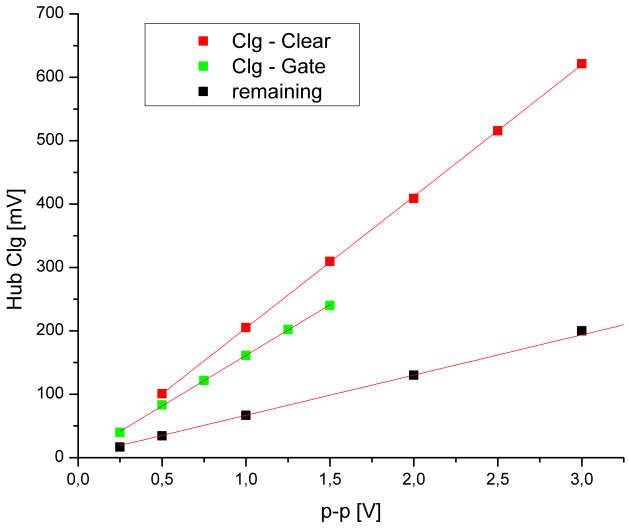


Figure 12.6: Measured coupling between clear, gate and clear gate

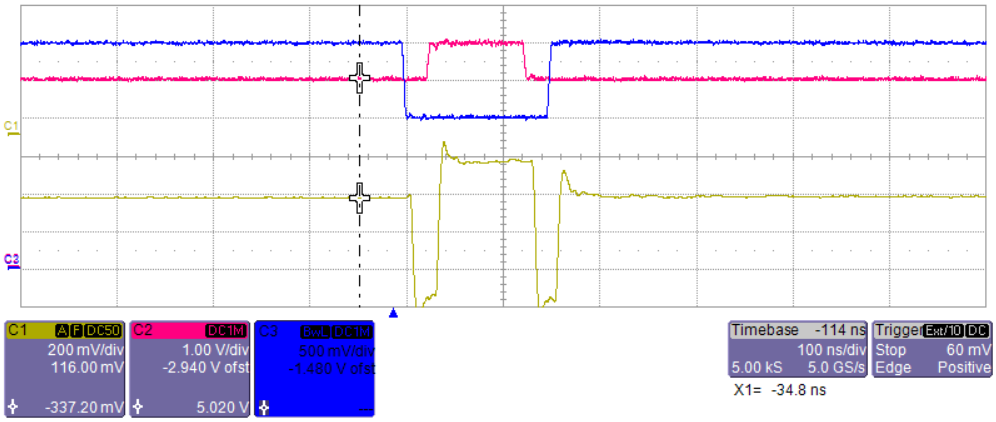
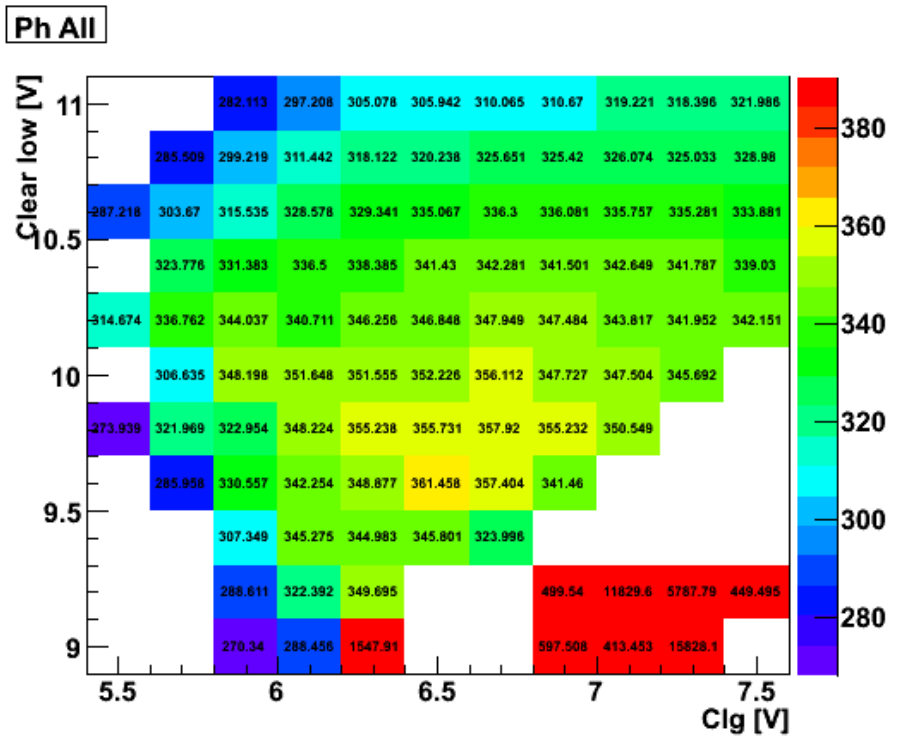
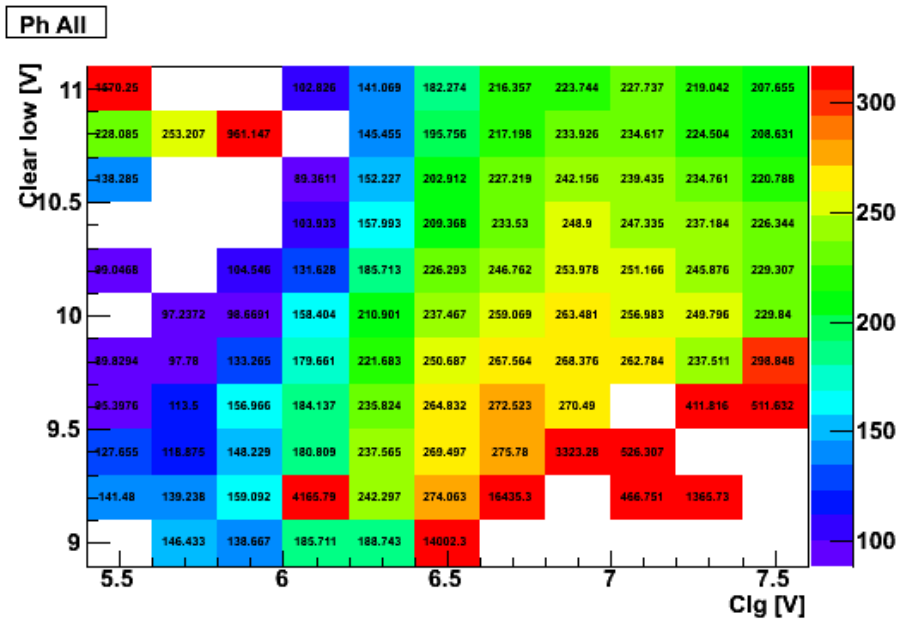


Figure 12.7: Variation of the clear gate voltage (yellow) for a typical readout sequence starting with the gate on pulse ($1V_{pp}$,blue) and a short clear pulse $1V_{pp}$, in red.

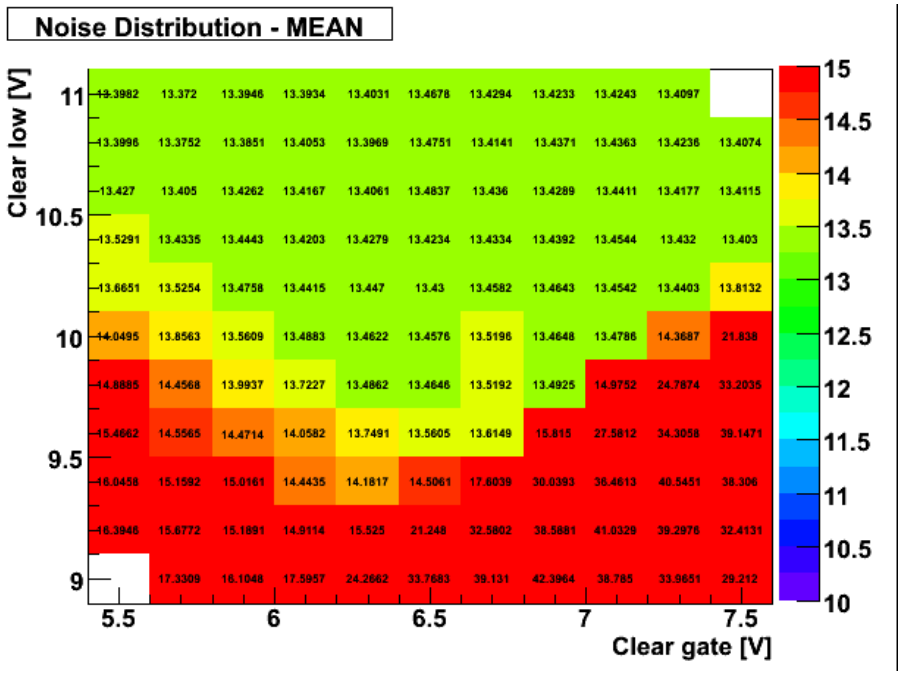


(a) Cluster pulse height in the coupled part

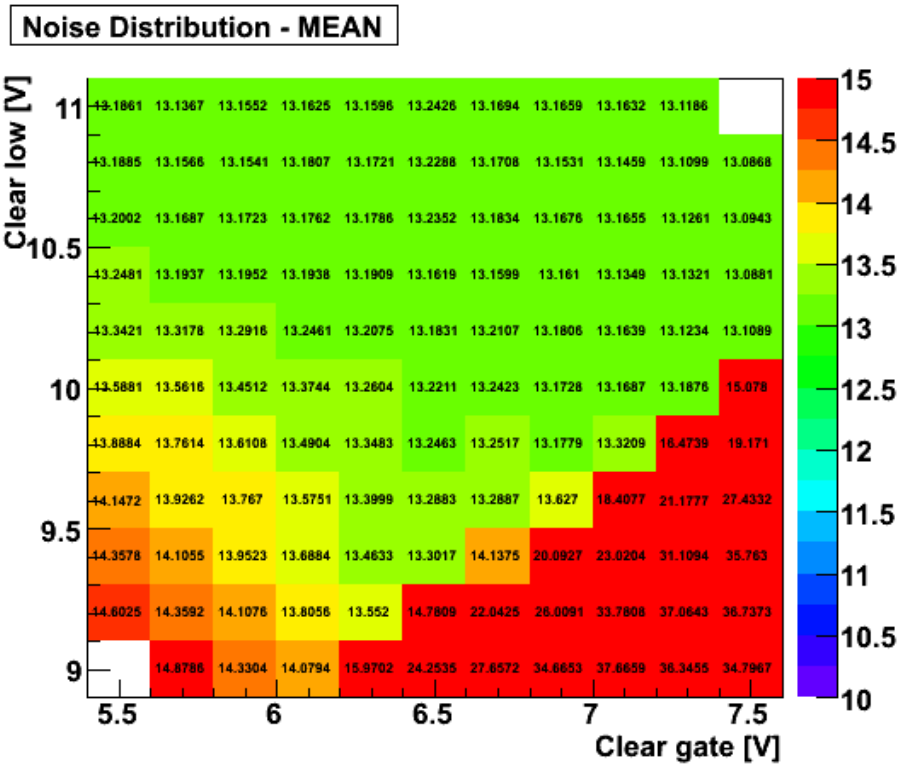


(b) Cluster pulse height in the uncoupled part

Figure 12.8: Cluster pulse height of both the capacitive coupled part and uncoupled part of the matrix, showing that the coupling lead to a significantly improved performance



(a) Average noise in the coupled part



(b) Average noise in the uncoupled part

Figure 12.9: Average noise of both the capacitive coupled part and uncoupled part of the matrix, showing that both parts have approximately the same noise

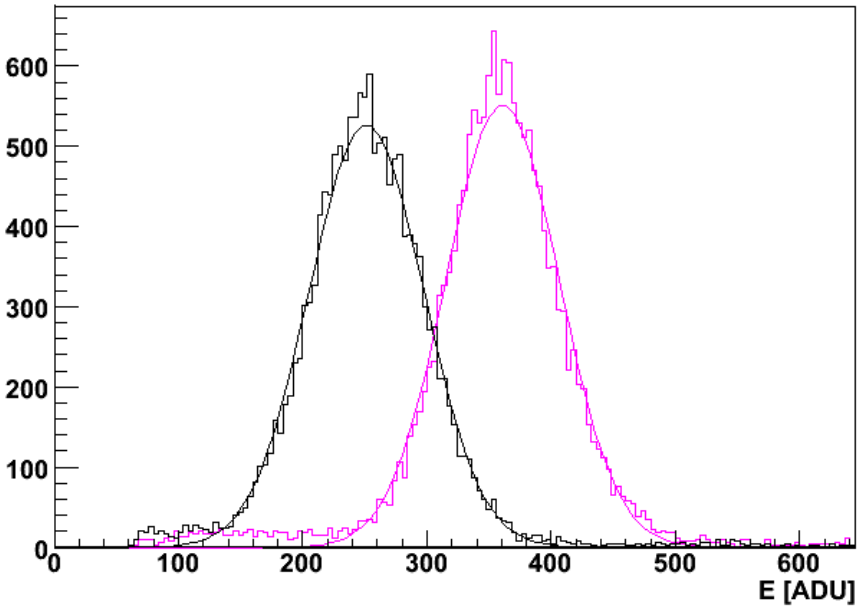
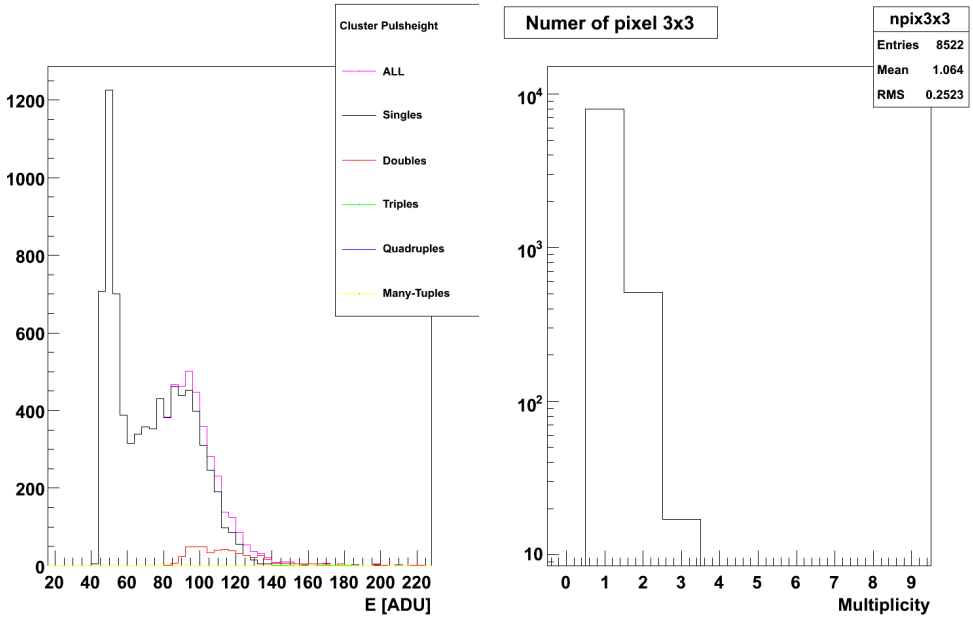
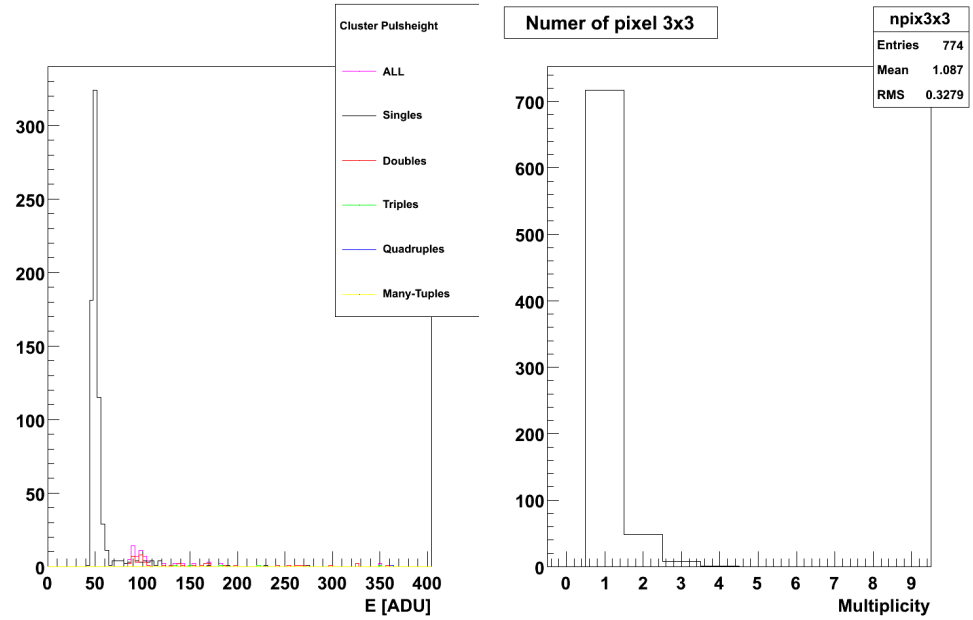


Figure 12.10: Cd^{122} spectrum of the coupled and uncoupled half showing the superior performance of the CCCG matrix



(a) Iron 55 spectrum from 3000 frames



(b) Reference measurement from 1000 dark frames

Figure 12.11: Iron 55 detection; cluster pulse height distribution and multiplicity of the clusters

Part II

Radiation Hardness of DEPFET active pixel sensors

Chapter 13

Radiation effects on Semiconductor Detectors

Virtually every particle detector will be exposed to radiation during its usage. It is of great importance to know the impact of the radiation on the performance of the detector.

Two forms of radiation damage can be distinguished: the non ionizing damage which introduces defects in the volume of the semiconductor (bulk damage) and the ionizing damage which is responsible for the threshold voltage shift in MOS devices and the creation of trap levels which lead to an increase in low frequency noise (interface damage).

This chapter gives an overview over these effects. Further information can be found in [74, 48, 53, 51, 46].

13.1 Non ionizing radiation damage

Microscopic picture The microscopic reason for bulk damage is lattice damage - silicon atoms are displaced by impinging radiation. The displacement damage has an energy threshold of 25eV [46]. The energy necessary to overcome this threshold is about 175eV for neutrons and 260keV for electrons - thus interaction with x-rays does not produce any bulk damage.

Figure 13.1 shows the non ionizing radiation damage for various particles versus the energy normalized to 1MeV neutrons. The displayed quantity is the displacement damage cross section D which is proportional to the non ionizing energy loss (NIEL).

The various damage types - vacancies, di-vacancies (V-V), interstitials can be characterized by their location within the band gap. Depending on the location the defects acts as generation - recombination centers, traps or acceptors.

NIEL hypothesis Over many years it was believed that all damage effects are proportional to the displacement damage. However it was found that the NIEL hypothesis is only valid for the bulk generated leakage.

However not for the change of effective dopant concentration where a strong dependence on the type and energy of the impinging radiation is found [46].

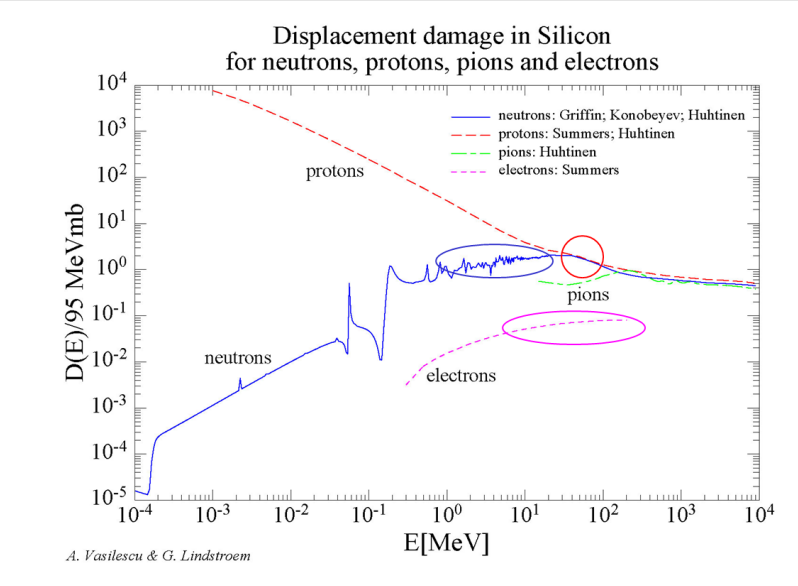


Figure 13.1: Displacement damage for electrons, neutrons and protons normalized to 1MeV neutrons

Furthermore the base material has a significant impact on the change of effective dopant concentration. Oxygenated silicon was found to suppress build up of positive space charge effectively.

The effects are the generation of leakage, change of effective doping and decrease of trapping time are described in the next sections.

13.1.1 Leakage current

The direct excitation of carriers from the valence into the conduction band is unlikely in silicon since such excitations require additional momentum transfer due to the indirect band gap of silicon.

Mid gap stats created by radiation damage are very effective for current generation since the probability is exponentially depending on the barrier height.

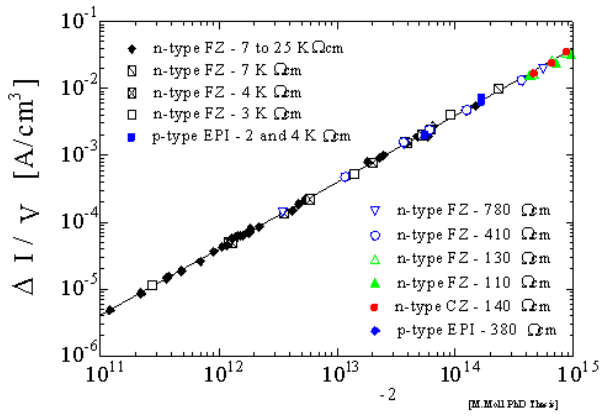
Figure 13.2a show leakage current for various silicon base materials plotted against the radiation dose. The leakage generation is similar for most of the materials showing that the effects are characteristic for silicon. Moreover the leakage increases linear with the fluency.

The bulk generated leakage current of a reverse biased diode after irradiation could be parameterized as

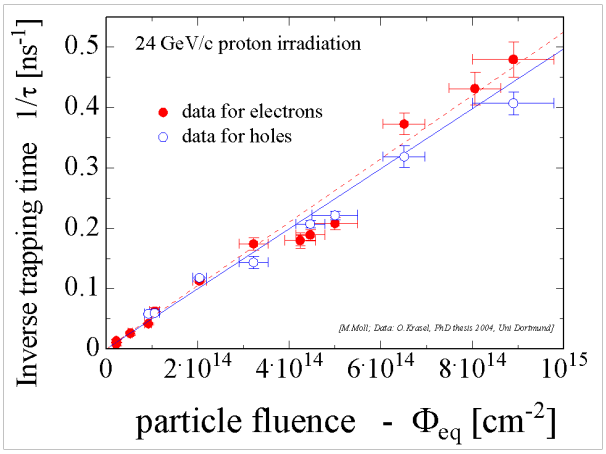
$$I_{leak} = I_0 + \alpha \Phi A d \text{ [74]}, \tag{13.1}$$

where A is the area and d the thickness of the device and I_0 the initial current. Φ is flux of the radiation and α the current related damage constant.

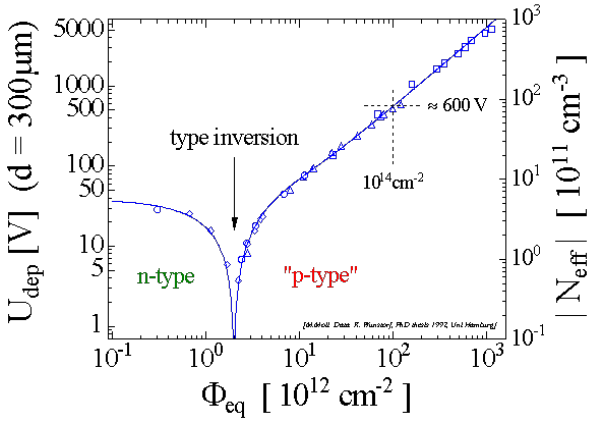
By using the relative hardness of figure 13.1 and the damage coefficient for



(a) Leakage current vs. fluency



(b) Inverse trapping time



(c) Effective dopant concentration

Figure 13.2: Effects of bulk damage: 13.2a showing the increase of leakage current, 13.2b demonstrates the increase of charge collection inefficiency and figure 13.2c shows the change of effective dopant concentration. Figures taken from [53]

1MeV neutrons of $\approx 4 \cdot 10^{-17}$A/cm the leakage arising from irradiation could be simply estimated.

Even if the expected fluency at ILC is quite low compared to LHC or sLHC ($10^{14} - 10^{16}$ $1\text{MeVn}_{\text{equ}}/\text{cm}^2$) one has to take into account that the integration time is around 50μs at ILC compared to ≈20ns at the strip detectors used at LHC thus the sensitivity to leakage is much higher at ILC.

13.1.2 Change of effective doping

The change of effective doping is also related to deep level defects. These levels act as acceptor consequently leading to an increase of positive space charge. At high fluency n-type silicon behaves as p-type after irradiation - space charge sign inversion.

Figure 13.2c depicts the effective dopant concentration versus the fluency showing that the inversion occurs well above 10^{12} $1\text{MeVn}_{\text{equ}}/\text{cm}^2$, [5].

Furthermore the change of effective doing depends on the used base material. Oxygenated silicon was found to be less susceptible to this effect.

At ILC the inner layer of the vertex detector will be exposed by one order of magnitude less, see chapter 3.3.5. Space charge sign inversion will play no role.

13.1.3 Decrease of trapping time

Shallow states - defect states close to the conducting or valence band - act as traps. Carriers are captured and released after a characteristic time.

The amount of charge lost while collection is approximately $\exp(-t_{col}/\tau_{trap})$. The inverse trapping time is depicted in figure 13.2b. At the typical fluency at ILC the expected effect should be negligible.

13.2 Ionizing radiation damage

The DEPFET as MOS device is also susceptible to ionizing radiation damage. The MOS interface reacts in two ways:

- threshold voltage shift
- increase of interface states.

Both effects are described in the following two sections.

13.2.1 Threshold voltage shift

Basic principle Ionizing particles hitting the MOS structure excite electron - hole pairs similar to silicon. The pair creation in SiO_2 is 18eV [16]. However the mobility of electrons and holes is very different in SiO_2 - $20\text{cm}^2/\text{Vs}$ and $10^{-9}\text{cm}^2/\text{Vs}$ [37]. The electrons are easily swept away by a electrical field while the holes have are likely to be trapped in zones with high defect density - the Si-SiO_2 interface.

This means that ionizing radiation leads to a positive charge up of the MOS interface. For the actual operation of the DEPFET this implies that the steering voltages must be adopted to compensate the positive charge. The shift in operation voltage is called threshold voltage shift.

Bias dependence Above all the threshold voltage shift was found to depend on the voltage applied to the MOS structure. Figure 13.3b shows the behavior under various bias conditions.

The lowest shift is obtained for zero field conditions; in this case the carriers are not separated thus recombination is very likely. The idea is depicted in figure 13.3c.

Under positive bias the observed threshold voltage shift is maximal. The holes are moving towards the interface where the trapping probability is maximal.

Negative fields show a moderate increase compared to the zero field configuration. The carriers are separated and the holes are moving towards the gate. Nevertheless holes are also created in the interface region where trapping is likely.

Oxide thickness Also the oxide thickness plays an important role. Figure 13.3a shows the voltage shift at positive field for various oxide thicknesses. Oxides with a thickness above 20nm show a shift scaling like $\propto d_{ox}^2$. However below 20nm, the trend described before, is broken and the shifts decrease much faster.

The reason for this behavior is the compensation of the positive charge via tunneling of electrons through the oxide. Modern CMOS processes which utilize oxides with thickness with a few nm are regarded as intrinsically radiation hard, due to this reason.

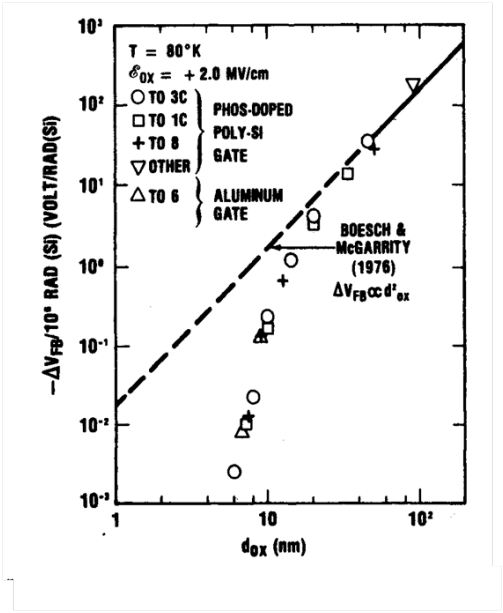
However the quadratic scaling is only valid for positive fields. In the other cases a linear behavior is observed [87]. This has important impact when thresholds voltage shift on DEPFET level is considered. A linear decrease of the threshold voltage shift is compensated by the increases in the transconductance g_m.

13.2.2 Interface states

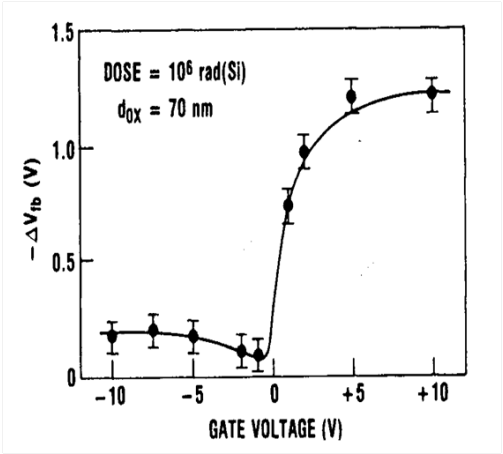
Besides the creation of fixed oxide charges, described in the previous section, a second effect occurs - the increase of the interface state density.

The impact of interface states is threefold:

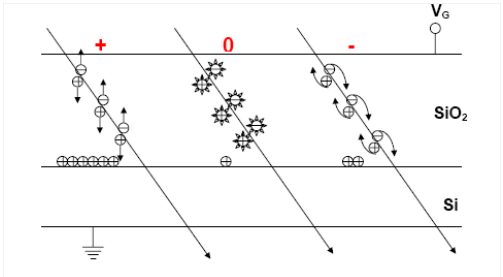
- additional threshold voltage shift
- increase of subthreshold slope
- decrease of mobility



(a) Thickness dependence for positive bias [51]



(b) Field dependence from [51]



(c) Physical motivation from [87]

Figure 13.3: Impact of radiation on MOS structure: Oxide thickness dependence, field dependence and the physical model

Subthreshold slope The characteristics of the MOSFET show an exponential increase of the current below the threshold. Plotted semi logarithmically the inverse slope of this curve could be expressed as

$$S = \frac{kT}{q} \ln 10 \left(1 + \frac{C_d + C_{it}}{C_{ox}}\right) [77]. \tag{13.2}$$

C_{it} is the capacitance related to the density interface traps D_{it}; $C_{it} = qD_{it}$. Thus the difference of the inverse slope before and after irradiation exhibits information of the number of created interface states:

$$\Delta S = kT \ln 10 \frac{\Delta D_{it}}{C_{ox}} [77]. \tag{13.3}$$

Impact on mobility The dependence of the mobility on the number of interface traps N_{it} could be parameterized as

$$\mu = \frac{\mu(0)}{1 + \alpha_{it} \Delta N_{it}}. \tag{13.4}$$

Where ΔN_{it} is the increase of interface states due to irradiation. α is a constant in the order of $10^{-12} 1/\mathrm{cm}^2$ [75].

The decrease in mobility leads directly to a decrease of g_m as well as g_q (see equation 4.3) thus being a relevant issue for the detector operation.

Relation to 1/f noise The increased number of interface states has also impact on the low frequency noise. As described in chapter 6.2.2 the low frequency noise is related to the number of interface states thus an increase has also impact of the SNR of the DEPFET.

13.3 Questions to be answered

The chapter introduced the issues related to radiation damage. The following questions must be answered to assure that the DEPFET preserves his performance while operation at ILC:

- Related to bulk damage:
  - Impact of bulk damage? Extend of leakage current?
  - Required operation temperature to limit the leakage to acceptable level?
- Related to interface damage:
  - Extend of threshold voltage shift on both MOS structures (gate and clear gate)?
  - Are there intrinsic inhomogeneities?
  - Behavior of 1/f noise related to additional interface states?
  - Matrix effects - like clear-clear isolation?

  - Breakdown of oxides due to the increased fields after irradiation?
  - How is the amplification affected by irradiation? (Mobility)

- General questions for operation:
  - What radiation inhomogeneities could be tolerated?
  - Impact of radiation on the resolution?

Chapter 14

Impact of bulk damage

This chapter deals with the impact of bulk damage on the DEPFET detector. As pointed out in the previous chapter the increase of leakage current will be the most important effect.

The first section presents the analysis of two single pixel structures irradiated with neutrons from a spallation source and with low energy protons.

The discussion and crosscheck of the measurements is performed in the following sections.

14.1 Analysis of irradiated samples

To study the impact of bulk damage two irradiations with neutrons and protons where performed. The actual irradiation and dosimetry was done by Davis Contarado at LBNL in Berkeley. A summary of the applied doses is given in table 14.1.

The table gives also the equivalent operation time at ILC to reach the applied doses. Especially the proton irradiation is very harsh compared to the expected doses.

Both devices are single pixel structures - an isolated double pixel. Thus questions related to the matrix operation could not be answered with this irradiation.

Since protons damage both the bulk and the interface a separate section which deals with the interface damage is presented in the next chapter.

Type	Energy [MeV]	Dose [$1/cm^2$]	Dose equ. [$1MeV_{n,equ}/cm^2$]	ILC equiv. time [a]
Protons	30	$1.2 \cdot 10^{12}$	$3 \cdot 10^{12}$	35
Neutrons	1-20	$1.6 \cdot 10^{11}$	$2.4 \cdot 10^{11}$	3

Table 14.1: Summary of bulk damaging irradiations

14.1.1 Neutron irradiation

The neutron irradiated sample was analyzed with respect to leakage current and spectroscopic performance. A change of the electrical characteristics - transconductance and threshold voltage - was not found. As expected since the neutral neutrons dominantly with the nucleus and not with the electrons of the shell.

Spectroscopic performance Figure 14.1 shows the spectroscopic performance of the device. The depicted spectrum is Fe^{55} taken at 6°C. Evidently the structure is working and is still able to separate K_α and K_β at 5.9keV and 6.3K.

The equivalent noise charge (ENC) depending on the shaping time is depicted at 14.1. To limit the leakage current the temperature was set to -18°C. A unirradiated reference is also displayed showing that after cooling the performance is similar to the unirradiated structure.

Leakage current The leakage current was directly evaluated at room temperature to $8.9e^-/\mu s$. The impact on the system performance is discussed in the last section 14.3.

14.1.2 Proton irradiation

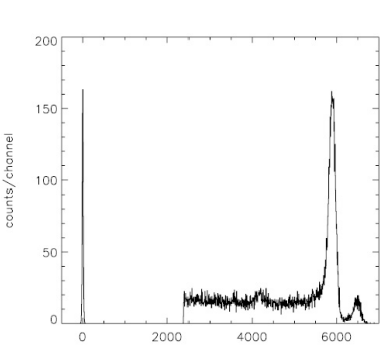
Spectroscopic performance The spectroscopic performance is summarized in figure 14.2. The device is still working after the adaption of the steering voltages. The spectrum was taken at $-18\,^\circ$C showing still an increased noise compared to the unirradiated sample.

The ENC versus the shaping time is depicted in figure 14.2c. At high temperature the noise is dominated by leakage current $ENC_{leak} \approx \sqrt{\tau I_{leak}}$. However at low temperatures the energy resolution shows still an increase.

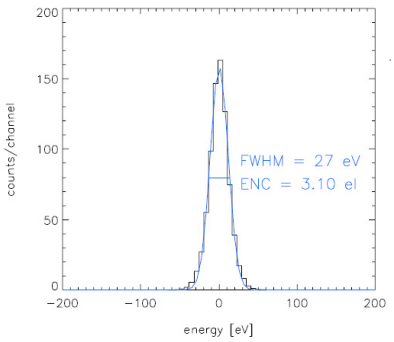
Leakage current The leakage current versus the temperature is depicted in figure 14.3. The two curves show two different operation conditions. The temperature measurement was improved for the black one by incorporating a temperature sensor directly on the ceramics. The first measurement used the temperature sensor from the climate chamber which was not in direct contact with the setup thus incomplete thermalization caused the spread.

The fits are based on equation 6.10 showing that leakage behaves as expected thus allowing to scale the measured values. At room temperature the current is around $120e^-/\mu s$ decreasing to $18e^-/\mu s$ at $0\,^\circ$C.

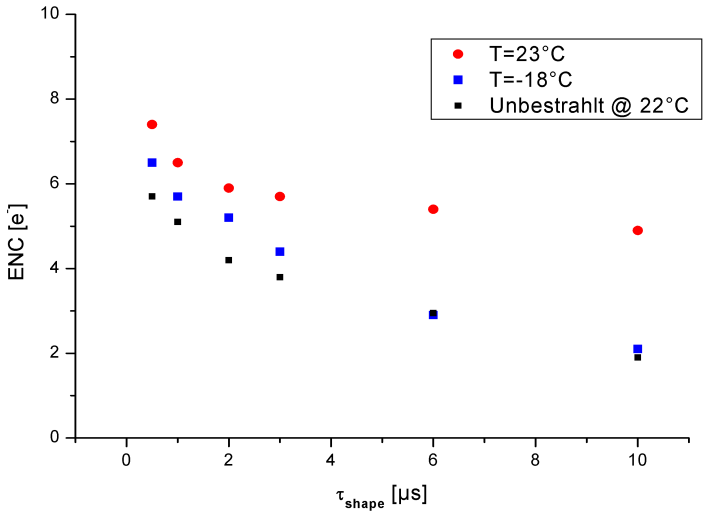
Consistency Since the leakage is proportional to the applied 1MeV equivalent neutron dose the measured leakage current should scale as the dose. At room temperature $120e^-/\mu s$ where measured for the protons and $8.9e^-/\mu s$ for



(a) Fe^{55} at 4°C

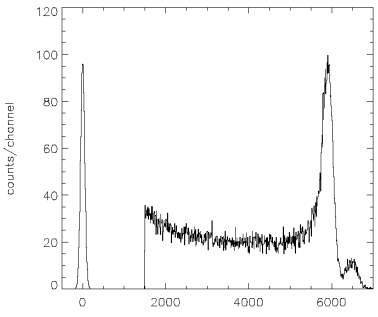


(b) Noise peak at 4°C

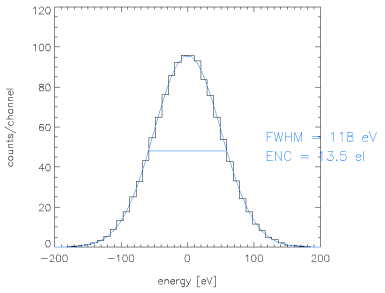


(c) ENC vs. τ

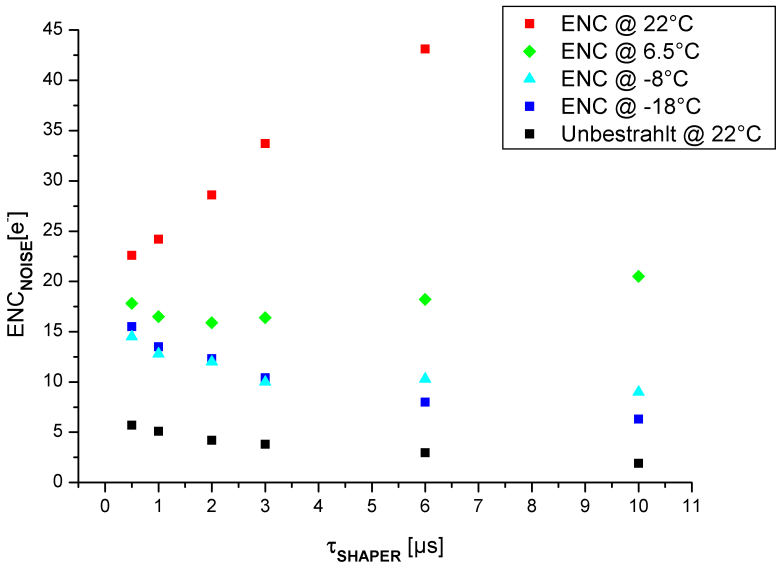
Figure 14.1: Spectroscopic behavior after neutron irradiation



(a) Fe^{55} at -18deg C



(b) Noise peak at -8deg C



(c) ENC vs. τ

Figure 14.2: Spectroscopic behavior after proton irradiation

the neutrons. The factor between the applied fluency is 12.5 and between the leakage currents is 13.5.

Taking into account that the sensitive volume of the single pixel structures is not well defined and could depend on the actual operation conditions the values are consistent.

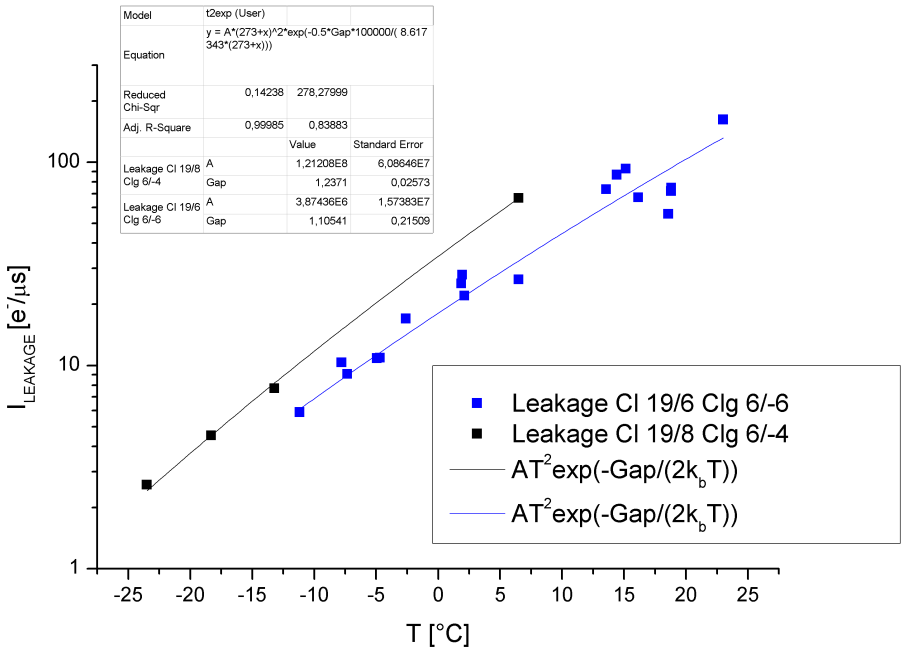


Figure 14.3: Leakage current after proton irradiation

14.2 Expectation from NIEL scaling

Since the NIEL hypothesis is correct for the leakage current, see section 13.1, it is possible to estimate the leakage. Assuming

- the current related damage constant as $4 \cdot 10^{-17}\mathrm{A/cm}^2$,
- a sensitive area of $24\mu\mathrm{m}^2$,
- and a thickness of $450\mu\mathrm{m}$

the current at room temperature could be directly calculated from equation 13.1. Table 14.2 shows the results of this calculation for the performed irradiations and the expected 5 years dose in the inner layer.

The calculation shows that the single pixel structures tend to underestimate the leakage current significantly.

Type	fluency [$1MeV_{n,equ}/cm^2$]	I_{leak} measured [$e^-/\mu s$]	I_{leak} calculated [$e^-/\mu s$]
p	$3 \cdot 10^{12}$	120	194
n	$2.4 \cdot 10^{11}$	8.9	15.5
5 years ILC	$4.25 \cdot 10^{11}$	-	27.54

Table 14.2: Calculation of the leakage current at 20°C for the performed irradiations and after five years operation in the inner layer

14.3 Impact on detector performance

Discussion The previous sections shows the results from two irradiations intended to study the impact of bulk damage on the detector performance. Both irradiations are consistent with each other. The temperature dependence studied for the proton irradiated sample is as expected from theory.

However the calculated value for the leakage current, derived from a damage constant of $4 \cdot 10^{-17} A/cm^2$, show a systematic deviation towards higher currents. To obtain a conservative result, the higher values are assumed to be correct for the following discussion.

Noise contribution from bulk damage Table 14.3 shows the expected shot noise for various scenarios with varying thickness and integration time. The leakage currents are still at room temperature - no cooling is assumed. Allowing a decrease of the SNR by 2 percent, a shot noise of $20e^-$ could be tolerated, if the overall readout noise is $100e^-$.

The bulk damage is caused by the electron positron pairs created from beamstrahlung, see table 3.2. Thus the outer layers are much less exposed to the pairs.

	$25\mu s$	$100\mu s$	$250\mu s$
$50\mu m$	9 e^-	18 e^-	$28e^-$
$75\mu m$	11 e^-	22 e^-	34 e^-

Table 14.3: Shot noise contribution at room temperature for various readout time / detector thickness scenarios

Summary The analysis shows that the impact of shot noise created by bulk damage is no severe problem for the operation of a DEPFET based vertex detector at ILC.

Only a timing like the TESLA baseline (see table 3.2 would require a modest cooling. Assuming the latest ILC timing requirements with a integration time of $25\mu s$ in the inner and $100\mu s$ in the outer layers it is possible to operate the detector at 20 ° C which is quite comfortable.

This is in strong contrast to other detector concepts which require a significant cooling like the CCD option. To limit trapping effects due radiation damage the necessary temperatures range from ≈ 250K[73] or even lower ≈ 230K like reported in [72] .

In addition the operation temperature has strong impact on the power budget. The power which could be carried by a cold gas stream is proportional to the temperature difference of the incoming gas and the temperature of the detector. Thus at a given entrance temperature - limited by the isolation to the outer detector - the allowed power consumption increases with the acceptable detector operation temperature.

Chapter 15

Interface damage

This chapter is dedicated to the interface damage, studying the impact of ionizing radiation on the MOS structures of the DEPFET, namely the effects on the:

1. threshold voltage
2. mobility - g_m,g_q
3. interface states

The first section shows the results of the single pixel irradiations. The proton irradiations and for completeness a summary of a first irradiation survey presented in [13].

Since the single pixel structures are not fully comparable to matrices a setup to irradiate mini matrices has been developed, see section 15.2.

This allowed for the first time to study pixels in a realistic environment. Moreover the setup allows biasing the device completely. The conditions are as close as possible to the real bias conditions in an experiment.

Special attention was given to the second MOS structure - the clear gate. Since it has significant impact on the performance, see chapter 11, its threshold voltage shift was investigated, too.

Matrix effect The matrices allowed also to investigate effects related to them:

1. clear-clear isolation, see 15.3
2. transistor - transistor variations, see 15.6

Technology The examinations evaluate the standard DEPFET technology. Especially variations on the oxide processing (growth, etching) could have impact on the threshold voltage shift.

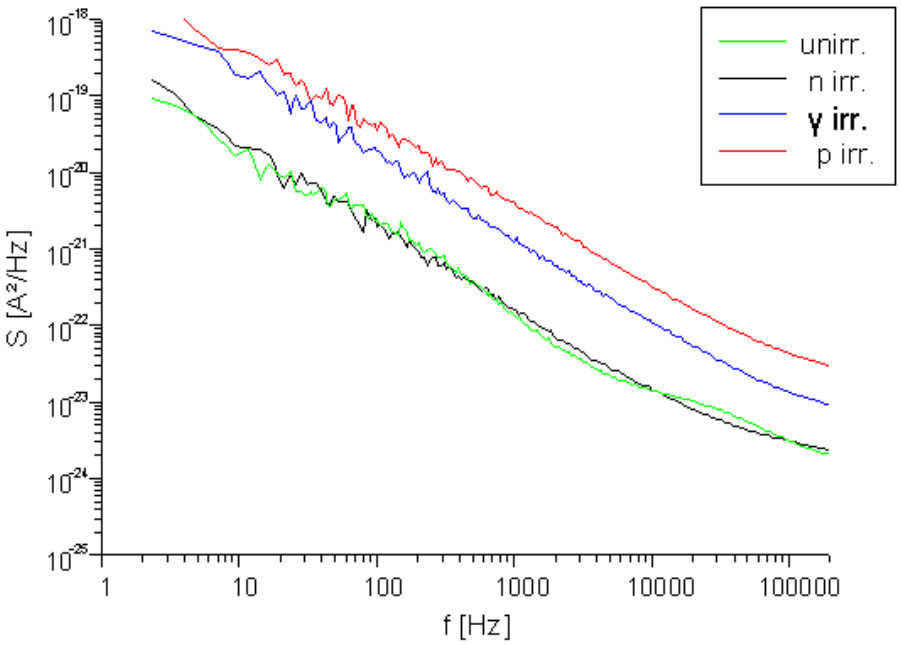


Figure 15.1: Noise power density for proton, neutron and gamma irradiation [4]

15.1 Single pixel irradiations

15.1.1 Proton irradiation

As pointed out in section 14.1.2 the noise of the irradiated sample is enhanced even at low temperatures where the leakage current is limited.

Low frequency noise The low frequency noise was directly measured showing an increase of nearly one order of magnitude, see figure 15.1. The other irradiations are also depicted for comparison.

Electrical characteristics The electrical characteristics are shown in figure 15.2. The transfer characteristics $I_{ds}(U_{gs})$ is shown in the top graph. Evidently a threshold voltage shift is visible. The shift is 5.6V at an ionizing dose of 284kRad.

Above all the sub threshold slope increased from 102mV/dec to 326mV/dec. This is consistent with increase in low frequency noise.

The transconductance is depicted in the lower plot of figure 15.2 showing that the g_m is noticeably reduced from 33.5μS to 28.5 μS at 50 μA- a decrease of 15%.

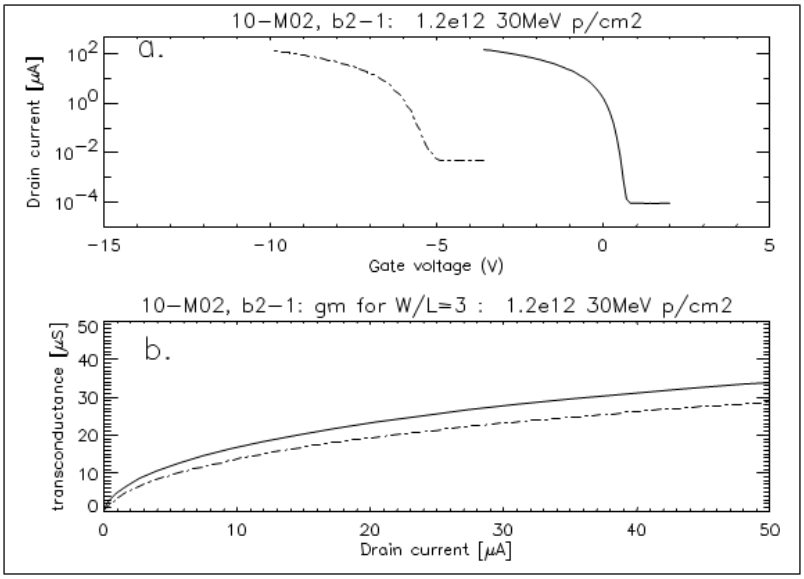


Figure 15.2: Electrical characteristics after proton irradiation of 283kRad showing a threshold shift of 5.6V and an increase of the subthreshold slope of 224mV/dec

15.1.2 Gamma irradiation

A first investigation of the impact of ionizing radiation was performed with gamma radiation [13]. Various devices with different geometry were irradiated. The gate-source voltage was fixed at two values simulating a DEPFET in OFF and ON state. Moreover a bulk voltage of 10V was applied.

The measured threshold shift and the annealing at room temperature is depicted in figure 15.3.

15.2 Mini matrix irradiation setup

The previous described irradiations were performed with all ports (gate, clear gate, clear, backside) grounded or partially biased. The next step was to perform irradiations under full bias. To achieve this, a board which allows switching between irradiation conditions and analysis conditions was developed within this thesis.

The setup must allow applying the following bias voltages:

- gate - source voltage U_{gs} (ON / OFF) separately for rows under test and the rest
- drain - source voltage U_{ds}
- bulk voltage
- clear gate voltage

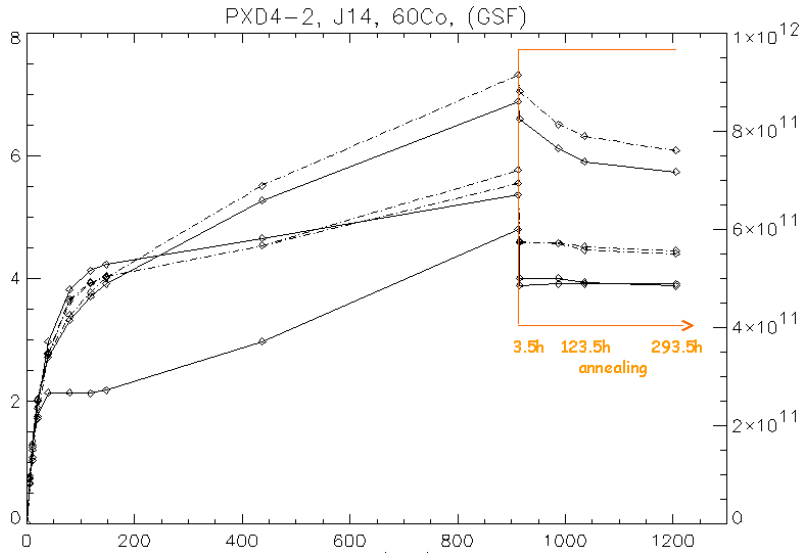


Figure 15.3: Threshold shift of gamma irradiation taken from [13]

- backside voltage for depletion
- clear voltage (constant for analysis / pulsed for irradiation)

In addition the gate voltage and clear voltage must be separately accessible for the rows under test. To analyze a distinct transistor a single drain contact must be accessible.

Figure 15.4 shows a picture of the irradiation board. The device under test is mounted on a 40 pin carrier. The pin assignment was made in a way to be compatible with the single pixel setup which allows to perform spectroscopic as well as g_q measurements.

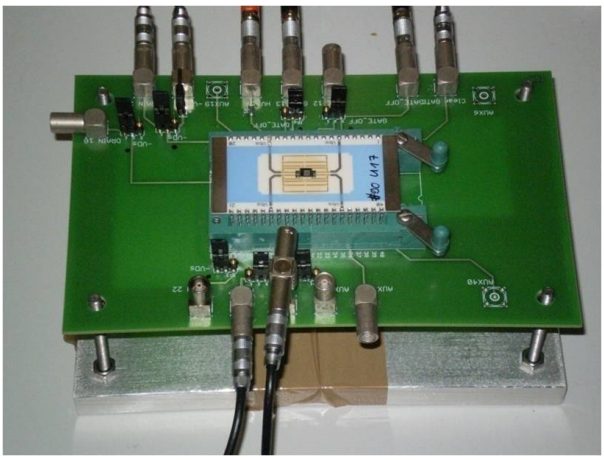


Figure 15.4: Picture of the irradiation board

Irradiation condition Table 15.1 gives a summary of the applied bias under irradiation. The detector was fully biased and the hole volume was depleted. Moreover the potential on the clear was clocked with a period of 50μs.

The potentials applied to the MOS structures - clear gate and gate - could change while irradiation.

Voltage	Value [V]	Variable while irradiation
U_{gs}	+5	adaptive
U_{ds}	-5	fixed
bulk	+15	fixed
clear gate	-0.5	adaptive
backside	+180	fixed
clocked clear	+18/+5 (1μs/50μs)	fixed

Table 15.1: Irradiation conditions

Stability under irradiation Since the dose rate used for the irradiation O(150kRad/h) is much larger than under real experimental conditions it is necessary to assure that biasing is stable while irradiation.

To limit the current a shunt resistor (400kΩ) is used to bias the backside. The current into the backside was directly measured at a dose rate of 185kRad/h - 0.5μA. This current leads to a voltage drop of 0.2V. Since the detector is operated 40V over depletion the voltage drop is negligible.

The charge flowing into a pixel could be estimated to 7ke$^-$/cycle. The potential change of the internal gate is about 80mV. This change is not able to change the state (ON/OFF) of the pixel - the FET is typically operated at a voltage of +4V above the threshold.

The considerations show that the biasing of the DEPFET while irradiation could be regarded as stable.

15.3 Measurement program

MOS structures The irradiations are intended to study both MOS structures of the DEPFET - the gate and clear gate. The behavior of the gate is important since the performance of transistor depends strongly on it.

For the clear gate structure the impact on the mobility and interface states is of minor importance. However the g_q and clear performance are very sensitive to the clear gate voltage. Thus the threshold shift on the clear gate must be studied under realistic operation conditions.

The threshold shift of the clear gate could be directly measured utilizing the parasitic clear gate transistor. By applying a voltage, negative enough, a current can flow. The current path is indicated in figure 15.5 with the purple arrows.

Since no shallow p is under the clear gate the threshold voltage is typically 4V below the threshold of the gate.

Matrix Effects In contrast to previous irradiations which were based on single pixel structures the matrices allow to investigate matrix effects.

One possible effect is the clear - clear isolation. Since a voltage difference of O(10V) is applied between to neighbouring rows it could be possible that a current flows between these clear contacts. The current path is indicated in figure 15.5 with the red rows. If this current exceed the driving capabilities of the switcher this could result in a severe problem.

Especially for matrices where the clear gates are separated for each row e.g. the capacitive coupled clear gate matrices is an issue.

Above all the analysis could reveal unexpected phenomena which have impact on the performance.

Transistor - transistor variations The irradiation of similar transistors allows also to study device intrinsic variations of the response to ionizing radiation.

Extension of the dose The irradiations aim to increase the dose into the MRad regime. The reason for that is twofold: On the one hand studying the possible limitations of DEPFET and on the other in view of new applications like SuperBelle, see chapter 5.4.

Since it is very likely that the irradiation is not homogeneous within an detector module. The extended range could serve as basis for an analysis of pre irradiations to limit the effects of inhomogeneities, see chapter 16.

15.4 Gate and clear gate threshold shifts

The threshold shifts are investigated with respect to two biasing schemes:

- constant bias while irradiation
- bias adapted with respect to the measured shift

In principle the last scheme is the most relevant one. Especially the level applied to the clear gate must be adapted to assure that the performance is stable. The level applied to the gate (the gate off value) could remain unchanged as long as the switcher allows to apply a proper gate on value. Thus the first scheme is more relevant for the gate.

15.4.1 Threshold shift of the gate

The threshold voltage shift of the gate in depicted in figure 15.6. The applied bias is depicted as solid line. The first graph shows the irradiation with constant bias - the bias was fixed for most of the time.

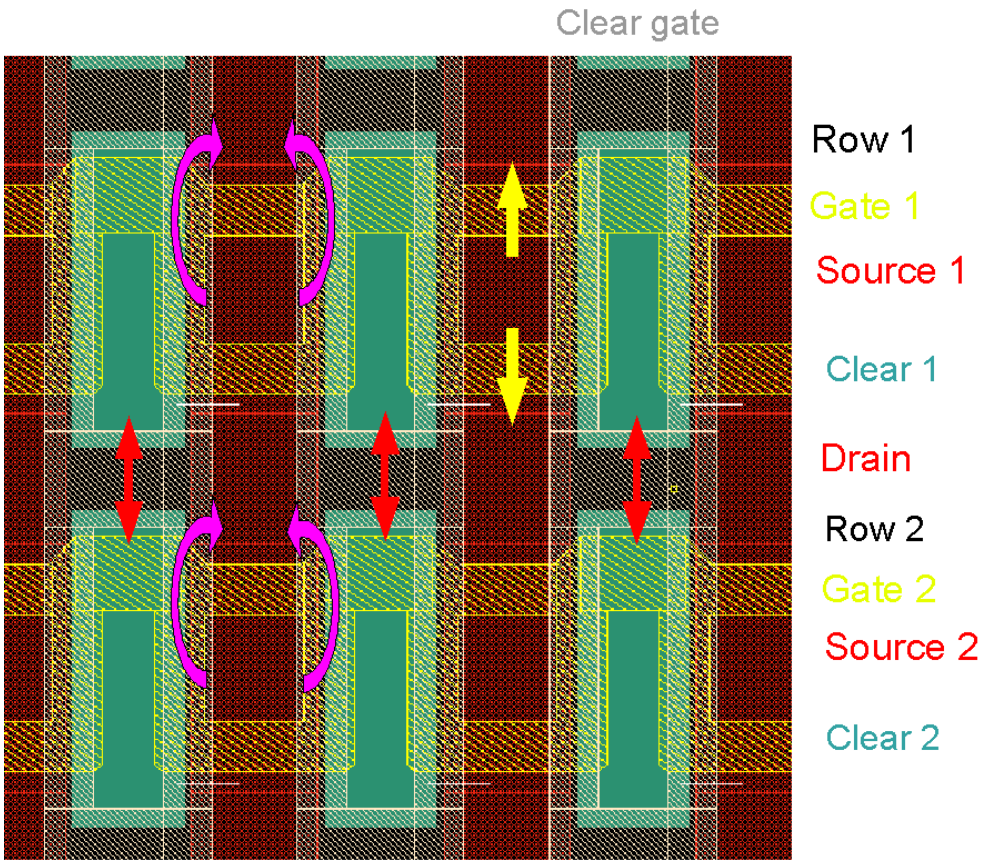


Figure 15.5: Layout of a matrix showing two rows with double pixels. The various current paths are indicated by arrows. The p++ source and drain implantation in red; n+ clear implant in green; Poly 1 in yellow and poly 2 grey

The second one shows threshold under full adaption of the bias. Evidently the full adaption leads to a significant higher threshold voltage shifts than the constant bias. Moreover the increase is linear and shows no indication of saturation.

This behavior is in contradiction to the simple picture that the applied voltage to the gate drops over the hole fully depleted bulk thus the electrical field is small compared to the situation in a MOS structure.

15.4.2 Threshold shift of the clear gate

Figure 15.7 shows the similar measurement for the clear gate. The fixed bias remained constant besides one adaption. However the adaptive scheme depicted in 15.7b was not fully adopted since the structures become very delicate to handle if the large voltages are applied to the clear gate. A breakthrough of the poly 1 - poly 2 insulator would have lead to problems when investigating the transistor-transistor variations which was the main goal of this measurement.

Nevertheless also the clear gates show a similar behavior than the gates: the adaption of the bias leads to a buildup of the threshold voltage shift.

Common to both measurements is the fast increase of the threshold voltage shift at the beginning.

This fast increase is of great interest when inhomogeneous irradiation is regarded.

15.4.3 Bias dependence

Gate Evidently the biasing has a strong impact on the observed shifts, even if the detector is fully depleted. This is in contradiction to the simple picture that the applied voltage to the gate drops over the whole bulk.

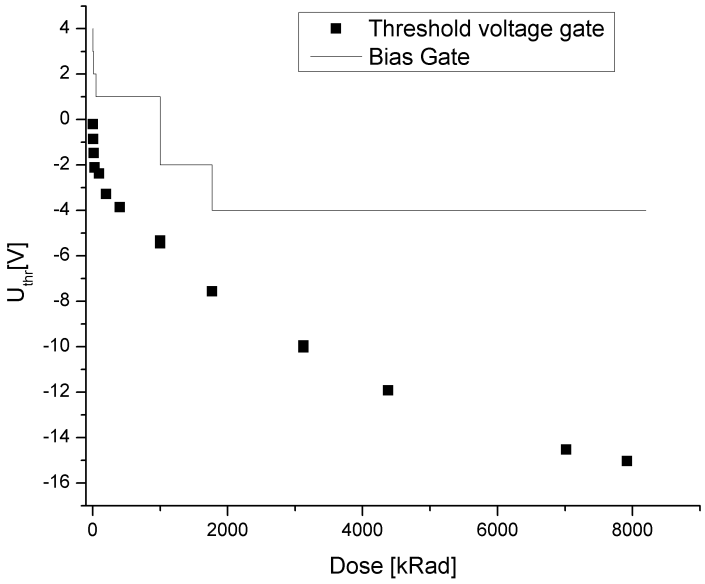
A simple finite element calculation revealed a more realistic picture: The source and drain regions are kept on a fixed potential thus in the small overlapping regions - under diffusion of the source and drain p++ implant under the gate - high fields are existing. Especially the source region is vital for the operation of the FET since the holes must be injected form the source.

Figure 15.8 shows finite element calculation (FEM) of the potentials in the source region.

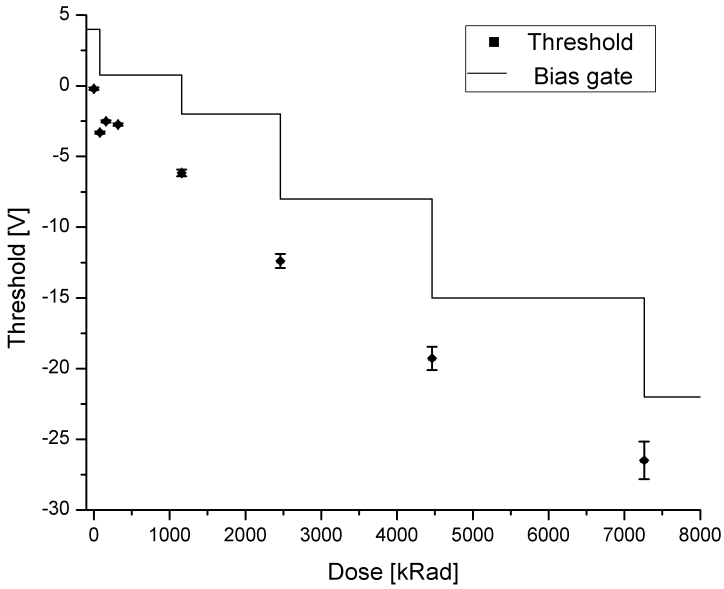
Clear gate The bias dependence is also visible on the clear gate. The previously described argument can be applied in a similar way. The current path for the clear gate transistor is depicted in figure 15.5. The potential of the clear is fixed in the same way thus leading to the same effect - a bias dependence.

15.4.4 Room temperature annealing

As pointed out in chapter 14.1 the detector can operate at room temperature (20°C). Since the shot noise due to leakage current created by non ionizing

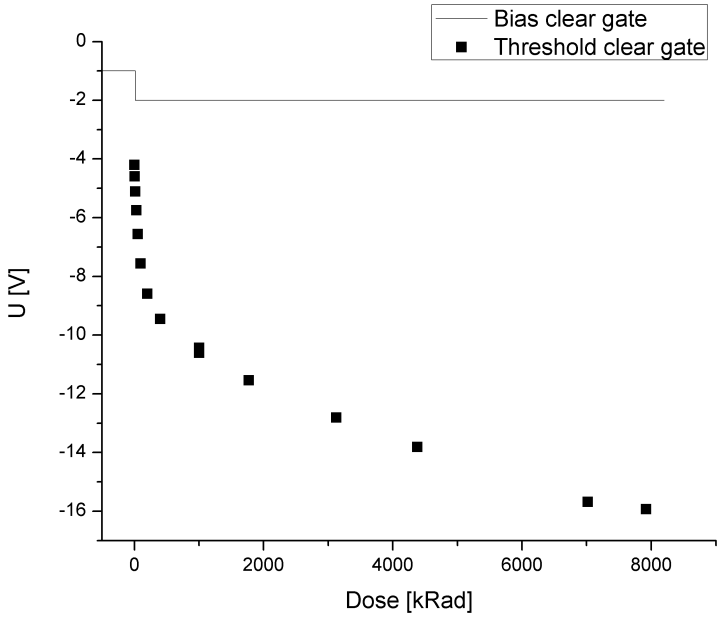


(a) Threshold gate not adapted

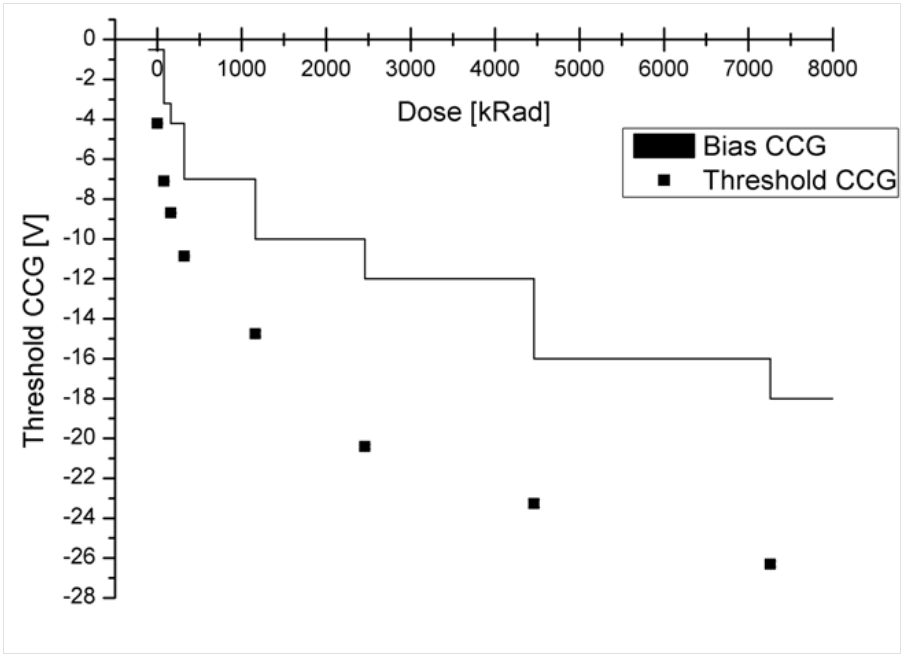


(b) Threshold gate adapted

Figure 15.6: Threshold shift of the gate for fully adaptive biasing and a fixed one



(a) Threshold shift on the clear gate with fixed biasing



(b) Threshold shift on the clear gate with partially adaptive biasing

Figure 15.7: Threshold shift on the clear gate, showing that adaptive biasing leads to a significant increase of the threshold voltage shift

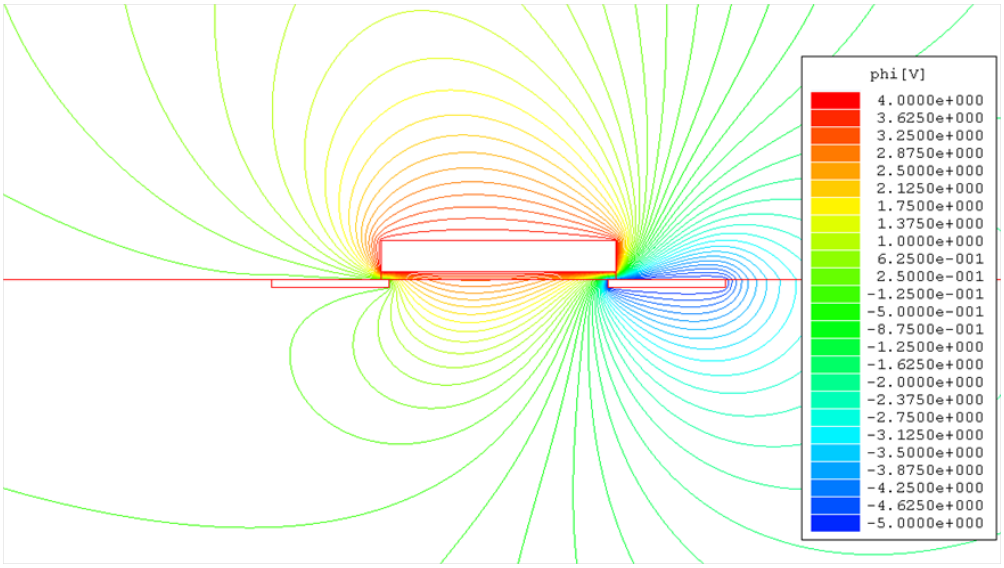


Figure 15.8: FEM simulation of the source region of the DEPFET; source at ground (left contact), gate at +4V (middle), drain at -5V (right contact), oxide 200nm

radiation damage is acceptable at the readout speed and thickness of an ILC vertex detector.

The elevated temperature already leads to an annealing of threshold voltage shift while operation.

Adaptive biasing Figure 15.9 shows the effect of room temperature annealing on the gate. The irradiation was performed with adapted biasing. A strong annealing is observed, reducing the threshold voltage shift from 26V to 16V. The annealing process reduced the buildup of the threshold voltage shift significantly.

15.5 Interface states

Number density The interface state density was evaluated using the relation described in chapter 13.2.2. Figure 15.10 shows the increase of the sub threshold slope with the dose.

Impact on mobility The impact of the increased number of interface states on the mobility was studied by evaluated by measuring the transconductance g_m. Figure 15.11 shows the transconductance before and after irradiation plotted against the current. After room temperature annealing a decrease of the transconductance is remaining. At $100\mu A$ the g_m is reduced by 14 percent.

This shows that the mobility is noticeably reduces. The mobility is a necessary requirement to achieve a high g_q, compare to chapter 9. Thus a decrease

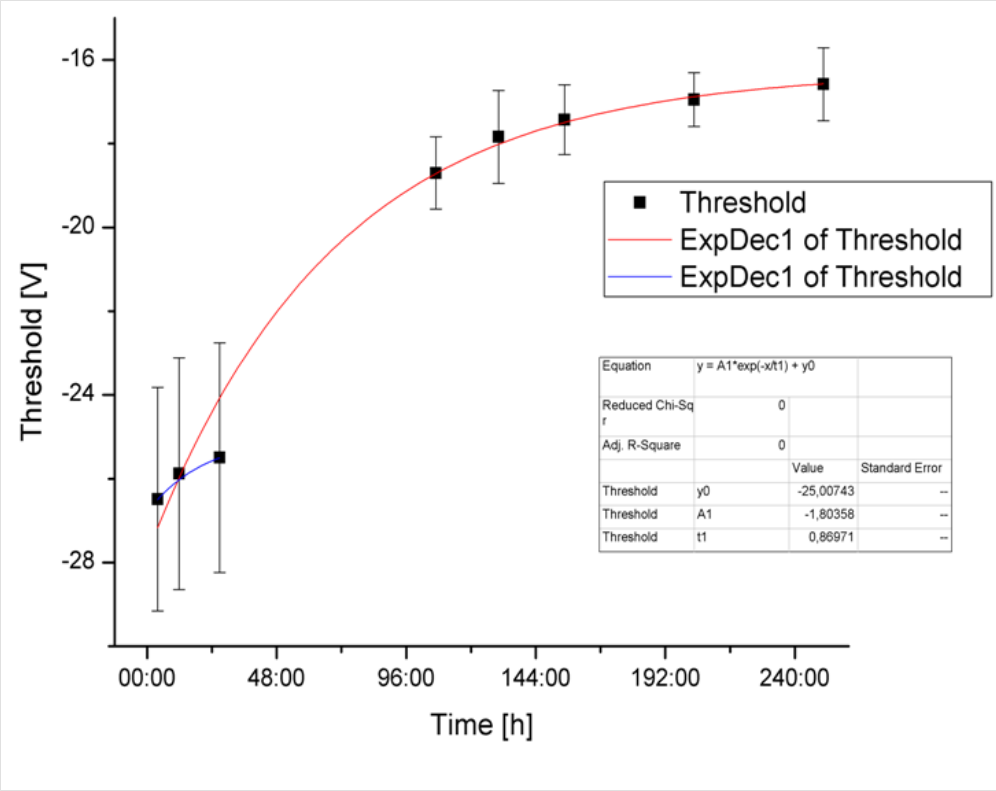


Figure 15.9: Room temperature annealing of the threshold voltage shift - after irradiation with adaptive biasing. The error bars showing the development of the range of the threshold voltages, see section 15.6

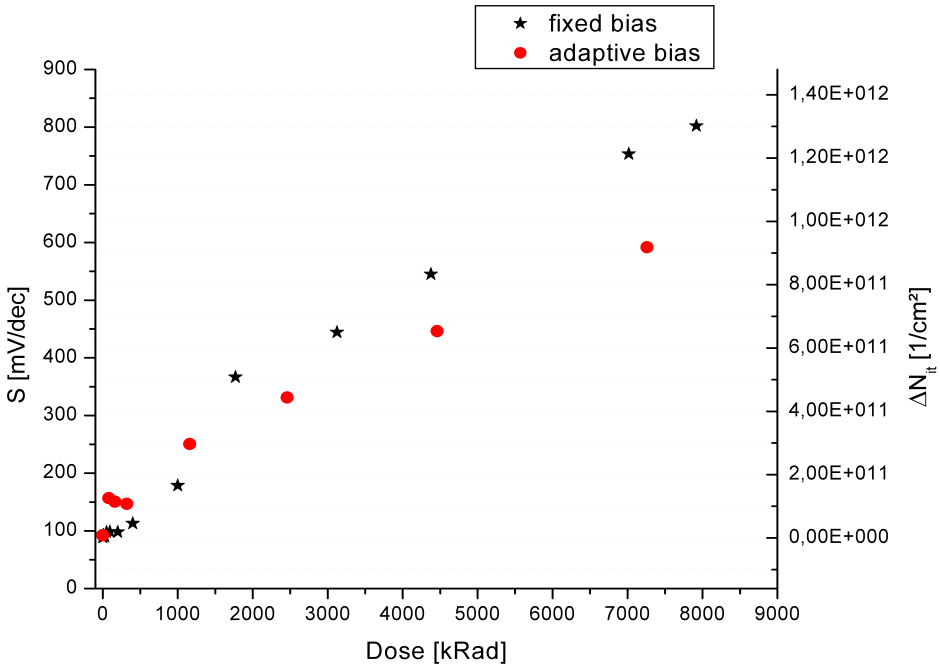


Figure 15.10: Subthreshold slope and interface state density

of the internal amplification by the same amount could be expected.

15.6 Transistor-transistor variations

The intrinsic variations of the threshold voltage shift were evaluated using 16 neighboring transistors of the mini matrix. Thus the spatial extend of the area is below $256 \cdot 256 \mu m^2$. The beam spot has a diameter of 20mm thus the dose could be regarded as constant.

Gate Figure 15.12a shows the range - the difference of minimal and maximal measured value - versus the dose. The range stays constant until 500kRad are reached - this region displays the intrinsic variations due to processing.

At higher doses the range increases linearly with the dose, similar to the threshold itself (see the section 15.4.1) and reaches a final value of 2.8V at 8MRad.

The effect of room temperature annealing is depicted in figure 15.12b showing that room temperature annealing leads to an significant improvement of the situation. The threshold range drops from 2.8V to 0.8V.

For the doses at ILC of 250kRad after 5 years (without safety factor) this effect could be neglected.

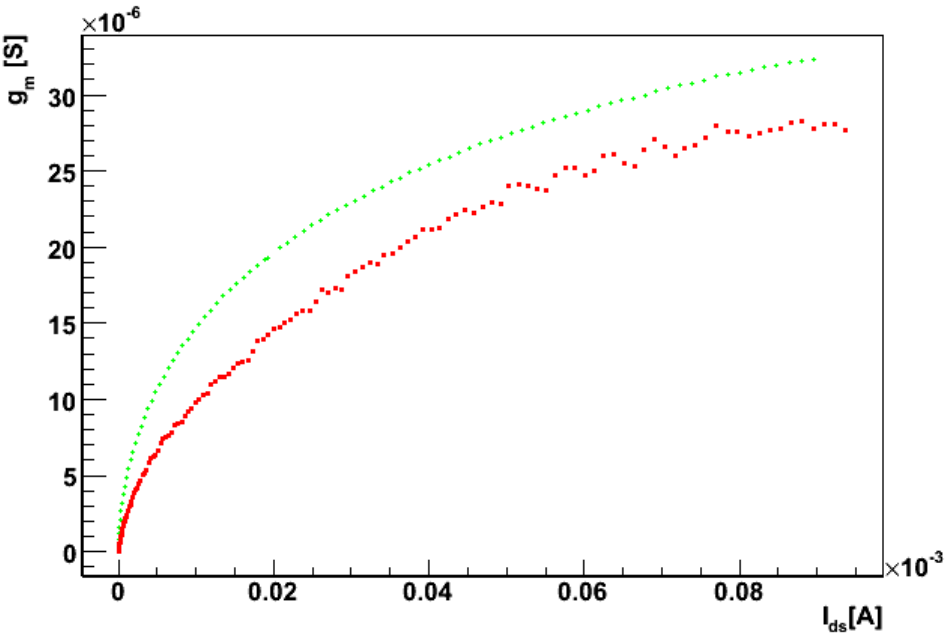


Figure 15.11: Transconductance g_m before irradiation (green) and after 8MRad and 256h room temperature annealing (red).

Clear gate The dispersion on the clear gate is as important as on the gate. The used matrices are of th common clear gate type this means that the clear gate of a single row is not accessible thus dispersions are averaged out.

A precise evaluation could be done utilizing the clear performance of each pixel. At low clear high voltage O(10V) the clear performance is very sensitive to the clear gate setting. By sweeping the clear gate the onset of the full clear could be determined. Such measurements will be possible with the currently developed mini matrix setup.

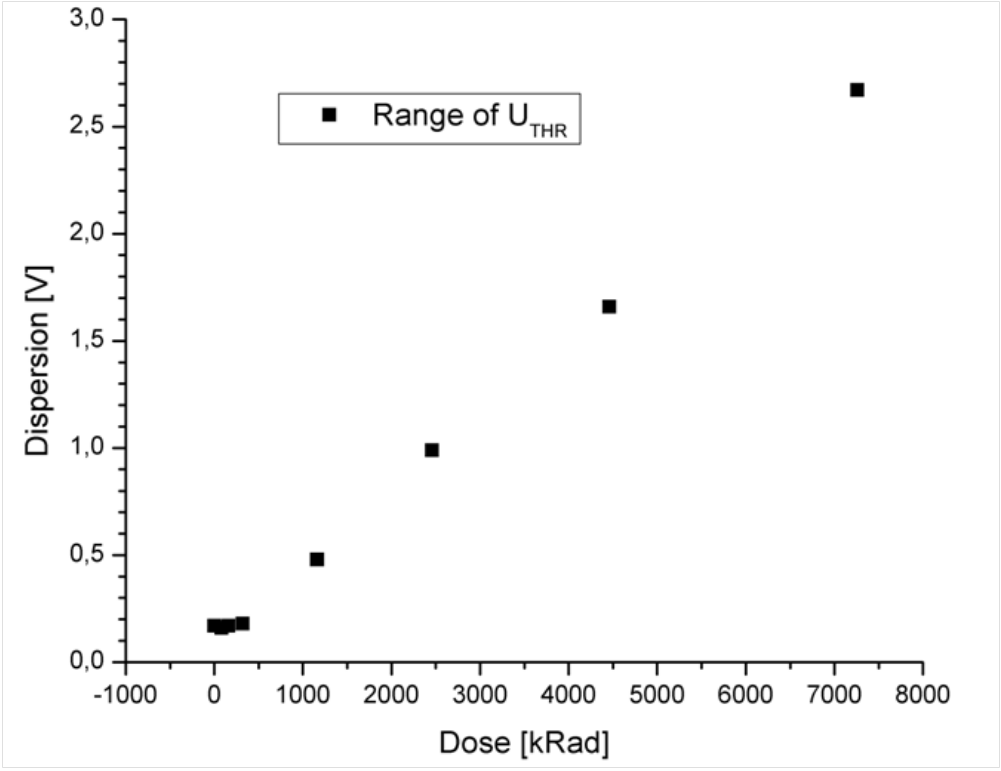
15.6.1 Source of the variation

One reason for the increase of the variation of the threshold voltage could be found in the source gate region.

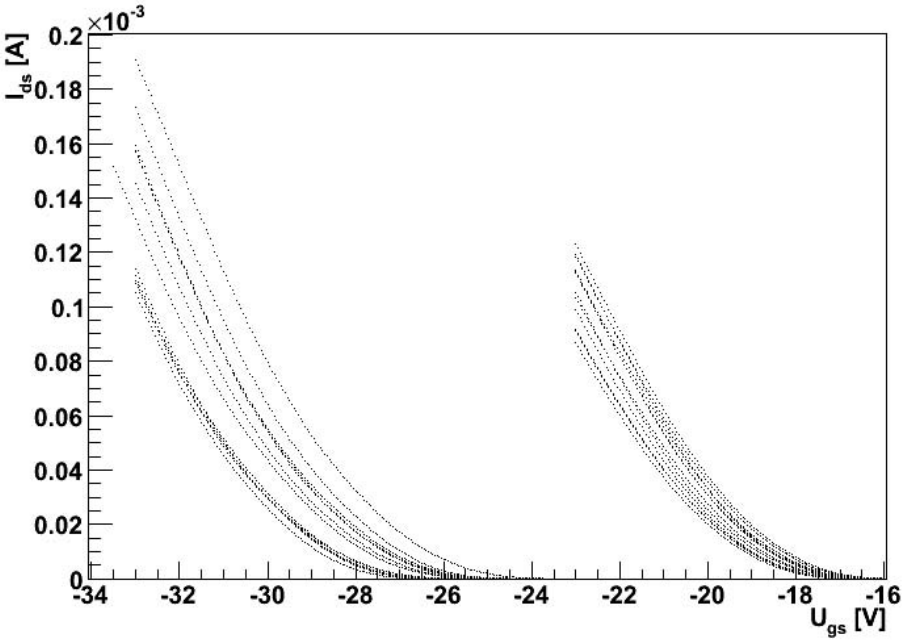
The output characteristics is shown in figure 15.13.

In the irradiated state the characteristic shows strong deviation from the linear regime at low drain source voltages. The current does not increase linear as expected and realized in the unirradiated case. This is a sign for a bottle neck for the holes in the source region - if in the source region the oxide shows a higher voltage shift the threshold voltage is locally lower and a higher drain source voltage is required to overcome this barrier.

In principle this is equivalent to a serial connection of two transistors - a short one with a negative threshold voltage and a long one with a less negative threshold voltage.



(a) Dispersion of threshold voltage of neighboring transistors



(b) Transfer characteristics after irradiation and after 258h room temperature annealing

Figure 15.12: Dispersion of threshold voltage of neighboring transistors and annealing

The fields in this region are varying strongly with the overlaps of the gate and the source implantation. The roughness of the gate thus leads to a varying overlaps and thus to the dispersion.

This behavior is an additional hint for the observed bias dependence, see section 15.4.3.

After room temperature annealing this behavior is reduced to an extend that is hardly visible, see 15.13. Also the dispersion drops from 2.8V to 0.8V. This shows that the dispersion is closely related to the source region.

15.7 Clear - Clear isolation

The clear-clear isolation (see the current path on page 134, figure 15.5)was directly evaluated by varying the clear potential at one distinct row. The current flowing into this contact was directly measured.

The new PXD5 devices have a bias resistor which enables to bias the clear and gate with one connection. This results in a standing current if a potential difference is applied. The resistors are made in way that the driving capabilities of the switcher chips are not exceeded.

Thus the measurement precision is limited due to this current. However it is only necessary to assure that the currents flowing do not exceed the driving capabilities.

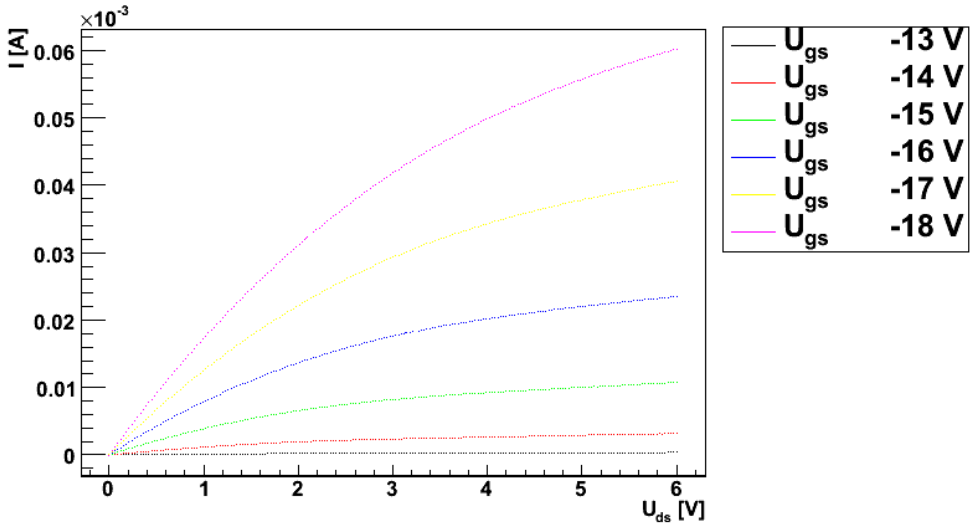
Figure 15.14 shows the current flowing into the clear of one row (the other rows are on 16V). The linear dependence on the voltage is clearly visible. Only for a clear gate setting of 0V a deviation is visible. Since the threshold shift on the clear gate is about 10V at this point this setting is far to positive for DEPFET operation.

After adopting the clear gate voltage no excess current is visible. Thus clear-clear isolation is no problem for the investigated matrix type.

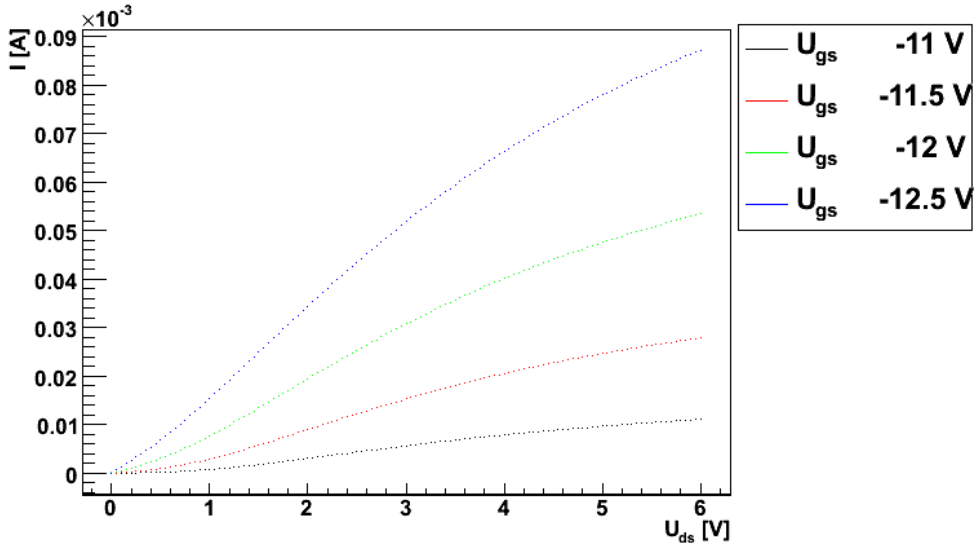
15.8 Spectroscopic performance

The spectroscopic performance after heavy irradiation was studied utilizing an RC-CR shaper. The equivalent noise charge is depicted in 15.15a. In addition a Fe^{55} spectra is shown in the figure below. The spectroscopic performance is still very good.

The measurement shows that the DEPFET is still operational after 8MRad. There are no further effects which lead to a decrease of performance.



(a) Output characteristics after room temperature annealing



(b) Output characteristics directly after irradiation at 3MRad

Figure 15.13: Output characteristics $I_{ds}(U_{ds})$ while irradiation and after, demonstrating that a bottleneck for charge carrier exists in the source region

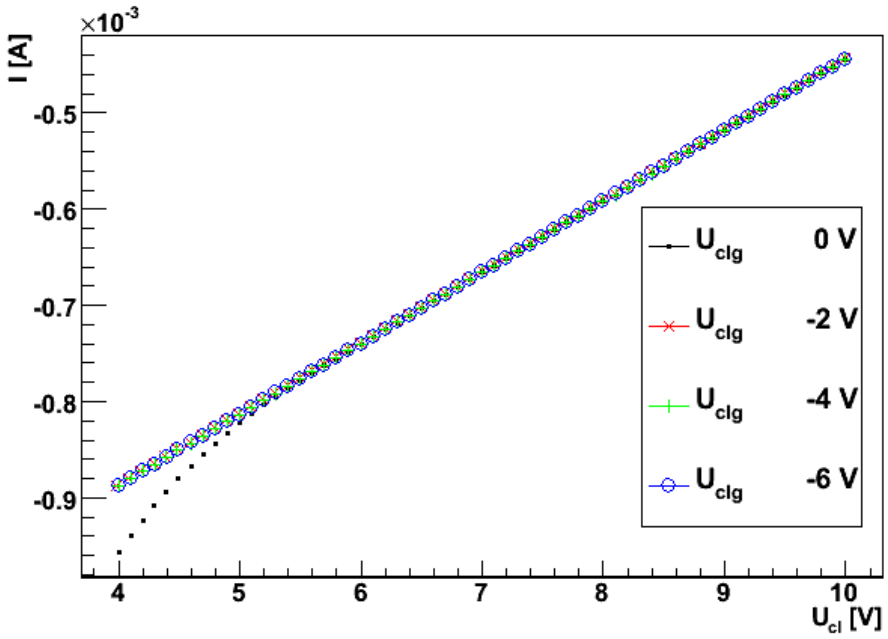


Figure 15.14: Clear - clear isolation at 4 MRad

15.9 Summary

The chapter gave a broad overview of the effects of ionizing radiation on the DEPFET. The impact has been studied on the basis of single pixel structures and then extended to mini matrices.

Single pixel irradiations The proton irradiation allows investigating both non ionizing and ionizing radiation damage. The results for the NIEL damage are presented in the previous chapter 14.

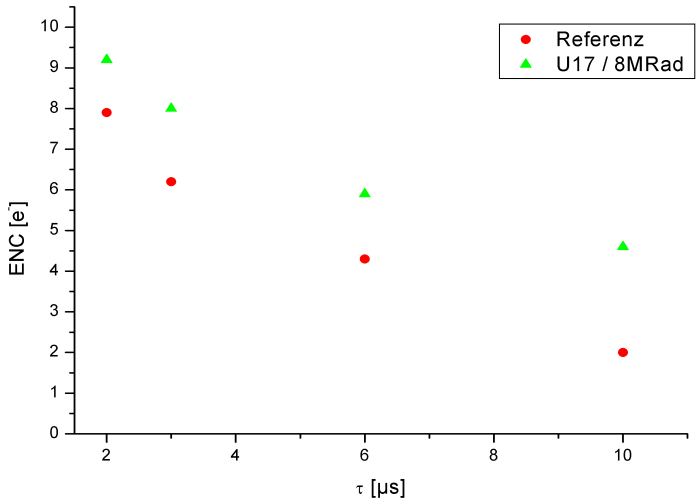
The investigated proton irradiated sample showed a slightly higher threshold voltage shift compared to the gamma and x-ray irradiation - 5.6V at 283kRad. The low energy protons (30MeV - 33MeV/cm [55]) as radiation with high linear energy transfer (LET) have a very dense and columnar charge deposition different to the deposition of the low energy electrons created by x-rays. Thus the comparison is difficult.

Mini matrix irradiation The mini matrix irradiations extended the performed irradiations into up to 8MRad. These measurements demonstrate for the first time that DEPFET matrices are operational after this dose.

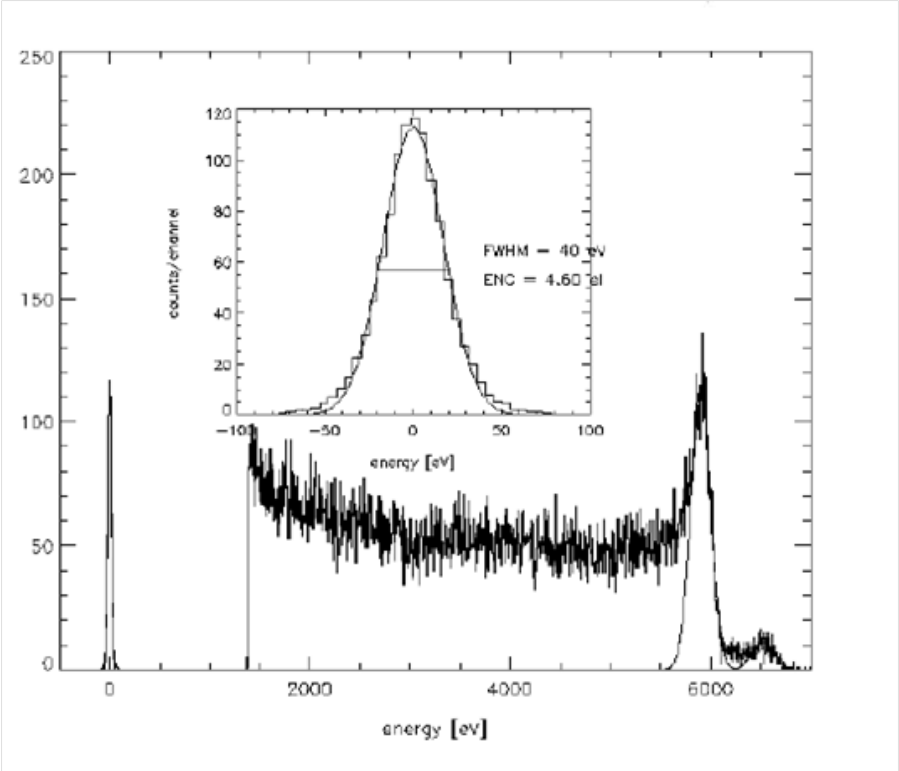
Matrix effects are investigated, but there is no indication that problems due to the direct neighbourship of the pixels are exist.

The observed spectroscopic performance is still good, the equivalent noise charge is below $5e^-$. Thus the impact of the increased 1/f noise is acceptable.

The transconductance after 8MRad is decreased by 14% thus the internal amplification is expected to suffer by the same amount.



(a) ENC vs. shaping time after 8MRad



(b) Fe^{55} spectra after 8MRad

Figure 15.15: Spectroscopic performance of the DEPFET after 8MRad ionizing radiation

The measurements confirmed the dependence of the threshold voltage shift on the biasing conditions of the DEPFET. The threshold voltage shifts strongly depend on the biasing of the DEPFET during irradiation. The adaptive biasing shows an linear increase of the threshold with the dose. The saturation like observed for a fixed bias is not visible anymore. The behavior could be attributed to the increased fields in the gate source region.

Besides this the parallel irradiation of 96 transistors allowed to investigate transistor-transistor variations. It was found that dispersion of the thresholds increases with the dose. After 8MRad the dispersion was about 2.8V resulting into a severe dispersion of the current through the pixels. However room temperature annealing decreased the dispersion to an level of 0.8V.

Outlook The performed irradiations revealed several new features. Especially the bias dependence makes it necessary for future irradiations to have a dedicated bias scheme during irradiation, depending on the envisaged switcher chips and their switching capabilities.

A realistic bias scenario for a large range switcher could be: starting at a gate off voltage of $\approx +5$V, adopting until 0V is reached and afterwards remaining constant. This would significantly limit the buildup of the threshold voltage shift as observed in the fully adoptive measurement.

Since the radiation at ILC will mainly consist of electrons it necessary to perform irradiations with this particle type. As learned from the proton irradiation different incident particles lead to different threshold voltage shifts. Electron irradiations will allow to get final confidence that the threshold voltage shifts will be below 5V at 1MRad.

The observed fast increase of the threshold voltage shift at the beginning is an important issue when dealing with inhomogeneous irradiation.

Chapter 16

Impact of irradiation inhomogeneities

As pointed out in the previous chapter ionizing radiation leads to significant shift in the operation parameters which make an adjustment necessary. Shifts resulting from inhomogeneous radiation especially in r $-\phi$ - perpendicular to the readout direction - are difficult to compensate. Thus the question arises: What amount of inhomogeneities could be tolerated?

The first section gives an overview of simulations carried out to investigate the number of background hits and their spatial distribution.

In the second section the dispersion of the operation parameters of cells which experience different doses is investigated.

In the following the impact of this dispersion on the system performance is discussed, taking into account the various readout scenarios:

- common clear gate operation
- clocked clear gate operation
- capacitive coupled clear gate

16.1 Inhomogeneities in the ILD vertex detector

The background and its spatial distribution is investigated in [85] and [26]. Figure 16.1 shows the background along the z axis and ϕ.

Since the ionizing radiation is mainly caused by the background hits, inhomogeneities in the hit distribution are directly related to variations of radiation dose.

The geometry for the simulation is taken from the ILD concept. The crossing angle is 14mRad.

The color of the plots refers to different cuts of the hit time - green a short hit time, blue a large one. Since the hit time is proportional to the traveled path of the particles it is possible to distinguish direct hits (short hit time) from backscattered ones (large hit time).

The spikes visible in both figures along ϕ are artifacts. Since the ladders have overlapping regions hits are counted twice.

Especially the number of backscattered particles is very sensitive to the layout of the forward region. By introducing A Detector Integrated Dipole (anti - DID) it is possible to reduce the background significantly. Moreover the anti-DID leads to a much more homogeneous hit pattern along ϕ, see figure 16.1b and 16.1a.

Conclusion The analysis showed that an inhomogeneous irradiation is extremely likely. Especially without anti-DID magnet the vertex detector has to cope with inhomogeneities along the ϕ direction. Also along the z direction inhomogeneities of about 20% are visible.

16.2 Inhomogeneities and parameter dispersion

This section investigates the variation of the operation parameter due to inhomogeneities of the radiation. The figure of merit used here is the range of the parameter dispersion from higher irradiated parts to the lowest exposed parts. An analysis of the spatial distribution is not performed.

A small dispersion is sufficient to assure that the inhomogeneities could be tolerated.

The dispersion ΔU is calculated from the measured threshold voltage shifts via

$$\Delta U = U_{thr}\left(D\right) - U_{thr}\left(\frac{D}{1+\frac{\delta}{100}}\right). \tag{16.1}$$

δ is the inhomogeneity of the radiation. An inhomogeneity of 100% means that one zone receives 100kRad and another 200kRad.

16.2.1 Clear gate

Figure 16.2 shows the dispersion on the clear gate. The calculation based on equation 16.1, using the depicted fit model as basis.

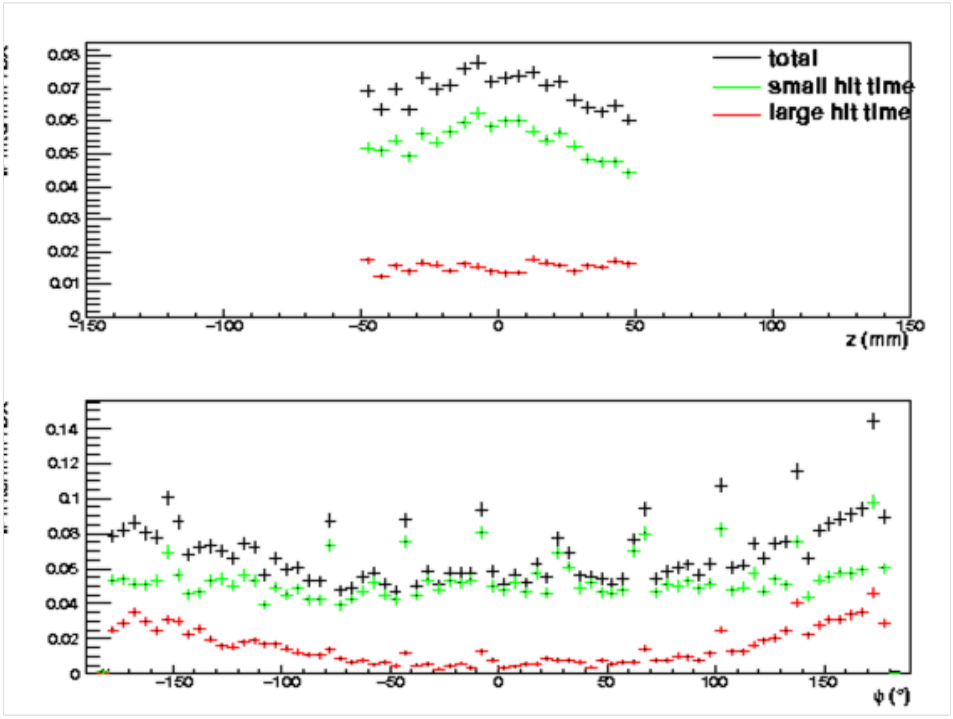
The fit is an empirical model, a second order polynomial in $log(Dose)$, which reflects the features of the measurement: the fast increase at low dose and the saturation at higher doses.

The dispersion increases very fast until 1MRad is reached - the region of interest for ILC. Beyond 1MRad the increase is limited.

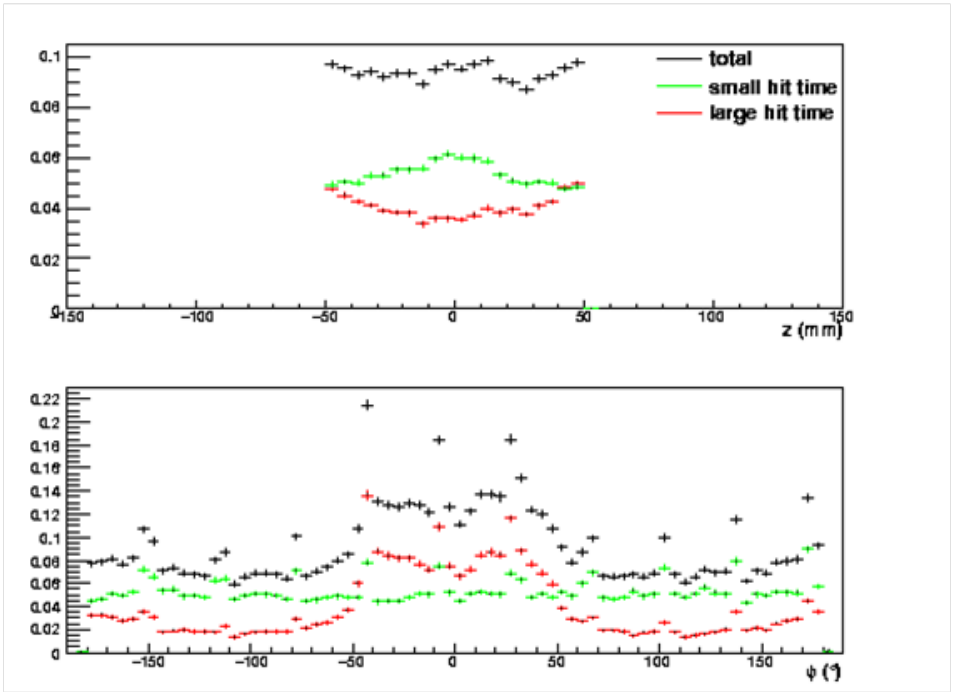
16.2.2 Gate

The dispersion on the gate is depicted in figure 16.3. The analysis is similar to the clear gate.

Compared to the clear gate the dispersion is significant higher and does not show a saturation behavior. This is related to the different shape of the

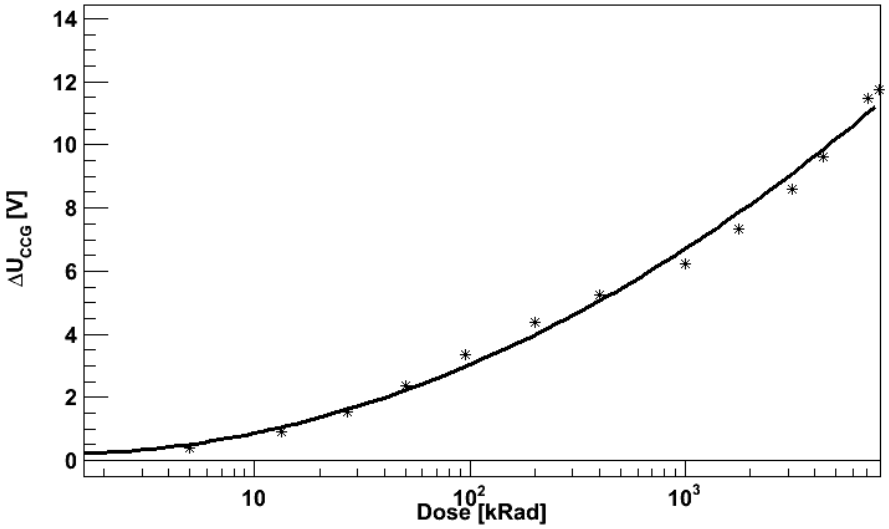


(a) Hit distribution in the first layer with anti-DID, from [26]

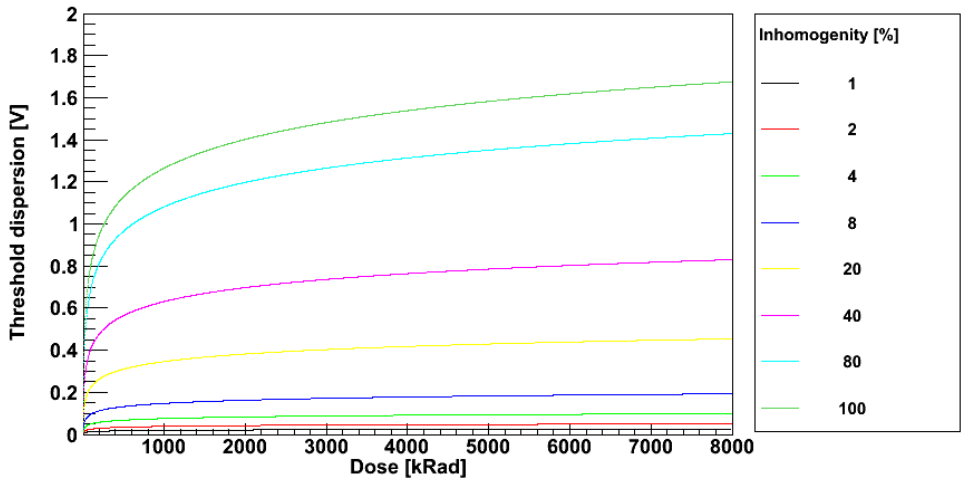


(b) Hit distribution in the first layer without anti-DID, from [26]

Figure 16.1: Hit distribution in the ILD detector along z and ϕ; showing that significant inhomogeneities could appear



(a) Empirical fit model



(b) Parameter dispersion

Figure 16.2: Empirical model of the clear gate threshold voltage shift and the resulting parameter dispersion

threshold voltage shift which shows a less pronounced saturation behavior than the clear gate.

16.3 Impact on system performance

The previous section analyzed the dispersion of the operation parameters under inhomogeneous irradiation. This section gives an answer to the question:

What is the impact on the system performance, namely the impact on the internal amplification which determines the signal? The noise of the overall readout chain is dominated by the frontend. This allows directly judging the effect on the SNR.

In general readout schemes, which are robust under changes of the operation parameters, are preferable. Thus variations in the operation parameters have only limited impact on the system performance.

16.3.1 Gate

The impact of parameter dispersions on the gate could be directly evaluated using the results from chapter 9. The dependence of the internal amplification on the gate source voltage is depicted in figure 16.4.

The observed dependence shows a saturation behavior for high gate source voltages. As pointed out in section 9.3.2 this behavior could be related to a mobility reduction and a reduction of the influence efficiency.

In presence of inhomogeneous radiation the saturation is beneficial. By operating the detector at moderate high gate source voltage the sensitivity to parameter dispersions is reduced. A direct measure of the sensitivity is the slope of the curve.

Assuming an operating point of U_{gs}=5V ($I_{ds} = 120\mu$A a dispersion of 1.8V leads to a decrease of the amplification of 10%. A further increase of the current could improve the robustness even more. Thus a tradeoff between power consumption and robustness against inhomogeneous radiation could be performed.

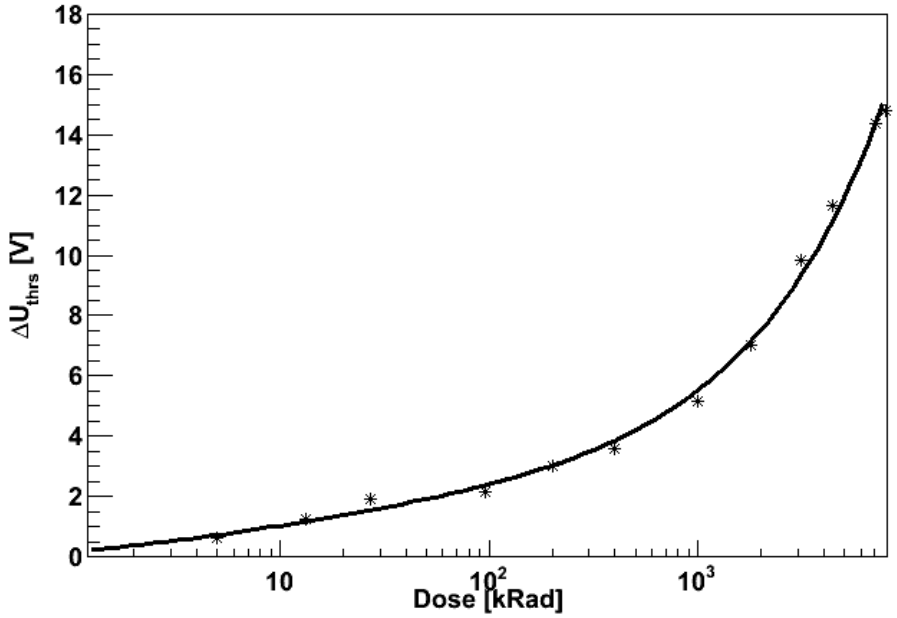
Even if the dispersion has minor impact on the amplification it has strong impact on the variation of the pedestal currents.

16.3.2 Clocked clear gate operation

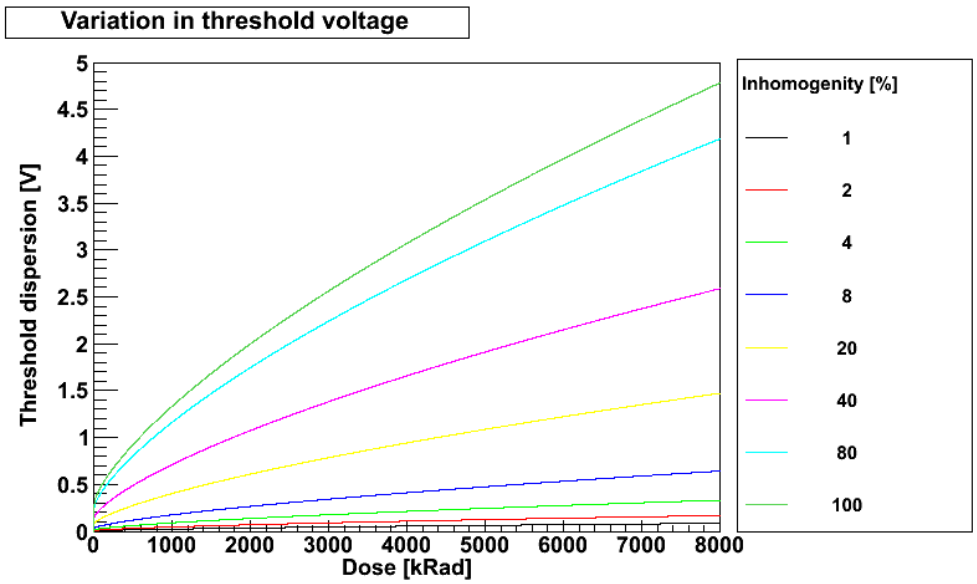
The impact of inhomogeneities on the clear gate is studied separately for the clocked clear gate and common clear gate operation. The clocked clear gate operation has the advantage of offering an additional parameter for optimization.

Even if the clocked clear gate is not foreseen as possibility for the ILC vertex detector it is of interest since the capacitive coupled clear gate, see chapter 12, exhibits the same behavior with respect to the clear low value.

In internal amplification was studied in dependence of the clear gate low value. The result is depicted in 16.5a. On the first sight the results are very



(a) Empirical fit model



(b) Parameter dispersion

Figure 16.3: Empirical model of the threshold voltage shift on the gate and the resulting parameter dispersion

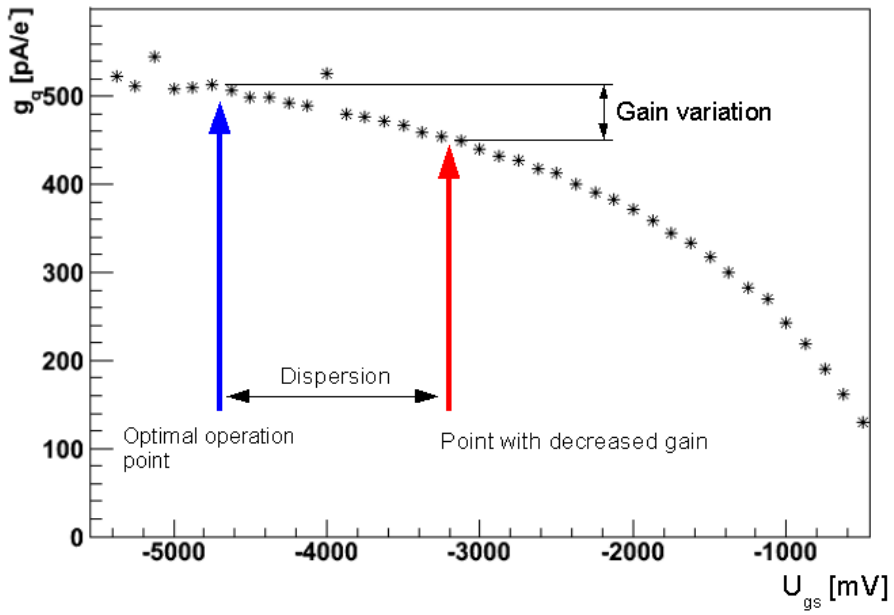


Figure 16.4: Dependence of the internal amplification on the gate source voltage, PXD5 standard matrix, $I_{ds} \approx 125\mu A$ at -5V. The impact of an inhomogeneous irradiation is indicated by the arrows and the resulting variation of the gain.

promising the internal amplification is stable over a range of more than 3V. Thus inhomogeneities leading to a dispersion of the operation parameter will have no impact on the system performance!

However a closer look to region below a clear gate value of -3V shows that the onset of the parasitic clear gate transistor leads to a significant increase of the intrinsic noise of the DEPFET. The ENC is depicted in figure 16.5b. This behavior will be even more pronounced with longer matrices where the parasitic current will be even higher.

16.3.3 Common clear gate operation

The common clear gate configuration the situation is more difficult since the proper setting for the clear gate are a tradeoff between a high internal amplification and a good clear performance. This leads to the situation that the detector is operated on an unstable optimum.

A slice for various clear high settings is depicted in figure 16.6. The unstable optima are clearly visible. However the situation improves with higher clear high values. Thus for 20V clear high - accessible with the switcher 4/5 see section 7.3 - the situation will be similar to the clocked clear gate operation.

16.4 Discussion

The chapter showed that inhomogeneous irradiation is likely and an analysis of the impact of inhomogeneous irradiation is necessary.

The problem related to inhomogeneous radiation is variation of the optimal parameter settings of the DEPFET over an zone which has to be operated with a fixed set of voltages i.e. at least the area operated by a single switcher ASIC.

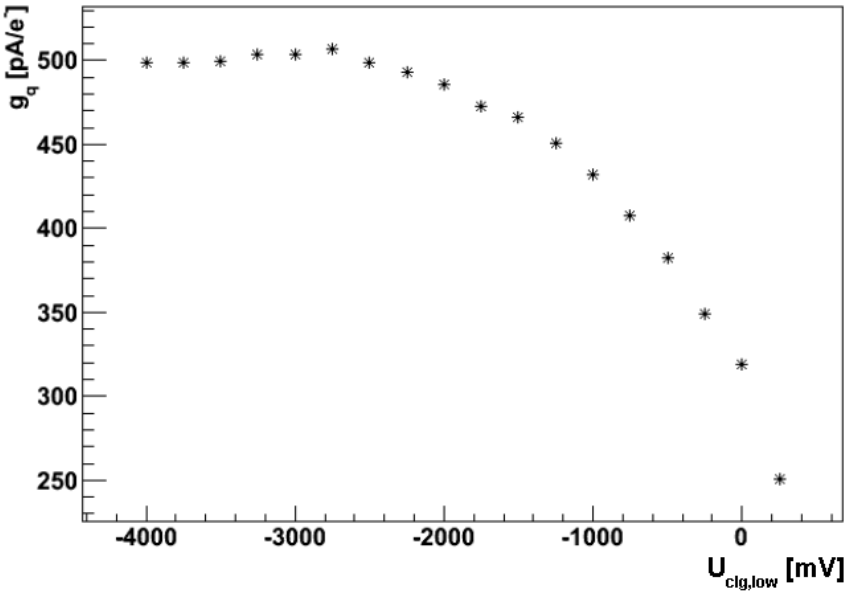
The variation of the operating points of the gate and clear gate was calculated using the performed irradiations from chapter 15. This analysis showed that the dispersion is below 1.5V for both gate and clear gate at an level of 100% in homogeneity and a dose below 1MRad (250kRad plus safety factor of 4).

For the vertex detector layers 2-5 the situation is significantly better. The doses are expected to be smaller, see figure 3.5 on page 24. Thus both the threshold voltage shift and the possible dispersion are limited.

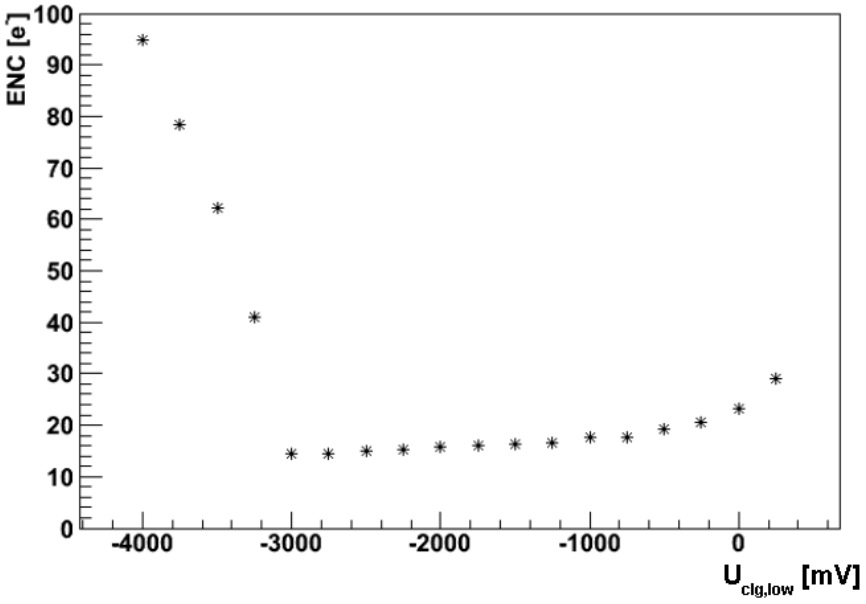
The impact of the internal amplification was studied using the current standard matrices from the PXD 5 production with 6 micron gate length.

The gate was behaves quite robust under variations of the threshold, since the internal amplification shows a saturation. The situation on the clear gate is more complex because gain is strongly depended on the available clear high voltage and clear gate setting.

Clear high level $\approx$ 20 V A robust situation is achieved when a clear high level of 20V could be applied. In this case the clear gate setting could be set



(a) Internal amplification vs. clear gate low



(b) ENC vs. clear gate low

Figure 16.5: Internal amplification and ENC vs. clear gate low in clocked clear gate operation; Clear (low/high) 15V/3.3V, Clear gate high 0.25V, Gate On -4.6V

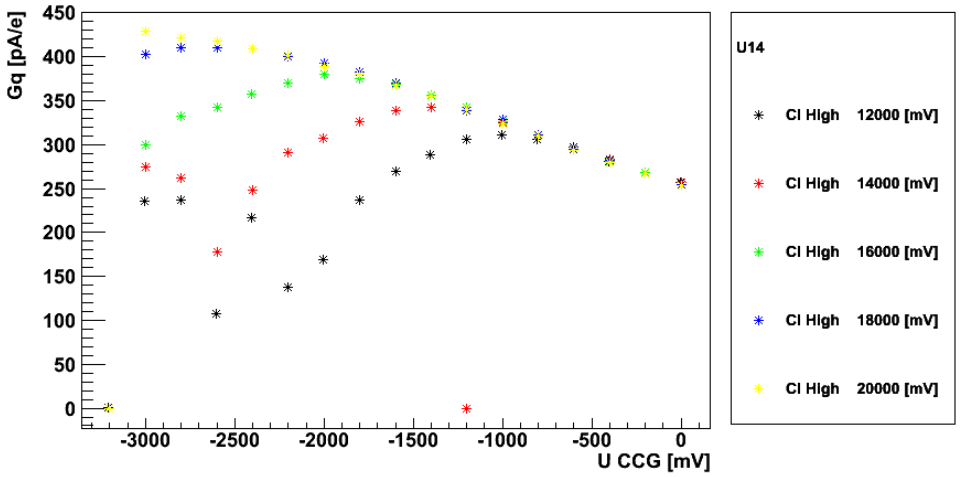


Figure 16.6: Slice through figure 11.4a , showing that the common clear gate operation exhibits an unstable optimum

in a way where the change of the gain is small with respect to changes of the voltage.

The Switcher 5 will allow access this parameter space.

Clear high level ≈ 10 V At moderate clear high level of 10V like accessible with the Switcher 3 the situation more difficult. The common clear gate configuration shows a fast drop off of the gain.

Chapter 17

Improving the intrinsic radiation hardness

The previous chapters showed that the DEPFET is working even after 8MRad ionizing dose. It is also possible to operate the DEPFET in an environment where inhomogeneous irradiation is present. However strong inhomogeneous irradiation along the $r - \phi$ direction will lead to a significant decrease of the performance.

Thus it would be advantageous to improve the intrinsic radiation hardness of the DEFPET detector. A first step towards an improved radiation hardness was done in [87]. Thinner oxides in combination with silicon nitride layer showed a significant smaller threshold voltage shift.

The reason for the improvement could be found in the nitride layer: the nitride provides trapping centers for electrons vice versa to the oxide; thus compensating the buildup of positive space charge in the oxide.

The flat band voltage shift[1] for an oxide of 85nm thickness with a nitride layer of 10nm is depicted in figure 17.1.

The shift is limited to 2.4V even at 10MRad. Thus a significant improvement of the threshold voltage shift is achieved. Moreover the combination of oxide/nitride was not subject to an optimization. This means that further improvements could be expected.

However the thinner oxides will reduce the internal amplification by 40, which make it necessary to improve the gain by means of smaller gate length, which requires technological improvements.

[1]The flat band voltage is a measure for the impact of space charge in the oxide of MOS structures. It is the equivalent of the threshold voltage shift of MOSFET´s

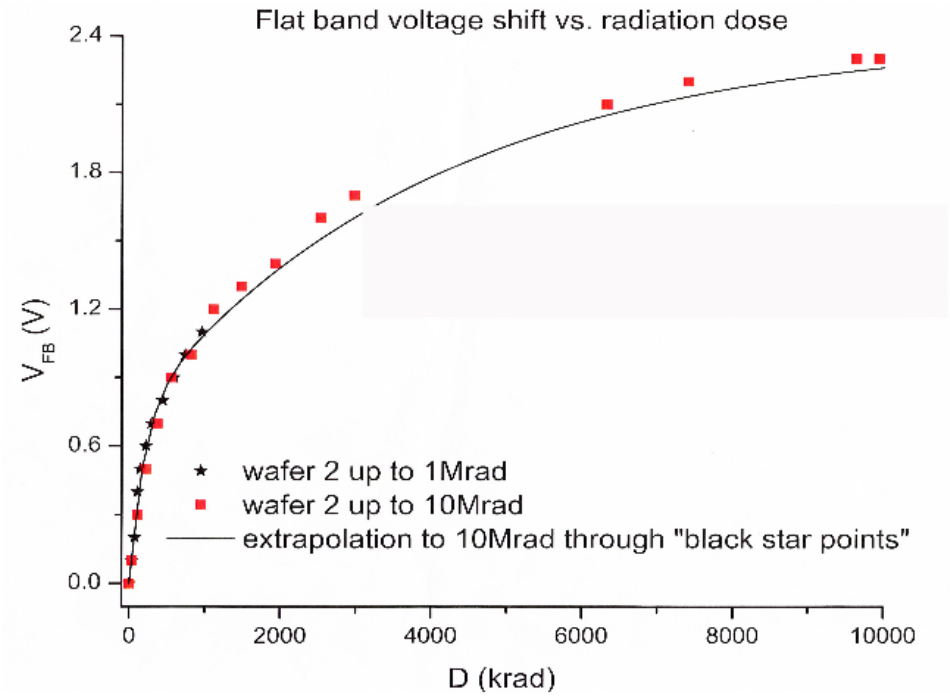


Figure 17.1: Flat band voltage shift for MOS capacitors versus the dose for an oxide/nitride thickness of 85nm/10nm [86]

Part III

Readout concepts

Chapter 18

Readout Concepts

As pointed out in chapter 3.3 the timing requirements as stated in the TESLA technical design report [18]are revisited leading to a significant faster readout.

An evident measure to increase the speed is the change of the readout direction. In the first layer this leads to an increase of a factor 4 and in the outer layers a factor 5.6 could be achieved. The drawback of this approach is the significant increase of the size of the balconies [1] of the modules - the frontend and data handling processor are moved from the end of the barrels into them. This means also that the dominant source of power dissipation is moved into the barrel region instead of the end.

The change of the readout direction means a significant change of the detector concept. Furthermore significant complications emerge when going this way.

Thus the question arises: Are there further methods to increase the readout speed of the detector?

The sections give an introduction of the currently used and two alternative readout schemes:

- Correlated double sampling
- Single sample
- Integration mode

18.1 CDS

The correlated double sampling (CDS) currently is the standard method for readout. The CDS provides an efficient suppression of the low frequency noise. Furthermore the direct subtraction of the current before and after the clear provides an efficient way to reduce the demands on the dynamic range of the frontend. The subtraction immediately removes the pedestal currents and limits the remaining signal to a minimum.

Figure 18.1 shows a pixel wise view of the CDS.

[1] The balconies are the inactive edges of sensor. They are used to place the ASICs

Readout time However the correlated double sampling has the drawback that the frame time T_{frame} is limited by the finite sampling time and the time to perform a clear. The frame time for CDS is given by:

$$T_{frame} = n_{row} \left(2T_{sample} + T_{clear}\right) \tag{18.1}$$

Sensitivity to clear performance Furthermore the signal derived by the difference of two samples

$$I_{signal} = I_{sample1} - I_{sample2} \tag{18.2}$$

is sensitive to incomplete clear.

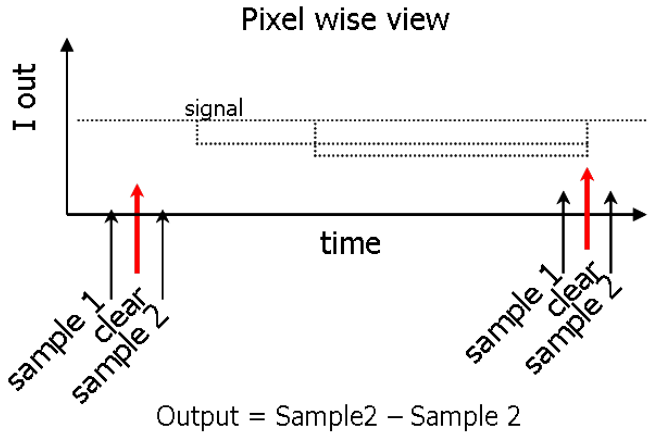


Figure 18.1: Correlated double sampling

18.2 Single sample

The idea of the single sample scheme is depicted in figure 18.2.

Readout time This scheme improves the readout time since only one settling time is required for the readout. The frame time is given by

$$T_{frame} = n_{row} \left(T_{sample} + T_{clear}\right). \tag{18.3}$$

Assuming equal sample and clear time, an improvement of 30% is achieved compard to CDS.

However already the pedestal subtraction poses a first problem: Since the second sample is not available a fixed pedestal must be used. Thus the signal current could be derived as

$$I_{signal} = I_{sample1} - I_{Pedestal}. \tag{18.4}$$

Sensitivity to clear performance The sensitivity for an incomplete clear is limited on the first sight. However remaining charge can be detected in the following frame. This may lead to additional hits. In this case it is also necessary to assure a full clear to achieve stable baseline.

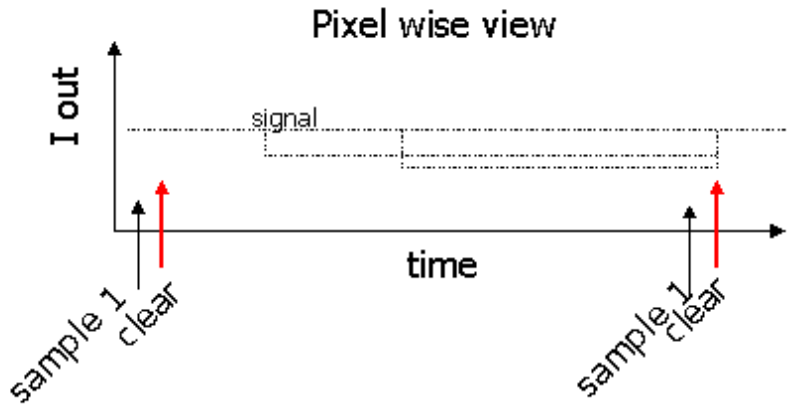


Figure 18.2: Single sample scheme

18.3 Integration mode

The idea of the integration mode is shown in figure 18.3. The signal is integrated over a complete bunch train without a clear in between. The time resolution is achieved by consecutive measurements of the fill level of each pixel.

The integration mode offers the largest improvement of the frame time:

$$T_{frame} = n_{row} T_{sample} \tag{18.5}$$

The time resolution and the signal is derived by

$$I_{signal} = I_n - I_{n-1} \tag{18.6}$$

the difference of two samples.

Sensitivity to clear performance The integration mode is not sensitive to an incomplete clear, since the clear is performed outside the bunch train. In addition this scheme does not rely on fast switcher chips for the clear anymore.

Both clear and clear gate could be clocked with the moderate frequency of 5Hz - the repetition frequency of the accelerator.

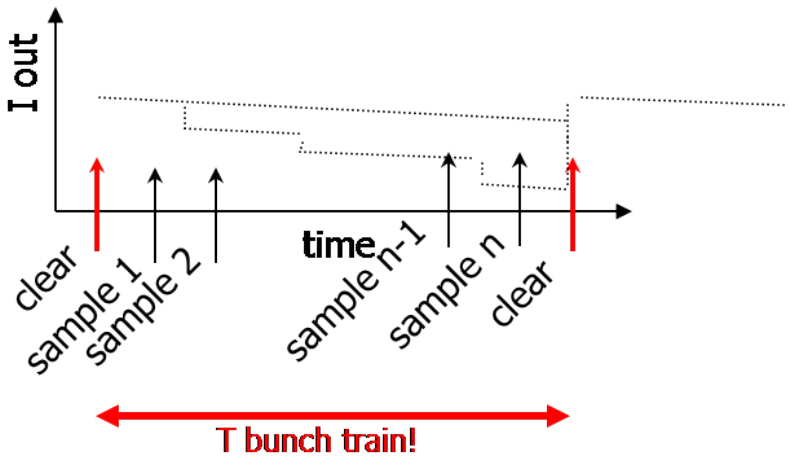


Figure 18.3: Integration mode

Chapter 19

Integration Mode

The "integration mode" scheme is the most promising with respect to the ILC operation conditions - it fully exploits the ILC timing scheme.

This chapter discusses the various issues related to the this concept namely:

- 1/f noise
- shot noise
- charge handling capacity
- clear performance

However this and the single sample scheme also poses the highest demands with respect to uniformity to the detector. Variations of the current due to radiation or intrinsic ones have direct impact on the requirements for the frontend.

19.1 Dynamic range of the DEPFET

The integration scheme requires that the internal gate of the DEPFET accommodates the hole singnal and leakage current of a bunch train.

19.1.1 Signal due to hits

Average number of hits The dominant source of hits are the electron positron pairs created by beamstrahlung. The number of hits per bunch crossing and layer is depicted in 19.1b. The average number of hits per pixel and bunch train is shown in figure 19.1a - numbers from 3.2 on page 18. The calculation assumed an average multiplicity of 4.

Statistical distribution Even if the average rate per pixel and bunch train is small there is still a finite probability that more hits have to be accommodated in a pixel. The underlying distribution is the Poisson distribution. The probability to have N hits in a pixel at an average rate of λ is given by

$$P(N, \lambda) = \frac{\lambda^N e^{-\lambda}}{k!}. \tag{19.1}$$

The probability to have a certain number of hits per pixel and train is shown in figure 19.2a.

The readout scheme should not degrade the efficiency of the hit detection, due to overflow. Figure 19.2b shows that 99.99% of all trains lead to less or equal 4 hits per pixel in the inner layer.

Thus the charge of 4 hits could be regarded as a conservative estimate for the maximal expected signal. Since each hit deposits around 4000 electrons around 16000e^- must be accommodated in the internal gate.

19.1.2 Leakage current

A second contribution to the charge which has to be accommodated is the leakage current. The expected charge from leakage current for various temperatures and integration times is depicted in figure 19.3. The leakage current after irradiation was taken from chapter 14.1.

Before irradiation the leakage current does not contribute to the dynamic range. However after an irradiation of 5 years ILC operation the contribution is as high as 3000 electrons at room temperature.

Requirement Taking into account the charge due to leakage current and hits - 19ke^- - the DEPFET will be able to accommodate all charge generated by hits and leakage current even after irradiation. The charge handling capacity of the DEPFET is measured in chapter 10. With reasonable clear gate setting 50ke^- could be stored in the internal gate. Thus the DEPFET is able to be used in the integration mode in the ILC environment.

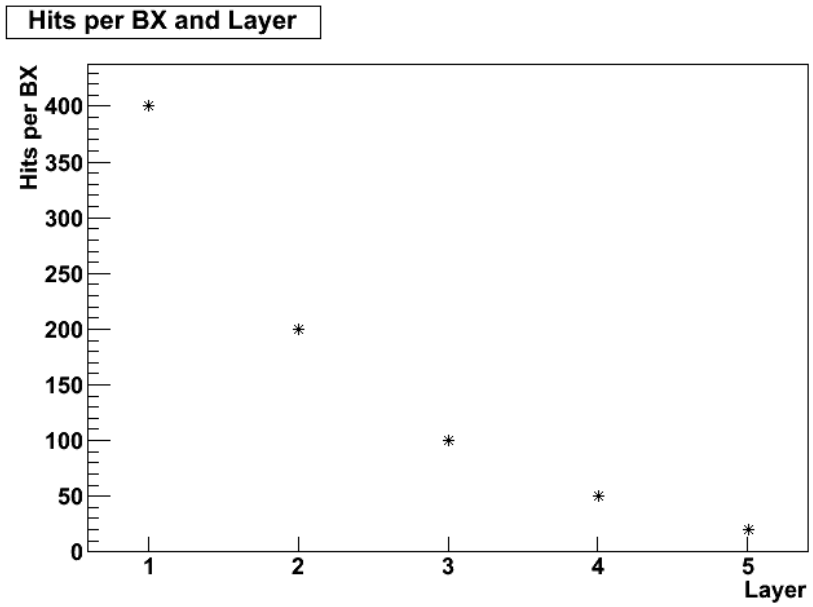
19.2 Impact on noise

This section studies the impact of the integration schemes with respect to:

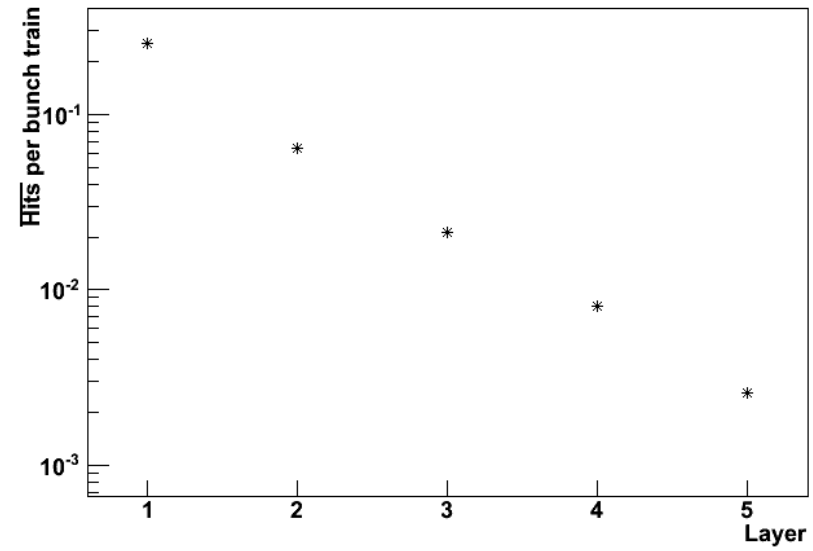
- white noise
- shot noise
- 1/f noise

White noise The contribution of white noise could be directly judged using equation 6.17. Evidently it does not matter for the white noise if two consecutive samples are taken with 50ns of 50μs in between. Thus the contribution of white noise does not change compared to standard CDS.

Low frequency noise However the low frequency noise is increased when going towards longer time differences. To estimate this effect the low frequency noise was calculated numerically using equation 6.18. The results are depicted in figure 19.4. The graph shows an approximately logarithmic dependence, thus

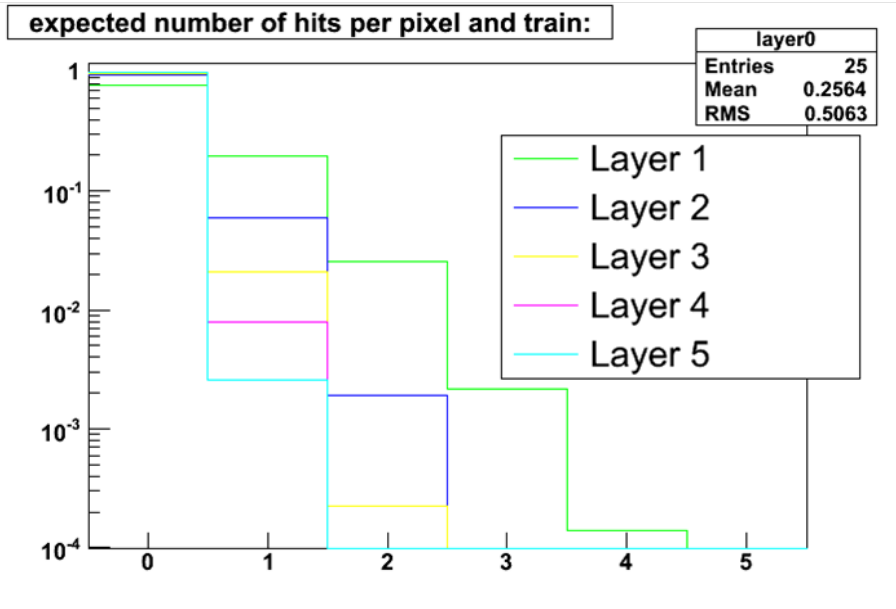


(a) Hits per bunch crossing and layer

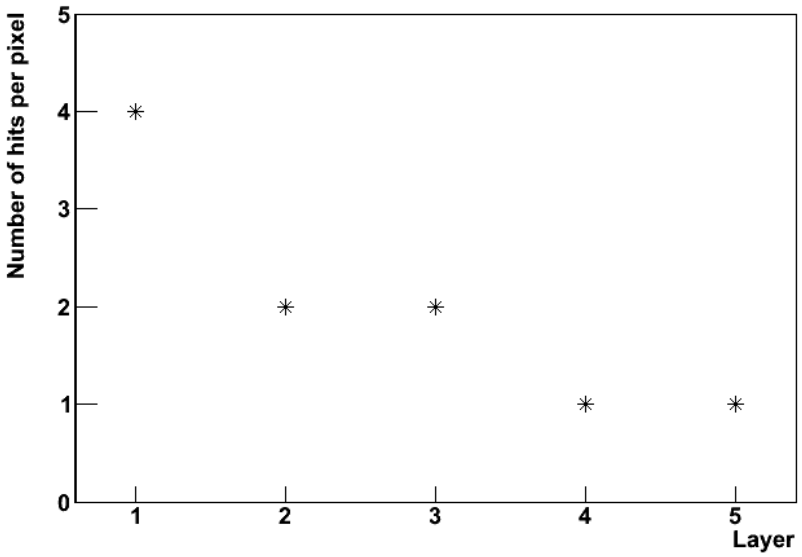


(b) Average number of hits per pixel and bunch train

Figure 19.1: Number of hits per bunch crossing and layer and the resulting average number of hits per bunch train and pixel



(a) Distribution of hits



(b)

Figure 19.2: Statistical distribution of hits

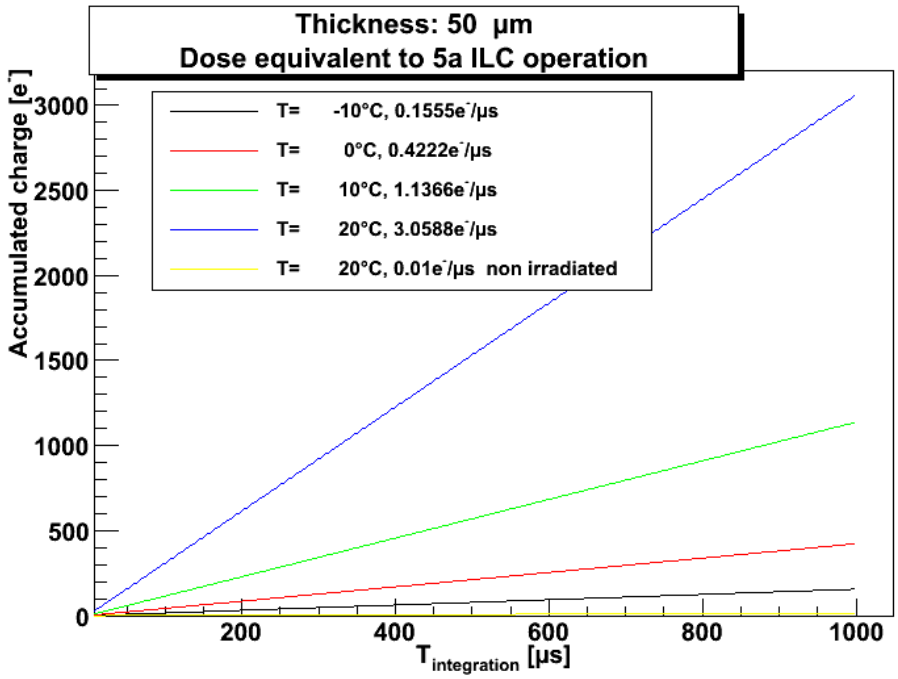


Figure 19.3: Contribution of leakage current to the dynamic range after 5 years ILC operation for various temperatures

the increase of 1/f noise from 20ns towards 50μs is limited. The noise increases from 0.9nA towards 1.7nA. Assuming a gain of 500pA/e$^-$ the contribution is negligible.

Shot noise On the first sight one may expect that the shot noise increases since the leakage current is integrated over the whole bunch train. This is only true when single samples are investigated.

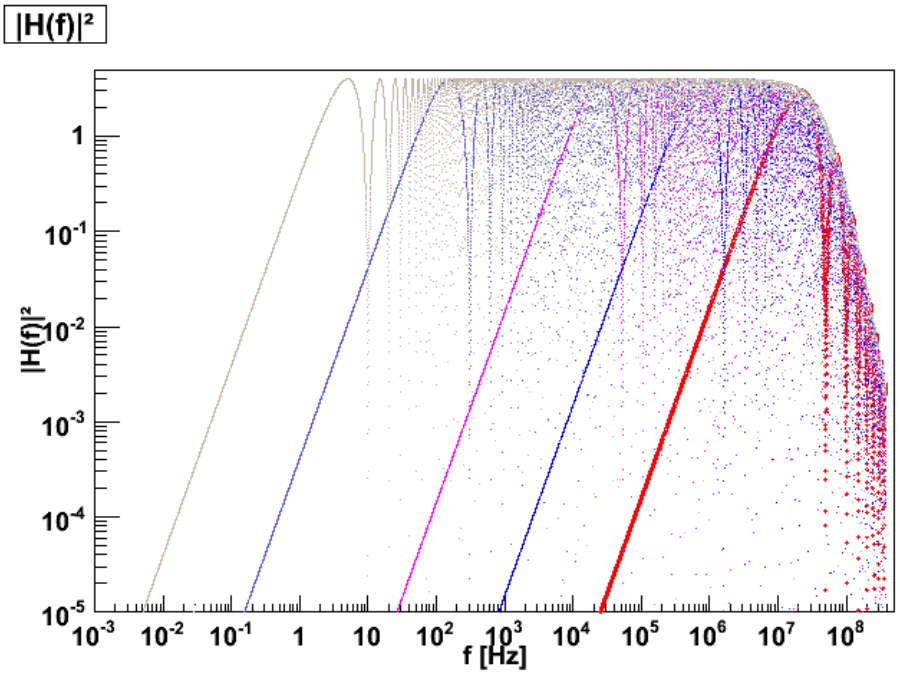
By performing the difference of two consecutive samples the shot noise contribution is only due to the leakage current which was integrated between these samples. The leakage integrated until the first sample acts as a fixed offset which is canceled by the difference.

This shows that the conclusions drawn in section 8.1 and 14 are also valid for the integration mode scheme.

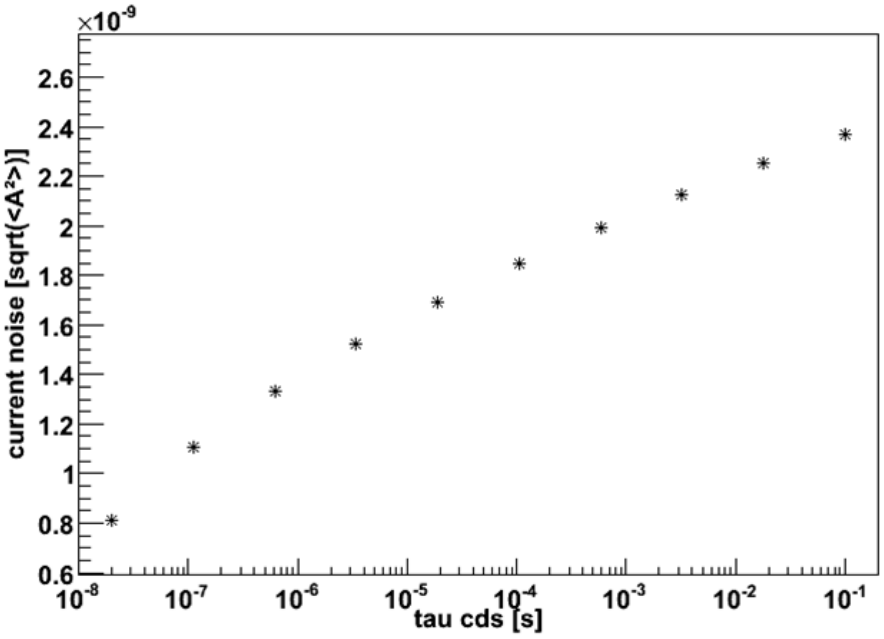
19.3 Impact on clear performance

The integration mode has the advantage that the clear could performed outside the bunch train. This allows to

- perform a common clear to the hole matrix and
- does not rely on dedicated switcher circuits.



(a) Response function CDS



(b) 1/f noise

Figure 19.4: Response of correlated double sampling for various CDS times and the 1/f noise contribution versus the CDS time. The bandwidth limit is fixed with a 60MHz second order low pass.

By performing the clear outside the bunch train it is not necessary to apply a clear pulse to a separate row. Thus a common clear could be applied to the whole matrix. Furthermore the timing requirements are relaxed since the inactive phase of the accelerator is 200ms.

System complexity The integration mode allows reducing the system complexity with respect to the number of switching ASICs significantly. The clear switcher is not necessary any more. This allows a higher fill factor - more active area.

19.4 Impact on frontend

The previous analysis showed that the integration mode is feasible with respect to the intrinsic properties of the DEPFET. However a final decision is only possible by incorporating the frontend into the analysis. Since all performance goals of the vertex detector including power consumption must be met.

An important input parameter for the frontend is the dynamic range. Since the separate samples must be stored at least over one frame time it is reasonable to assume that the samples are directly digitized. Moreover this allows exploiting the improvements in digital circuitry: smaller feature sizes allow building faster circuitry into a smaller footprint.

However one can show that analog to digital converter are governed by the following scaling law:

$$\frac{Speed\ Precision^2}{Power} = \frac{1}{A^2 C_{ox}} [83]. \tag{19.2}$$

A is a technology depended constant. At a given speed - required from the frame time - an increased precision must be compensated by a significant increase of power consumption.

This shows that the required dynamic range is an important quantity for the readout scheme.

Table 19.1 shows a summary of the required dynamic range of the frontend, assuming a gain of 500pA/e$^-$. The number of his per bunch train are estimated in section 19.1. The common mode was estimated using the current common mode with an safety factor of 4. The pedestals variations were measured to 10% [65] assuming a current of 100μA.

The overall SNR must be kept in the same range than for the conventional readout (50nA). Thus a least significant bit (LSB) of 50nA would add a negligible amount of digitization noise (LSB/$\sqrt{12}$). This shows that an effective number of 9 Bits is sufficient to cover the signals from the integration mode readout scheme.

	$I[\mu A]$
Signal current to house 99.99% of the bunchtrains	8
Common mode	0.5
Leakage current	1.5
Pedestal variations at $I_{ds} = 100\mu A$	10
Sum:	20

Table 19.1: Dynamic range for the frontend in the integration mode readout scheme

19.5 Experimental validation

Sequence Figure 19.5a shows the used timing for the demonstration for the integration mode readout concept. The length of the integration phase is set to 1ms. The green pulses indicate the sampling strobes - the points where the ADC samples.

Spectroscopic measurement The previously described sequence was used to perform a spectroscopic measurement. The spectrum derived from consecutive samples is depicted in figure 19.5b. The spectroscopic performance with an ENC of 12.8e^- in the noise peak is even better than in conventional CDS. This could be attributed to the fact that no distortions due to the clear process are present.

19.6 Summary

The investigations show that the integration mode allows to to increase the speed by 60% compared to the standard correlated double sampling.

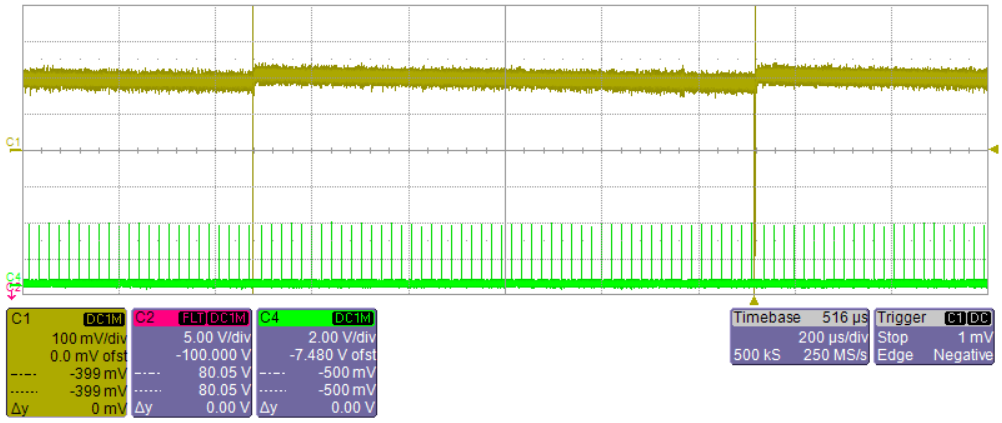
The capacity of the internal gate is able to house all hits during a bunch train and the leakage current without a significant increase of inefficiency.

The increase of the low frequency noise due to the increased time between two samples in a pixel is shown to be lower than 2nA which is equivalent to 4e^- at gain of 500pA/e^- . Moreover the contributions of white noise and shot noise are not increased compared to CDS.

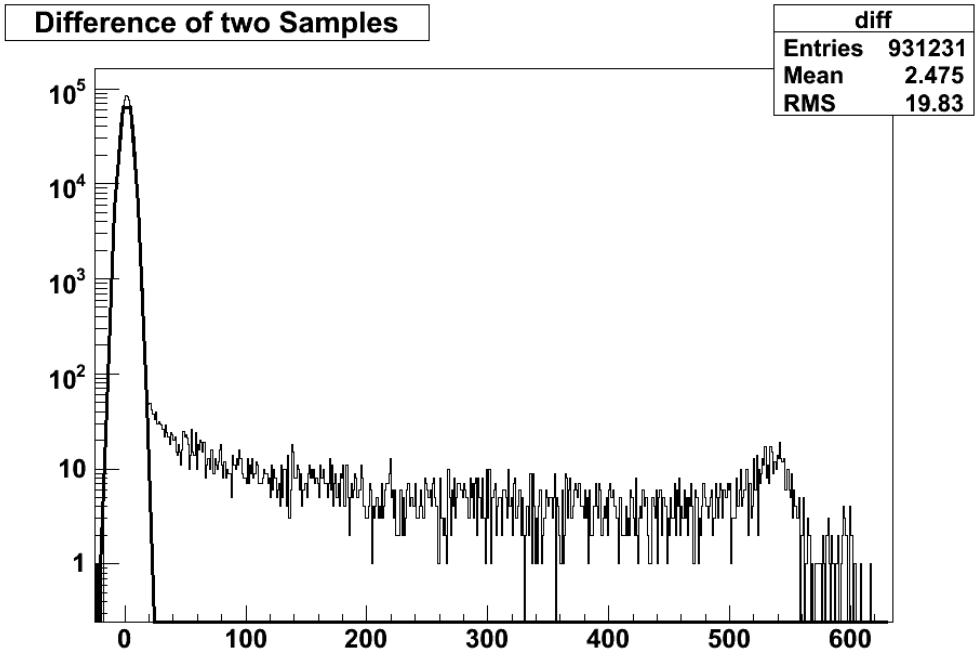
The integration mode will allow to fully utilize the performance of the DEPFET with respect to the clear process and internal amplification. Since the clear process will be in the inactive phase of the accelerator, which allows to use the clocked clear gate configuration for the clear. The clear gate setting in the integration phase could be set in a way that an optimal internal amplification is achieved, compare to chapter 11.

Thus from the DEPFET point of view the integration mode is working.

However integration mode sets new requirements to the fronted circuitry. It is shown that effective 9Bits are needed to digitize the signal currents of the matrix - 1 Bit more than the DCD.



(a) Sequence



(b) Fe^{55} spectra

Figure 19.5: Demonstration of the integration mode: (a) used sequence with 1ms integration time, sampling strobes in green (b) resulting Fe^{55} spectrum from the differences of two consecutive sampling strobes

A final decision of the feasibility will be possible when the impact on the frontend is investigated.

Chapter 20

Summary and outlook

The conducted research was focused on the properties of the DEPFET with respect to the requirements of the vertex detector at the International Linear Collider.

The vertex detector will incorporate an unprecedented combination of granularity and speed. To reach the ambitions performance goals a broad set of examinations has been performed.

Noise and internal amplification The material budget of 0.1% X_0 in the barrel region limits the active volume which generates signal.

A direct measurement of the noise contribution of the DEPFET showed that an equivalent noise charge below $50e^-$ could be expected at the required speed. This shows that the DEPFET could be regarded as low noise device.

Low noise operation is not a sufficient criterion to achieve a high SNR for good spatial resolution and efficiency. The signal generated from the DEPFET is determined by the internal amplification. Currently used standard matrices exhibit a gain of 300-350pA/e^-.

Investigations on test structures showed that an internal amplification of up to 1.4nA/e^- is possible. Moreover the empirical dependence of the gain was compared to a theoretical model. The found deviations could be attributed to a decrease of the mobility and a increase of the parasitic capacitance toward neighbouring electrodes.

Nevertheless a significant improvement of the overall system performance could be expected from an increased gain.

Clear performance Another important issue related to the operation of DEPFET detectors is the clear performance. A novel method to judge the clear performance was developed within this thesis - the comparison method. The systematic investigations showed that it is possible to achieve a full clear with a voltage swing below 10V.

In addition the measurements revealed a new feature: a modulation of the internal amplification with the clear gate voltage. This is reason why similar pixel layouts operated with the single pixel setup or with the DEPFET system

(CURO and Switcher 2) show an amplification of up to 500pA/e^- and 300-350pA/e^- respectively.

Since the new Switcher 4 and 5 will have a significant increased range of at least 20V, it will be possible to operate the matrices at clear gate voltages allowing to fully exploit internal amplification.

Capacitive coupled clear gate The capacitive coupled clear gate (CCCG) is a new Clear scheme which allows combining the advantages of a clocked clear gate operation with the simplicity of the common clear gate operation.

The CCCG was investigated twofold: a dedicated test structure allowed a direct measurement of couplings and on a $64 \cdot 128$ pixel matrix.

The analysis shows that the coupling of the clear gate on the gate is within the expectations. However also a strong parasitic coupling on the gate was found, which limits voltage swing on the clear gate.

Nevertheless the CCCG matrix showed a superior performance with respect to the internal amplification and noise. The internal amplification was improved to 470pA/e^- - the highest measured with a system based on the CURO and Switcher 2. The lower noise allowed the detection of Fe^{55} for the first time.

Radiation hardness Even if lepton colliders are expected to show low backgrounds compared to hadron collider, the vertex detector at the ILC will be exposed to a non negligible amount of ionizing and non ionizing radiation.

The impact of non ionizing radiation was studied using proton and neutron irradiations. The observed leakage currents will allow operating the detector close to room temperature - a result of the fast readout and the small thickness of the detector.

Since the DEPFET is a MOS device it is also susceptible to ionizing radiation which leads to a shift of the operation voltages due to build up of positive space charge in the oxide.

The irradiations performed with low energetic x-rays showed that the DEPFET matrices are still operational after 8MRad, far beyond the ILC requirements. The observed threshold voltage shifts are typically around 15V at 8MRad and around 5V at 1MRad. The extend of the threshold voltage shift requires to adapt the working parameters while operation.

Moreover the irradiations showed that the threshold voltage shift are depending strongly on the biasing conditions of the DEPFET similar to the well known behavior of MOS structures.

Also a first investigation of the impact of inhomogeneous irradiation on the DEPFET has been performed. The results show that the DEPFET is able to withstand moderate inhomogeneities.

Readout concepts The requirements for the readout speed as stated in the TESLA TDR were too optimistic as current investigations showed. An obvious measure to increase the speed of the DEPFET is the change of the readout direction.

Moreover alternative methods to increase the speed exist. The integration mode was investigated with respect to requirements of the ILC vertex detector. The integration mode allows speeding up the frame time by 60% since the conventional sample clear sample cycle is exchanged with a simple sample for each row. The clear is performed outside the bunch train.

It was shown that the DEPFET is able to accumulate all the generated charge generated by hits and leakage current. Moreover the increase of low frequency noise does not compromise the system performance.

From the device point of view the integration mode could be used at ILC.

Nevertheless an opened question is the actual realization of the frontend which must handle an increased dynamic range and must store the data of one entire frame.

Outlook The thesis shows that the DEFPET is an excellent candidate for the ILC vertex detector.

The investigations conducted within this thesis were based on single pixel structures, mini matrices and 64*128 pixel arrays. The final detectors will have a size of about 1024*5120 in the outer layers. Increasing the number of pixels by almost three orders of magnitude compared to the investigated structures.

This increase leads apparently to new questions:

- Yield of the wafer scale devices?
- Parameter dispersions? (pedestal currents, clear performance, internal amplification)

As pointed out the threshold voltage shifts due to ionizing radiation make it necessary to adapt the operation voltages. The performed measurements stimulate measures to improve the intrinsic radiation hardness of the DEPFET to limit the extend of the threshold voltage shift. Investigations performed on MOS structures with thinner dielectrics (oxide and nitride) [87] are very promising.

The usage of thin dielectrics also poses new questions:

- How could one compensate the decrease of the internal amplifications due to the thinner oxides?
- Are technological variations required or is a compensation via the drain source current possible?

Appendix A

List of symbols

Symbol	Meaning
General	
c	Speed of light
β	v/c
γ	Gamma factor $\frac{1}{\sqrt{1-v^2/c^2}}$
p,$\mathbf{p}$	Momentum, bold: momentum vector
L	Luminosity
H_D	Luminosity enhancement factor
X_0	Radiation length
ϵ_0	Dielectric constant
k	Boltzmann constant
Material parameters	
N_D	Donor concentration
ϵ	Specific dielectric constant
E_g	Energy of the band gap (Si 1.12eV)
μ_h	Mobility of holes
Transistor parameters	
U_{gs}	Gate - Source voltage
I_{ds}	Drain - Source current
U_{ds}	Drain - Source voltage
U_{thr}	Threshold voltage
g_m	transconductance of FET
W	Width of the transistor gate
L	Length of the transistor gate
d_{ox}	Thickness of the oxide
C_{ox}	Oxide capacitance $\frac{1}{\epsilon_0\epsilon_{ox}}\frac{WL}{d}$
C'_{ox}	Sheet capacitance $\frac{1}{\epsilon_0\epsilon_{ox}}\frac{1}{d}$
g_q	Internal amplification

Table A.1: List of symbols

Symbol	Meaning
Noise related parameters	
v_n	Voltage noise density
i_n	Current noise density
ENC	Equivalent noise charge
SNR	Signal to noise ratio
ENB	Equivalent noise bandwidth
Radiation damage related	
α	Current related damage constant
Φ	Particle flux density
S	Subthreshold slope
N_{it}	Interface state density
ΔU_{thr}	Threshold voltage shift

Table A.2: List of symbols, continuation

Appendix B

List of investigated structures

Structure	Wafer	Geometry	Performed investigations
J14	PXD4 10 non HE	W = 20, variable L	g_q,g_m,noise at high bandwidth
J14	PXD4 HE	W=20, variable L	g_q, clear performance
M02	PXD4 10 non HE	W = 20, L=6	proton irradiation, g_m, spectroscopic performance, leakage current
M05	PXD4 non HE	W = 20, L=6	neutron irradiation, g_m, spectroscopic performance, leakage current
H01	PXD5 S90	W=10 L=6.4	test beam 2007 pre characterization
F11	PXD5 S90	W=9, variable L	g_q
F12	PXD5 S90	W=15, variable L	g_q
F13	PXD5 S90	W=25, variable L	g_q
U12	PXD5 S90	W=10.8, L=6	g_q, dynamic range, spectroscopic performance
U14	PXD5 S90	W=7.4, L=6	g_q,clear performance
U25	PXD5 S90	W=10.8, L=6	g_q,clear performance, alternative readout concepts
U25	PXD5 90	W=10.8, L=6	X-ray irradiation, U_{thr}, g_m, spectroscopic performance, leakage current
U14	PXD5 90	W=7.4, L=6	X-ray irradiation, U_{thr}, g_m, spectroscopic performance, leakage current, high statistics evaluation
U44	PXD5 91	W=10, L=6	CCCG test structure, couplings
L01	PXD5 91	W=10, L=6	CCCG matrix, optimization, g_q, spectroscopic performance, test beam 2008

Table B.1: List of investigated structures

Appendix C

Derivation of current characteristics

This part gives a short derivation of the current voltage characteristics of p channel MOSFET, since this dependence plays an important role in many discussions carried out in the thesis. The steps required to incorporate the influence of the charge in the internal gate are marked red. The given steps are similar to the derivation in [48] - with one exception - the treatment of the charge in the internal gate from the beginning.

At beginning of strong inversion the potential on the channel Ψ_s related to the distance of the intrinsic level and the Fermi level Ψ_b by

$$\Psi_s = -2\Psi_b$$

To calculate the current flowing through the transistor it is necessary to calculate the charge density at the interface. The surface density could be related to the applied voltage at the gate, the space charge region and the charge influenced by electrons in the internal gate while inversion by

$$Q_C = -\epsilon_{ox}\epsilon_0 E_{ox} + \epsilon_{ox}\epsilon_0 E_s + \frac{Q_{int}}{WL}$$

since the overall device is neutral, with

$$E_s = -\frac{qN_D}{\epsilon_{ox}\epsilon_0} d_{max}$$

$$E_{ox} = \frac{1}{d_{ox}} \left(V_{GS} - V_{FB} - \Psi_c\right)$$

Assuming that the MOS structure is in strong inversion thus a conducting channel is existing and underneath a depletion zone with width d_s is established.

The width of this depletion zone is given by

$$d_s = \sqrt{\frac{2\epsilon\epsilon_0}{qN_a} \left(\phi_s - V_{sub}\right)}$$

The threshold voltage could be derived by the requirement that the charge density is 0 at U_{THR}.

When a current is flowing a voltage drop will occur thus changing the potential in channel like

$$\Psi_s = V_c(y) - 2\Psi_B.$$

Since charge is conserved the current on each point in the channel is constant thus the identity

$$LI_d = \int_L^0 I_d dy \tag{C.1}$$

is evidently true. The relation must hold for ALL the charges in the channel, e.g. a charge sheet with constant density would violate this relation.

$$I_d = -v(y) Q_c(y) W = -\mu_p E_y(y) Q_c(y) W = -W \mu_p Q_c(y) \frac{dV_c E_y(y)}{dy}(y) \tag{C.2}$$

The charge density could be rewritten as

$$Q_c = -\left[C'_{ox}\left(V_G - V_{FB} - \Psi_s + \frac{Q_{int}}{C'_{ox} W L}\right) + \sqrt{\epsilon\epsilon_0 q N_D (V_{sub} - \phi_s)}\right]. \tag{C.3}$$

At this step it becomes evident the simple argument, which leads to the definition of an equivalent change of the gate voltage when a charge is present in the internal gate, is indeed the proper description of the signal generation process.

By introducing the new quantity - the effective gate potential V_{Geff} as

$$V_{G,eff} = V_G + \frac{Q_{int}}{C'_{ox} W L} = V_G + \frac{Q_{int}}{C_{ox}} \tag{C.4}$$

the next steps in the calculation are similar to a conventional FET.

$$I_D = -v(y) Q_c(y) W = -\mu_h E_y(y) Q_c(y) W \tag{C.5}$$

$$= -\mu_h \frac{dV_c}{dy} Q_c(y) W \tag{C.6}$$

$$= \mu_h \frac{dV_c}{dy}\left[C_{ox}(V_{G,eff} - V_{FB} - \Psi_s) + \sqrt{\epsilon\epsilon_0 q N_D (V_{sub} - \phi_s)}\right] \tag{C.7}$$

The steps assuming a constant mobility: a linear dependence of the drift velocity on the electrical field. The last step uses equation C.3. The integration boarders are the drain potential at L=0 and $V_c = 0$ at the pinch off point.

With help of equation C.1 the drain current could be written as

$$
\begin{aligned}
I_d = \frac{1}{L}\int_L^0 I_d dy &= \frac{W}{L}\mu_h \int_{V_c=0}^{V_D} Q_c\left(V_c\right) dV_c \\
&= \frac{W}{L}\mu_h C_{ox} \int_{V_c=0}^{V_D} \{(V_G - V_{FB} - 2\Psi_B - V_c) \\
&\quad + \frac{\sqrt{\epsilon\epsilon_0 q N_D}}{C_{ox}}\sqrt{(V_{sub} + 2\phi_B + V_c)}\Big\} dV_c \\
&= -\frac{W}{L}\mu_h C_{ox}\left\{\left(V_G - V_{FB} + 2\Psi_B - \frac{V_D}{2}\right)V_D\right. \\
&\quad \left. -\frac{2}{3}\frac{\sqrt{\epsilon\epsilon_0 q N_D}}{C_{ox}}\left[(V_{sub} + 2\Phi_B - V_D)^{3/2} - (V_{sub} + 2\Phi_B)^{3/2}\right]\right\}. \quad \text{(C.8)}
\end{aligned}
$$

Determination of the saturation voltage As long as no pinch off occurs - drain and source are connected by a charge sheet - the current will increase linear with the drain source voltage. This is called linear regions.

When the pinch off occurs - the charge density in the channel is zero close to the drain - a further increase of the drain source voltage will not lead to a increase of the current. The FET is in saturation. This behavior could be understood by the fact that the increase of the lateral electrical field E_y and the decrease of the charge density are compensating each other.

Thus the saturation voltage could be calculated by requiring that the charge density is $Q_c = 0$ and the surface potential is at the onset of strong inversion $\Psi_s = V_D - 2\Psi_B$

$$
\begin{aligned}
V_{D,sat} = V_G - V_{FB} + 2\Psi_B + \\
\frac{1}{C_{ox}^{,2}}\epsilon\epsilon_0 q N_D\left[1 + \sqrt{1 + 2\frac{C_{ox}^{,2}}{\epsilon\epsilon_0 q N_D}\left(V_{sub} - V_G - V_{FB}\right)}\right]. \quad \text{(C.9)}
\end{aligned}
$$

Thus the current in the saturation region is given by:

$$
\begin{aligned}
I_{D,sat} = -\frac{W}{L}\mu_h C_{ox}\left\{\left(V_G - V_{FB} + 2\Psi_B - \frac{V_{D,sat}}{2}\right)V_{D,sat}\right. \\
\left. -\frac{2}{3}\frac{\sqrt{\epsilon\epsilon_0 q N_D}}{C_{ox}}\left[(V_{sub} + 2\Phi_B - V_{D,sat})^{3/2} - (V_{sub} + 2\Phi_B.)^{3/2}\right]\right\}. \quad \text{(C.10)}
\end{aligned}
$$

Simplification Since most of the FET as well as the DEPFET is operated with a constant bulk voltage it is possible to incorporate the bulk effect into the threshold.

Thus leading to:

$$
I_D = \frac{W}{L}\mu_p C_{ox}^{,}\left\{\left(V_G^{,} - V_D\right)V_D\right\} \quad \text{(C.11)}
$$

and

$$V_G^{'} = V_G - V_T = V_G - \left[V_{FB} - 2\Psi_B - \frac{1}{C_{ox}^{'}} \sqrt{2\epsilon\epsilon_0 q N_A \left(V_{sub} + 2\Psi_B \right)} \right] \quad \text{(C.12)}$$

The saturation voltage could be derived similar in a similarly by requiring

$$\frac{\delta I_D}{\delta V_D} = 0, \quad \text{(C.13)}$$

which leads to

$$V_D = V_G^{'} I_{D,sat} = \frac{W}{L} \mu_p C_{ox}^{'} \frac{V_{D,sat}^2}{2} = \frac{W}{L} \mu_p C_{ox}^{'} \frac{V_G^{'2}}{2}.$$

This is the commonly used formula. The impact of charge in the internal gate is incorporated via equation C.4 defining the effective potential applied to the gate.

The small signal parameter g_m and g_q are shown in section 4.3.

Appendix D

Analysis of matrix measurements

Since the analysis of matrix measurements using the 128×64 is used extensively in chapter 12 the algorithm used for it is presented here.

In general the measured signal of pixel $M_{i,j}$ could be parameterized by the following ansatz:

$$M_{(i,j)} = S_{(i,j)} + N\left(\sigma_{(i,j)}, 0\right) + N\left(\sigma_j, 0\right) + Ped_{(i,j)} \tag{D.1}$$

The aim of the analysis is to reveal the signal $S_{(i,j)}$ of each pixel from the measured value. $N(\sigma, 0)$ are normal distributed random numbers with mean value 0 and standard deviation σ with individual values for each pixel or row.

The second term is the individual pixel noise defining the threshold for the detection of a signal. The third term is the common mode noise which is "common" for a whole row and therefore it is possible to correct for it. The last term is the pedestal - an offset - which is assumed to be constant over many frames for each pixel.

If one of these assumptions is not correct due to a slow drift after temperature change for example one has to take this into account and limit the number of frames for the estimation of these values. Since the runs analyzed are quite small only a few minutes algorithms with these adaptive feature are not further investigated.

The analysis has the following steps:

1. Calculating the pedestals for each pixel
2. Calculating the noise for each pixel
3. Performing the pedestal correction
4. Performing common mode (CM) correction
5. Search for seeds
6. Clustering around the seeds

An additional complication is the fact that in many measurements no dark frames, frames without signals, are available. Since signals in the frames would lead to an overestimate of the noise as well of the pedestals thus the analysis has to be prepared for that. Also the common mode correction is quite susceptible to this effect since a hit in a row where the correction is applied induces a strong bias the average value if it is not excluded.

D.0.1 Pedestal and noise calculation

The pedestal is an offset in the measurement of the charge collected in a pixel introduced by offsets in the readout chain or by the DEPFET itself due to leakage currents.

In case dark frames are available the pedestal could be calculated easily since the signal $S_{(i,j)}$ is vanishing and the other two contributions to the measured value are normal distributed with mean 0 thus a averaging over a number of frames is sufficient. The achievable precision in the estimate is proportional to

$$\sigma_{ped} = \sqrt{\frac{\sigma_{noise}^2 + \sigma_{cm}^2}{n}}$$

By using thousand frames to calculate the pedestal the precision is improved by a factor 33 compared to the combined common mode and readout noise.

The actual algorithm uses an average over a certain number of frames as starting point for the calculation

$$Ped\,(i,j)_{initial} = \frac{1}{n}\sum_{k=0}^{k<n} M\,(i,j)_k$$

The first iteration of the noise is done using all measured values a complication is the fact that the common mode has to be corrected in advance thus the pedestals have to be removed

$$M\,(i,j)_{ped} = M\,(i,j) - Ped\,(i,j)_{initial}$$

and on this values the common mode correction has to be applied which is described in the next section. Assuming that the $M\,(i,j)_{ped,cmd}$ are common mode and pedestal corrected measurements.

$$Noise\,(i,j)_{initial} = \sqrt{\frac{1}{n}\sum_{k=0}^{k<n} M\,(i,j)_{ped,cmd,k}^2 - \overline{M\,(i,j)}_{ped,cmd}^2}$$

Taking into account that the number of hits in each frame even with a strong source not exceeds 80 hits thus 320 pixels out of 8000 are hits these estimates are already quite good.

The next iteration is done in a similar way but including a 4σ cut to reject signals.

D.0.2 Common mode correction

The common mode is introduced to the measurement for example by pickup which couples on the gates thus leading to an increase of current in a whole row or in cases where an readout ASIC draws exceptional high current leading to a voltage drop in the ASIC affection all channels similar.

To estimate the common mode it is necessary to use a robust estimator since only 128 pixel in a double row could be used for the estimation. In this case a truncated mean is used to calculate the common mode. Typically between 2 and 4 of the highest measurements are rejected in the calculation. The median would although offer a possibility.

$$CMD\left(j\right) = \sum_{i} M\left(i,j\right)_{ped} \;\; averaging\; over\; 128 - n_{trunc} - lowest\; values$$

In the next step the common mode $CMD\left(j\right)$ is subtracted from the respective row.

$$M\left(i,j\right)_{ped,cmd} = M\left(i,j\right)_{ped} - CMD\left(j\right)$$

D.0.3 Clustering

After the pedestal and the common mode correction is performed the remaining contributions from equation D.1 are

$$S_{(i,j)} + N\left(\sigma_{(i,j)}, 0\right). \tag{D.2}$$

The individual noise of each pixel is not further reducible. So it must be kept as small as possible by design of the detector.

The clustering is done in a twofold way:

1. seed finding
2. clustering around the seeds

Seed finding To distinguish pixels with hits to those without a cut is applied. For the seed finding this cut is typically set to $5 \cdot \sigma_{i,j}$ of the estimated pixel noise.

The cut must high enough that no noise is accepted as hit and as small as possible so that no signal is rejected.

Clustering around the seeds Since the actual signal clusters are larger than one pixel, hits in neigbouring pixels must be added to the seed. The algorithm uses a search area of $3 \cdot 3$ pixels around the seed. This is sufficient for source measurements, for analysis of inclined tracks in test beam this assumption would be wrong.

The clustering around the seed is done with a smaller cut on the noise $3 \cdot \sigma_{i,j}$ to limit the bias on the total signal height.

The total signal of the cluster around the seed pixel (i,j) is thus given by:

$$S_{clu} = \sum_{(k,l)} M\left(k,l\right)_{ped,cmd} \left(k,l\right) \in \left\{ ROI \cap M\left(k,l\right)_{ped,cmd} \geq 3 \cdot \sigma_{i,j} \right\} \quad \text{(D.3)}$$

The region of interest (ROI) is the search area of $3 \cdot 3$ pixels around the seed.

Additional cuts To assure that close by clusters are not merged an additional cut is applied. This is done by the requirement that only clusters are accepted where no further seeds are neighboring to the edge of the search area.

Hot pixels Moreover the analysis revealed that the edge of the matrix (3 pixels) showed an enhanced noise thus the search area was limited on the edge. A cut on the noise of the pixels allows rejecting hot pixel - pixel with an enhanced noise compared to the average.

Bright pixels Bright pixels are pixels with exceptional high or low pedestal values. The analysis allows rejecting these pixels by introducing additional cuts on the pedestal value.

List of Figures

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